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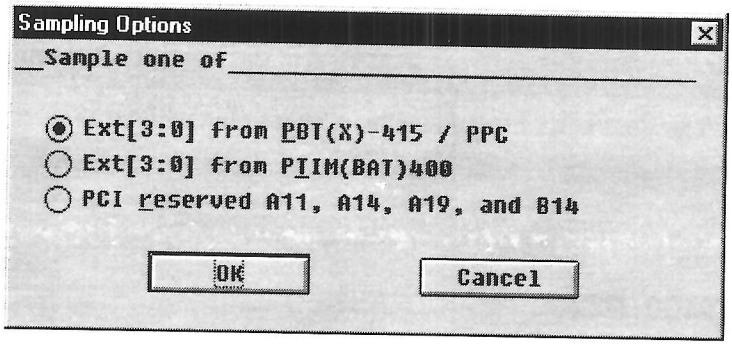


Figure 8.6 The Sampling Options dialog box

Note! The reserved signals A11, A14, A19, and B14. are referring to pin locations on the PCI connector.

8.4 Trace Menu

The `Trace` menu features the run, halt, and display functions for creating and displaying PCI Bus traces for one or more targets.

8.4.1 Run T400_PCI


The "Run" tool bar button

The `Run T400_PCI` command starts the analyzer for the target currently selected. A status dialog box is displayed. See Section 8.4.6 .

8.4.2 Run Multiple


The "Run Multiple" tool bar button

The `Run Multiple` command starts simultaneous operation of all the analyzers present in the actual hardware configuration. For example, both the PBT-415 and the 400MHz Timing Analyzer can run at the same time. A status dialog box is displayed. See Section 8.4.6.

8.4.3 Halt T400_PCI


The "Halt" tool bar button

The `Halt T400_PCI` command halts the current target. Normally the trace acquisition stops by itself when the trace is full, but if a trigger is not found, this command can be useful to halt the acquisition.

8.4.4 Halt All


The "Halt All" tool bar button

The `Halt All` command halts all running targets.

8.4.5 Show T400_PCI


The "Show PCI" tool bar button

The `Show T400_PCI` command displays an alphanumeric trace list from the currently selected T400_PCI target. This list is normally displayed automatically when a trace is full, but if the trace was halted manually this command can be used. The command will also be executed by double clicking in the T400_PCI field on the status line.

8.4.6 Sampling Status

The `Sampling Status` dialog box is displayed during a trace run. It shows which targets are available, and the status of them. In Figure 8.7 the targets are PCI and T400_PCI, whereof the PCI target is not running, and the T400_PCI target is has completed the trace.

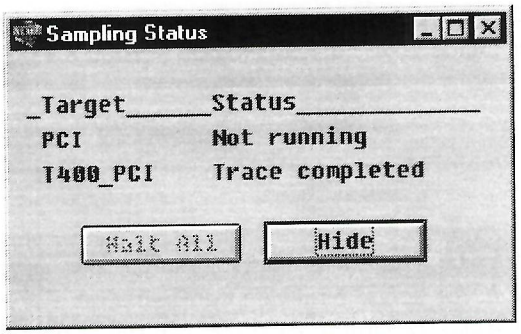


Figure 8.7 The Sampling Status dialog box

8.5 PBAT66 Window - Menu Items


The "PBAT66" tool bar button

When selecting the `Pbat` menu item, or pressing the `Pbat` tool bar button, the PBAT66 Bus Violation window appears with new menu bar items and new tool bar buttons. In addition a new `Pbat` status line appears above the old one. This new status line features direct mouse control of the most important `Pbat` options, i.e. an option is toggled on and off by double clicking with the mouse in the field of the desired option.

8.5.1 Violations Menu

8.5.1.1 Enable


The "Enable" tool bar button

The `Enable` command enables the Anomaly Trigger for screening of the PCI Bus traffic for violations, as explained in Section 6.3.2. The `enable/disable` command is also available at the `Pbat` status line.

8.5.1.2 Disable


The "Disable" tool bar button

The `Disable` command disables the Anomaly Trigger, as explained in Section 6.3.2. The `enable/disable` command is also available at the `Pbat` status line.

8.5.1.3 Clear


The "Clear" tool bar button

The `Clear` command will clear all previously detected violations, and start screening for the next violation.

8.5.1.4 Simulate

The `Simulate` command is only available when running in off-line mode, i.e. when the PC is not connected to the tracer. It runs a simulation of the PBAT66 Bus Violation window.

8.5.2 Mask Menu

When screening the PCI bus for violations, it may be helpful to mask violations that are not important in the working context, i.e. disable the violations that are not of interest, so that the PBAT66 will not trigger on them.

8.5.2.1 Select


The "Select" tool bar button

The `Select` command is used to turn off Black Cockpit mode. See Section 6.3.3.

8.5.2.2 Select All


The "Select All" tool bar button

The `Select All` command enables all the possible violations. See Section 6.3.1.

8.5.2.3 Select None


The "Select None" tool bar button

The `Select None` command disables all possible violations. See Section 6.3.1.

8.5.3 Modes


The "Modes" tool bar button

The `Modes` menu item displays a dialog box where the user may set options for the Anomaly Trigger. Most of the options are also available at the `Pbat` status line at the bottom of the window. All the options are explained thoroughly in Section 6.3.3.

8.6 Setups Menu

8.6.1 Initialize

The `Initialize` command resets the current setup to default values, i.e. all event patterns are reset to "don't care" (x) values, and the Trigger Condition window is reset to sampling in 400MHz timing mode with trigger at Start of Trace when Anything is valid for more than 0 ns.

8.6.2 Load

The `Load Setup` command opens the dialog box in Figure 8.8, which shows a list of all saved setups, in addition to the default setup "Default". Select the desired setup and press the OK button, or double click on it.

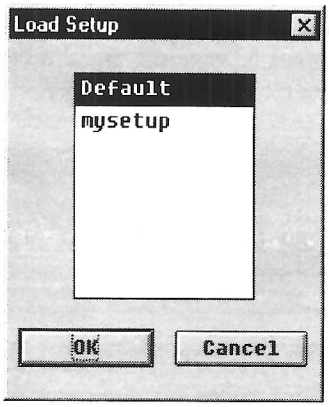


Figure 8.8 The Load Setup dialog box

8.6.3 Store

The `Store` command gives the user the opportunity to store customized setups for use at a later time. Be aware of the fact that all setups will be lost if the Non-Volatile Memory is cleared. See Section 8.7.3.

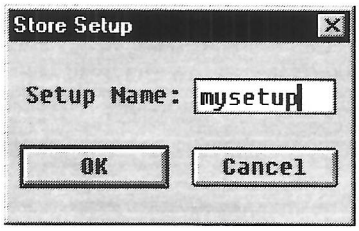


Figure 8.9 The Store Setup dialog box

8.6.4 Delete

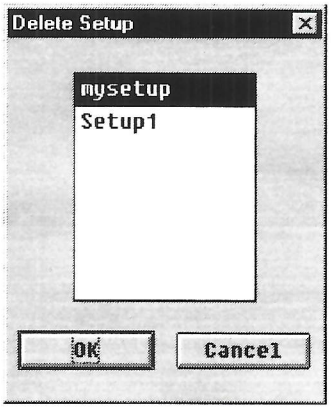


Figure 8.10 The Delete Setup dialog box

The Delete setup command opens the dialog box in Figure 8.10. All setups, except the default setup which cannot be deleted, are shown in the list. Select the setup to be deleted and press the OK button, or double click on it.

8.6.5 Make Current

A setup can not be run if it is not the current setup. (Except when doing Trace/Run Multiple). The Make Current command makes the active setup the current setup.

8.7 Utilities Menu

8.7.1 Communication

The Communication menu controls the communication between the BusView software on the PC and the PBT-415.

8.7.1.1 Connect

The Connect command connects the PC to the PBT-415 according to the settings in the Port Settings dialog box. See Section 8.7.1.3.

8.7.1.2 Disconnect

The Disconnect command disconnects the PC from the PBT-415.

8.7.1.3 Port Settings

The Port Settings command opens the dialog box in Figure 8.11, which allows the user to set the desired port settings for the PBT-415.

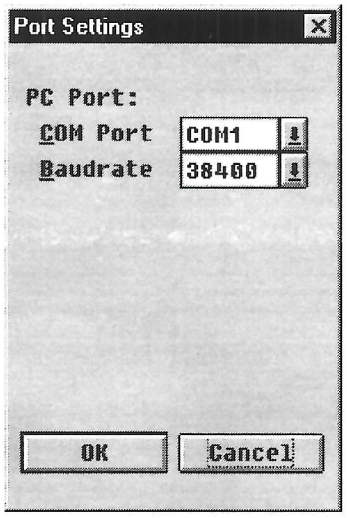


Figure 8.11 The Port Settings dialog box

8.7.2 Update Tracer Firmware

The `Update Tracer Firmware` command opens the dialog box in Figure 8.12, which gives a step by step instruction for how to update the tracer firmware.

Note!

The analyzer is always shipped with all necessary firmware loaded into FLASH PROMs on the board. Reloading of the firmware is only necessary when a new firmware version is issued, or a fatal system error has occurred.

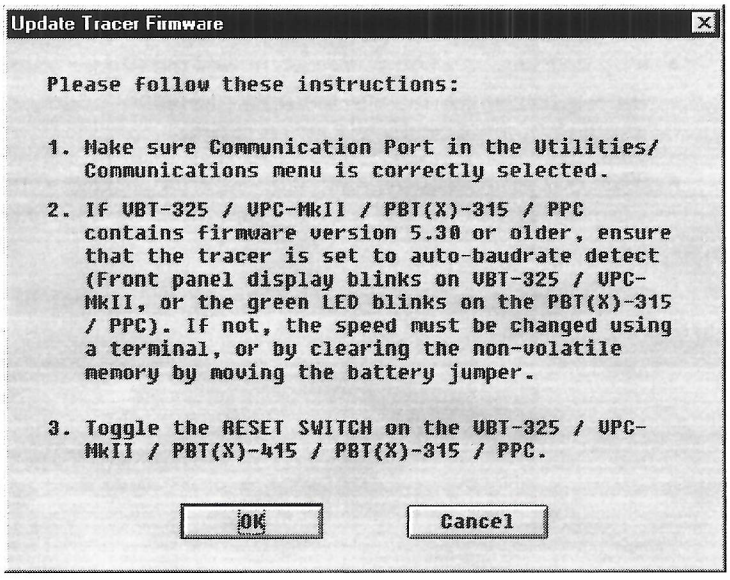


Figure 8.12 The Update Tracer Firmware dialog box

8.7.3 Clear Non Volatile Memory

The `Clear Non-Volatile Memory` command opens the info box in Figure 8.13. Be aware that the tracer will be reset, and that all trace data and setups will be lost.

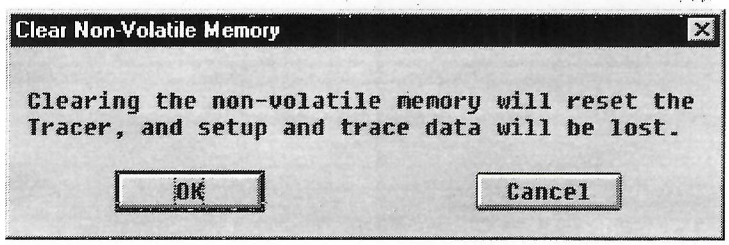


Figure 8.13 The Clear Non-Volatile Memory info box

8.7.4 Trigger Output Options

The `Trigger Output` command opens the dialog box in Figure 8.14, which controls the trigger output on the front panel of the PBT-415.

Trigger source

The `Trigger Source` option controls whether the trigger output should come from the PBT-415, the PBAT66, or the 400MHz Timing Analyzer. If the PBAT or the PTIM are selected the `Mode` and the `Polarity` options are grayed.

Mode

- The `Level on Trigger` option makes the trigger output go active when the trigger sample occurs, and stay active until a new `Trace/Run` is given.
- The `Follow Trigger` option makes the trigger output go active when the trigger sample occurs, but revert to inactive state on the next sample that does not match the trigger condition.
- The `Follow Store` option makes the trigger output go active on samples satisfying the `Store` condition in the current state of the Sequencer.

Polarity

The `Polarity` option decides whether the trigger output signal should be active high or low.

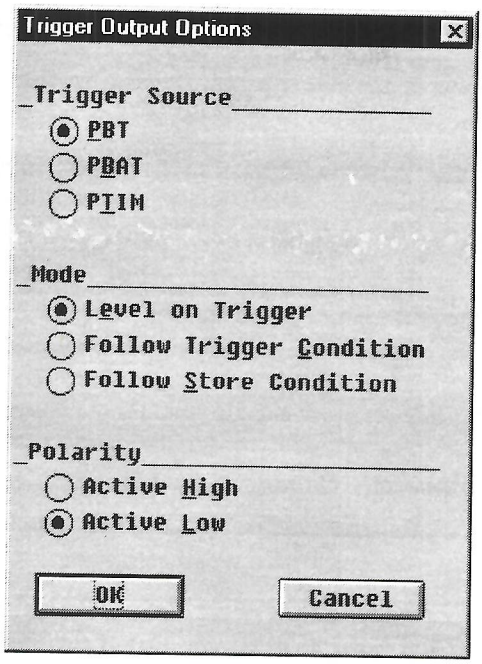


Figure 8.14 The Trigger Output options dialog box

8.7.5 Simulated Hardware

The `Simulated Hardware` command opens a dialog which tells which hardware modules are available for simulating the analyzer. The command is only available when the tracer is off-line.

8.7.6 User Interface Options

Save desktop settings on exit

BusView will start up with the same windows and setups as the last time it was running.

Show percentage completed dialog box when connecting

At start-up BusView loads the tracer status. With this option activated BusView displays an info box showing the percentage of the tracer status that has been loaded.

Show sampling status at trace run

The sampling status dialog box is displayed during trace run when this option is selected. The dialog box continuously displays the current sampling status.

Use simulated LEDs in status line

This is an option selecting whether the status "lamps" at the status line at the bottom of the BusView window should look "three dimensional" or not.

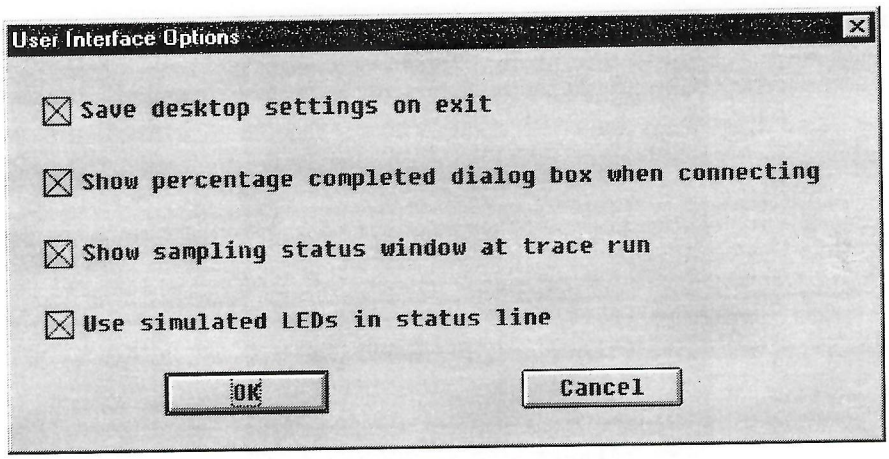


Figure 8.15 The User Interface Options dialog box

8.7.7 Selftest

The `Selftest` command starts an extensive test of the analyzer. The selftest procedure finishes with a reset, causing all trace data to be lost.

8.7.8 Reset Analyzer

The `Reset Analyzer` command resets the analyzer. All trace data will be lost.

8.7.9 Specials

The `Specials` command allows the user to read and set the current ECO (Engineering Change Order) level, PCB revision, and Time and Date. The ECO level is normally set during Manufacturing, and if a hardware ECO upgrade has been performed.

8.8 Window Menu

The `Window` menu contains help for the user to arrange the open windows and icons in the best possible way.

8.8.1 Cascade



The "Cascade" tool bar button

The `Cascade` command arranges all the open windows in a cascade.

8.8.2 Tile Horizontally


The "Tile Horizontally" tool bar button

The `Tile Horizontally` command puts the open windows side by side horizontally.

8.8.3 Tile Vertically


The "Tile Vertically" tool bar button

The `Tile Vertically` command puts the open windows side by side vertically.

8.8.4 Arrange Icons


The "Arrange Icons" tool bar button

The `Arrange Icons` command arranges all the iconized windows at the bottom of the BusView main window.

8.8.5 Alphanumeric List


The "Alphanumeric List" tool bar button

The `Alphanumeric List` command opens an alphanumeric list of the current trace buffer. More than one list can be open at the same time.

8.8.6 Waveform


The "Waveform" tool bar button

The `Waveform` command opens a waveform display of the current trace buffer. More than one waveform display can be open at the same time.

8.8.7 Select Window

The `Select Window` command opens the dialog box in Figure 8.16, where the user can select which window to be displayed in front.

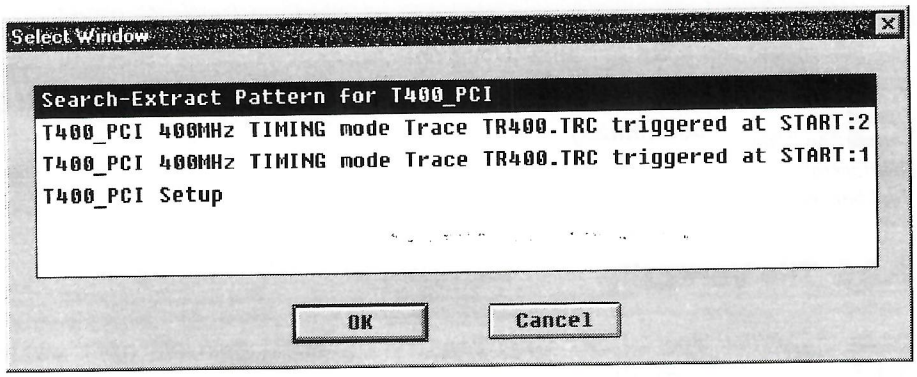


Figure 8.16 The Select Window dialog box

8.9 Help Menu

The `Help` menu contains a full featured On-line Help manual for BusView.

8.9.1 Index


The "Help Index" tool bar button

The `Index` command opens the List of Contents of the Help file.

8.9.2 Topic Search


The "Topic Search" tool bar button

The `Topic Search` command enables a list of Help items where the user can search for a desired item.

8.9.3 Context Help


The "Context Help" tool bar button

The `Context Help` command is only available in the PBAT66 window, and is used to give a detailed explanation to the selected violation. Mark a violation and select Context Help, click at the Context Help tool bar button, or use the keyboard short cut **Ctrl-F1**.

8.9.4 Using help

The `Using Help` command offers a guide to how the help feature works.

8.10 Trace Display Window - Menu Items

When a trace is taken and displayed, BusView enters the Trace Display window. The Trace Display window features some new menu bar items, and some new tool bar items. The Trace Display window is slightly different when the trace is displayed as an alphanumeric list compared to when it is displayed as a waveform.

8.10.1 Search Menu

BusView features a Search and Extract mechanism where the user can define search/extract patterns.

Edge jumping is a feature in Waveform display, which allows the user to jump to the nearest falling or rising edge of the selected signal(s).

8.10.1.1 Edit Search Pattern


The "Edit Search Pattern" tool bar button

The `Edit Search Pattern` command displays the window in Figure 8.17, which allows the user to define one search pattern and one extract pattern.

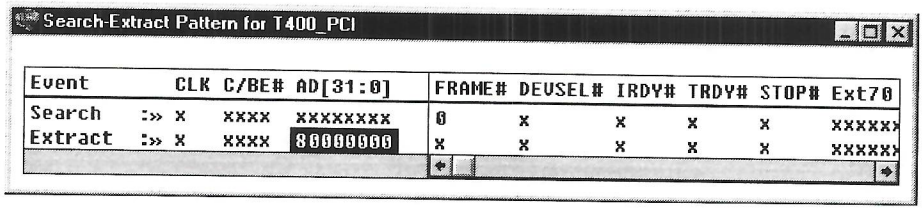


Figure 8.17 The Edit Search Pattern window

8.10.1.2 Extract


The "Extract" tool bar button

The `Extract` command extracts all trace lines from the current trace buffer which matches the extract pattern defined in Section 8.10.1.1, and displays them in an alphanumeric trace list.

ESC can be used to cancel the extract operation.

Warning! The Ext7 field is not valid as long as `Extract` is activated.

8.10.1.3 Search

The `Search` command searches for the first trace line in the current trace buffer that matches the search pattern defined in Section 8.10.1.1. The cursor jumps to the matching trace line.

ESC can be used to cancel the search operation.

Warning! The Ext7 field is not valid as long as `Search` is activated.

8.10.1.4 Next Match


The "Next Match" tool bar button

The `Next Match` command makes the cursor jump to the next line in the current trace buffer that matches the search pattern defined in Section 8.10.1.1.

8.10.1.5 Previous Match


The "Previous Match" tool bar button

The `Previous Match` command makes the cursor jump to the previous line in the current trace buffer that matches the search pattern defined in Section 8.10.1.1.

8.10.1.6 Previous Edge


The "Previous Edge" tool bar button

The `Previous Edge` command is only available in Waveform display mode, and makes the cursor jump to the previous edge of the currently selected signals. The `Edge Options` command sets whether it searches for a rising edge, a falling edge, or any edge. See Section 8.10.1.8 below.

8.10.1.7 Next Edge


The "Next Edge" tool bar button

The `Next Edge` command is only available in Waveform display mode, and makes the cursor jump to the next edge of the currently selected signals. The `Edge Options` command sets whether it searches for a rising edge, a falling edge, or any edge. See Section 8.10.1.8 below.

8.10.1.8 Edge Options

The `Edge Options` command defines if the Search commands "Next Edge" and "Previous Edge" should search for a rising edge, a falling edge, or any edge. The command is only available in Waveform display mode.

8.10.2 Jump Menu

To allow the user to jump easily from one place in the trace buffer to another, a set of "jump" tools are developed.

8.10.2.1 First Line


The "First Line" tool bar button

The `First Line` command makes the cursor jump to the first line of the trace buffer.

8.10.2.2 Last Line


The "Last Line" tool bar button

The `Last Line` command makes the cursor jump to the last line of the trace buffer.

8.10.2.3 Trigger Line


The "Trigger Line" tool bar button

The `Trigger Line` command makes the cursor jump to the trigger line. The trigger line can be at Start of Trace, 25% of Trace, 50% of Trace, 75% of Trace, and End of Trace, according to Section 8.3.7.

8.10.2.4 Marker Y

The `Marker Y` command makes the cursor jump to the position of the Y-marker in the trace buffer. For more information about markers, see Section 8.10.4.

8.10.2.5 Marker Z

The `Marker Z` command makes the cursor jump to the position of the Z-marker in the trace buffer. For more information about markers, see Section 8.10.4.

8.10.2.6 Line Number


The "Line Number" tool bar button

The `Line Number` command opens the Jump to Line dialog box, which gives the user opportunity to type in which line in the trace buffer the cursor should jump to.

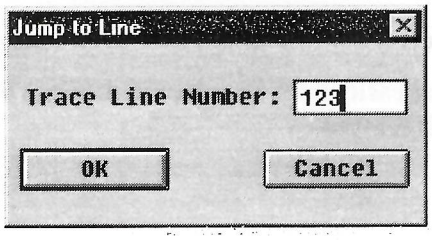


Figure 8.18 The Jump to Line dialog box

8.10.3 Format Menu

The `Format` menu contains items suitable for formatting the Trace Display window to the taste of the user. It applies to both the alphanumeric, and the waveform Trace Display window.

8.10.3.1 Scale


The "Scale" tool bar button

The `Scale` command opens the dialog box in Figure 8.19. By using the slide control, by changing the percentage, or by clicking at the "Zoom In/Out" buttons at each end of the slide control, the user may change the axis of the waveforms in the Trace Display window. The "Zoom In/Out" buttons increase/decrease the sample size by a factor of 2.

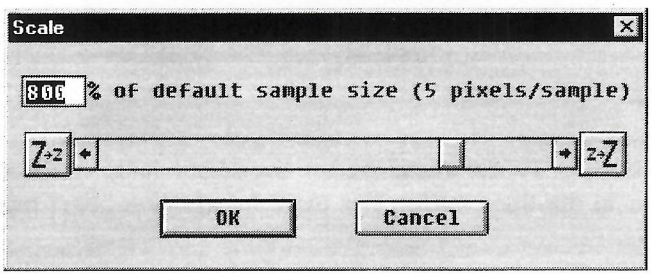


Figure 8.19 The Scale dialog box

8.10.3.2 Zoom In


The "Zoom In" tool bar button

The `Zoom In` command increases the sample size by a factor of 2, i.e. it is used to get a closer look at the waveform diagrams.

8.10.3.3 Zoom Out


The "Zoom Out" tool bar button

The `Zoom Out` command decreases the sample size by a factor of 2, i.e. it is used to get an overview of the trace buffer.

8.10.3.4 Decoding and Formatting


The "Decoding & Formatting" tool bar button

The `Decoding and Formatting` command allows the signal at the cursor position to be presented in a decoded form (with mnemonics). A dialog box with one or two options appears, depending on which signal field is selected. The first option enables/disables *global* decoding/formatting, and the second option enables/disables decoding/formatting for that specific signal field.

8.10.3.5 Trace Signals

The signal fields in a trace display can be moved, removed, and deleted according to the wishes of the user. See Section 8.2.1. When the Trace Display window looks the way the user wants it, the template can be saved, closed, and reopened at a later time.

Open Template

The `Open Template` command opens the dialog box in Figure 8.20, which allows the user to open any previously stored trace display template. Select the desired template and press the OK button, or double click on it.

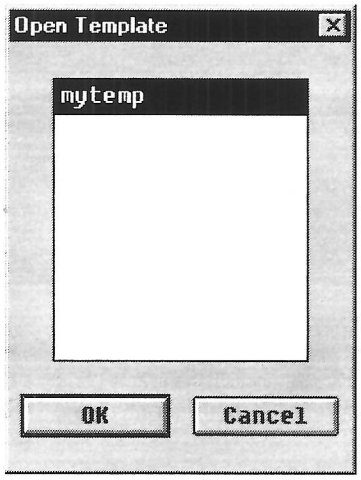


Figure 8.20 The Open Template dialog box

Save Template

The `Save Template` command opens the dialog box Figure 8.21, where the user can type a name of the template to be saved.

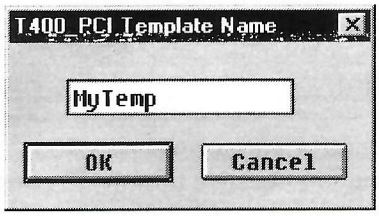


Figure 8.21 The Save Template dialog box

Delete Template

The `Delete Template` command opens the dialog box in Figure 8.22. Select the template to be deleted and press the OK button, or double click on it.

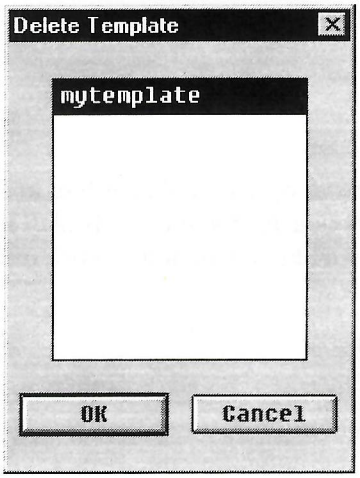


Figure 8.22 The Delete Template dialog box

8.10.4 Marker Menu

By default there are two markers in the waveform window, the T-marker which marks the trigger position, and the X-marker which is moveable. The time difference between the two markers is displayed above the waveforms in the Waveform window.

The Y(Z)-marker is an additional marker which the user can move around as desired. If the Y(Z)-marker is the first marker inserted into the waveforms, the time difference X-Y(Z) is displayed above the waveforms. If it is the second

marker inserted, both the time differences X-Y(Z) and Z(Y)-Y(Z) are displayed above the waveforms.

Markers are moved by selecting them with the mouse and dragging them to the desired spot. The Y and Z-markers are moved with the right mouse button, and the X-marker is moved with the left mouse button.

Note! The markers are only available in the waveform window.

8.10.4.1 Set Marker Y


The "Marker Y" tool bar button

The `Marker Y` command inserts the Y-marker into the waveform window.

8.10.4.2 Set Marker Z


The "Marker Z" tool bar button

The `Marker Z` command inserts the Z-marker into the waveform window.

8.10.4.3 Delete Marker Y

The `Delete Marker Y` command removes the Y-marker from the waveform window.

8.10.4.4 Delete Marker Z

The `Delete Marker Z` command removes the Z-marker from the waveform window.

9. PCI BUS ANOMALIES

9.1 Figures

All the figures in this chapter are "snap-shots" from BusView with the PTIMBAT400-PB. The PTIMBAT400-PB samples at 400 MHz (i.e. one sample every 2.5ns), and this is the reason why the **CLK** signal sometimes does not have a 50% duty cycle.

9.2 Setup Requirements

The PTIMBAT400 checks that the setup time is met on all required signal lines. The setup time is checked regardless of the frequency in the PCI system i.e. if the PCI clock frequency is 25MHz, the PTIMBAT400 checks that the boards in this system meet the setup time as if it was running at 33.33MHz.

The PTIMBAT400 checks the setup time as follows:

33.33MHz The PTIMBAT400/PBAT66 samples the PCI signals 24ns after every rising clock edge, and compares this value with a sample made 29ns after the rising edge of the clock. If these two values are the same, stability is assumed. If data is marginal, it will often differ between these measurement points.

66.66MHz The PTIMBAT400/PBAT66 samples the PCI signals 12ns after every rising clock edge, and compares this value with a sample made 15ns after the rising edge of the clock. If these two values are the same, stability is assumed. If data is marginal, it will often differ between these measurement points.

A board could be slow in putting valid data on the bus and still meet the 7ns (3ns at 66.66MHz) setup time in a system not running at maximum frequency. If the system is running at 25MHz the clock period is 40ns (1/25MHz), and the board could put out data 33ns after the clock, and still meet the required 7ns setup time. However, if this board is later put in a 33.33MHz system, it would fail, but we would never know unless we were running the PTIMBAT400 in that faster system.

9.3 C/BE[3::0]# Unstable

C/BE[3::0]# - Unstable according to 33.33MHz/66.66MHz setup timing requirements (7ns/3ns) on rising edge of **CLK**. The Command must be stable in the address phase. Byte Enables must be stable on the clock following the address phase, the clock following each completed data phase, and remain valid every clock during the entire data phase regardless of wait states.

In Figure 9.1 and Figure 9.2, **C0** and **BE0#** break the 7ns timing requirements, i.e. they are not stable until 5ns before the rising edge of **CLK**.

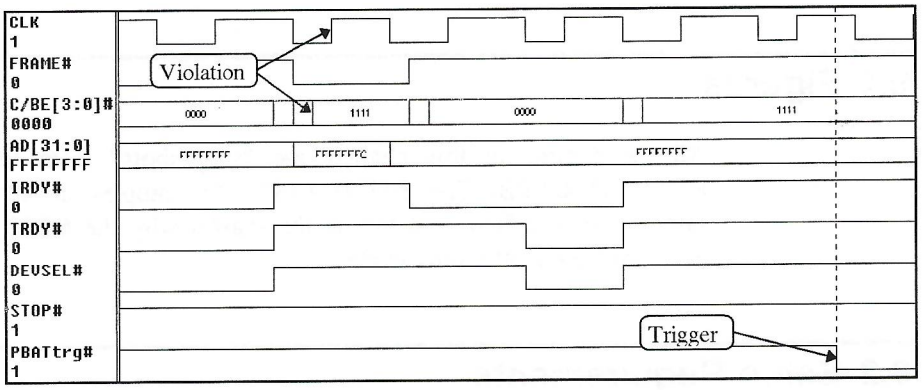


*Figure 9.1 **C0** unstable*

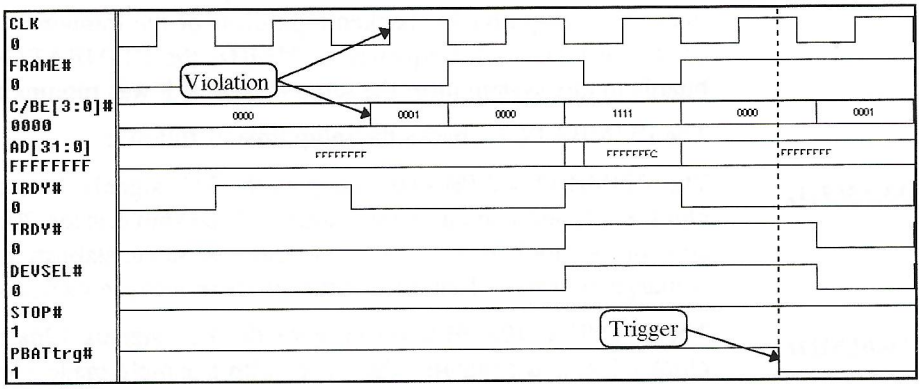


*Figure 9.2 **BE0#** unstable*

PCI Spec. 2.1

Page 246 Rule 3a, Command.

Rule 3b, Byte Enables

9.4 AD[31::0] Unstable

AD[31::0] - Unstable according to 33.33MHz/66.66MHz setup timing requirements (7ns/3ns) on rising edge of **CLK**. Address must be stable in address phase. Data must be stable when **TRDY#** is asserted on read, when **IRDY#** is asserted on write, and when **IRDY#** is asserted in Special cycle command.

In Figure 9.3 and Figure 9.4 the **A0** and **D0** break the 7ns timing requirements, i.e. they are not stable until 5ns before the rising edge of **CLK.**

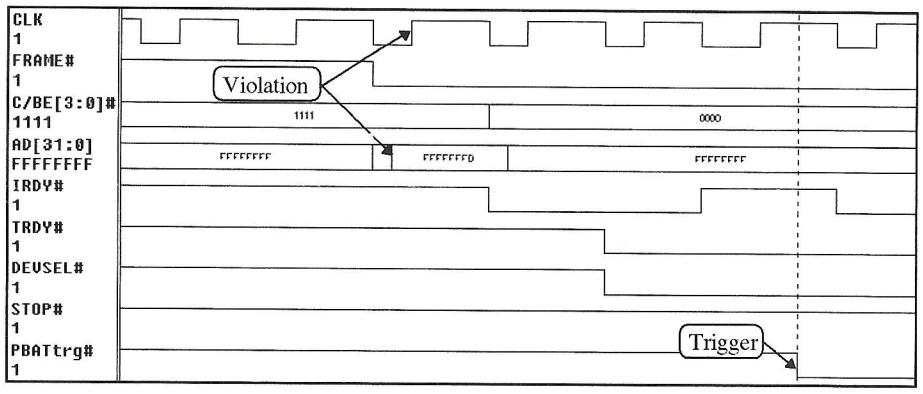


*Figure 9.3 **A0** unstable*

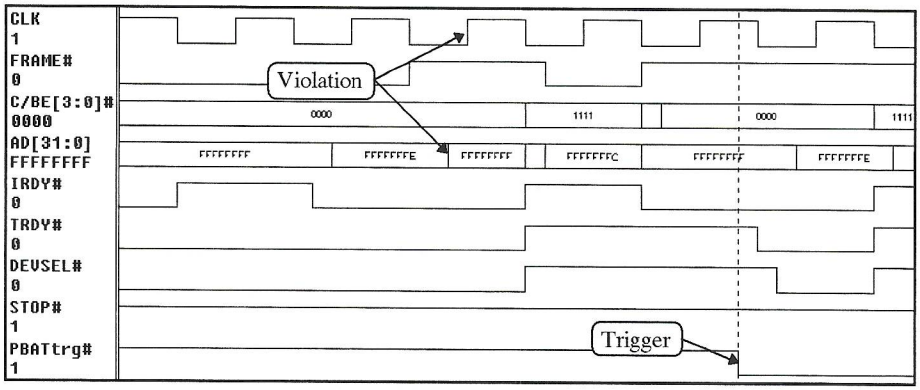


*Figure 9.4 **D0** unstable*

PCI Spec. 2.1

Page 245

Rule 2a, Address.

Rule 2c, Data read/write.

Rule 2e Data Special Cycle

9.5 PAR Unstable

PAR - Parity signal unstable according to 33.33MHz/66.66MHz setup timing requirements (7ns/3ns) on rising edge of **CLK**. **PAR** must be stable the clock following the valid time of **AD[31::00]**.

In Figure 9.5, **PAR** breaks the 7ns timing requirements, i.e. it is not stable until 5ns before the rising edge of **CLK**.

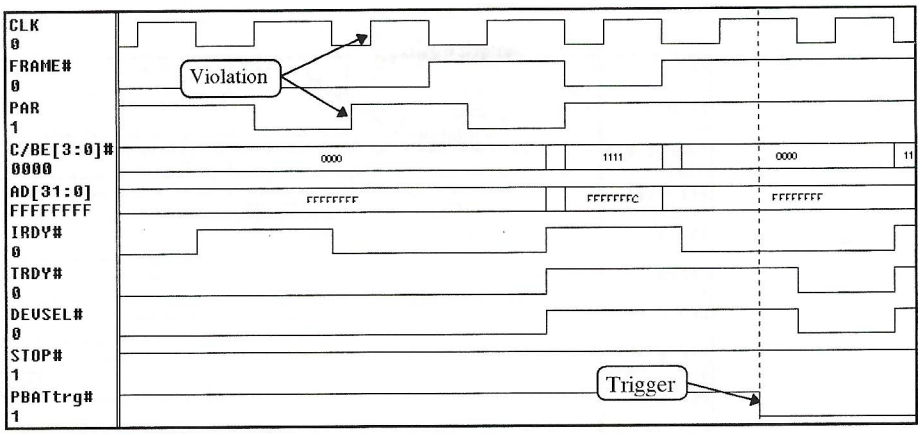


*Figure 9.5 **PAR** unstable*

PCI Spec. 2.1

Page 246 Rule 4

9.6 Master Ctrl Unstable

PCI master control signals (**FRAME#, IRDY#** or **LOCK#**) are unstable according to 33.33MHz/66.66MHz setup timing requirements (7ns/3ns) on all rising edges of **CLK**.

In Figure 9.6, Figure 9.7, and Figure 9.8, the **FRAME#, IRDY#**, and **LOCK#** signals break the 7ns timing requirements, i.e. they are not stable until 5ns before the rising edge of **CLK**.

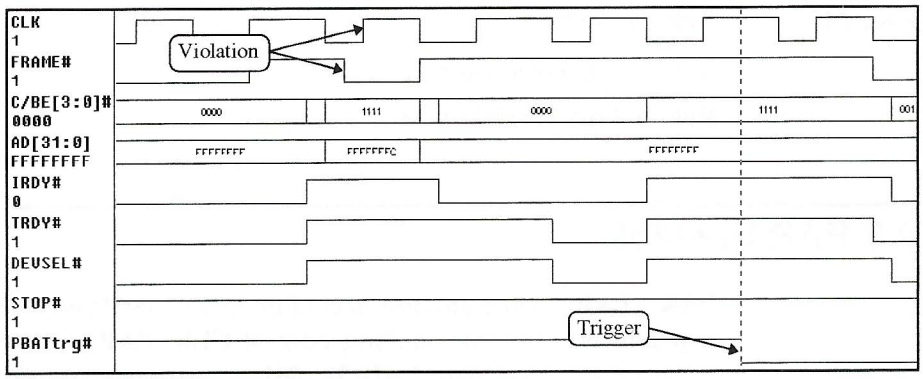


*Figure 9.6 **FRAME#** unstable*

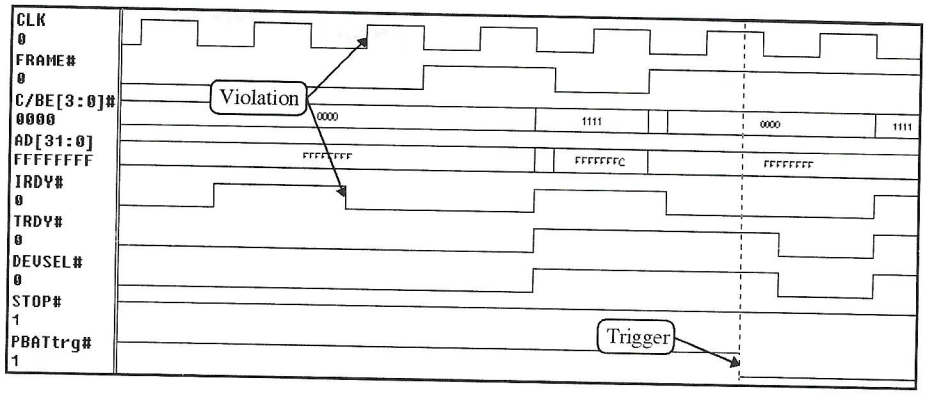


*Figure 9.7 **IRDY#** unstable*

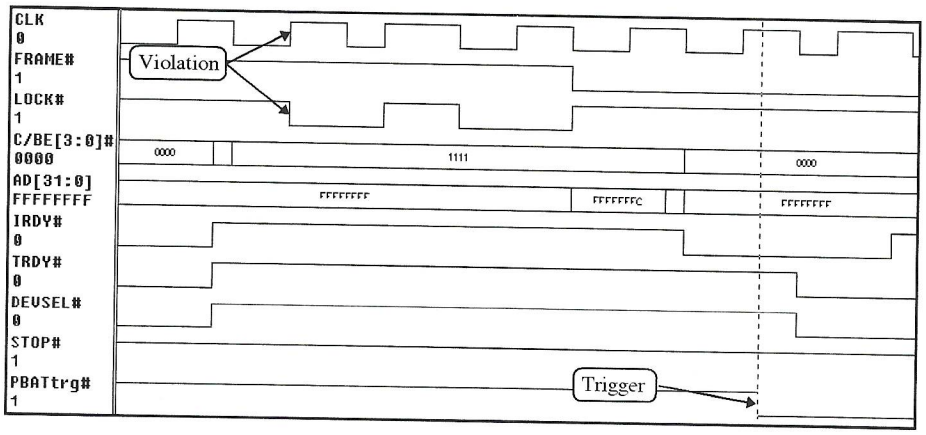


*Figure 9.8 **LOCK#** unstable*

PCI Spec. 2.1

Page 245 Rule 1

9.7 Target Ctrl Unstable

PCI target control signals (**DEVSEL#**, **TRDY#** or **STOP#**) are unstable according to 33.33MHz/66.66MHz setup timing requirements (7ns/3ns) on all rising edges of **CLK**.

In Figure 9.9, Figure 9.10, and Figure 9.11, the **DEVSEL#**, **TRDY#**, and **STOP#** signals break the 7ns timing requirements, i.e. they are not stable until 5ns before the rising edge of **CLK**.

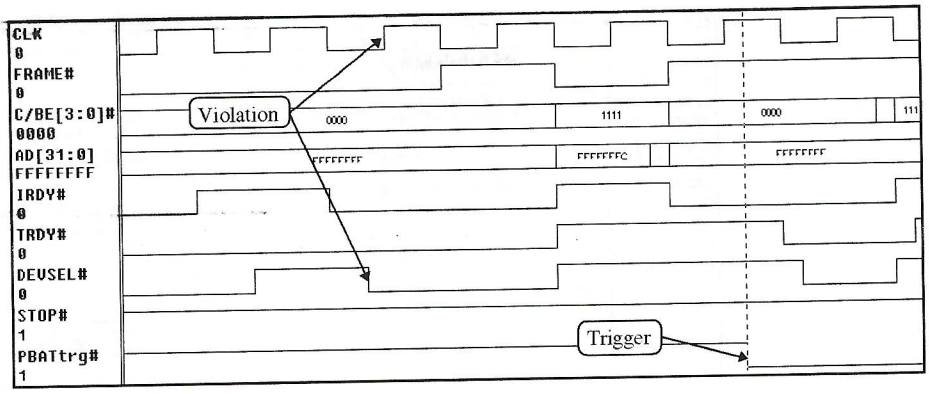


Figure 9.9 ***DEVSEL#*** *unstable*

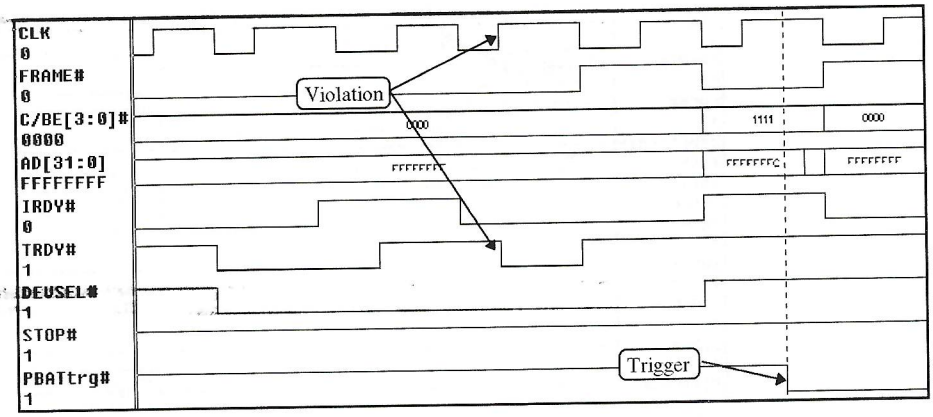


Figure 9.10 ***TRDY#*** *unstable*

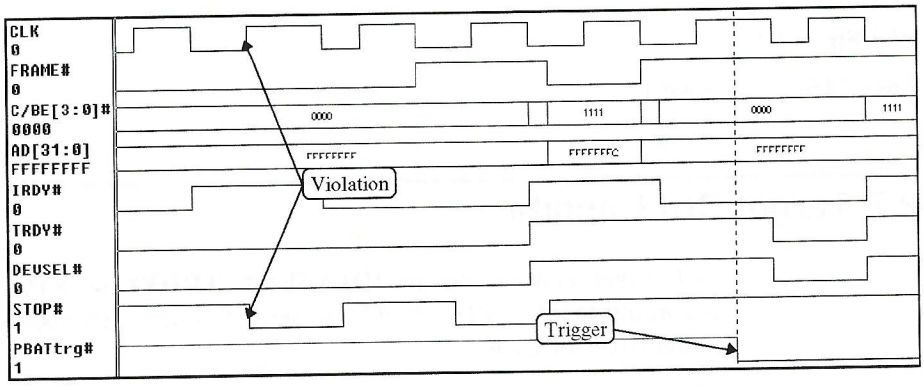


Figure 9.11 ***STOP#*** *unstable*

PCI Spec. 2.1

Page 245 Rule 1

9.8 Misc. signals Unstable

Miscellaneous signals (**PERR#**, **SDONE** or **SBO#**) unstable according to 33.33MHz/66.66MHz setup timing requirements (7ns/3ns) on all rising edges of **CLK**.

In Figure 9.12, Figure 9.13, and Figure 9.14, **PERR#**, **SDONE** and **SBO#** break the 7ns timing requirements, i.e. they are not stable until 5ns before the rising edge of **CLK**.

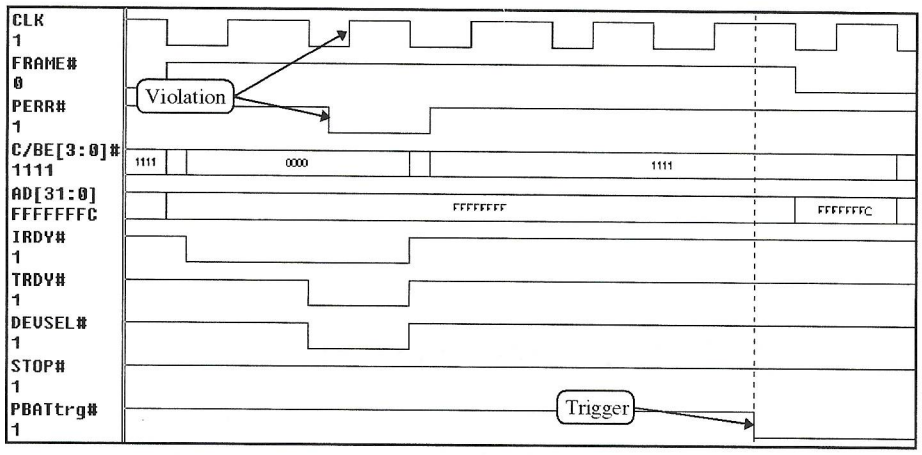


Figure 9.12 ***PERR#*** *unstable*

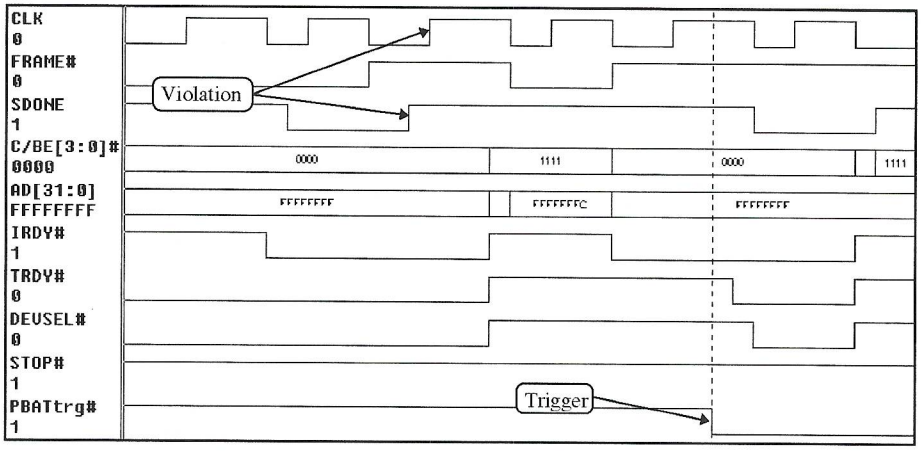


Figure 9.13 ***SDONE*** *unstable*

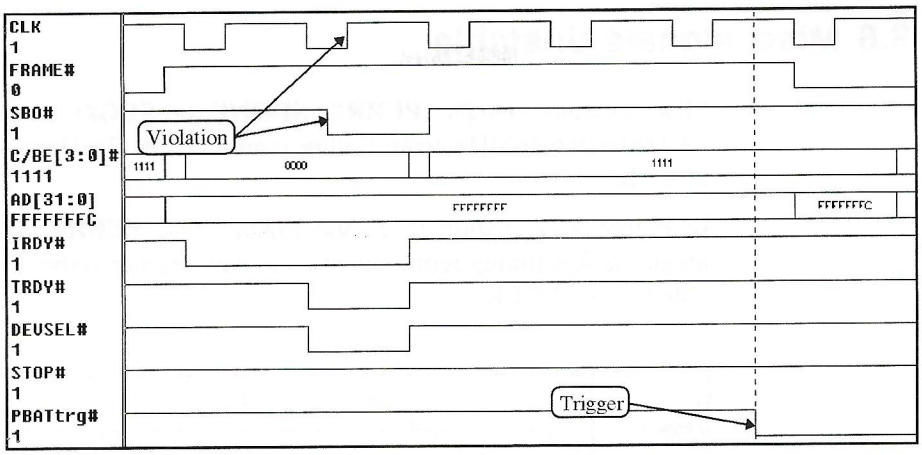


*Figure 9.14 **SBO#** unstable*

PCI Spec. 2.1

Page 245 Rule 1

9.9 Illegal FRAME# Re-Assertion

Once **FRAME#** is de-asserted, it cannot be reasserted during the same transaction. A transaction is not finished until both **FRAME#** and **IRDY#** is de-asserted.

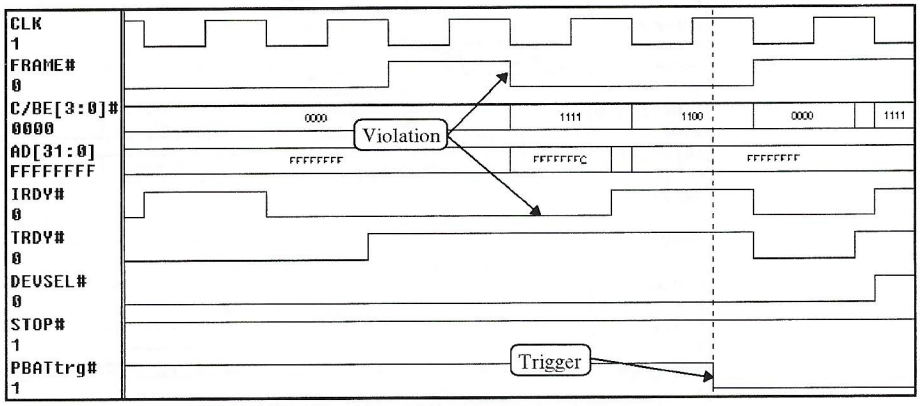


*Figure 9.15 Illegal **FRAME#** re-assertion*

PCI Spec. 2.1 Section 3.3.3.1

Page 246 Rule 8b

9.10 Illegal FRAME# or IRDY# Change

Once a master has asserted **IRDY#,** it cannot change **FRAME#** or withdraw **IRDY#** until current data phase completes.

A data phase is completed on every rising clock edge where both **IRDY#** and **TRDY#** are asserted.

In Figure 9.16, the target inserts a wait state, and thus the data phase does not complete until the clock cycle where both **IRDY#** and **TRDY#** are asserted again. The PBAT66 flags an error because **FRAME#** is de-asserted before that happens.

In Figure 9.17, the target inserts a wait state ,but the master de-asserts **IRDY#** before the target completes the data phase with TRDY#.

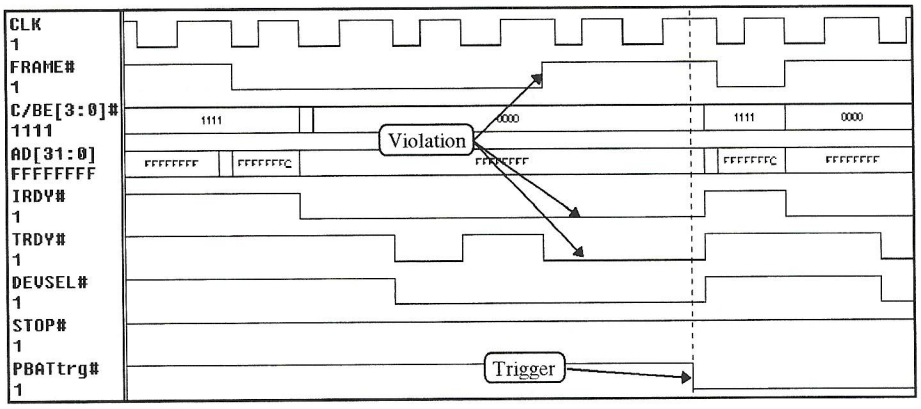


*Figure 9.16 Illegal change of **FRAME***

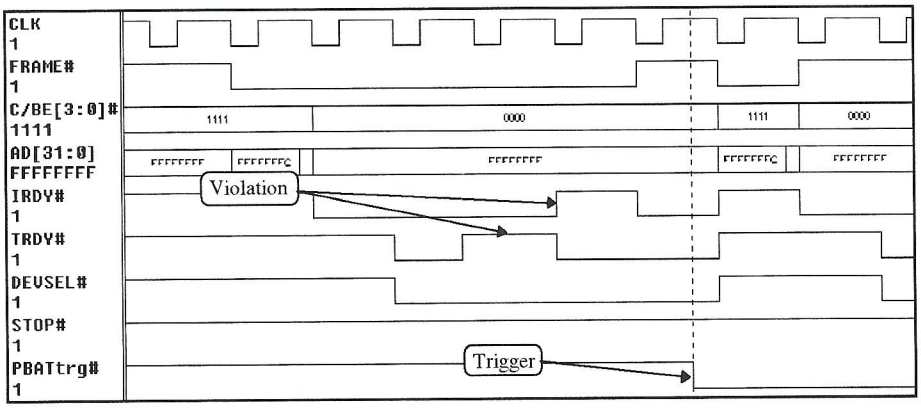


*Figure 9.17 Illegal change of **IRDY#***

PCI Spec. 2.1 Section 3.1.1

Page 246 Rule 8d

9.11 FRAME# off Before IRDY#

FRAME# can not be de-asserted before **IRDY#** is asserted.

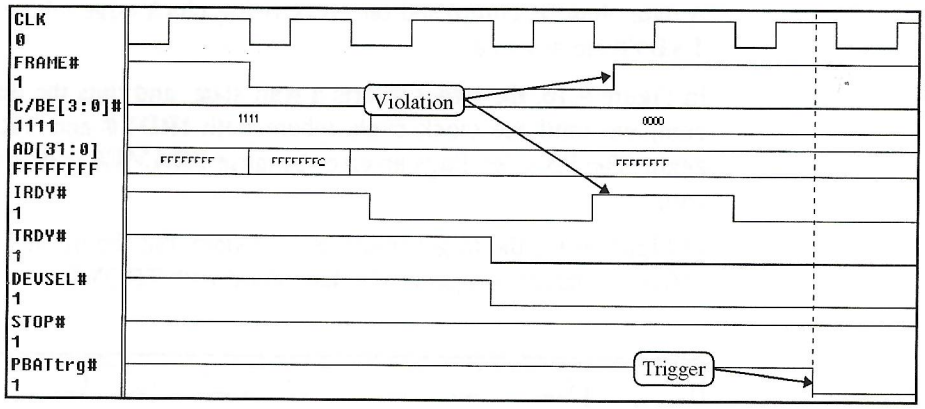


Figure 9.18 ***FRAME#*** *de-asserted before* ***IRDY#*** *is asserted*

PCI Spec. 2.1 Section 3.3.1, and Section 3.3.2

Page 246 Rule 8c

9.12 FRAME# off in DAC

FRAME# must remain asserted for the cycle following a Dual Address Command (DAC).

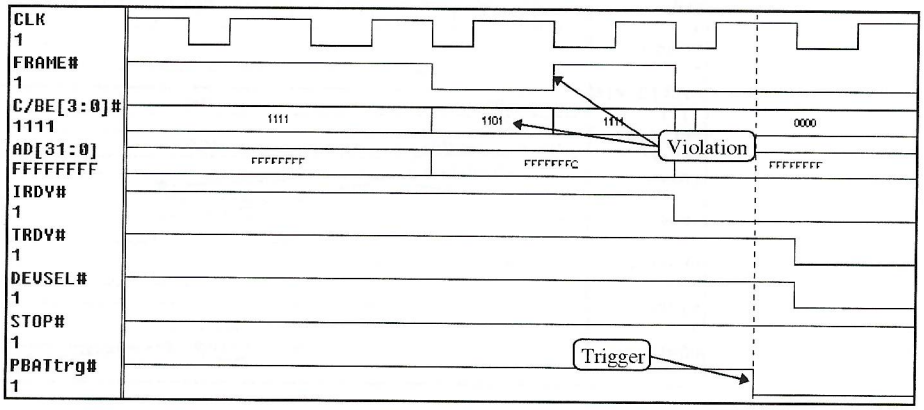


Figure 9.19 ***FRAME#*** *de-asserted after DAC*

PCI Spec. 2.1 Section 3.10.1

9.13 Illegal FRAME# to IRDY#

IRDY# Timing Violation, **IRDY#** must be asserted within 8 clocks of **FRAME#**.

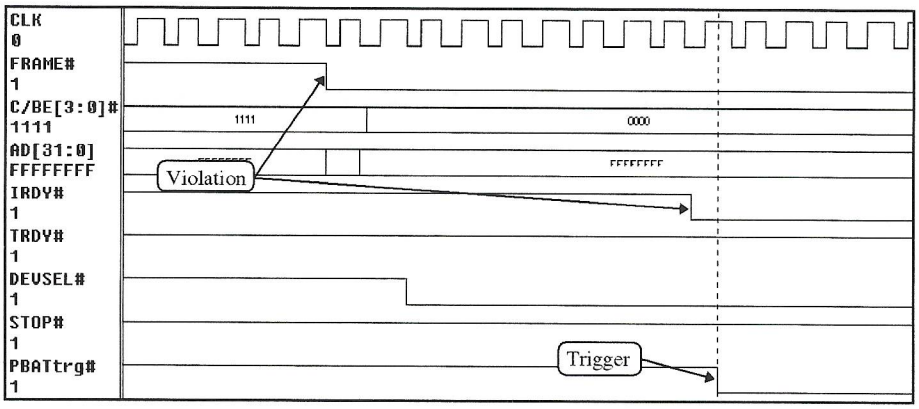


*Figure 9.20 9 (more than 8) clock cycles from **FRAME#** to **IRDY#***

PCI Spec. 2.1 Section 3.5.3.1

Page 248 Rule 27

9.14 Illegal IRDY# Assertion

IRDY# must be de-asserted in turn-around cycle (address phase).

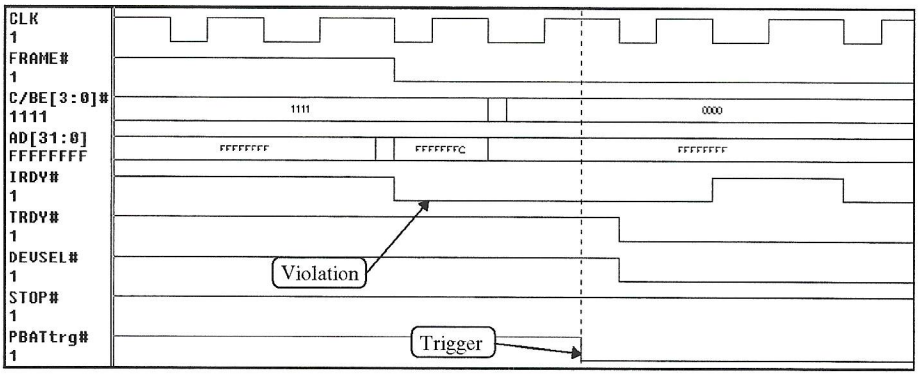


*Figure 9.21 **IRDY#** is asserted in turn-around cycle*

PCI Spec. 2.1 Section 3.2.4

9.15 Illegal LOCK# Assertion

LOCK# must be asserted the clock following the address phase and kept asserted to maintain control.

LOCK# must be released whenever an access is terminated by Target-Abort or Master-Abort.

Once lock is established, the target remains locked until both **FRAME#** and **LOCK#** are sampled de-asserted or the target signals Target-Abort.

In Figure 9.22, **LOCK#** is released too late.

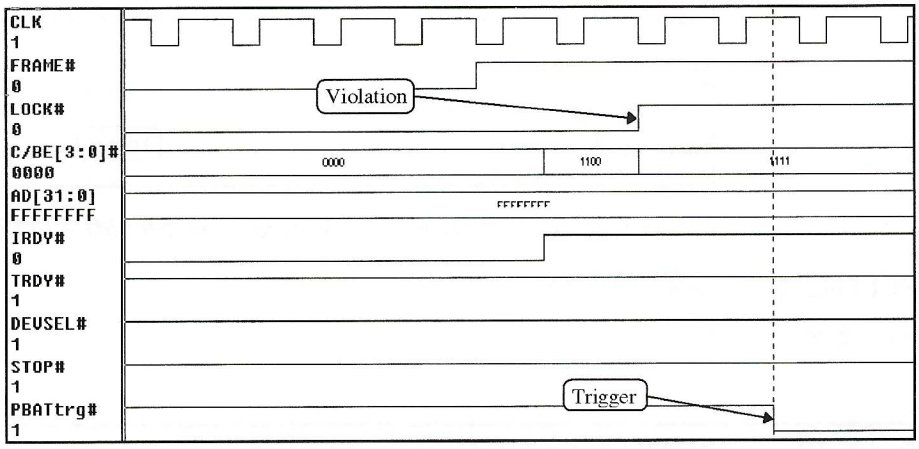


*Figure 9.22 Illegal **LOCK#** de-assertion*

PCI Spec. 2.1 Section 3.6

Page 245 Rule 32e,g

Rule 31b

9.16 First LOCK# not Read

The first transaction of a **LOCK#** operation must be a read transaction.

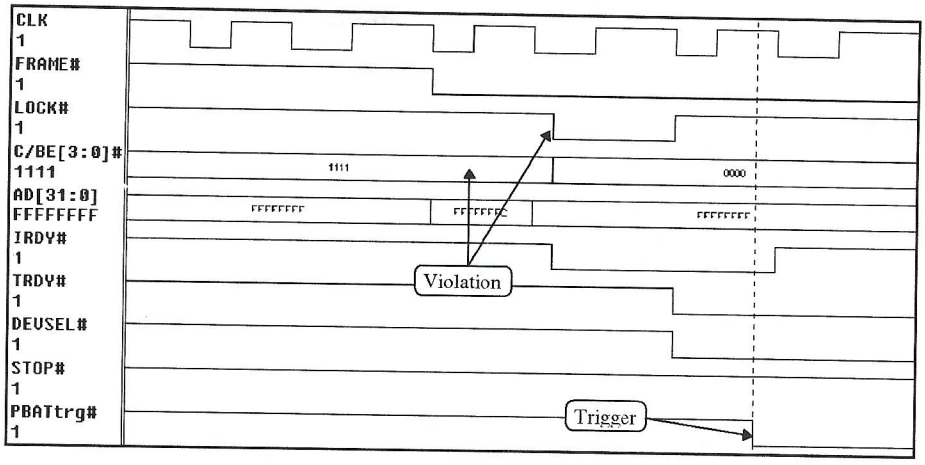


*Figure 9.23 **LOCK#** operation is not a Read transaction*

PCI Spec. 2.1 Section 3.6

Page 249 Rule 32d

9.17 Target Protocol Errors

- **DEVSEL#** cannot be de-asserted while **STOP#** is asserted, see Figure 9.24.
- **TRDY#** can not be active on Target-Abort.
- Target must issue **DEVSEL#** before any other response. In Figure 9.25, **TRDY#** is asserted before **DEVSEL#**.

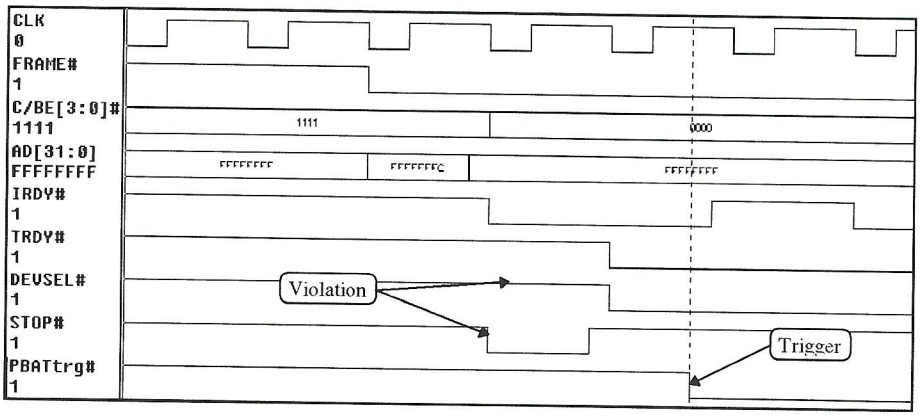


*Figure 9.24 Illegal **DEVSEL#** assertion*

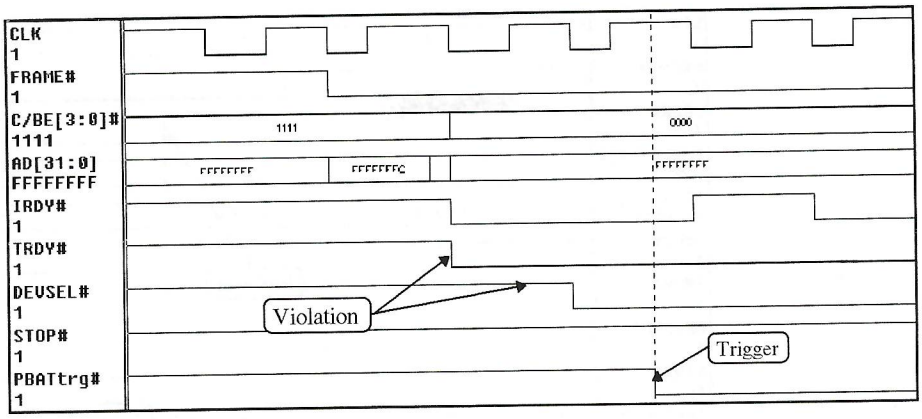


*Figure 9.25 **TRDY#** asserted without **DEVSEL#***

PCI Spec. 2.1 Section 3.3.3.2.1 and 3.7.1

Page 249 Rule 34

9.18 Illegal TRDY# Assertion

The first data phase on a Read transaction requires a turnaround cycle with **TRDY#** de-asserted.

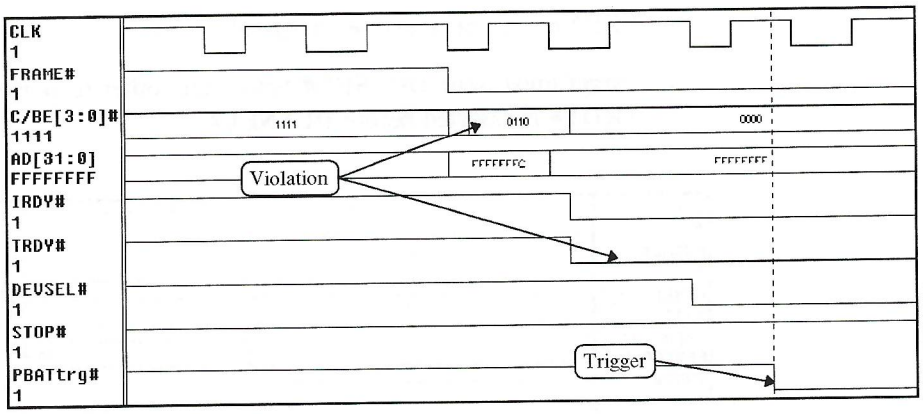


*Figure 9.26 **TRDY#** is asserted in a Turn-Around cycle*

PCI Spec. 2.1 Section 3.3.1

9.19 Illegal Target Change

Once a TARGET has asserted **TRDY#** or **STOP#,** it cannot change **DEVSEL#**, **TRDY#**, or **STOP#** until the current data phase completes.

The current data phase is not completed until both **TRDY#** and **IRDY#** are sampled asserted, and thus the target cannot de-assert **DEVSEL#** the way it is shown in Figure 9.27.

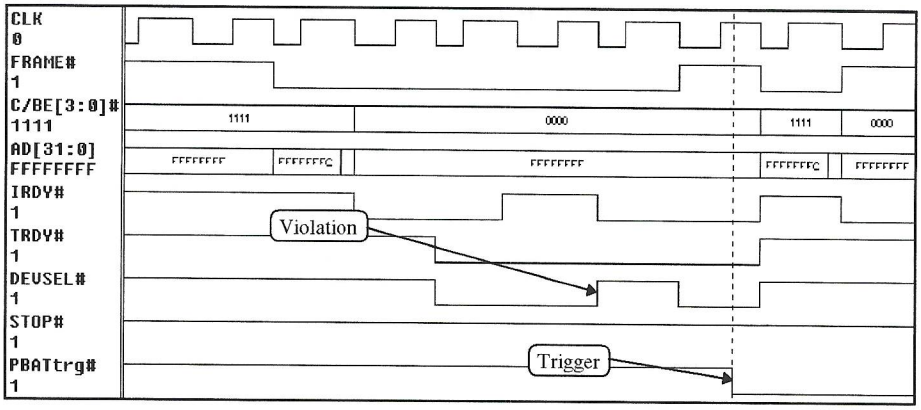


*Figure 9.27 Illegal de-assertion of **DEVSEL#** during data phase*

PCI Spec. 2.1

Page 247 Rule 12d

9.20 Illegal DEVSEL# off

Once a target has asserted **DEVSEL#**, it must not be de-asserted until the last data phase has completed.

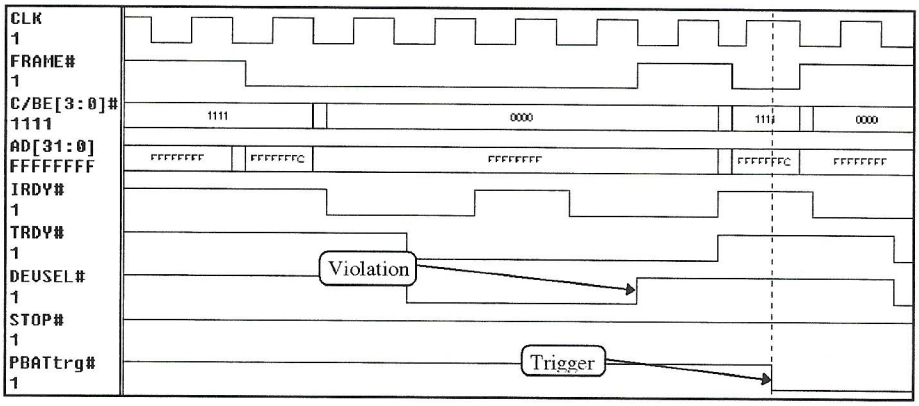


*Figure 9.28 **DEVSEL#** de-asserted before last data phase*

PCI Spec. 2.1

Page 247 Rule 15

9.21 Illegal DEVSEL# on/off

DEVSEL# should not be asserted in the address phase or when the bus is idle. **DEVSEL#** should not be de-asserted before the transaction is completed, unless it is a Target-Abort termination.

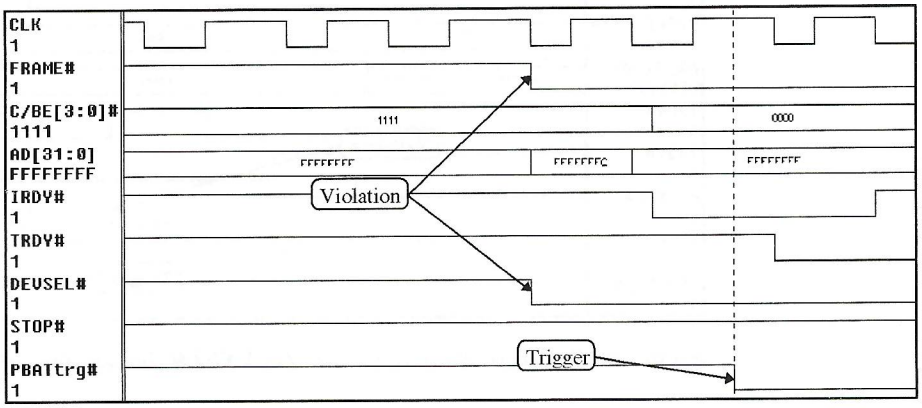


*Figure 9.29 **DEVSEL#** asserted at start of address phase*

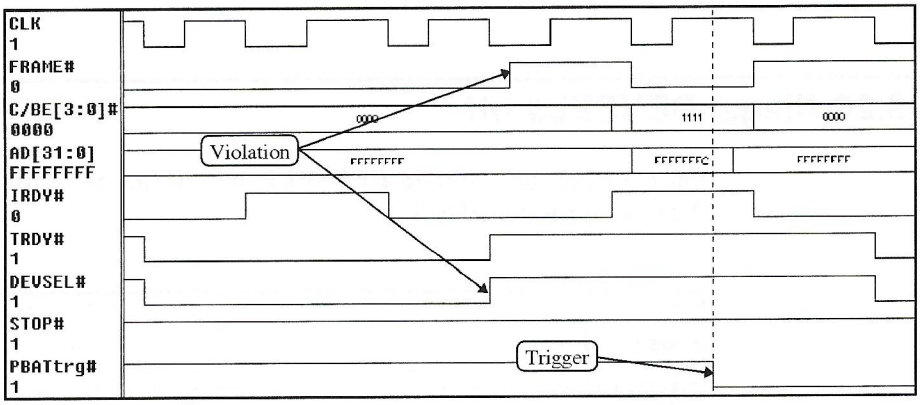


*Figure 9.30 Illegal **DEVSEL#** de-assertion without Target Abort*

PCI Spec. 2.1

Page 249 Rule 33, 35

9.22 Abnormal STOP#

Abnormal stops can be divided into three points:

- **STOP#** fails to be de-asserted the cycle immediately after **FRAME#** is sampled de-asserted.
- When **STOP#** is low, **FRAME#** and **IRDY#** cannot both be high.

- Once **STOP#** is asserted, it must remain asserted until **FRAME#** is de-asserted.

Figure 9.31 and Figure 9.32 violates the two first rules, respectively.

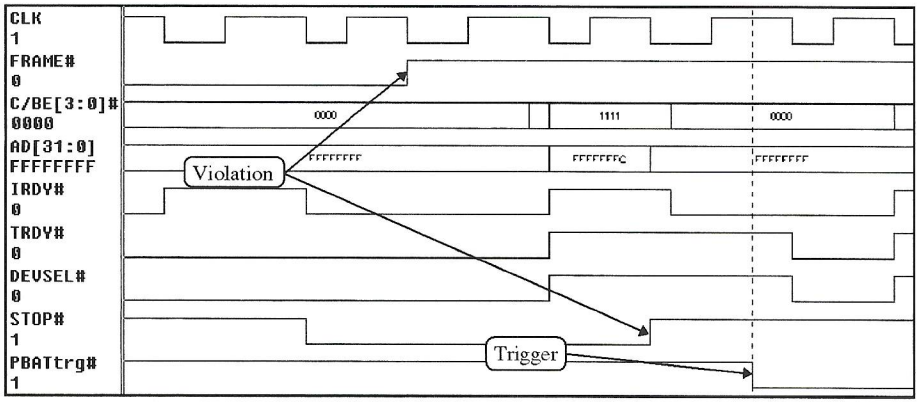


*Figure 9.31 **STOP#** is de-asserted too late*

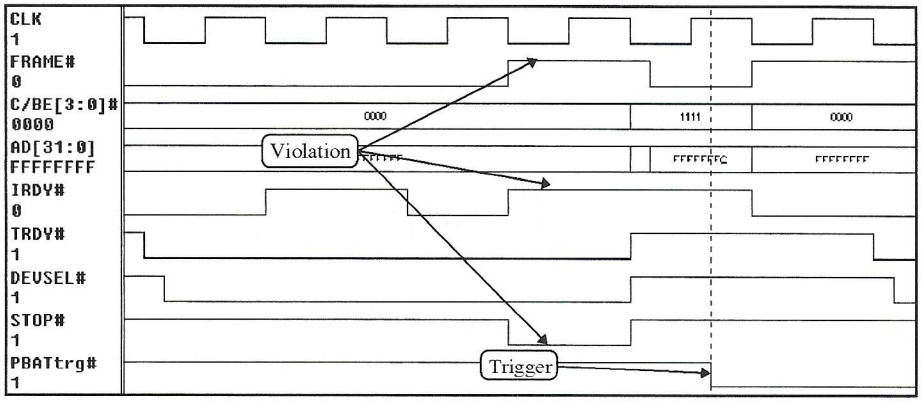


*Figure 9.32 Illegal **FRAME#** and **IRDY#** with **STOP#***

PCI Spec. 2.1

Page 247 Rule 12c,f

9.23 Illegal STOP# to FRAME# off

When **STOP#** is asserted with **FRAME#** active, the Master must de-assert **FRAME#** as soon as it can drive **IRDY#**.

In Figure 9.33, the master drives **IRDY#**, but **FRAME#** remains asserted.

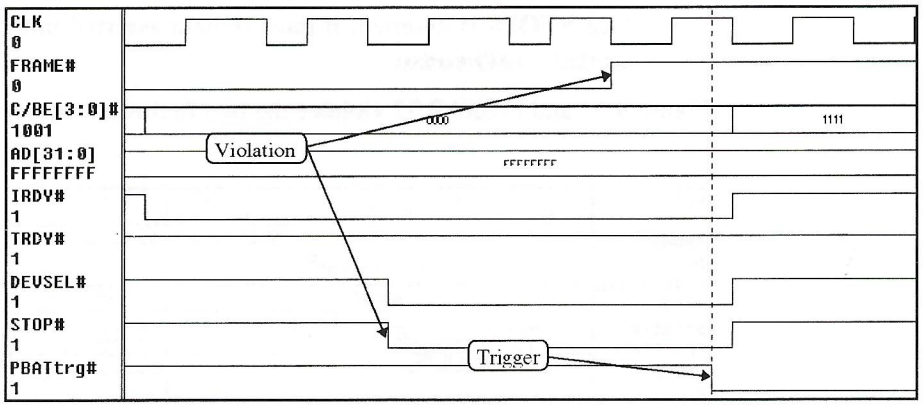


*Figure 9.33 **FRAME#** is de-asserted too late*

PCI Spec. 2.1

Page 247 Rule 12e

9.24 Illegal A1, A0 & BE[3::0]#

A target must abort I/O transfers with illegal combination of **AD1, AD0** and corresponding **C/BE#** for I/O cycle.

The legal combinations are shown in Table 9.1.

AD1	AD0	C/BE[3]#	C/BE[2]#	C/BE[1]#	C/BE[0]#
0	0	x	x	x	0
0	1	x	x	0	1
1	0	x	x	0	1
1	1	0	1	1	1

*Table 9.1 Legal combinations of **C/BE[3::0]#** and **AD[1::0]***

In Figure 9.34, **C/BE#** is 0x0001 and **AD[1::0]**=00, which is not a valid combination.

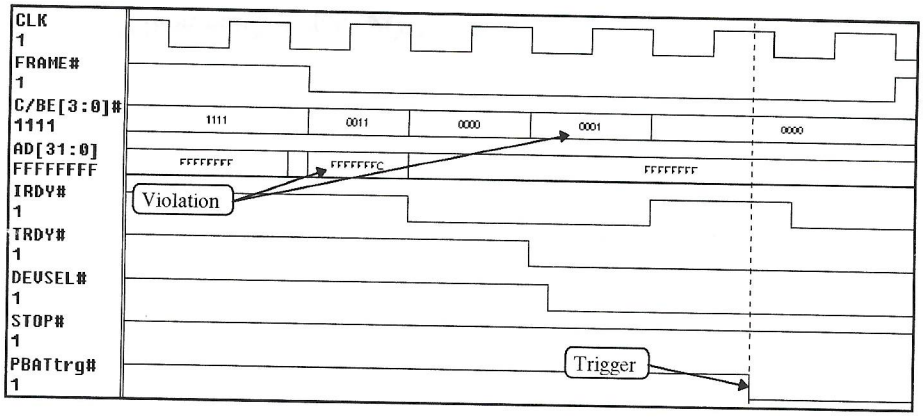


*Figure 9.34 Illegal combination of **C/BE[3::0]#** and **AD[1::0]***

PCI Spec. 2.1 Section 3.3.2

9.25 Illegal Command Response

Targets must not respond to **Reserved** (0100, 0101, 1000 or 1001) commands or the **Special Cycle** (0001) command.

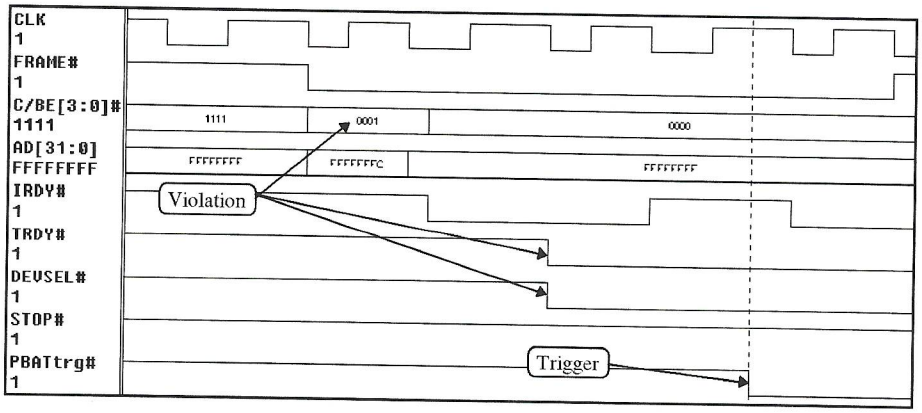


Figure 9.35 Target is responding to a Special Cycle

PCI Spec. 2.1 Section 3.1.1, and Section 3.7.2

9.26 Illegal A1/A0 Memory Commands

All 2.1 compliant devices with **AD[1::0]** equal to 0,1 and 1,1 must terminate the data transfer after the first data phase, when the Command field indicates a memory command.

In Figure 9.36, **STOP#** should be asserted to indicate termination after the first data phase.

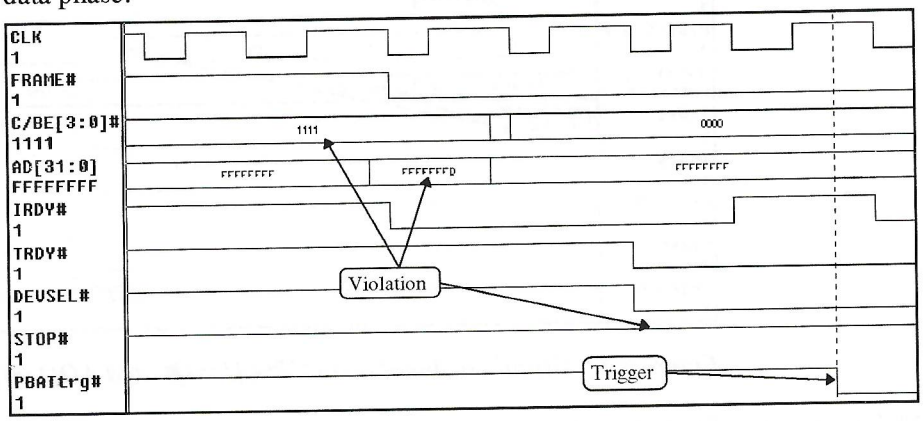


Figure 9.36 The transaction is not terminated after the first data phase

PCI Spec. 2.1 Section 3.2.2

9.27 Illegal Linear Address Incrementing Mode

The Memory Write & Invalidate Command can only use the Linear Address Incrementing Mode (**AD[1::0]** = 0,0).

In Figure 9.37, the **C/BE#** field signals a Memory Write & Invalidate Command, but the Address is 0xFFFFFFFD, i.e. **AD[1::0]** = 0,1.

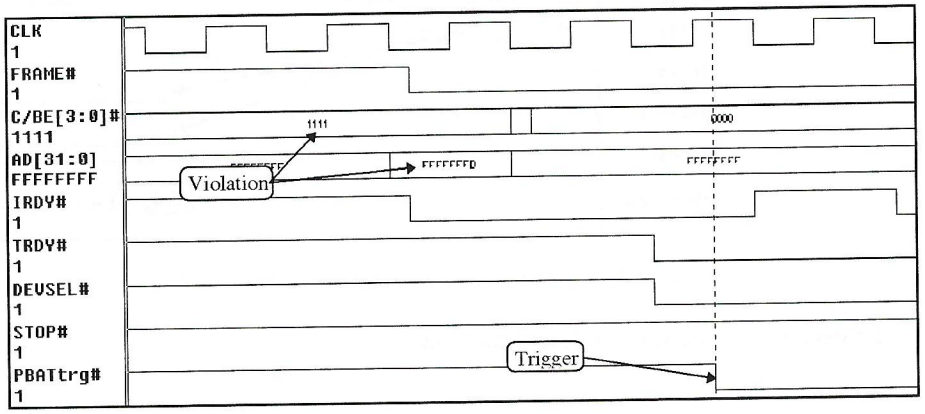


*Figure 9.37 **AD[1::0]** ≠ 0,0 in Mem. Write & Invalidate Cmd.*

PCI Spec. 2.1 Section 3.2.2

9.28 Illegal Configuration 0 Cycle

Type 0 Configuration cycle claimed by a Bridge device. Type 0 configuration cycles are not propagated beyond the local PCI Bus. It must be claimed by a local device within SLOW decode timing, or terminated with Master-Abort. Type 0 configuration cycle is when AD[1::0] = 00.

In Figure 9.38, **DEVSEL#** is not asserted until the 4th clock after the 1st **FRAME#**, violating the SLOW decode timing requirements.

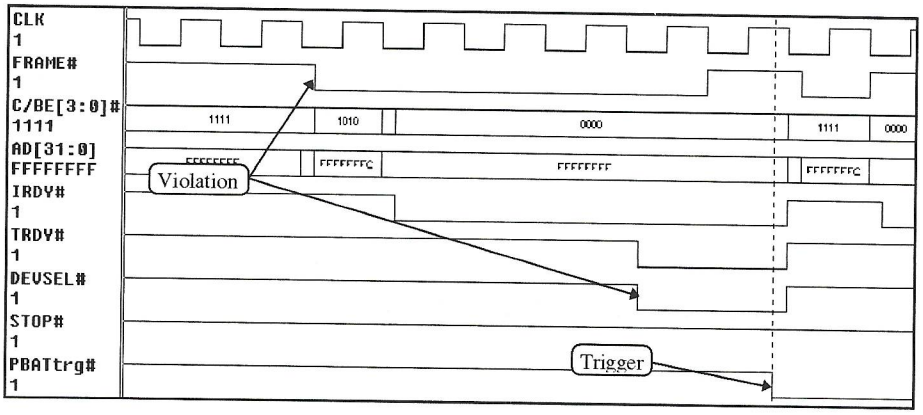


Figure 9.38 SUB decode is not allowed in Config. 0 cycles

PCI Spec. 2.1 Section 3.7.4

9.29 BE[3::0]# Change in Data

Byte Enables must be valid throughout each data phase independent of the state of **IRDY#**. **IRDY#** can be de-asserted to add wait states, but Byte Enables must remain valid prior to actual data transfer.

A data phase cannot be completed before **TRDY#** is asserted, so **BE[3::0]#** must be valid until **TRDY#** is asserted regardless of the **IRDY#** state. This is clearly not the case in Figure 9.39.

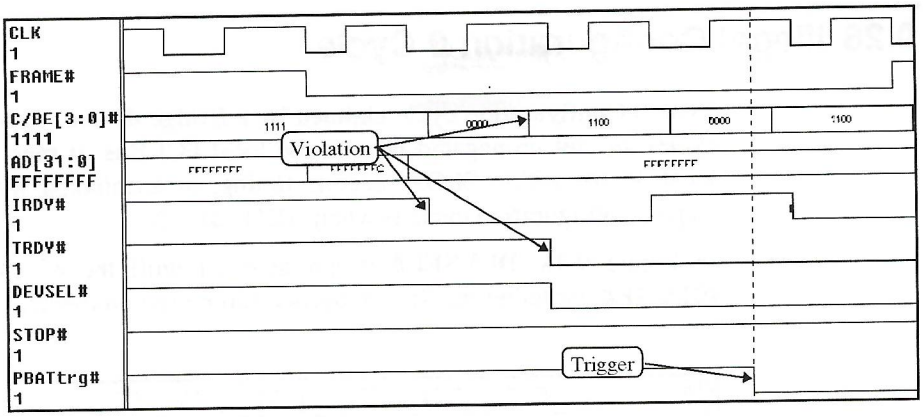


*Figure 9.39 **BE[3::0]#** must be valid regardless of **IRDY#** state*

PCI Spec. 2.1 Section 3.2.3

Section 3.3.1

9.30 PERR# only on Data Transfer

PERR# must be reported 2 clocks after the data transfer in which the error occurred.

Write transaction

PERR# can be asserted prior to the actual transfer in which an error occurred when **IRDY#** is asserted and the target is inserting wait states.

Read transaction

PERR# can be asserted prior to the actual transfer in which an error occurred when **TRDY#** is asserted and the master is inserting wait states.

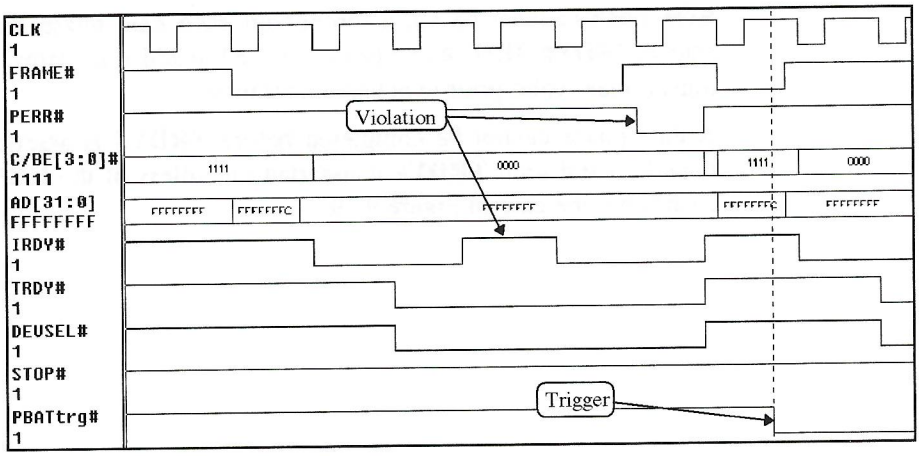


*Figure 9.40 **PERR#** reports an error from a cycle with no data transfer*

PCI Spec. 2.1 Section 3.8.2.1

9.31 Too Many Clocks in Cycle

Initial Data Transfer must complete in 16 clock cycles, and each successive data transfer within 8 clock cycles.

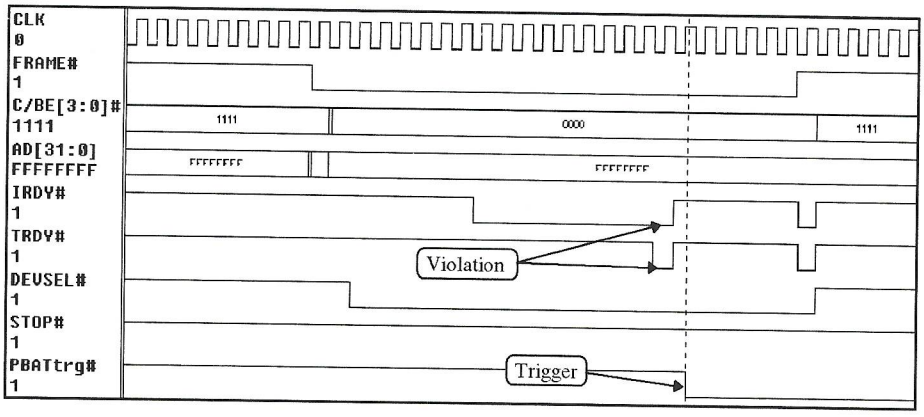


Figure 9.41 Initial Data Transfer has too many (17) clock cycles

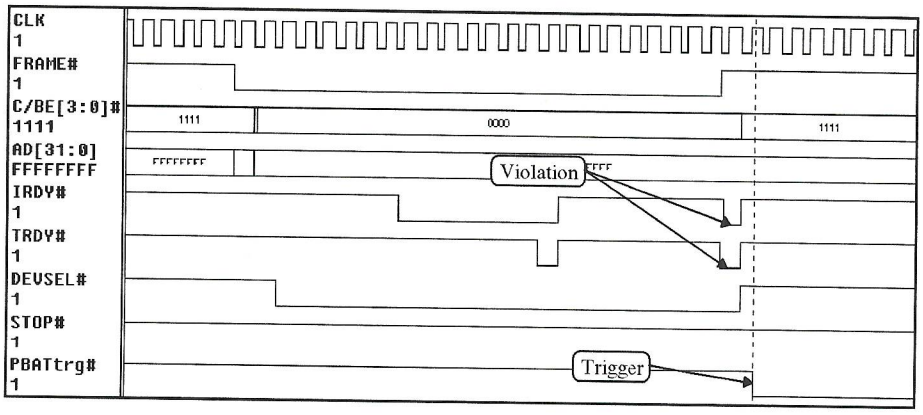


Figure 9.42 Second Data Transfer has too many (9) clock cycles

PCI Spec. 2.1 Section 3.5.3.1

Page 248 Rule 25, 26

9.32 Missing Master Abort

The master must terminate a cycle when **DEVSEL#** is not asserted on the 4th **CLK** after the 1st **FRAME#**.

In Figure 9.43, **DEVSEL#** is not asserted until the 5th clock after the 1st **FRAME#**, and thus the master should have terminated the cycle.

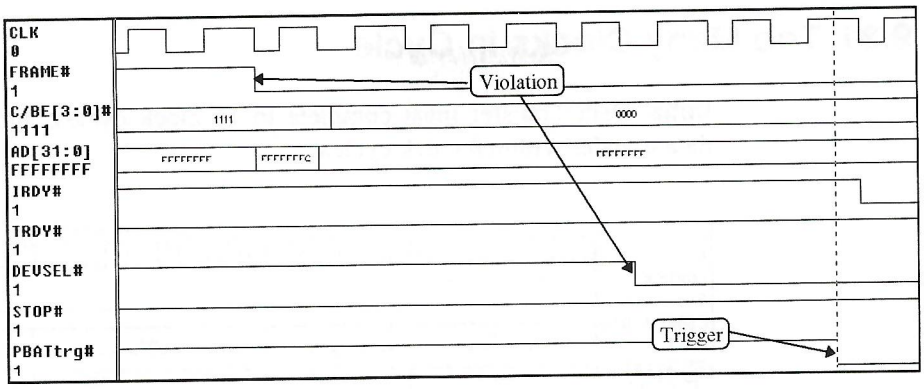


Figure 9.43 Master Abort is missing

PCI Spec. 2.1 Section 3.7.1

9.33 Illegal Master Abort

If **DEVSEL#** is asserted, Master Abort is not permissible.

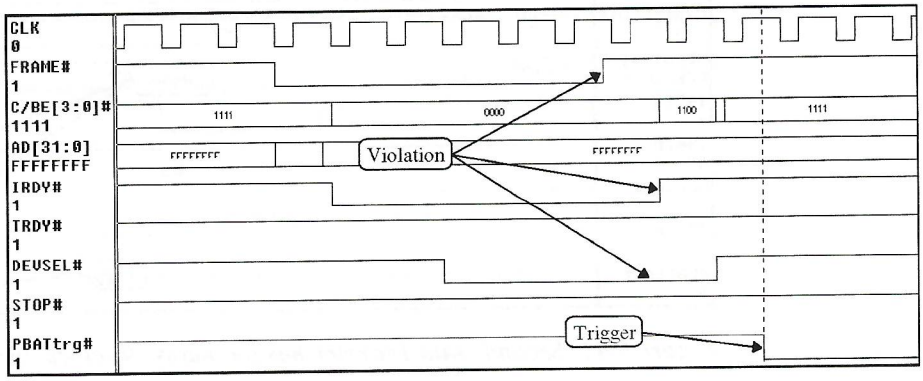


*Figure 9.44 Illegal Master Abort, **DEVSEL#** is asserted*

PCI Spec. 2.1 Section 3.3.3.1

9.34 Illegal Back-To-Back

DEVSEL#, TRDY# or **STOP#** must be de-asserted the clock following the completion of the last data phase. If they remain asserted for an additional clock, as shown in Figure 9.45, a fast Back-To-Back cycle is not allowed.

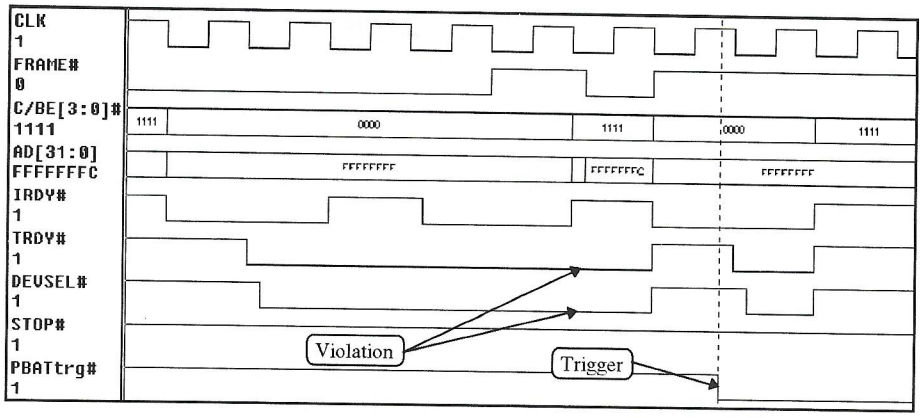


*Figure 9.45 **TRDY#** should not be asserted*

PCI Spec. 2.1

Page 247 Rule 12f

9.35 Clock < 28.5ns

Minimum clock period for 33.33MHz is 30ns.

Note! The minimum clock period must not be violated for any single clock cycle.

9.36 Data Phase Parity Error

PCI bus **PAR** does not correctly reflect the parity of **AD[31::0]** and **C/BE[31::0]** in the data phase. **PAR** is reported the clock after the data phase. The number of ones on **AD[31::0]**, **C/BE[31::0]**, and **PAR**, should equal an even number.

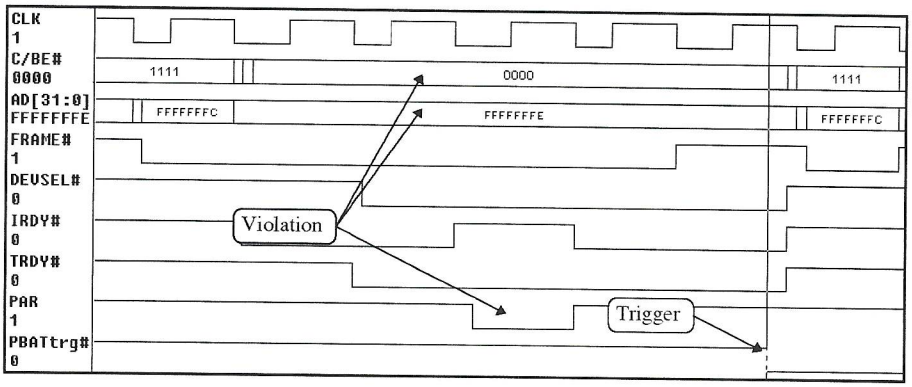


Figure 9.46 Data phase parity error

PCI Spec. 2.1 Section 3.8.1

9.37 Address Phase Parity Error

PCI bus **PAR** does not correctly reflect the parity of **AD[31::0]** and **C/BE[31::0]** in the address phase. **PAR** is reported the clock after the address phase. The number of ones on **AD[31::0]**, **C/BE[31::0]**, and **PAR**, should equal an even number.

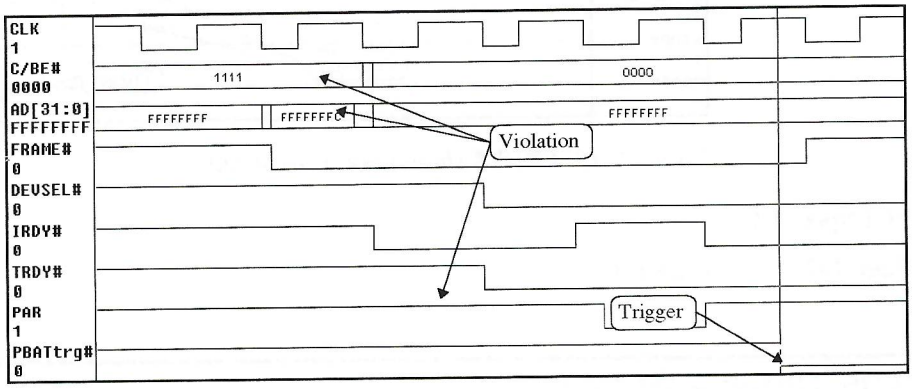


Figure 9.47 Address phase parity error

PCI Spec. 2.1 Section 3.8.1

9.38 Master Abort

Master Abort is not a violation, but trigger output will be generated to detect such cycles.

PCI Spec. 2.1 Section 3.3.3.1

9.39 Target Abort

Target Abort is not a violation, but trigger output will be generated to detect such cycles.

PCI Spec. 2.1 Section 3.3.3.2.1

9.40 RST# Asserted

PCI bus **RST#** asserted is not a violation, but trigger output will be generated to indicate **RST#** active on bus.

PCI Spec. 2.1 Section 2.2.1

10. TERMINAL USER INTERFACE

10.1 Differences from BusView

The main difference from controlling the PTIMBAT400 from BusView to controlling it from VT100 (or some other terminal emulator) is the lack of a mouse. Everything is controlled from the keyboard. Figure 10.1 shows how to switch between the different screens. Underlined keys are accelerator keys that can be used instead of the cursor keys and carriage return.

Note! For a thorough description of how to edit and control the PTIMBAT400 using the Terminal User Interface, please refer to the PBT-415 User's Manual, Chapter 9.

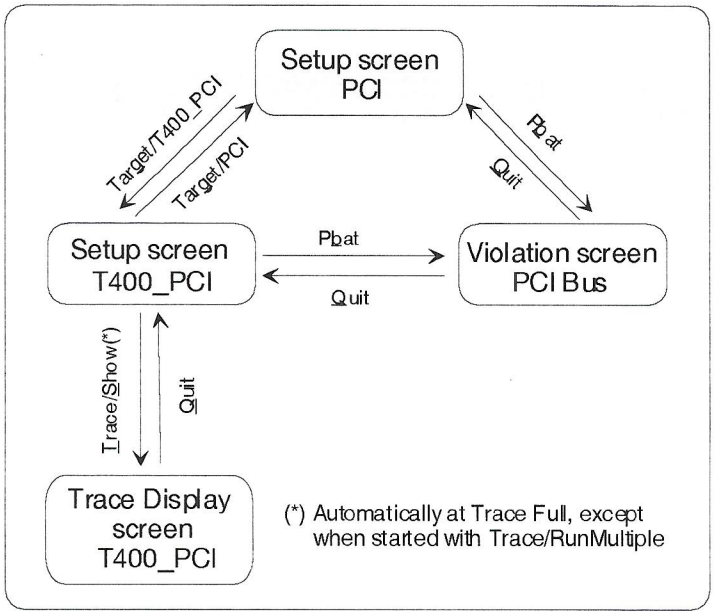


Figure 10.1 Screen control using the Terminal User Interface

10.2 Commands

There are very few commands that differ from the commands in BusView. In the Setup screen a new menu bar item has occurred, the `Target` menu bar item. The `Target` menu enables switching between the PCI Setup screen and the T400_PCI Setup screen, as shown in Figure 10.1.

Typing a `b` switches to the PBAT66 screen. The PBAT66 screen is shown in Figure 10.2, and contains the list of violations.

Selecting violations

Placing the cursor in the PBAT66 screen is done by typing `m` for `Mask`, followed by an `s` for `Select`. Move around with the cursor keys, and use the `SPC` key to toggle violations on and off.

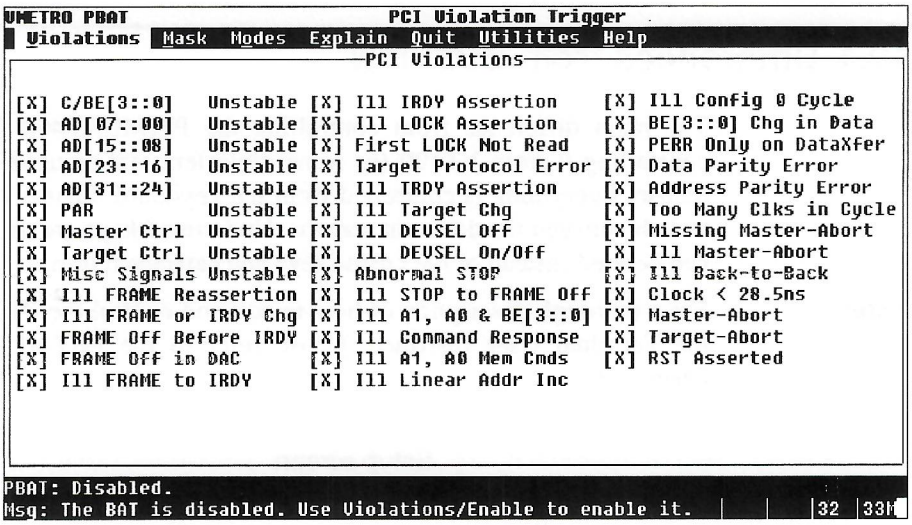


Figure 10.2 The PBAT66 screen

Explanations to violations

An explanation to a violation is shown by selecting a violation, as described above, and then typing an `x` for `Explain`, or CR. A pop-up window appears describing the selected violation.

Violations are highlighted

A violation that is occurring on the bus is highlighted, either in inverse video (as in Figure 10.2), or with high intensity. The preferred option is selected in the `Modes` menu.

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