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REED25

25-Channel Dry-Reed Relay IP Module Hardware Reference

Document No. B-T-MR-REED25##-A-0-A2

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's 25-channel dry-reed relay IP Module, referred to as the REED25, which contains 25 independent contact sets (part number BHAS-REED25).

1.1.2 Scope

This reference manual covers the physical and operational description of the REED25, from both hardware and software perspectives. It also contains detailed technical information about the performance characteristics of the REED25, and some typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Conventions

- Called functions are italicized: *OpenConnect()*.
- Data types are italicized: *int*.
- Function parameters are bolded: **Action**.
- Path names are italicized: *utility/sw/cfg*.
- File names are bolded: **config.c**.
- Path file names are italicized and bolded: ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix; for example 0x7E.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded.

```
c:\>ls
file1           file2               file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.
- An 'Active Low' signal on a hardware product has a slash (/) prefix; for example, /SYNC.

1.2 Related Information

- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)
- ANSI/VITA 4-1995 published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA.

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Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain, and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

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- E-mail: **support@systran.com**
- Fax: **(937) 252-1349**

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- E-mail: i**nfo@systran.com**
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2. PRODUCT OVERVIEW

2.1 Overview

The REED25 is a singlewide IP Module board, conforming both mechanically and electrically to the ANSI /VITA 4-1995. For a typical quad-IP Module carrier, it can provide up to 100 independent sets of form-A dry-reed-relay contacts for a single slot on a computer bus backplane, or be mixed with other IP Modules for a more customized, modular I/O system solution. When used with the VMESC5 carrier, Systran's five-slot IP Module carrier, up to 125 relay contacts can be used in a single VME6U slot.

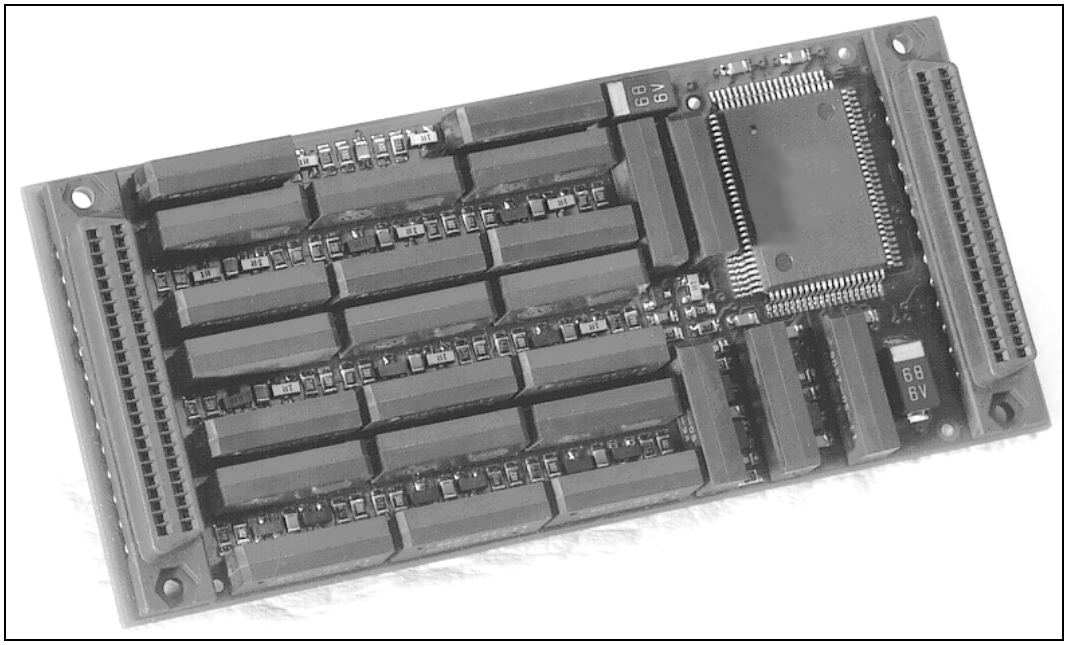


Figure 2-1 REED25 Board

2.2 Features

- 25 Single-pole, single-throw, Form-A dry-reed relays.
- Two 16-bit write/read-back registers with no wait states.
- Maximum current carrying capacity of 1 Amp per channel.
- Maximum switching current capability of 0.5 Amp per channel.
- Ultra-small size → highest possible density.

2.3 Related Products

Software: 'C' library and OS-9 device driver routines and documentation.
ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

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2.4 Block Diagram Description

NOTE: The IP Module signal references, transfer and cycle types discussed in this document are explained in detail in the ANSI/VITA 4-1995 IP Module Specifications.

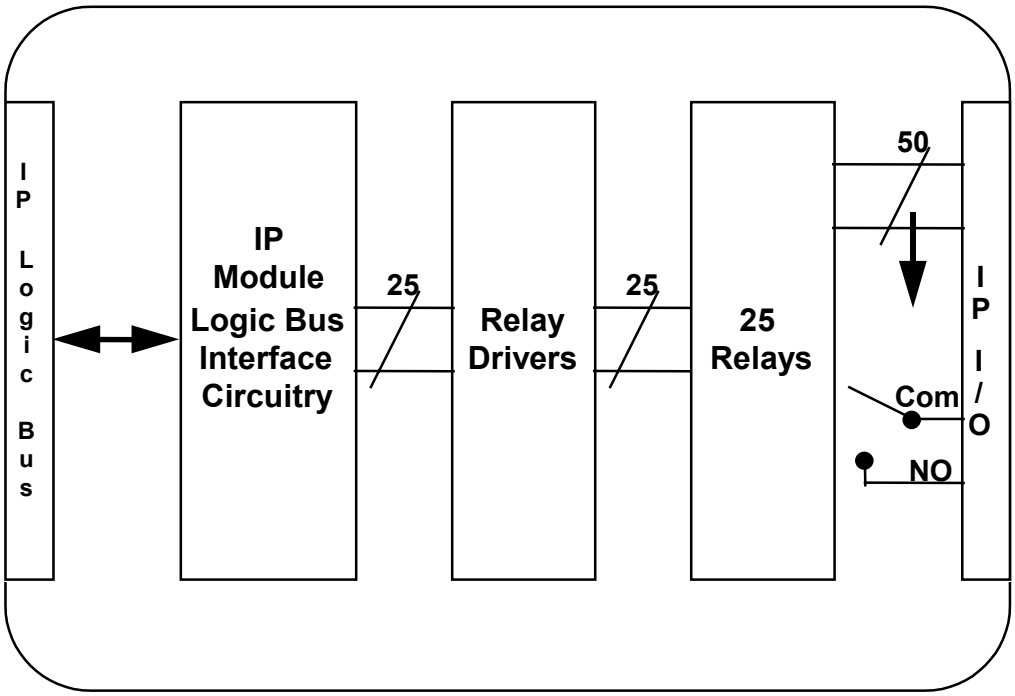


Figure 2-2 Top-Level Block Diagram

Due to the simplicity of this product, there is only a simplified block diagram of the REED25, as presented in Figure 2-2. On the left side is the IP Logic Bus connector through which all transfers between the IP Module carrier and the REED25's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface Circuitry" contains the write/read-back data register, the ID "PROM" data, and IP Module transfer sequence/control and data bus interface logic. This block is completely implemented with a single EPLD device.

The block labeled "Relay Drivers" consists of 25 npn transistors, which are used to energize/de-energize the relays.

The block labeled "25 Relays" contains 25 reed relays, each with form-A contacts, consisting of a "common" and "normally open" pair of contacts. These 50-relay contacts are directly connected to the block (connector) labeled "IP I/O".

2.5 Detailed Description

The REED25 was developed using VHDL and Synthesis, targeted to Altera EPLDs, schematic captured and integrated into standard logic devices, connectors and discrete components using VIEWlogic and associated packages.

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2.5.1 Relay Details

The relays are general-purpose grade dry-reed relays with a 5 V coil. These relays also have a coil suppression diode (1N4148 or equivalent) in parallel to the coil. The REED25 reduces magnetic interaction between adjacent relays using magnetically shielded relays, orienting the poles of adjacent rows in opposite directions, and maximizing the distance between the rows. The magnetic shielding of the relays also reduces potential EMI interference in the I/O subsystem.



NOTE: Due to the permanent magnet-polarization architecture used in these relays, exercise care in the placement of this board in close proximity to strong, external magnetic fields, such as those found near power transformers, large magnets (some motors, speakers, etc.) since operational characteristics may be affected.

2.5.2 Contacts

The rated switching voltage is 200 V for both DC load and AC resistive load. The maximum switching current is 0.5 A, while the maximum carrying current is 1.0 A. The maximum initial static resistance is 0.150 Ω, while the maximum dynamic contact resistance is 0.200 Ω. The minimum insulation resistance is 10^{12} Ω.

2.5.3 High Frequency

When using relays to switch high-frequency signals, the signals may leak through the stray capacitance across the contact, even if it is open. The manufacturer's rating for the typical capacitance across open contacts with the coil grounded is 0.1 pF. The rated capacitance between the open contact and coil, as well as closed contact to coil, is 2.0 and 4.0 pF, respectively. These figures, used in a high-frequency response analysis, can help determine if the REED25 is well suited for a particular application.

2.5.4 Contact-Protection Circuits

When the relay contacts of this product are used to switch inductive loads, such as other relay coils, motors, transformer primaries/secondaries, clutches, lamp ballasts, valves, solenoids, etc., it is always important to protect the contacts by absorbing the voltage surges induced when these loads are switched off. This counter EMF is usually in the hundreds, and sometimes thousands of volts range, and is the primary contributor to contact failure via oxidation, or welding in extreme cases. There are many ways of accomplishing this task; some good, some accepted and not very good, and some never-to-be-used techniques.

One protection technique is the use of a capacitor in parallel with the relay contacts in series with an inductive load. This is effective for arc suppression when the relay contacts open. However, the contacts are susceptible to welding when closed. This occurs when the energy stored in the capacitor when the contacts are open discharges when the relay contacts are closed. The protection technique of placing a capacitor in parallel with the load has similar results. While useful in minimizing arc across the relay contacts as they open, the contacts are susceptible to welding since charging current flows to the capacitor when the relay contacts close.

A safer, acceptable technique involves placing a series resistance in the capacitor leg of the circuits described above. This technique requires a good understanding of the load characteristics, or a lot of test/experimentation. A general guide for resistor and capacitor

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selections might be to select a resistance such that there is approximately 0.5 to 1.0 Ω per volt across the open contacts, and about 0.5 to 1.0 µF per ampere of current through the closed contacts.



NOTE: If the RC network is across the relay contact (instead of across the load) then care must be taken that the load impedance is significantly smaller than that of the RC network for AC applications. The RC network could lengthen the release time of a relay-type load for applications with the RC network in parallel with the load.

For DC applications (not easy to accomplish for AC circuits), a diode can be placed in parallel with the inductive load to protect the relay contacts against excessive counter EMF conditions and their resultant failure modes. This is accomplished by connecting the diode's cathode to the positive load connection, and the anode to the negative load connection. The diode should have a reverse breakdown voltage rating of at least ten times the circuit voltage with a forward current rating at least as large as the load current. Also, this diode protection scheme lengthens the relay-type release time significantly (typically 5 to 10 times normal).

A simple modification to the last (diode) protection scheme speeds up the release time significantly. By connecting a zener diode between the anode of the "regular" diode and the negative load connection (zener's anode → diode's anode; zener's cathode → load's negative connection), the relay contacts are protected and maintain good response characteristics. The zener diode's "zener voltage" should be about the same as the load's supply voltage. This protection scheme is for DC applications only

A highly recommended scheme that works well for all DC and AC applications for inductive loads involves the placement of a varistor in parallel with the inductive load. The use of a varistor only slightly increases the release time.

Obviously, not all loads are primarily inductive in nature. Lamps, and capacitive loads present an inverse problem. Relay contacts must supply massive amounts of start-up or in-rush current when turning on these kinds of loads. Large currents flowing through closing contacts often result in welded (together) contacts. The most common technique for protecting relay contacts for loads with high in-rush current characteristics is to place inductance (choke, coil) and/or resistance in series with the load to limit the initial turn-on current to a level that the relay contacts can safely handle.

Some typical, very generalized, in-rush current to running current ratios might be: purely resistive load ≈1; sodium vapor lamp load ≈1→ 3; mercury vapor lamp load ≈3 → 5 (for up to 5 minutes); motor loads ≈5 → 10 (for up to 500 ms); transformer loads ≈5 → 15; incandescent lamp and solenoid loads ≈10 → 20 (for up to 300 ms); capacitive loads ≈20 → 40 (for up to 33 ms).

It is important to place the protection circuitry as close to the load or the relay contacts as is physically possible to maximize protection. Increased distances will diminish the effectiveness of the protection devices due to increased impedances caused by connection wires. If long wires must be used, it is recommended that series resistance is included to counter the effects of the increased circuit capacitance added by the wiring.

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2.5.5 REED25 Cleaning

If, for some reason, this product requires cleaning, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol.



CAUTION: Do NOT use gasoline or thinner type solvents to clean this product.

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3. INSTALLATION

3.1 Unpack the REED25

The contents of the REED25 shipping packages are listed in Table 3-1.

Table 3-1 Contents of REED25 Shipping Packages

Qty	Description
1	REED25 Printed Circuit Assembly
1	REED25 User Manual *

* One manual is shipped for each board ordered. You may purchase extra manuals by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number. (for example, BTMR- REED25).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Visually Inspect the REED25

Examine the REED25 to determine if any damage occurred during shipping.

3.3 Install the REED25



NOTE: The REED25 is an Electrostatic Sensitive Device (ESD). Therefore the hardware installation of the REED25 must be conducted on a good anti-static workbench to protect the IP Module and carrier boards. The IP Module carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the REED25 can be completed.

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The tools required for the REED25 installation are listed in Table 3-2.

Table 3-2 REED25 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

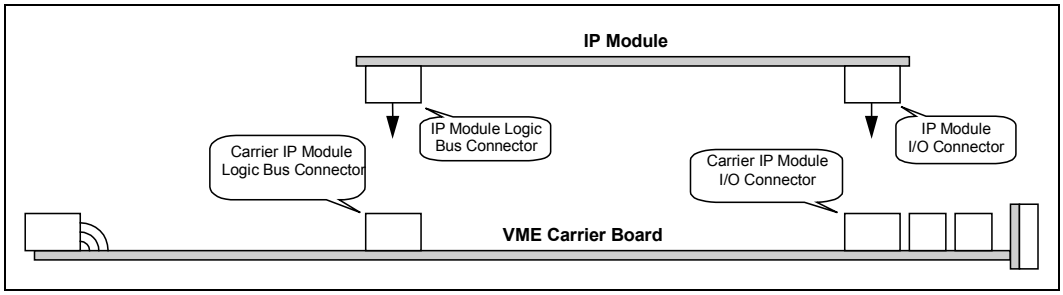


Figure 3-1 REED25 Installed on a VME IP Module Carrier

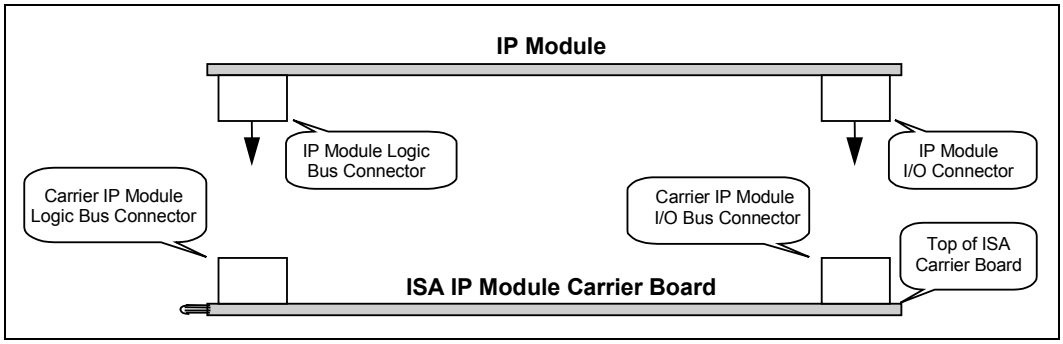


Figure 3-2 REED25 Installed on an ISA IP Module Carrier

Figure 3-1 shows the REED25 installed on a VME IP Module carrier, and Figure 3-2 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board hardware reference manual for more information.

Perform the following steps referring to the appropriate figures and table described above. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the installation of the REED25 can be made.
3. Remove the REED25 from the shipping package and place it on the ESD bench.

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4. Install the REED25 onto the carrier board by applying adequate and equal pressure to the REED25 board at both ends.
*5. Install four M2x5 mm flat head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the REED25 to the carrier board.

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Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
Intreq1*	44	N_INTREQ1
A4	43	IPA4
intreq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

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Table 3-4 IP Module I/O Connector Pin Assignments

IP Module Logic Bus Pin #	Signal Names
50	RLY24NO
49	RLY24COM
48	RLY23NO
47	RLY23COM
46	RLY22NO
45	RLY22COM
44	RLY21NO
43	RLY21COM
42	RLY20NO
41	RLY20COM
40	RLY19NO
39	RLY19COM
38	RLY18NO
37	RLY18COM
36	RLY17NO
35	RLY17COM
34	RLY16NO
33	RLY16COM
32	RLY15NO
31	RLY15COM
30	RLY14NO
29	RLY14COM
28	RLY13NO
27	RLY13COM
26	RLY12NO
25	RLY12COM
24	RLY11NO
23	RLY11COM
22	RLY10NO
21	RLY10COM
20	RLY9NO
19	RLY9COM
18	RLY8NO
17	RLY8COM
16	RLY7NO
15	RLY7COM
14	RLY6NO
13	RLY6COM
12	RLY5NO
11	RLY5COM
10	RLY4NO
9	RLY4COM
8	RLY3NO
7	RLY3COM
6	RLY2NO
5	RLY2COM
4	RLY1NO
3	RLY1COM
2	RLY0NO
1	RLY0COM

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4. PERFORMANCE

4.1 Overview

The figures in this section are a collection of typical rise/fall, and board response times to various system stimuli and IP Module cycles.

Timing measurements were conducted on the REED25 (serial #100) using an HP model 16500A Logic Analyzer with a 1GHz Timing Master Module, model 16515A in slot C. The REED25 was installed in the IP Module slot 'A' of a Motorola MVME-162-01 VME processor IP Module carrier board. Figure 4-1 shows the test configuration for the oscilloscope and state timing measurements.

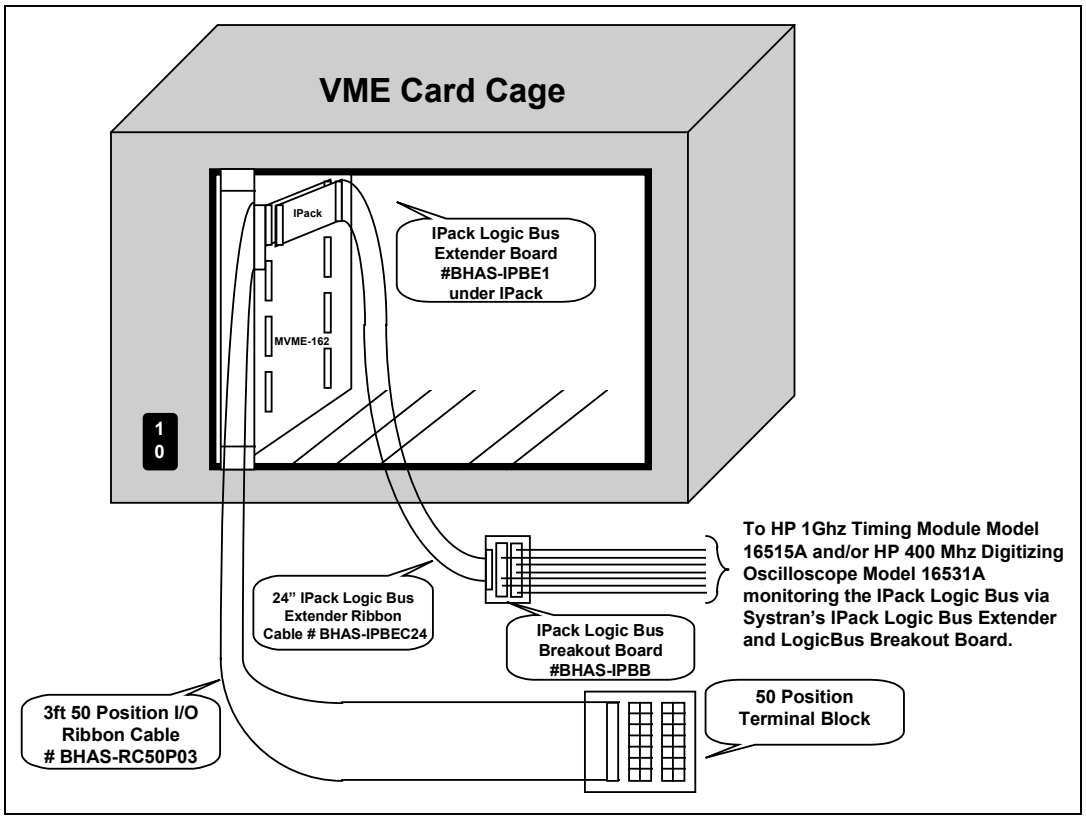


Figure 4-1 IP Module Test Configuration for Oscilloscope and State Timing Measurements

4.2 Performance Measurements

There are three basic sets of performance measurements being presented:

- IP Module access times
- Relay attack and release times
- Contact break-to-make and bounce times

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At least one representative analyzer snapshot is presented for each type of measurement, and all values are tabulated.



NOTE: These measurements are typical results at room temperature for the unit under test, and consequently do not represent "worst case" specifications.

All signals, except "RCOM0", were retrieved from the IP Module Logic Bus Breakout Board (BHAS-IPLBB) as shown in Figure 4-1. On the 50-position terminal block at the end of the three-foot I/O cable, pin #2 was grounded, and pin #1 (RCOM0) was pulled high to an external +5 Vdc power source through a 1KΩ resistor.

4.3 IP Module Access Times

Figure 4-2 presents a typical logic state analyzer snapshot of an ID transfer. The first rising edge of ICLK is the beginning of the ID select cycle. The second rising edge of ICLK is the start of the termination cycle when this IP Module drives the IPD bus (only IPD0 is shown), and asserts the N_ACK signal. Table 4-1 shows the IP Module access times.



NOTE: The IPD bus has weak pull-ups on its signal lines that eventually float high a couple of ICLK cycles following the end of the 125 ns termination cycle.

This IP Module tristates its IPD bus drivers at the same time it negates N_ACK.

Table 4-1 IP Module Access Times, ID READ

Parameter/Event	Typical Time (ns)
ICLK ↑ to IPD0 ↓ High impedance to logic low	12
ICLK ↑ to N_ACK ↓ (Assertion)	8
ICLK ↑ to N_ACK ↑ (Negation)	7

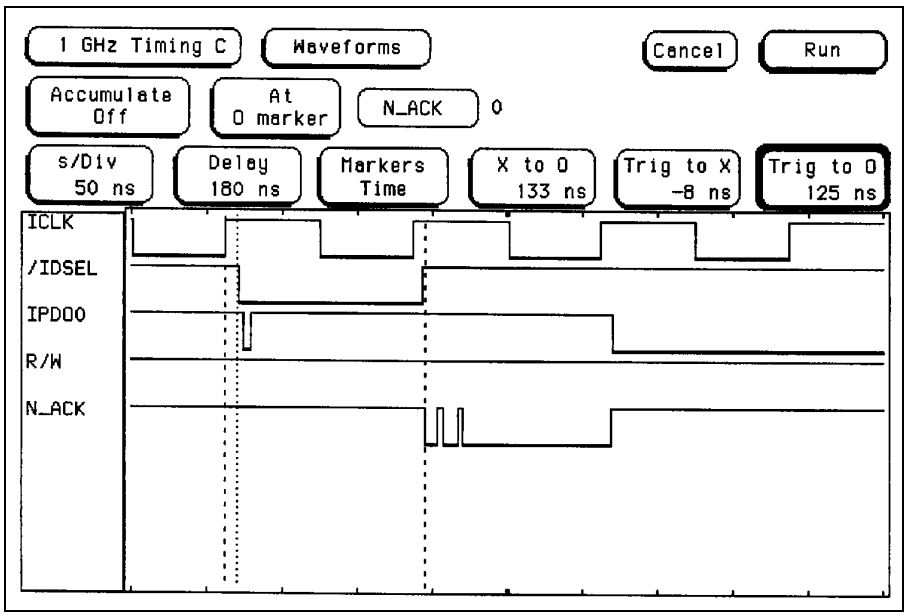


Figure 4-2 Typical Logic State Analyzer Snapshot of an ID Transfer

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Similarly, Figures 4-3 and 4-4 demonstrate typical I/O read and I/O write cycles. Tables 4-2 and 4-3 show the IP Module access times for I/O read and I/O write cycles, respectively.

Table 4-2 IP Module Access Times, I/O READ Cycle

Parameter/Event	Typical Time (ns)
ICLK to IPD0 High impedance to logic low	14
ICLK to N_ACK (Assertion)	8
ICLK to N_ACK (Negation)	8

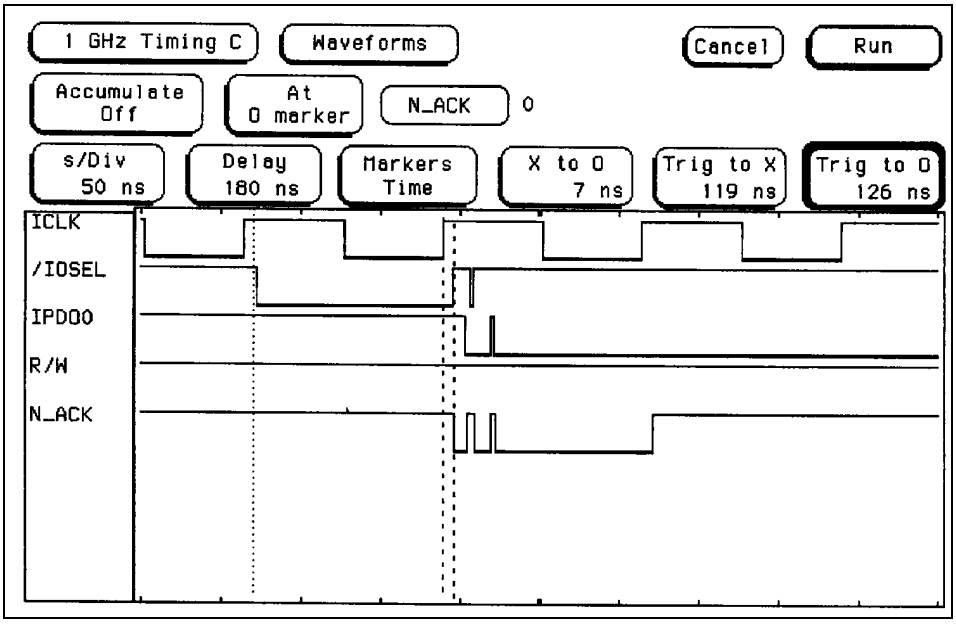


Figure 4-3 Typical Logic State Analyzer Snapshot of an I/O Read Cycle

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Table 4-3 IP Module Access Times, I/O Write Cycle

Parameter/Event	Typical Time (ns)
ICLK to N_ACK (Assertion)	7
ICLK to N_ACK (Negation)	7

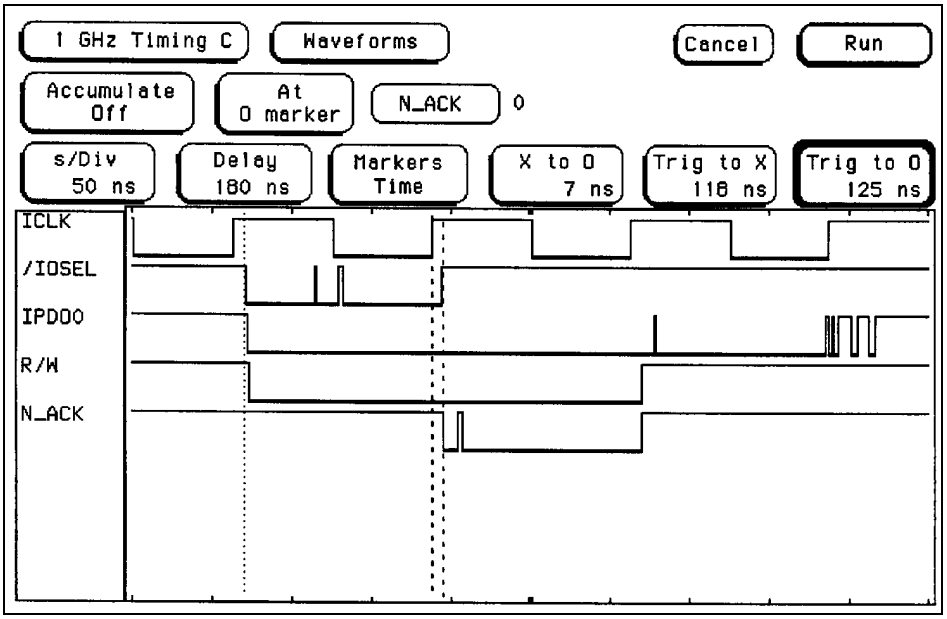


Figure 4-4 Typical Logic State Analyzer Snapshot of an I/O Write Cycle

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4.4 Relay Attack and Release Times

Figure 4-5 presents a typical logic analyzer snapshot that captures the relay's attack times, including the relay driver delays.

The second set of signal assertions (between the first and second time markers in Figure 4-5) are those captured during the automatic read/verify operation performed after the write that caused the relay to change state.

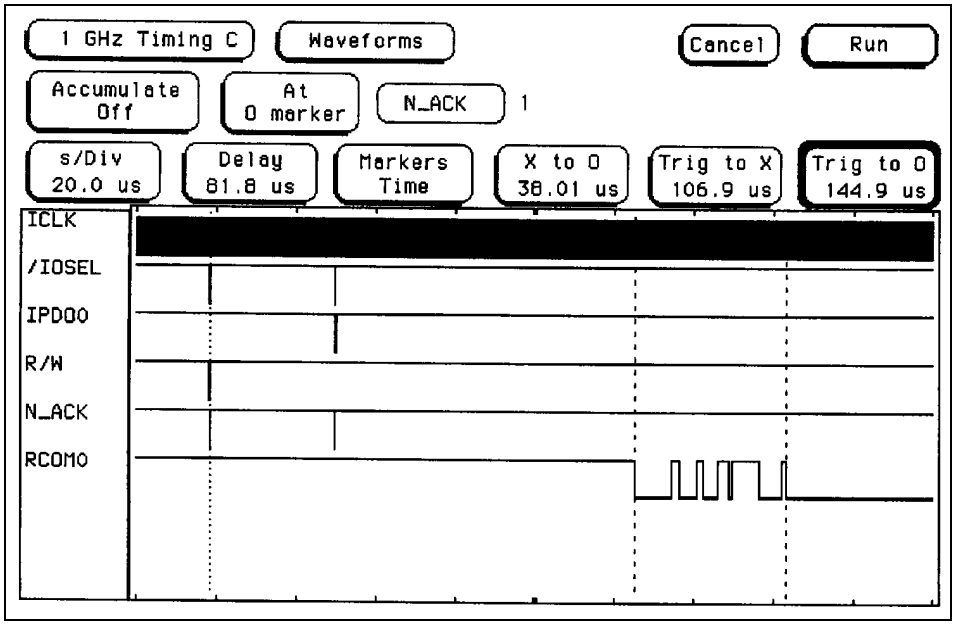


Figure 4-5 Typical Relay Attack Times

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Figure 4-6 presents a snapshot that captures the relay's release times, including the relay driver delays.

As above, the second set of signal assertion is again the result of the automatic read/verify operation performed after the I/O write.

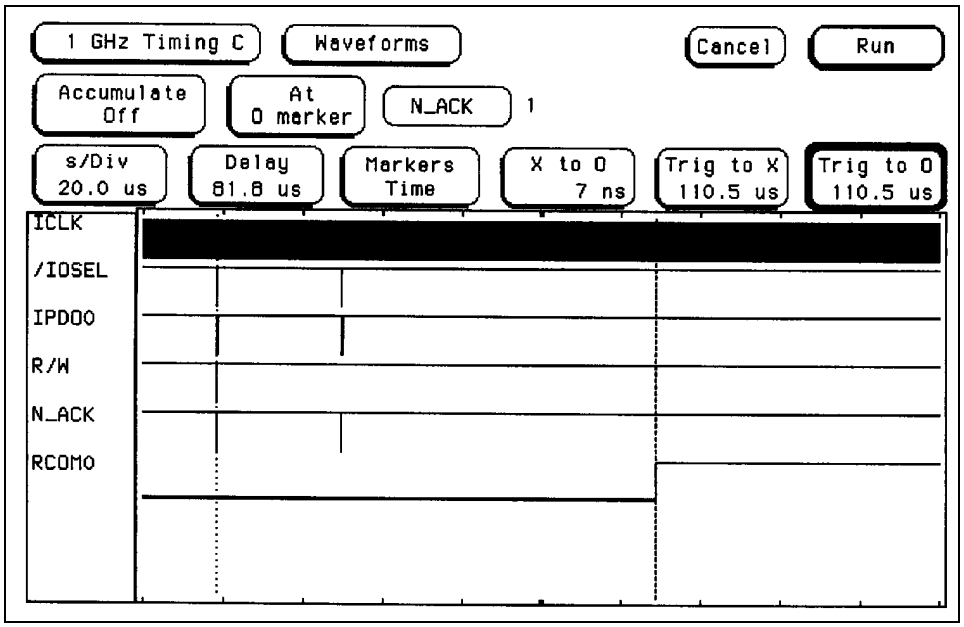


Figure 4-6 Typical Relay Release Times

Table 4-4 Relay Attack/Release Times

Turning Relay	Typical Time To First Make/Break (µs)	
ON	(MAKE)	106.9
OFF	(BREAK)	110.5

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4.5 Contact Bounce Times

Figure 4-5, which captures typical attack times, also presents information about typical contact bounce times (see Table 4-5).



NOTE: There was no measurable "break" bounce time (less than or equal to 1ns).

Table 4-5 Contact Bounce Times

Turning Relay	Event Timed		Typical Time (µs)
ON	MAKE	First to last closure	38.01
OFF	BREAK	Break bounce	0.0

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APPENDIX A

SPECIFICATIONS

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A.1 Specifications

MECHANICAL: SINGLEWIDE IP MODULE

- Measurements: 1.800” x 3.900” x 0.275” (above board)
  4.572 cm x 9.906 cm x .699 cm
- Weight: 1.788 oz, 50.69 grams
- Board thickness: 0.062”, 0.157 cm nominally, (4 layer)

PROTOCOL: SINGLEWIDE IP MODULE TRANSFERS

- 8 MHz clock rate
- No wait cycles on any transfer type
- Hold cycles supported on all valid transfer types
- Complete (no partial) address decoding
- I/O transfers: 8-, 16-bit writes, 16-bit reads
- Two 16-bit I/O locations:
  - Maximum read/write rate: 4 MTransfers/second, sustained
- ID transfers: 8-bit read (only)
  - Zero fill on upper byte
  - Twelve bytes, including CRC
  - Systran’s manufacturer’s ID = 0x45, = “E” ASCII
  - REED25’s model number = 0x6E, “n” ASCII
  - Cyclic Redundancy Check value = 0xAC
  - Maximum read rate: 4 Mtransfers/second, sustained
- Memory transfers: not supported
- Interrupt Vector transfers: not supported
- DMA activity: none supported
- No acknowledgment on unsupported transfer attempts:
  - Memory read and write, Interrupt read, ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

- All relays de-energized (read of all zeros ‘0000’ from both I/O locations)
- No access permitted or acknowledged during RESET

POWER REQUIREMENTS

- Power: +5Vdc @ 78 mA (typical, all relays OFF)
  +5Vdc @ 558 mA (typical, all relays ON)
  +12Vdc @ 0 mA
  -12Vdc @ 0 mA

PERFORMANCE CHARACTERISTICS

- Electrical characteristics: Refer to Section 5.0 on Performance

ABSOLUTE MAXIMUM RATING

- I/O connected relay contacts
  - Maximum switching voltage: 200 Vdc, 200 Vac
  - Maximum switching current: 0.5 A

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  - Maximum carry current: 1.0 A
  - Maximum contact rating: 10 W
- Maximum initial static contact resistance: 0.150 Ω (50 mV @ 10 mA)
- Maximum initial dynamic contact resistance:
  - 0.200 Ω (0.5 V, 50 mA at 100Hz, 1.5 msec)
- Typical capacitance:
  - Across open contacts: 0.1 pF (coil grounded)
  - From open contact to coil: 2.0 pF
  - From closed contact to coil: 4.0 pF
- Dielectric strength minimum
  - Between contacts: 250 Vdc, 250 Vac
  - Contacts to coil: 1500 Vdc, 1500 Vac
  - Shield to coil: 1500 Vdc, 1500 Vac

RECOMMENDED OPERATING CONDITIONS

- Supply voltage: +4.75 V → +5.25 V
- Logic Interface: IndustryPack specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

- Temperature:
  - (Operating): 0 C to +70 C
  - (Storage): -40 C to +85 C
- Humidity (Noncondensing): 5% to 95%
- Vibration (Operating): 10 G's RMS, 20-2000 Hz, random
- Shock (Operating): 50 G's Max.
- Altitude (Operating): 10,000 feet

MEAN TIME BETWEEN FAILURES (MTBF):

- 36,788 hours per MIL-HDBK-217F

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APPENDIX B

TYPICAL APPLICATIONS

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B.1 Applications

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the REED25 IP Module to solve a problem. This appendix will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.1.1 5-to-1 Multiplexer

The REED25 is ideal for switching high frequency signals, such as video. This could be used to direct one of N signals (that is, from different video cameras) to a single destination (a monitor), effectively functioning as an N-to-1 multiplexer.

This example will show how to implement a 5-to-1 multiplexer (mux) for differential signals. Table B-1 illustrates how this could be configured from a single REED25. The table also outlines one possible scheme for connecting the signals to this mux.

Table B-1 5-To-1 Multiplexer Connections

SIGNAL	RELAY #	COMMON PIN #	NORMALLY OPEN PIN #
SIG_1_+	0	1	2
SIG_1_-	1	3	4
SIG_2_+	2	5	6
SIG_2_-	3	7	8
SIG_3_+	4	9	10
SIG_3_-	5	11	12
SIG_4_+	6	13	14
SIG_4_-	7	15	16
SIG_5_+	8	17	18
SIG_5_-	9	19	20

The normally open contacts of the positive signals (relays 0, 2, 4, 6, and 8) are then tied together and connected to the non-inverting output, OUT_+. Similarly, the normally open contacts of the negative signals (relays 1, 3, 5. 7. and 9) are also tied together and connected to the inverting output, OUT_-.

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B.1.2 Programming Example

- At power-up, the Data Registers' values are '0x0000', corresponding to all relays de-energized. No input signal is selected as an output for the multiplexer.
- Write '0x0003' to Data Register 0. Relays 0 and 1 are now energized. The video switch now selects signal 1.
- Write '0x0000' to Data Register 0. All relays are now de-energized.
- Write '0x000C' to Data Register 0. Relays 2 and 3 are now energized. The video switch now selects signal 2.
- Write '0x0000' to Data Register 0. All relays are now de-energized.
- Write '0x0030' to Data Register 0. Relays 4 and 5 are now energized. The video switch now selects signal 3.
- Write '0x0000' to Data Register 0. All relays are now de-energized.
- Write '0x00C0' to Data Register 0. Relays 6 and 7 are now energized. The video switch now selects signal 4.
- Write '0x0000' to Data Register 0. All relays are now de-energized
- Write '0x0300' to Data Register 0. Relays 8 and 9 are now energized. The video switch now selects signal 5.
- Write '0x0000' to Data Register 0. All relays are now de-energized.



NOTE: All relays used are de-energized before selecting a new output using the video switch. This is to allow the contacts of the previously energized relays to "break" before the contacts of the two relays that will be energized "make" a connection. The REED25 does allow multiple relays (up to all 25) to be energized/de-energized at once. However, in this example if the writes of '0x0000' were not made to de-energize the relays, the input signals to the video switch could be momentarily shorted together.

B.2 Matrix Switch

The differential multiplexer (see Figure B-1) can be used in multiples to implement an N-by-M matrix switch. This example will outline the implementation of a 5x5 matrix switch. This allows any of 5 sources to be dynamically connected to any of 5 destinations. The sources could include a wide range of signals, such as those generated by a digital-to-analog converter, waveform generator, or pulse generator. Similarly, the destinations could include a wide range of instruments, such as a voltmeter, frequency counter, oscilloscope, spectrum analyzer, or an A/D front end to a DSP.

Ten 5-to-1 multiplexers are used to form this 5x5 matrix switch as shown in Figure B-2. Each signal (consisting on both a non-inverting and inverting line) is drawn as a single line for simplicity. In addition, each pair of contacts is drawn as a single contact for the same reason. The five source multiplexers (muxes) actually operate as de-multiplexers (de-muxes), each allowing its single input signal to be driven to one of the five outputs. Each of the five outputs of each de-mux is then connected to an input of each of the destination muxes. Each of the five destination muxes selects one of its five inputs as its output. In this fashion, any of the five sources can be arbitrarily connected to any of the five destinations.

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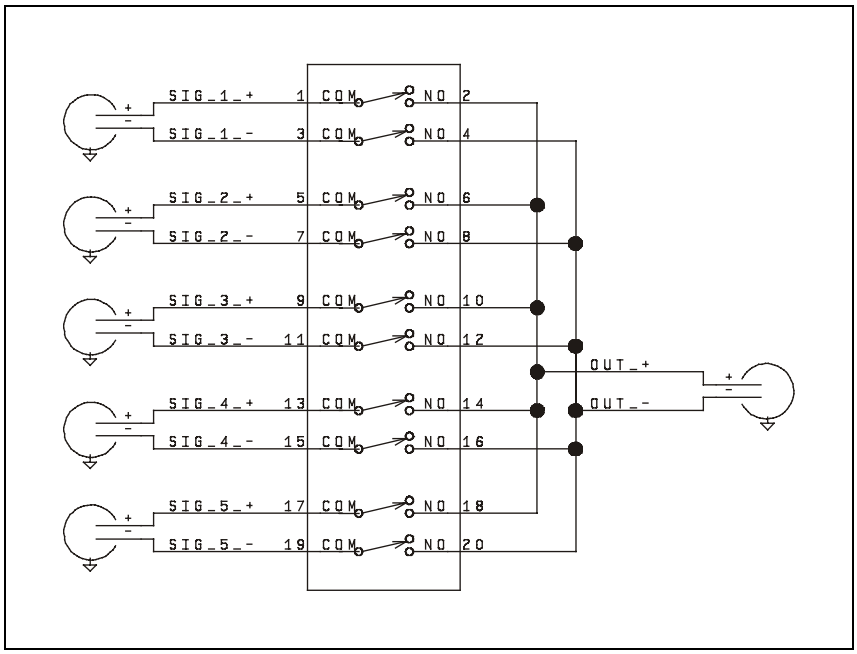


Figure B-1 5-to-1 Differential Multiplexer

NOTE: As is the case with the 5-to-1 multiplexer outlined above, each of the destination muxes must select no more than one of its sources to avoid possibly shorting the input signals. Thus, to select a new signal, put all of the relays into a de-energized state before energizing the two relays which will then select this signal. In this manner, if there is only one pair of contacts closed for each destination mux at a given instant, it is impossible to short the signals to the matrix switch. However, it is recommended practice to only allow the source de-muxes to drive one output each by only allowing one set of contacts to be energized for each de-mux. This will also prevent reducing the drive of the matrix switch's inputs, and will reduce possible ringing by not using the other four lines, which would essentially act like unterminated transmission lines.

Each of the muxes and de-muxes requires five pairs of contacts, or 10 reed relays. Thus, the matrix switch requires a total of 100 reed relays, which can be provided by only four REED25s. However, this is not the ideal situation since the implementation of at least two of the muxes would be divided over multiple REED25s. This would make it potentially more difficult to write software that ensured that only one contact pair for each mux was closed at a given instant. A better approach would be to use five REED25s, with each REED25 implementing two muxes (or de-muxes).

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These concepts can be readily extended to create a matrix of arbitrary size. For example, a 6x2 matrix switch can be implemented by using six 1-to-2 demuxes and two 6-to-1 muxes. A NxM matrix switch requires N 1-to-M demuxes and M N-to-1 muxes, or a total of 2NM sets of contacts. Since differential signals are being switched, this requires a total of 4NM reed relays. In addition, multiple matrix switches can be cascaded to implement even larger matrix switches, but this is beyond the scope of this discussion.

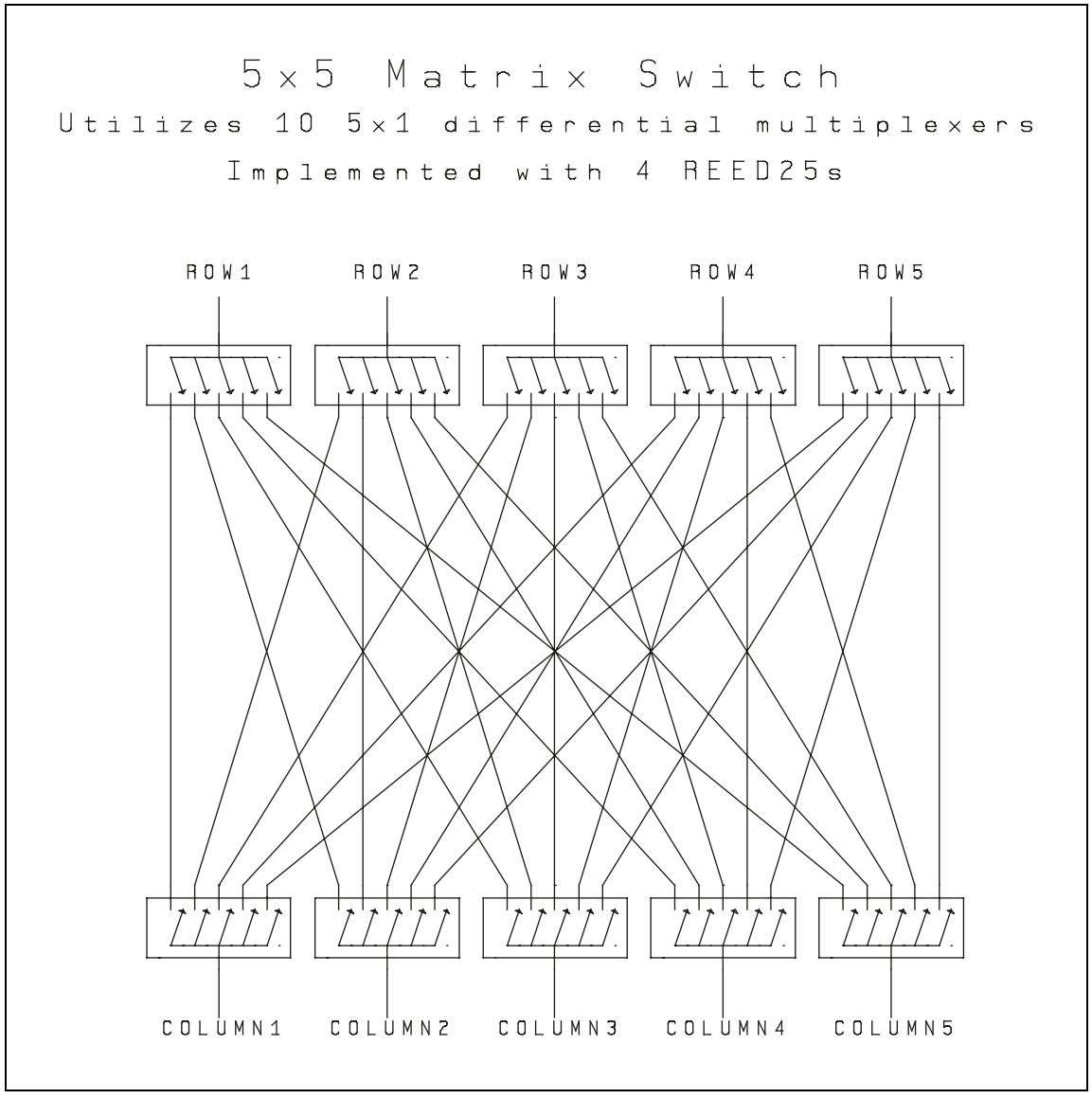


Figure B-2 5 by 5 Matrix Switch

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APPENDIC C

PROGRAMMING GUIDE

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C.1 Overview

This section of the manual describes the operation of the REED25 from the software perspective, detailing the REED25 registers and providing programming examples. A more detailed description of the hardware can be found in Chapter 2, PRODUCT overview, and Appendix B, TYPICAL APPLICATIONS.

C.2 Description

The REED25 is a simple-to-use IP Module card with 25 SPST dry-reed relays. All 25 relays are controlled (energized/de-energized) by writing to one of two 16-bit registers. When a relay is de-energized, the normally open contacts are open. When a relay is energized, the normally open contacts are closed.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible, due to the never-changing information it presents. It saves space, lowers costs, improves reliability, and enables this IP Module to provide "no-wait" read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) READs as all zeroes during valid ID READ-only accesses.

Table C-1 is the REED25 emulated ID Address Space PROM listing.

Table C-1 REED25 ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0X00	ASCII "I"	0x49
IPA = 0X01	ASCII "P"	0x50
IPA = 0X02	ASCII "A"	0x41
IPA = 0X03	ASCII "C"	0x43
IPA = 0X04	SYSTRAN's ID	0x45
IPA = 0X05	REED25's Model Number	0x6E
IPA = 0X06	Revision Level	0x30
IPA = 0X07	Reserved	0x00
IPA = 0X08	Low Byte Driver ID	0x00
IPA = 0X09	High Byte Driver ID	0x00
IPA = 0X0A	Number of Bytes Used	0x0C
IPA = 0X0B	CRC	0xAC

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C.4 IP Module I/O Address Map

The REED25's I/O Address Map contains two registers in the IP Module I/O space (IPA = 0x00 and IPA = 0x01). The address detector circuitry is fully decoded.



NOTE: Any attempt to access I/O addresses at and above 0x02 will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IP Module resides.

Table C-2 is the REED25 I/O Address map and contains two data registers.

Table C-2 REED25 I/O Address Space Listing

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	[15:8]	[7:0]	Data Register 16 bits
IPA = 0x01	[24]	[23:16]	Data Register 16 bits

C.5 Word Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VME BUS Address	PC-AT BUS Address	NuBus Address	IP Module Address
BASE + 0x0	BASE + 0x0	BASE + 0x2	IPA = 0X00
BASE + 0x2	BASE + 0x2	BASE + 0x6	IPA = 0X01
BASE + 0x4	BASE + 0x4	BASE + 0xA	IPA = 0X02
BASE + 0x6	BASE + 0x6	BASE + 0xE	IPA = 0X03
BASE + 0x8	BASE + 0x8	BASE + 0x12	IPA = 0X04
BASE + 0xA	BASE + 0xA	BASE + 0x16	IPA = 0X05
BASE + 0xC	BASE + 0xC	BASE + 0x1A	IPA = 0X06
BASE + 0xE	BASE + 0xE	BASE + 0x1E	IPA = 0X07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0X08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0X09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA = 0X0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0X0B

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C.6 Byte Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VME BUS Address	PC-AT BUS Address	NuBus Address	IP Module Address	Byte-Lane *
BASE + 0x1	BASE + 0x0	BASE + 0x3	IPA = 0X00	0
BASE + 0x0	BASE + 0x1	BASE + 0x2	IPA = 0X00	1
BASE + 0x3	BASE + 0x2	BASE + 0x7	IPA = 0X01	0
BASE + 0x2	BASE + 0x3	BASE + 0x6	IPA = 0X01	1
BASE + 0x5	BASE + 0x4	BASE + 0xB	IPA = 0X02	0
BASE + 0x4	BASE + 0x5	BASE + 0xA	IPA = 0X02	1
BASE + 0x7	BASE + 0x6	BASE + 0xF	IPA = 0X03	0
BASE + 0x6	BASE + 0x7	BASE + 0xE	IPA = 0X03	1
BASE + 0x9	BASE + 0x8	BASE + 0x13	IPA = 0X04	0
BASE + 0x8	BASE + 0x9	BASE + 0x12	IPA = 0X04	1
BASE + 0xB	BASE + 0xA	BASE + 0x17	IPA = 0X05	0
BASE + 0xA	BASE + 0xB	BASE + 0x16	IPA = 0X05	1
BASE + 0xD	BASE + 0xC	BASE + 0x1B	IPA = 0X06	0
BASE + 0xC	BASE + 0xD	BASE + 0x1A	IPA = 0X06	1
BASE + 0xF	BASE + 0xE	BASE + 0x1F	IPA = 0X07	0
BASE + 0xE	BASE + 0xF	BASE + 0x1E	IPA = 0X07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0X08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0X08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0X09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0X09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0X0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0X0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0X0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0X0B	1

* Byte-lane 1 not applicable for ID Space

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C.7 Data Registers Bit Description (IPA=0x00 → 0x01)

The REED25 has two 16-bit-wide registers, with each bit of Data Register 0 and each of the lower 9 bits of Data Register 1 corresponding to a relay. The REED25 supports word (16-bit) reads, and word and byte (8-bit) writes. Byte writes are non-destructive to the adjacent byte. On power-up, all bits are set to zero (all relays de-energized).

C.7.1 Data Register 0 (IPA = 0x00)

Table C-5 Data Register 0 Description

Bit#	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	RL 15	RL 14	RL 13	RL 12	RL 11	RL 10	RL 9	RL 8	RL 7	RL 6	RL 5	RL 4	RL 3	RL 2	RL 1	RL 0
R/W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W	R W
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RL15 - RL0: These bits control the energization of relays 15 to 0. Bit 0 corresponds to relay 0, bit 1 to relay 1, ... , bit 15 to relay 15. If the bit is set to 0, the corresponding relay is de-energized. If the bit is set to 1, the relay is energized.

C.7.2 Data Register 1 (IPA = 0x01)

Table C-6 Data Register 1 Description

Bit#	Bits 15 to 8	8	7	6	5	4	3	2	1	0
Bit Name	Not Used Read as 0's	RL 24	RL 23	RL 22	RL 21	RL 20	RL 19	RL 18	RL 17	RL 16
R/W		RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State		0	0	0	0	0	0	0	0	0

RL24 - RL16: These bits control the energization of relays 24 to 16. Bit 0 corresponds to relay 16, bit 1 to relay 17, ... , bit 8 to relay 24. If the bit is set to 0, the corresponding relay is de-energized. If the bit is set to 1, the relay is energized.

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C.8 Programming Example

The following example illustrates how to program the REED25 device. In the power-up state, all of the relays are de-energized. As previously stated, if a relay is de-energized, the normally open contacts are open. If a relay is energized, the normally open contacts are closed.

- At power-up, the data registers' values are '0x0000' corresponding to all relays de-energized.
- Write '0x0001' to Data Register 0.
- Relay 0 is now energized, all other relays are de-energized.
- Write '0x8000' to Data Register 0.
- Relay 15 is now energized, all other relays are de-energized.
- Write '0xFFFF' to Data Register 0.
- Relays 0 to 15 are now energized, all other relays are de-energized.
- Write '0x0001' to Data Register 1.
- Relays 0 to 16 are now energized, all other relays are de-energized.
- Write '0x01FF' to Data Register 1.
- All relays are now energized.
- Write '0x0000' to Data Register 0.
- Relays 0 to 15 are now de-energized. Relays 16 to 24 are still energized.
- Write '0x0000' to Data Register 1.
- All relays are now de-energized.

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GLOSSARY

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[x:y] ---------- Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane ---------- 8 bits of a data bus on octal boundaries.

doublewide ---------- An IP Module that is twice the size of a singlewide board.

DMA ---------- Direct memory access.

EPLD ---------- Erasable Programmable Logic Device.

ID PROM ---------- The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IP Module logic bus ---------- A synchronous, 4 MTransfers/sec, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

IPDbus ---------- IP Module Data Bus.

ISR ---------- Interrupt Service Routine.

MTBF ---------- Mean Time Between Failures.

npn transistor ---------- A bipolar junction transistor (BJT) consisting of three semiconductor regions: the emitter region (*n* type), the base region (*p* type), and the collector region (*n* type).

ns, µs, ms ---------- Nanoseconds, microseconds, and milliseconds respectively.

singlewide ---------- An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

slew rate ---------- The rate of change in analog output in terms of volts/time.

SPST ---------- Single-pole, single-throw switch.

VHDL ---------- Very high-speed integrated circuit Hardware Description Language.

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