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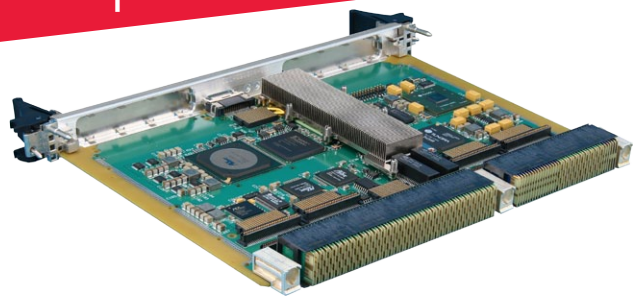




Data Sheet

VPX6-185 VPX

Freescale Power Architecture™ MPC8640/1-based Single Board Computer



Features

- Single or dual-core Freescale Power Architecture™ MPC8640/8641 CPU up to 1.33 GHz
  - x2 e600 processor cores
  - Each core has 64 KB L1 cache
  - Each core has 1 MB L2 cache with ECC
  - 21.3 GFLOPs @1.33 GHz (dual-core)
- MPC8640/1 additional features
  - x2 DDR2 memory controllers with ECC
  - x4 Gigabit Ethernet (GbE) controllers
  - Serial I/O controller
  - x2 I2C channels
  - x2 PCI Express® (PCIe) interfaces
  - x1 Serial RapidIO® (sRIO) interface
  - Integrated DMA controllers
- Up to 2 GB DDR2 SDRAM with ECC
  - Dual-channel memory controllers
- 256 or 512 MB flash with write protection
- Permanent Alternate Boot Site (PABS) provides backup boot capability
- 128 KB AutoStore NVSRAM with hardware write protection
- VITA 46 core fabric with both sRIO and PCIe interfaces
- User configurable
  - Up to four sRIO interfaces up to 3.125 Gbps
  - Up to two PCIe interfaces at 2.5 Gbps
- 4 GbE interfaces
  - x1 front panel - Standard product air-cooled only (configurable backplane)
  - x3 backplane
- x2 XMC/PMC mezzanine sites
  - x1 100 MHz PCI-X PMC or 8-lane PCIe XMC
  - x1 66 MHz PCI-X PMC or 4-lane PCIe XMC
- x4 asynchronous EIA-232 serial ports
- Up to four HDLC/SDLC-capable sync/async EIA-232/422/485 serial channels
- Up to 14 VTTL discrete I/O signals
- Up to 16 EIA-422/485 differential discrete signals (x8 inputs, x8 outputs)
- Multi-board synchronous clock
- 2-channel MIL-STD-1553 option
- 8- or 16-bit SCSI interface option
- 2-channel Serial ATA (SATA) 1.0 option
- x2 USB 2.0 ports
- x6 general-purpose 32-bit timers in Core Functions FPGA
- x4 general-purpose DMA controllers
- x8 31-bit OS timers (MPC864x MPIC), x4 per processor core
- x2 avionics-style watchdog timers

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Features continued

- Real-time clock (RTC) with VBAT switchover
- x4 temperature sensors
- VME64x interface option
- Supports 5V-only operation
- Continuum Software Architecture (CSA) firmware with extensive diagnostics
- VxWorks® 6.x Workbench® 2.x support
- Wind River® Linux® GPP LE 3.x
- Continuum Vector™ DSP library
- Continuum Insights Multi-processor development tools
- Continuum Inter-Processor Communications™ (IPC)
- INTEGRITY® from Green Hills® Software, consult factory for availability
- LynxOS 5.0 from LynuxWorks®, consult factory for availability
- Range of air- and conduction-cooled ruggedization levels available

Overview

The VPX6-185 is one of a family of modules from Curtiss-Wright Controls Defense Solutions to employ the new open-architecture VITA 46 standard. VITA 46, also known as "VPX" was collaboratively developed by COTS industry leaders which included prime military integrators to marry high-speed serial interconnect such as sRIO and PCIe. It is well suited to the military/aerospace which can take advantage of and utilize this form factor and feature set in their demanding applications. The VPX6-185 provides single board computer (SBC) functionality to the Curtiss-Wright VPX family that includes quad-processor DSP, FPGA accelerator and XMC/PMC carrier modules.

The VPX6-185 is based on the MPC8640/1 processor. Available in single-core and dual-core versions with AltiVec™ and up to 2 GB of high-bandwidth DDR2 SRAM, the VPX6-185 provides high-performance processing, the massive 10 GB/s bandwidth of VPX and a long list of features and I/O interfaces to satisfy the most demanding requirements of embedded computing.

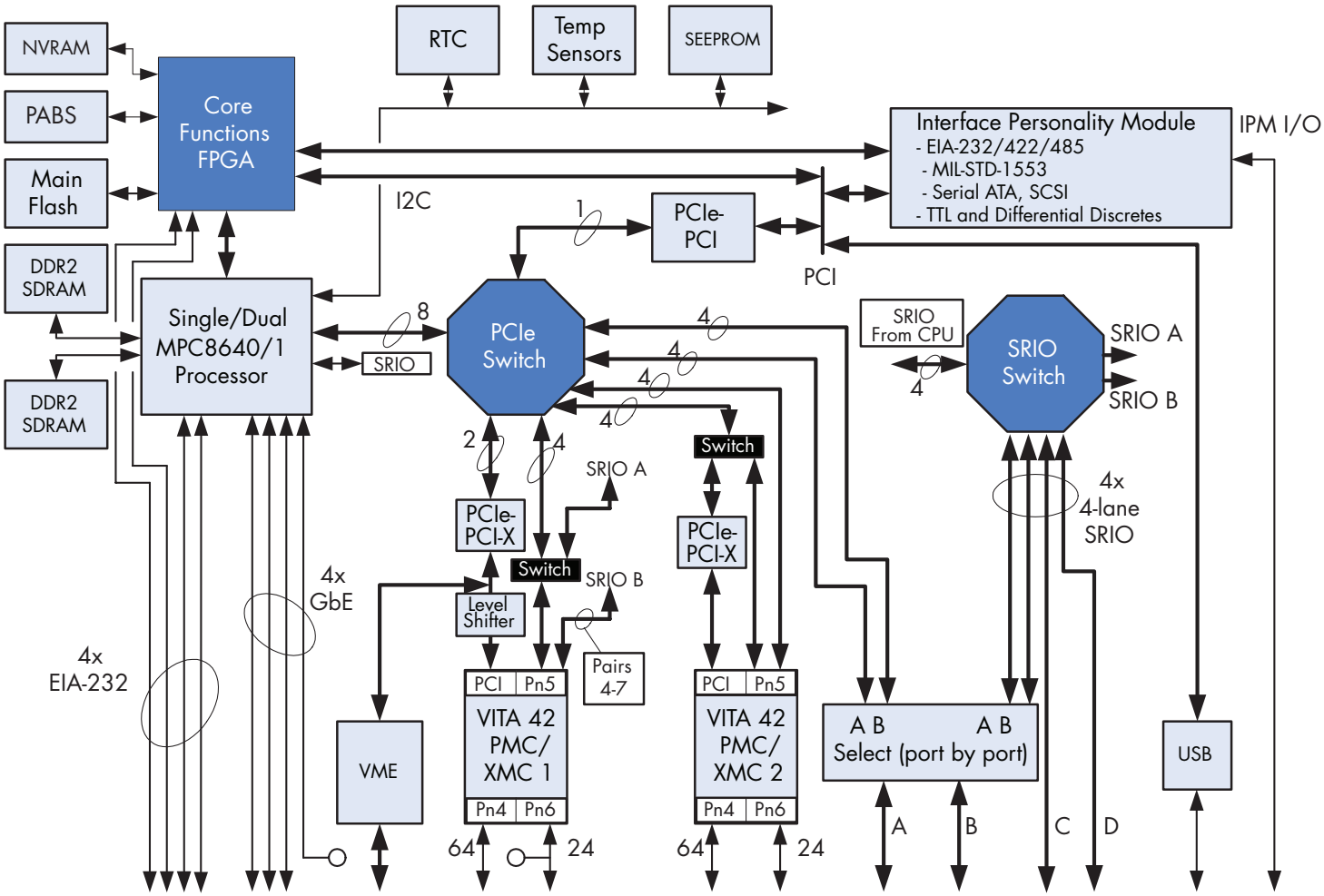
Available in a full range of environmental build grades the VPX6-185 is targeted to the challenging data- and digital signal-processing needs of tactical aircraft, armored vehicles and harsh environment naval systems. For retrofit and technology insertion applications, the VPX6-185 offers a superset of the I/O features of earlier generations of Curtiss-Wright VME 18x PowerPC™ SBCs As a member of Curtiss-Wright continuously evolving stream of PowerPC SBCs including the SVME/DMV-179, 181, 182, and 183, the VPX6-185 supports the life- cycle model of successive technology insertions throughout a platform's lifetime.

The VPX6-185 will occupy a standard 0.8" slot and may be used for upgrading existing VME systems in the same footprint. The VPX6-185 is also available in the VITA 48 (VPX REDI) format with covers to support two level maintenance LRM requirements. Air-cooled variants are delivered with 1" front panels.

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Figure 1: VPX6-185 VPX Block Diagram



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VPX Module Format

The Versatile Performance Switching (VPX) module format, governed by the VITA 46 specification and the associated VITA 48 Ruggedized Enhanced Design Implementation (REDI) was established to address the fundamental requirement to provide open-architecture modules that incorporate the high-speed serial interconnect technology that is becoming pervasive in high performance computing. The VPX standard was developed by the leading providers of military COTS modules to address the major issue of high-speed serial interconnect, as well as incorporating numerous improvements learned after years of integrating VME and CompactPCI® (cPCI) modules. The VPX standard, in short provides:

- 3U and 6U Eurocard form factors preserve chassis mechanical designs
- Support four x4 serial interfaces as the primary fabric
- Support 128 differential pairs for modern high-speed interfaces such as DVI, SATA, SFPDP, SAS and custom sensor interfaces
- Optional support of VME for interoperability with legacy equipment
- Support of higher power modules and improved cooling
- Improved logistics with two-level maintenance and keying

The VPX module format provides many benefits to integrators of high-performance multi-processor systems for radar, electro-optical and signal intelligence applications. In particular sRIO is suited to high-bandwidth communications between processors in a VPX system, while PCIe functions as a fast connection between processors and the new generation of XMC modules which can easily be placed on VPX format carrier cards.

Dual Core Freescale Power Architecture MPC8640/1 Processor

The processing function of the VPX6-185 is provided by the MPC8640/1. The MPC8640/1 provides in a single package one or two e600 cores, dual DDR2 memory controllers with ECC, a sRIO interface, two PCIe interfaces, GbE controllers and serial I/O controllers.

The e600 core and AltiVec units of the MPC8640/1 processor are based on the proven internals of the MPC7448 processor, offering a large 1 MB internal L2 cache. Existing C, assembly and AltiVec assembly code will run on the MPC8640/1 without change.

The MPC8640/1 processor integrates controller functions that previously required the use of an external bridge. In addition to the benefit of reduced size and higher reliability, the integrated dual memory controllers of the MPC8640/1 provide a much higher level of performance and reduced latency. Table 1 compares the key characteristics (and performance gains) of the MPC8640/1 to a previous generation VME-183 SBC based on the MPC7448 processor.

Table 1: VME-183 to VPX6-185 Comparison

	183	185
Processor (AltiVec)	Dual 1.2 GHz MPC7448	Dual-core 1.33 GHz MPC8640/1D
GFLOPS	19.2 @ dual 1.2 GHz	21.3 @ dual 1.33 GHz
CPU Bandwidth to Memory	1 GB/s (MPX bus @133 MHz)	8.6 GB/s (DDR266)
Memory Banks	1	2
Memory Bandwidth	2 GB/s (DDR133)	8.6 GB/s (DDR266)
SDRAM Read Latency (TS to TA)	~105 ns	~55 ns
I/O Fabric	Integral VME ~40 MB/s StarFabric (PMC) ~400 MB/s	4x sRIO, 8x PCIe
I/O Bandwidth	Integral VME ~40 MB/s StarFabric (PMC) ~400 MB/s	sRIO fabric - 1.25 GB/s each direction

VPX Fabric Interface

The VPX6-185 provides users with the option of using either sRIO or PCIe interfaces to connect with other VPX cards in a system. sRIO is suited for processor to processor communications and would be used to build a system with the VPX6-185, CHAMP-AV6 and CHAMP-FX2 family of VPX products. PCIe is suited to connecting with PCIe and PCI-based peripheral devices. The VPX-185 makes use of its PCIe fabric interfaces to support the VPX6-215 ExpressReach XMC/PMC carrier card. The ExpressReach allows users to easily add extra XMC/PMC modules into a system by extending the local PCIe fabric of the VPX-185 across a VPX backplane. See Figure 2, VPX System using sRIO and PCIe. The VPX6-185 provides two fabric ports which may be configured to operate as sRIO or PCIe and two fabric ports that operate permanently as sRIO. The configuration of the ports is controlled by parameters stored in non-volatile memory. Changes to the port configuration are made via the CSA user interface. A system reboot is required to affect any changes to the port configuration.

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Dual Data Rate (DDR2) SDRAM

The VPX6-185 has two independent DDR2 memory controllers supporting DDR2 SDRAM. The VPX6-185 may be fitted with 512 MB, 1 GB, or 2 GB of SDRAM (The 512 MB option uses one bank/controller). The DDR2 interface operates at a rate up to 500 MHz resulting in a peak bandwidth of 4.3 GB/s per memory bank, 8.6 GB/s total.

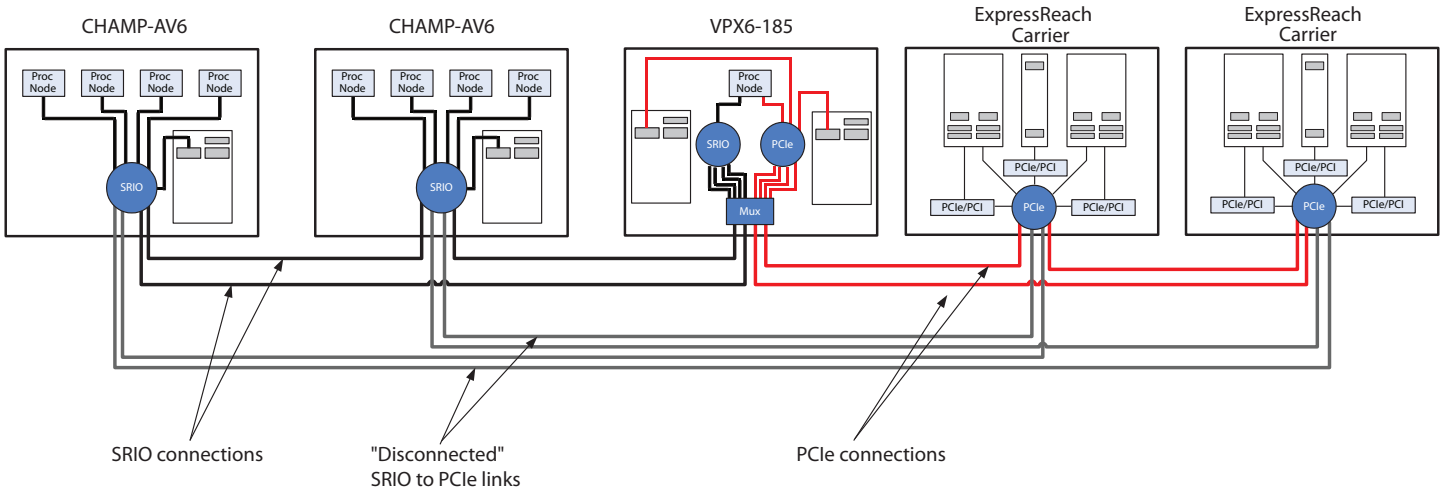
To preserve data integrity, the SDRAM is provided with Error Checking and Correcting (ECC) circuitry that detects and corrects all single-bit data errors, detects all double-bit errors, and detects all 3- and 4-bit errors within the same nibble. The SDRAM is accessible from the processor and from the PCIe and sRIO interfaces. Subject to the configuration of BSP settings controlling the memory management of the MPC8640/1 processor, the memory can be accessed from other boards via sRIO, local XMC/PMC devices, remote XMC/PMC devices on ExpressReach carrier cards and the VMEbus.

Flash Memory

The VPX6-185 is available with 256 or 512 MB of flash memory. The flash will retain data for 20 years at +85°C. Note: these figures assume the sector the data is in has less than 1,000 erase cycles. The data retention drops as erase cycle count increases. After 1,0000 cycles, data retention is for 10 years. After 100,000 cycles, data corruption will likely be noticeable in one year. Read performance of the flash array is optimized in order to minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical.

For absolute security against inadvertent flash programming or corruption, a hardware jumper is provided to disable writing to flash. The CSA firmware of the VPX6-185 provides flash programming functions with support for downloading flash images over Ethernet. See the separate CSA firmware data sheet for details. See the Non-volatile Memory Security section for more information on write protection and scrub features.

Figure 2: VPX System with Mixed PCI and sRIO



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Permanent Alternate Boot Site (PABS)

PABS provides a backup boot capability in the event that the firmware in the main flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main flash without removing the card from the system in which it is installed. An onboard jumper and a backplane signal (ALT_BOOT) are provided to cause the card to boot from PABS, thus allowing a user to reinstall the standard firmware load. The PABS feature guarantees that a card will never need to be removed from a system to perform flash updates.

NVSRAM

A Simtek 14CA8N AutoStore NVSRAM provides fast, non-volatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes the AutoStore NVSRAM just like standard SRAM, with no special programming algorithm required. Upon detecting a power loss, an Autostore cycle is performed and all 128 KB are automatically transferred from the on-chip SRAM to the on-chip EEPROM using energy stored in an onboard capacitor. At the next power-up a recall cycle is performed to transfer the EEPROM contents back to the SRAM, where the application code can now utilize the stored data to continue normal operation. The number of recall cycles is unlimited: the maximum number of store cycles is 1,000,000 and the data retention period is 100 years. For security against inadvertent writes to NVSRAM, a hardware jumper is provided to disable writes to the device. Cards are configured for shipment with NVSRAM reprogramming enabled in hardware.

Non-volatile Memory Security

The VPX6-185, as well as other Curtiss-Wright Continuum Architecture products, provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices, flash, PABS flash, NVSRAM and FPGA PROM may be individually write-protected by a hardware jumper. The jumpers may be visually inspected to conform to security procedures. To facilitate with the management of sealed-box systems, a backplane signal (NVMRO) may be asserted to over-ride the hardware write protection. The CSA firmware of the VPX6-185 provides non-volatile scrub functions to perform a secure erase per NISPOM requirements.

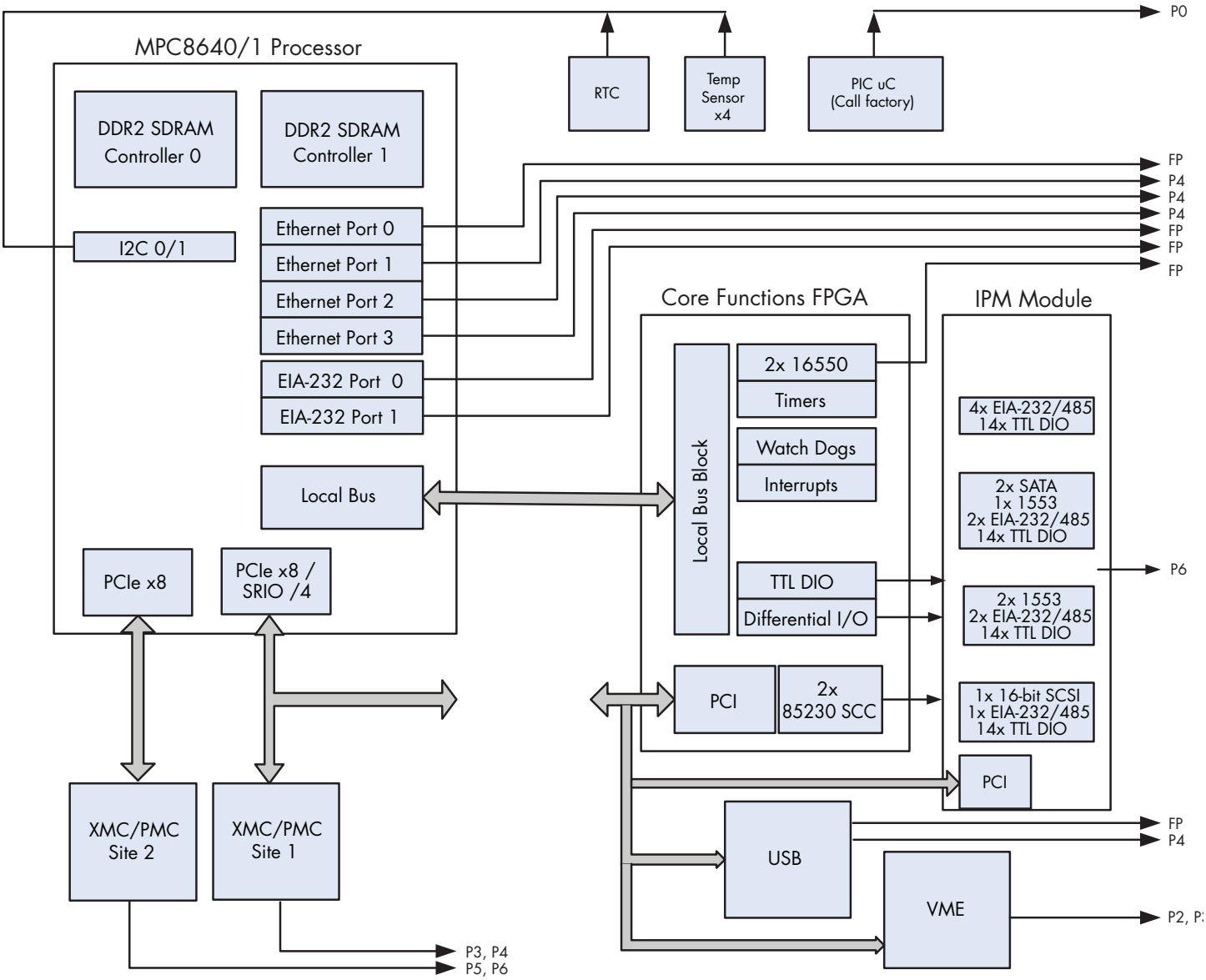
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The VPX6-185 I/O System

The VPX6-185 features a large number of I/O interfaces including EIA-232, EIA-422/485 serial, USB, Ethernet, MIL-STD-1553, SATA, SCSI, TTL and differential discrete I/O. The details of the I/O interfaces are described in the following paragraphs. The VPX6-185 provides for an I/O expansion facility with the inclusion of the Interface Personality Module (IPM). The IPM concept, carried forward from the VME-182,183 and 184 SBCs, is a connectorized subassembly that can either simply provide physical-level transceivers for controller devices implemented in the Core Functions FPGA or it can host PCI peripherals such as a SATA interface device. Some of the optional I/O features are implemented with IPM modules. Refer to Table 2 for a summary of the I/O configurations that are available on the VPX6-185.

Figure 3: I/O Subsystem Diagram



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Four GbE Interfaces

The VPX6-185 is equipped with up to four 10/100/1000Base-TX Ethernet interfaces, all implemented within the MPC8640/1. Three of the Ethernet ports are routed to the backplane connector P4. One port is factory configured to be present on the front panel connector (air-cooled cards) for standard product variants or to the backplane connector P4 for customer specific variants (note that this shares XMC site 1 differential I/O pairs). The Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9 KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence.

8/16-Bit SCSI-2 Interface Option (upon customer specific request)

The VPX6-185 optionally provides a single-ended, 8- or 16-bit Ultra SCSI (SCSI-2) interface, based on the LSI Logic 53C875 SCSI controller. The 53C875 is a highly autonomous device and transfers data to and from PCI via an internal SCSI DMA controller and an associated DMA FIFO, minimizing the loading of the main PowerPC processors. As a PCI master the 53C875 is capable of zero wait-state data bursts at 132 MB/s, conserving both PCI bus and main memory bandwidth. In 16-bit mode the device supports peak transfer rates of 40 MB/s synchronous and 14 MB/s asynchronous. In 8-bit mode peak transfer rates on the SCSI bus are 20 MB/s in synchronous mode and 7 MB/s asynchronous. See Table 2 for configurations that include SCSI.

Dual SATA Interface Option

The VPX6-185 optionally provides two SATA 1.0 (1.5 GB/s) interfaces based on the Silicon Image 3124 device. Each interface incorporates several performance-enhancing features such as:

- Independent DMA channel with 2K FIFO
- Independent command fetch, scatter/ gather, and command execution

See Table 2 for configurations that include SATA.

Four EIA-232 Serial Ports

All VPX6-185 configurations have a minimum of four EIA-232 serial channels. The EIA-232 serial ports (channels 1,2,7,8) support asynchronous communications with one transmit and one receive signal. All four ports are connected to both a front panel connector and the backplane connector. One serial port supports the use of the DTR signal to automatically detect the connection of a data terminal and can be used to control the boot-up sequence of the card if desired. Two of the serial ports are implemented in a 16550-based controller in the Core Functions FPGA. The other two ports utilize the MPC8640/1 DUART. The baud rate of all four ports can be set independently from 300 to 115200.

Four EIA-232/422/485 Serial Port Option

The VPX6-185 is available in configurations with 1, 2 or 4 additional serial ports (channel numbers 3-6). These additional serial ports are implemented with 85230 Serial Communication Controller (SCC) cores in both the Core Functions FPGA and in all of the IPM modules. All of the serial ports support asynchronous communication with baud rates of 300 to 115200. All of the serial ports support synchronous HDLC/SDLC communications at up to 2.0 MB/s. In synchronous mode a full range of data encoding schemes are supported. (NRZ, NRZI Mark, NRZI Space, FM0, FM1, Manchester, and Differential Manchester) The synchronous ports support separate transmit and receive clock signals and can use internal or external clocking, or clock encoded schemes. All of the serial ports support software selection of either EIA-232 (async only) or EIA-442/485 (sync or async) signal levels. See the Differential Discrete I/O section below for information on how the VPX6-185 provides the capability to control each of the EIA-422/485 drivers and receivers as differential-mode discrete signals for use as serial control signals or general purpose I/O. See Table 2 for configurations that include the optional 232/422/485 serial channels.

LVTTL Discrete Digital I/O Option

The VPX6-185 optionally provides 14-bits of LVTTL compatible discrete digital I/O. Each bit is individually programmable to be an input or output. Each I/O bit is capable of generating an interrupt upon a change of state, programmable to detect either edge. Each bit has a 10K pull-up resistor to 5 V. The output drive current is 24 mA. See Table 2 for configurations that include the optional DIO signals.

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Differential Discrete Digital I/O

The VPX6-185 provides the capability to control each of the EIA-422/485 drivers and receivers as differential-mode discrete signals via registers in the Core Functions FPGA. This allows flexibility in how the drivers and receivers are used. The choice of whether the drivers and receivers are attached to serial ports or used as discrete differential I/O is software selectable on a per-serial channel basis. When configured as discrete differential I/O, the drivers can be used as general-purpose differential mode control signals unrelated to serial I/O requirements. Differential discrete inputs can generate an interrupt upon a change of state, with programmable edge direction. Note that if the serial channel physical levels are set to EIA-232, then discrete digital I/O at EIA-232 levels is obtained.

Two USB 2.0 Ports

The VPX6-185 incorporates a Phillips ISP1562 to provide two USB 2.0 ports. Each port can handle high-speed (480 MB/s), full-speed (12 MB/s), and low-speed (1.5 MB/s) operation. When operating at low-speed or full-speed, each port is managed by independent OHCI-compliant controllers internal to the device. One EHCI-compliant controller manages any ports operating in high-speed mode.

One USB port is accessible on the front panel connector and the other is accessible on the P4 connector. Each port provides a +5 V output to power external USB devices such as keyboards.

Two Channel MIL-STD-1553 Option

The VPX6-185 provides up to two MIL-STD-1553 channels implemented with DDC 65864 micro-ACE TE devices offering the following key features:

- Support for MIL-STD-1553A, MIL-STD-1553B Notice 2, and STANAG 3838 protocols
- BC, RT, MT modes independently selectable for each channel
- Choice of transformer-coupled (standard) or direct-coupled outputs (on a special order basis)
- MIL-STD-1760 amplitude compliant
- 64 K words of RAM per channel, with parity
- PCI interface is 33 MHz, 32-bit and supports burst writes with a FIFO for up to one complete MIL-STD-1553 message
- Transmit Inhibit input for each channel
- Bus Controller features:
  - Highly autonomous bus controller with built-in message sequence control engine for multi-frame message scheduling, branching, and asynchronous message insertion
  - Programmable inter-message gap size
  - Single frame or auto-repeat modes
  - Automatic retries
  - Time-tag can be transmitted with Synchronize with Data mode code
  - External Trigger input for each channel
- Remote Terminal features
  - Programmable illegalization of RT commands
  - Busy bit programmable on a sub-address basis
  - 16-bit time-tag option with options of 2, 4, 8, 16, 32, or 64 µsec/LSB based on internal clock
  - External time-tag clock input
  - Time-tag can be set via Synchronize with Data mode code
  - External Subsystem Flag input
- Monitoring Terminal features
  - Selective message monitor mode, use for selecting monitoring based on RT address, Transmit/Receive bit, and Sub-address
  - Simultaneous RT and monitor modes The RT address for each channel can be set by software

A backplane configuration input is provided for each channel that can cause the RT address to be set by subset of the TTL discrete digital I/O lines. To meet the MIL-STD-1760 First Response requirement of an RT response within 150 msec, one of the MIL-STD-1553 channels initializes as an RT with the Busy status word bit set. This requires that the MIL-STD-1553 channel be configured to set the RT address in hardware.

Curtiss-Wright's driver software for the VPX6-185's MIL-STD-1553 channels provides a flexible, easy to use, and robust applications programming interface (API). The driver supports BC, RT, and MT modes of operation, and offers a high degree of compatibility to the proven software driver provided for Curtiss-Wright's popular PMC-601 MIL-STD-1553 module. Source code is provided for user reference. The MIL-STD-1553 driver for the VPX6-185 is sold separately from the hardware and the VPX6-185 BSPs. See separate data sheet for details.

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Table 2: Summary of I/O Options

Mode	Front Panel (air-cooled only)	Backplane Connector P1 – P6
0 (standard product)	◆ EIA-232 serial channels 1, 2, 7, 8 ◆ Serial cable detect ◆ GbE port 4 ◆ USB port 2 ◆ Card reset	◆ EIA-232 serial channels 1, 2, 7, 8 ◆ Serial cable detect ◆ GbE ports 1-3 ◆ Optional Ethernet port 4 ◆ USB port 1 ◆ Card fail output ◆ Alternate boot input ◆ NVMRO input ◆ Reset input ◆ PMC1 Pn4 I/O (64 pins) ◆ XMC1 Pn5 I/O (12 diff pairs) ◆ PMC2 Pn4 I/O (64 pins) ◆ XMC2 Pn5 I/O (12 diff pairs)
1 (by customer specific request)	Same	Same as Mode 0 with additional: ◆ 8-bit SCSI ◆ EIA-422/485 serial channels 3-4 ◆ 14 DIO
4 (by customer specific request)	Same	Same as Mode 0 with additional: ◆ 16-bit SCSI ◆ EIA-422/485 serial channel 3 ◆ 14 DIO
6 (standard product)	Same	Same as Mode 0 with additional: ◆ EIA-422/485 serial channels 3-6 ◆ 14 DIO
8 (by customer specific request)	Same	Same as Mode 9 only with MIL-STD-1553 channel 1
9 (standard product)	Same	Same as Mode 0 with additional: ◆ MIL-STD-1553 channels 1-2 ◆ EIA-422/485 serial channels 3-4 ◆ 14 DIO
11 (standard product)	Same	Same as Mode 0 with additional: ◆ MIL-STD-1553 channel 1 ◆ SATA channels 1-2 ◆ EIA-422/485 serial channels 3-4 ◆ 14 DIO
12 (standard product)	Same	Same as Mode 11 but without MIL-STD-1553

Real-Time Clock (RTC)

A Maxim/Dallas Semiconductor DS3231 RTC chip provides the RTC function. It contains registers for century, year, month, day, hours, minutes, and seconds. The RTC is capable of generating alarm interrupts. The RTC draws its power from an onboard power supply. In the event of loss of backplane +5 V power, the RTC will automatically switch over to draw power from the backplane VBAT line (P1-G3).

Multi-board Synchronous Clock

The VPX6-185 includes a special purpose counter which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. The counter can be set to roll-over to a pre-load value and interrupt on roll-over. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors. The MBSC makes use of the VITA 46 reference clock and does not require any special backplane wiring. See the section on Continuum Insights Multiprocessor tools for information on how the MBSC can be used to coordinate timing between multiple boards.

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Table 3: VPX6-185 Timing Resources

Timer	Implementation	Type	Size	Tick Rate/Period	Maximum Duration
PowerPC Time Base Register	x1 per CPU	Free Running Counter	64-bit	125 MHz/8 nsec	4,676 yrs
PowerPC Decrementer	x1 per CPU	Presettable, Readable Downcounter	32-bit	125 MHz/8 nsec	34.35 sec
General Purpose #0-7	MPC864x MPIC	Presettable, Readable Downcounter with auto-read and stop options	31-bit	62.5 MHz/16 nsec	34.36 sec
RTC Alarm	RTC	Alarm Interrupt	-	-	-
Watchdog timers (1 per CPU)	Core Functions FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	25-bit	1 MHz/1 usec	33.55 sec
System Timers #1-6	Core Functions FPGA	Presettable, readable downcounter with interrupt on terminal count	32-bit	50 MHz/20 nsec	85.9 sec

Extensive Timing Resources

The VPX6-185 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in Table 3.

Avionics Watchdog Timers

The VPX6-185 provides a watchdog timer for each of the two processor cores. Each watchdog timer is a pre-settable down-counter with a resolution of 1 µsec. Time-out periods from 1 msec to 32 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts. A watchdog event indicator discrete signal is output to the backplane.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in “Avionics” mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event.

General Purpose DMA Controllers

The MPC8640/1 provides a 4-channel DMA controller that is available for general purpose use. The DMA controller can be used for transferring blocks of data between the SDRAM, flash memory, device bus peripherals, sRIO-mapped memory and the PCI busses. The DMA controllers support direct and descriptor-driven chained operation. The DMA controllers can support source and destination striding. The DMA controllers also feature a bandwidth management feature to allow the user to control the distribution of bandwidth between the four DMA channels.

For transferring data over VME at high-speeds, the optional Tundra Tempe VME interface chip provides a 2-channel DMA engine that can be programmed to employ VME 2eSST block transfer cycles.

VME Interface Option

The VPX6-185 is equipped with a VME master/slave interface that supports the VME64x, 2eVME, and 2eSST protocols. The interface is implemented with the Tundra Tsi148 PCI/X to VME bridge. The Tsi148 supports the newest 2eSST VMEbus transfer protocol offering the maximum possible VME performance, while retaining full backwards compatibility with legacy VME systems. The VMEbus can be mapped into the memory space of the MPC8640/1 and similarly transfers from VME can be destined for the VPX6-185 local SDRAM. The Tsi148 features internal DMA engines to move data between local memory and the VMEbus.

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XMC/PMC Sites

The VPX6-185 is equipped with two mezzanine sites, each capable of supporting IEEE 1386 PMC or VITA 42.3 XMC modules. The VPX6-185 takes full advantage of the VPX standard by providing 64-bits of Pn4 I/O and 12-pairs of differential Pn6 I/O from each of its mezzanine sites to the backplane connectors. The I/O is mapped according to the VITA 46.9 draft specification which provides for controlled impedance, matched length differential pairs. XMC/PMC Site 1 provides the software selectable option of utilizing a 4-lane PCIe, or 4-lane sRIO host interface on the Pn5 connector. The sRIO interface may be used in conjunction with the Curtiss-Wright XMC-255 module to extend the system sRIO fabric to a front panel connector. See the paragraph later in this data sheet describing the XMC-255.

On conduction-cooled cards, the XMC/PMC sites adhere to the VITA 20- 2001 (R2005) conduction-cooled PCI Mezzanine Card (PMC) standard specifications. To optimize the thermal transfer from XMC/PMC modules to the base card the standard VPX6-185 thermal frame incorporates both the Primary and Secondary thermal interfaces as defined by VITA 20-2001.

The VPX6-185 is capable of hosting Processor PMCs in non-Monarch mode as described in the VITA 32-2003 draft standard (the Monarch# signal is left floating). The VPX6-185 does not support the optional second PCI agent, the optional EREADY signal, or the optional RESETOUT# signal.

Table 4 XMC/PMC site specifications provides details on the capabilities of both mezzanine sites.

Table 4: VPX6-185 PMC/XMC Specifications

Function	Site 1	Site 2
Location	Top of card	Bottom of card
PCI Interface	PCI-X 64-bit 66 MHz via 2-lane PCIe/PCI bridge	PCI-X 64-bit 100 MHz via 4-lane PCIe/PCI bridge
PCIe Interface	◆ 4-lane per VITA 42.3 ◆ 1 GB/s peak simultaneous transmit and receive	◆ Up to 8-lane per VITA 42.3 (Note 1) ◆ 2 GB/s peak simultaneous transmit and receive
sRIO Interface	◆ Selectable 4-lane per VITA 42.2 (Link 0) ◆ 4-lane fixed on pairs 4-7 (Link 1)	N/A
Pn4 I/O	64-bits to VITA 46 P3 per VITA 46.9 rule 5-5, pattern P64 (P3-64s)	64-bits to VITA 46 P5 per VITA 46.9 rule 5-5, pattern P64 (P5-64s)
Pn6 I/O	12 differential pairs to VITA 46 P4 per VITA 46.9 rule 5-5, pattern x12D (P4-x12d) (Note 2)	12 differential pairs to VITA 46 P6 per VITA 46.9 rule 5-5, pattern x12D (P6-x12d)
Differential Routing	100 Ohm differential, 50 Ohm nominal for both Pn4 and Pn6 I/O signals	
VIO	Jumper select for 3.3 V or 5 V	3.3 V operation only
3.3 V Power	Provided from onboard PSU, 13 W maximum to any one site. 20 W total maximum. The 3.3 V is sequenced with the main board power.	
5.0 V Power	◆ Drawn from backplane 5.0 V ◆ 20 W maximum to any one site, 30 W maximum total. The 5 V is sequenced with the main board power.	

Notes:
1. The lower 4-lanes of the PCIe interface are either switched to the PCIe/PCI bridge for PMC operation, or switched to the J5 connector for XMC operation.
2. The VPX6-185 has an option to route the 4th GbE to the backplane. In this configuration the GbE signals replace the upper four XMC differential pairs of site 1.

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Designed for Harsh Environments

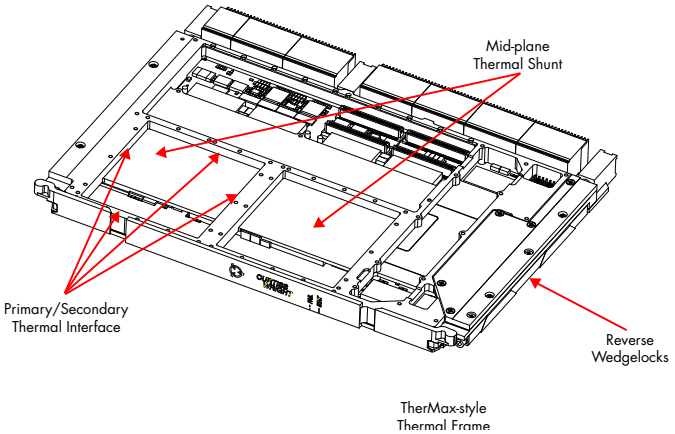
To cost-effectively address a diverse range of military/ aerospace applications, the VPX6-185 is available in a range of ruggedization levels, both air- and conduction-cooled. All versions are functionally identical, with air-cooled versions available in Curtiss-Wright ruggedization levels 0 and 100, and conduction-cooled versions in levels 100 and 200. Curtiss-Wright's standard Ruggedization Guidelines define the environmental tolerance of each ruggedization level (see Curtiss-Wright Ruggedization Guidelines factsheet for more information).

Enhanced Thermal Management for Conduction-Cooled Applications

For those demanding application environments that require conduction-cooling, the VPX6-185 uses a combination of thermal management layers within the Printed Wiring Board (PWB) and an aluminum thermal frame that provides a cooling path for the PMC sites and for high-power components such as the processors, caches, and bridge device. The VPX6-185 thermal frame employs a number of innovative design techniques to keep the temperature rise of the electronic components to a minimum, thus increasing the long-term reliability of the product:

- Heat-pipe transfers processor heat to both card edges
- Provision of both primary and secondary thermal interfaces on PMC sites
- Mid-plane thermal shunts for PMC sites
- TherMax design approach
- Full-width thermal interface to back-side slot wall

Figure 4: Representative Thermal Frame



Mid-plane Thermal Shunts for PMCs

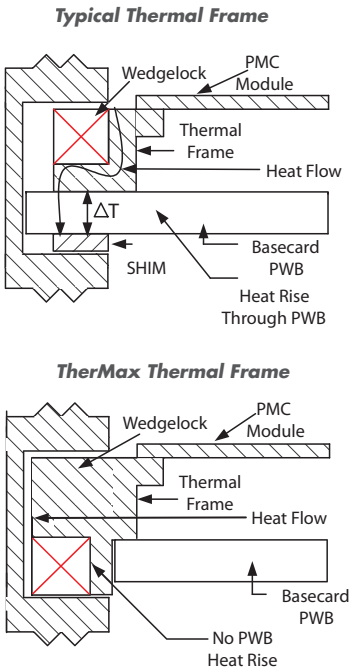
To optimize the conduction-cooling of high-performance, high-power PMC modules such as graphics or networking PMCs, the VPX6-185 thermal frame incorporates mid-plane thermal shunts for the PMC sites. High-power PMCs can include a mating cooling surface on the PMC module to contact the mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC modules can significantly lower the heat rise from the VPX6-185 card edge to the PMC components. The midplane thermal shunt does not impinge on the VITA 20- allowed component height. Note: One mezzanine site keep out area is restricted due to the heat pipe.

TherMax-style Thermal Frame

A TherMax thermal frame provides an unbroken metallic path from the PMC sites and shunted components to the back- side cooling surface of the card therefore minimizing the temperature rise to these devices. In comparison, a typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB which has a high thermal resistance compared to aluminum.

Figure 5: TherMax Diagram

A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame



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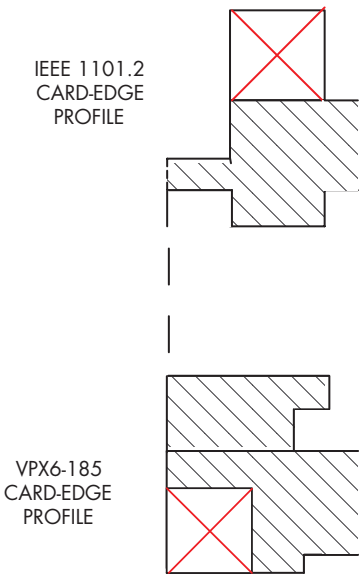


Full-width Thermal Interface to Back-side Slot Wall

To minimize the temperature rise from the mating slot wall of conduction-cooled enclosures to the back-side thermal interface region of the VPX6-185, the VPX6-185 thermal frame maximizes the thermal interface area by extending the frame to the full width of the card, as illustrated in Figure 6. This deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis, has the benefit of lower card operating temperatures and increased long term reliability. During test and integration activities where it may be desirable to install a conduction-cooled VPX6-185 into an air-cooled card-cage, this can normally be accomplished simply by removing the card guides.

Figure 6: Card-edge Profile Deviates from IEEE 1101.2

VPX6-185 *Card-Edge Profile is Optimized to Provide a Full-width Thermal Interface to the Back-side Slot Wall*



XMC-255 Serial RapidIO Extender

The VPX6-185 supports a facility to extend the sRIO fabric to a front panel connector. This feature can be used to connect two separate VPX chassis' together, or to make connections between slots that are not present in the backplane. This feat is accomplished with the use of the Curtiss-Wright XMC-255 sRIO Extender XMC module. The XMC-255 has circuitry to regenerate two sRIO channels that it receives on Pn5. These sRIO channels are then output to Infiniband style front panel connectors. Standard Infiniband cables may then be used to make connections to matching VPX6-185/255 boards. The speed of operation of the port (1, 2.5 or 3.125 GB/s) will depend on the length of cable between systems.

The XMC-255 takes advantage of the VPX6-185 option to select a sRIO port to be presented to the XMC site 1 Pn5 connector. The XMC-255 is offered in air-cooled format, in temperature range 0 and 1. Consult Curtiss-Wright for more information concerning the XMC-255.

Status Indicators and Controls

The VPX6-185 SBC provides run/fail status by asserting a backplane signal and illuminating a red front panel LED in the event the diagnostics detect a card failure. There are also two software controlled green LEDs that the application can use to indicate status of each CPU core independently. A card reset signal is available on the backplane connectors and on the front panel connector on air-cooled cards. The front panel cable for the VPX6-185 includes a push button switch that interfaces to this signal to allow the card to be reset without doing a full system reset.

COP Emulator Interfaces

The VPX6-185 can be optionally fitted with a connector on the rear of the PWB to provide access to the MPC8640/1 COP interface. This is a low profile connector that when installed intrudes into the keep-out space between cards. Consult Curtiss-Wright for more information if you need to use a COP emulator with the VPX6-185.

Temperature Sensors

The VPX6-185 provides temperature sensors to measure board and processor temperatures. There is a sensor at each edge of the card, one sensor in close proximity to the processor and one sensor to directly measure the die temperature of the MPC8640/1 using its thermal diode feature. The sensors can be read by software, and they may be configured to generate an interrupt in case of an over temperature condition.

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Software Support

Continuum Software Architecture (CSA)

The VPX6-185 is supported by a suite of firmware, RTOS BSPs, communication libraries and signal processing libraries. The Continuum Software Architecture is Curtiss-Wright's suite of firmware and BSP APIs that is common to SBCs (VME, cPCI and VPX) and multi-processor boards. Developers of mixed systems will find a common set of features and software interfaces for all future processing products from Curtiss-Wright. The Continuum Software Architecture is comprised of:

Continuum Firmware Monitor

The monitor provides a command line interface over serial port or Ethernet to allow a user to perform a variety of system integration activities with the card. The monitor provides debug and display commands, diagnostic results display and exerciser controls, non-volatile memory programming and declassification and programming of parameters used to control boot-up and diagnostics.

Continuum Built-in Test (BIT)

BIT is a library of diagnostic routines to support Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) designed to provide 95% fault coverage.

Operating System Software

The VPX6-185 is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported or planned for the VPX6-185.

- VxWorks 6.x, Workbench 2.x from Wind River Part number DSW-185-006-CD
- Curtiss-Wright developed Wind River Linux GPP LE is available (3.x) - part number: DSW-185-6100-GPP
- INTEGRITY from Greenhills Software. Consult factory for availability
- LynxOS 5.0 from LynuxWorks. Consult factory for availability.

Continuum Inter-Processor Communications (IPC) Library

The IPC Library is a library of functions designed to enable high-performance, low-latency message passing. IPC allows processors to communicate task-to-task, on the same card over local interconnect or between boards over a system level interconnect. IPC supports several transport mechanisms including PCI/PCIe, StarFabric and sRIO.

Applications developed on CHAMP-AV2/3/4/6 or SVME/DMV-183/184/185 will port to the VPX6-185 with no changes related to the IPC layer.

Continuum IPC provides low-overhead block data transfers, segmented block data transfers and signaling between processors to assist in high-bandwidth data movement. See the Continuum IPC Library data sheet for more details.

Continuum Vector Library

The VPX6-185 derives its floating-point performance from the pair of AltiVec Vector processing units within the MPC8460/1D processor. The Continuum Vector Library provides over 200 functions optimized for the AltiVec unit, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for the Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector data sheet for detailed information.

Continuum Insights Multiprocessor Development Tools

Complex systems with many processing nodes and networked interconnect architecture require specialized tools to debug and verify their operation. The Continuum Insights tools facilitate the development of such systems by providing a graphical representation of the configuration, real-time performance and network traffic of systems under development. Based on the Eclipse IDE and Wind River Systems' Workbench platform development tools, the Insights tools provide:

- Instrumentation and analysis tools to collect real-time system event data. A post run-time analysis tool allows developers to debug and verify critical interaction among multiple processors. Event data can be collected from processing nodes in the system synchronized to a common precision time-base.
- Run-time system monitoring with graphical display of threads, processor utilization, task allocations and fabric performance of individual nodes or clusters of nodes. The monitoring tool encourages real-time user interaction to control processes or data transfers by displaying results in a "dashboard-like" display format.
- Network analysis tool to view the system physical topology, measure network bandwidth loads, manage and optimize packet routing with awareness of IPC-defined end-points so developers can easily correlate traffic to the system software.

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Cables and Rear Transition Modules

The VPX6-185 features a high-density front panel connector on air-cooled versions of the board. A cable is available, part number CBL-185-FPL-000 that breaks out the signals to a number of standard connectors. The cable provides four 9-pin DE-9 connectors for EIA-232 channels, one RJ-45 connector for GbE, one USB connector and a card reset push-button.

To gain access to the backplane I/O signals of the VPX6-185, a Rear Transition Module (RTM) will be available, part number RTM6-185-000. The RTM6 is a 6Ux80 mm (1101.10 compliant) module with a rear face plate and injector/ejector handles that plugs into the rear of the VPX backplane to make connections with the I/O signals emanating from the VPX6-185. The VPX6-185 RTM features a 100-pin high-density connector that in conjunction with a breakout cable provides access to all of the base-card I/O and IPM module I/O. Different breakout cables are available for each basecard/IPM combination. The RTM provides additional high-speed connectors to provide access to PMC/XMC I/O.

Figure 7: RTM6-185 and Cable Set

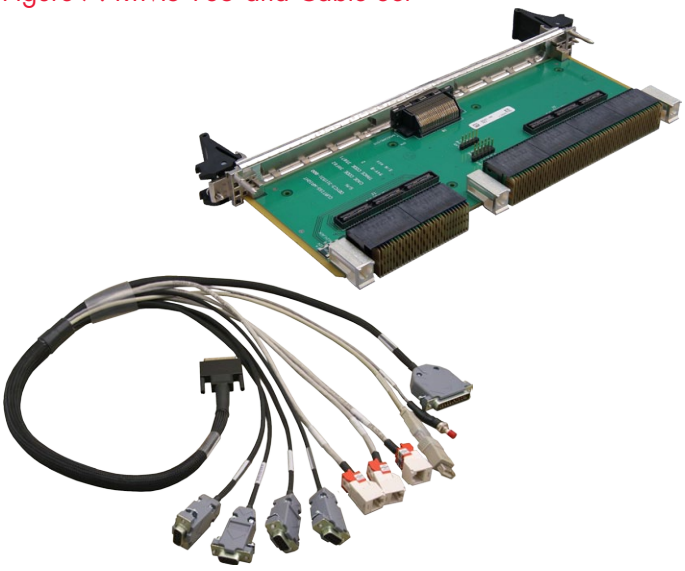


Table 5: VPX6-185 RTM and Cables

Cable Number	Connects To	Description
CBL-185-FPL-000	VPX6-185 Front Panel Cable	Front panel break-out cable for VPX6-185 providing x4 9-pin D connectors for RS-232 ports, x1 RJ-45 jack for GbE, x1 USB type A receptacle, and x1 push-button reset switch.
CBL-185-IPM-006	VPX6-185 RTM IPM Mode 6 Cable	Breakout cable for VPX6-185 in pin-out Mode 6. Provides separate branches for x2 9-pin D connectors for RS-232 ports and x4 25-pin D connectors for RS-422/485 ports. This cable connects to the high-density connector for IPM-specific I/O on RTM6-185-000.
CBL-185-IPM-009	VPX6-185 RTM IPM Mode 9 Cable	Break-out cable for VPX6-185 in Mode 8 (single MIL-STD-1553) and Mode 9 (dual MIL-STD-1553) versions. Provides separate branches and connectors for the transformer-coupled MIL-STD-1553 signals, MIL-STD-1553 configuration inputs, x2 RS-232/422/485 ports, and 25-pin female D connector for TTL discretes. Connectors for MIL-STD-1553 signals are 3-lug Twinax bulkhead jack connectors (Trompeter part number BJ79-47). This cable connects to the high-density connector for IPM-specific I/O on RTM6-185-000.
CBL-185-IPM-011	VPX6-185 RTM IPM Mode 11 Cable	Break-out cable for VPX6-185 in Mode 11.
CBL-185-IPM-012	VPX6-185 RTM IPM Mode 12 Cable	Break-out cable for VPX6-185 in Mode 12.
CBL-185-RPL-000	VPX6-185 Rear Panel Cable (RTM)	Break-out cable for VPX6-185 RTM providing x4 RS-232 ports on DE-9 connectors, x3 GbE ports on RJ45 jacks, x1 USB on USB plug, x1 push button reset switch and x1 DB25 pin contacts (male) offering DIO, CARDFAIL and ALT_BOOT.
RTM6-185-000	RTM VPX6-185	RTM for the VPX6-185 - contains x2 PMC/XMC I/O interface connectors and a dual ultra SCSI connector for base card and IPM I/O. Access is provided to VPX6-185 IPM I/O, board I/O (serial ports, Ethernet, USB), and XMC and PMC sites.
RIM-185-000	PMC RTM Interface Module (RIM)	PMC RTM Interface Module (RIM) for the RTM6-185. This RIM provides a generic connection to the VPX6-185 PMC sites of the VPX6-185 RTM. 64-pins of PMC I/O is provided on a front panel 78-pin DSUB connector for easy access. QTY 2 PMC RIM modules are provided.
CBL-185-JTAG	JTAG Test Connector	Connectors to VPX6-185 test connector and provides 2x8 0.1" pitch header for JTAG/COP emulator.

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Power Consumption

See Table 6 for power consumption figures for the VPX6-185 standard product variant base-cards. Power consumption increases as operating temperature rises. Table 6 figures are for the highest rated operating temperature while executing a test application generating CPU processing loads and data traffic representative of a typical customer application.

The VPX6-185 is designed to run off 5 V, and does not draw current from the other voltage rails for normal operation. It does draw current of 3.3 V_AUX, which is less than 50 ma. Hence, power consumption in the table below is for 5 V only.

See Table 8 for power consumption figures for the Interface Personality Modules available with the VPX6-185.

Table 6: Standard Product Variant Power Requirements

Ruggedization Level	Part Number	Reference Configuration	Typical Power (W)
Level 0 Air-cooled	VPX6-185-A01A000	MPC8640 @ 1.0 GHz, 512 M DDR2 with VME	35
	VPX6-185-A01A600	MPC8640D @ 1.0 GHz, 1 GB DDR2 with VME	44
	VPX6-185-A01B600	MPC8640D @ 1.0 GHz, 1 GB DDR2	45
	VPX6-185-A01B500	MPC8640D @ 1.25 GHz, 2 GB DDR2	52
Level 100 Air-cooled	VPX6-185-A11A000	MPC8640 @ 1.0 GHz, 512 M DDR2 with VME	37
	VPX6-185-A11A600	MPC8640D @ 1.0 GHz, 1 GB DDR2 with VME	47
	VPX6-185-A11B600	MPC8640D @ 1.0 GHz, 1 GB DDR2	45
	VPX6-185-A11B500	MPC8640D @ 1.25 GHz, 2 GB DDR2	54
Level 200 Conduction-cooled	VPX6-185-C21A000	MPC8640 @ 1.0 GHz, 512 M DDR2 with VME	37
	VPX6-185-C21A600	MPC8640D @ 1.0 GHz, 1 GB DDR2 with VME	47
	VPX6-185-C21B600	MPC8640D @ 1.0 GHz, 1 GB DDR2	45
	VPX6-185-C21B500	MPC8640D @ 1.25 GHz, 2 GB DDR2	54

Notes:
1. Typical power is measured power while running stress test software that exercises CPU and board functions including AltiVec. The actual power consumption observed will vary by application.
2. For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption figures. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption figures.

Table 7: Voltage Requirements

Ruggedization Level	Voltage	Typical Power
All	+5 V VS3	See Table 6
All	+/- 12 V_AUX, routed to PMC sites	0
All	+ 12 V VS1, VS2, not used	0
All	+ 3.3 V_AUX	50 ma

Note:
For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption figures. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption figures.

Table 8: IPM Power Requirements

Ruggedization Level		Typical Power (W)
All	Mode 6 IPM	2
All	Mode 9 IPM with both MIL-STD-1553 channels at 50% Tx time	5
All	Mode 9 IPM with both MIL-STD-1553 channels at 25% Tx time	3
All	Mode 11 IPM with MIL-STD-1553 channels at 50% Tx time	4
All	Mode 11 IPM with MIL-STD-1553 channels at 25% Tx time	3
All	Mode 12 IPM	2

Note:
For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption figures. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption figures.

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Specifications

The tables below show the power, dimensions and weight characteristics of the card.

Table 9: VPX6-185 Dimensions and Weight

Option	Dimensions	Weight (grams)
Air-cooled 0.8"	per VITA 46 draft 0.8" pitch	600
Air-cooled 1.0" option	per VITA 46 draft 1.0" pitch	650
Conduction-cooled	per VITA 46 draft 0.8" pitch	775
Conduction-cooled LRM	per VITA 46 draft 0.85" pitch	900
IPM		39 max

Notes
1. The air-cooled format is designed to fit chassis with 0.8" slot pitch. For convenience it is offered with a 1" front panel to accommodate installation in 1" pitch chassis.
2. Air-cooled cards available in temperature ranges 0 and 1.*
3. Conduction-cooled cards available in temperature ranges 1 and 2.
4. Conduction cooled cards available in a covered, 2-level maintenance LRM configuration.
5. Refer to Ruggedization Guidelines factsheet for more information.

Table 10: VPX6-185 Cooling Requirements

Configuration	Temperature Range	Air-Flow
Dual-core up to 1.33 GHz	-40 to 71 °C	15 CFM

Note
1. Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The air-flow specifications are for worst case (highest power) conditions, without any PMC/XMCs installed. Curtiss-Wright can supply additional recommendations for specific power/temperature/altitude scenarios and pressure drop characteristics of the VPX6-185 support the design and testing of cooling subsystems.

Ruggedization Levels

Air-cooled cards are available in levels 0, 100.

Conduction-cooled cards are available in levels 100 and 200 and a 2-level maintenance (LRM) configuration with ESD protective covers. See the Curtiss-Wright Ruggedization Guidelines factsheet for more information.

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Ordering Information

The VPX6-185 is ordered with the following part numbers. VPX6-185-UVWXYYY, where U, V, X & Y denote cooling method, temperature range, mechanical format and functional configuration respectively. Not all possible configurations are offered, consult Curtiss-Wright for available configurations.

VPX6 - 185 - UVWXYZZ

- I/O Mode IPM options 00, 06, 09, 11, 12
- Core Processing:
  - 0: MPC8640 @ 1.0 GHz, 512 MB DDR2, 256 MB flash
  - 1, 4: Reserved
  - 5: MPC8640D @1.25 GHz, 2 GB DDR2, 512 MB flash
  - 6: MPC8640D @1.0 GHz, 1 GB DDR2, 256 MB flash
  - 9: Custom configuration
- Backplane I/F:
  - A: x4 fabric ports configurable as sRIO or PCIe, VME
  - B: x4 fabric ports configurable as sRIO or PCIe, no VME
  - Z: custom configuration
- Mechanical Format:
  - 1: 0.8" pitch, no 2-level maintenance support, 1" faceplate
  - 3: 0.85" pitch, 2-level maintenance support (covers)
- Temperature Range:
  - 0: 0 to 50 °C
  - 1: -40 to 71 °C (air-cooled only)
  - 2: -40 to 85 °C
  - 5: -25 to 50 °C (level 50, customer specific only)
- Cooling Method:
  - A: Air-cooling
  - C: Conduction-cooling
- Model Number
- Standard Prefix for 6U VPX Cards

The following base card variants are available as standard product:

- VPX6-185-A01A000
- VPX6-185-A01A600
- VPX6-185-A01B600
- VPX6-185-A01B500
- VPX6-185-A11A000
- VPX6-185-A11A600
- VPX6-185-A11B600
- VPX6-185-A11B500
- VPX6-185-C21A000
- VPX6-185-C21A600
- VPX6-185-C21B600
- VPX6-185-C21B500

Table 11: 185 VPX Mappings

Supported OpenVPX/VITA 65 Profiles	185 Variant
MOD6-PER-4F-12.3.1-2	VPX6-185-xxxAxxx VPX6-185-xxxBxxx
MOD6-PAY-4F2T-12.2.2-1	VPX6-185-xxxAxxx VPX6-185-xxxBxxx
MOD6-BRG-4F1V2T-12.5.1-1	VPX6-185-xxxAxxx

Note: The above variants do not use power from VS1+VS2. The cards use only power from VS3=+5V.

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Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcdefense.com/sales

Email: defensesales@curtisswright.com

Technical Support

For technical support:

Website: www.cwcdefense.com/support

Email: support1@cwcembedded.com

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