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CHAMP-AV8 (VPX6-462)
VPX QUAD-CORE
INTEL CORE™ i7
DSP BOARD

HARDWARE USER'S MANUAL

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PREFACE

PURPOSE

This manual describes the OpenVPX (VITA 65) based CHAMP-AV8 and applies to L0 (commercial) and L100/L200 (air-cooled and conduction-cooled) products. When differences exist between these versions of the product, the differences will be noted. After explaining the capabilities of the CHAMP-AV8, the manual provides the procedure for installing it and checking its operation.

AUDIENCE

This document is aimed at readers with a technical understanding of hardware engineering fundamentals, as well as a basic understanding of the VPX, PCIe, and digital signal processing hardware and software.

SCOPE

This manual contains the following chapters:

Chapter 1, "Product Overview". This chapter provides an overview of the features and functions of the CHAMP-AV8 product. This includes a technical description and a block diagram.

Chapter 2, "Pre-Installation Tasks". This chapter discusses tasks that must be performed before installing the CHAMP-AV8 in a system, including checking power requirements.

Chapter 3, "Hardware Installation". This chapter explains how to install the CHAMP-AV8 into a VPX chassis and verify that it is operating correctly.

Appendix A, "Connector Pin Assignments". This appendix lists the interface connector pinouts for the CHAMP-AV8.

Appendix B, "Statement of Memory Volatility". This appendix contains the Curtiss-Wright "Certificate of Memory Volatility" and provides a description of the various types of memory available on the CHAMP-AV8 hardware.

Appendix C, "Memory Write Protection". This appendix provides information and procedures for hardware memory write protection.

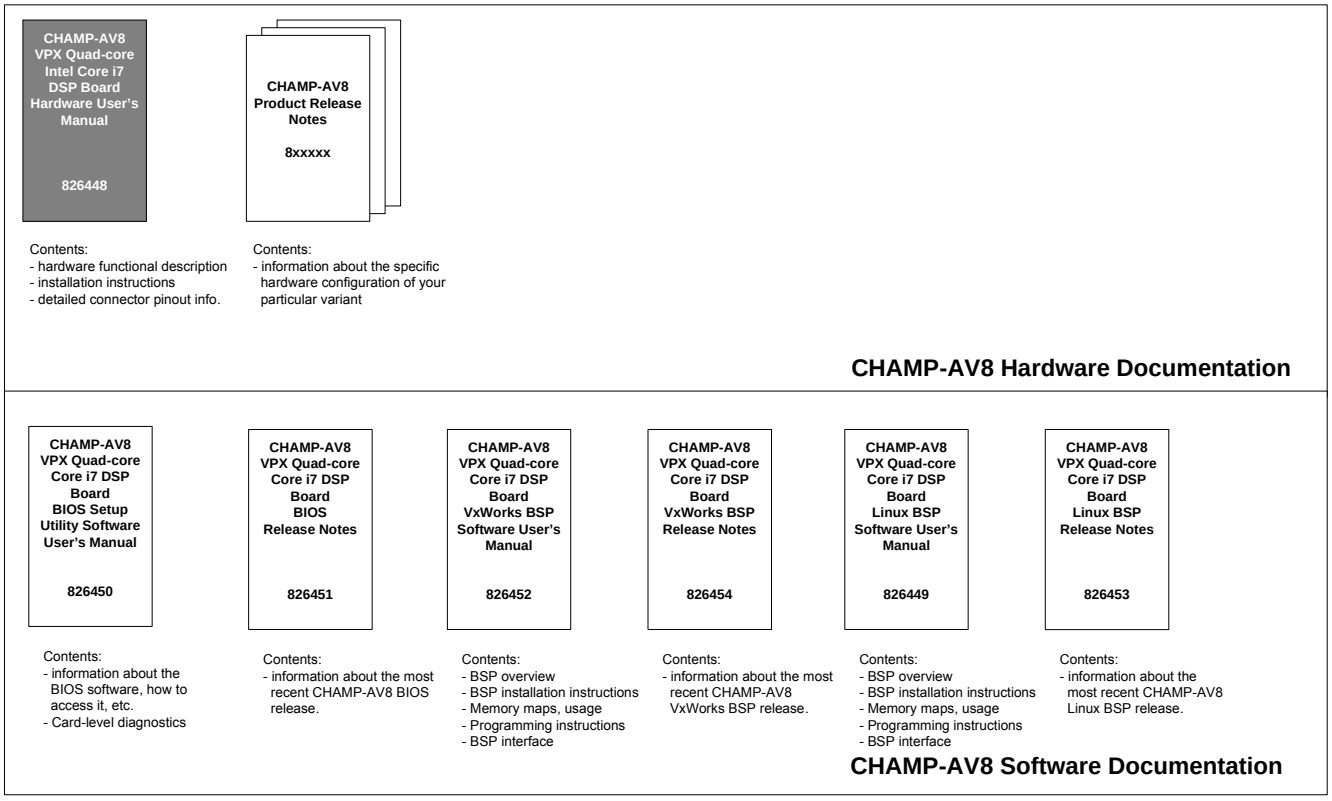
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DOCUMENTATION ROADMAP

The figure below will help you understand what documentation is available for the CHAMP-AV8. These documents are provided in Portable Document Format (PDF) format (readable by Adobe® Acrobat® Reader software), and are available from our Continuum Support Center web site at:

http://csc.cwcdefense.com/

Figure 1: Documentation Roadmap



RELATED SOFTWARE DOCUMENTS

For information on installing the CHAMP-AV8 software, refer to the CHAMP-AV8 Linux BSP Software User's Manual, Curtiss-Wright document number 826449. Alternatively, installation information can be found in the CHAMP-AV8 VxWorks BSP Software User's Manual, Curtiss-Wright document number 826452.

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REFERENCE DOCUMENTATION

Refer to the following standards for information about the specifications the CHAMP-AV8 is designed for compliance with:

- VITA 46.0-2007 - Advance Module Format, R1.2
- VITA 46.3 - 4x Serial RapidIO Signal Mapping for VITA 46, Revision 0.5
- VITA 46.4 - PCI Express Mapping and Advanced Switch Signal Mapping for VITA 46, Draft 0.5
- VITA 46.9 - VITA 46 PMC/XMC Pinout Mapping, Revision 0.9
- VITA 46.10 - Rear Transition Module for VITA 46, Revision 0.08
- VITA 42.0 - XMC Specification, Revision 0.29
- VITA 42.3-2006 - XMC PCI Express Protocol Layer Standard
- VITA 48.0 - Enhanced Rugged Design Implementation, Draft 0.17
- VITA 48.1 - Air Cooling applied to VITA 46, Draft 0.20
- VITA 48.2 - Conduction Cooling applied to VITA 46, Draft 0.14
- VITA 65 - OpenVPX System Specifications, ANSI/VITA 65-2010
- PCI Express Base Specification Revision 2.1., March 4, 2009, PCI-SIG
- Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange, ANSI/TIA/EIA-232-F-1997, September 30, 1997
- RapidIO Interconnect Specification, Part IV: Physical Layer 1x/4x, LP Serial Specification, Revision 1.2, June 2002
- Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange, ANSI/TIA/EIA-232-F-1997, September 30, 1997
- Electrical Characteristics of Balanced Voltage Digital Interface Circuits (ANSI/TIA/EIA-422-B-1994) (R2000) (R2005), May 1994
- XMC PCI Express Protocol Layer Standard, ANSI/VITA 42.3-2006, 2006
- IEEE Standard for Information Technology, Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, IEEE 802.3-2008, 2008

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CONVENTIONS USED IN THIS MANUAL

This manual uses various icon conventions and abbreviations to make the information clearer and easier to read. These conventions cover typography for such elements as sample software code and keystrokes, signal meanings, and graphical elements for important information such as warnings or cautions.

Product Naming Conventions

The generic product name "CHAMP-AV8" is used throughout this manual to represent the following more specific product variants:

- VPX6-462-A (commercial non-ruggedized or air-cooled rugged version of the CHAMP-AV8)
- VPX6-462-C (conduction-cooled rugged version of the CHAMP-AV8)

Typographic Conventions

Table 1 lists the typographical conventions used in this documentation package.

Table 1: Typographic Conventions

Item	Convention	Example
Keystrokes	Keys are listed as they appear on most keyboards, surrounded by < > marks. Combinations of key-strokes appear within a single set of < > brackets.	Type < Ctrl-Alt-C > to return to the previous menu. Type < Esc > to exit.
File Names	File names are set in italics.	Copy the file named *bootA.exe.*
Directory Names	Directory names show the full directory path. The last directory in the path does not have a trailing slash following it.	Go to the *c:\windows\temp\backup* directory.
Monitor Displays and Code	Prompts and other text appearing on monitors is set in monospace type (Lucida Console font).	`Copyright (c) 2015, Curtiss-Wright Controls, Inc.`
Text entered	Any information you need to enter is set in bold monospace type (Lucida Console font).	**yes**
Monitor Com-mands	Within paragraphs, monitor commands are shown in bold face.	**fwupd**

Signal Conventions

Table 2 lists symbols that can follow a signal name. For example, the asterisk (*) is used with a VMEbus signal name, such as BERR*.

Table 2: Signal Conventions

Symbol	Description
_H	The signal is active HIGH.
_L	The signal is active LOW.
P	The signal is the positive signal in a differential pair.
N	The signal is the negative signal in a differential pair.

Abbreviations

Table 3 on page xvii lists the abbreviations used to describe the size of a memory device or a range of addresses.

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Table 3: Memory Size Abbreviations

Abbreviation	Convention
1 Kbyte	1,024 bytes
1 Mbyte	1,024 Kbytes
1 Gbyte	1,024 Mbytes

Acronyms

The following is a list of acronyms associated with the CHAMP-AV8 product:

AC	Alternating Current
ANSI	American National Standards Institute
AT	Anti-Tamper
BIT	Built-In Test
BMC	Baseboard Management Controller
BT	Base-T (Ethernet)
CBIT	Continuous Built-In Test
CCA	Circuit Card Assembly
CHF	Common Hardware Features
CLD	Card Level Diagnostics
CPU	Central Processing Unit
DC	Direct Current
DDIO	Differential Discrete Input Output
DDR	Double Data Rate
DIO	Discrete Input Output
DMA	Direct Memory Access
DVT	Design Verification Test
ECC	Error Correction Code
EEPROM	Electrically Erasable Programmable Read Only Memory
EIA	Electronic Industries Association
EMI	Electro Magnetic Interference
EPROM	Erasable Programmable Read Only Memory
FPGA	Field Programmable Gate Array
GND	Ground
GPIO	General Purpose Input Output
HUM	Hardware User's Manual
I/F	Interface
IBIT	Initiated Built-in Test
I/O or IO	Input/Output
IEEE	Institute of Electrical and Electronic Engineers

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IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LPB	Local Processor Block
LPC	Low Pin Count
MBSC	Multi-Board Synchronous Clock
MTBF	Mean Time Between Failures
NVRAM	Non-Volatile Random Access Memory
PABS	Permanent Alternate BOOT Site
PBIT	Power-up Built-In Test
PCH	Platform Controller Hub
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PCISIG	PCI Special Interest Group
PICMG	PCI Industrial Computer Manufactures Group
PMC	PCI Mezzanine Card
PROM	Programmable Read-Only Memory
PSB	Processor-Specific Block
PWB	Printed Wiring Board
RAM	Random Access Memory
RTM	Rear Transition Module
SATA	Serial ATA
SDRAM	Synchronous Dynamic RAM memory
SHMUART	Shared Memory UART
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SRIO	Serial RapidIO
SSD	Solid State Drive
TPM	Trusted Platform Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VITA	VMEbus International Trade Association
VPD	Vital Product Data
XMC	Switched Mezzanine Card

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Memory Addresses

Unless otherwise stated, all memory addresses are shown in hexadecimal notation.

Icons

The following icons are used throughout the documentation package:



Tip

Tips provide extra information on the subject matter. This could include hints about how to use your current Curtiss-Wright card to its maximum potential.



Note

This is a note. The note icon highlights exceptions and special information.



Caution

This is a caution. The caution icon indicates non-catastrophic incidents, complex practices, or procedures which, if not observed, could result in damage to the hardware. Cautions include specific instructions for avoiding or minimizing these incidents.



Warning

This is a warning. The warning icon indicates procedures in the manual that, if not carried out, or if carried out incorrectly, could cause physical injury, electrical damage to equipment, or a non-recoverable corruption of data. Warnings include instructions for preventing such damage.

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TECHNICAL SUPPORT INFORMATION

If you are unable to resolve installation or configuration-related difficulties using the guidance provided in this document, contact Technical Support or check out the Continuum Support Center web site for additional assistance:

http://csc.cwcdefense.com/

Once registered, you will have online access to additional or updated technical documentation, in addition to software components, etc. as these items become available.

To Access Curtiss-Wright Technical Support

For Technical Support and Repair and Warranty services information, go to the Curtiss-Wright web site:

http://www.cwcdefense.com/

and click on the "SUPPORT" link near the top of the page. This will bring up the following web page:

http://www.cwcdefense.com/support.html

From here you can fine-tune your inquiry:

Type of Request:

- Technical Support
- Repair and Warranty Services

Select By:

- Product Type
- Location
- Former Company Name

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1 PRODUCT OVERVIEW

IN THIS CHAPTER

This chapter discusses the high-level features of the CHAMP-AV8 product. The following topics are discussed:

- "General Description" on page 1-2
- "Feature Summary" on page 1-3
- "Technical Description" on page 1-5
  - "Quad-Core Intel Core i7 Processors" on page 1-6
  - "PCI Express Architecture" on page 1-7
  - "Core Functions FPGA" on page 1-12
  - "Double Data Rate (DDR3) SDRAM with ECC" on page 1-13
  - "Protected Boot Flash Memory" on page 1-14
  - "NAND Flash Memory" on page 1-14
  - "Non-Volatile RAM (NVRAM)" on page 1-15
  - "Non-Volatile Memory Security" on page 1-15
  - "XMC Site" on page 1-15
  - "Utility Features, Semaphores, Timers" on page 1-16
  - "Avionics Style Watchdog Timer" on page 1-16
  - "Multi-board Synchronous Clock" on page 1-17
  - "Serial Ports" on page 1-17
  - "1000Base-T Ethernet" on page 1-19
  - "1000Base-BX Ethernet" on page 1-20
  - "USB and SATA Interfaces" on page 1-20

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  - "LVTTL Discrete Digital I/O" on page 1-21
  - "EIA-422 Differential Discrete Digital I/O" on page 1-21
  - "Voltage, Current, and Temperature Sensors" on page 1-22
  - "Indicator LEDs" on page 1-23
  - "Cables and Rear Transition Modules" on page 1-24
  - "RTC/CMOS RAM Backup Power" on page 1-24
  - "Interrupt Controller" on page 1-24
- "Specifications" on page 1-31
  - "VPX Compliance" on page 1-31
  - "Power Requirements" on page 1-32
  - "Dimensions" on page 1-33
  - "Weight" on page 1-33
  - "Ruggedization Levels" on page 1-34
- "Physical Characteristics" on page 1-35
  - "VPX6-462-A Front Panel" on page 1-37
  - "Mating Connectors" on page 1-39
- "Overview of Available Software" on page 1-40
  - "Built In Test (BIT) Firmware" on page 1-40
  - "Operating System Software" on page 1-40
  - "Continuum IPC™ Library" on page 1-40
  - "Continuum Vector™ Library" on page 1-41

GENERAL DESCRIPTION

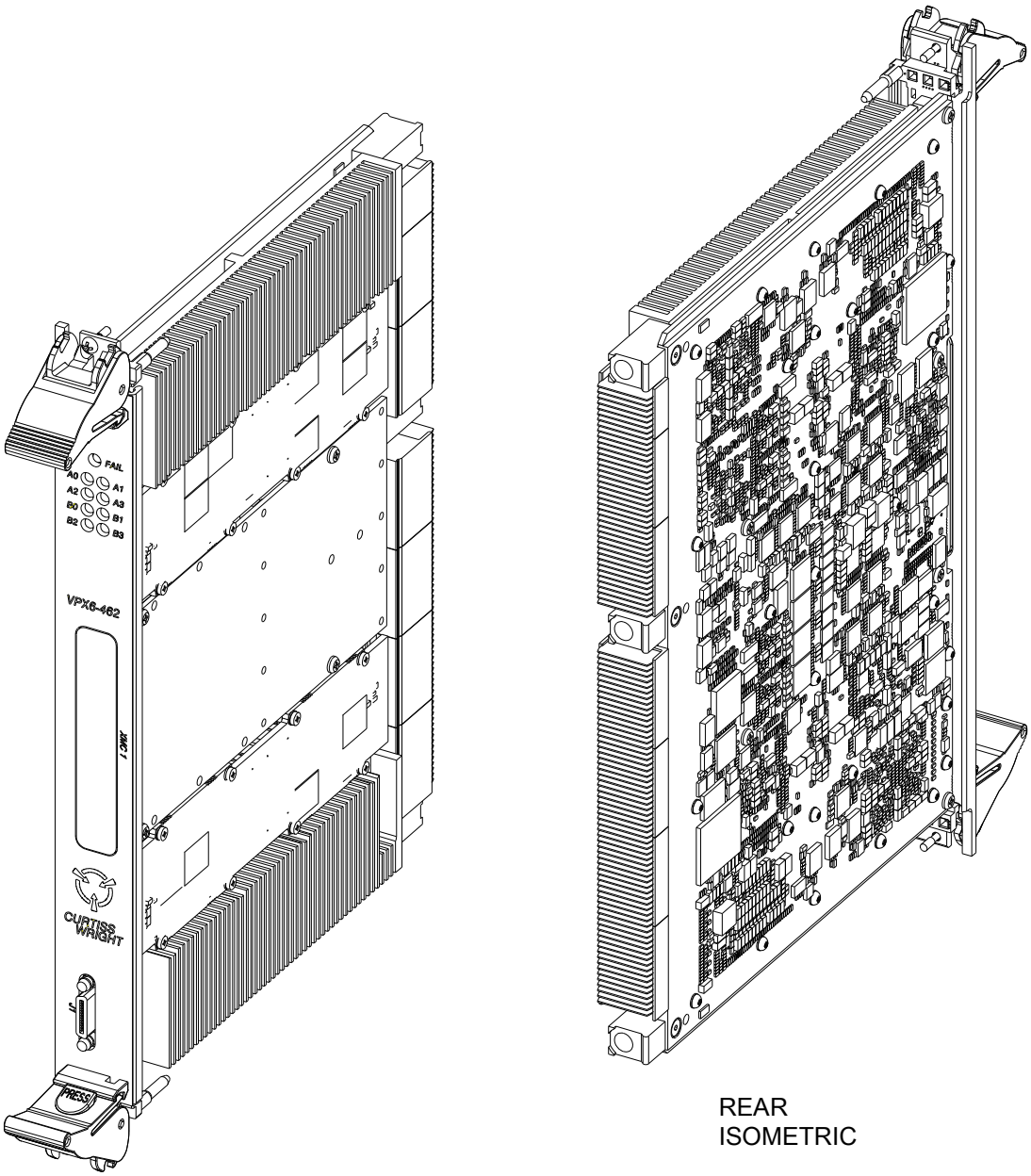
The CHAMP-AV8 multi-processing board brings the floating point performance of the Intel Core i7 architecture to VPX form factor standard. Utilizing a pair of second generation Intel i7-2715QE or third generation Intel i7-3612QE quad-core processors, the CHAMP-AV8 delivers up to 269 GFlops of performance.

The CHAMP-AV8 features a high-bandwidth PCIe architecture, featuring on-board PCIe connections between the processors and the PMC/XMC site. With 8GB of user flash and 4GB of SDRAM per node, the CHAMP-AV8 handles applications with demanding storage, data logging and sensor processing needs.

The CHAMP-AV8 is supported with an extensive suite of software, including support for Linux and VxWorks. Under the VxWorks OS, the Continuum Interprocessor Communication (IPC) and Continuum Vector SSE optimized signal processing libraries are also available.

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Figure 1.1: Air-Cooled CHAMP-AV8 Isometric View



FEATURE SUMMARY

- Two Intel® Core™ i7 second (i7-2715QE) or third (i7-3612QE) generation processors running at up to 2.1GHz
- Hyper-threading technology
- Up to 269 GFlops computing performance
- 4GB DDR3 SDRAM with ECC per processor

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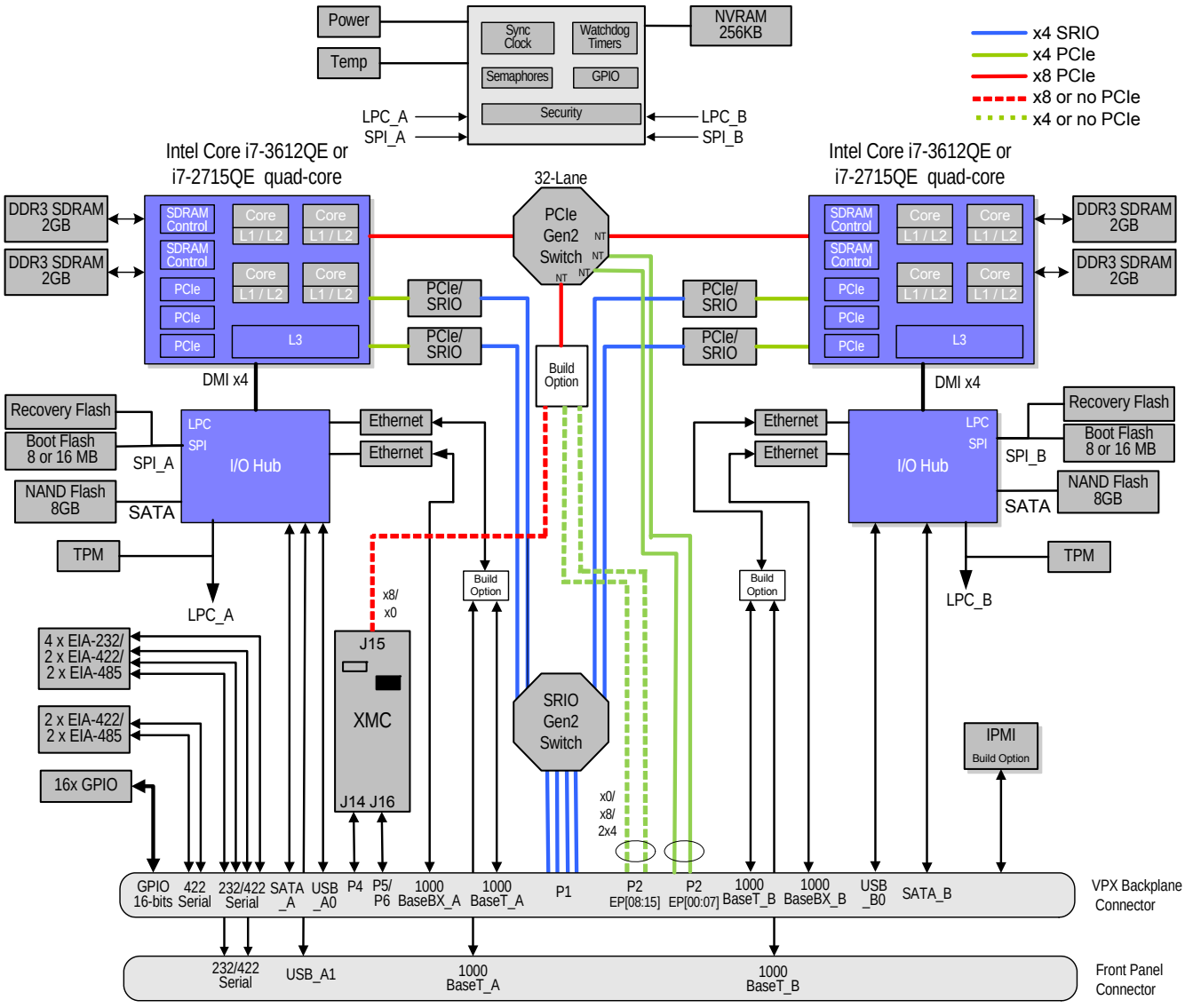
- 8 GB NAND flash on SATA per processor
- Protected backup boot flash
- 256 KB NVRAM
- Secure write-protection on all non-volatile memory
- De-classify function to erase non-volatile memory
- Trusted Platform Management (TPM)
- PCI Express® (PCIe) local fabric with 2 GB/s bi-directional inter-processor bandwidth
- Gen2 Serial RapidIO® (sRIO) Data Plane interface, 8 GB/s bi-directional bandwidth (5 Gbps data rate, default setting)
- On-board Gen2 sRIO switch
- Gen2 PCIe Expansion Plane interface on P2, up to 8 GB/s bidirectional bandwidth
- Eight-channel PCIe DMA controller to off-load CPUs
- Two 1000Base-T Ethernet interfaces
- Two 1000Base-BX Ethernet interfaces
- One XMC mezzanine site
- Serial ports: each node has one EIA-422 port always present, plus either two EIA-232 ports or one EIA-422 port (software configurable)
- Three USB 2.0 interfaces
- Two eSATA interfaces
- 16 LVTTL I/O signals with interrupt
- Differential discrete I/O
- 12 general purpose timers
- Avionics watchdog timer
- 16 semaphore registers
- Multi-board synchronous clock feature
- Temperature sensors, Voltage and current sensors for measuring power consumption
- User-variable processor frequency to control power consumption
- Continuum Software Architecture firmware
- VxWorks® 64-bit BSP supporting SMP
- Fedora 64-bit BSP supporting SMP
- Continuum Vector™ AVX/SSE optimized DSP function library
- Continuum Insights multi-processor development tools
- Continuum IPC inter-processor communications library
- Range of air- and conduction-cooled ruggedization levels available
- VITA 48 1" pitch
- VITA 65 compliant with the MOD6-PAY-4F1Q2U2T-12.2.1-11/12 module profile.

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TECHNICAL DESCRIPTION

With reference to the high level block diagram illustrated in Figure 1.2 below, the operation of the CHAMP-AV8 is described in the following sections.

Figure 1.2: CHAMP-AV8 Functional Block Diagram



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QUAD-CORE INTEL CORE I7 PROCESSORS

The CHAMP-AV8 incorporates two second or third generation Intel Core i7 quad-core processors, which are a low power embedded implementation of micro-architecture code name Sandy Bridge. A major advancement for DSP applications is the introduction of the 256-bit AVX floating-point instructions. The AVX vector unit is backwards compatible with SSE instructions and doubles the peak floating-point performance over the previous generation. At 2.1 GHz, each Core i7 processor provides a peak 135 GFlops. With two processors, the CHAMP-AV8 provides 270 GFlops of performance.

Featuring a dual-channel, 1333 MHz DDR3 SDRAM interface, each CPU has a peak memory bandwidth of 21 GB/s. The 2nd and 3rd generation Core processors feature many improvements in the cache subsystem designed to increase hit-rate and lower latency. Each core contains first-level instruction and data caches (32 KB, 4-way) and a second level unified cache (256 KB, 8-way).

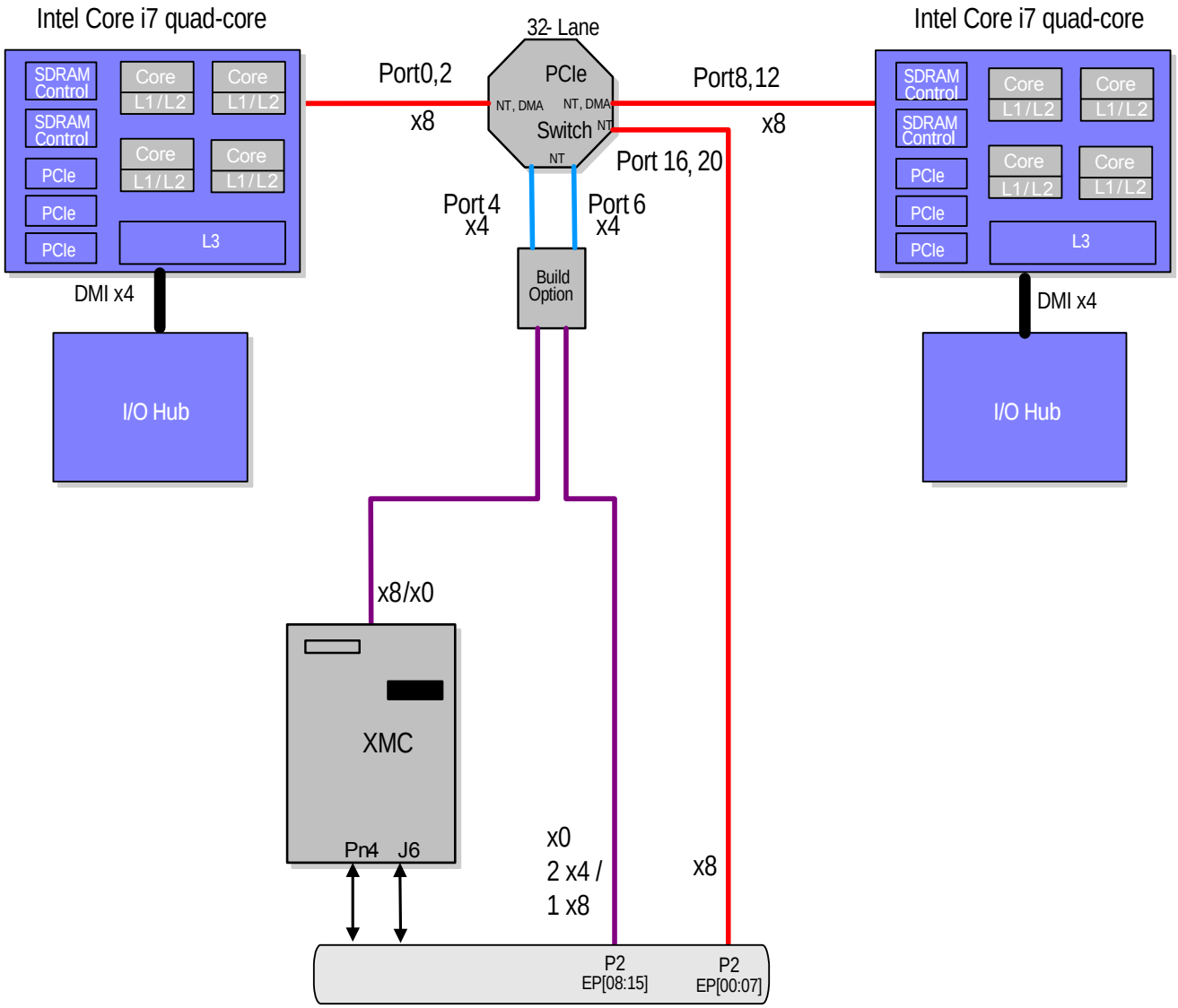
A large third level cache (6 MB 16-way) is shared between all processor cores. Intel's Hyper-Threading technology enables each core to execute two software threads concurrently. Hyper-Threading results in a higher utilization rate of the CPU execution units and thus a greater rate of instructions per unit of time.

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PCI EXPRESS ARCHITECTURE

The CHAMP-AV8 makes use of the PCIe interfaces included in the CPU to share and transfer data between the processors, between cards via the P2 Expansion Plane connectors, and to communicate with the XMC site, as shown in Figure 1.3 below.

Figure 1.3: CHAMP-AV8 PCI Express Distribution



Each processor connects with an on-board PCIe switch via an 8-lane Gen2 PCIe interface. The PCIe switch features non-transparent ports allowing each processor a full memory map, and access to the memory of the other processor. The CHAMP-AV8 presents two PCIe ports to the P2 expansion plane connector to form connections to I/O devices and/or other cards enabled with PCIe on P2 (such as the CHAMP-AV8). See Table 1.1, "XMC/Expansion Plane Interface Build-Time Options for PCIe," on page 1-8 for details. PCIe switch ports connected to P2 and/or the XMC site may be configured to enable or disable non-transparency, and may therefore be used with endpoints or root complexes.

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Note

The standard XMC connector defined by VITA 42.0-2008, and used on the CHAMP-AV8, is rated for signalling rates of at least 3.125GHz. The CHAMP-AV8 is designed to maximize signal integrity; however, PCIe Gen 2 speeds (5GHz) are not guaranteed to properly function to the XMC site.

Table 1.1: XMC/Expansion Plane Interface Build-Time Options for PCIe

XMC	EP[00:03]	EP[04:07]	EP[08:11]	EP[12:15]
x8	x4	x4	N/C	N/C
x8	x8		N/C	N/C
N/C	x4	x4	x4	x4
N/C	x8		x8	

Notes
1. The EPxx references are from the VITA 65 specification which defines the mapping of x4/x8/x16 ports to the P2 connector. The CHAMP-AV8 does not support x16 configurations.
2. The standard product configuration is XMC x8, EP00-EP07 x8, EP08-EP15 N/C (the second highlighted row in the table). Contact the factory for other configurations, due to build-time option requirements.
3. N/C = No connection

Enabled by the ability to configure non-transparent ports and partitions in the PCIe switch, there are no limitations due to multiple root complexes within the PCIe network. The PCIe Switch also features a four-channel DMA controller. The DMA offloads data movement overhead from the processors and is typically used to move data between processors and to/from the XMC and/or Expansion Plane devices. The DMA controllers operate from a descriptor queue in memory and features source and destination address striding, to facilitate data reorganization needs.

The PCIe switch is capable of internal partitions, which may be reconfigured from the BIOS. For further details, please see Appendix A in the CHAMP-AV8 BIOS Software User's Manual, Curtiss-Wright document 826450.

The default partition is illustrated in Figure 1.4, "PCIe Switch Partitions," on page 1-9. With this default partition, PCIe circuitry on the XMC site or EP[08:15] (depending on the build option selected) is enumerated by CPU A and cannot be addressed directly from CPU B. PCIe circuitry interfaced to EP[00:07] is enumerated by CPU B and cannot be addressed directly from CPU A.

Some XMC cards may contain graphics or boot devices, such as SATA drives and PXE Ethernet interfaces. These XMC modules typically require integrated option ROMs to enable proper PCIe enumeration on Intel processor systems.

Note

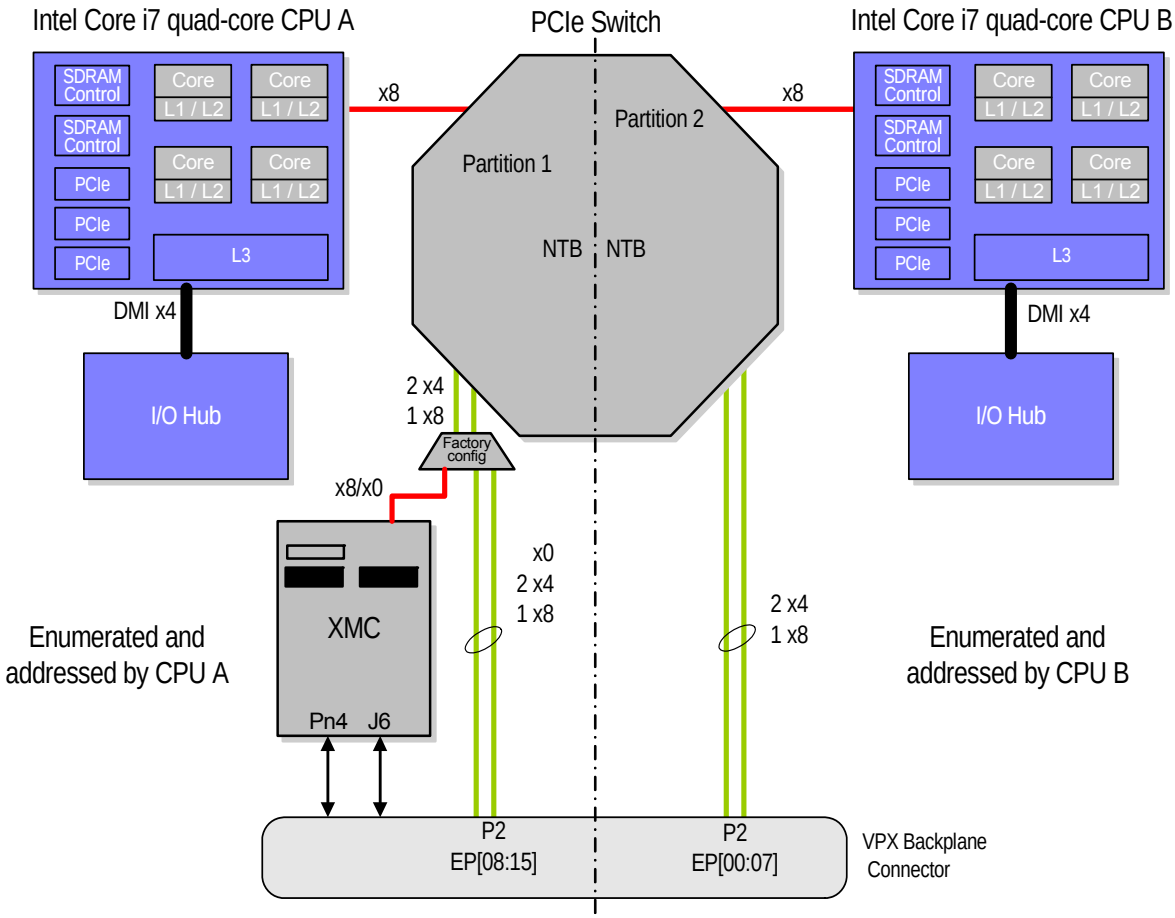
Please consult the factory before selecting a video or boot device XMC for use on the CHAMP-AV8. XMCs without option ROMs may be usable on the CHAMP-AV8, perhaps with a BIOS software modification.

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Note

PCIe connections will typically auto-negotiate their link operating speed if different generations of PCIe are mixed. For example, when mixing older hardware boards such as the VPX6-185 or the CHAMP-AV6 with the CHAMP-AV8, the off-board PCIe links can establish a common link speed in order to communicate. However, PCIe link speed and other off-board PCIe signal parameters can be set to discrete values using BIOS settings. See the BIOS User's Manual, Curtiss-Wright document 826450, for more information.

Figure 1.4: PCIe Switch Partitions



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SRIO FABRIC

The CHAMP-AV8 provides PCIe-SRIO bridge devices and an SRIO Gen2 switch to connect the SRIO backplane fabric with the Intel Processors. Each processor connects to either one or two PCIe-SRIO bridges providing up to 8 GB/s total bandwidth on-board. An 8-port SRIO switch is connected to the processors and the four ports on the data plane connector via the PCIe-SRIO bridges. This provides both on-board switching as well as off-board SRIO fabric connectivity and enables distributed switching architectures, avoiding the need for a separate switch card. The PCIe-SRIO bridges operate at a SRIO link maximum rate of 5Gbps.

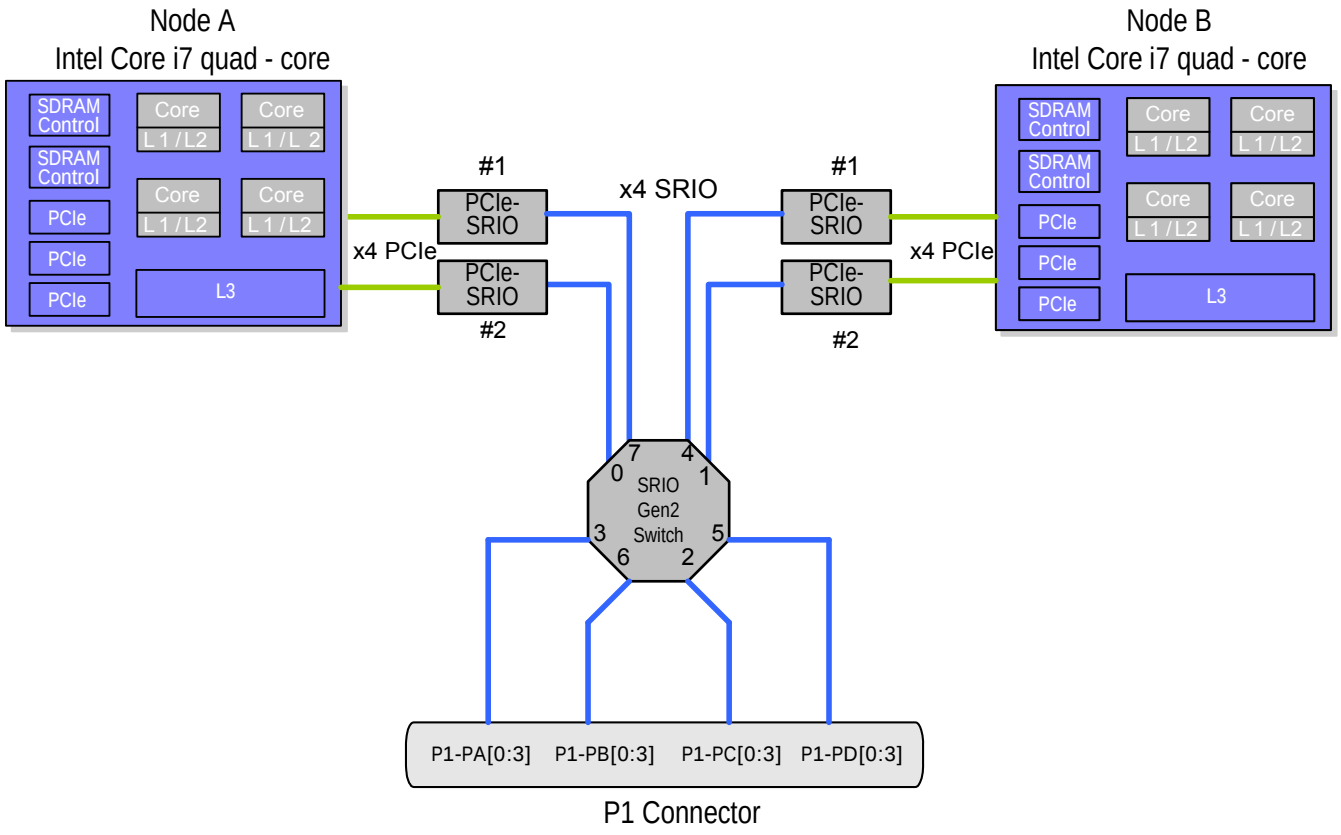
Multiple CHAMP-AV8 cards may be connected using the SRIO fabric interface. Table 1.2 below and Figure 1.5 on page 1-11 show the SRIO port numbers and mapping to the processor and the backplane.

Table 1.2: CPS-1432 SRIO Switch Port Numbering

SRIO Switch Port	Connection
0	Node A PCIe-SRIO Bridge 2
1	Node B PCIe-SRIO Bridge 2
2	Backplane Port C
3	Backplane Port A
4	Node B PCIe-SRIO Bridge 1
5	Backplane Port D
6	Backplane Port B
7	Node A PCIe-SRIO Bridge 1

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Figure 1.5: CHAMP-AV8 SRIO Port Connections



Note

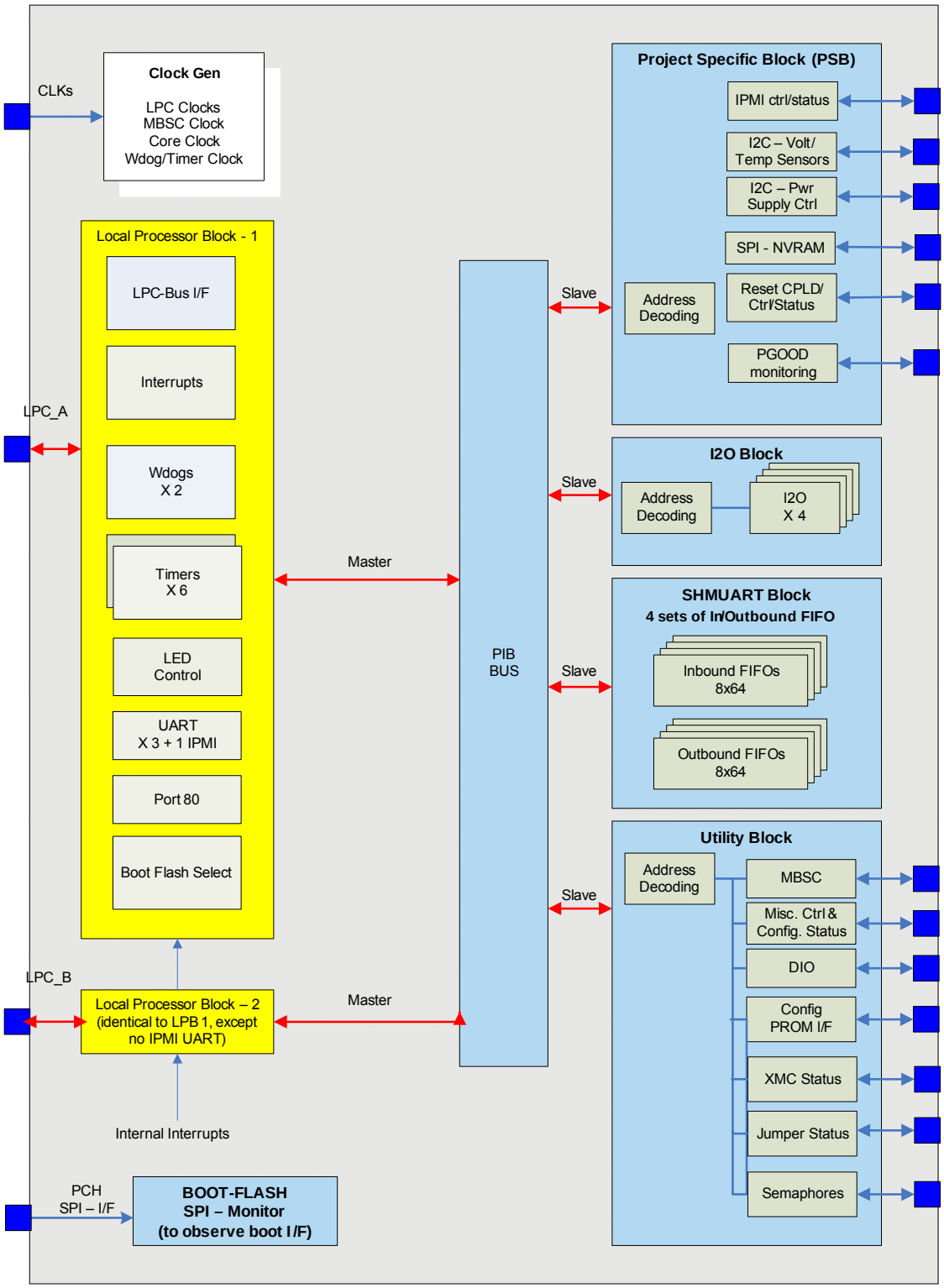
SRIO connections do NOT auto-negotiate their link operating speed if different generations of SRIO are mixed. For example, when mixing older hardware boards such as the VPX6-185 or the CHAMP-AV6 (which support Gen 1 speed, 3.125 Gbaud) with the CHAMP-AV8 (defaults to Gen 2, 5.00 Gbaud, but supports 3.125 Gbaud) the off-board SRIO link speed must be set to values supported on both boards. In this case the CHAMP-AV8 would be down-graded to the Gen 1 speed. See the BIOS User's Manual, Curtiss-Wright document 826450, for more information.

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CORE FUNCTIONS FPGA

The Core Functions FPGA (CF-FPGA) is illustrated in block diagram format below in Figure 1.6.

Figure 1.6: Core Functions FPGA Block Diagram



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The Core Functions FPGA provides a set of internal resources and interfaces to external devices accessible by the processor on the board. Each processor node accesses the FPGA with a Low Pin-Count (LPC) bus through its associated Platform Controller Hub (PCH). The FPGA connects to the two LPC buses through two Local Processor Blocks (LPB). In addition to the LPC interface function, the LPB contains a set of resources unique to the node that are inaccessible to the other node. The Processor Interface Block (PIB) arbitrates and passes transactions from the LPC bus to the shared resources. The PIB acts as a switch fabric between the LPB and the shared resources. The shared resources accessible by all nodes are located in the Project Specific resources Block (PSB), the Utility Block (UB), System Monitor, I2O, and SHMUART.

I2O Block

The CHAMP-AV8 includes an I2O block. There are four separate I2O modules in the I2O block (one per processor core).

Each module consists of:

- Inbound Doorbell Register
- Inbound Buffer Free Queue
- Inbound Buffer Post Queue
- Outbound Message Register

The I2O Inbound Doorbell Registers send and receive short messages between CPUs with access to global memory space. Each I2O unit has four 32-bit Inbound Doorbell Registers, each assigned to an owner CPU. The owner CPU for each register is software-configurable. This allows other CPUs in the fabric to communicate directly with the owner. Writing to an Inbound Doorbell Register causes an interrupt request to the owner CPU. As with the Doorbell Registers, there are four 32-bit Inbound Message Queues, each with an owner. Each queue holds 512 messages. The Inbound Post Queue holds posted messages from the fabric to owner CPUs. The owner CPU fetches the next message process from the queue tail; a CPU posts messages to the queue head. The Inbound Free Queue holds available inbound free messages (data buffer addresses) for CPUs to use. The owner CPU places free messages at the queue head; CPUs fetch free messages from the queue tail. The outbound message register is simply a 32-bit register used by the owner CPU to advertise his Processor ID to the rest of the fabric. The owner CPU writes this register and the non-owner reads it.

DOUBLE DATA RATE (DDR3) SDRAM WITH ECC

Each processor node on the CHAMP-AV8 supports up to 4GB of DDR3 SDRAM for a total of 8GB on the board. Each processor features two DDR3 memory channels. With two channels of DDR3-1333, each processor achieves a peak memory bandwidth of over 21GB/s. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors.

The memories reside on a separate module, one per node, and connect to the base board via stacking connectors.



Note

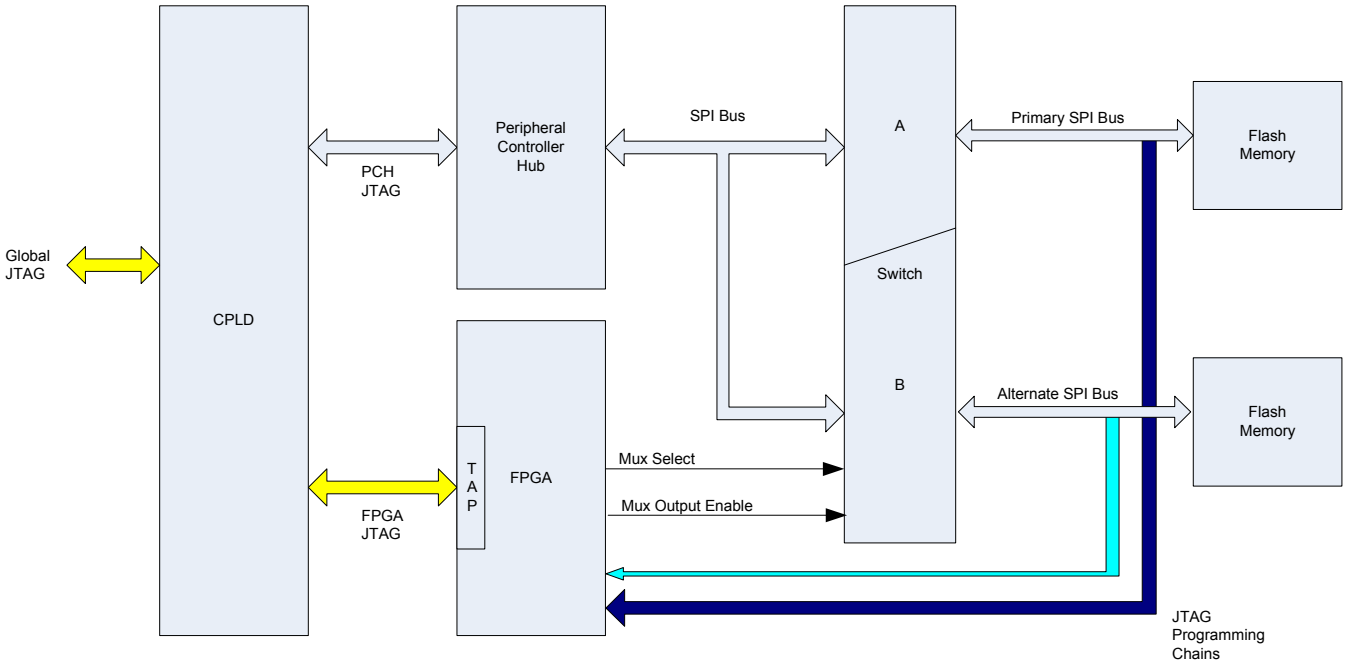
Consult the factory for updated information on the availability of the 8GB variant of the CHAMP-AV8.

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PROTECTED BOOT FLASH MEMORY

Each processor is equipped with NOR Flash memory used to store the system BIOS and Power-on Built-In Test (PBIT) diagnostics firmware. Boards with the second generation Core processor i7-2715QE have an 8MB NOR Flash. Boards with third generation Core processor i7-3612QE have a 16MB NOR Flash. In the event of accidental corruption of the primary boot Flash, the CHAMP-AV8 is fitted with secondary boot Flash devices (also known as the Permanent Alternate Boot Site, or PABS). Thus, each processor node contains two 8MB NOR Flash devices—one for main boot flash and one for PABS.

Figure 1.7: Boot Flash SPI Bus Architecture



By application of a common hardware jumper, or assertion of a backplane signal (ALT_BOOT_L), both processors will boot from the secondary flash (PABS) to regain operation of the card and recovery of the primary flash. Both primary and secondary boot flash devices feature hardware write-protection jumpers (JB7 for the primary boot flash and JB5 for the secondary boot flash - see Table 2.3, "Jumper Block Definition," on page 2-7 for more details).

NAND FLASH MEMORY

The CHAMP-AV8 features 8 GB of NAND flash per processor (16 GB total per CHAMP-AV8) for storage of the operating system and user application software. A SATA interface connects the PCH to a NAND flash-based Solid State Drive (SSD). Software accesses the flash via the operating system file system. The SSD contains a Flash Controller that implements bad block management and wear levelling functions. For maximum reliability and longevity, Single Level Cell (SLC) technology flash devices are used. Hardware jumpers are provided to disable write access to the NAND flash (jumper, JB1) – see Table 2.3, "Jumper Block Definition," on page 2-7 for more details.

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NON-VOLATILE RAM (NVRAM)

A 256 KB non-volatile memory device based on ferro-electric technology (F-RAM) provides non-volatile storage of mission state data that must be preserved when power is removed.

During normal operation, application software views the NVRAM like a standard SRAM, except that data is retained after power is removed. A serial interface NVRAM is used on the CHAMP-AV8, accessible via API functions. Both processors have access to the NVRAM device via the Core Functions FPGA. Data written to the NVRAM is immediately non-volatile.

The device is rated for a minimum of 100 Trillion (10^{14}) read/write cycles. The data retention period is >10 years. For security against inadvertent writes to NVRAM, a hardware write-protection feature is provided (jumper, JB6) – see Table 2.3, “Jumper Block Definition,” on page 2-7 for more details.

NON-VOLATILE MEMORY SECURITY

The CHAMP-AV8, as well as other Curtiss-Wright Controls Continuum Architecture products, provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices, boot flash, backup boot flash, NAND flash, NVRAM and FPGA PROM may be write-protected by hardware jumpers. The jumpers may be visually inspected to conform to security procedures. The firmware of the CHAMP-AV8 provides a non-volatile memory scrub function to perform a secure erase per NISPOM requirements. See Appendix B, "Statement of Memory Volatility" for details of memory devices present on the CHAMP-AV8.

XMC SITE

The CHAMP-AV8 is equipped with one XMC site, as a build option, that provides additional user I/O on a P14 connector. This site complies with ANSI/VITA 42.0 and ANSI/VITA 42.3.

The CHAMP-AV8 uses a 10 mm XMC stacking height.

The XMC site's PCIe interface connects to an on-board PCIe Switch. By default, the PCIe Switch is partitioned such that CPU A enumerates the XMC's PCIe network. CPU B can access the XMC site via a non-transparent buffer in the PCIe switch. For more details about the PCIe network, partitioning, and changing partitions, refer to section “PCI Express Architecture” on page 1-7, along with the CHAMP-AV8 BIOS Software User's Manual, Curtiss-Wright document 826450.

Certain XMC modules, such as graphics cards and boot devices, require option ROMs to enable proper boot-time PCIe network enumeration on the CHAMP-AV8. Without an option ROM present on such XMCs, a BIOS modification may be required to build in option ROM support.



Note

Please consult the factory prior to installing a video or boot device XMC on the CHAMP-AV8.

XMC modules are supported per the VITA 42.3 standard. The XMC-only site is equipped with an 8-lane PCIe Gen 1 interface providing up to 2 GB/s transmit and 2 GB/s receive simultaneously. Additional I/O capability is provided by site connectors J16 and J14. Because of the large number of possible connections between these connectors and the backplane, VITA 46.9 defines a number of connection profiles. The pins on J16 are routed to the backplane as described in the connection profile: P5w3P6-X38s+X8d+X12d. The pins on J14 are routed as differential pairs to the backplane as described in the connection profile: P3w1-P64s.

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UTILITY FEATURES, SEMAPHORES, TIMERS

The CHAMP-AV8 features a number of utility features to facilitate multi-processor application software. The board provides 16 hardware semaphore registers which are useful to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques, and avoids the use of shared memory to access the semaphores.

The CHAMP-AV8 provides six general purpose 32-bit timers. These may be configured for a timeout value between 20ns and 85 seconds, with a resolution of 20ns. Each timer may be configured to generate an interrupt to either processor. The current timer value may be read at any time by software. Up to two timers may be reserved to support operating system features.

AVIONICS STYLE WATCHDOG TIMER

The CHAMP-AV8 provides two watchdog timers for each processor. Each watchdog timer is a pre-settable down-counter with a resolution of 1 µsec. Time-out periods from 0ms to 33.6 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts. The watchdog timer can be used in two ways:

- As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register.
- For increased system integrity, the watchdog can be configured to operate in "Avionics" mode, whereby a minimum interval between writes to the watchdog register is also enforced. Writing to the watchdog register too soon or too late causes an exception event.

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MULTI-BOARD SYNCHRONOUS CLOCK

The CHAMP-AV8 includes a special purpose counter which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. The counter can be set to roll-over to a pre-load value and interrupt on rollover. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors.

SERIAL PORTS

The CHAMP-AV8 provides six serial ports. Two of these ports, one for each processor, are EIA-422/485 electrical interfaces. The other four serial ports are user-configurable to operate with either EIA-232 or EIA-422/485 electrical interfaces. The default configuration of the four user-configurable ports is EIA-232. When configured to operate in EIA-422/485 mode, one port utilizes the pins that are otherwise used by two EIA-232 ports. The following configurations are possible:

- Four EIA-232, two from each processor node.
- Two EIA-232 from processor node A and one EIA-422/485 from processor node B.
- One EIA-422/485 from processor node A and two EIA-232 from processor node B.
- Two EIA-422/485, one from each processor node.

In both EIA-232 and EIA-422/485 configurations, the ports support transmit and receive signals only. Internally the signals are routed through an FPGA which could optionally be configured to provide a synchronous capability. Consult the factory for more information.

Two ports (one from each processor node, denoted as serial ports A0 and B0) are connected to both the front panel connector (air-cooled cards) and to the backplane connector. Two additional serial ports, one from each processor node and denoted as A1 and B1 are connected to the backplane connector. The serial ports support asynchronous operation up to 115 Kbaud.

EIA-232/422/DDIO Control

CHAMP-AV8 EIA-232/422 Scheme

On the CHAMP-AV8, processor node A has access to four UARTs, and node B has access to three. Two UART ports on each node (A1/A0/B1/B0) are connected to on-board EIA-232/422 transceiver integrated circuits. The EIA-232/422 IC is a dual mode device which can be configured either as (4 x EIA-232) or (2 x EIA-422) transceivers. Another UART in each node (A2/B2) is connected to EIA-422 transceiver chips to form dedicated EIA-422 ports. The remaining UART (A3) is currently unused.

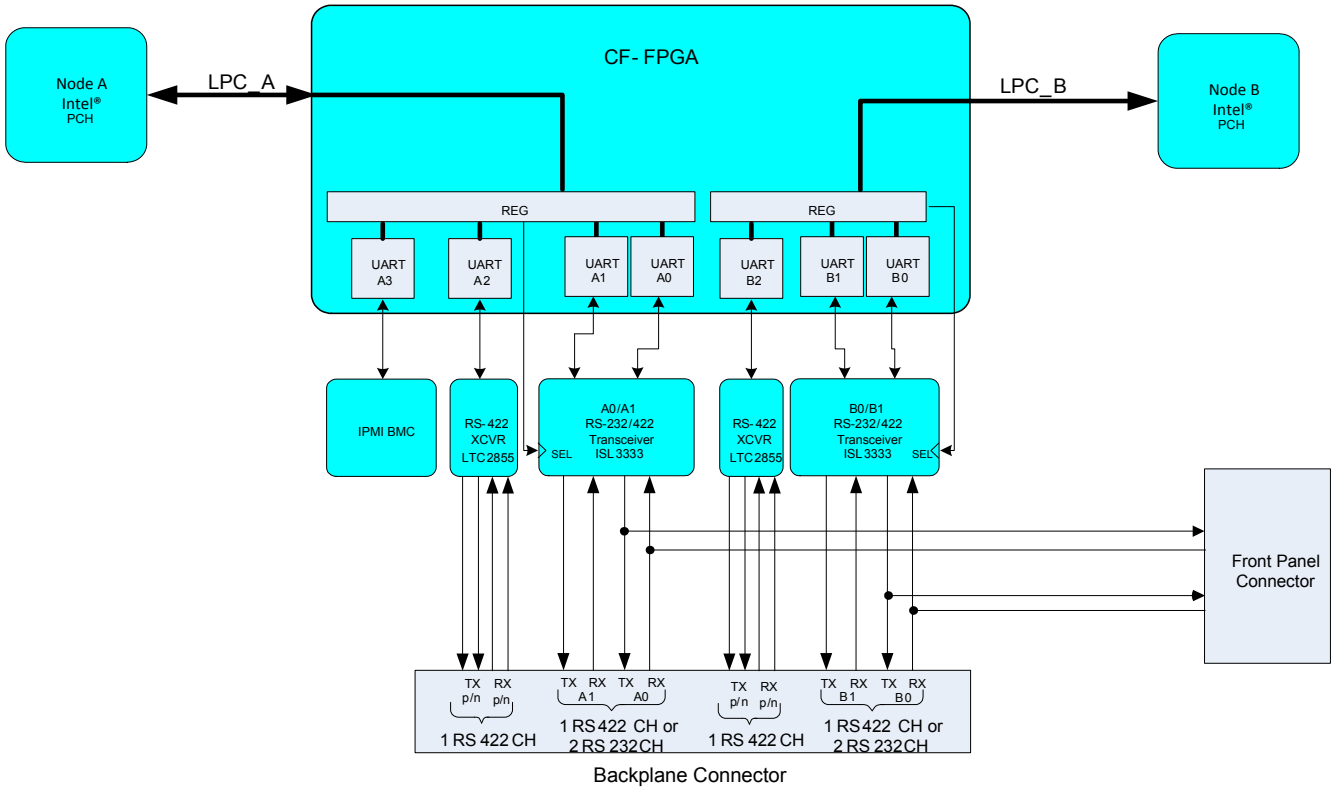
The following combinations are supported by the Core Functions FPGA for serial port multiplexing:

1. Two EIA-232 and one EIA-422 per node (total of six).
2. Two EIA-232 and one EIA-422 from Node A and two EIA-422 from Node B
3. Two EIA-422 from node A and two EIA-232, one EIA-422 from Node B
4. Two EIA-422 per node

When EIA-422 mode is selected for the dual-mode ports on either nodes A or B, UARTs A0/B0 are used to control the EIA-422 channels, and UARTs A1/B1 are disconnected. Figure 1.8 below shows a system-level implementation diagram for the UART and EIA-232/422 transceiver.

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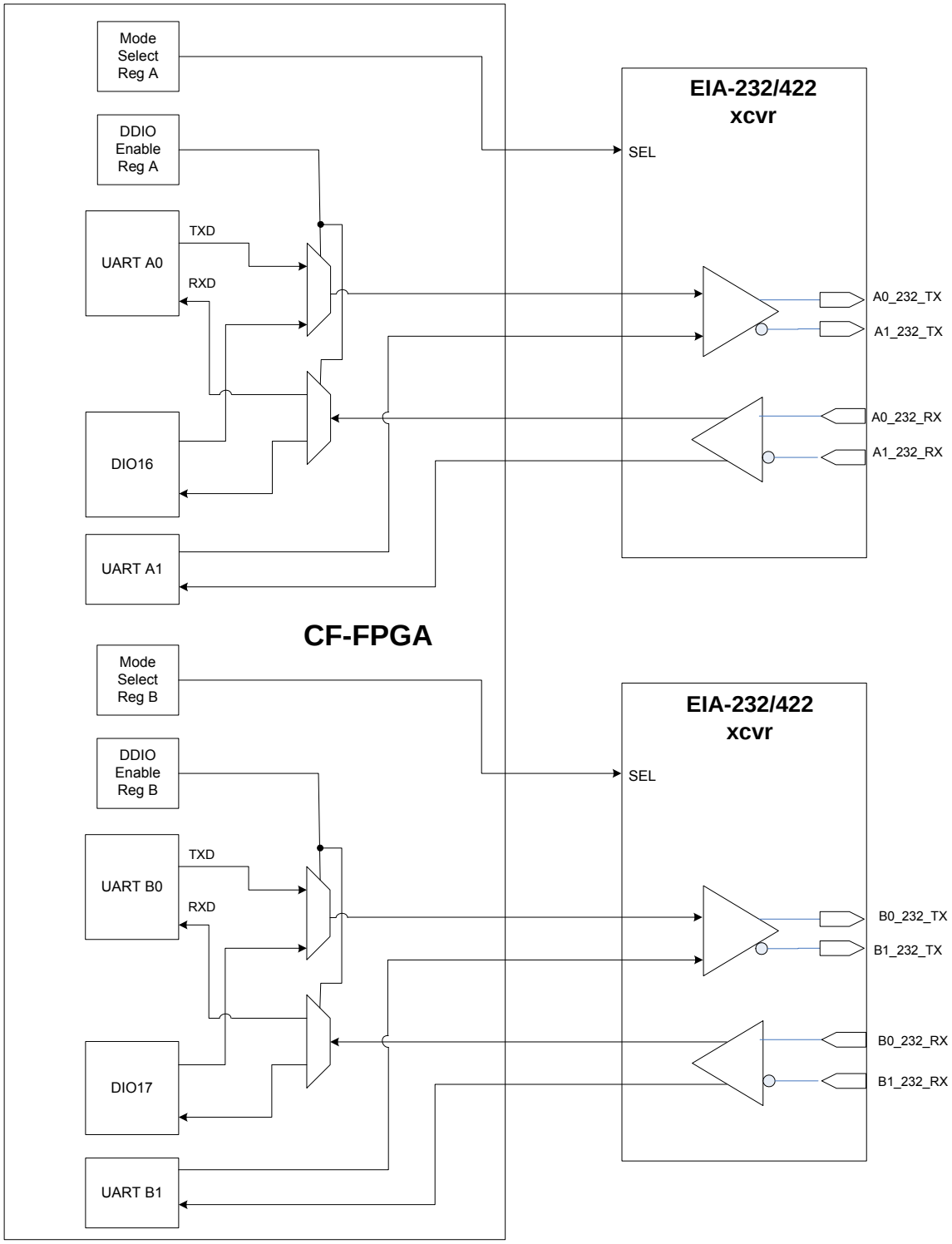
Figure 1.8: CHAMP-AV8 Serial Port Implementation



Access to the two dual-mode EIA-232/422 transceivers are multiplexed by the FPGA between DIO[16] and UART A0 (also between DIO[17] and UART B0). This allows a DIO port to take control of a EIA-422 differential pair, thus forming a DDIO (Differential DIO) port. Figure 1.9, "CHAMP-AV8 Serial Port Detail," on page 1-19 illustrates how the control registers are used to control switching between the DIO registers, UART ports, and the EIA-232/422 dual-mode transceiver.

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Figure 1.9: CHAMP-AV8 Serial Port Detail



1000BASE-T ETHERNET

Each processor on the CHAMP-AV8 is equipped with a 10/100/1000Base-T Gigabit Ethernet interface. On air-cooled versions of the CHAMP-AV8, the Ethernet ports are available at the front panel or backplane connector as a build-time option. For conduction-cooled versions, Ethernet is available via the backplane only.

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1000BASE-BX ETHERNET

Each processor on the CHAMP-AV8 is equipped with a 1000Base-BX Gigabit Ethernet interface. These interfaces are routed to backplane connector P4 in accordance with ANSI/VITA 65. Redrivers are supplied on the CHAMP-AV8 to allow link tuning.

USB AND SATA INTERFACES

USB Interfaces

The CHAMP-AV8 has a total of three USB 2.0 interfaces. Each processor has a USB interface routed to the VPX P6 connector, which is available through the USB/eSATA connector on RTM6-462-000. Node A has an additional USB interface routed to the front panel connector (air-cooled VPX6-462-A only). A current-limited USB power supply is provided for each interface.

USB Port Protection

Each USB port has input supply protection via a current-limiting switch with auto-reset. The switch protects against both overload and short-circuit conditions to guarantee a 500 mA maximum supply load for a high power port (5 unit loads), as specified in the USB Specification Revision 2.0 (para. 7.2.1). Additionally, the switch generates a fault signal to notify the system via the PCH when it detects a thermal overload (160 °C), current-limit, under-voltage lockout, or short-circuit fault.

SATA Interfaces

Each processor node provides a SATA interface to the P6 backplane connector.

RTM6-462-000 provides a USB/eSATA connector that allows external storage access to these SATA interfaces.

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LVTTL DISCRETE DIGITAL I/O

There are 16 Digital I/O (DIO) bits which are accessible at the backplane connector. Each bit is individually programmable to be an input, output, or I/O. Each bit configured as an input may be used to trigger an interrupt which is further programmable to be either level or edge-sensitive. Both levels and transition directions may be detected. Each DIO's input port contains a filtering function that filters all pulses <= 40 ns. The DIO bits are controlled through a set of registers in the CF-FPGA. The DIO bit functions can be programmed independently.

The signals for the lower two DIO bits (DIO[1:0]) can be used as the MBSC synchronization signals as described in the MBSC section. When configured in MBSC mode, the DIO [1:0] cannot function as DIO.

In addition to performing input and output through the processor data lines, the DIO input channels can also be routed to the available Local Processor Block Interrupt Controllers. The DIO registers, together with the Local Processor Block (LPB) interrupt controller, can perform the DIO interrupt handling solution. DIO pin signal level or edge events can trigger interrupts. Each active DIO bit must be unmasked and enabled in the CF-FPGA. The CF-FPGA combines and routes the DIO level interrupts to the appropriate processor interrupt lines.

Each LVTLL I/O line is pulled high to 3.3V with an on-board 10 KOhm resistor located between a FET-based bus transceiver and the CF-FPGA. The digital I/O lines are 5V tolerant at the backplane.

For more information on programming the DIO, consult the BSP User's Manual.

EIA-422 DIFFERENTIAL DISCRETE DIGITAL I/O

The CHAMP-AV8 provides the capability to control the outputs of the two drivers on the dual-mode EIA-232/422 transceivers which are normally controlled by UARTs A0/B0. In a similar fashion, there are registers that can read the state of the EIA-232/422 receivers. In total there are two inputs and two outputs. Each input may be configured to generate an interrupt. When configured as discrete differential I/O, the drivers and receivers are used as general-purpose differential-mode control signals and not as serial EIA-232/422 I/O.

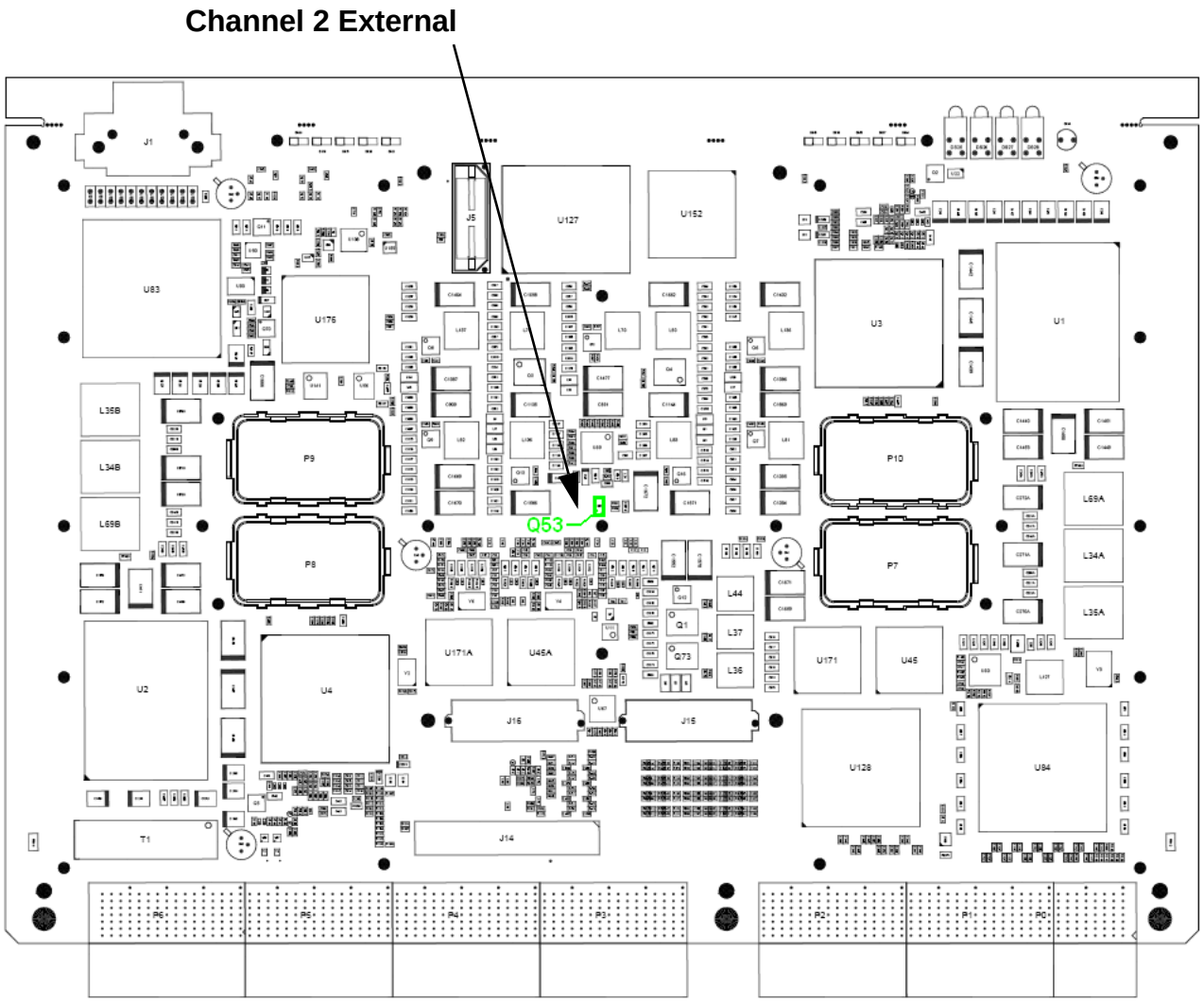
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VOLTAGE, CURRENT, AND TEMPERATURE SENSORS

The CHAMP-AV8 is equipped with a suite of voltage, current, and temperature sensors that provide users with visibility into the environmental conditions encountered by the board. The CHAMP-AV8 features current and voltage sensors for the backplane power rails, enabling the user to measure the instantaneous voltage input and current draw of the entire board. The current drawn by any installed mezzanine module is included in the current measurements. Since the power consumption of the board depends on many factors including the processor clock frequency, the nature of the software, SDRAM loading, and the operating temperature of the board, the ability to measure the actual power for a given application eliminates guesswork in system power consumption estimates.

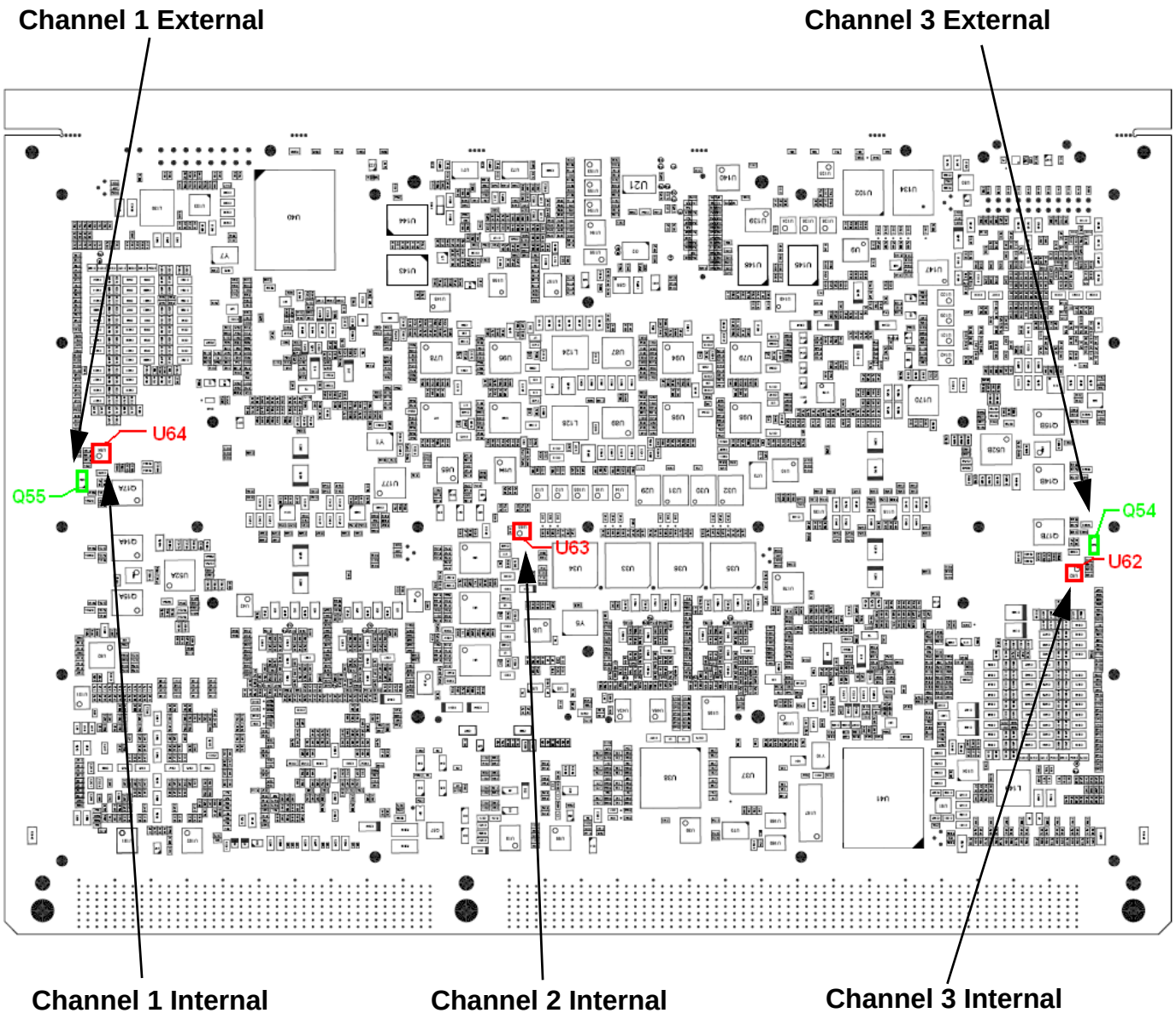
The CHAMP-AV8 also provides a number of temperature sensors. There are sensors for the edges and center of the board, and the processor die. Figure 1.10 (below) and Figure 1.11 on page 1-23 show the locations of the card edge and board center temperature sensors provided on the top and bottom of the CHAMP-AV8 board. The usage of these sensors is described in the BSP manuals. The internal temperature sensor monitoring channels are realized through the use of embedded sensors inside of ADT7461 sensing devices. The external temperature sensor channels are implemented by connecting remote transistors to the external temperature monitoring channels of the ADT7461s.

Figure 1.10: Location of Voltage, Current, and Temperature Sensors (Primary Side)



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Figure 1.11: Location of Voltage, Current, and Temperature Sensors (Secondary Side)



INDICATOR LEDS

The CHAMP-AV8 provides eight user-controllable green LEDs. These are visible on the front panel of air-cooled boards or on the back side of conduction-cooled boards. There is an additional red LED on the front panel of both versions that indicates a failure determined by the on-board diagnostic firmware. A backplane signal is also asserted in conjunction with the fail LED. See "LED Diagnostics" on page 3-14 for additional details.

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CABLES AND REAR TRANSITION MODULES

The CHAMP-AV8 features a high-density front panel connector on air-cooled versions of the board. The connector provides access to two EIA-232 serial ports, two Gigabit Ethernet ports (subject to the Ethernet built-time option), one USB port, and a board reset input. A cable is available that breaks out the signals to a number of standard connectors. See "CBL-462-FPL-000 (903075-000)" on page 2-6 for additional details.

A Rear Transition Module (RTM) is available (part number RTM6-462-000) to provide easy access to the backplane I/O signals. The RTM is a 6U x 80mm (IEEE 1101.10 compliant) module with a rear face plate and injector/ejector handles that plugs into the rear of the VPX backplane to make connections with the I/O signals on the CHAMP-AV8 VPX connectors. The RTM provides connectors for Gigabit Ethernet (2), EIA-232 (4), EIA-422/485 (2), and USB/eSATA (2).

The RTM also features a number of switches and headers for access to other CHAMP-AV8 signals and I/O ports. The RTM is intended for development purposes and is not tested or warranted for deployment. See "RTM6-462-000 Connections" on page 3-11 for more information.

RTC/CMOS RAM BACKUP POWER

Backup power is only supported by the optional VBAT from the backplane.

There are 256 bytes of static RAM within each PCH device that provide real time clock time-keeping functions as well as general purpose storage. Backup power is only supported by the optional VBAT from the backplane. Connect an external 3V power source to the backplane P1-VBAT input (P1-G3). No write protection is provided for this memory.

The CHAMP-AV8 uses a backup power storage system to prolong viability of the RTC during power down and brown outs. This backup power storage is an integrated solution that provides backup energy storage and power management for systems requiring power bridging and/or secondary power.

The capacity of the backup storage device is 50 µAh. The current draw of the RTC circuit (located in the Cougar Point PCH) with power removed is 6 µA, at room temperature. Therefore, the battery life when the board is powered down at room temperature is approximately 5.83 hours.

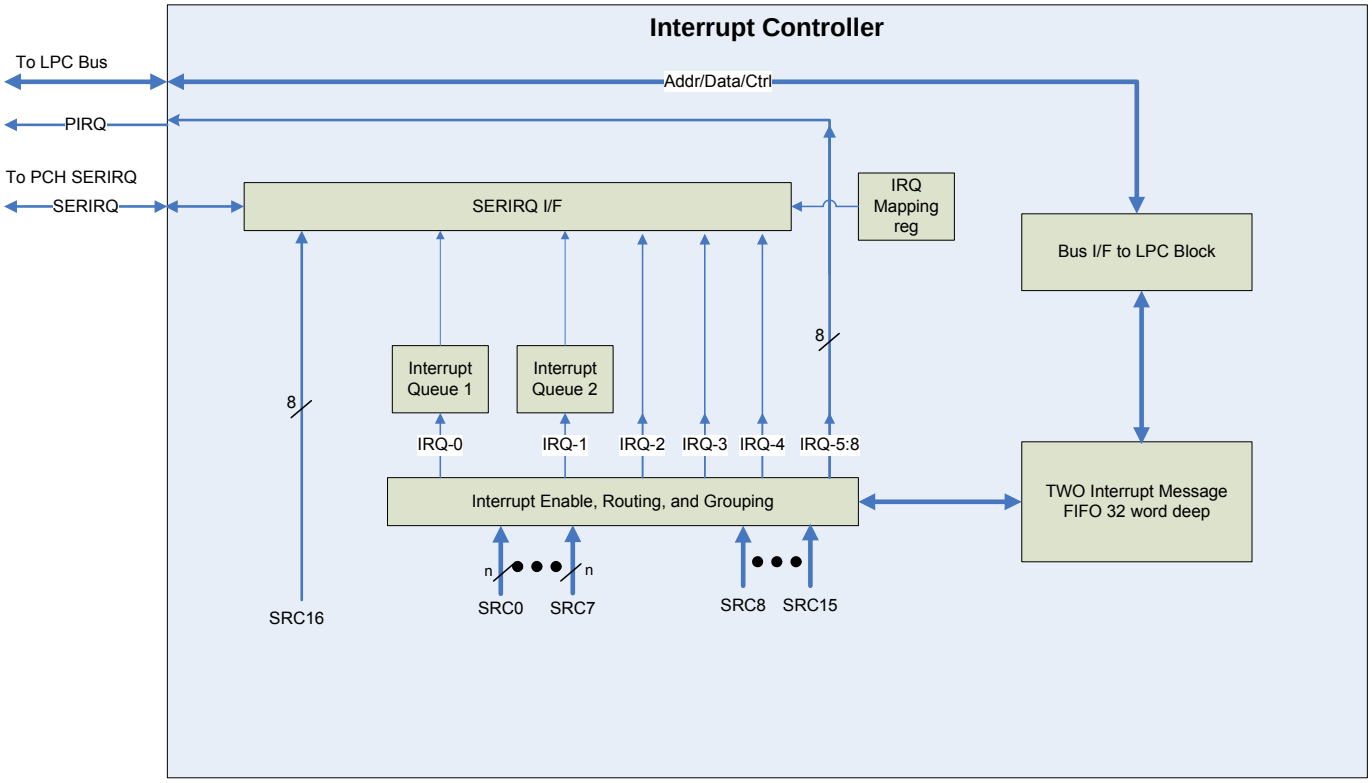
INTERRUPT CONTROLLER

The interrupt control module provides the required control and monitoring function to consolidate and route the external and internal interrupts sources, and drives the interrupt input to the processors through the serial IRQ protocol, as well as four discrete IRQ outputs (IRQ5-8).

The interrupt controller is comprised of four logical blocks. The first block provides source routing, grouping, status, and enable/disable, and masking provisions for each interrupt source. The second block implements SERIRQ protocol. The interrupts from the controller can be dispatched to the processor using this block. A third block provides LPC bus module access I/F. This interface is used by the processor to access registers residing in the interrupt controller. The fourth block implements a messaging interface to communicate interrupt events to the processor. Figure 1.12 provides a top-level interrupt controller block diagram.

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Figure 1.12: CHAMP-AV8 Interrupt Controller Block Diagram



All interrupt source lines are aggregated into the 17 different interrupt source groups SRC0- 16. SRC0-15 inputs go through the routing control logic and get combined/routed to any of the 13 internal IRQ lines. Interrupt input SRC16 is a special 8 bit wide input port in that it bypasses the routing logic and is connected directly to the serialIRQ frame generator. SRC16 is provided so that 16550 UART interrupts can be handled in a way that's compatible with legacy drivers.

The internal IRQ signals fall into three different categories: IRQ0-1 are routed to the serial IRQ port and they have message FIFOs (discussed below). IRQ2-4 are routed to serial IRQ but have no message FIFOs. IRQ5-8 bypass the serial IRQ and are routed to four discrete output ports.

The first IRQ group (IRQ0-1) has a pair of message FIFOs. Upon detection of an interrupt event, FPGA hardware pushes a message into the message FIFO and clears the status register. The SERIRQ protocol is used to communicate the pending interrupt to the processor. Upon notification, the processor reads the message FIFO to determine the interrupt source and does not have to clear the status register. This interrupt mechanism minimizes the latency incurred for interrupt processing.

The second IRQ group (IRQ2-4) is routed to the CPU using the SERIRQ protocol. These IRQs do not have a message FIFO. The CPU must read the interrupt source register from the FPGA and must clear the status.

The third group (IRQ5-8) is routed directly to PIRQx inputs of the PCH. Upon notification, the CPU uses the PCI interrupt servicing method.

Interrupt Source Grouping

The interrupt sources are grouped into 17 input busses. The first eight groups (SRC0-7) are vectors of up to 32 interrupts each. The number of interrupts by group is defined by parameters. The eight groups SRC8-15 are scalars and are composed of only one interrupt each. Group SRC16 is a vector of up to eight interrupt inputs.

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The incoming interrupts consist of two different types:

- Unlatched Interrupts - Status is visible in "Read-Only" interrupt status registers. These interrupts are cleared at the source function.
- Latched Interrupts - Status is visible in and also cleared with "Read / Write-Clear" registers. These registers are required to store the occurrence of transient events, such as timer roll-overs and watchdog exceptions.

The table below summarizes how the interrupt sources are assigned to groups.

Table 1.3: Interrupt Input Connections

Interrupt	Input Latch	Group
General Purpose timers (lower 2 of each node) [4] Watchdog timers [4] MBSC [1] General Purpose timers (local node) [4]	Latched	SRC0 SRC1
I2O Interrupts (Doorbell, post q wr, overflow) [6] 1 PPS signal	Latched	SRC2
Discrete I/O [10]	Unlatched	SRC3
SPI interface [1] I2C interfaces [2] SMBus ALERT signals [2] PROCHOT [2]	Unlatched	SRC4 SRC5
SHMUART [12] SRIO Multi-cast Interrupt [1] SRIO Switch Interrupt [1] PCIe Switch Interrupt [1]	Unlatched	SRC6 SRC7
UNUSED	Unlatched	SRC8
UNUSED	Unlatched	SRC9
UNUSED	Unlatched	SRC10
UNUSED	Unlatched	SRC11
UNUSED	Unlatched	SRC12
UNUSED	Unlatched	SRC13
UNUSED	Unlatched	SRC14
UNUSED	Unlatched	SRC15
UART_0	Unlatched	SRC16[0]
UART_1	Unlatched	SRC16[1]
UART_2	Unlatched	SRC16[2]
UART_3 (UNUSED)	Unlatched	SRC16[3]
UNUSED	Unlatched	SRC16[4]
UNUSED	Unlatched	SRC16[5]
UNUSED	Unlatched	SRC16[6]
UNUSED	Unlatched	SRC16[7]

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Interrupt Routing

Each interrupt line within a source group is routed to a status register, but first passes through test assertion and enabling logic. If latching is enabled for that bit, the status register latches the edge of the interrupt pulse and holds the condition until cleared by a write to the status register. If latching is not enabled, the status register is read-only and not writable. In addition the test register can be used to force any of the interrupt bits, allowing software to emulate the assertion of any of the interrupt sources. The enable register bit, if 1, allows the interrupt to pass through, or else it is blocked.

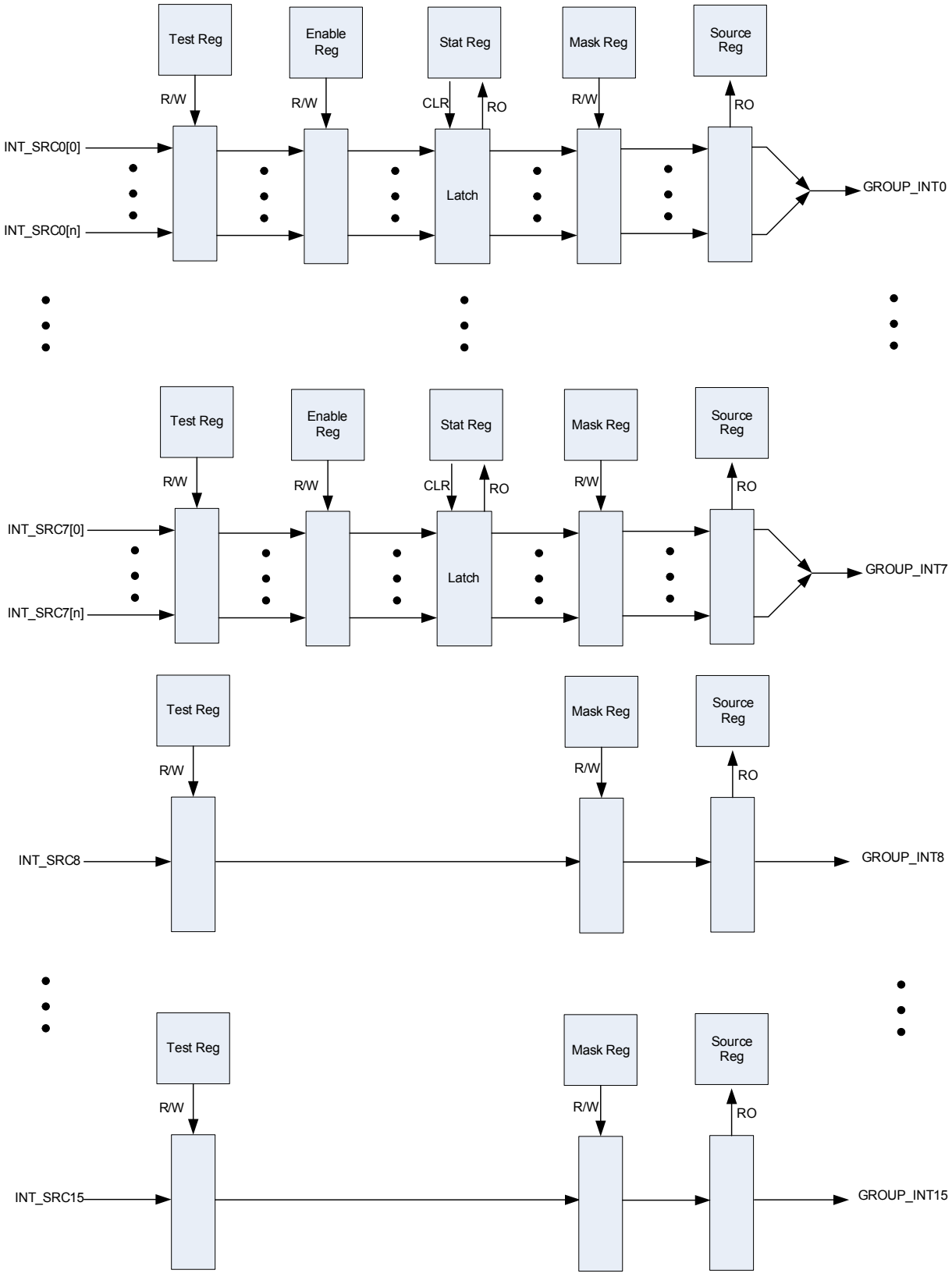
After the status register, each bit within a source group passes through a mask register that acts like the enable register. If the mask bit is 1, it allows the interrupt through, or else it is blocked.

Each interrupt line in the source group is then tied to the source register bits that indicate the state of the interrupt line at this stage of the routing. See Figure 1.10, "Interrupt Routing Block (Part A)," on page 1-22 for an illustration of this.

After passing through the source register, all of the bits (up to 32) in the source group are combined into a single line, such that if any of the bits are asserted, then the single output line is also asserted. This output line is referred to as GROUP_INTx in Figure 1.13, “Interrupt Routing Block (Part A),” on page 1-28.

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Figure 1.13: Interrupt Routing Block (Part A)



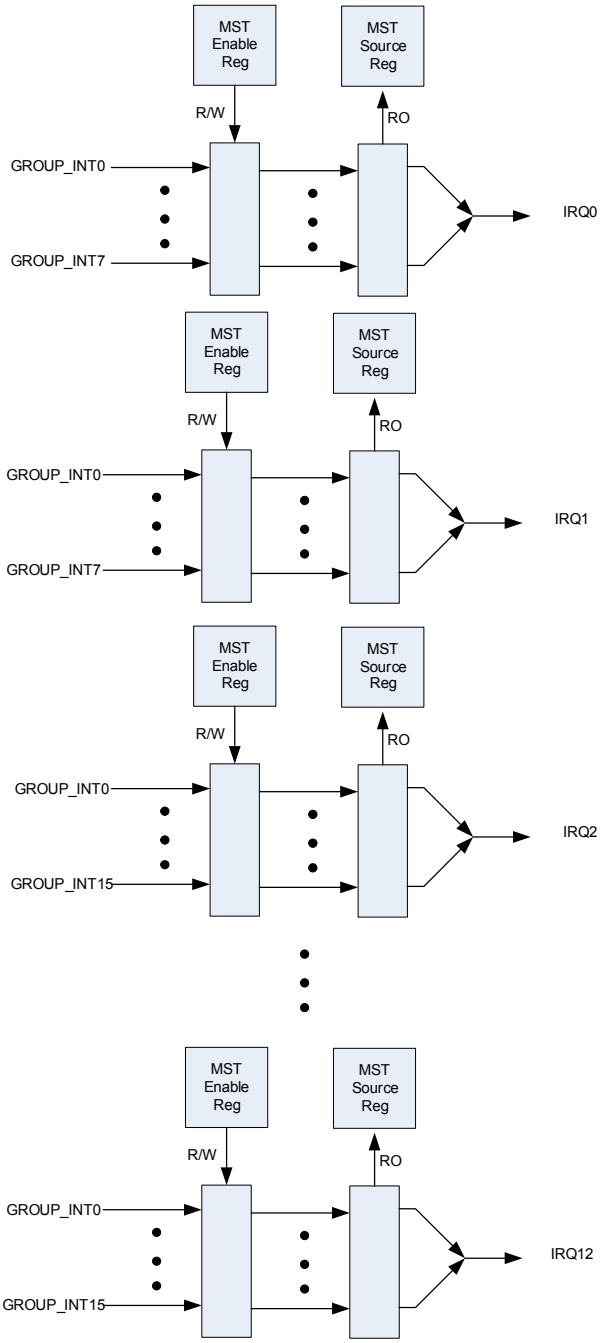
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Figure 1.14 below shows how each GROUP_INTx line feeds to each of the 13 IRQ outputs. Each of the 16 GROUP_INTx lines can be individually enabled to feed into a particular IRQ via a MST Enable Register. After the enable register, each bit status is sampled and fed to a MST Status Register. After this stage, all enabled GROUP_INTx bits are combined into the single IRQx output, such that if any enabled GROUP_INTx bit is asserted, the IRQx line is also asserted.

Note

IRQ0 and IRQ1 can only have the vector input groups SRC7-0 assigned to them. The scalar groups SRC15-8 cannot be assigned to these IRQs.

Figure 1.14: Interrupt Routing Block (Part B)



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Interrupt Messaging FIFO

Each enabled interrupt event for IRQ0-1 will generate a message vector which will be stored in the interrupt message FIFO. There is a separate FIFO for each IRQ. Only edge-mode interrupts are supported, and software must ensure that only edge-mode interrupts are routed to these IRQs. Anytime an enabled interrupt occurs, it will send a single message into the message FIFO. The message indicates that "interrupt X has occurred". The CPU will be able to read the message to determine which interrupt occurred, which is much faster than having to read multiple interrupt status registers.

Serial IRQ Interface

Of the thirteen IRQ outputs from the routing/control block, IRQ0-4 will be sent to the PCH using a serial IRQ scheme. In addition, SRC16 (8 bits wide) are also sent to PCH over the serial IRQ. This allows a single signal to be used to report interrupt requests to the CPU. The signal used to transmit this information is shared between the PCH and all peripherals that support serial interrupts. The signal line, SERIRQ, is synchronous to the PCI clock, and follows the sustained tri-state protocol that is used by all PCI signals.

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SPECIFICATIONS

The CHAMP-AV8 board meets the specifications outlined in the following sections.

VPX COMPLIANCE

ANSI/VITA 46.0-2007, VITA 46.3, ANSI/VITA 46.9-2010, ANSI/VITA 65-2010.

Table 1.4: VPX Compliance Summary

Mode	Profile Supported
Module profile (pinout)	MOD6-PAY-4F1Q2U2T-12.2.1-11/12
Slot profile	SLT6-PAY-4F1Q2U2T-12.2.1
XMC signal routing to backplane	XMC J16: P5w3P6-X38s+X8d+X12d XMC J14: P3w1-P64s (routed as differential pairs)

Table 1.5: XMC Compatibility Identification Block

Standard XMC.3					
P15			P16		
PCIe			I/O		
Standard			N/A		
8 Lane	Link 0	2.5Gb/s	N/A	N/A	N/A



Note

See ANSI/VITA 42.3-2006, Section 6.0 and Table 6-1, for a definition of the XMC Compatibility Identification Block.

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POWER REQUIREMENTS

Table 1.6: Power Requirements

Power Supply Requirements (per ANSI/VITA 46.0-2007)	Mnemonic	Description	Nominal Value	Tolerance
	Vs1/Vs2	+12.0VDC	12.0V	± 5%
	+3.3V_AUX	+3.3VDC	3.3V	± 5%
	+12V_AUX(see Note 2)	+12VDC	+12.0V	± 5%
	-12V_AUX(see Note 2)	-12VDC	-12.0V	± 5%
	VBAT(see Note 4)	Battery Backup	+3.0V	+2.7V (min) +3.5V (max)

Notes: 1. Power consumption (Watts) will vary depending on processor frequency, application usage, and ambient temperature.
2. ±12VAux for XMC only (not used by CHAMP-AV8 basecard).
3. Vs3 (+5.0 VDC) is not used by the CHAMP-AV8.
4. VBAT is optional. VBAT sources current only when the board is shutdown or main power is "off". When the CPU is running, VBAT current is 0 Amps.

Power Supply Requirements

- Base-board +12V P/S requirement (no XMC), typical current draw is less than 12A.
- Base-board AUX +3.3V P/S requirement, typical current draw is less than 0.3A.

Overall Thermal Power Dissipation

- Thermal power dissipation (no XMC), typical dissipation is less than 135W.



Cross Reference

See "Detailed Power Requirements" on page 2-3 for additional information.

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DIMENSIONS

Table 1.7 lists the physical dimensions of the CHAMP-AV8.

Table 1.7: CHAMP-AV8 Dimensions

Parameter	Dimensions
Height	233.2 mm (9.181 in.)
Depth	159.8 mm (6.293 in.)

Notes: 1. Front panel hardware on air-cooled modules includes: injector/extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).
2. Uses a full width thermal interface surface to maximize thermal performance which is a small deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in a standard air-cooled chassis.

WEIGHT

Table 1.8 lists the weight of the CHAMP-AV8.

Table 1.8: CHAMP-AV8 Weight

Card Type	Mass
Air-cooled CHAMP-AV8 Level 0	1.05kg
Air-cooled CHAMP-AV8 Level 100	1.15kg
Conduction-cooled CHAMP-AV8 Level 200	1.25kg



Note

Tolerance for the above numbers are +/- 0.05kg.

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RUGGEDIZATION LEVELS

Listed below are the Curtiss-Wright ruggedization levels available for the CHAMP-AV8.

Table 1.9: VPX6-462-A Air-Cooled Ruggedization Levels

	Level 0	Level 100
Operating Inlet Air Temperature[4]	0 °C to 50 °C	-40 °C to 71 °C
Non-Oper. Temperature (Storage)	-40 °C to 85 °C	-55 °C to 125 °C
Operating Humidity	0 to 95% non-condensing	0 to 100% non-condensing
Non-Oper. Humidity (Storage)	0 to 95% non-condensing	0 to 100% condensing
Vibration Sine[1]	2 g peak, 15-2k Hz	10 g peak, 15-2k Hz
Vibration Random[2]	0.01 g^2/Hz, 15-2k Hz	0.04 g^2/Hz, 15-2k Hz
Shock[3]	20 g peak	30 g peak
Conformal Coat[5]	No	Yes

Notes:
1. Sine vibration based on sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15 to 44 Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Air flow requirements are 20 CFM for L0 and 24 CFM for L100. Consult factory for further details. Ruggedization is qualified with air flowing in the direction of P6 to P0.
5. Conformal coating type is manufacturing site specific. Consult factory for details.
6. The operation of the card may require derating at higher temperatures. Consult the factory for details.

Table 1.10: VPX6-462-C Conduction-Cooled Ruggedization Levels

	Level 100	Level 200
Operating Card Edge Temperature[4]	-40 °C to 71 °C	-40 °C to 85 °C
Non-Oper. Temperature (Storage)	-55 °C to 125 °C	-55 °C to 125 °C
Operating Humidity	0 to 100% non-condensing	0 to 100% non-condensing
Non-Oper. Humidity (Storage)	0 to 100% condensing	0 to 100% condensing
Vibration Sine[1]	10 g peak, 15-2k Hz	10 g peak, 15-2k Hz
Vibration Random[2]	0.1 g^2/Hz, 15-2k Hz	0.1 g^2/Hz, 15-2k Hz
Shock[3]	40 g peak	40 g peak
Conformal Coat[5]	Yes	Yes

Notes:
1. Sine vibration based on sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15 to 44 Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Temperature measured at card edge.
5. Conformal coating type is manufacturing site specific. Consult factory for details.
6. The operation of the card may require derating at higher temperatures. Consult the factory for details.

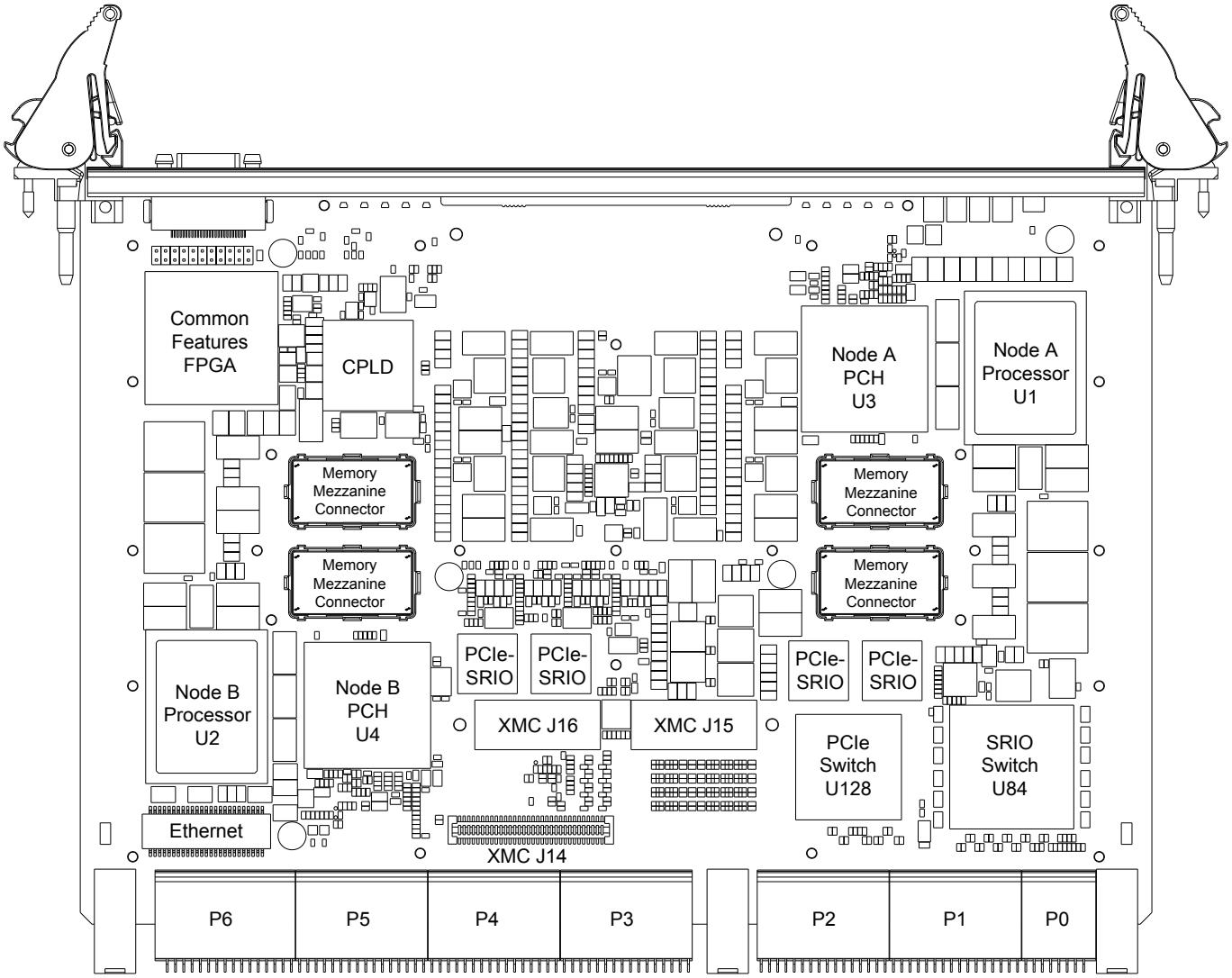
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PHYSICAL CHARACTERISTICS

Figure 1.15 shows the location of the major components and the mating connectors on the top side of the CHAMP-AV8 (some hardware has been removed from this drawing to make all of the components visible).

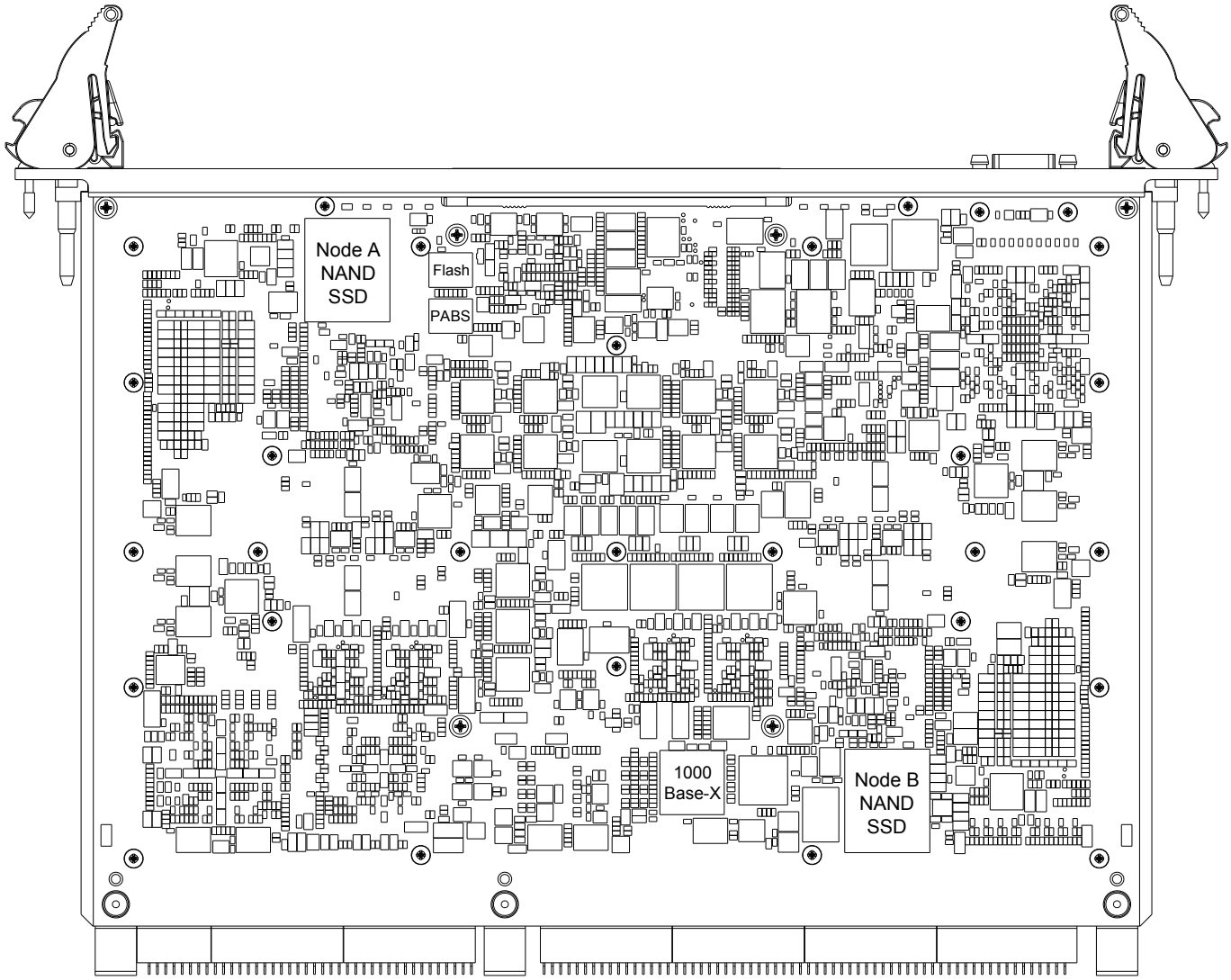
All ruggedization levels of the CHAMP-AV8 board have a thermal shunt that covers some of the components.

Figure 1.15: CHAMP-AV8 Board Layout—Primary Side)



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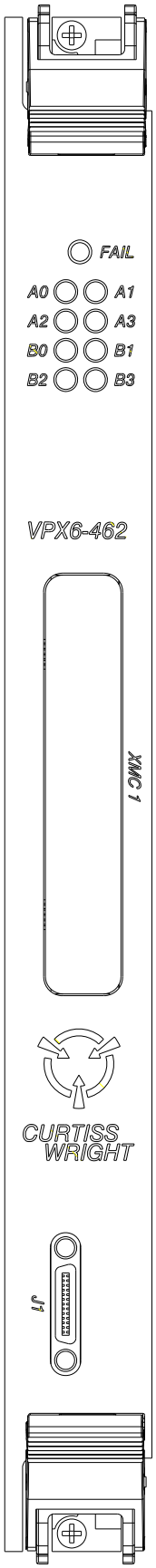
Figure 1.16: CHAMP-AV8 Board Layout—Secondary Side



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VPX6-462-A Front Panel

An illustration showing the front panel that is mounted on the air-cooled version of the CHAMP-AV8 (also known as the VPX6-462-A) is provided below, along with a brief description of the indicators and connectors it provides.



Red FAIL LED: A red LED on the front panel is used to indicate a failure determined by the on-board diagnostic firmware.

Processor Status LEDs A0, A1, A2, A3, B0, B1, B2, B3: Each of the processors has a processor LED register that controls the green processor status LEDs seen opposite and two of the surface mount status LEDs on the PWB.

XMC Slot: An opening is provided on the VPX6-462-A front panel to provide access to connectors that may be incorporated on an optional XMC module that may be installed on the basecard PWB. If there is no XMC module mounted, the opening is filled with a bezel.

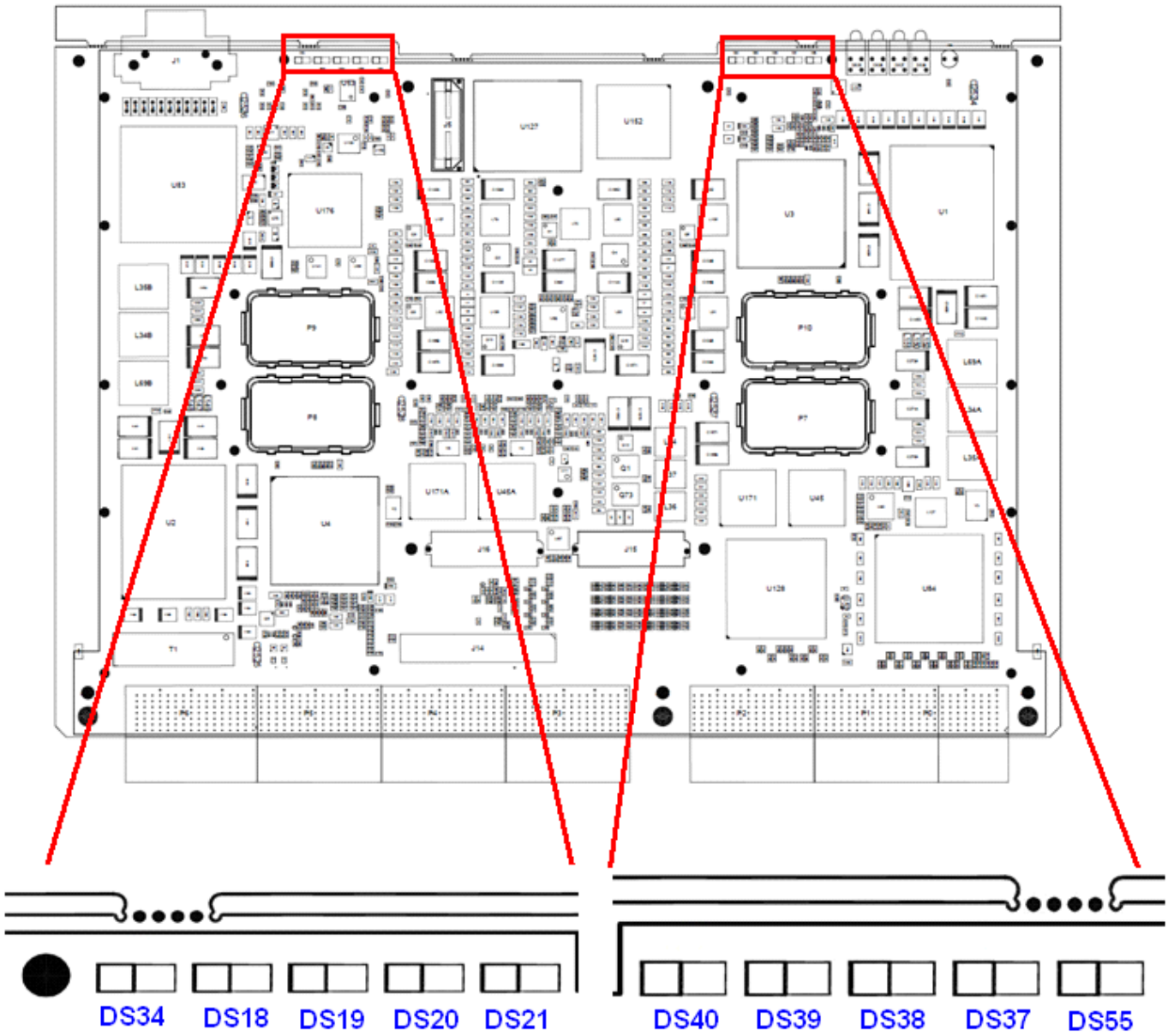
J1 Connector: The J1 connector provides one EIA-232 serial interface and one GigE interface (subject to build-time option) to each processor node. J1 also provides one USB connection to the node A processor and supports a reset signal which when asserted resets the entire card.

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LOCATION OF STATUS LEDS ON CONDUCTION-COOLED VARIANT

For conduction-cooled variants, the Processor Status LEDS, the Fail LED and the Thermal Failure LED, are all mounted on the top-side of the board assembly, as shown in Figure 1.17 below. A description of LED behaviour can be found in Table 3.7, "Summary of LED Behavior," on page 3-15.

Figure 1.17: Status LEDS on Conduction-Cooled Variants



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MATING CONNECTORS

Table 1.11 summarizes these connectors, providing a brief description and an indication of what functions/interfaces are supported by each.

Table 1.11: Summary of CHAMP-AV8 Connectors, Functions Supported

Connector Designation	Description	Supported I/O Configurations
J1	26-pin front panel connector (VPX6-462-A version CHAMP-AV8 only)	The J1 connector provides two serial interfaces, one to each processor node, designated A0 and B0. The J1 connector also provides two GigE interfaces, one to each processor node, designated Ethernet A and Ethernet B. The connector also provides one USB port (USB_A1) to the node A processor and supports a reset signal which when asserted resets the entire card.
J14, J15, J16	Connectors for PMC I/O on XMC module site, compliant with IEEE P1386 and XMC module site.	The J14 connector used for interconnection with PMC user I/O signals on an optional XMC module. All 64 PMC user I/O signals are accessible via the base board P3 connector. The J15 connector is the primary XMC connector as defined in VITA 42.0 and the J16 connector is mapped to XMC I/O and mapped to the base board P5 and P6 connectors.
P0	VITA 46 P0 Utility Connector	Provides power and ground connectors to the chassis backplane as well as Geographical Addressing, Differential reference clock, system reset, JTAG and Aux Clk signals.
P1	VITA 46 P1 SRIO Fabric Connector	High Speed Serial RapidIO interconnect as well as various VITA 46 and AV8 reserved and system signals: SYSCON_L, CARD_FAIL_L, CF_ALT_BOOT_L, PB_RESET_L CARD_FAIL_L, PB_RESET_L, GDiscrete1
P2	VITA 46 P2 PCIe Expansion Connector	Provides two PCIe interfaces on the expansion plane and includes support for one eight-lane port and an optional 4-lane/8-lane PCIe port (build-time option).
P3	VITA 46 P3 XMC Site's PMC User I/O Connector	Provides up to 64 bits of PMC user I/O from the XMC P14 connector to the backplane. The 64 bits are routed as 32 differential pairs.
P4	VITA 46 P4 Basecard I/O Connector	Provides access to the JTAG Selection, PMBus, backplane jumper signals, RS-232/422 serial channels and Ethernet 1000Base-BX and 1000Base-T ports.
P5	VITA 46 P5 XMC User I/O Connector	Provides 38 bits of single ended XMC I/O and 8 pairs of high-speed differential XMC I/O. I/O is routed from the XMC site's J16 connector.
P6	VITA 46 P6 XMC/DIO/SATA/USB Connector	Provides 12 pairs of high-speed differential XMC I/O that is routed from the XMC site's J16 connector; 16-bits of DIO.



Cross Reference

For complete descriptions of all the basecard mating connectors, including detailed pinout listings and electrical characteristics of signals, refer to Appendix A of this manual.

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OVERVIEW OF AVAILABLE SOFTWARE

The following sections outline the various software components associated with the CHAMP-AV8:

BUILT IN TEST (BIT) FIRMWARE

The CHAMP-AV8 hosts a BIOS package that performs both board initialization as well as Power-up Built-In Test (PBIT). PBIT consists of a set of essential tests that provide confidence that the hardware is operating correctly, as well as test sequencing which is stored in flash memory and is tailorable.

Additional diagnostic capabilities are exercisable from the BSP, such as Initiated BIT (IBIT). Like PBIT, the IBIT capability is tailorable, but in addition these tests can be invoked at any time. When invoked in an offline, i.e. maintenance mode, these tests can provide robust testing, such as duration and stress testing that would not be appropriate for most operational modes.



Cross Reference

For more information see the "PBIT Diagnostic Tool" section of the CHAMPtools Software User's Manual, as well as the CHAMPtools IBIT/CBIT User's Manual.

OPERATING SYSTEM SOFTWARE

The CHAMP-AV8 is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported on the CHAMP-AV8.

- VxWorks 6.x, Workbench 3.x from Wind River. (Part number DSW-462-000-VXW)
- Fedora Linux Software Development Kit from Curtiss-Wright (part number DSW-462-001-LNX)

CONTINUUM IPC™ LIBRARY

The Continuum Inter-Processor Communications (IPC) Library (available for the VxWorks OS platform only) is a library of functions designed to enable high performance, low-latency message passing. Continuum IPC allows processors to communicate task-to-task, on the same card over local interconnect, or between boards over a system level interconnect. Continuum IPC supports several transport mechanisms including Serial RapidIO® (SRIO). Applications developed on CHAMP-AV6 or SVME/DMV-183/184/185 will port to the CHAMP-AV8 with no changes related to the Continuum IPC layer. Continuum IPC provides low-overhead block data transfers, segmented block data transfers and signaling between processors to assist in high-bandwidth data movement. See the Continuum IPC Library data sheet for more details.

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CONTINUUM VECTOR™ LIBRARY

The CHAMP-AV8 derives its floating-point performance from the Intel AVX vector processing unit. Available for both Linux and VxWorks OS platforms, the Continuum Vector Library provides over 200 functions optimized for the SSE unit, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for the Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector data sheet for detailed information.

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2 PRE-INSTALLATION TASKS

IN THIS CHAPTER

This chapter discusses the following topics:

- "Unpacking the Card" on page 2-2
- "Checking Hardware Requirements" on page 2-2
  - "Chassis Requirements" on page 2-2
  - "Backplane Requirements" on page 2-2
  - "Detailed Power Requirements" on page 2-3
  - "BIOS Configuration Parameters" on page 2-4
  - "XMC Module Installation Requirements" on page 2-4
  - "XMC Site" on page 2-4
  - "Cable Requirements" on page 2-6
- "Configuring Jumpers" on page 2-7
  - "Configuration Jumper Locations" on page 2-8

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UNPACKING THE CARD



Warning

To avoid personal injury or damage to this Circuit Card Assembly, disconnect the chassis from its power source before removing or installing any cards.

This Circuit Card Assembly uses components that are sensitive to electrostatic discharges. It must be kept sealed in its conductive package until just before you install it. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card. Static discharges can damage integrated circuits.

To unpack the card from its protective package, follow these steps:

1. Unpack the Circuit Card Assembly from the shipping carton in a suitable work area. If the shipping carton appears to be damaged, request that an agent of the shipper or carrier be present during unpacking and inspection.
2. Find the packing list. Make sure all the items on the list are present.
3. Save the packing material for storing or reshipping the card.
4. If your CHAMP-AV8 was shipped with an XMC module installed, make sure it is firmly attached to the basecard.

CHECKING HARDWARE REQUIREMENTS

Make sure the various hardware requirements summarized beginning on page 2-2 have been met before you install the CHAMP-AV8.

CHASSIS REQUIREMENTS

The air-cooled (VPX6-462-A) Level 000 and Level 100 CHAMP-AV8 cards are designed to be installed in an air-cooled chassis.

Conduction-cooled Level 100 and Level 200 (VPX6-462-C) CHAMP-AV8 cards are designed to be installed in a conduction-cooled chassis.



Cross Reference

Refer to the Ruggedization Capabilities described on http://www.cwcdefense.com/ for more information.

BACKPLANE REQUIREMENTS

The CHAMP-AV8 boards are designed to be used with the VITA 65 backplanes with the following Slot and Module profiles:

- Slot Profile: SLT6-PAY-4F1Q2U2T-12.2.1
- Module Profile: MOD6-PAY-4F1Q2U2T-12.2.1-11/12

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DETAILED POWER REQUIREMENTS

The CHAMP-AV8 requires +12 V and +3.3 V power supplies in order to operate. Table 2.1 shows the voltage and current requirements for the CHAMP-AV8.

Table 2.1: Voltage and Current Requirements

Power Supply Requirements (per ANSI/VITA 46.0–2007)	Mnemonic	Description	Nominal Value	Tolerance
	VS1, VS2	+12.0 VDC	12.0 V	±5%
	3.3V_AUX	+3.3 VDC	3.3 V	±5%
	+12V_AUX (see Note 1)	+12 VDC	+12.0 V	±5%
	-12V_AUX (see Note 1)	-12 V	-12.0 V	±5%
	VBAT (see Note 2)	Battery Backup	+3V	+2.7V (min) +3.5V (max)

Notes: 1. The ± 12V_AUX supplies are not used by the CHAMP-AV8 baseboard circuitry. However, they are routed to the XMC site on the board. Therefore the current drawn from these supplies is XMC module-dependent.
2. VBAT is optional. VBAT sources current only when board is shutdown or main power is “off”. When CPU is running, VBAT current is 0 Amps.

For proper operation of the CHAMP-AV8, the board must be installed in a VPX chassis that meets the requirements of the following standards:

- VITA 46 Base Specification, ANSI/VITA 46.0-2007, 2007
- OpenVPX System Specification, ANSI/VITA 65-2010, 2010

The backplane voltages must meet all of the requirements specified in these documents. Missing or below-level voltages will cause the power detection circuitry on the board to hold the board in a powered down state. The power detection circuitry does not monitor the 12VAux supplies since these power rails are used only to provide ±12V to the XMC site (no on-board circuitry uses these voltages). When missing or below level backplane voltage other than ±12V causes the board to be is held in a powered down state, ±12V is not gated to the XMC site, thereby also powering down the XMC.

In order to ensure proper operation of the CHAMP-AV8 board, the remote voltage sense lines for the 12V and 3.3V power must be connected from the power supplies to the voltage rails on the backplane. Chassis units (with built-in power supplies) furnished by most vendors should already have these lines connected. However, if the chassis is powered from a user-supplied power source, these lines must be connected. Consult the power supply user manual if you have questions concerning the proper connection of these lines.



Caution

12 V and 3.3 V power must be supplied to the board through the VPX backplane.

The VPX chassis power supplies must be properly sized for the system and must utilize remote backplane sensing to properly regulate the backplane voltages.

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Power Supply Requirements

Baseboard 12 V power supply requirement for each CHAMP-AV8 is minimum 12 A. Baseboard 3.3 V power supply requirement for each CHAMP-AV8 is minimum 0.5 A.

Overall Thermal Power Dissipation

Thermal power dissipation, typical application is 100 W. Thermal power dissipation, maximum is 130 W.



Note

These numbers do not include XMC power usage, which may be differently distributed than the baseboard power, but should be added to it if an XMC is used.

BIOS CONFIGURATION PARAMETERS

The on-board BIOS contains configuration parameters that are used to configure certain features of the board. These parameters are explained in the BIOS User's Manual. For initial power-up of the board, there should be no need to modify these parameters. Each processor node has a separate BIOS and BIOS configuration. BIOS configuration changes intended for both processor nodes must be performed twice (once per node).

XMC MODULE INSTALLATION REQUIREMENTS

The CHAMP-AV8 provides one XMC only site. This site is located on the on the top of the card and is supported by connectors J14, J15 and J16.

See Figure 1.6, "Core Functions FPGA Block Diagram," on page 1-12 for an illustration of the CHAMP-AV8 board layout.

The XMC site is designed to conform to the following specifications:



Warning

Please note that the CHAMP-AV8 does not provide a keying pin due to board real estate restrictions.

Installing an XMC with incompatible signaling levels can cause permanent damage to the CHAMP-AV8 baseboard as well as the XMC.

Review your XMC module's power requirements carefully to ensure that you do not install an incorrect XMC in the CHAMP-AV8 XMC site.

XMC I/O

The CHAMP-AV8 supports backplane user I/O through the VPX connectors (see "CHAMP-AV8 I/O Mapping" on page A-8 for details).

XMC SITE

The VITA 42 standard and subsidiary specifications define the XMC mezzanine module format which adds high-speed data interfaces and I/O capability to the PMC standard. Together these improvements allow for the next generation of mezzanine modules with improved throughput to the host processor and dramatically increased I/O bandwidth.

The CHAMP-AV8 is equipped with one XMC mezzanine site that is available as a build option and connected to the base board PCIe switch. This site supports either a 4-lane Gen1 PCIe interface that is capable of 1 Gbyte/s or an 8-lane (x8) Gen1 PCIe interface capable of 2 Gbyte/s simultaneously in both transmit and receive directions.

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The XMC site provides traditional PMC I/O, single ended XMC I/O, and high-speed differential XMC I/O. The traditional PMC I/O consists of 64 bits of I/O that are differentially routed between the XMC J14 connector and the CHAMP-AV8 backplane P3 connector.

The CHAMP-AV8 utilizes a 10 mm XMC stacking height.

Mezzanine Module Power Considerations

The CHAMP-AV8 supplies voltages to the XMC site according to VITA 42. The supplied voltages are listed in Table 2.2, along with their maximum supply currents. These maximum supply currents are specified by VITA 42 at 1 Ampere per XMC connector pin. The CHAMP-AV8 is capable of providing these currents.

Performance of the CHAMP-AV8 may be impacted by a specific XMC card installed on the XMC site. Heat dissipated by the XMC will raise the temperature of CHAMP-AV8 basecard components. At elevated inlet air or card edge temperature, the CHAMP-AV8's microprocessors may throttle, reducing performance. Although the CHAMP-AV8 supports high wattage XMC cards and is designed to supply maximum current according to the VITA 42 standard, the thermal impact on the basecard should be assessed.

Caution

When installing an XMC on the CHAMP-AV8, careful characterization of the XMC performance should be done. Technical Support may also be consulted. Depending on the particular application and configuration, various conditions can occur that could adversely affect (and possibly extend oustide of the product specification) the baseboard, XMC, or chassis. These conditions include, but are not limited to excessive heating of baseboard and XMC components. Factors affecting this include, but are not limited to: maximum operating temperature of the board (air temperature for air-cooled boards and card edge temperature for conduction-cooled boards), airflow (air-cooled boards), baseboard power dissipation (application specific), and the location and density of the hot components on the XMC and/or the baseboard.

Depending upon application usage, the CHAMP-AV8 may require operational derating when used in conjunction with a mezzanine. Consult the factory for guidance.

Table 2.2: Maximum Supply Current for XMC Site

Supply	Maximum Supply Current
12 VPWR	8A
3.3V_AUX	1A
3.3V	4A
+12V	1A
-12V	1A

Note

The use of a mezzanine may induce lowered CPU performance at elevated temperatures. Consult the factory for guidance.

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CABLE REQUIREMENTS

A Front Panel interface cable is available to support the CHAMP-AV8. This cable is identified as:

- CBL-462-FPL-000 (CHAMP-AV8 Standard Front Panel Cable Assembly - see Figure 2.1)

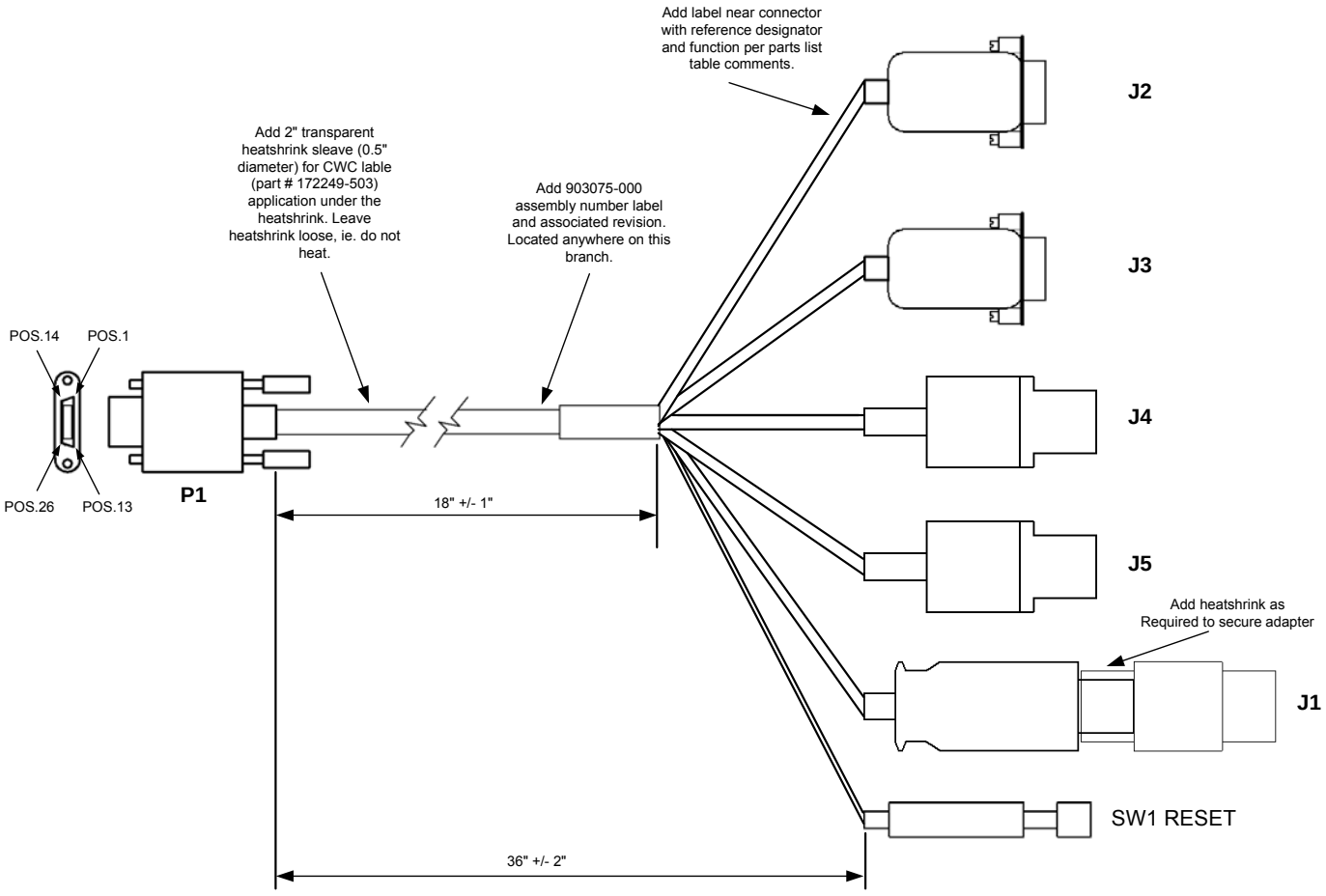
CBL-462-FPL-000 (903075-000)

Figure 2.1 shows a cable drawing of the CHAMP-AV8 Standard Front Panel Cable Assembly (CBL-462-FPL-000). The cable assembly provides access to the following CHAMP-AV8 signals: USB A (J1); RS-232 Port A0 (J2); RS-232 Port B0 (J3); Ethernet Port 0 (J4); Ethernet Port 1 (J5); Reset Switch (SW1).

Caution

The CHAMP-AV8 front panel cable is different than that used on the CHAMP-AV6, even though the physical front panel connector is the same. To use the CHAMP-AV8 front panel, the user must employ CBL-462-FPL-000.

Figure 2.1: CBL-462-FPL-000 (CHAMP-AV8 Standard Front Panel Cable Assembly)



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CONFIGURING JUMPERS

Table 2.3 defines the jumpers (JB1 - JB11) on the CHAMP-AV8 that reside at the front of the board near the LEDs (see Figure 2.2 on page 2-8). Jumpers are available for selecting various board operational modes. Jumpers identified as Reserved must be left in the default setting and only changed under the direction of Customer Support.



Warning

Please make sure that the board is not powered on when configuring board jumpers and that you observe proper static control procedures when handling the card.

Table 2.3: Jumper Block Definition

Jumper	On	Off	Default
JB1	Write protect NAND flash	Enable writing to NAND flash	Off
JB2	SOFT_JUMP0 = 0 (registered and software defined jumper)	SOFT_JUMP0 = 1 (registered and software defined jumper)	Off
JB3	SOFT_JUMP1 = 0 (registered and software defined jumper)	SOFT_JUMP1 = 1 (registered and software defined jumper)	Off
JB4	Enable writing to PROMs (SPD, GigE, PCIe)	Write protect PROMs (SPD, GigE, PCIe)	Off
JB5	Enable writing to PABS Flash	Write protect PABS Flash	Off
JB6	Write protect NVRAM	Enable writing to NVRAM	Off
JB7	Write protect Primary Flash	Enable writing to Primary Flash	Off
JB8	Boot from PABS site	Boot from Primary Flash	Off
JB9	Watchdog disable	Watchdog enable	Off
JB10	USB disable	USB enable	Off
JB11	Prevents CHAMP-AV8 from asserting System Reset during power-on reset. If the CHAMP-AV8 is declared the System Controller (SYSCON), this setting will have no effect - the CHAMP-AV8 will still be able to assert System Reset (as required by VITA 46.0).	Allows the CHAMP-AV8 to assert System Reset during power-on reset, as permitted by ANSI/VITA 46.0, Permission 4-11.	Off

Note: See the CHAMP-AV8 BIOS User's Manual for additional information describing the various boot modes.

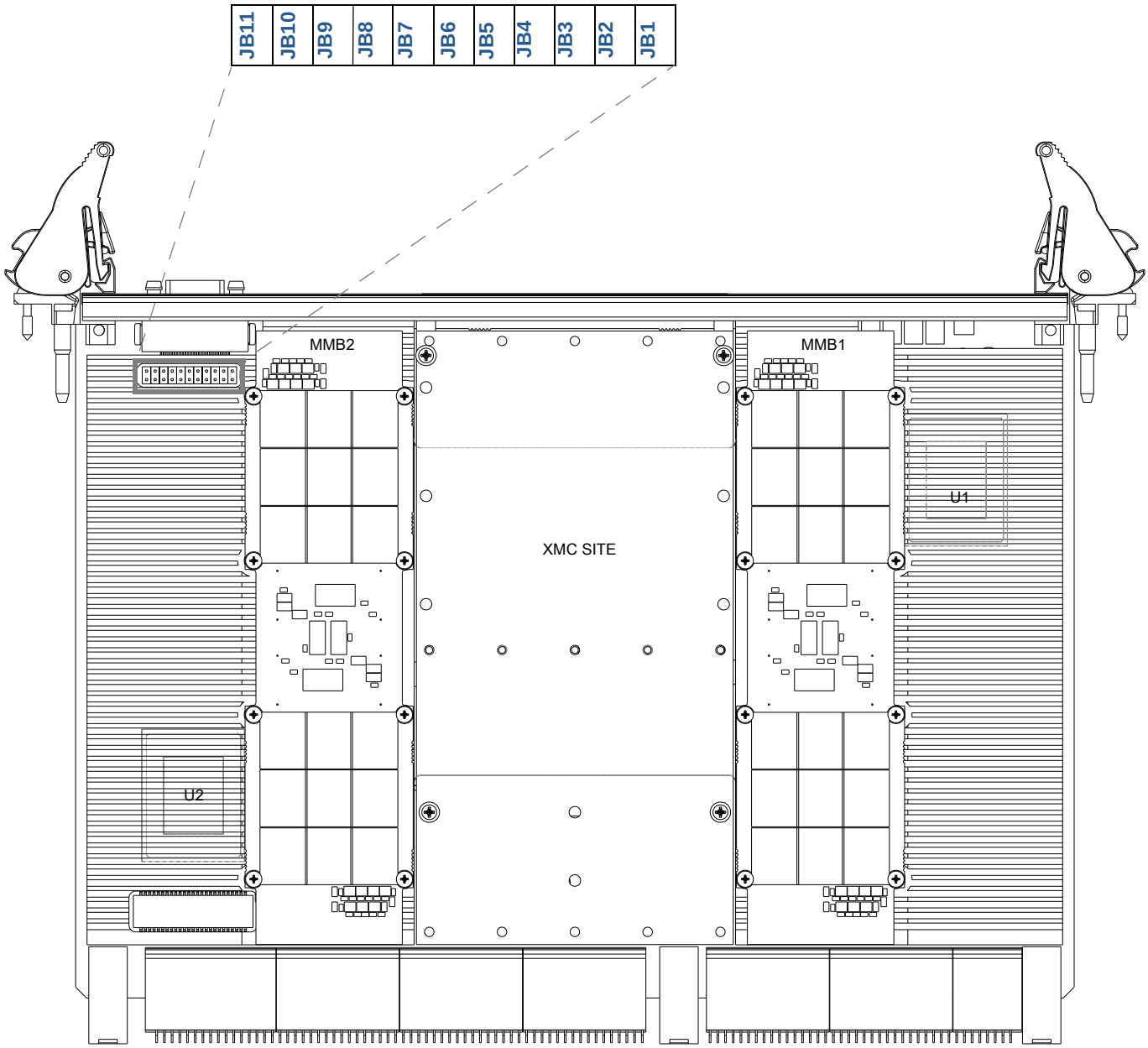


Cross Reference

A Rear Transition Module (RTM) is available for the CHAMP-AV8, that provides an alternative method of configuration control through the manipulation of specific backplane interface control signals. See "Rear Transition Module (RTM) Configuration Switches" on page A-57 for details.

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Figure 2.2: Configuration Jumper Locations



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3 HARDWARE INSTALLATION

IN THIS CHAPTER

This chapter provides the following information and procedures:

- "Installation Prerequisites" on page 3-3
  - "Installation Checklist" on page 3-3
  - "Unpack and Configure the Card" on page 3-3
  - "Install the XMC Module on the Basecard" on page 3-3
  - "Choose a VPX Slot Location" on page 3-4
- "Quick Installation and Power Up Procedure" on page 3-4
- "Detailed Installation Procedure" on page 3-4
  - "Insert the Basecard in the Chassis" on page 3-4
  - "Connect a Terminal" on page 3-5
  - "Connect Ethernet Ports" on page 3-6
  - "CBL-462-FPL-000 Front Panel Cable Connections" on page 3-8
  - "Booting: Entering the BIOS Setup Utility" on page 3-11
  - "Initiate the Power-Up Sequence" on page 3-12
  - "Display the Initial Screen Message" on page 3-13
- "Troubleshooting" on page 3-14
  - "Verify Insertion in Chassis" on page 3-14
  - "LED Diagnostics" on page 3-14
  - "LED Start-Up Sequence (Power On)" on page 3-19
  - "LED Start-Up Sequence (Reset)" on page 3-20
  - "Sign-on Message Garbled" on page 3-20

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INTRODUCTION

This chapter provides the following information and procedures:

- summary of installation prerequisites
- quick installation and power-up procedure
- detailed installation procedure
- displaying the initial screen message; and
- troubleshooting installation problems.



Cross Reference

Please refer to the CHAMPtools Software User's Manual for more detailed information describing the BIOS and the PBIT capabilities.

ELECTRO-STATIC DISCHARGE (ESD) PRECAUTIONS



Warning

This card uses components that are sensitive to electrostatic discharges. It must be kept in its conductive package until the installation begins. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card; static discharge can damage integrated circuits.

Turn the power off before inserting or removing cards from the VPX chassis. Failure to do so could damage the card circuitry or cause personal injury.

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INSTALLATION PREREQUISITES

Before installing the CHAMP-AV8 in your chassis, please take a moment to review the following items and planning considerations:

INSTALLATION CHECKLIST

Make sure you have the following items before proceeding with the installation:

- The CHAMP-AV8 board
- A VPX chassis with P0 connector. The chassis must be capable of providing +12 Volts on the VITA 46 VS1 and VS2 rails and +3.3 Volts on the VITA 46 3.3V_AUX rail. VS3 is not used (normally would be +5 Volts). For XMC usage, the chassis may also provide +12V_AUX and -12V_AUX (dependent on XMC requirements). An air-cooled chassis must provide a minimum inlet air flow of 20 CFM for L0 variants or 24 CFM for L100 variants, to ensure adequate cooling.
- A front panel cable, part number CBL-462-FPL-000, attached to a computer with a terminal emulator program capable of operating at 115200 baud. The front panel cable is used for air-cooled variants only.
- Standard Ethernet cables with RJ-45 connectors.
- The Board Support Package CD-ROM

UNPACK AND CONFIGURE THE CARD

Ensure that you complete the pre-installation tasks described in Chapter 2 of this manual and the pre-installation tasks described in the User's Manuals for any XMC module you need to install on the CHAMP-AV8.

INSTALL THE XMC MODULE ON THE BASECARD

If the XMC module is not already installed on the basecard, install it on your basecard using the appropriate mounting kit.



Cross Reference

Please refer to "XMC Module Installation Requirements" on page 2-4 for important information concerning the factors you need to consider before mounting an XMC Module on your CHAMP-AV8.

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CHOOSE A VPX SLOT LOCATION

If you want the CHAMP-AV8 to be the System Controller (SYSCON), install it in a slot that has a jumper allowing it to be the System Controller slot. If you are using another card as the SYSCON, the CHAMP-AV8 may be installed in any unoccupied slot.



Caution

For air-cooled boards, ensure the chassis is capable of generating minimal air flow required for proper cooling: 20 CFM for L0 variants or 24 CFM for L100 variants.

QUICK INSTALLATION AND POWER UP PROCEDURE

After configuring the backplane jumpers, perform the following steps:

1. With power off, install the CHAMP-AV8 into the chassis. Ensure the VPX connectors are fully engaged.
2. Connect the front panel cable (CBL-462-FPL-000) to the front panel port (air-cooled variants only) and the computer that will run the terminal emulator software.
3. Run the terminal emulation program. Set the serial port for 115200 baud, 8 data bits, no parity, 1 stop bit, and XON/XOFF flow control.
4. Apply power to the chassis. The red LED DS41 on the back of the card will come on and then turn off to indicate a successful load of the CF-FPGA. The front panel red FAIL LED will turn off. The board will initialize, displaying the BIOS splash screen.

At power-up, the front panel red Fail LED should turn off (see "LED Diagnostics" on page 3-14). If the red Fail LED fails to turn off, turn the power off then check the seating of the card and verify that the chassis supplies the proper backplane power (+12 V and +3.3 V).



Cross Reference

Please refer to the CHAMPtools Software User's Manual for detailed software installation procedures.

DETAILED INSTALLATION PROCEDURE

INSERT THE BASECARD IN THE CHASSIS

Ensure that the chassis power is turned off before inserting the card.

Air-Cooled L000/100 CHAMP-AV8

An air-cooled basecard is equipped with a faceplate compliant with IEEE 1101.10. The large ejectors/injectors on this faceplate facilitate insertion of the basecard into the chassis. Always use the injectors to seat the card in the chassis. Never press on the front panel to seat the card. Pressing on the front panel can cause the front panel to bow enough to damage the board and its components.

Once the basecard is inserted in the chassis, secure it by tightening the screws at the top and bottom of the faceplate.

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Caution

Never press forcefully on the front panel. Pressing forcefully on the front panel can cause the front panel to bow enough to damage the board and its components.

Conduction-Cooled L100/200 CHAMP-AV8

With conduction-cooled base cards, you must use a significant amount of insertion force to mate the backplane connectors with the VPX backplane. Use extra care when aligning and inserting your basecard into your chassis, to ensure that a secure mechanical and electrical connection is made between the card and the backplane mating connectors.

Once the basecard is inserted in the chassis, use a 3/32 hex torque driver/wrench to tighten the wedgelocks at the top and bottom of the card. The required torque is 6 in-lbs (67.8 N-cm).


Caution

Wedgelocks must be properly tightened before operating the board. Failure to properly tighten the wedgelocks can cause excessive over-heating of the CHAMP-AV8 board. The required torque for the wedgelocks is 6 in-lbs (67.8 N-cm).

CONNECT A TERMINAL

In order to access the features available within the embedded firmware on the CHAMP-AV8, you'll need to attach a terminal or PC-emulated equivalent to the Node A Serial Port 0 interface on the card. You can connect a terminal to the CHAMP-AV8 in one of the following ways:

- via the front panel connector (see "VPX6-462-A Front Panel" on page 1-37) using front panel cable CBL-462-FPL-000 (J2) (for the air-cooled version product only);
- via the J2 connector for Node A or J3 connector for Node B using RTM6-462-000 to facilitate the connection, available from the factory (for both air-cooled and conduction-cooled version products).


Tip

Default serial communication parameters are 115200 N, 8, 1 (115200 baud, no parity, 8 bits, 1 stop bit). Flow control is via software (XON/XOFF).

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CONNECT ETHERNET PORTS

For air-cooled versions of the board with the front panel Ethernet build option, both Ethernet ports MUST be accessed through the front panel connector using front panel cable CBL-462-FPL-000 (and can NOT be accessed through the VPX P4 connector). This can be accomplished by connecting a standard Ethernet cable between CBL-462-FPL-000 J4 and your Ethernet LAN.

For the air-cooled board with a backplane Ethernet build option, and for all conduction-cooled boards, the Ethernet port connections MUST be made through the VPX P4 connector. The connection through the VPX P4 connector can be made in one of the following ways:

- through the RTM6-462-000 Rear Transition Module. Once the RTM6-462-000 is connected to the back of the VPX slot in the chassis, a standard Ethernet cable can be connected to the "10/100/1000 ENET1" RJ-45 connector (J9 connector for Node A and J10 connector for Node B) on the RTM6-462-000.
- by wiring directly to the appropriate VPX P4 backplane connector pins.

Ethernet LEDs

The CHAMP-AV8 provides twelve LEDs on the bottom side of the PWB that provide link status and activity information for the Ethernet 1000 Base-T and 1000 Base-X ports. See Figure 3.1 on page 3-7 for details.

The function of these LEDs is as follows:

On Node A

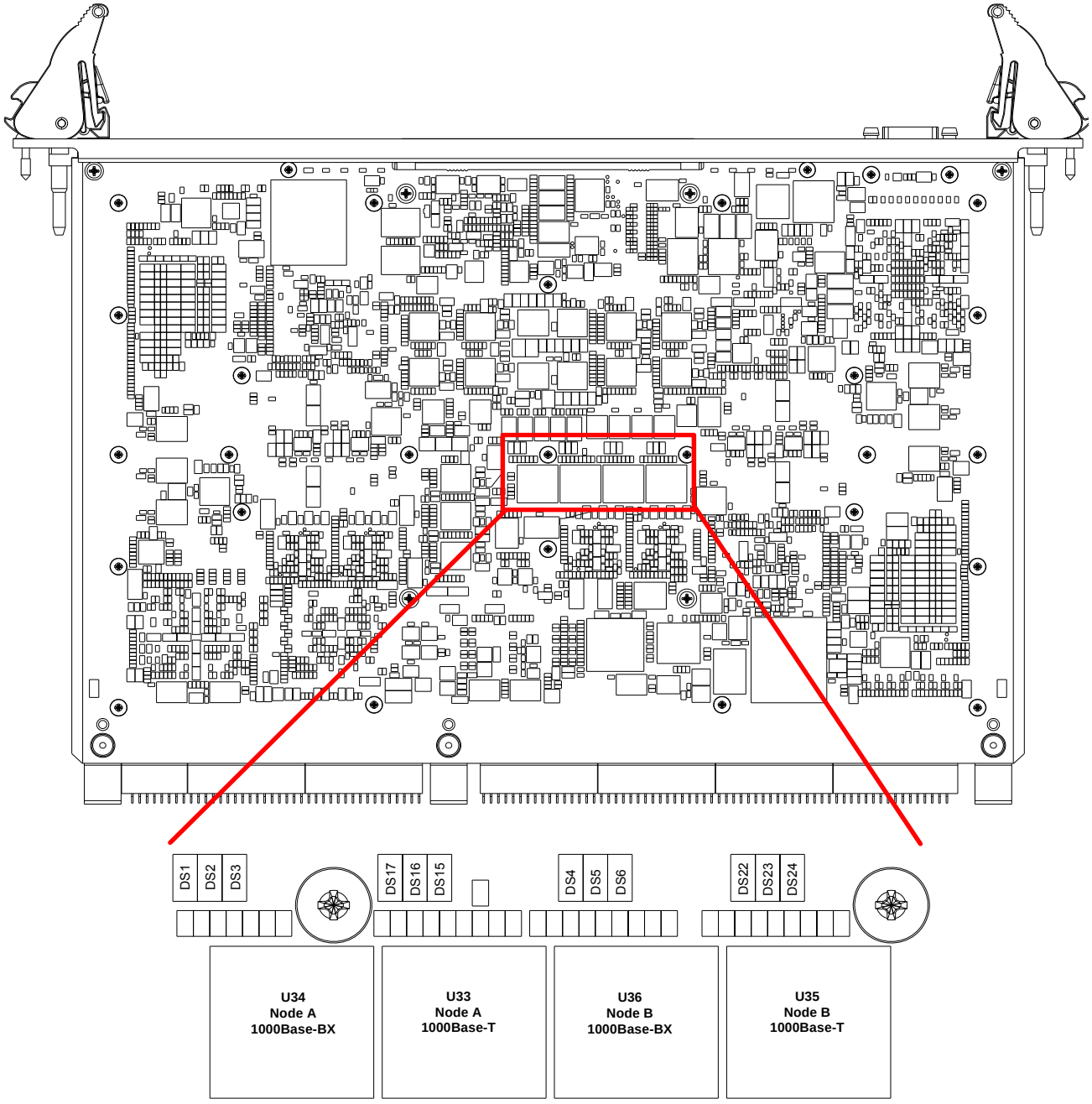
1000 Base-X (U34)	Function	LED
LED0_MODE	mode 0 = LINK_10/1000	DS3
LED1_MODE	mode 1 = LINK_100/1000	DS2
LED2_MODE	mode B = ACTIVITY	DS1
1000 Base-T (U33)	**Function**	**LED**
LED0_MODE	mode 0 = LINK_10/1000	DS15
LED1_MODE	mode 1 = LINK_100/1000	DS16
LED2_MODE	mode B = ACTIVITY	DS17

On Node B

1000 Base-X (U36)	Function	LED
LED0_MODE	mode 0 = LINK_10/1000	DS6
LED1_MODE	mode 1 = LINK_100/1000	DS5
LED2_MODE	mode B = ACTIVITY	DS4
1000 Base-T (U35)	**Function**	**LED**
LED0_MODE	mode 0 = LINK_10/1000	DS24
LED1_MODE	mode 1 = LINK_100/1000	DS23
LED2_MODE	mode B = ACTIVITY	DS22

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Figure 3.1: Location of CHAMP-AV8 Ethernet Activity LEDs



SOLDER SIDE (SECONDARY) SHOWN

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CBL-462-FPL-000 FRONT PANEL CABLE CONNECTIONS

The cable assemblies described in "Cable Requirements" on page 2-6 are available from Curtiss-Wright by ordering individual cables by their part numbers. Should you need to develop your own cabling solution, please refer to Appendix A of this manual for complete interface pinout listings for the front panel interface (as well as the VPX P0 through P6 interfaces).

Caution

The CHAMP-AV8 front panel cable is different than that used on the CHAMP-AV6, even though the physical front panel connector is the same. To use the CHAMP-AV8 front panel, the user must employ CBL-462-FPL-000.

Front Panel Cable J1 Connector (USB)

When connected to the front panel of the CHAMP-AV8, CBL-462-FPL-000 provides access to a USB 2.0 port via the J1 connector on the cable. This USB port connects to the Node A PCH only. There is no front panel USB connection to the Node B PCH. The pin assignments of the J1 connector are as follows:

Table 3.1: CBL-462-FPL-000 USB (J1) Signal Mapping

Signal Name	From P1 Pin	To J1 Contact	Comments
USB_A1_5V	11	1	
USB_A1_P	12	3	
USB_A1_N	25	2	
USB_A1_GND	26	4	

Front Panel Cable J2 Connector (EIA-232)

When connected to the front panel of the CHAMP-AV8, CBL-462-FPL-000 provides access to EIA-232 Node A Serial Port 0 via the J2 connector on the cable. The pin assignments of the J2 (Female DB-9) connector are as follows:

Table 3.2: CBL-462-FPL-000 EIA-232 Node A Serial Port 0 (J2) Signal Mapping

Signal Name	From P1 Pin	To J2 Contact	Comments
RS232_A0_TX	2	2	
RS232_A0_RX	15	3	
RS232-GND	1	5	

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Front Panel Cable J3 Connector (EIA-232)

When connected to the front panel of the CHAMP-AV8, CBL-462-FPL-000 provides access to EIA-232 Node B Serial Port 0 via the J3 connector on the cable. The pin assignments of the J3 (Female DB-9) connector are as follows:

Table 3.3: CBL-462-FPL-000 EIA-232 Node B Serial Port 0 (J3) Signal Mapping

Signal Name	From P1 Pin	To J3 Contact	Comments
RS232_B0_TX	13	2	
RS232_B0_RX	14	3	
RS232-GND	1	5	

Note

The CHAMP-AV8 serial ports do not provide access to the CTS and RTS signals. Therefore, software handshaking (XON/XOFF) must be used.

Note

The CHAMP-AV8 EIA-232 serial channels are configured as DCE (Data Communications Equipment). The EIA-232 serial channels on personal computers and terminals are configured as DTE, therefore a null modem is NOT required for communication between the CHAMP-AV8 and a PC terminal.

Front Panel Cable J4 Connector (Ethernet Port A)

When connected to the front panel of the CHAMP-AV8, CBL-462-FPL-000 provides access to Ethernet Port A via the J4 connector on the cable, on boards with the front panel Ethernet factory build option. The pin assignments of the J4 (Female RJ45) modular jack are as follows:

Table 3.4: CBL-462-FPL-000 Ethernet Port A (J4) Signal Mapping

Signal Name	From P1 Pin	To J4 Contact	Comments
ENET_A_TRD_P0	6	1	Twisted pair 1
ENET_A_TRD_N0	19	2	Twisted pair 1
ENET_A_TRD_P1	5	3	Twisted pair 2
ENET_A_TRD_N1	18	6	Twisted pair 2
ENET_A_TRD_P2	4	4	Twisted pair 3
ENET_A_TRD_N2	17	5	Twisted pair 3
ENET_A_TRD_P3	3	7	Twisted pair 4
ENET_A_TRD_N3	16	8	Twisted pair 4

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Front Panel Cable J5 Connector (Ethernet Port B)

When connected to the front panel of the CHAMP-AV8, CBL-462-FPL-000 provides access to Ethernet Port B via the J5 connector on the cable, on boards with the front panel Ethernet factory build option. The pin assignments of the J5 (Female RJ45) modular jack are as follows:

Table 3.5: CBL-462-FPL-000 Ethernet Port B (J5) Signal Mapping

Signal Name	From P1 Pin	To J5 Contact	Comments
ENET_B_TRD_P0	7	1	Twisted pair 1
ENET_B_TRD_N0	20	2	Twisted pair 1
ENET_B_TRD_P1	8	3	Twisted pair 2
ENET_B_TRD_N1	21	6	Twisted pair 2
ENET_B_TRD_P2	9	4	Twisted pair 3
ENET_B_TRD_N2	22	5	Twisted pair 3
ENET_B_TRD_P3	10	7	Twisted pair 4
ENET_B_TRD_N3	23	8	Twisted pair 4

Front Panel Cable SW1 Reset Pushbutton

When connected to the front panel of the CHAMP-AV8, CBL-462-FPL-000 provides access to a reset function via the SW1 Pushbutton on the cable. The pin assignments of SW1 pushbutton are as follows:

Table 3.6: CBL-462-FPL-000 Reset Pushbutton (SW1) Signal Mapping

Signal Name	From P1 Pin	To SW1 Contact	Comments
PB_RESET_L	24	1	
PB_RESET_GND	26	2	



Cross Reference

To facilitate connections to the interfaces on the CHAMP-AV8 via the backplane, a Rear Transition Module (RTM6-462-000) has been developed. For detailed information about the interfaces and configuration controls provided by the RTM, please refer to "Rear Transition Module (RTM)" on page A-52.

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BOOTING: ENTERING THE BIOS SETUP UTILITY

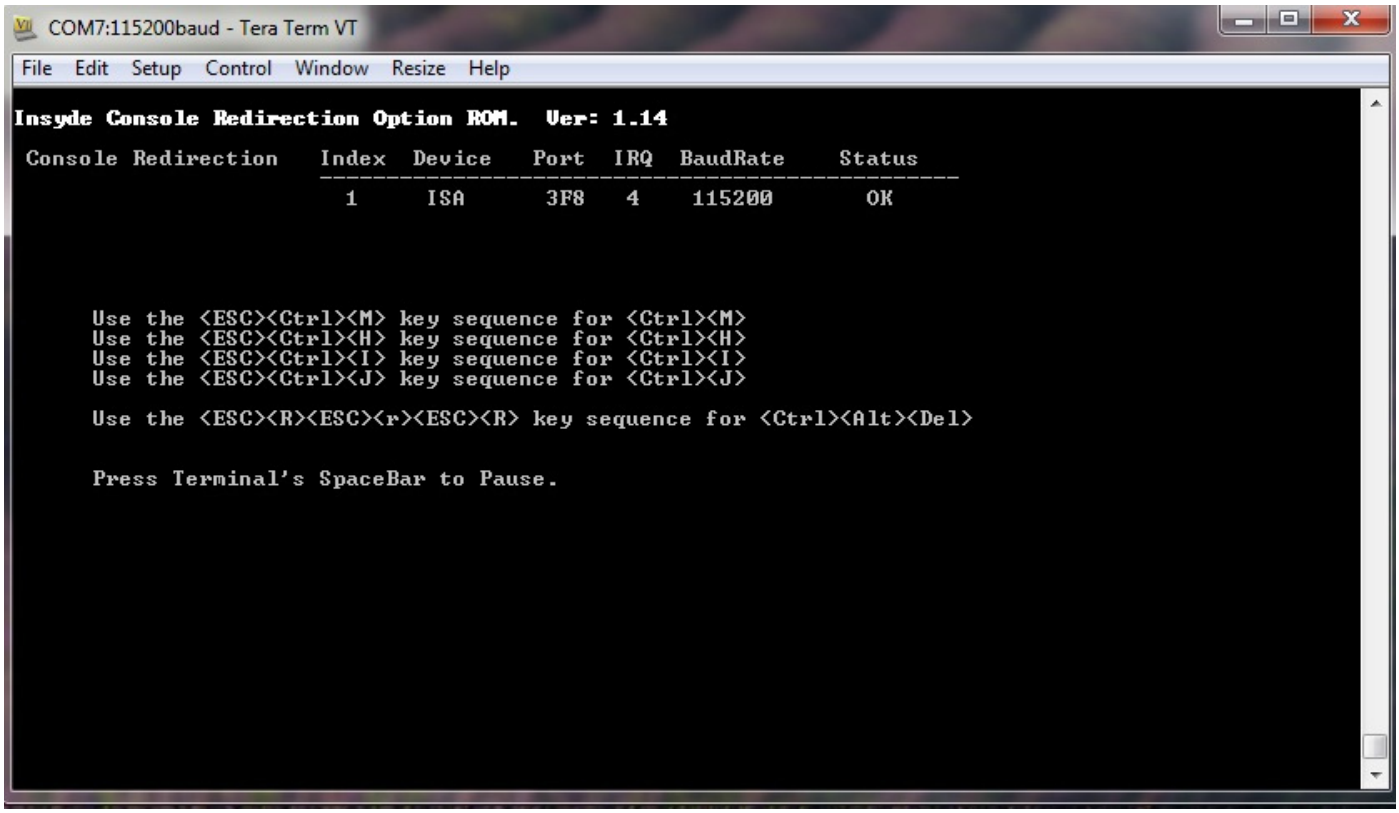
The BIOS is an embedded program that runs on both processors at hardware reset. Two copies of the BIOS reside in Flash memory for each processor node. These are stored as primary and alternate boot images. The primary image is field-upgradable. This approach allows the alternate image to be used if errors in the primary image upgrade process are encountered.

The BIOS configures all on-board resources and brings the board to an operational state and passes control to the operating system. Once the resources are configured, the PBIT application is executed if enabled. PBIT validates operation of the hardware devices present on the board. After completing initialization with a satisfactory result from PBIT, the BIOS either transitions to an application program, or interacts with the serial port accepting and processing maintenance commands.

Because the CHAMP-AV8 does not contain a video port, a serial terminal is required for communication during the board boot process. See "Connect a Terminal" on page 3-5 for details. One terminal is required per processor.

Serial Console Setup: As the system boots a text-based boot screen similar to the one shown below appears:

Figure 3.2: System Boot Screen



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Boot Choices

With the splash/text boot screen displayed, the following choices are available:

- Boot normally by doing nothing (you have about 2 seconds in which to press an alternate key). The initial Boot Menu screen seen in Figure 3.2 displays for a few seconds after which the board boots from the disk/device with the topmost priority as set in BIOS.
- Go directly to Initial Boot Menu screen.
  - Press any key except ENTER.
- Enter BIOS setup
  - Press F2 function key (USB keyboard only).
- Enter Boot Manager
  - Press F12 function key (USB keyboard only).



Cross Reference

Refer to the CHAMP-AV8 BIOS Setup Utility Software User's Manual (document 826450) for more information on the BIOS Setup Utility and Boot Manager.

An example of the initial screen message you will see once BIOS has completed is shown in "Display the Initial Screen Message" on page 3-13.

INITIATE THE POWER-UP SEQUENCE

This section describes the normal power-up behaviour of the CHAMP-AV8.

Each node of the CHAMP-AV8 boots independently. Upon power-up, an on-board power sequencer/reset controller turns on power supplies and asserts board reset signals according to preset timing. Once the processors are powered, each processor executes its BIOS, contained in boot flash devices dedicated for each node.

During boot, the user can elect to enter the BIOS setup utility by pressing the F2 key on a terminal connected via serial port to the CHAMP-AV8. Each processor requires a separate serial connection, and therefore a separate key press.

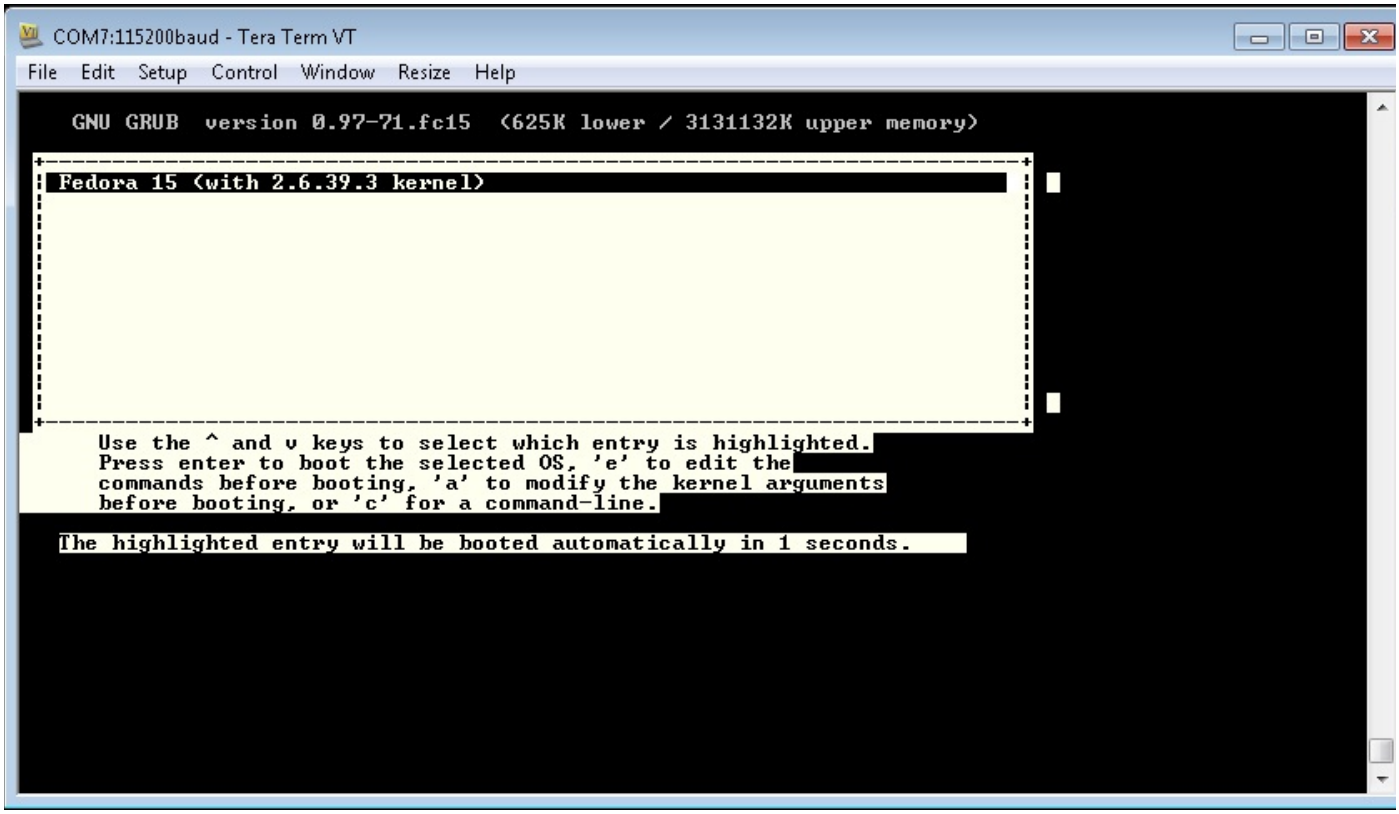
When the BIOS execution completes, the processor continues execution according to the first boot device recognized, per the priority established by that processor's BIOS boot configuration.

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DISPLAY THE INITIAL SCREEN MESSAGE

After power on, you have the option (available for about three seconds) to press the F2 key to activate the BIOS setup utility. If you don't press the F2 key, then you will see the following GRUB (GRand Unified Bootloader) loading message as follows:

Figure 3.3: GRUB Loading Message



After a couple of seconds, you will see Linux start loading, ultimately concluding with the login prompt as shown below:

```
Linux AV8 2.6.39.3 #45 SMP Fri Sep 7 10:44:41 EDT 2012 x86_64 x86_64 x86_64 GNU/Linux
Fedora release 10)
AV8 login:
```


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TROUBLESHOOTING

VERIFY INSERTION IN CHASSIS

Power down the chassis. Make sure that the card is properly seated in the VME chassis. Because of the five-row backplane, a considerable amount of insertion force is required to seat the card. Always utilize the injectors to seat the card.

LED DIAGNOSTICS

The CHAMP-AV8 has a front panel red Fail LED, eight front panel green Processor Status LEDs (air-cooled boards only), and eight green surface-mount LEDs. During the board power-up and reset sequences, the LEDs provide board diagnostic information.

Red Fail LED

The front panel red Fail LED indicates the health status of the CHAMP-AV8 board. The power sequencing circuitry monitors the backplane 12V and 3.3 V supplies. Once both supplies have reached their nominal voltage levels, the power sequencing circuitry turns on the on-board power. When on-board (sequenced) power is applied, the red Fail LED illuminates, indicating that on-board power is applied. The red Fail LED will remain illuminated as the boot software executes. Once the board successfully boots and PBIT passes (if enabled), the boot software then turns off the red Fail LED, indicating that a fault condition has not been detected. If a fault condition is detected, the boot software will not turn off the red Fail LED. After a board reset, the red Fail LED will automatically illuminate and remain illuminated until the board has successfully booted as described above.

Green Front Panel Processor Status LEDs

At power-on, the eight front panel green Processor Status LEDs provide board status information. After the CF-FPGA has been successfully configured, the green Processor Status LEDs will illuminate. As the boot software initializes each processor node, the software will turn the respective LED off. Once the board has successfully booted, the LEDs will be turned off and become available for user control through the board registers. After a board reset, the green Processor Status LEDs will automatically illuminate and remain illuminated until the boot software initializes each processor node as described above.

Green Surface Mount Status LEDs

At power-on, the eight green surface mount Status LEDs provide board status information. After the CF-FPGA has been successfully configured, the green surface mount Status LEDs will illuminate. After the boot software has initialized all of the processor nodes, the software will turn off all of the green Status LEDs. Once the board has successfully booted, the LEDs will be turned off and become available for user control through the board registers.

After a board reset, the green surface mount Status LEDs will automatically illuminate and stay illuminated until the boot software initializes all of the processor nodes as described above.



Cross Reference

Additional LEDs are provided that show link status and activity for Ethernet 1000Base-BX and 1000Base-T ports, SATA and PCI express links. See Table 3.7, "Summary of LED Behavior," on page 3-15 for a description of LED behavior.

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Table 3.7: Summary of LED Behavior

Location	Reference Designator	Color	LED Purpose/ Function	Behavior during Normal Operation or Feature in Use	Behavior during Abnormal Operation or Feature Not in Use
Front Panel – Air Cooled	A0 (DS28-1)	Green	Processor status indicator - Node A core 0 Same as DS37.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	A1 (DS28-3)	Green	Processor status indicator - Node A core 1 Same as DS38.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	A2 (DS27-1)	Green	Processor status indicator - Node A core 2 Same as DS39.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	A3 (DS27-3)	Green	Processor status indicator - Node A core 3 Same as DS40.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	B0 (DS25-1)	Green	Processor status indicator - Node B core 0 Same as DS21.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	B1 (DS25-3)	Green	Processor status indicator - Node B core 1 Same as DS20.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	B2 (DS26-1)	Green	Processor status indicator - Node B core 2 Same as DS19.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	B3 (DS26-3)	Green	Processor status indicator - Node B core 3 Same as DS18.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Front Panel – Air Cooled	FAIL (DS54)	Red	Fail LED Same as DS55.	OFF – Turned off by firmware	ON – Defaults to on by hardware and must be turned off by on-board diagnostic firmware.

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Table 3.7: Summary of LED Behavior (Continued)

Location	Reference Designator	Color	LED Purpose/ Function	Behavior during Normal Operation or Feature in Use	Behavior during Abnormal Operation or Feature Not in Use
Top of PWB Conduction–Cooled	DS37	Green	Processor status indicator - Node A core 0 Same as DS28-1.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS38	Green	Processor status indicator - Node A core 1 Same as DS28-3.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS39	Green	Processor status indicator - Node A core 2 Same as DS27-1.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS40	Green	Processor status indicator - Node A core 3 Same as DS27-3.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS21	Green	Processor status indicator - Node B core 0 Same as DS25-1.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS20	Green	Processor status indicator - Node B core 1 Same as DS25-3.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS19	Green	Processor status indicator - Node B core 2 Same as DS26-1.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS18	Green	Processor status indicator - Node B core 3 Same as DS26-3.	ON – Turned on by firmware	OFF – Defaults off and must be turned on by firmware when the processor status is good.
Top of PWB Conduction–Cooled	DS55	Red	Fail LED Same as DS54.	OFF– Turned off by firmware	ON – Defaults to on by hardware and must be turned off by on-board diagnostic firmware

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Table 3.7: Summary of LED Behavior (Continued)

Location	Reference Designator	Color	LED Purpose/ Function	Behavior during Normal Operation or Feature in Use	Behavior during Abnormal Operation or Feature Not in Use
Bottom of PWB	DS9	Green	PCIe switch port 16 link-up indicator	ON – Indicates PCIe link-up status to the x8 link on P2 expansion plane (EP00:EP07)	OFF – Indicates PCIe link-down status to the x8 link on P2 expansion plane (EP00:EP07)
Bottom of PWB	DS10	Green	PCIe switch port 4 link-up indicator	ON – Indicates PCIe link-up status to either the XMC site or the P2 expansion plane (depending on build option)	OFF – Indicates PCIe link-down status on the XMC x8 link or the build option link on the P2 Expansion Plane (EP08:EP15)
Bottom of PWB	DS11	Green	PCIe switch port 0 link-up indicator	ON – Indicates PCIe link-up status between the PCIe switch and the Node B processor	OFF – Indicates PCIe link-down status between the PCIe switch and the Node A processor
Bottom of PWB	DS12	Green	PCIe switch port 8 link-up indicator	ON – Indicates PCIe link-up status between the PCIe switch and the Node B processor	OFF – Indicates PCIe link-down status between the PCIe switch and the Node B processor
Bottom of PWB	DS15	Green	Node A 1000Base-T link status bit 0	ON – Indicates the 1000 Mbps link is established and maintained	N/A
Bottom of PWB	DS16	Green	Node A 1000Base-T link status bit 1	ON – Indicates the 1000Mbps link is established and maintained Flashing – Indicates the link is established and there is transmit or receive activity	OFF – Indicates the link is down
Bottom of PWB	DS17	Green	Node A 1000Base-T link status bit 2	ON – Indicates the 1000Mbps link is established and maintained	OFF – Indicates the 1000Mbps link is down
Bottom of PWB	DS24	Green	Node B 1000Base-T link status bit 0	ON – Indicates the 1000 Mbps link is established and maintained	N/A
Bottom of PWB	DS23	Green	Node B 1000Base-T link status bit 1	ON–Indicates the link is established and there is no transmit and receive activity Flashing – Indicates the link is established and there is transmit and receive activity	OFF – Indicates the 1000Mbps link is down
Bottom of PWB	DS22	Green	Node B 1000Base-T link status bit 2	ON – Indicates the 1000Mbps link is established and maintained	OFF – Indicates the 1000Mbps link is down

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Table 3.7: Summary of LED Behavior (Continued)

Location	Reference Designator	Color	LED Purpose/ Function	Behavior during Normal Operation or Feature in Use	Behavior during Abnormal Operation or Feature Not in Use
Bottom of PWB	DS3	Green	Node A 1000Base-BX MDI/Copper-side interface link status bit 0	OFF – Indicates the 1000 Mbps link is down. This LED is expected to stay off during normal operation for 1000Base-BX	N/A
Bottom of PWB	DS2	Green	Node A 1000Base-BX MDI/Copper-side interface link status bit 1	ON – Indicates the link is established and there is no transmit and receive activity. Flashing – Indicates the link is established and there is transmit and receive activity.	OFF – Indicates the 1000 Mbps link is down
Bottom of PWB	DS1	Green	Node A 1000Base-BX MDI/Copper-side interface link status bit 2	ON – Indicates the 1000 Mbps link is established and maintained	OFF – Indicates the 1000 Mbps link is down
Bottom of PWB	DS6	Green	Node B 1000Base-BX MDI/Copper-side interface link status bit 0	OFF – Indicates the 1000 Mbps link is down This LED is expected to stay off during normal operation for 1000 Base-BX	N/A
Bottom of PWB	DS5	Green	Node B 1000Base-BX MDI/Copper-side interface link status bit 1	ON – Indicates the link is established and there is no transmit and receive activity	OFF – Indicates the 1000 Mbps link is down
Bottom of PWB	DS4	Green	Node B 1000Base-BX MDI/Copper-side interface link status bit 2	ON – Indicates the 1000 Mbps link is established and maintained	OFF – Indicates the 1000 Mbps link is down
Bottom of PWB	DS35	Green	Indicates SATA activity on Node A on-board Solid State Drive or an external SATA drive. This does not indicate link status.	ON – Indicates activity on the SATA link. OFF – Indicates no SATA activity	N/A
Bottom of PWB	DS36	Green	Indicates SATA activity on Node B on-board Solid State Drive or an external SATA drive. This does not indicate link status.	ON – Indicates activity on the SATA link. OFF – Indicates no SATA activity	N/A

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Table 3.7: Summary of LED Behavior (Continued)

Location	Reference Designator	Color	LED Purpose/ Function	Behavior during Normal Operation or Feature in Use	Behavior during Abnormal Operation or Feature Not in Use
Bottom of PWB	DS7	Green	1000Base-BX	Reserved	Reserved
Bottom of PWB	DS8	Green	1000Base-BX	Reserved	Reserved
Bottom of PWB	DS41	Red	Configurator FPGA Load Status	OFF – Indicates FPGA loaded successfully	ON – Indicates FPGA failed to load successfully
Bottom of PWB - Air Cooled	DS42	Red	Thermal failure Indicator	Off - Indicates the board is operating within its acceptable temperature range	ON – Indicates that an excessive temperature condition has been detected
Top of PWB – Conduction Cooled	DS34	Red	Thermal failure Indicator	Off - Indicates the board is operating within its acceptable temperature range	ON – Indicates that an excessive temperature condition has been detected
Bottom of PWB	DS13	Green	FPGA	Not intended for customer use	
Bottom of PWB	DS29, DS30, DS31, DS32, DS33	Green	CPLD	Not intended for customer use	

LED START-UP SEQUENCE (POWER ON)

The power-on LED start-up sequence is a follows:

1. Front panel red Fail LED illuminates:
   - indicates on-board power applied
2. Front panel green Processor Status LEDs (air-cooled boards) or surface mount Green Status LEDs (conduction-cooled boards) illuminate:
   - indicates successful FPGA programming
3. Front panel green Processor Status LEDs are turned off (one node at a time):
   - indicates successful initialization of respective node
4. Surface mount green Status LEDs are turned off:
   - indicates successful initialization of all nodes
5. Front panel red Fail LED

   Normal Boot Mode:
   - turned off - indicates successful boot and PBIT passed (if PBIT enabled)
   - begins flashing - indicates failure

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Recovery Boot Mode: flashing

Boot Inhibit Mode: flashing

LED START-UP SEQUENCE (RESET)

The reset LED start-up sequence is a follows:

1. Front panel red Fail LED, front panel green Processor Status LEDs, and surface mount Status LEDs all illuminated:
   - indicates board reset
2. Front panel green Processor Status LEDs are turned off (one node at a time):
   - indicates successful initialization of respective node
3. Surface mount green Status LEDs turned off:
   - indicates successful initialization of all nodes
4. Front panel red Fail LED

   Normal Boot Mode:
   - turned off - indicates successful boot and PBIT passed (if PBIT enabled)
   - begins flashing - indicates failure

   Recovery Boot Mode: flashing

   Boot Inhibit Mode: flashing

SIGN-ON MESSAGE GARBLED

If the sign-on message is garbled, check that your terminal settings match 115200, 8, N, 1 (115200 baud, 8 data bits, no parity, 1 stop bit). Also, ensure that you are using a cable compatible with those listed in "Cable Requirements" on page 2-6.

THE NEXT STEP



Cross Reference

Once the hardware is correctly configured and installed in the chassis, the next step is to install the CHAMPtools software. See the section "Software Installation" in Chapter 2 of your CHAMPtools Software User's Manual, which is included in Acrobat pdf format on your CHAMPtools CD-ROM.

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A

CONNECTOR PIN ASSIGNMENTS

IN THIS APPENDIX

This appendix provides the interface pinout information for each of the connectors on the CHAMP-AV8. The following connectors are described:

- "Connector Overview" on page A-3
  - "Backplane VPX Connectors" on page A-3
  - "About VITA 46 and ANSI/VITA 65" on page A-4
  - "CHAMP-AV8 I/O Mapping" on page A-8
  - "Using the CHAMP-AV8 Pinout Configurator" on page A-10
- "Backplane VPX Connectors—Detailed Description" on page A-14
  - "CHAMP-AV8 P0 Utility Connector Pin Assignments" on page A-14
  - "Corresponding VPX Backplane J0 Utility Connector Pin Assignments" on page A-16
  - "CHAMP-AV8 P1 (SRIO Fabric) Connector Pin Assignments" on page A-17
  - "Corresponding VPX Backplane J1 (SRIO Fabric) Connector Pin Assignments" on page A-19
  - "CHAMP-AV8 P2 (PCIe Expansion) Connector Pin Assignments" on page A-20
  - "Corresponding VPX Backplane J2 (PCIe Expansion) Connector Pin Assignments" on page A-22
  - "CHAMP-AV8 P3 (XMC Site's PMC User I/O) Connector Pin Assignments" on page A-23
  - "Corresponding VPX Backplane J3 (XMC Site's PMC User I/O) Connector Pin Assignments" on page A-25
  - "CHAMP-AV8 P4 (Basecard I/O) Connector Pin Assignments" on page A-26
  - "Corresponding VPX Backplane J4 (Basecard I/O) Connector Pin Assignments" on page A-29

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  - "CHAMP-AV8 P5 (XMC User I/O) Connector Pin Assignments" on page A-30
  - "Corresponding VPX Backplane J5 (XMC User I/O) Connector Pin Assignments" on page A-32
  - "CHAMP-AV8 P6 (XMC/DIO/SATA/USB) Connector Pin Assignments" on page A-33
  - "Corresponding VPX Backplane J6 (XMC/DIO/SATA/USB) Connector Pin Assignments" on page A-35
- "J1 Front Panel Connector" on page A-36
- "XMC Site's PMC J14 Connector" on page A-39
  - "XMC Site's PMC J14 User I/O Connector" on page A-39
- "XMC J15 and J16 Connectors" on page A-42
  - "XMC J15 Connector" on page A-42
  - "XMC J16 User I/O Connector" on page A-45
- "Rear Transition Module (RTM)" on page A-52
  - "Rear Transition Module Panel-Mounted Connectors" on page A-54
  - "Rear Transition Module (RTM) Configuration Switches" on page A-57
  - "Rear Transition Module (RTM) PWB Header Connectors" on page A-58

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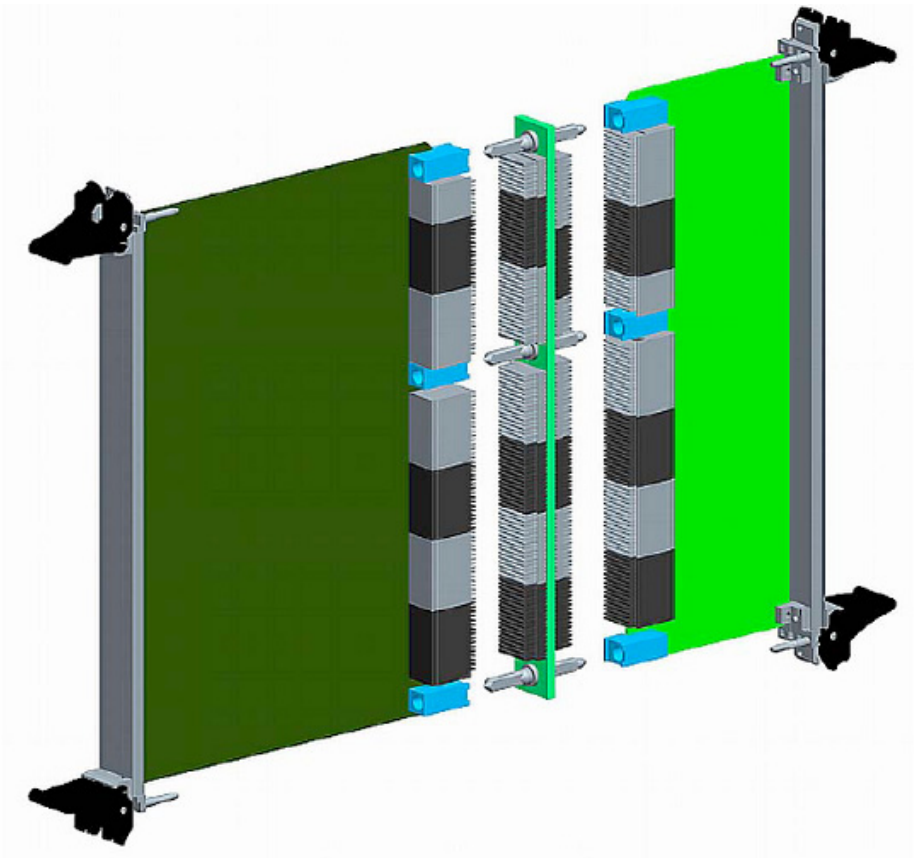
CONNECTOR OVERVIEW

This appendix provides the interface pinout information for each of the connectors on the CHAMP-AV8, and explains how you can use the Pinout Configurator utility to generate custom pinout tables based on the type and location of any XMC modules you choose to install on the basecard. The corresponding VPX Backplane interface pin assignments are also provided.

BACKPLANE VPX CONNECTORS

The industry VITA 46 series standards define the details of VPX system connectors from the front plug-in module to the backplane front-side, backplane rear-side, and Rear Transition Module (RTM), including mechanical dimensions, part numbers, and electrical pin definitions. Figure A.1 below provides an illustration of how the VPX connectors are mated from a system point of view.

Figure A.1: VPX System Connectors Overview



Note

A Rear Transition Module (RTM) is available to facilitate connectivity with the CHAMP-AV8. Detailed information about the RTM is provided in "Rear Transition Module (RTM)" on page A-52.

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ABOUT VITA 46 AND ANSI/VITA 65

The CHAMP-AV8 meets the requirements set out in the VITA 46.0 (base specification), VITA 46.3 (SRIO on P1), and VITA 65 (PCIe on P2 and 1000Base-BX on P4). VPX delivers significantly more I/O capability, almost twice what would be expected from a VME 64X class card. All I/O pins are multi-gigabyte capable up to 6.25 Gbits/sec. And with the auxiliary VITA 48 standard there is the option for significantly more power dissipation per slot.

The CHAMP-AV8 employs Tyco VPX RT2 connectors, that incorporate a wafer style design that provides tightly controlled impedance, low insertion loss, and less than 3% crosstalk at signalling rates up to 6.25Gbaud. By default, the CHAMP-AV8 is configured for 5Gbaud SRIO backplane interfaces.

The wafer converts a 7-row interface on the "P" (CHAMP-AV8 PWB) side of the connector, to a 9-row interface on the "J" (backplane) side of the connector. Tables for both sides of the connector are provided starting on page A-15 of this appendix.

Figure A.2 shows the module construction and differential tracking of the signal traces of the Tyco 7-row MultiGig RT-2 connector.

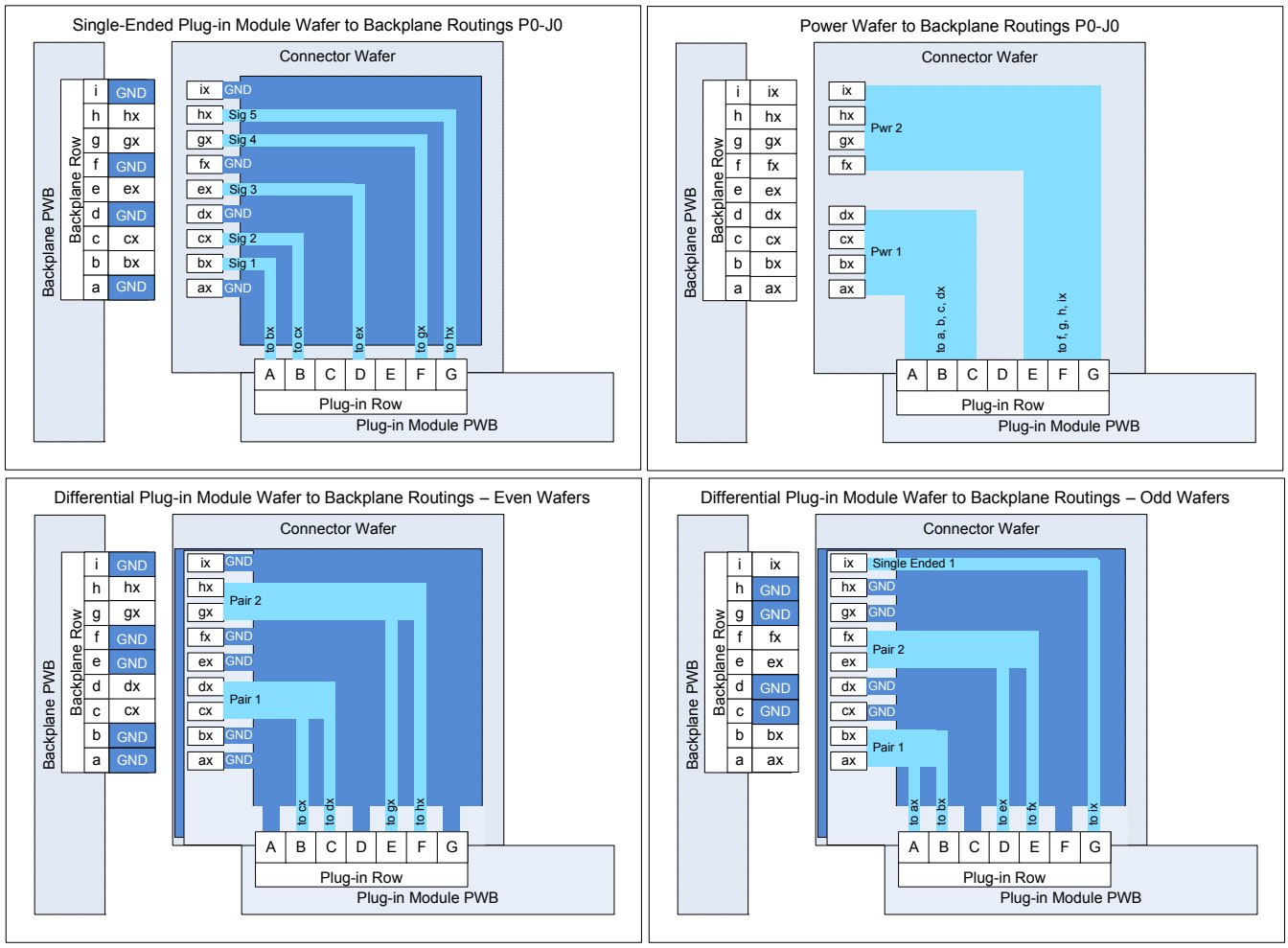
Figure A.2: VPX RT2 Type Connector



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With reference to Figure A.3 below, four types of wafers are used, including power, single ended, or differential (with odd or even routing configurations). The P0 through P6 connectors on the CHAMP-AV8 employ these different wafer types in specific combinations to meet the requirements of the interface.

Figure A.3: VPX RT2 Wafer Routings



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VPX P0 Utility Connector

The backplane P0 provides power supplies, testing, clock, and I2C utilities, etc, for the VPX system. With reference to Figure A.3 on page A-5, the CHAMP-AV8 P0 connector uses the following combination of wafers:

Table A.1: Wafer Usage - CHAMP-AV8 P0 Utility Connector

Wafer Number	Wafer Type
1	Power
2	Power
3	Power
4	Single-Ended
5	Single-Ended
6	Single-Ended
7	Differential (odd)
8	Differential (even)

VPX P1 - P6 Connectors

The P1 to P6 connectors provide Open-VPX SRIO Data Plane links and GE Control Plane links, and employ the following wafers:

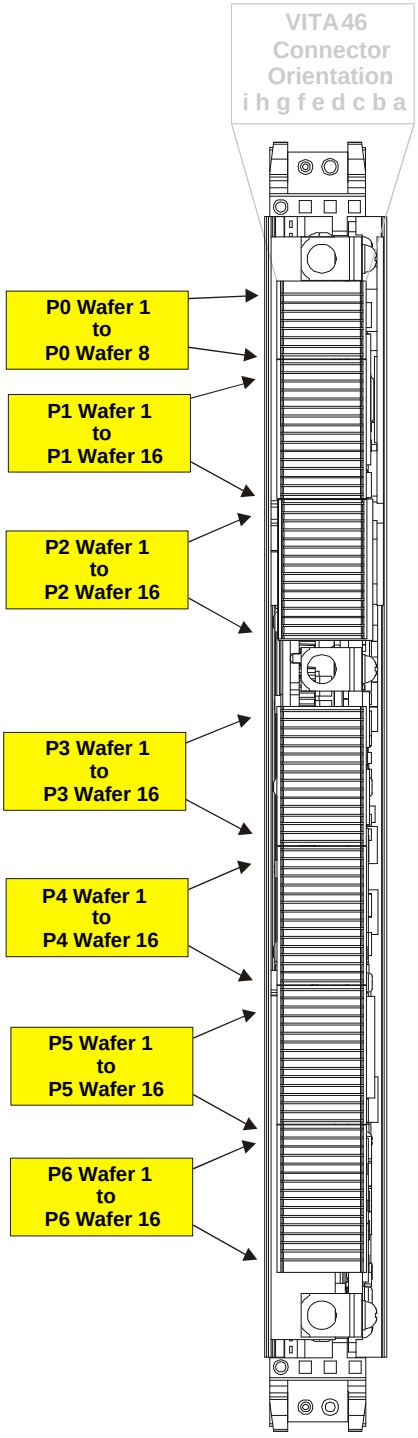
Table A.2: Wafer Usage - CHAMP-AV8 P1-P6 Connectors

Wafer Number	Wafer Type
1	Differential (odd)
2	Differential (even)
3	Differential (odd)
4	Differential (even)
5	Differential (odd)
6	Differential (even)
7	Differential (odd)
8	Differential (even)
9	Differential (odd)
10	Differential (even)
11	Differential (odd)
12	Differential (even)
13	Differential (odd)
14	Differential (even)
15	Differential (odd)
16	Differential (even)

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The layout of the VPX P0 through P6 connectors is shown in Figure A.4 below:

Figure A.4: CHAMP-AV8 Backplane P0-P6 Connector Orientation

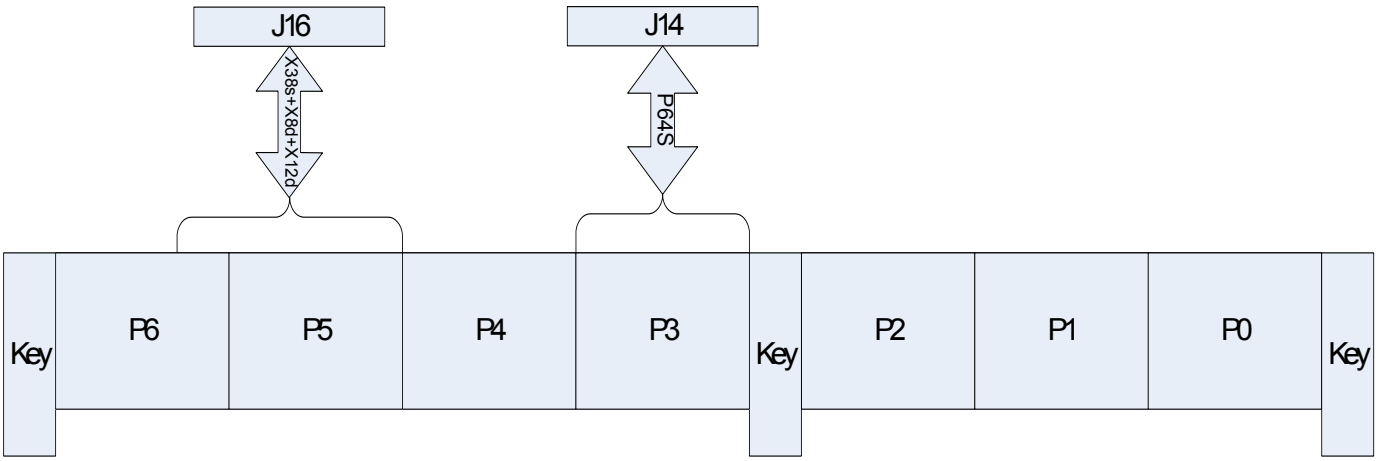


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CHAMP-AV8 I/O MAPPING

With reference to Figure A.5, the I/O mapping of the various CHAMP-AV8 connectors is summarized in the following sections.

Figure A.5: I/O Mapping to the CHAMP-AV8 VITA 46 Connectors



XMC I/O Mapping

The CHAMP-AV8 incorporates one XMC site that populates both the PMC (J14) and the XMC (J16) I/O connectors.

- The XMC J14 connector (PMC I/O) is mapped to the VITA 46 P3 connector according to VITA 46.9 P64s pattern. See "Corresponding VPX Backplane J2 (PCIe Expansion) Connector Pin Assignments" on page A-22 for details.
- The XMC J16 connector (XMC I/O) is mapped to the VITA 46 P5 and P6 connectors according to VITA 46.9, P5w3P6-X38s+X8d+X12d pattern. See "CHAMP-AV8 P5 (XMC User I/O) Connector Pin Assignments" on page A-30 and "CHAMP-AV8 P6 (XMC/DIO/SATA/USB) Connector Pin Assignments" on page A-33 for details.

VITA 46 P0 Utility Connector

The P0 connector on the CHAMP-AV8 supports the following functions/interfaces:

- Power and Ground (BP12V, 3V3AUX, 12AUX, N12AUX, GND) signals
- Geographical Addressing (GA_L[4:0] and GAP_L) signals
- Differential Reference Clock (REF_CLK_P/N) signals
- System Reset (SYSRST_L) signal
- JTAG (TCLK, TDO, TDI, TMS, TRST_L) signals
- AUX_CLK_P/N signals
- No Connect (NC) signals

See "CHAMP-AV8 P0 Utility Connector Pin Assignments" on page A-14 for additional details.

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VITA 46 P1 Fabric Connector

The P1 connector on the CHAMP-AV8 supports the following functions/interfaces:

- V46 Fabric Connections (Four 4x Ports)
- Reserved Bus (BP_GDISCRETE1) signal
- VITA 46 and CHAMP-AV8 System Signals (SYSCON_L, CARD_FAIL_L, PB_RESET_L)
- Nominal 3V battery connection (VBAT)
- No Connect (NC) Signals (NC_RFU, NC_IO_RSRV)

See "CHAMP-AV8 P1 (SRIO Fabric) Connector Pin Assignments" on page A-17 for additional details.

VITA 46 P2 PCIe Expansion Connector

The P2 connector on the CHAMP-AV8 supports the following functions/interfaces:

- PCIe expansion plane - supports up to two eight-lane PCIe ports (see Table 1.1, "XMC/Expansion Plane Interface Build-Time Options for PCIe," on page 1-8 for details).

See "CHAMP-AV8 P2 (PCIe Expansion) Connector Pin Assignments" on page A-20 for additional details.

VITA 46 P3 XMC Site's PMC User I/O Connector

The P3 connector on the CHAMP-AV8 supports the following functions/interfaces:

- Utilized for XMC J14 user I/O as per the VITA 46.9 P64s pattern.
- No Connect (NC) Signals

See "Corresponding VPX Backplane J2 (PCIe Expansion) Connector Pin Assignments" on page A-22 for additional details.

VITA 46 P4 Basecard I/O Connector

The P4 connector on the CHAMP-AV8 supports the following functions/interfaces:

- CHAMP-AV8 JTAG Selection Signals (JTSEL_L, JPROC[3:0])
- Reset/Power Sequencer/JTAG CPLD JTAG Chain Signals
- CHAMP-AV8 Backplane Jumper Signals
- CHAMP-AV8 EIA-422/485 Serial Ports (RS422_[A2/B2] TX/RX)
- CHAMP-AV8 EIA-232 Serial Ports (RS232_[A0/A1/B0/B1] TX/RX)
- 1000Base-T Ports (ETH[A/B]_TRX[0:3])
- 1000Base-BX Ports (UTP[A/B] TX/RX)

See "CHAMP-AV8 P4 (Basecard I/O) Connector Pin Assignments" on page A-26 for additional details.

VITA 46 P5 XMC User I/O Connector

The P5 connector on the CHAMP-AV8 supports the following functions/interfaces:

- XMC Site Single Ended User I/O (38 signals) from XMC J16 connector (XMC_C[19:01] and XMC_F[19:01])
- XMC Site Differential User I/O (8 of the 20 pairs) from XMC J16 connector (XMC_DP[03:00] and XMC_DP[13:10])

See "CHAMP-AV8 P5 (XMC User I/O) Connector Pin Assignments" on page A-30 for additional details.

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VITA 46 P6 XMC/DIO/SATA/ USB Connector

The P6 connector on the CHAMP-AV8 supports the following functions/interfaces:

- XMC Site Differential User I/O (12 of the 20 pairs) from XMC J16 connector (XMC_DP[09:04] and XMC_DP[19:14])
- DIO Signals (DIO[15:0])

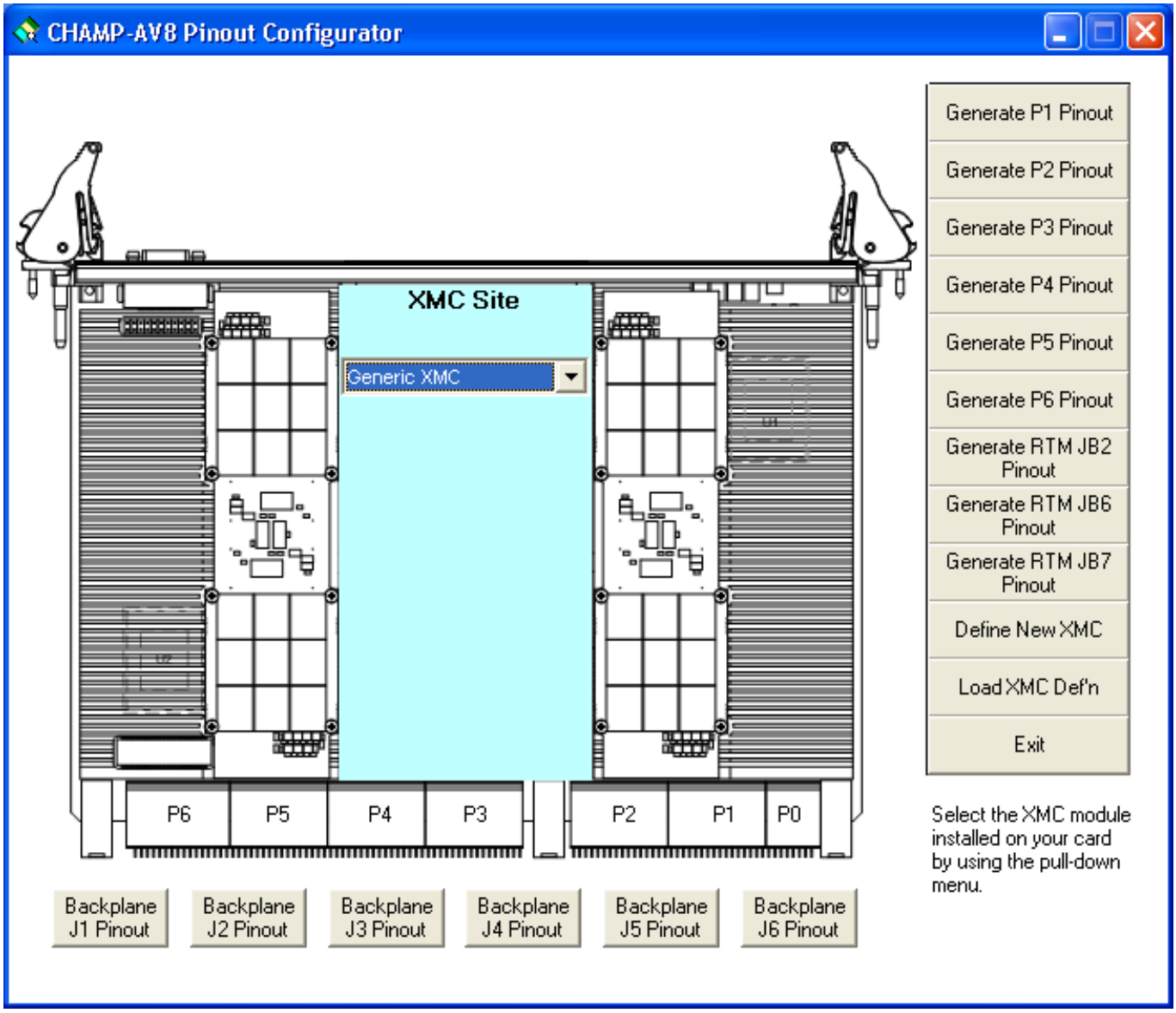
See "CHAMP-AV8 P6 (XMC/DIO/SATA/USB) Connector Pin Assignments" on page A-33 for additional details.

USING THE CHAMP-AV8 PINOUT CONFIGURATOR

The backplane pinouts of the CHAMP-AV8 vary according to the XMC modules installed on the basecard. The Continuum Support Center website (http://csc.cwcdefense.com) provides a Windows utility that generates the pinout configuration based on the modules installed. This utility lets you choose from existing Curtiss-Wright XMC modules, or describe pinouts for third-party or future Curtiss-Wright modules. Figure A.6 shows the Pinout Configurator's Main Window.

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Figure A.6: CHAMP-AV8 Pinout Configurator Main Window



SELECTING THE XMC MODULE

1. The main window has one drop-down list for the single XMC slot on the CHAMP-AV8. From the drop-down list, choose the module you have installed (see Figure A.6 on page A-11).

Cross Reference

If your CHAMP-AV8 has an XMC module installed that is not listed in the drop-down list, refer to "Defining New XMC Modules" on page A-13.

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GENERATING PINOUTS

2. To generate a connector pinout table for your CHAMP-AV8, click a **Generate Pinout** button. The application displays the corresponding pinout table for your configuration, as shown in the example in Figure A.7 below.

   You may adjust the column widths of the table by dragging the column guides in the header row.

Figure A.7: Sample P5 Pinout Table

CHAMP-AV8 P5 Connector Pin Assignments

Drag the column guides to adjust the width.

XMC Site is Generic XMC

	G	F	E	D	C	B	A
1	Not Connected	GND	Not Connected	Not Connected	GND	Not Connected	Not Connected
2	GND	Not Connected	Not Connected	GND	Not Connected	Not Connected	GND
3	Not Connected	GND	Not Connected	Not Connected	GND	XMC1-C1	XMC1-F1
4	GND	XMC1-C2	XMC1-C3	GND	XMC1-F2	XMC1-F3	GND
5	Not Connected	GND	XMC1-C4	XMC1-C5	GND	XMC1-F4	XMC1-F5
6	GND	XMC1-C6	XMC1-C7	GND	XMC1-F6	XMC1-F7	GND
7	Not Connected	GND	XMC1-C8	XMC1-C9	GND	XMC1-F8	XMC1-F9
8	GND	XMC1-C10	XMC1-C11	GND	XMC1-F10	XMC1-F11	GND
9	Not Connected	GND	XMC1-C12	XMC1-C13	GND	XMC1-F12	XMC1-F13
10	GND	XMC1-C14	XMC1-C15	GND	XMC1-F14	XMC1-F15	GND
11	Not Connected	GND	XMC1-C16	XMC1-C17	GND	XMC1-F16	XMC1-F17
12	GND	XMC1-C18	XMC1-C19	GND	XMC1-F18	XMC1-F19	GND
13	Not Connected	GND	XMC1-A1	XMC1-B1	GND	XMC1-D1	XMC1-E1
14	GND	XMC1-A3	XMC1-B3	GND	XMC1-D3	XMC1-E3	GND
15	Not Connected	GND	XMC1-A11	XMC1-B11	GND	XMC1-D11	XMC1-E11
16	GND	XMC1-A13	XMC1-B13	GND	XMC1-D13	XMC1-E13	GND

CHAMP-AV8 Signal XMC Module Signal Print Save to File... Show Basecard Signal Pairs Close Window

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SAVING THE PINOUT TABLE

3. To save a pinout table to a text file, click the **Save to File** button. The Pinout Configurator saves the table as a comma-delimited file, in which table cells are separated by commas. You can import this table into any software application that can convert this format into a table.

   In Word, highlight the table text, then select Table -> Convert Text to Table.

DEFINING NEW XMC MODULES

The Pinout Configurator lets you add pinout configurations for additional XMC modules not included with the utility. Follow these steps to define a new XMC module:

1. Click the **Define New XMC** button on the main window.

   The Custom XMC window appears.

2. Enter a name for the module.
3. Enter the signal name for each pin in the text box corresponding to that pin.
4. If you want to save the module for future use, click the **Save to File** button.
5. To use the new XMC module definition, click the **Add to XMC Lists** button. The new module is listed at the bottom of the drop-down list in the main window.

LOADING XMC MODULE DEFINITIONS

To load a previously saved XMC module definition file, follow these steps:

1. Click the **Load XMC Def'n** button on the Pinout Configurator main window.
2. Choose the text file containing the XMC module definition from the Open dialog box, then click **Open**.

To use the loaded XMC module definition, click the **Add to XMC Lists** button.

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BACKPLANE VPX CONNECTORS—DETAILED DESCRIPTION

The tables in this section show the mapping of CHAMP-AV8 signals to the VPX backplane connectors.

Cross Reference

VPX is the name given to the family of VITA 46 standards available from:

http://www.VITA.com/

For detailed information describing the mapping of the 7-row VPX board connectors to the 9 row VPX backplane connectors, refer to section 7.6 "Backplane Pin Mappings" in ANSI/VITA 46.0, VPX Baseline Standard, which is available for purchase from the above web site.

CHAMP-AV8 P0 UTILITY CONNECTOR PIN ASSIGNMENTS

The pinout tables are presented in the order of the rows when looking from the backplane, (that is, i, h, g, f, e, d, c, b, a). Figure A.8 shows the location of the contacts on the CHAMP-AV8 VITA 46 P0 Utility connector.

Figure A.8: CHAMP-AV8 P0 Utility Connector

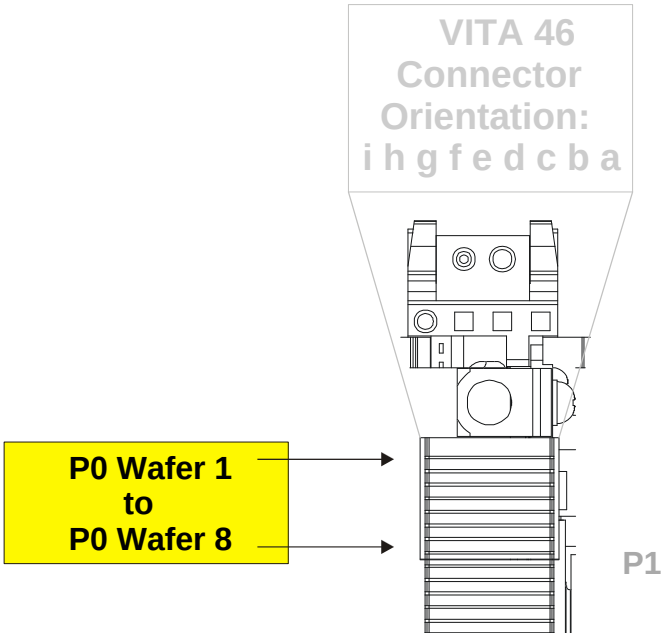


Table A.3 and Table A.4 on page A-15 describe the signals that are available on the P0 Utility connector on the CHAMP-AV8.

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Table A.3: P0 Utility Connector Pin Assignments

Wafer No.	Row G Signal	Row F Signal	Row E Signal	Row D Signal	Row C Signal	Row B Signal	Row A Signal
1	Vs1_BP12V	Vs1_BP12V	Vs1_BP12V	NC	Vs2_BP12V	Vs2_BP12V	Vs2_BP12V
2	Vs1_BP12V	Vs1_BP12V	Vs1_BP12V	NC	Vs2_BP12V	Vs2_BP12V	Vs2_BP12V
3	Vs3_NC_BP_5V	Vs3_NC_BP_5V	Vs3_NC_BP_5V	NC	Vs3_NC_BP_5V	Vs3_NC_BP_5V	Vs3_NC_BP_5V
4	SM2_BP_I2C1_SCL	SM3_BP_I2C1_DAT	GND	-12V_AUX	GND	SYSRST_L	NVMRO
5	GAP_L	GA4_L	GND	3.3V_AUX	GND	SM0_BP_I2C0_SCL	SM1_BP_I2C0_DAT
6	GA3_L	GA2_L	GND	+12V_AUX	GND	GA1_L	GA0_L
7	TCK	GND	TDO	TDI	GND	TMS	TRST_L
8	GND	REF_CLK_N	REF_CLK_P	GND	BP_AUX_CLK_N	BP_AUX_CLK_P	GND

Table A.4: P0 Utility Connector Signal Definitions

CHAMP-AV8 Signal	Description
Vs1_BP12V	+12V Power; 12V ± 5%, Max Nominal Ripple ≤ 240 mV, up to 24 A - Vs1
Vs2_BP12V	+12V Power; 12V ± 5%, Max Nominal Ripple ≤ 240 mV, up to 24 A - Vs2
Vs3_NC_BP_5V	No Connect - Vs3
3.3V_AUX	+3.3V Auxiliary Power; 3.3V±5%, Nominal Ripple ≤ 30 mV; 1 A max
+12V_AUX	+12V Power; 12V ± 5%, Nominal Ripple ≤ 50 mV; 1 A max
-12V_AUX	-12V Power; -12V ± 5%, Nominal Ripple ≤ 50 mV; 1 A max
GA4_L:GA0_L; GAP_L	Geographical Address Inputs 0-4 and Parity; Must pull-up to 3.3V on-board.
NVMRO	Non-Volatile Memory Read Only - Active high signal that prevents any non-volatile memory from being updated; pulled-up to 3.3VAUX on backplane; can only be driven low by backplane. **Note**: this signal does not write-enable the PABS (Permanent Alternate Boot Select) Flash memory.
REF_CLK_P REF_CLK_N	Differential bussed reference clock; 25 MHz ±100 ppm; 45% to 55% duty cycle; M-LVDS signaling; rise and fall time > 1 ns; driven by SYS_CON.
SYSRST_L	System Reset; pulled-up to 3.3VAUX on backplane; usually driven by SYSCON but can be driven by any board in the system.
TCLK, TDO, TDI, TMS, TRST_L	JTAG Signals; TCLK, TDO, and TDI are pulled-up to 3.3V on-board; TRST_L is pulled-down.
BP_AUX_CLK_P BP_AUX_CLK_N	Differential bussed reference clock; 1 Hz +50 ppm; minimum pulse width of 100 µs; LVDS signaling; rise and fall time ≥ 1 ns; driven by SYS_CON.
SM0_BP_I2C0_SCL, SM1_BP_I2C0_DAT	System management I^2C bus number 1.
SM2_BP_I2C1_SCL, SM3_BP_I2C1_DAT	System management I^2C bus number 2.
NC	No connect.
GND	Ground signals as defined in VITA 46.0.

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CORRESPONDING VPX BACKPLANE J0 UTILITY CONNECTOR PIN ASSIGNMENTS

Backplane J0 Pin assignments are shown below in Table A.5:

Table A.5: VPX Backplane J0 Pin Assignments

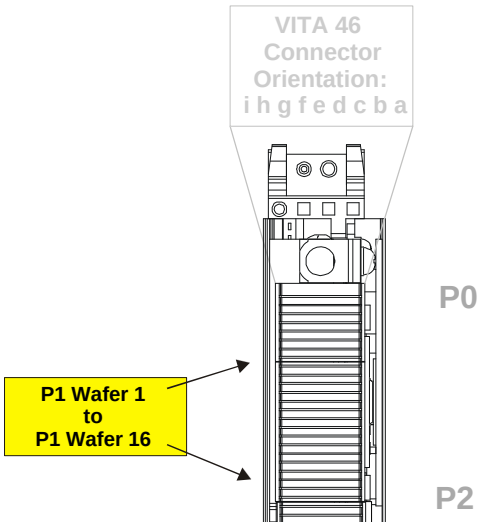
Pin	Row i Signal	Row h Signal	Row g Signal	Row f Signal	Row e Signal	Row d Signal	Row c Signal	Row b Signal	Row a Signal
1	Vs1_BP12V	Vs1_BP12V	Vs1_BP12V	Vs1_BP12V	N/C	Vs2_BP12V	Vs2_BP12V	Vs2_BP12V	Vs2_BP12V
2	Vs1_BP12V	Vs1_BP12V	Vs1_BP12V	Vs1_BP12V	N/C	Vs2_BP12V	Vs2_BP12V	Vs2_BP12V	Vs2_BP12V
3	Vs3_NC_BP_5V	Vs3_NC_BP_5V	Vs3_NC_BP_5V	Vs3_NC_BP_5V	N/C	Vs3_NC_BP_5V	Vs3_NC_BP_5V	Vs3_NC_BP_5V	Vs3_NC_BP_5V
4	GND	SM2_BP_I2C1_SCL	SM3_BP_I2C1_DAT	GND	-12V_AUX	GND	SYSRST_L	NVMRO	GND
5	GND	GAP_L	GA4_L	GND	3.3V_AUX	GND	SM0_BP_I2C0_SCL	SM1_BP_I2C0_DAT	GND
6	GND	GA3_L	GA2_L	GND	+12V_AUX	GND	GA1_L	GA0_L	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST_L
8	GND	REF_CLK_N	REF_CLK_P	GND	GND	BP_AUX_CLK_N	BP_AUX_CLK_P	GND	GND

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CHAMP-AV8 P1 (SRIO FABRIC) CONNECTOR PIN ASSIGNMENTS

The P1 connector is a 16 wafer VPX RT2 type connector shown in Figure A.9. The connector provides access to the Serial RapidIO (SRIO) fabric interfaces of the CHAMP-AV8. The pinout tables are presented in the order of the rows when looking from the backplane, (that is, i, h, g, f, e, d, c, b, a).

Figure A.9: CHAMP-AV8 P1 SRIO Fabric Connector



See Table A.6 for connector pin assignments and Table A.7 on page A-18 for signal definitions.

Table A.6: P1 SRIO Fabric Connector Pin Assignments

Wafer No.	Row G Signal	Row F Signal	Row E Signal	Row D Signal	Row C Signal	Row B Signal	Row A Signal
1	BP_GDISCRETE1	GND	PA_TX_N0	PA_TX_P0	GND	PA_RX_N0	PA_RX_P0
2	GND	PA_TX_N1	PA_TX_P1	GND	PA_RX_N1	PA_RX_P1	GND
3	VBAT	GND	PA_TX_N2	PA_TX_P2	GND	PA_RX_N2	PA_RX_P2
4	GND	PA_TX_N3	PA_TX_P3	GND	PA_RX_N3	PA_RX_P3	GND
5	SYS_CON_L	GND	PB_TX_N0	PB_TX_P0	GND	PB_RX_N0	PB_RX_P0
6	GND	PB_TX_N1	PB_TX_P1	GND	PB_RX_N1	PB_RX_P1	GND
7	NC_RFU	GND	PB_TX_N2	PB_TX_P2	GND	PB_RX_N2	PB_RX_P2
8	GND	PB_TX_N3	PB_TX_P3	GND	PB_RX_N3	PB_RX_P3	GND
9	CF_ALT_BOOT_L	GND	PC_TX_N0	PC_TX_P0	GND	PC_RX_N0	PC_RX_P0
10	GND	PC_TX_N1	PC_TX_P1	GND	PC_RX_N1	PC_RX_P1	GND
11	CARD_FAIL_L	GND	PC_TX_N2	PC_TX_P2	GND	PC_RX_N2	PC_RX_P2
12	GND	PC_TX_N3	PC_TX_P3	GND	PC_RX_N3	PC_RX_P3	GND
13	NC_IO_RSRV	GND	PD_TX_N0	PD_TX_P0	GND	PD_RX_N0	PD_RX_P0
14	GND	PD_TX_N1	PD_TX_P1	GND	PD_RX_N1	PD_RX_P1	GND
15	MASKABLE RESET_L	GND	PD_TX_N2	PD_TX_P2	GND	PD_RX_N2	PD_RX_P2
16	GND	PD_TX_N3	PD_TX_P3	GND	PD_RX_N3	PD_RX_P3	GND

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Table A.7: P1 SRIO Fabric Connector Signal Definitions

CHAMP-AV8 Signal	Description
PA_TX_P[0:3] PA_TX_N[0:3]	SRIO Port A Transmit Data Pairs - 4x-LP Transmit Pairs P1-DP**X**+/- (X =1,3,5,7)
PA_RX_P[0:3] PA_RX_N[0:3]	SRIO Port A Receive Data Pairs - 4x-LP Receive Pairs P1-DP**X**+/- (X =0,2,4,6)
PB_TX_P[0:3] PB_TX_N[0:3]	SRIO Port B Transmit Data Pairs - 4x-LP Transmit Pairs P1-DP**X**+/- (X =9,11,13,15)
PB_RX_P[0:3] PB_RX_N[0:3]	SRIO Port B Receive Data Pairs - 4x-LP Receive Pairs P1-DP**X**+/- (X =8,10,12,14)
PC_TX_P[0:3] PC_TX_N[0:3]	SRIO Port C Transmit Data Pairs - 4x-LP Transmit Pairs P1-DP**X**+/- (X =17,19,21,23)
PC_RX_P[0:3] PC_RX_N[0:3]	SRIO Port C Receive Data Pairs - 4x-LP Receive Pairs P1-DP**X**+/- (X =16,18,20,22)
PD_TX_P[0:3] PD_TX_N[0:3]	SRIO Port D Transmit Data Pairs - 4x-LP Transmit Pairs P1-DP**X**+/- (X =25,27,29,31)
PD_RX_P[0:3] PD_RX_N[0:3]	SRIO Port D Receive Data Pairs - 4x-LP Receive Pairs P1-DP**X**+/- (X =24,26,28,30)
CHAMP-AV8 Signal	**Description**
BP_GDISCRETE1	Used for MBSC Sync Signal.
SYS_CON_L	SYSCON_L - VITA 46.0 signal that indicates which slot is the system controller. Open collector driven by backplane; pull-up to 3.3V is implemented on board. When driven low by the backplane, the CHAMP-AV8 will become the source of the SYSRST_L and REF_CLK_P/N signals.
CF_ALT_BOOT_L	Alternate Boot Enable Input - Maps the boot chip select on all of the processors to the Permanent Alternate Boot Site (PABS) PROM; pull-up to 3.3V is implemented on board.
CARD_FAIL_L	Card Fail Output - Active low signal that indicates a card failure. This signal uses 3.3V LVCMOS signaling.
MASKABLE RESET_L	Pushbutton Reset input - Active low, open collector signal that initiates a board reset; pulled up to 3.3V on board. This signal is also available on the front panel J1 connector pin 19 (air-cooled variants).
VBAT	VITA 46.0 VBAT Power
GND	Ground signals as defined in VITA 46.0.
NC_RFU	Reserved IO Signal - Reserved by Curtiss-Wright
NC_IO_RSRV	Reserved IO Signal - Reserved by Curtiss-Wright

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CORRESPONDING VPX BACKPLANE J1 (SRIO FABRIC) CONNECTOR PIN ASSIGNMENTS

Backplane J1 pin assignments are shown below in Table A.8.

Table A.8: VPX Backplane J1 Pin Assignments

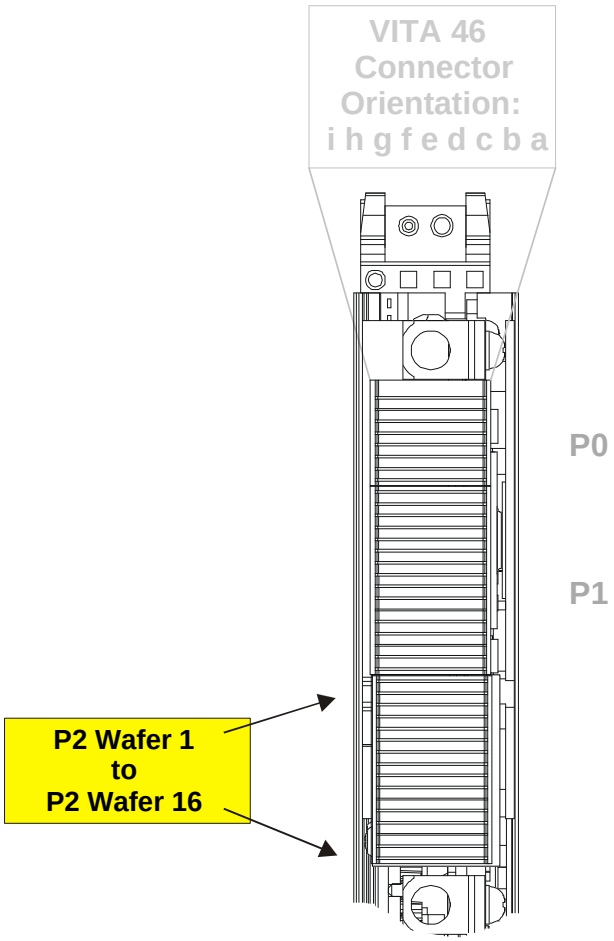
Pin	Row i Signal	Row h Signal	Row g Signal	Row f Signal	Row e Signal	Row d Signal	Row c Signal	Row b Signal	Row a Signal
1	BP_GDISCRETE1	GND	GND	PA_TX_N0	PA_TX_P0	GND	GND	PA_RX_N0	PA_RX_P0
2	GND	PA_TX_N1	PA_TX_P1	GND	GND	PA_RX_N1	PA_RX_P1	GND	GND
3	VBAT	GND	GND	PA_TX_N2	PA_TX_P2	GND	GND	PA_RX_N2	PA_RX_P2
4	GND	PA_TX_N3	PA_TX_P3	GND	GND	PA_RX_N3	PA_RX_P3	GND	GND
5	SYS_CON_L	GND	GND	PB_TX_N0	PB_TX_P0	GND	GND	PB_RX_N0	PB_RX_P0
6	GND	PB_TX_N1	PB_TX_P1	GND	GND	PB_RX_N1	PB_RX_P1	GND	GND
7	NC_RFU	GND	GND	PB_TX_N2	PB_TX_P2	GND	GND	PB_RX_N2	PB_RX_P2
8	GND	PB_TX_N3	PB_TX_P3	GND	GND	PB_RX_N3	PB_RX_P3	GND	GND
9	CF_ALT_BOOT_L	GND	GND	PC_TX_N0	PC_TX_P0	GND	GND	PC_RX_N0	PC_RX_P0
10	GND	PC_TX_N1	PC_TX_P1	GND	GND	PC_RX_N1	PC_RX_P1	GND	GND
11	CARD_FAIL_L	GND	GND	PC_TX_N2	PC_TX_P2	GND	GND	PC_RX_N2	PC_RX_P2
12	GND	PC_TX_N3	PC_TX_P3	GND	GND	PC_RX_N3	PC_RX_P3	GND	GND
13	NC_IO_RSRV	GND	GND	PD_TX_N0	PD_TX_P0	GND	GND	PD_RX_N0	PD_RX_P0
14	GND	PD_TX_N1	PD_TX_P1	GND	GND	PD_RX_N1	PD_RX_P1	GND	GND
15	MASKABLERESET_L	GND	GND	PD_TX_N2	PD_TX_P2	GND	GND	PD_RX_N2	PD_RX_P2
16	GND	PD_TX_N3	PD_TX_P3	GND	GND	PD_RX_N3	PD_RX_P3	GND	GND

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CHAMP-AV8 P2 (PCIE EXPANSION) CONNECTOR PIN ASSIGNMENTS

The P2 connector is a 16 wafer VPX RT2 type connector shown in Figure A.10. The connector provides two (2) four-lane (x4) PCIe ports on the CHAMP-AV8. The pinout tables are presented in the order of the rows when looking from the backplane, (that is, i, h, g, f, e, d, c, b, a).

Figure A.10: CHAMP-AV8 VITA 46 P2 Connector



See Table A.9 on page A-21 for connector pin assignments and Table A.10 on page A-21 for signal definitions.

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Table A.9: P2 PCIe Expansion Plane Connector Pin Assignments

Wafer No.	Row G Signal	Row F Signal	Row E Signal	Row D Signal	Row C Signal	Row B Signal	Row A Signal
1	NC	GND	EP_00_PCIE_TX_N	EP_00_PCIE_TX_P	GND	EP_00_PCIE_RX_N	EP_00_PCIE_RX_P
2	GND	EP_01_PCIE_TX_N	EP_01_PCIE_TX_P	GND	EP_01_PCIE_RX_N	EP_01_PCIE_RX_P	GND
3	NC	GND	EP_02_PCIE_TX_N	EP_02_PCIE_TX _P	GND	EP_02_PCIE_RX_N	EP_02_PCIE_RX_P
4	GND	EP_03_PCIE_TX_N	EP_03_PCIE_TX_P	GND	EP_03_PCIE_RX_N	EP_03_PCIE_RX_P	GND
5	NC	GND	EP_04_PCIE_TX_N	EP_04_PCIE_TX_P	GND	EP_04_PCIE_RX_N	EP_04_PCIE_RX_P
6	GND	EP_05_PCIE_TX_N	EP_05_PCIE_TX_P	GND	EP_05_PCIE_RX_N	EP_05_PCIE_RX_P	GND
7	NC	GND	EP_06_PCIE_TX_N	EP_06_PCIE_TX_P	GND	EP_06_PCIE_RX_N	EP_06_PCIE_RX_P
8	GND	EP_07_PCIE_TX_N	EP_07_PCIE_TX_P	GND	EP_07_PCIE_RX_N	EP_07_PCIE_RX_P	GND
9	NC	GND	EP_08_PCIE_TX_N	EP_08_PCIE_TX_P	GND	EP_08_PCIE_RX_N	EP_08_PCIE_RX_P
10	GND	EP_09_PCIE_TX_N	EP_09_PCIE_TX_P	GND	EP_09_PCIE_RX_N	EP_09_PCIE_RX_P	GND
11	NC	GND	EP_10_PCIE_TX_N	EP_10_PCIE_TX_P	GND	EP_10_PCIE_RX_N	EP_10_PCIE_RX_P
12	GND	EP_11_PCIE_TX_N	EP_11_PCIE_TX_P	GND	EP_11_PCIE_RX_N	EP_11_PCIE_RX_P	GND
13	NC	GND	EP_12_PCIE_TX_N	EP_12_PCIE_TX_P	GND	EP_12_PCIE_RX_N	EP_12_PCIE_RX_P
14	GND	EP_13_PCIE_TX_N	EP_13_PCIE_TX_P	GND	EP_13_PCIE_RX_N	EP_13_PCIE_RX_P	GND
15	NC	GND	EP_14_PCIE_TX_N	EP_14_PCIE_TX_P	GND	EP_14_PCIE_RX_N	EP_14_PCIE_RX_P
16	GND	EP_15_PCIE_TX_N	EP_15_PCIE_TX_P	GND	EP_15_PCIE_RX_N	EP_15_PCIE_RX_P	GND

Table A.10: P2 PCIe Expansion Plane Connector Signal Definitions

CHAMP-AV8 Signal	Description
EP_X_PCIE_RX_P EP_X_PCIE_RX_N (X =0,1,2,3)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 0,2,4,6)
EP_X_PCIE_TX_P EP_X_PCIE_TX_N (X =0,1,2,3)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 1,3,5,7)
EP_X_PCIE_RX_P EP_X_PCIE_RX_N (X =4,5,6,7)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 8,10,12,14)
EP_X_PCIE_TX_P EP_X_PCIE_TX_N (X =4,5,6,7)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 9,11,13,15)
EP_X_PCIE_RX_P EP_X_PCIE_RX_N (X=8,9,10,11)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 16,18,20,22)
EP_X_PCIE_TX_P EP_X_PCIE_TX_N (X=8,9,10,11)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 17,19,21,23)
EP_X_PCIE_RX_P EP_X_PCIE_RX_N (X=12,13,14,15)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 24,26,28,30)
EP_X_PCIE_TX_P EP_X_PCIE_TX_N (X=12,13,14,15)	VITA65 Expansion Plane PCI express lanes P2-DP**X**+/- (**X** = 25,27,29,31)
NC	No Connect
GND	Ground signals as defined in VITA 46.0.

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CORRESPONDING VPX BACKPLANE J2 (PCIE EXPANSION) CONNECTOR PIN ASSIGNMENTS

Backplane J2 pin assignments are as shown below in Table A.11.

Table A.11: VPX Backplane J2 Pin Assignments

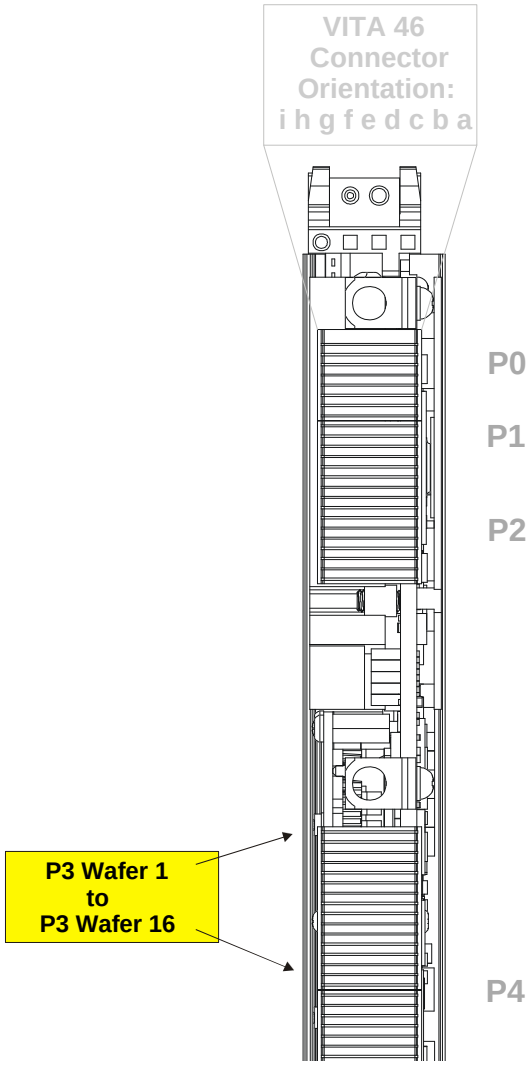
Pin	Row i Signal	Row h Signal	Row g Signal	Row f Signal	Row e Signal	Row d Signal	Row c Signal	Row b Signal	Row a Signal
1	NC	GND	GND	EP_00_PCIE_TX_N	EP_00_PCIE_TX_P	GND	GND	EP_00_PCIE_RX_N	EP_00_PCIE_RX_P
2	GND	EP_01_PCIE_TX_N	EP_01_PCIE_TX_P	GND	GND	EP_01_PCIE_RX_N	EP_01_PCIE_RX_P	GND	GND
3	NC	GND	GND	EP_02_PCIE_TX_N	EP_02_PCIE_TX _P	GND	GND	EP_02_PCIE_RX_N	EP_02_PCIE_RX_P
4	GND	EP_03_PCIE_TX_N	EP_03_PCIE_TX_P	GND	GND	EP_03_PCIE_RX_N	EP_03_PCIE_RX_P	GND	GND
5	NC	GND	GND	EP_04_PCIE_TX_N	EP_04_PCIE_TX_P	GND	GND	EP_04_PCIE_RX_N	EP_04_PCIE_RX_P
6	GND	EP_05_PCIE_TX_N	EP_05_PCIE_TX_P	GND	GND	EP_05_PCIE_RX_N	EP_05_PCIE_RX_P	GND	GND
7	NC	GND	GND	EP_06_PCIE_TX_N	EP_06_PCIE_TX_P	GND	GND	EP_06_PCIE_RX_N	EP_06_PCIE_RX_P
8	GND	EP_07_PCIE_TX_N	EP_07_PCIE_TX_P	GND	GND	EP_07_PCIE_RX_N	EP_07_PCIE_RX_P	GND	GND
9	NC	GND	GND	EP_08_PCIE_TX_N	EP_08_PCIE_TX_P	GND	GND	EP_08_PCIE_RX_N	EP_08_PCIE_RX_P
10	GND	EP_09_PCIE_TX_N	EP_09_PCIE_TX_P	GND	GND	EP_09_PCIE_RX_N	EP_09_PCIE_RX_P	GND	GND
11	NC	GND	GND	EP_10_PCIE_TX_N	EP_10_PCIE_TX_P	GND	GND	EP_10_PCIE_RX_N	EP_10_PCIE_RX_P
12	GND	EP_11_PCIE_TX_N	EP_11_PCIE_TX_P	GND	GND	EP_11_PCIE_RX_N	EP_11_PCIE_RX_P	GND	GND
13	NC	GND	GND	EP_12_PCIE_TX_N	EP_12_PCIE_TX_P	GND	GND	EP_12_PCIE_RX_N	EP_12_PCIE_RX_P
14	GND	EP_13_PCIE_TX_N	EP_13_PCIE_TX_P	GND	GND	EP_13_PCIE_RX_N	EP_13_PCIE_RX_P	GND	GND
15	NC	GND	GND	EP_14_PCIE_TX_N	EP_14_PCIE_TX_P	GND	GND	EP_14_PCIE_RX_N	EP_14_PCIE_RX_P
16	GND	EP_15_PCIE_TX_N	EP_15_PCIE_TX_P	GND	GND	EP_15_PCIE_RX_N	EP_15_PCIE_RX_P	GND	GND

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CHAMP-AV8 P3 (XMC SITE'S PMC USER I/O) CONNECTOR PIN ASSIGNMENTS

The P3 connector is a 16 wafer VPX RT2 type connector shown in Figure A.11. The connector provides access to the differential PMC User I/O on the XMC site's J14 connector. The pinout tables are presented in the order of the rows when looking from the backplane, (that is, i, h, g, f, e, d, c, b, a).

Figure A.11: P3 XMC Site's PMC User I/O Connector



See Table A.12 on page A-24 for the connector pin assignments and Table A.12 on page A-24 for signal definitions.

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Table A.12: P3 XMC Site's PMC User I/O Connector Pin Assignments

Wafer No.	Row G Signal	Row F Signal	Row E Signal	Row D Signal	Row C Signal	Row B Signal	Row A Signal
1	NC	GND	PMC_01	PMC_03	GND	PMC_02	PMC_04
2	GND	PMC_05	PMC_07	GND	PMC_06	PMC_08	GND
3	NC	GND	PMC_09	PMC_11	GND	PMC_10	PMC_12
4	GND	PMC_13	PMC_15	GND	PMC_14	PMC_16	GND
5	NC	GND	PMC_17	PMC_19	GND	PMC_18	PMC_20
6	GND	PMC_21	PMC_23	GND	PMC_22	PMC_24	GND
7	NC	GND	PMC_25	PMC_27	GND	PMC_26	PMC_28
8	GND	PMC_29	PMC_31	GND	PMC_30	PMC_32	GND
9	NC	GND	PMC_33	PMC_35	GND	PMC_34	PMC_36
10	GND	PMC_37	PMC_39	GND	PMC_38	PMC_40	GND
11	NC	GND	PMC_41	PMC_43	GND	PMC_42	PMC_44
12	GND	PMC_45	PMC_47	GND	PMC_46	PMC_48	GND
13	NC	GND	PMC_49	PMC_51	GND	PMC_50	PMC_52
14	GND	PMC_53	PMC_55	GND	PMC_54	PMC_56	GND
15	NC	GND	PMC_57	PMC_59	GND	PMC_58	PMC_60
16	GND	PMC_61	PMC_63	GND	PMC_62	PMC_64	GND

Table A.13: P3 XMC Site's PMC User I/O Connector Signal Definitions

CHAMP-AV8 Signal	Description
PMC_[64:01]	PMC/XMC Site's Differential User I/O Mapping from CHAMP-AV8 J14 connector mapped in accordance with the P64s pattern defined in VITA 46.9d0.25. The adjacent signals in a column (e.g. PMC_01 and PMC_03) are routed differentially. The electrical characteristics of the PMC I/O will depend on the PMC used. Please consult the PMC user's manual for more information.
NC	No Connect
GND	Ground signals as defined in VITA 46.0

Routing Rules for P64s Signals

- shall be routed as point-to-point differential pairs
- shall have differential impedance of ~100 Ohms
- shall have single ended impedance of ~60 Ohms
- length matching within a pair: Signal-to-Signal ≤ 25 mils
- length matching across all pairs: Signal-to-Signal ≤ 200 mils

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CORRESPONDING VPX BACKPLANE J3 (XMC SITE'S PMC USER I/O) CONNECTOR PIN ASSIGNMENTS

CHAMP-AV8 to backplane J3 pin assignments are shown below in Table A.14.

Table A.14: VPX Backplane J3 Pin Assignments

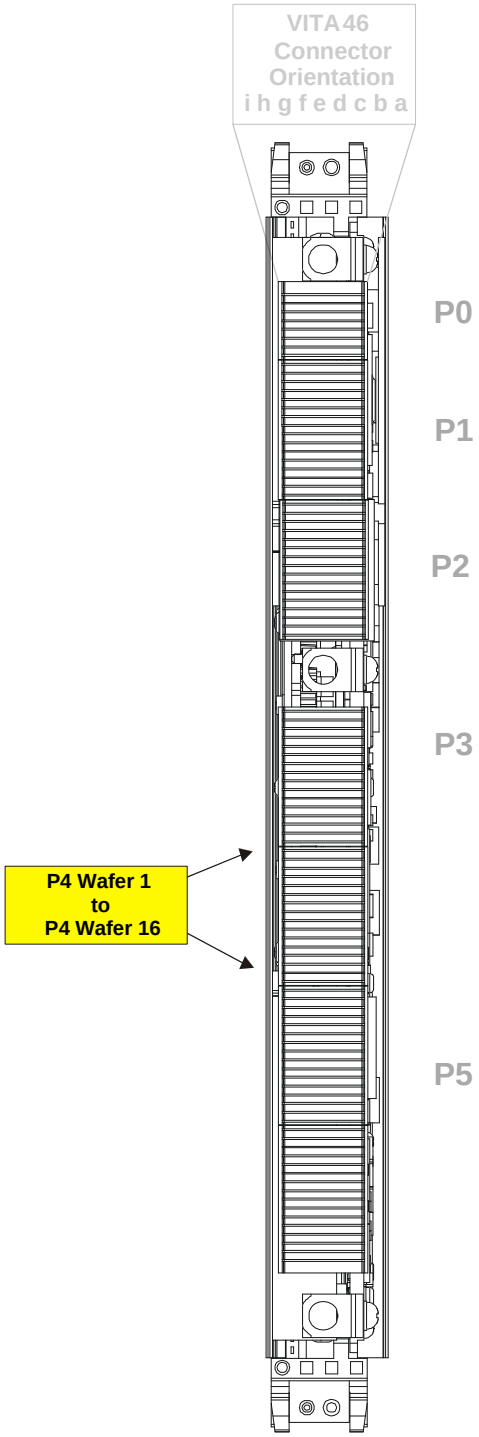
Pin	Row i Signal	Row h Signal	Row g Signal	Row f Signal	Row e Signal	Row d Signal	Row c Signal	Row b Signal	Row a Signal
1	NC	GND	GND	PMC_01	PMC_03	GND	GND	PMC_02	PMC_04
2	GND	PMC_05	PMC_07	GND	GND	PMC_06	PMC_08	GND	GND
3	NC	GND	GND	PMC_09	PMC_11	GND	GND	PMC_10	PMC_12
4	GND	PMC_13	PMC_15	GND	GND	PMC_14	PMC_16	GND	GND
5	NC	GND	GND	PMC_17	PMC_19	GND	GND	PMC_18	PMC_20
6	GND	PMC_21	PMC_23	GND	GND	PMC_22	PMC_24	GND	GND
7	NC	GND	GND	PMC_25	PMC_27	GND	GND	PMC_26	PMC_28
8	GND	PMC_29	PMC_31	GND	GND	PMC_30	PMC_32	GND	GND
9	NC	GND	GND	PMC_33	PMC_35	GND	GND	PMC_34	PMC_36
10	GND	PMC_37	PMC_39	GND	GND	PMC_38	PMC_40	GND	GND
11	NC	GND	GND	PMC_41	PMC_43	GND	GND	PMC_42	PMC_44
12	GND	PMC_45	PMC_47	GND	GND	PMC_46	PMC_48	GND	GND
13	NC	GND	GND	PMC_49	PMC_51	GND	GND	PMC_50	PMC_52
14	GND	PMC_53	PMC_55	GND	GND	PMC_54	PMC_56	GND	GND
15	NC	GND	GND	PMC_57	PMC_59	GND	GND	PMC_58	PMC_60
16	GND	PMC_61	PMC_63	GND	GND	PMC_62	PMC_64	GND	GND

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CHAMP-AV8 P4 (BASECARD I/O) CONNECTOR PIN ASSIGNMENTS

The P4 connector is a 16 wafer VPX RT2 type connector shown in Figure A.12. The connector provides access to the basecard I/O of the CHAMP-AV8. The pinout tables are presented in the order of the rows when looking from the backplane, (that is, g, f, e, d, c, b, a).

Figure A.12: P4 Basecard I/O Connector



See Table A.15 on page A-27 for the connector pin assignments and Table A.16 on page A-27 for signal definitions.

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Table A.15: P4 Basecard I/O Connector Pin Assignments

Wafer No.	Row G Signal	Row F Signal	Row E Signal	Row D Signal	Row C Signal	Row B Signal	Row A Signal
1	BP_PABS_A_CS0_L	GND	JTSEL_L	JPROC2	GND	JPROC1	JPROC0
2	GND	IPMI_SERIAL_OUT	PMBUS_SDA	GND	PMI_TDI	PMI_TDO	GND
3	BP_PABS_A_CLK	GND	PMBUS_SCL	JPROC3	GND	PMI_TCK	PMI_TMS
4	GND	IPMI_SERIAL_IN	CF_NAND_WR_DIS_L	GND	BP_PORT80_EN_L	PMI_JTSEL_L	GND
5	BP_PABS_A_SO	GND	CF_FLASH_WR_DIS_L	CF_NVRAM_WR_DIS_L	GND	CF_PABS_WR_EN_L	CF_PROM_WR_EN_L
6	GND	CF_SOFT_JUMP_L_1	CF_SOFT_JUMP_L_0	GND	CF_WD_DIS_L	RS232_A0_RX	GND
7	BP_PABS_A_SI	GND	RS422_RXA2_N	RS422_RXA2_P	GND	RS422_TXA2_N	RS422_TXA2_P
8	GND	RS422_RXB2_N	RS422_RXB2_P	GND	RS422_TXB2_N	RS422_TXB2_P	GND
9	BP_PABS_B_CS0_L	GND	RS232_A1_TX	RS232_A1_RX	GND	RS232_A0_TX	PMI_TRST_L
10	GND	RS232_B0_TX	RS232_B0_RX	GND	RS232_B1_TX	RS232_B1_RX	GND
11	BP_PABS_B_CLK	GND	UTP_B_TX_N	UTP_B_TX_P	GND	UTP_B_RX_N	UTP_B_RX_P
12	GND	UTP_A_TX_N	UTP_A_TX_P	GND	UTP_A_RX_N	UTP_A_RX_P	GND
13	BP_PABS_B_S0	GND	ETH_A_TRX1_N	ETH_A_TRX1_P	GND	ETH_A_TRX0_N	ETH_A_TRX0_P
14	GND	ETH_A_TRX3_N	ETH_A_TRX3_P	GND	ETH_A_TRX2_N	ETH_A_TRX2_P	GND
15	BP_PABS_B_SI	GND	ETH_B_TRX1_N	ETH_B_TRX1_P	GND	ETH_B_TRX0_N	ETH_B_TRX0_P
16	GND	ETH_B_TRX3_N	ETH_B_TRX3_P	GND	ETH_B_TRX2_N	ETH_B_TRX2_P	GND

Table A.16: P4 Basecard I/O Connector Signal Definitions

CHAMP-AV8 Signal	Description
JTSEL_L	JTAG Select Signal; pulled up to 3.3V on-board.
JPROC[3:0]	Select JTAG Mode; pulled up to 3.3V on-board.
PMI_TCK,PMI_TDO, PMI_TDI, PMI_TMS, PMI_TRST_L	Reserved for Curtiss-Wright use.
PMI_JTSEL_L	Reserved for Curtiss-Wright use.
PMBUS_SDA, PMBUS_SCL	I^2C interface to power regulators only.
IPMI_SERIAL_OUT, IPMI_SERIAL_IN	Reserved for Curtiss-Wright use. IPMI FPGA debug - LVTTL UART interface. No Connect on production units
CF_NVRAM_WR_DIS_L	NVRAM Write Disable
CF_FLASH_WR_DIS_L	Flash Write Disable
CF_PABS_WR_EN_L	PABs Write Enable
CF_NAND_WR_DIS_L	NAND Flash Write Disable
CF_PROM_WR_EN_L	PROM Write Enable

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Table A.16: P4 Basecard I/O Connector Signal Definitions (Continued)

CHAMP-AV8 Signal	Description
CF_SOFT_JMP_L[1:0]	Software Jumpers
CF_WD_DIS_L	Watchdog Disable - Disables watchdog reset (Active low).
RS422_A2_TX_P/N RS422_A2_RX_P/N RS422_B2_TX_P/N RS422_B2_RX_P/N	RS-422/485 or RS232 Ports 3 and 4. NOTE: RS422_TX3_P may be used as RS232_TX3, RS422_RX3_P may be used as RS232_RX3, RS422_TX4_P may be used as RS232_TX4, RS422_RX4_P may be used as RS232_RX4.
RS232_A0_TX RS232_A1_TX RS232_B0_TX RS232_B1_TX RS232_A0_RX RS232_A1_RX RS232_B0_RX RS232_B1_RX	Four base card RS232 (EIA-232) Ports.
ETHA_TRX[0]_P/N ETHA_TRX[1]_P/N ETHA_TRX[2]_P/N ETHA_TRX[3]_P/N ETHB_TRX[0]_P/N ETHB_TRX[1]_P/N ETHB_TRX[2]_P/N ETHB_TRX[3]_P/N	1000Base-T, Nodes A and B: GigE signals selected via build option between front panel J1 connector and backplane P4 connector. GigE signals are not present on these pins when configured for front panel connection. Mapped in accordance with VITA 65 specification.
UTPA_TX_P/N UTPA_RX_P/N UTPB_TX_P/N UTPB_RX_P/N	1000Base-BX, Nodes A and B: Signals that are always present on the P4 connector. Mapped in accordance with VITA 65 specification.
BP_PORT80_EN_L	PORT80 Enable – Reserved for Curtiss-Wright use
BP_PABS_[A/B]_CS0_L BP_PABS_[A/B]_CLK BP_PABS_[A/B]_S0 BP_PABS_[A/B]_SI	PABS interface– Reserved for Curtiss-Wright use

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CORRESPONDING VPX BACKPLANE J4 (BASECARD I/O) CONNECTOR PIN ASSIGNMENTS

CHAMP-AV8 to backplane J4 pin assignments are shown below in Table A.17.

Table A.17: VPX Backplane J4 Pin Assignments

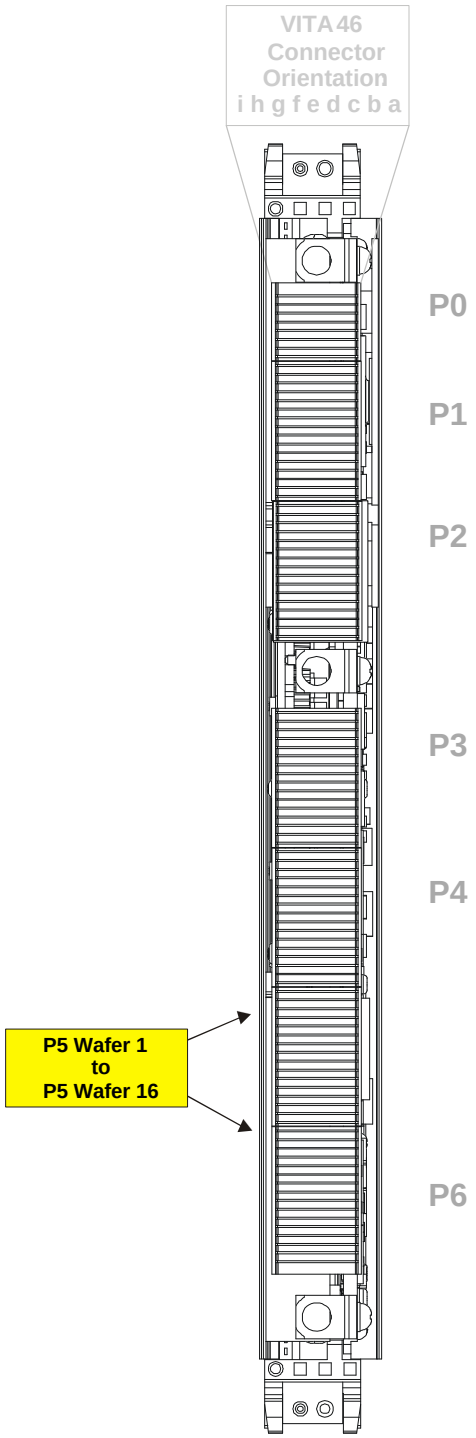
Pin	Row i Signal	Row h Signal	Row g Signal	Row f Signal	Row e Signal	Row d Signal	Row c Signal	Row b Signal	Row a Signal
1	BP_PABS_A_CS0_L	GND	GND	JTSEL_L	JPROC2	GND	GND	JPROC1	JPROC0
2	GND	IPMI_SERIAL_OUT	PMBUS_SDA	GND	GND	PMI_TDI	PMI_TDO	GND	GND
3	BP_PABS_A_CLK	GND	GND	PMBUS_SCL	JPROC3	GND	GND	PMI_TCK	PMI_TMS
4	GND	IPMI_SERIAL_IN	CF_NAND_WR_DIS_L	GND	GND	BP_PORT80_EN_L	PMI_JTSEL_L	GND	GND
5	BP_PABS_A_SO	GND	GND	CF_FLASH_WR_DIS_L	CF_NVRAM_WR_DIS_L	GND	GND	CF_PABS_WR_EN_L	CF_PROM_WR_EN_L
6	GND	CF_SOFT_JUMP_L_1	CF_SOFT_JUMP_L_0	GND	GND	CF_WD_DIS_L	RS232_A0_RX	GND	GND
7	BP_PABS_A_SI	GND	GND	RS422_RXA2_N	RS422_RXA2_P	GND	GND	RS422_TXA2_N	RS422_TXA2_P
8	GND	RS422_RXB2_N	RS422_RXB2_P	GND	GND	RS422_TXB2_N	RS422_TXB2_P	GND	GND
9	BP_PABS_B_CS0_L	GND	GND	RS232_A1_TX	RS232_A1_RX	GND	GND	RS232_A0_TX	PMI_TRST_L
10	GND	RS232_B0_TX	RS232_B0_RX	GND	GND	RS232_B1_TX	RS232_B1_RX	GND	GND
11	BP_PABS_B_CLK	GND	GND	UTP_B_TX_N	UTP_B_TX_P	GND	GND	UTP_B_RX_N	UTP_B_RX_P
12	GND	UTP_A_TX_N	UTP_A_TX_P	GND	GND	UTP_A_RX_N	UTP_A_RX_P	GND	GND
13	BP_PABS_B_SO	GND	GND	ETH_A_TRX1_N	ETH_A_TRX1_P	GND	GND	ETH_A_TRX0_N	ETH_A_TRX0_P
14	GND	ETH_A_TRX3_N	ETH_A_TRX3_P	GND	GND	ETH_A_TRX2_N	ETH_A_TRX2_P	GND	GND
15	BP_PABS_B_SI	GND	GND	ETH_B_TRX1_N	ETH_B_TRX1_P	GND	GND	ETH_B_TRX0_N	ETH_B_TRX0_P
16	GND	ETH_B_TRX3_N	ETH_B_TRX3_P	GND	GND	ETH_B_TRX2_N	ETH_B_TRX2_P	GND	GND

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CHAMP-AV8 P5 (XMC USER I/O) CONNECTOR PIN ASSIGNMENTS

The P5 connector is a 16 wafer VPX RT2 type connector shown in Figure A.13. The connector provides access to the XMC User I/O of the CHAMP-AV8. The pinout tables are presented in the order of the rows when looking from the backplane, (that is, i, h, g, f, e, d, c, b, a).

Figure A.13: P5 XMC User I/O Connector



See Table A.18 on page A-31 for connector pin assignments and Table A.19 on page A-31 for signal definitions.

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Table A.18: P5 XMC User I/O Connector Pin Assignments

Wafer No.	Row G Signal	Row F Signal	Row E Signal	Row D Signal	Row C Signal	Row B Signal	Row A Signal
1	NC	GND	NC	NC	GND	NC	NC
2	GND	NC	NC	GND	NC	NC	GND
3	NC	GND	NC	NC	GND	XMC_C01	XMC_F01
4	GND	XMC_C02	XMC_C03	GND	XMC_F02	XMC_F03	GND
5	NC	GND	XMC_C04	XMC_C05	GND	XMC_F04	XMC_F05
6	GND	XMC_C06	XMC_C07	GND	XMC_F06	XMC_F07	GND
7	NC	GND	XMC_C08	XMC_C09	GND	XMC_F08	XMC_F09
8	GND	XMC_C10	XMC_C11	GND	XMC_F10	XMC_F11	GND
9	NC	GND	XMC_C12	XMC_C13	GND	XMC_F12	XMC_F13
10	GND	XMC_C14	XMC_C15	GND	XMC_F14	XMC_F15	GND
11	NC	GND	XMC_C16	XMC_C17	GND	XMC_F16	XMC_F17
12	GND	XMC_C18	XMC_C19	GND	XMC_F18	XMC_F19	GND
13	NC	GND	XMC_A1	XMC_B1	GND	XMC_D1	XMC_E1
14	GND	XMC_A3	XMC_B3	GND	XMC_D3	XMC_E3	GND
15	NC	GND	XMC_A11	XMC_B11	GND	XMC_D11	XMC_E11
16	GND	XMC_A13	XMC_B13	GND	XMC_D13	XMC_E13	GND

Table A.19: P5 XMC User I/O Connector Signal Definitions

CHAMP-AV8 Signal	Description
XMC_C[19:01] XMC_F[19:01]	XMC Single-Ended User I/O Mapping from XMC J16 connector (38 single ended signals). These connection supports high-speed single-ended signals.
XMC_DP[3:0]_P XMC_DP[3:0]_N XMC_DP[13:10]_P XMC_DP[13:10]_N	XMC Differential User I/O Mapping from XMC J16 connector to V46 P5 connector (8 pairs). Mapped in accordance with V46.9, P5w3P6-X38s+X8d+X12d pattern.
NC	No Connect
GND	Ground signals as defined in VITA 46.0.



Note

Electrical characteristics of XMC signals are determined by the XMC module used. Please consult the XMC module User's Manual for exact details.

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CORRESPONDING VPX BACKPLANE J5 (XMC USER I/O) CONNECTOR PIN ASSIGNMENTS

CHAMP-AV8 to backplane J5 pin assignments are shown below in Table A.20.

Table A.20: VPX Backplane J5 Pin Assignments

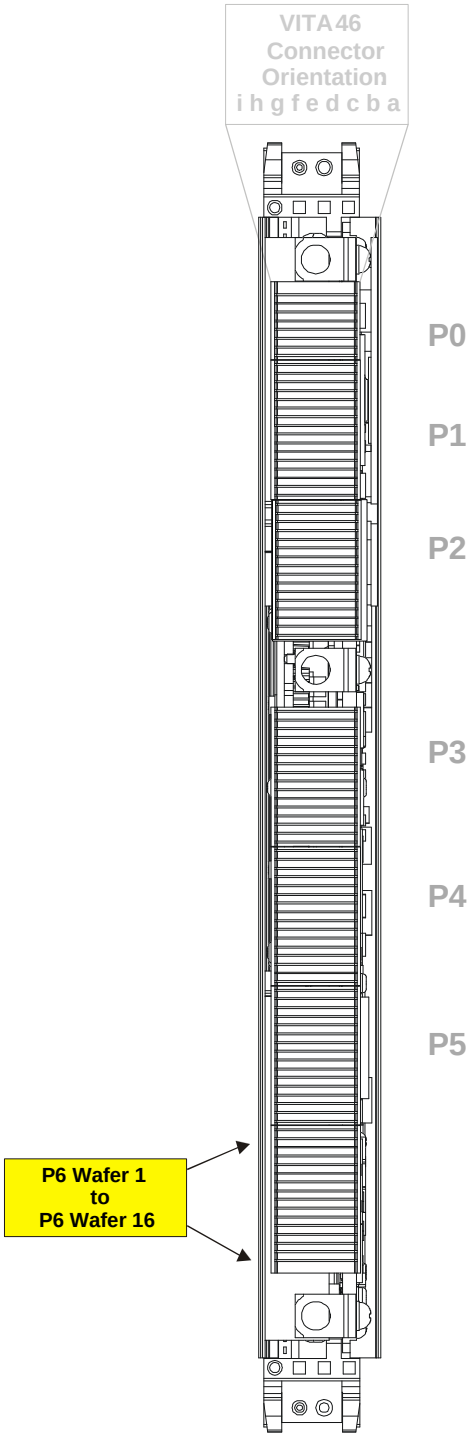
Pin	Row i Signal	Row h Signal	Row g Signal	Row f Signal	Row e Signal	Row d Signal	Row c Signal	Row b Signal	Row a Signal
1	NC	GND	GND	NC	NC	GND	GND	NC	NC
2	GND	NC	NC	GND	GND	NC	NC	GND	GND
3	NC	GND	GND	NC	NC	GND	GND	XMC_C01	XMC_F01
4	GND	XMC_C02	XMC_C03	GND	GND	XMC_F02	XMC_F03	GND	GND
5	NC	GND	GND	XMC_C04	XMC_C05	GND	GND	XMC_F04	XMC_F05
6	GND	XMC_C06	XMC_C07	GND	GND	XMC_F06	XMC_F07	GND	GND
7	NC	GND	GND	XMC_C08	XMC_C09	GND	GND	XMC_F08	XMC_F09
8	GND	XMC_C10	XMC_C11	GND	GND	XMC_F10	XMC_F11	GND	GND
9	NC	GND	GND	XMC_C12	XMC_C13	GND	GND	XMC_F12	XMC_F13
10	GND	XMC_C14	XMC_C15	GND	GND	XMC_F14	XMC_F15	GND	GND
11	NC	GND	GND	XMC_C16	XMC_C17	GND	GND	XMC_F16	XMC_F17
12	GND	XMC_C18	XMC_C19	GND	GND	XMC_F18	XMC_F19	GND	GND
13	NC	GND	GND	XMC_A1	XMC_B1	GND	GND	XMC_D1	XMC_E1
14	GND	XMC_A3	XMC_B3	GND	GND	XMC_D3	XMC_E3	GND	GND
15	NC	GND	GND	XMC_A11	XMC_B11	GND	GND	XMC_D11	XMC_E11
16	GND	XMC_A13	XMC_B13	GND	GND	XMC_D13	XMC_E13	GND	GND

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CHAMP-AV8 P6 (XMC/DIO/SATA/USB) CONNECTOR PIN ASSIGNMENTS

The P6 connector is a 16 wafer VPX RT2 type connector shown in Figure A.14. The connector provides access to the XMC/DIO/SATA/USB User I/O of the CHAMP-AV8. The pinout tables are presented in the order of the rows when looking from the backplane, (that is, i, h, g, f, e, d, c, b, a).

Figure A.14: P6 XMC/DIO/PCIe Connector



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See Table A.21 below for connector pin assignments and Table A.22 for signal definitions.

Table A.21: P6 XMC/DIO/SATA/USB Connector Pin Assignments

Wafer No.	Row G Signal	Row F Signal	Row E Signal	Row D Signal	Row C Signal	Row B Signal	Row A Signal
1	DIO0	GND	XMC_A5	XMC_B5	GND	XMC_D5	XMC_E5
2	GND	XMC_A7	XMC_B7	GND	XMC_D7	XMC_E7	GND
3	DIO1	GND	XMC_A9	XMC_B9	GND	XMC_D9	XMC_E9
4	GND	XMC_A15	XMC_B15	GND	XMC_D15	XMC_E15	GND
5	DIO2	GND	XMC_A17	XMC_B17	GND	XMC_D17	XMC_E17
6	GND	XMC_A19	XMC_B19	GND	XMC_D19	XMC_E19	GND
7	DIO3	GND	NC	NC	GND	NC	NC
8	GND	SATA_A_TXN1	SATA_A_TXP1	GND	SATA_A_RXN1	SATA_A_RXP1	GND
9	DIO4	GND	SATA_B_TXN1	SATA_B_TXP1	GND	SATA_B_RXN1	SATA_B_RXP1
10	GND	NC	NC	GND	NC	NC	GND
11	DIO5	GND	NC	NC	GND	NC	NC
12	GND	USB_A0_N	USB_A0_P	GND	USB_B0_N	USB_B0_P	GND
13	DIO6	GND	USB_A0_ POWER	NC	GND	USB_B0_ POWER	NC
14	GND	NC	NC	GND	NC	NC	GND
15	DIO7	GND	DIO8	DIO9	GND	DIO10	DIO11
16	GND	DIO12	DIO13	GND	DIO14	DIO15	GND

Table A.22: P6 XMC/DIO/SATA/USB Connector Signal Definitions

CHAMP-AV8 Signal	Description
XMC_DP[9:4]_P/N XMC_DP[19:14]_P/N	XMC Differential User I/O Mapping from XMC J16 connector to V46 P5 connector (12 pairs). Mapped in accordance with V46.9, P5w3P6-X38s+X8d+X12d pattern.
DIO[7:0]	DIO Signals - Single ended.
DIO[15:8]	DIO Signals - Single ended (could be used as differential in future).
SATA_[A:B]_TX_P1/N1 SATA_[A:B]_RX_P1/N1	SATA links
USB_[A:B]0_P/N USB_[A:B]0_PWR	USB ports
GND	Ground signals as defined in VITA 46.0.

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CORRESPONDING VPX BACKPLANE J6 (XMC/DIO/SATA/USB) CONNECTOR PIN ASSIGNMENTS

CHAMP-AV8 to backplane J6 pin assignments are shown below in Table A.23.

Table A.23: VPX Backplane J6 Pin Assignments

Pin	Row i Signal	Row h Signal	Row g Signal	Row f Signal	Row e Signal	Row d Signal	Row c Signal	Row b Signal	Row a Signal
1	DIO0	GND	GND	XMC_A5	XMC_B5	GND	GND	XMC_D5	XMC_E5
2	GND	XMC_A7	XMC_B7	GND	GND	XMC_D7	XMC_E7	GND	GND
3	DIO1	GND	GND	XMC_A9	XMC_B9	GND	GND	XMC_D9	XMC_E9
4	GND	XMC_A15	XMC_B15	GND	GND	XMC_D15	XMC_E15	GND	GND
5	DIO2	GND	GND	XMC_A17	XMC_B17	GND	GND	XMC_D17	XMC_E17
6	GND	XMC_A19	XMC_B19	GND	GND	XMC_D19	XMC_E19	GND	GND
7	DIO3	GND	GND	NC	NC	GND	GND	NC	NC
8	GND	SATA_A_TXN1	SATA_A_TXP1	GND	GND	SATA_A_RXN1	SATA_A_RXP1	GND	GND
9	DIO4	GND	GND	SATA_B_TXN1	SATA_B_TXP1	GND	GND	SATA_B_RXN1	SATA_B_RXP1
10	GND	NC	NC	GND	GND	NC	NC	GND	GND
11	DIO5	GND	GND	NC	NC	GND	GND	NC	NC
12	GND	USB_A0_N	USB_A0_P	GND	GND	USB_B0_N	USB_B0_P	GND	GND
13	DIO6	GND	GND	USB_A0_ POWER	NC	GND	GND	USB_B0_ POWER	NC
14	GND	NC	NC	GND	GND	NC	NC	GND	GND
15	DIO7	GND	GND	DIO8	DIO9	GND	GND	DIO10	DIO11
16	GND	DIO12	DIO13	GND	GND	DIO14	DIO15	GND	GND

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J1 FRONT PANEL CONNECTOR



Note

The direction of the signals in the table describing the J1 front panel connector is from the point of view of the baseboard.

Table A.24: J1 Front Panel Connector Description

Pin No.	Signal Name	Dir	Description	Electrical Characteristics
1	GND	GND	Signal Ground	GND
2	RS232_A0_TX	O	Front Panel Serial Port A TX	EIA-232
3	FP_ETH_A_N3	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
4	FP_ETH_A_P2	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
5	FP_ETH_A_N1	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
6	FP_ETH_A_P0	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
7	FP_ETH_B_P0	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
8	FP_ETH_B_P1	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
9	FP_ETH_B_P2	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
10	FP_ETH_B_P3	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
11	FP_USB_A_5V	O	USB Power	USB 2.0
12	FP_USB_A_P	I/O	USB Data	USB 2.0
13	RS232_B0_TX	O	Front Panel Serial Port B TX	EIA-232
14	RS232_B0_RX	I	Front Panel Serial Port B RX	EIA-232
15	RS232_A0_RX	I	Front Panel Serial Port A RX	EIA-232
16	FP_ETH_A_P3	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
17	FP_ETH_A_N2	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
18	FP_ETH_A_P1	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
19	FP_ETH_A_N0	I/O	Front Panel Ethernet Port Node A	IEEE 802.3
20	FP_ETH_B_N0	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
21	FP_ETH_B_N1	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
22	FP_ETH_B_N2	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
23	FP_ETH_B_N3	I/O	Front Panel Ethernet Port Node B	IEEE 802.3
24	PB_RESET_L	I	Push Button Reset	
25	FP_USB_A_N	I/O	USB Data	USB 2.0

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Table A.24: J1 Front Panel Connector Description (Continued)

26	GND	GND	Signal Ground	GND
27	CHASSIS_GND	CGND	Chassis Ground	CGND
28	CHASSIS_GND	CGND	Chassis Ground	CGND

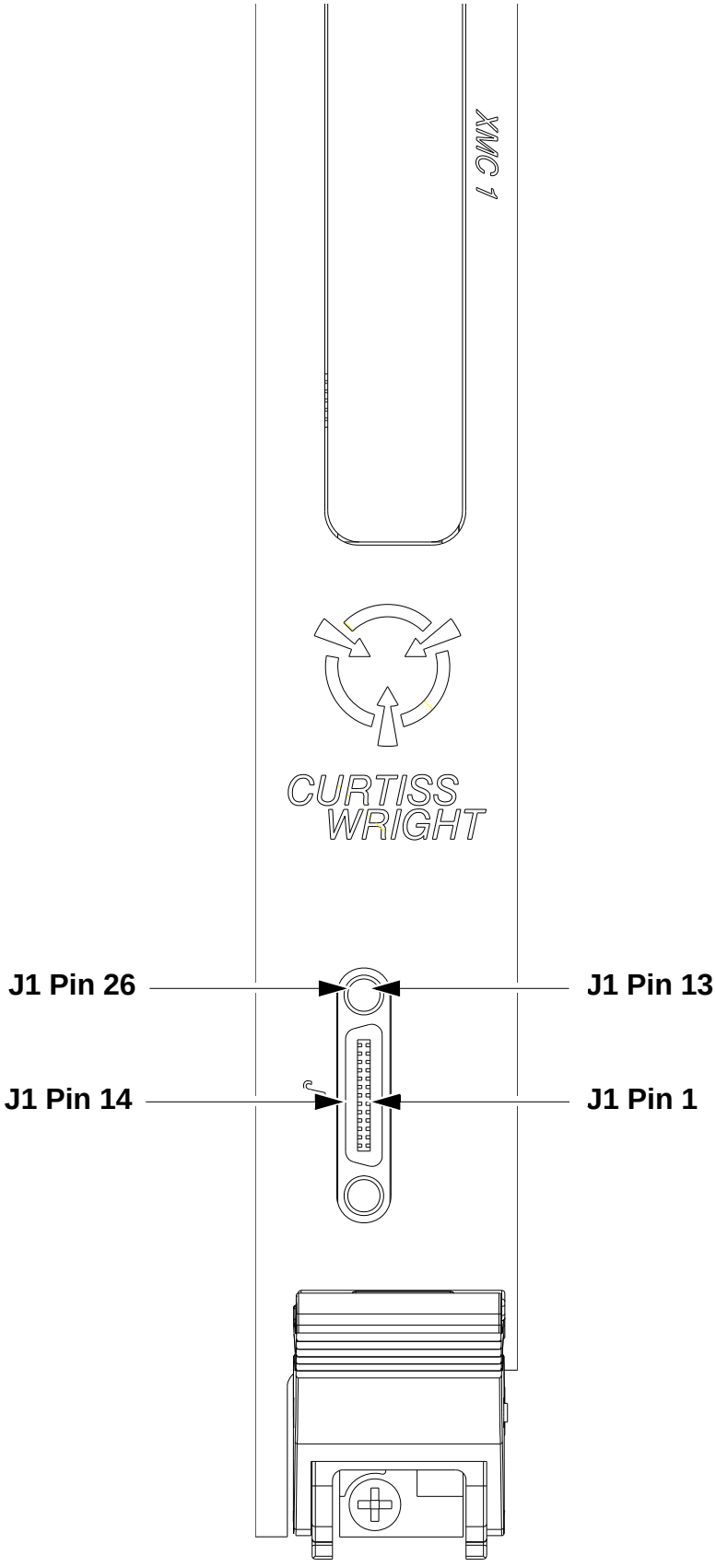


Note

The CHAMP-AV8 J1 front panel connector is designed for use with the front panel cable described in "CBL-462-FPL-000 (903075-000)" on page 2-6.

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Figure A.15: J1 Contact Numbering Arrangement (Looking into the Front Panel)



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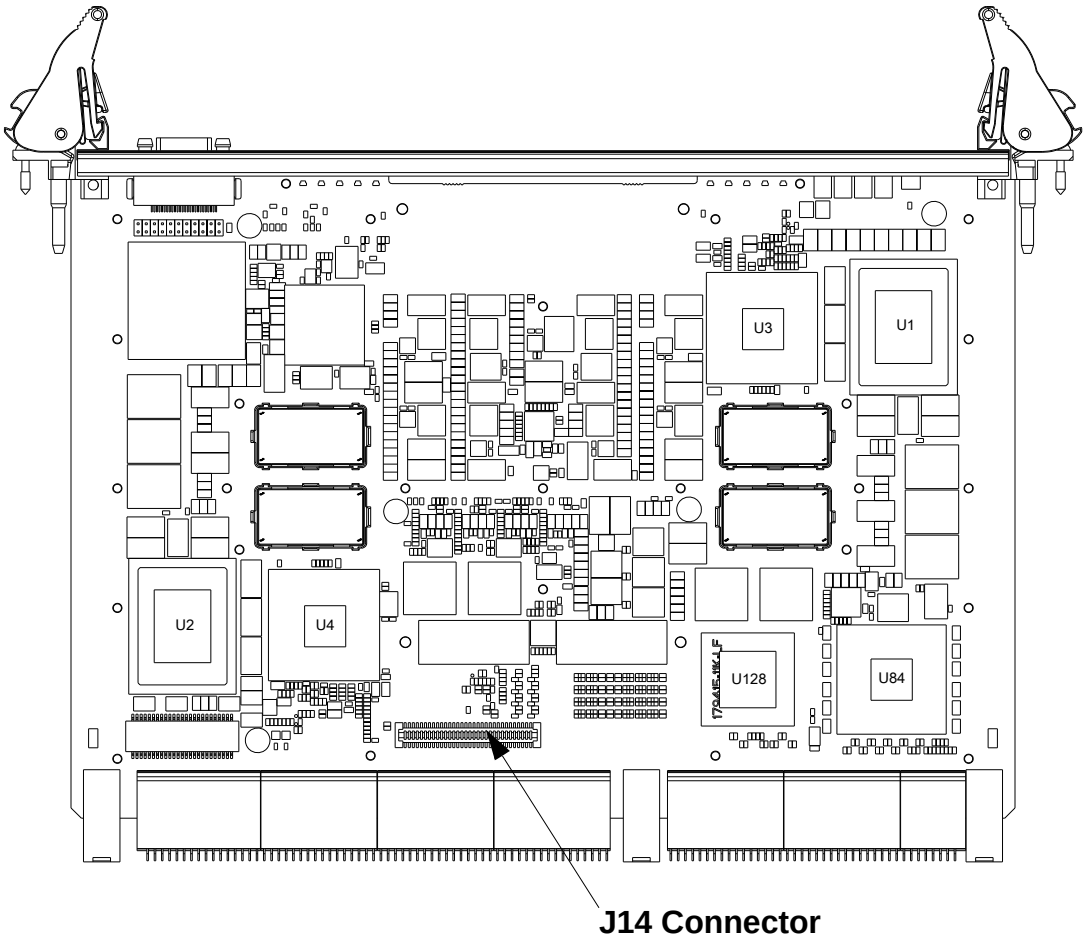
XMC SITE'S PMC J14 CONNECTOR

The CHAMP-AV8 incorporates an XMC site that supports legacy PMC user I/O. The XMC's legacy PMC I/O connector location is shown in Figure A.16 and described in the following section.

Note

The direction of the signals in the table describing the PMC J14 connector is from the point of view of the baseboard.

Figure A.16: Location of CHAMP-AV8 J14 Connector



XMC SITE'S PMC J14 USER I/O CONNECTOR

Table A.25 on page A-40 lists the pin assignments for the connector referenced J14. This connector is part of the XMC site's legacy PMC user I/O, and is referenced as Pn4/Jn4 in the PMC specification IEEE 1386.1-2001. The table maps the J14 signals to the corresponding VITA 46/48 P3 connector pins. The signals are differentially routed between the J14 connector and the P3 backplane connector in accordance with the P64s pattern defined in VITA 46.9d0.25. The adjacent signals in a given column on the P3 connector (e.g. J14-01 and J14-03) are routed differentially.

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Table A.25: J14 Connector Description (Pn4/Jn4 User Defined I/O)

PMC J14 Pin Number	VITA 46/48 P3 Connector Pin Number	PMC Differential Routing Partner on P3 / Corresponding J14 Pin Number	Direction	Description
1	P3-E1	P3-D1/J14-03	I/O	J14-01 connection to P3 connector
2	P3-B1	P3-A1/J14-04	I/O	J14-02 connection to P3 connector
3	P3-D1	P3-E1/J14-01	I/O	J14-03 connection to P3 connector
4	P3-A1	P3-B1/J14-02	I/O	J14-04 connection to P3 connector
5	P3-F2	P3-E2/J14-07	I/O	J14-05 connection to P3 connector
6	P3-C2	P3-B2/J14-08	I/O	J14-06 connection to P3 connector
7	P3-E2	P3-F2/J14-05	I/O	J14-07 connection to P3 connector
8	P3-B2	P3-C2/J14-06	I/O	J14-08 connection to P3 connector
9	P3-E3	P3-D3/J14-11	I/O	J14-09 connection to P3 connector
10	P3-B3	P3-A3/J14-12	I/O	J14-10 connection to P3 connector
11	P3-D3	P3-E3/J14-09	I/O	J14-11 connection to P3 connector
12	P3-A3	P3-B3/J14-10	I/O	J14-12 connection to P3 connector
13	P3-F4	P3-E4/J14-15	I/O	J14-13 connection to P3 connector
14	P3-C4	P3-B4/J14-16	I/O	J14-14 connection to P3 connector
15	P3-E4	P3-F4/J14-13	I/O	J14-15 connection to P3 connector
16	P3-B4	P3-C4/J14-14	I/O	J14-16 connection to P3 connector
17	P3-E5	P3-D5/J14-19	I/O	J14-17 connection to P3 connector
18	P3-B5	P3-A5/J14-20	I/O	J14-18 connection to P3 connector
19	P3-D5	P3-E5/J14-17	I/O	J14-19 connection to P3 connector
20	P3-A5	P3-B5/J14-18	I/O	J14-20 connection to P3 connector
21	P3-F6	P3-E6/J14-23	I/O	J14-21 connection to P3 connector
22	P3-C6	P3-B6/J14-24	I/O	J14-22 connection to P3 connector
23	P3-E6	P3-F6/J14-21	I/O	J14-23 connection to P3 connector
24	P3-B6	P3-C6/J14-22	I/O	J14-24 connection to P3 connector
25	P3-E7	P3-D7/J14-27	I/O	J14-25 connection to P3 connector
26	P3-B7	P3-A7/J14-28	I/O	J14-26 connection to P3 connector
27	P3-D7	P3-E7/J14-25	I/O	J14-27 connection to P3 connector
28	P3-A7	P3-B7/J14-26	I/O	J14-28 connection to P3 connector
29	P3-F8	P3-E8/J14-31	I/O	J14-29 connection to P3 connector
30	P3-C8	P3-B8/J14-32	I/O	J14-30 connection to P3 connector
31	P3-E8	P3-F8/J14-29	I/O	J14-31 connection to P3 connector

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Table A.25: J14 Connector Description (Pn4/Jn4 User Defined I/O) (Continued)

32	P3-B8	P3-C8/J14-30	I/O	J14-32 connection to P3 connector
33	P3-E9	P3-D9/J14-35	I/O	J14-33 connection to P3 connector
34	P3-B9	P3-A9/J14-36	I/O	J14-34 connection to P3 connector
35	P3-D9	P3-E9/J14-33	I/O	J14-35 connection to P3 connector
36	P3-A9	P3-B9/J14-34	I/O	J14-36 connection to P3 connector
37	P3-F10	P3-E10/J14-39	I/O	J14-37 connection to P3 connector
38	P3-C10	P3-B10/J14-40	I/O	J14-38 connection to P3 connector
39	P3-E10	P3-F10/J14-37	I/O	J14-39 connection to P3 connector
40	P3-B10	P3-C10/J14-38	I/O	J14-40 connection to P3 connector
41	P3-E11	P3-D11/J14-43	I/O	J14-41 connection to P3 connector
42	P3-B11	P3-A11/J14-44	I/O	J14-42 connection to P3 connector
43	P3-D11	P3-E11/J14-41	I/O	J14-43 connection to P3 connector
44	P3-A11	P3-B11/J14-42	I/O	J14-44 connection to P3 connector
45	P3-F12	P3-E12/J14-47	I/O	J14-45 connection to P3 connector
46	P3-C12	P3-B12/J14-48	I/O	J14-46 connection to P3 connector
47	P3-E12	P3-F12/J14-45	I/O	J14-47 connection to P3 connector
48	P3-B12	P3-C12/J14-46	I/O	J14-48 connection to P3 connector
49	P3-E13	P3-D13/J14-51	I/O	J14-49 connection to P3 connector
50	P3-B13	P3-A13/J14-52	I/O	J14-50 connection to P3 connector
51	P3-D13	P3-E13/J14-49	I/O	J14-51 connection to P3 connector
52	P3-A13	P3-B13/J14-50	I/O	J14-52 connection to P3 connector
53	P3-F14	P3-E14/J14-55	I/O	J14-53 connection to P3 connector
54	P3-C14	P3-B14/J14-56	I/O	J14-54 connection to P3 connector
55	P3-E14	P3-F14/J14-53	I/O	J14-55 connection to P3 connector
56	P3-B14	P3-C14/J14-54	I/O	J14-56 connection to P3 connector
57	P3-E15	P3-D15/J14-59	I/O	J14-57 connection to P3 connector
58	P3-B15	P3-A15/J14-60	I/O	J14-58 connection to P3 connector
59	P3-D15	P3-E15/J14-57	I/O	J14-59 connection to P3 connector
60	P3-A15	P3-B15/J14-58	I/O	J14-60 connection to P3 connector
61	P3-F16	P3-E16/J14-63	I/O	J14-61 connection to P3 connector
62	P3-C16	P3-B16/J14-64	I/O	J14-62 connection to P3 connector
63	P3-E16	P3-F16/J14-61	I/O	J14-63 connection to P3 connector
64	P3-B16	P3-C16/J14-62	I/O	J14-64 connection to P3 connector

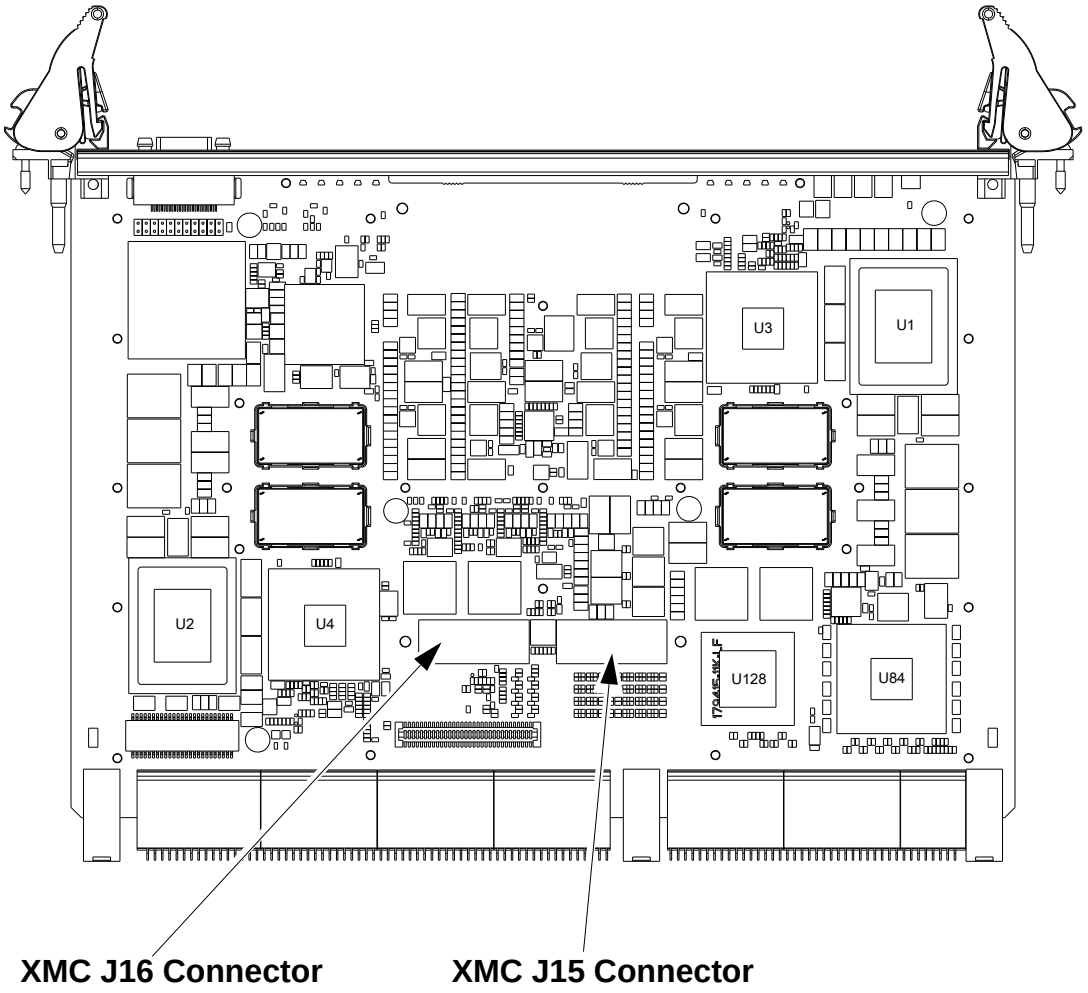
Note: The electrical characteristics of each signal in the above table are XMC module-dependent.

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XMC J15 AND J16 CONNECTORS

The CHAMP-AV8 incorporates a single width XMC site in accordance with VITA 42.0 and VITA 42.3. The XMC site includes the connectors designated J15 and J16 as shown in Figure A.17.

Figure A.17: Location of CHAMP-AV8 XMC J15 and J16 Connectors



XMC J15 CONNECTOR

Table A.26 on page A-43 lists the pin assignments for the XMC J15 connector. The J15 connector is the primary XMC connector as defined in V42.0. The XMC supports a single x8, x4, x2, or x1 PCI link in accordance with V42.3.

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Table A.26: J15 Primary XMC Connector Pin Assignments

Pin No.	Row A Signal	Row B Signal	Row C Signal	Row D Signal	Row E Signal	Row F Signal
1	XMC_TX_P0	XMC_TX_N0	3V3	XMC_TX_P1	XMC_TX_N1	12V0
2	GND	GND	XMC_TRST_L	GND	GND	XMC_RST_L
3	XMC_TX_P2	XMC_TX_N2	3V3	XMC_TX_P3	XMC_TX_N3	12V0
4	GND	GND	XMC_TCK	GND	GND	XMC_RSTIN_L
5	XMC_TX_P4	XMC_TX_N4	3V3	XMC_TX_P5	XMC_TX_N5	12V0
6	GND	GND	XMC_TMS	GND	GND	P12V
7	XMC_TX_P6	XMC_TX_N6	3V3	XMC_TX_P7	XMC_TX_N7	12V0
8	GND	GND	XMC_TDI	GND	GND	N12V
9	BGA_XMC_ GPIO_0	BGA_XMC_ GPIO_1	AT_BTEI_L	BGA_XMC_ GPIO_2	BGA_XMC_ GPIO_3	12V0
10	GND	GND	XMC_TDO	GND	GND	XMC_GA0
11	XMC_RXZ_P0	XMC_RXZ_N0	XMC_MBIST_L	XMC_RXZ_P1	XMC_RXZ_N1	12V0
12	GND	GND	XMC_GA1	GND	GND	XMC_PRESENT_L
13	XMC_RXZ_P2	XMC_RXZ_N2	3V3_AUX	XMC_RXZ_P3	XMC_RXZ_N3	12V0
14	GND	GND	XMC_GA2	GND	GND	SMB_THERM_ DATA
15	XMC_RXZ_P4	XMC_RXZ_N4	AT_VCCO	XMC_RXZ_P5	XMC_RXZ_N5	12V0
16	GND	GND	XMC_F_NVMRO	GND	GND	SMB_THERM_CLK
17	XMC_RXZ_P6	XMC_RXZ_N6	RFU_J25_C17	XMC_RXZ_P7	XMC_RXZ_N7	RFU _F17
18	GND	GND	AT_MTEI_L/RFU	GND	GND	AT_SCL/ RFU
19	B_CLK_PCH_ SRC0_P	B_CLK_PCH_ SRC0_N	AT_LBAT_L/RFU	XMC_WAKE_L	XMC_ROOT_L	AT_SDA/RFU

Table A.27: J15 Primary XMC Connector Signal Definitions

XMC Signal	Description
XMC_TX/RXZ_P/N[0:7]	Differential Transmit/Receive. These signals are used by the XMC to transmit / receive high-speed protocol-specific data to the carrier over the PCI Express interface.
B_CLK_PCH_SRC0_P/N	Differential reference clock for the PCI Express interface link. This signal is generated by the carrier and transmitted to the mezzanine.
XMC_WAKE_L	An open-drain, active low signal that is driven low by an XMC PCI Express function to reactivate the links main power rails and reference clocks. The CHAMP-AV8 does not support XMC wake functionality and pulls the signal up to 3.3V AUX.
XMC_ROOT_L	This signal shall be driven low by the carrier to enable the Root Complex features of a Processor XMC. The CHAMP-AV8 does not support this feature and pulls the signal up to 3.3V.
SMB_THERM_CLK	I2C serial clock.
SMB_THERM_DATA	I2C serial data
XMC_GA0:2	I2C channel select. These are inputs to the XMC and are driven as 011 on the CHAMP-AV8.
XMC_MBIST_L	XMC Built In Self Test. This signal is an output from the XMC and allows the carrier to determine whether an XMC has completed its built-in self test. If this signal is used by the XMC, it shall be asserted low at the de-assertion of MRSTI_L to indicate that the XMC is performing self-test and is not yet ready.

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Table A.27: J15 Primary XMC Connector Signal Definitions (Continued)

XMC_F_NVMRO	XMC Write Prohibit. This signal is an input to the XMC. When this signal is asserted high, the XMC shall disable writes to non-volatile memory on the XMC. The CHAMP-AV8 ties this signal to the VITA 46 NVMRO signal (VITA 46 P0-A4).
XMC_RST_L	This signal is an input to the XMC. When this signal is asserted low, the XMC shall initialize itself into a known state.
XMC_RSTIN_L	This signal is an output from the XMC. When asserted low by the XMC, the CHAMP-AV8 will initiate a board reset.
XMC_PRESENT_L	This signal allows the carrier to determine whether an XMC is present.
XMC_TDI, XMC_TDO, XMC_TCK, XMC_TMS, XMC_TRST_L	JTAG Signals
12V0	VPWR Power pins. These signals carry12V power from the carrier to the XMC. The CHAMP-AV8 supplies 12V sequenced power on the VPWR (power turn-on will be delayed with respect to the backplane power).
3V3	3.3 V Power pins. The 3.3V power is regulated to within 3.3V +/-0.3V. The power is sequenced with the 3V3 power supplied on the VPWR pins (power turn-on will be delayed with respect to the back-plane power).
3V3_AUX	3.3 V Auxiliary Power pin. The 3.3V_AUX power is supplied directly from the VITA 46 3.3V Aux (VITA 46 P0-D5) pin (power turn-on will occur prior to VPWR and 3.3V turn-on).
P/N12V	+/-12 V Auxiliary Power pin. The +/-12V power is supplied directly from the VITA 46 12V Aux (VITA 46 P0-D6) and N12V Aux (VITA 46 P0-D6) pins (power turn-on will occur prior to VPWR and 3.3V turn-on).
RSVD	Not available- Reserved for Curtiss-Wright use
RFU	Reserved for future use
GND	Ground signals as defined in VITA 42.0.

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XMC J16 USER I/O CONNECTOR

Table A.28 lists the pin assignments for the XMC J16 connector. The J16 connector is the secondary XMC connector as defined in V42.0 and is used for user I/O. The user I/O includes single ended and high speed differential signals routed between the J16 connector and the VITA 46/48 P5 and P6 connectors in accordance with the P5w3P6–X38s+X8d+X12d pattern defined in VITA 46.9.

Table A.28: J16 Secondary XMC Connector Pin Assignments

Pin No.	Row A Signal	Row B Signal	Row C Signal	Row D Signal	Row E Signal	Row F Signal
1	XMC_DP0_P	XMC_DP0_N	XMC_C01	XMC_DP1_P	XMC_DP1_N	XMC_F01
2	GND	GND	XMC_C02	GND	GND	XMC_F02
3	XMC_DP2_P	XMC_DP2_N	XMC_C03	XMC_DP3_P	XMC_DP3_N	XMC_F03
4	GND	GND	XMC_C04	GND	GND	XMC_F04
5	XMC_DP4_P	XMC_DP4_N	XMC_C05	XMC_DP5_P	XMC_DP5_N	XMC_F05
6	GND	GND	XMC_C06	GND	GND	XMC_F06
7	XMC_DP6_P	XMC_DP6_N	XMC_C07	XMC_DP7_P	XMC_DP7_N	XMC_F07
8	GND	GND	XMC_C08	GND	GND	XMC_F08
9	XMC_DP8_P	XMC_DP8_N	XMC_C09	XMC_DP9_P	XMC_DP9_N	XMC_F09
10	GND	GND	XMC_C10	GND	GND	XMC_F10
11	XMC_DP10_P	XMC_DP10_N	XMC_C11	XMC_DP11_P	XMC_DP11_N	XMC_F11
12	GND	GND	XMC_C12	GND	GND	XMC_F12
13	XMC_DP12_P	XMC_DP12_N	XMC_C13	XMC_DP13_P	XMC_DP13_N	XMC_F13
14	GND	GND	XMC_C14	GND	GND	XMC_F14
15	XMC_DP14_P	XMC_DP14_N	XMC_C15	XMC_DP15_P	XMC_DP15_N	XMC_F15
16	GND	GND	XMC_C16	GND	GND	XMC_F16
17	XMC_DP16_P	XMC_DP16_N	XMC_C17	XMC_DP17_P	XMC_DP17_N	XMC_F17
18	GND	GND	XMC_C18	GND	GND	XMC_F18
19	XMC_DP18_P	XMC_DP18_N	XMC_C19	XMC_DP19_P	XMC_DP19_N	XMC_F19

Table A.29: J16 Secondary XMC Connector Signal Definitions

XMC Signal	Description
XMC_DP[0:19]_P/N	Differential User I/O signals
XMC_C[01:19]	Row C Single ended XMC user I/O signals
XMC_F[01:19]	Row F Single ended XMC user I/O signals
GND	Ground signals as defined in VITA 42.0.

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Tables A.30 through A.35 list the row by row pin assignments for the connector referenced J16.

J16 Row A

Table A.30 lists the pin assignments for Row A of the connector referenced J16. The table maps the J16 Row A XMC User I/O signals to the corresponding VITA 46/48 P5 or P6 connector pins of the CHAMP-AV8 board. The signals are routed as high speed differential signals in accordance with the P5w3P6–X38s+X8d+X12d pattern defined in VITA 46.9.

Table A.30: XMC J16 User I/O Connector Description (Row A)

XMC J16 Row A Pin Number	VITA 46/48 P5/P6 Connector Pin Number	Direction	Description	Electrical Characteristics
J16-A1	P5-E13	I/O	XMC_DP0_P connection to P5 connector	Depends on XMC module
J16-A2		GND	GND	GND
J16-A3	P5-F14	I/O	XMC_DP2_P connection to P5 connector	Depends on XMC module
J16-A4		GND	GND	GND
J16-A5	P6-E1	I/O	XMC_DP4_P connection to P6 connector	Depends on XMC module
J16-A6		GND	GND	GND
J16-A7	P6-F2	I/O	XMC_DP6_P connection to P6 connector	Depends on XMC module
J16-A8		GND	GND	GND
J16-A9	P6-E3	I/O	XMC_DP8_P connection to P6 connector	Depends on XMC module
J16-A10		GND	GND	GND
J16-A11	P5-E15	I/O	XMC_DP10_P connection to P5 connector	Depends on XMC module
J16-A12		GND	GND	GND
J16-A13	P5-F16	I/O	XMC_DP12_P connection to P5 connector	Depends on XMC module
J16-A14		GND	GND	GND
J16-A15	P6-F4	I/O	XMC_DP14_P connection to P6 connector	Depends on XMC module
J16-A16		GND	GND	GND
J16-A17	P6-E5	I/O	XMC_DP16_P connection to P6 connector	Depends on XMC module
J16-A18		GND	GND	GND
J16-A19	P6-F6	I/O	XMC_DP18_P connection to P6 connector	Depends on XMC module

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J16 Row B

Table A.31 lists the pin assignments for Row B of the connector referenced J16. This connector is part of XMC site. The table maps the J16 Row B XMC User I/O signals to the corresponding VITA 46/48 P5 or P6 connector pins of the CHAMP-AV8 board. The signals are routed as high speed differential signals in accordance with the P5w3P6–X38s+X8d+X12d pattern defined in VITA 46.9.

Table A.31: XMC J16 User I/O Connector Description (Row B)

XMC J16 Row B Pin Number	VITA 46/48 P5/P6 Connector Pin Number	Direction	Description	Electrical Characteristics
J16-B1	P5-D13	I/O	XMC_DP0_N connection to P5 connector	Depends on XMC module
J16-B2		GND	GND	GND
J16-B3	P5-E14	I/O	XMC_DP2_N connection to P5 connector	Depends on XMC module
J16-B4		GND	GND	GND
J16-B5	P6-D1	I/O	XMC_DP4_N connection to P6 connector	Depends on XMC module
J16-B6		GND	GND	GND
J16-B7	P6-E2	I/O	XMC_DP6_N connection to P6 connector	Depends on XMC module
J16-B8		GND	GND	GND
J16-B9	P6-D3	I/O	XMC_DP8_N connection to P6 connector	Depends on XMC module
J16-B10		GND	GND	GND
J16-B11	P5-D15	I/O	XMC_DP10_N connection to P5 connector	Depends on XMC module
J16-B12		GND	GND	GND
J16-B13	P5-E16	I/O	XMC_DP12_N connection to P5 connector	Depends on XMC module
J16-B14		GND	GND	GND
J16-B15	P6-E4	I/O	XMC_DP14_N connection to P6 connector	Depends on XMC module
J16-B16		GND	GND	GND
J16-B17	P6-D5	I/O	XMC_DP16_N connection to P6 connector	Depends on XMC module
J16-B18		GND	GND	GND
J16-B19	P6-E6	I/O	XMC_DP18_N connection to P6 connector	Depends on XMC module

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J16 Row C

Table A.32 lists the pin assignments for Row C of the connector referenced J16. This connector is part of XMC site. The table maps the J16 Row C XMC User I/O signals to the corresponding VITA 46/48 P5 connector pins of the CHAMP-AV8 board. The signals are routed as single ended signals in accordance with the P5w3P6–X38s+X8d+X12d pattern defined in VITA 46.9.

Table A.32: XMC J16 User I/O Connector Description (Row C)

XMC J16 Row C Pin Number	VITA 46/48 P5 Connector Pin Number	Direction	Description	Electrical Characteristics
J16-C1	P5-B3	I/O	XMC_C01 connection to P5 connector	Depends on XMC module
J16-C2	P5-F4	I/O	XMC_C02 connection to P5 connector	Depends on XMC module
J16-C3	P5-E4	I/O	XMC_C03 connection to P5 connector	Depends on XMC module
J16-C4	P5-E5	I/O	XMC_C04 connection to P5 connector	Depends on XMC module
J16-C5	P5-D5	I/O	XMC_C05 connection to P5 connector	Depends on XMC module
J16-C6	P5-F6	I/O	XMC_C06 connection to P5 connector	Depends on XMC module
J16-C7	P5-E6	I/O	XMC_C07 connection to P5 connector	Depends on XMC module
J16-C8	P5-E7	I/O	XMC_C08 connection to P5 connector	Depends on XMC module
J16-C9	P5-D7	I/O	XMC_C09 connection to P5 connector	Depends on XMC module
J16-C10	P5-F8	I/O	XMC_C10 connection to P5 connector	Depends on XMC module
J16-C11	P5-E8	I/O	XMC_C11 connection to P5 connector	Depends on XMC module
J16-C12	P5-E9	I/O	XMC_C12 connection to P5 connector	Depends on XMC module
J16-C13	P5-D9	I/O	XMC_C13 connection to P5 connector	Depends on XMC module
J16-C14	P5-F10	I/O	XMC_C14 connection to P5 connector	Depends on XMC module
J16-C15	P5-E10	I/O	XMC_C15 connection to P5 connector	Depends on XMC module
J16-C16	P5-E11	I/O	XMC_C16 connection to P5 connector	Depends on XMC module
J16-C17	P5-D11	I/O	XMC_C17 connection to P5 connector	Depends on XMC module
J16-C18	P5-F12	I/O	XMC_C18 connection to P5 connector	Depends on XMC module
J16-C19	P5-E12	I/O	XMC_C19 connection to P5 connector	Depends on XMC module

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J16 Row D

Table A.33 lists the pin assignments for Row D of the connector referenced J16. This connector is part of XMC site. The table maps the J16 Row D XMC User I/O signals to the corresponding VITA 46/48 P5 or P6 connector pins of the CHAMP-AV8 board. The signals are routed as high speed differential signals in accordance with the P5w3P6–X38s+X8d+X12d pattern defined in VITA 46.9.

Table A.33: XMC J16 User I/O Connector Description (Row D)

XMC J16 Row D Pin Number	VITA 46/48 P5/P6 Connector Pin Number	Direction	Description	Electrical Characteristics
J16-D1	P5-B13	I/O	XMC_DP1_P connection to P5 connector	Depends on XMC module
J16-D2		GND	GND	GND
J16-D3	P5-C14	I/O	XMC_DP3_P connection to P5 connector	Depends on XMC module
J16-D4		GND	GND	GND
J16-D5	P6-B1	I/O	XMC_DP5_P connection to P6 connector	Depends on XMC module
J16-D6		GND	GND	GND
J16-D7	P6-C2	I/O	XMC_DP7_P connection to P6 connector	Depends on XMC module
J16-D8		GND	GND	GND
J16-D9	P6-B3	I/O	XMC_DP9_P connection to P6 connector	Depends on XMC module
J16-D10		GND	GND	GND
J16-D11	P5-B15	I/O	XMC_DP11_P connection to P5 connector	Depends on XMC module
J16-D12		GND	GND	GND
J16-D13	P5-C16	I/O	XMC_DP13_P connection to P5 connector	Depends on XMC module
J16-D14		GND	GND	GND
J16-D15	P6-C4	I/O	XMC_DP15_P connection to P6 connector	Depends on XMC module
J16-D16		GND	GND	GND
J16-D17	P6-B5	I/O	XMC_DP17_P connection to P6 connector	Depends on XMC module
J16-D18		GND	GND	GND
J16-D19	P6-C6	I/O	XMC_DP19_P connection to P6 connector	Depends on XMC module

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J16 Row E

Table A.33 lists the pin assignments for Row E of the connector referenced J16. This connector is part of XMC site. The table maps the J16 Row E XMC User I/O signals to the corresponding VITA 46/48 P5 or P6 connector pins of the CHAMP-AV8 board. The signals are routed as high speed differential signals in accordance with the P5w3P6–X38s+X8d+X12d pattern defined in VITA 46.9.

Table A.34: XMC J16 User I/O Connector Description (Row E)

XMC J16 Row E Pin Number	VITA 46/48 P5/P6 Connector Pin Number	Direction	Description	Electrical Characteristics
J16-E1	P5-A13	I/O	XMC_DP1_N connection to P5 connector	Depends on XMC module
J16-E2		GND	GND	GND
J16-E3	P5-B14	I/O	XMC_DP3_N connection to P5 connector	Depends on XMC module
J16-E4		GND	GND	GND
J16-E5	P6-A1	I/O	XMC_DP5_N connection to P6 connector	Depends on XMC module
J16-E6		GND	GND	GND
J16-E7	P6-B2	I/O	XMC_DP7_N connection to P6 connector	Depends on XMC module
J16-E8		GND	GND	GND
J16-E9	P6-A3	I/O	XMC_DP9_N connection to P6 connector	Depends on XMC module
J16-E10		GND	GND	GND
J16-E11	P5-A15	I/O	XMC_DP11_N connection to P5 connector	Depends on XMC module
J16-E12		GND	GND	GND
J16-E13	P5-B16	I/O	XMC_DP13_N connection to P5 connector	Depends on XMC module
J16-E14		GND	GND	GND
J16-E15	P6-B4	I/O	XMC_DP15_N connection to P6 connector	Depends on XMC module
J16-E16		GND	GND	GND
J16-E17	P6-A5	I/O	XMC_DP17_N connection to P6 connector	Depends on XMC module
J16-E18		GND	GND	GND
J16-E19	P6-B6	I/O	XMC_DP19_N connection to P6 connector	Depends on XMC module

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J16 Row F

Table A.35 lists the pin assignments for Row F of the connector referenced J16. This connector is part of XMC site. The table maps the J16 Row F XMC User I/O signals to the corresponding VITA 46/48 P5 connector pins of the CHAMP-AV8 board. The signals are routed as single ended signals in accordance with the P5w3P6–X38s+X8d+X12d pattern defined in VITA 46.9.

Table A.35: XMC J16 User I/O Connector Description (Row F)

XMC J16 Row F Pin Number	VITA 46/48 P5 Connector Pin Number	Direction	Description	Electrical Characteristics
J16-F1	P5-A3	I/O	XMC_F01 connection to P5 connector	Depends on XMC module
J16-F2	P5-C4	I/O	XMC_F02 connection to P5 connector	Depends on XMC module
J16-F3	P5-B4	I/O	XMC_F03 connection to P5 connector	Depends on XMC module
J16-F4	P5-B5	I/O	XMC_F04 connection to P5 connector	Depends on XMC module
J16-F5	P5-A5	I/O	XMC_F05 connection to P5 connector	Depends on XMC module
J16-F6	P5-C6	I/O	XMC_F06 connection to P5 connector	Depends on XMC module
J16-F7	P5-B6	I/O	XMC_F07 connection to P5 connector	Depends on XMC module
J16-F8	P5-B7	I/O	XMC_F08 connection to P5 connector	Depends on XMC module
J16-F9	P5-A7	I/O	XMC_F09 connection to P5 connector	Depends on XMC module
J16-F10	P5-C8	I/O	XMC_F10 connection to P5 connector	Depends on XMC module
J16-F11	P5-B8	I/O	XMC_F11 connection to P5 connector	Depends on XMC module
J16-F12	P5-B9	I/O	XMC_F12 connection to P5 connector	Depends on XMC module
J16-F13	P5-A9	I/O	XMC_F13 connection to P5 connector	Depends on XMC module
J16-F14	P5-C10	I/O	XMC_F14 connection to P5 connector	Depends on XMC module
J16-F15	P5-B10	I/O	XMC_F15 connection to P5 connector	Depends on XMC module
J16-F16	P5-B11	I/O	XMC_F16 connection to P5 connector	Depends on XMC module
J16-F17	P5-A11	I/O	XMC_F17 connection to P5 connector	Depends on XMC module
J16-F18	P5-C12	I/O	XMC_F18 connection to P5 connector	Depends on XMC module
J16-F19	P5-B12	I/O	XMC_F19 connection to P5 connector	Depends on XMC module

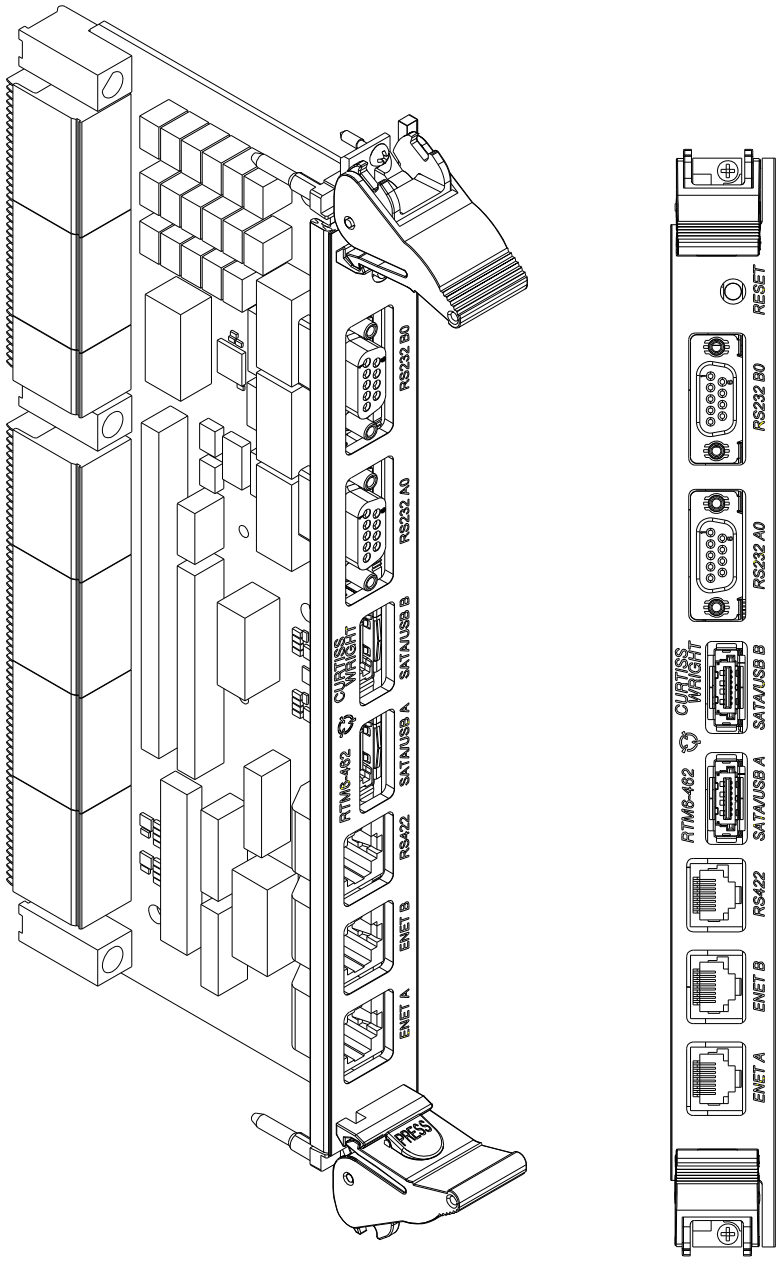
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REAR TRANSITION MODULE (RTM)

The Rear Transition Module (RTM) facilitates connections to the various I/O ports of the CHAMP-AV8.

An illustration of the various ports and the industry-standard connectors provided by the RTM is shown below in Figure A.18.

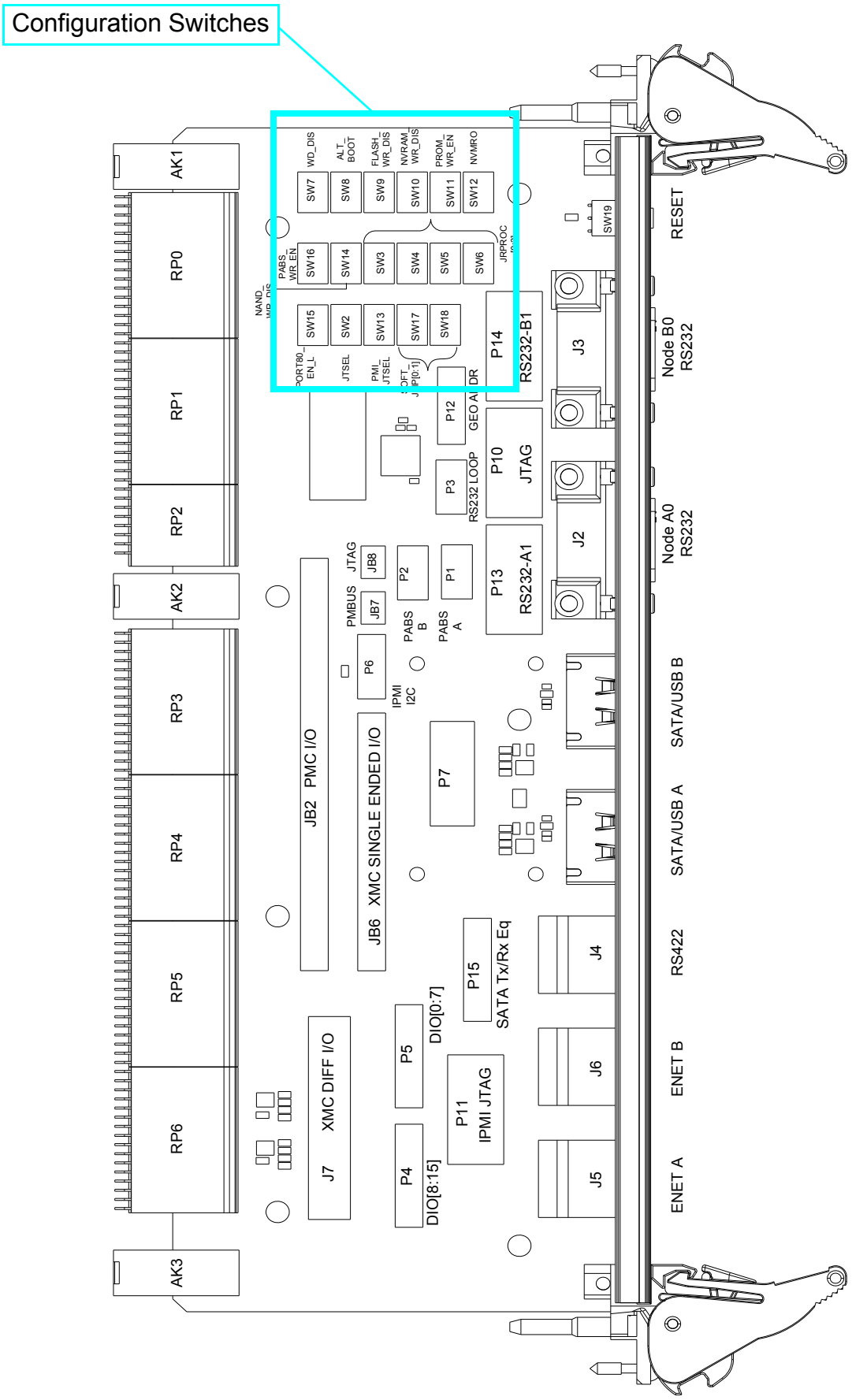
Figure A.18: CHAMP-AV8 Rear Transition Module Views



Additional interfaces and controls are made available on the RTM PWB, as seen in Figure A.19, "RTM Printed Wiring Board Component Side View," on page A-53.

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Figure A.19: RTM Printed Wiring Board Component Side View



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REAR TRANSITION MODULE PANEL-MOUNTED CONNECTORS

The pinout details for the industry-standard panel-mounted connector interfaces on the Rear Transition Module are provided in the following sections.

RTM ENET A, ENET B Connectors

Ethernet ports A and B are available on RJ-45 connectors via the RTM. Both ports will auto-select 10 Mbps, 100 Mbps or 1000 Mbps, depending on what they are connected to. Ethernet port A is accessed via the J5 connector and Ethernet port B is accessed via the J6 connector. The pinouts for both connectors are identical and shown below in Table A.36.

Table A.36: RTM ENET A (J5), ENET B (J6) Connector Details

Pin Number	J5 Signal name	J6 Signal name
1	ETH_A_TRX0_P	ETH_B_TRX0_P
2	ETH_A_TRX0_N	ETH_B_TRX0_N
3	ETH_A_TRX1_P	ETH_B_TRX1_P
4	ETH_A_TRX2_P	ETH_B_TRX2_P
5	ETH_A_TRX2_N	ETH_B_TRX2_N
6	ETH_A_TRX1_N	ETH_B_TRX1_N
7	ETH_A_TRX3_P	ETH_B_TRX3_P
8	ETH_A_TRX3_N	ETH_B_TRX3_N

RTM RS422 Connector

EIA-422 serial ports are available on an RJ-45 (J4) connector on the RTM. The pin-out for the two EIA-422 ports follows a Gigabit Ethernet pin-out on an RJ-45, so that a 1000Base- T Ethernet loopback cable can be used to loop each node's transmit data port to its respective receive data port. The transmit signals are outputs from the RTM and the receive signals are inputs to the RTM. The pin-out is shown below in Table A.37.

Table A.37: RTM RS422 (J4) Connector Details

Pin Number	J4 Signal name
1	RS422_A2_TX_P
2	RS422_A2_TX_N
3	RS422_A2_RX_P
4	RS422_B2_TX_P
5	RS422_B2_TX_N
6	RS422_A2_RX_N
7	RS422_B2_RX_P
8	RS422_B2_RX_N

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Note

Serial ports are labelled consecutively. Ports 1-4 are EIA-232 and 5-6 are EIA-422.

RTM EIA-232 Serial Port Connectors

EIA-232 serial ports are available through RTM connectors, J2 and J3 (labelled as COM A and COM B on the RTM connector panel). J2 connects to processor A's serial port, J3 to processor B's serial port, The pinout for the serial ports is provided in Table A.38 below.

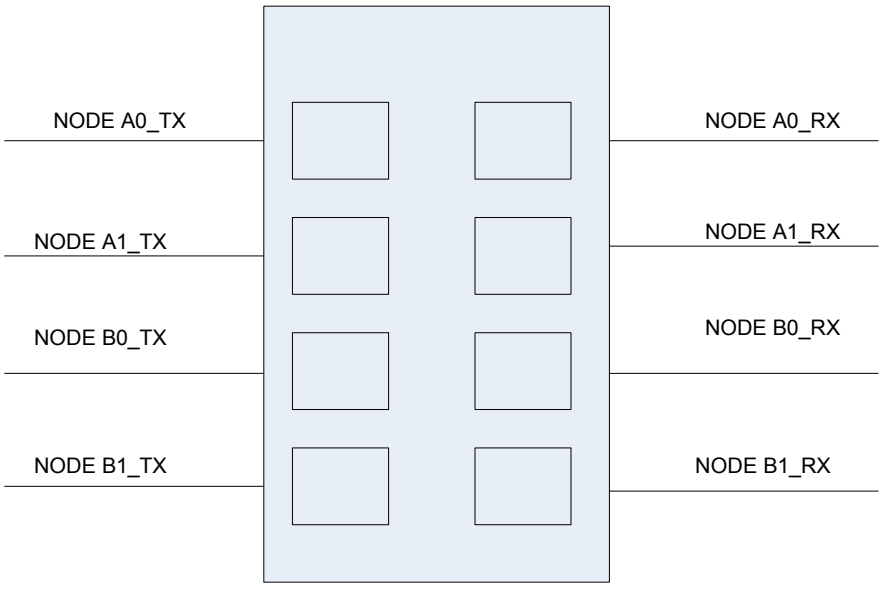
Table A.38: RTM EIA-232 COM Ports A-D (J2-J3) Connector Details

Pin Number	Signal Name	Description
2	TX	Data from processor UART
3	RX	Data to processor UART
4	DTR/NC	Connector J4: Data Terminal Ready signal (from PC)
5	GND	signal ground
1, 6-9	NC	these pins are not connected

Serial Port Loopback Control

RTM Jumper block P3, which is shown in Figure A.20 below, allows any of the EIA-232 ports to be put into loopback for testing purposes. Installing a jumper between transmit and receive "loops" transmits data back to the receive data line.

Figure A.20: Serial Port Loopback Control via RTM P3

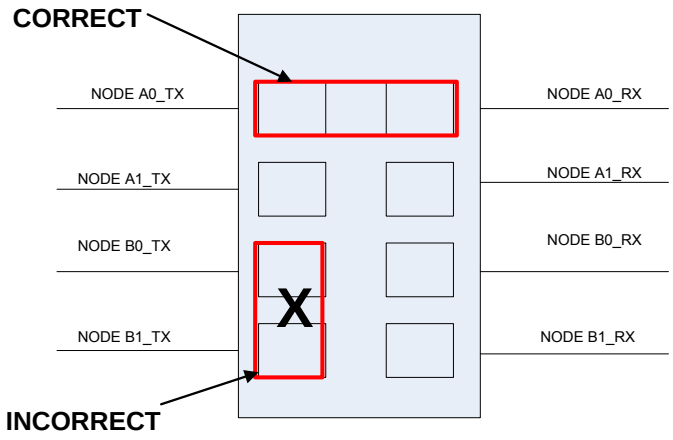


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Caution

1. Placing an EIA-232 port in loopback does not break the connection to the cable. Therefore any EIA-232 cables should be removed prior to placing a port in loopback.
2. Installing jumpers in the wrong orientation can potentially damage the board. Be careful to install jumpers only as shown. See Figure A.21 below.

Figure A.21: Proper Jumper Orientation for RTM P3 Jumpers



RTM JTAG Connector

The RTM JTAG connector is reserved for Curtiss-Wright use only.

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REAR TRANSITION MODULE (RTM) CONFIGURATION SWITCHES

As seen in Figure A.19 on page A-53, the RTM PWB provides a bank of configuration switches, numbered SW2 through SW14.

Table A.39: RTM SW2–SW18 Functions

RTM Switch	Silkscreen Label	ON	OFF	Default	AV8 Jumper
SW2	JTSEL	Enable JTAG mode	Disable JTAG mode	OFF	N/A
SW3	JPROC0	Selects JTAG scan chain when JTAG enabled	No effect when JTSEL is set to off	OFF	N/A
SW4	JPROC1			OFF	N/A
SW5	JPROC2			OFF	N/A
SW6	JPROC3			OFF	N/A
SW7	WD_DIS	Disable watchdog	Enable watchdog	OFF	JB9
SW8	ALT_BOOT	Boot from PABS flash	Boot from main boot flash	OFF	JB8
SW9	FLASH_WR_DIS	Write-protect primary boot flash	Writing enabled to primary boot flash	OFF	JB7
SW10	NVRAM_WR_DIS	Write-protect NVRAM	Writing enabled to NVRAM	OFF	JB6
SW11	PROM_WR_EN	Enable PROM writes to config PROMs (SPD, GigE, PCIe)	Disable writes to config PROMs	OFF	JB4
SW12	NVMRO	Pull NVMRO backplane signal low (see Table A.4 on page A-15 for details about the NVMRO signal). When in this state, it is possible to enable writes to main NAND flash, main boot flash, NVRAM, and FPGA PROM, independent of the setting of the associated RTM switch. This functionality is analogous to the VPX6-1957 "Curtiss-Wright Legacy Mode" described in the VPX6-1957 Hardware User's Manual (Curtiss-Wright document # 830214).	NVMRO signal is high (unless driven low by another board connected to the same backplane, or the CHAMP-AV8 JB10 jumper is ON – see Table 2.3 on page 2-7 for details).When in this state, writes to main NAND flash, main boot flash, NVRAM, and FPGA PROM may be disabled, as determined by the associated RTM switch. This functionality is analogous to the VPX6-1957 "Curtiss-Wright Legacy Mode" described in the VPX6-1957 Hardware User's Manual (Curtiss-Wright document # 830214).	OFF	N/A
SW13	PMI_JTSEL	Reserved for Curtiss-Wright Use	No effect during normal operation	OFF	N/A
SW14	NAND_WR_DIS	Write-protect SATA SSD device	Writing enabled to SATA SSD device	OFF	JB1
SW16	PABS_WR_EN	Writing enabled to PABS boot flash	Write-protect PABS boot flash	OFF	JB5

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Table A.39: RTM SW2–SW18 Functions (Continued)

RTM Switch	Silkscreen Label	ON	OFF	Default	AV8 Jumper
SW17	SOFT_JUMP0	The SOFT_JUMP0 and SOFT_JUMP1 switches on the RTM (which correspond to jumpers JB2 and JB3, respectively) are software readable, and can be used by software programs to branch logic in any way desirable by the programmer. These settings have no effect unless they are assigned a specific meaning or decision choice within a program.		OFF	JB2
SW18	SOFT_JUMP1			OFF	JB3

Cross Reference

See the *Software User's Manual, VPX6-460 BIOS*, document number 826450, for additional information describing the various boot modes and the operation of the SW0 and SW1 software jumpers. Jumper settings may be viewed using the BSP; refer to "sysBoardInfoShow()" and "sysJumperStateGet()" in the Software User's Manual, CHAMP-AV8 VxWorks BSP & Driver Suite, document number 826452, or in the Software User's Manual, CHAMP-AV8 Linux BSP & Driver Suite, document number 826449.

Caution

The SW16 switch is intended for factory use only, and as such should be left in the Off position, to avoid over-writing the contents of the PABS.

Note

Referring to Table A.39, when an RTM switch has a corresponding CHAMP-AV8 on-board jumper, either can affect the function. If either the switch is ON (closed) or the jumper is INSTALLED, or both, the non-default setting is selected.

Note

The NVMRO switch on the CHAMP-AV8's RTM has the opposite polarity when compared to the VITA 46 Specification. In other words, according to the VITA 46 spec, when a NVMRO jumper is installed (or the switch is closed), the non-volatile memories are write protected. On the CHAMP-AV8, when SW12 is closed the non-volatile memories are writable.

RTM Reset Pushbutton (SW1)

Mounted on the RTM face plate, SW1 is a normally-open, momentary contact switch used to reset the CHAMP-AV8. The other PWB-mounted switches (see Table A.39 on page A-57) are toggle switches that will stay in the position set.

REAR TRANSITION MODULE (RTM) PWB HEADER CONNECTORS

As seen in Figure A.19 on page A-53, the RTM PWB provides a group of headers on the PWB, numbered JB1 through JB8. These headers provide (for example) access to the Discrete I/O (DIO), PMC I/O, XMC I/O. With the increased accessibility afforded by the RTM, these interfaces become available for probing, wire-wrapping or attaching a cable for debug, as well as connections to other parts of the system.

Table A.40: RTM Header Functions

Header Number	Description
J7	XMC Differential I/O
JB2	XMC Site PMC I/O
JB6	XMC Single-Ended I/O

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Table A.40: RTM Header Functions (Continued)

Header Number	Description
JB7	PM Bus header (factory-use only)
JB8	FPGA PROM programming header (factory-use only)
P1	Back-up Boot Flash (PABS) programming header (factory use only)
P2	Back-up Boot Flash (PABS) programming header (factory use only)
P3	EIA-232 Serial Port loopback controls—see Figure A.19 on page A-53 for details.
P4	Discrete IO (DIO) Data 8:15
P5	Discrete IO (DIO) Data 0:7
P6	Reserved
P7	Front Panel Port Expander option (future upgrade)
P10	JTAG programming header (factory use only)
P11	JTAG programming header (factory use only)
P12	V46.0 Geographical Addressing Signals
P13	Node A1 IDC-10 serial ports (AT-Everex standard)
P14	Node B1 IDC-10 serial ports (AT-Everex standard)
P15	SATA re-drivers Transmit and Receive signal strength adjustment.



Note

Headers indicated as "Factory use only" are not intended for use in the field. Field operations are not supported. All Headers and their functions are listed for completeness.

RTM JB2 PMC I/O Header Pin Assignments

The CHAMP-AV8 PMC I/O (J14 on the CHAMP-AV8 board) is mapped to the RTM JB2 header as shown below in Table A.41.

Table A.41: RTM PMC I/O (JB2) Pin Assignments

PMC J14 Pin (Odd Numbers)	JB2 Pin	JB2 Pin	PMC J14 Pin (Even Numbers)
PMC_01	1	2	PMC_02
PMC_03	3	4	PMC_04
PMC_05	5	6	PMC_06
PMC_07	7	8	PMC_08
PMC_09	9	10	PMC_10
PMC_11	11	12	PMC_12
PMC_13	13	14	PMC_14

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Table A.41: RTM PMC I/O (JB2) Pin Assignments (Continued)

PMC J14 Pin (Odd Numbers)	JB2 Pin	JB2 Pin	PMC J14 Pin (Even Numbers)
PMC_15	15	16	PMC_16
PMC_17	17	18	PMC_18
PMC_19	19	20	PMC_20
PMC_21	21	22	PMC_22
PMC_23	23	24	PMC_24
PMC_25	25	26	PMC_26
PMC_27	27	28	PMC_28
PMC_29	29	30	PMC_30
PMC_31	31	32	PMC_32
PMC_33	33	34	PMC_34
PMC_35	35	36	PMC_36
PMC_37	37	38	PMC_38
PMC_39	39	40	PMC_40
PMC_41	41	42	PMC_42
PMC_43	43	44	PMC_44
PMC_45	45	46	PMC_46
PMC_47	47	48	PMC_48
PMC_49	49	50	PMC_50
PMC_51	51	52	PMC_52
PMC_53	53	54	PMC_54
PMC_55	55	56	PMC_56
PMC_57	57	58	PMC_58
PMC_59	59	60	PMC_60
PMC_61	61	62	PMC_62
PMC_63	63	64	PMC_64

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RTM P4 and P5 Discrete I/O (DIO) Header Pin Assignments

The CHAMP-AV8 Discrete I/O (DIO) signals are mapped to the RTM P4 and P5 headers as shown below in Table A.42. DIO[0:7] are routed as single ended signals, while DIO[8:15] are routed as differential I/O.

Table A.42: RTM Discrete I/O (P4, P5) Pin Assignments

DIO[0:7] Signals	P4 Pin	P5 Pin	DIO[8:15] Signals
DIO0	2	2	DIO8
DIO1	4	4	DIO9
DIO2	6	6	DIO10
DIO3	8	8	DIO11
DIO4	10	10	DIO12
DIO5	12	12	DIO13
DIO6	14	14	DIO14
DIO7	16	16	DIO15
GND	1, 3, 5, 7, 9, 11, 15	1, 3, 5, 7, 9, 11, 15	GND

RTM P12 Geographical Addressing Header Pin Assignments

On the CHAMP-AV8, the VITA 46 Geographical Addressing pins are routed to the CF-FPGA, so that the CHAMP-AV8 can determine which slot it is in. These pins are also mapped to the P12 header on the RTM.

Table A.43: RTM Geographical Address (P12) Pin Assignments

Signal Name	P12 Pin	P12 Pin	Signal Name
GA0_L	1	2	GND
GA1_L	3	4	GND
GA2_L	5	6	GND
GA3_L	7	8	GND
GA4_L	9	10	GND
GAP_L	11	12	GND

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RTM JB6 Single Ended XMC I/O Signals

On the CHAMP-AV8, the XMC Site Single-Ended User I/O signals are mapped to the RTM JB6 connector as shown below in Table A.44.

Table A.44: XMC Single Ended I/O (JB6) Pin Assignments

Signal Name	JB6 Pin	JB6 Pin	Signal Name
XMC_C01	1	2	XMC_F01
XMC_C02	3	4	XMC_F02
XMC_C03	5	6	XMC_F03
XMC_C04	7	8	XMC_F04
XMC_C05	9	10	XMC_F05
XMC_C06	11	12	XMC_F06
XMC_C07	13	14	XMC_F07
XMC_C08	15	16	XMC_F08
XMC_C09	17	18	XMC_F09
XMC_C10	19	20	XMC_F10
XMC_C11	21	22	XMC_F11
XMC_C12	23	24	XMC_F12
XMC_C13	25	26	XMC_F13
XMC_C14	27	28	XMC_F14
XMC_C15	29	30	XMC_F15
XMC_C16	31	32	XMC_F16
XMC_C17	33	34	XMC_F17
XMC_C18	35	36	XMC_F18
XMC_C19	37	38	XMC_F19
GND	39	40	GND

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RTM J7 Connector Assignments

On the CHAMP-AV8, the XMC Site Differential User I/O signals are mapped to the RTM J7 connector as shown below in Table A.45.

Table A.45: RTM XMC Differential User I/O (J7) Pin Assignments

Signal Name	J13 Pin	J13 Pin	Signal Name
XMC_DP0_P	1	2	XMC_DP10_P
XMC_DP0_N	3	4	XMC_DP10_N
XMC_DP1_P	5	6	XMC_DP11_P
XMC_DP1_N	7	8	XMC_DP11_N
XMC_DP2_P	9	10	XMC_DP12_P
XMC_DP2_N	11	12	XMC_DP12_N
XMC_DP3_P	13	14	XMC_DP13_P
XMC_DP3_N	15	16	XMC_DP13_N
XMC_DP4_P	17	18	XMC_DP14_P
XMC_DP4_N	19	20	XMC_DP14_N
XMC_DP5_P	21	22	XMC_DP15_P
XMC_DP5_N	23	24	XMC_DP15_N
XMC_DP6_P	25	26	XMC_DP16_P
XMC_DP6_N	27	28	XMC_DP16_N
XMC_DP7_P	29	30	XMC_DP17_P
XMC_DP7_N	31	32	XMC_DP17_N
XMC_DP8_P	33	34	XMC_DP18_P
XMC_DP8_N	35	36	XMC_DP18_N
XMC_DP9_P	37	38	XMC_DP19_P
XMC_DP9_N	39	40	XMC_DP19_N
N/C	41	42	N/C
N/C	43	44	N/C
N/C	45	46	N/C
N/C	47	48	N/C
N/C	49	50	N/C
N/C	51	52	N/C
N/C	53	54	N/C
N/C	55	56	N/C
GND	57	58	GND
GND	59	60	GND
GND	61	62	GND
GND	63	64	GND

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B

STATEMENT OF MEMORY VOLATILITY

IN THIS APPENDIX

This appendix contains the Curtiss-Wright Statement of Memory Volatility found in the following section:

- "CHAMP-AV8 Statement of Volatility" on page B-2

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CHAMP-AV8 STATEMENT OF VOLATILITY

The CHAMP-AV8 product contains different types of memory devices. This includes the volatile DDR3 (main memory) and several types of non-volatile memory devices. All CPU-accessible non-volatile memory devices may be write-protected by the installation of jumpers (or wire-wrapping of jumper posts), which are provided for this purpose.



Note

There are no battery-backed memories on the CHAMP-AV8.

The following Table B.1 describes all of the memory devices on the CHAMP-AV8 board and their associated procedures for write-protection and scrubbing. "RTM" refers to the CHAMP-AV8 Rear Transition Module, Curtiss-Wright part number RTM6-462-000.



Note

There are a number of ICs that contain non-volatile memory and are not accessible to either of the CPUs. These are typically treated as hardware configuration items (i.e., on-board power supply settings). These settings are included in the table for the sake of completeness. However, in normal use a user cannot write data to these devices.

Table B.1: Memory Devices Available On The CHAMP-AV8

Memory Type	Size	Volatility	Function	Accessible from CPU	Write-protection (Note 1)	Process to Clear
SDRAM DDR3	4 GB/CPU	Volatile	Main SDRAM for the processors.	Yes	None	Remove Power
NVRAM	256 KB	Non-volatile	NVRAM is for user application storage. It behaves as an SRAM, but retains its contents after power is removed	Yes	The memory is protected if jumper (or wire-wrap) JB6 is installed. **(Note 2)** **RTM SW12 must be Off**	See procedure in BIOS User's Manual, Curtiss Wright document 826450; Chapter 3, section "Scrub" on p. 4-8
BIOS SPI Flash	8 MB/CPU on boards with i7-2715QE 16 MB/CPU on boards with i7-3612QE	Non-volatile	Contains 1st level boot loading code and BIOS code.	Yes	The memory is protected if jumper (or wire-wrap) JB7 is installed. **RTM SW12 must be Off**	See procedure in BIOS User's Manual, Curtiss Wright document 826450; Chapter 3, section "Scrub" on p. 4-8

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Table B.1: Memory Devices Available On The CHAMP-AV8 (Continued)

Memory Type	Size	Volatility	Function	Accessible from CPU	Write-protection (Note 1)	Process to Clear
PABS SPI Flash	8 MB/CPU on boards with i7-2715QE 16 MB/CPU on boards with i7-3612QE	Non-volatile	Backup copy of the BIOS SPI Flash. Note: this boot flash device is intended for board recovery. Therefore, scrub is not supported. Curtiss-Wright recommends leaving the PABS flash write protected at all times.	Yes	The memory is protected if jumper (or wire-wrap) JB5 is NOT installed. RTM does not affect.	None
NAND Flash	8 GB/CPU	Non-volatile	Solid State Drive (SSD) used to store OS and Application code	Yes	The memory is protected if jumper (or wire-wrap) JB1 is installed. **RTM SW12 must be Off**	See procedure in BIOS User's Manual, Curtiss Wright document 826450; Chapter 3, section "Scrub" on p. 4-8.
CPLD	512 cells	Non-volatile	Internal logic device. This is programmed during manufacture. It is only accessible via special purpose hardware. Note: reprogramming would render card inoperable.	No	None	None
PSU controller NVRAM ZL2008 (Qty 12)	<1K	Non-volatile	Controls CPU PSU settings. This can only be written with external special purpose hardware	No	None	None
PSU controller NVRAM ZL2106 (Qty 3)	<1K	Non-volatile	Controls CPU PSU settings. This can only be written with external special purpose hardware	No	None	None
Xilinx PROM	32 Mbit	Non-volatile	Contains bit-stream for the Core Functions FPGA	Yes	The memory is protected if jumper (or wire-wrap) JB4 is NOT installed. **RTM SW12 must be Off** **Backplane NVRMO signal must be logic High.**	None
Serial EEPROM (6 devices)	512 kbit	Non-volatile	Configuration settings for PCIe switch, SRIO switch, and PCIe/SRIO bridges	Yes	The memory is protected if jumper (or wire-wrap) JB4 is NOT installed.	None

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Table B.1: Memory Devices Available On The CHAMP-AV8 (Continued)

Memory Type	Size	Volatility	Function	Accessible from CPU	Write-protection (Note 1)	Process to Clear
Serial Flash (4 devices)	4 Mbit	Non-volatile	Contains configuration settings for the 82574 Ethernet controllers	Yes	The memory is protected if jumper (or wire-wrap) JB4 is NOT installed. **RTM SW12 must be Off** **Backplane NVRMO signal must be logic High.**	None
EEPROM Dip Switch	24 bits	Non-volatile	Board configuration	Yes	The memory is protected if jumper (or wire-wrap) JB4 is NOT installed. **RTM SW12 must be Off** **Backplane NVRMO signal must be logic high**	None
DDR3 SPD EEPROM (4 devices)	4 kbit	Non-volatile	Contains DDR3 configuration settings	Yes	The memory is protected if jumper (or wire-wrap) JB4 is NOT installed. **RTM SW12 must be Off** **Backplane NVRMO signal must be logic High**	None

Table Note 1: The memory is write-protected if the stated condition is met.
Table Note 2: A software procedure must be performed to initiate the configuration before the jumper setting can take affect.

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C

MEMORY WRITE PROTECTION

IN THIS APPENDIX

This appendix provides clarifying information and procedures for hardware memory write protection. It discusses the following topics:

- "NVRAM Write Protection" on page C-2
- "BIOS SPI Flash Write Protection" on page C-3
- "On-Board SATA (NAND) Flash Write Protection" on page C-4

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NVRAM WRITE PROTECTION

Early versions of the CHAMP-AV8 BIOS and BSPs stored vital product data, or VPD, such as board serial number and similar information, in a memory block of the NVRAM. This required the NVRAM write protection mechanism to write-protect the block containing the VPD by default. The NVRAM hardware write-protect applied only to this block and not the entire device memory. A software script was required to modify the Hardware Write Protect jumper behaviour such that when installed, the entire NVRAM is write-protected.

Starting with BIOS version 1.0.2, Linux version 1.0.2, and VxWorks version 1.0.1, VPD relocation to one of the TSI721 SRIO-PCIe bridge configuration PROMs is supported. BIOS version 1.0.2 modifies the NVRAM write-protect mechanism such that the Hardware Write Protect jumper automatically protects the entire NVRAM, not just the VPD-reserved block. This change is made, even if the VPD is not moved from the NVRAM according to the procedure referenced below.

CHAMP-AV8 early access boards with part number VPX6-462-A04B130-E were shipped with software storing VPD in the NVRAM. Users are strongly encouraged to upgrade their BIOS and BSP to the latest versions, following the procedure in the BIOS release note, Curtiss-Wright document 82645 version 4 or later, to migrate VPD to the TSI721 configuration PROM. This will free up user memory space within the NVRAM and allow for full hardware write-protect without the need for software scripts.

All product-grade CHAMP-AV8 boards are shipped with VPD in a TSI721 device, and not in the NVRAM. By default, the hardware write-protect applies to the entire NVRAM (with part numbers of the form VPX6-462-xxxxxxx, having no -E suffix), and not just one block. The migration procedure referenced above is not required.

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BIOS SPI FLASH WRITE PROTECTION

Upon boot, the BIOS attempts to write to certain blocks of its Boot Flash, per normal BIOS boot algorithms. When write-protected, the BIOS still attempts these writes to memory. When read-backs show the write is unsuccessful, the BIOS continues to attempt further writes. Eventually, the process will time out and the BIOS boot continues. Boot time increases by tens of seconds when the Boot Flash is fully write-protected.

If the BIOS had not previously booted, for instance, when the BIOS Flash has been reprogrammed, the BIOS will not complete the boot process with the Hardware Write-Protect jumper in place. Ensure the Hardware Write-Protect jumper is not installed during the first boot after BIOS Flash reprogramming.

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ON-BOARD SATA (NAND) FLASH WRITE PROTECTION

Linux, as a part of its basic configuration, caches its file system. When cached, it has been observed that a write-protected SATA Flash may appear to delete a file. Once the file system has been made coherent with the NAND Flash, the "deleted" file will be seen to still be present.

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