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VME Optical Switch
Hardware Reference Manual

Document No. F-T-MR-L3VMEOSW-A-0-A1



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CE

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

The purpose of this manual is to describe the LinkXchange VME Optical Switch and to guide you through the process of unpacking, setup, and operation.

1.1.2 Scope

The information in this manual is intended for information systems personnel, systems coordinators, or highly skilled network users.

1.1.3 Style Conventions

- Hexadecimal values are written with a "0x" prefix. For example, 0x7e

1.2 Related Information

The following documents are referred to in this specification.

- ANSI/VITA 1-1994 American National Standard for VME64 (supersedes VME Specification Revision C.1, IEEE 1014-1987), VITA, 4/10/1995.
- VITA 1.1-199x VME64 Extensions Draft Standard (Draft 2.0), VITA, 9/5/1997.
- Systran Corp. - www.systran.com

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Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

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Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: support@systran.com
- Fax: (937) 252-1349
- World Wide Web address: www.systran.com

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To learn more about Systran products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

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- E-mail: info@systran.com
- World Wide Web address: www.systran.com

2. PRODUCT OVERVIEW

2.1 Overview

The LinkXchange VME Optical Switch is a 6U VME64X card, containing an 8x8 Photonic Switch. The LinkXchange VME Optical Switch provides non-blocking optical switching over a singlemode fiber-optic network. Using Micro-electromechanical systems (MEMS) technology, the Photonic Switch is capable of connecting up to eight point-to-point simultaneous fully optical connections out of sixty-four possibilities. No conversion of the lightwave takes place on the card; the signal is directed to a single port on the opposite plane. The card supports a range of wavelengths from 1290 nm to 1610 nm.

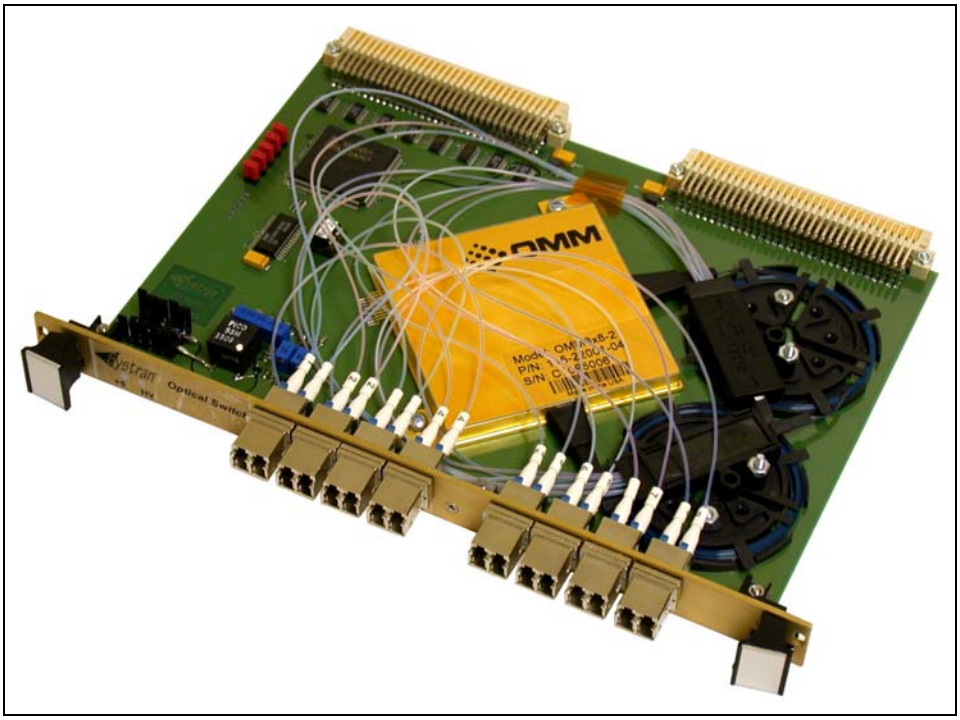


Figure 2-1 LinkXchange VME Optical Switch

2.2 VME Optical Switch Components

The LinkXchange VME Optical Switch is comprised of the following elements (the item number corresponds to the elements shown in Figure 2-2)

❶ Host VME64X interface
❷ Control & Status block, which houses the card configuration registers, providing direct control of the optical switch and configuration memory
❸ 8x8 non-blocking optical switch, which allows up to eight simultaneous point-to-point single mode optical connections out of sixty-four possible connections.
❹ Sixteen LC fiber connections in the VME faceplate: Eight connectors for each of the two optical planes

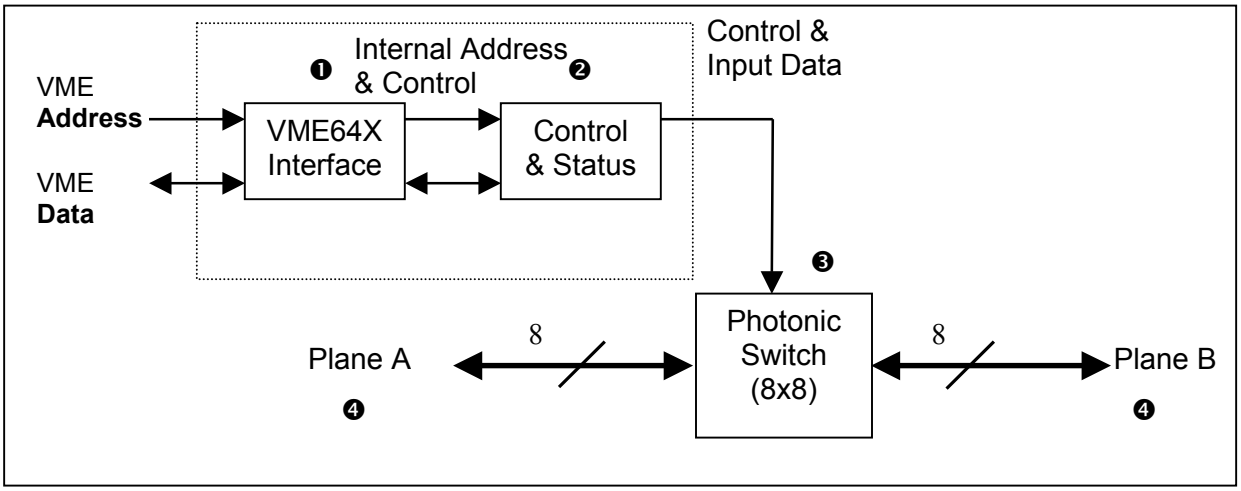


Figure 2-2 Block Diagram

2.2.1 VME64X Interface

The card design is based on the 6U VME64X form factor. Control of this card is accomplished via the VME interface by reading/writing to a set of card configuration registers: Setup, Switch (Photonic) Write, Switch (Photonic) Read, and Alarm. A[16] addressing and DO[8] data VME modes are recognized by the LinkXchange card.

2.2.2 Control and Status

The "Control & Status" block contains the control logic and card configuration registers.

The Setup register is an 8-bit R/W register that is used to set which VME IRQ signal is activated when an alarm is detected on the card. Available signals include IRQ1 to IRQ7. Setting the value to "000" disables the interrupt request. Additionally, a "Configure-On-Boot" (COB) option, and an immediate "Optical Switch Enable" (OEN) are also included. The COB option will enable the stored switch configuration after a reset or a power loss condition. When set, the OEN bit forces a load and enable of Photonic Switch with the configuration data that is in the internal serial-switch register.

The Switch Read/Write registers are comprised of two sets of eight 8-bit registers, one for setting the configuration (write) and one for read-back (read). In each of the registers, a bit corresponds to a particular mirror in the Photonic Switch. By setting this bit in the write register, the matching mirror will connect a designated port of (Optical) Plane A to a port of (Optical) Plane B.

A read-only Alarm register is provided for detection of improper high voltage levels and invalid switch configurations.

The high-voltage alarms indicate whether an overvoltage or an undervoltage situation has occurred.

An invalid switch configuration is detected when attempting to enable an invalid configuration in the switch. The new configuration **will not** be enabled, since the enable signal is disabled until the alarm is cleared. The Photonic Switch will remain in the previous configuration until a valid configuration is enabled.

CAUTION: Detection of an invalid high-voltage level will not cut off power to the Photonic Switch. It is advisable to use the VME IRQs in conjunction with the alarms to alert to such a condition.

2.2.3 8x8 Optical Switch

The heart of the LinkXchange VME Optical Switch is the MEMS 8x8 Photonic Switch. It is capable of supporting up to eight simultaneous point-to-point fully optical connections over singlemode fiber. There are sixty-four possible connection combinations supported by the card.

The Photonic Switch supports wavelengths of 1290 nm to 1610 nm over singlemode fibers with relatively low losses (less than 3 dB).

2.2.4 LC-LC Front Panel Interface

The optical interface to the Photonic Switch is a series of female LC jacks that are placed in the VME front panel as shown in Figure 2-3.

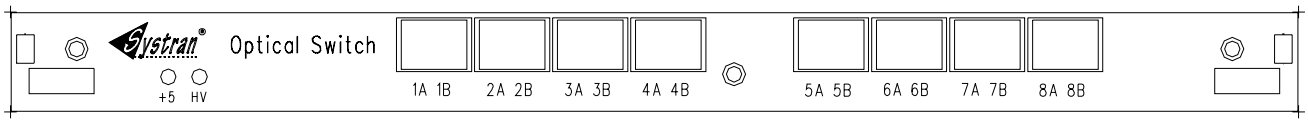


Figure 2-3 Front Panel Faceplate

2.3 Hardware Features

The LinkXchange VME Optical Switch card has the following hardware features:

- 6U VME64X form factor
- VME Slave
- Recognizes A[16] addressing and DO[8] data modes
- Non-blocking Photonic Switching capability
- 8x8 Point-to-Point Optical Switching Capability between Plane A and Plane B
- LC connections provided in VME Front Panel, eight for Plane A and eight for Plane B
- Product supports wavelengths of 1290 nm to 1610 nm
- Automatic Photonic Switch re-configuration from last stored configuration on power up from non-volatile memory (less than 11 ms), after VME reset deactivates.
- Front panel provides “+5V” Power OK and “HV” Power OK status indicators (See Figure 2-3).

2.4 LinkXchange VME Optical Switch Card Interfaces

The LinkXchange VME Optical Switch card consists of the following interfaces:

- A VME64X bus interface used for communication with a host computer.
- A series of Optical Fiber connectors (LC) used for communication with other fiber-optic devices.

2.4.1 VME Bus Interface

The LinkXchange VME Optical Switch card provides the following VME Bus interface features:

- Implemented using a Xilinx FPGA chip
- A[16] and DO[8] Slave capable
- Card base address space by five jumpers
- Configurable IRQ level (0 – 7, via setup register) – Default is 0

2.4.2 LC Fiber Interface

The LinkXchange VME Optical Switch card provides eight singlemode LC connections as interfaces to each of Plane A and Plane B with the following features per channel:

- Protocol Transparent
- Non-blocking
- Long wavelength (1290 nm – 1610 nm wavelengths)
- Typical optical power loss through the board, LC of Plane A to LC of Plane B is less than 3 dB

2.5 Topologies

The LinkXchange VME Optical Switch card is capable of operating in several topologies:

- Point-to-Point
- Arbitrated Loop
- Switch

2.5.1 Point-to-Point Connection

The LinkXchange VME Optical Switch is capable of supporting point-to-point connections as shown in Figure 2-4. Figure 2-5 is an example of multiple optical connections. In the example, multiple channels of a Systran Janus VME card are linked with similar channels of another card.

The ports of the LinkXchange Optical Switch are bi-directional. Therefore, the Photonic Switch may be configured in a variety of ways, as long as one port of Plane A connects with one port of Plane B. A point-to-point connection to multiple optical devices is shown in Figure 2-4. The Photonic Switch is totally non-blocking and will not delay the signal in any way.

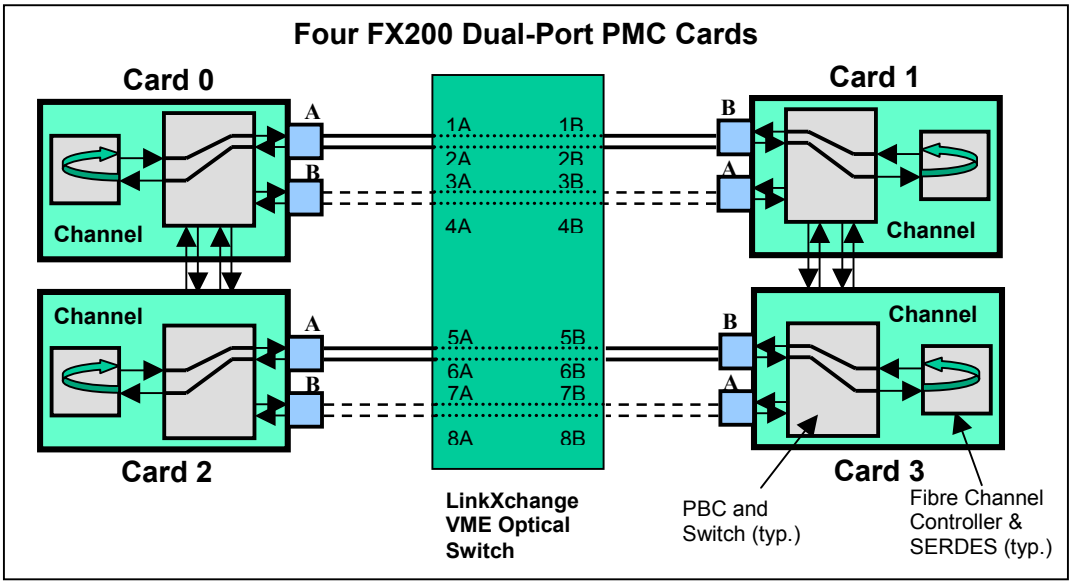


Figure 2-4 Point-to-Point Topology

2.5.2 Arbitrated Loop

Figure 2-5 is a depiction of a possible configuration of a LinkXchange VME Optical Switch in an arbitrated loop topology. Four node loops are created using the LinkXchange VME Optical Switch. Any port may be used in this configuration as long as any one port of Plane A is connected to only one port of Plane B of the Photonic Switch.

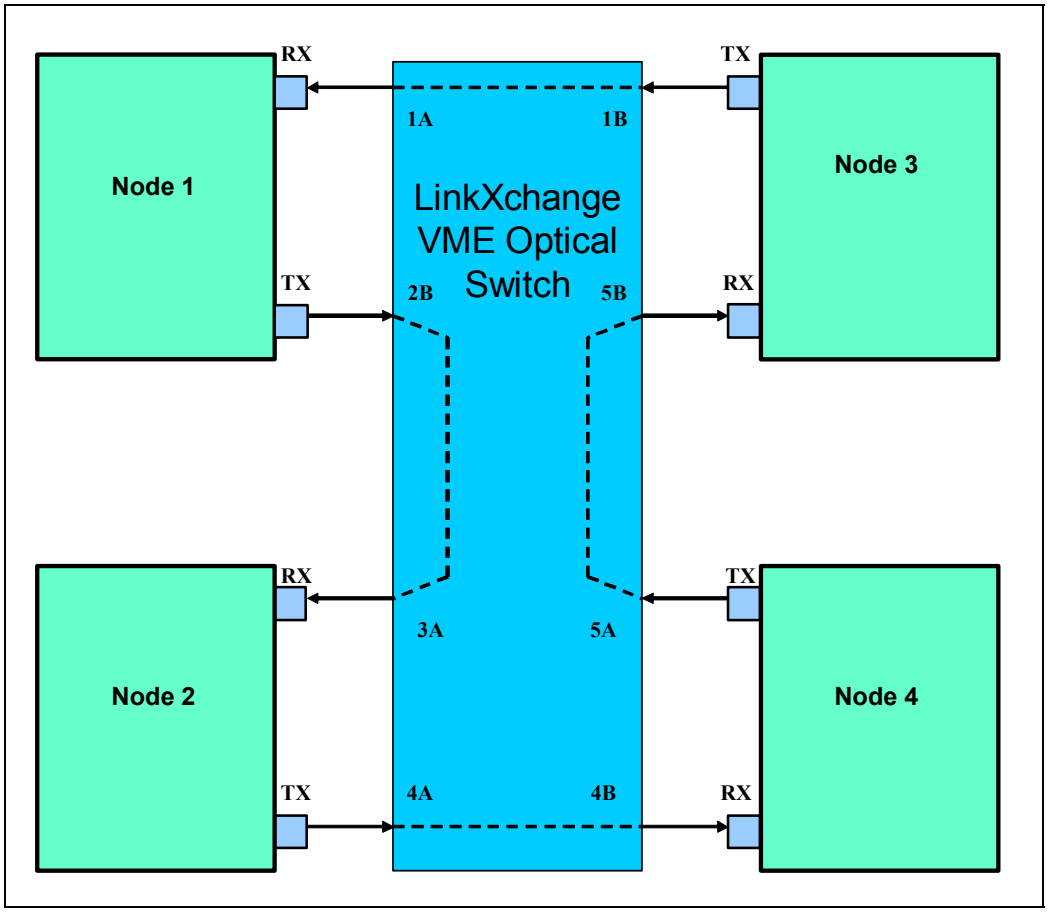


Figure 2-5 Arbitrated Loop with Four Nodes

2.5.3 Switch Topology

The LinkXchange VME Optical Switch can also be configured in a switch topology. Figure 2-6 shows two independent nodes using the LinkXchange card to connect them with a switch fabric.

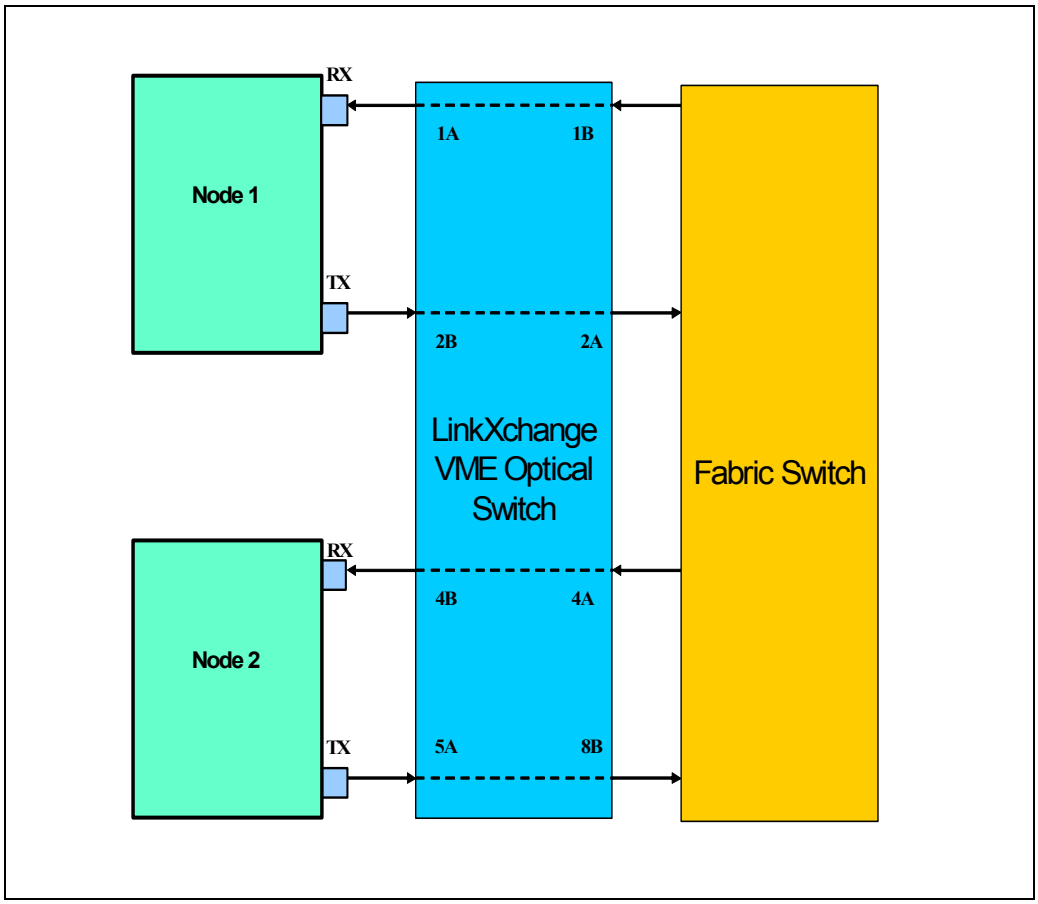


Figure 2-6 Switch Topology

2.6 Accessories

Systran offers Fiber-optic cables as an accessory for the LinkXchange VME Optical Switch card.

2.6.1 Cables

Long Wavelength singlemode Fiber-optical cable is available to support the desired LinkXchange VME Optical Switch Card fiber-optic physical media interface.

Call Systran's Customer Support at (800) 252-5601 or visit www.systran.com for additional information.

2.7 Functional Description

The LinkXchange VME Optical Switch Card provides the functional elements described in Section 2.2. These elements are described in more detail below.

2.7.1 VME64X Interface

The VME64X interface consists of VME64X connectors and Xilinx FPGA used as a VME Controller. The J1 and J2 VME connectors provide the electrical and mechanical interface to the VME bus for the LinkXchange VME Optical Switch Card. Refer to the American National Standard for VME64 and the American National Standard for VME64 Extensions for more information.

2.7.2 Control and Status

The Control and Status section of the LinkXchange VME Optical Switch card is comprised of several elements, which include the Xilinx FPGA, Non-volatile memory, VME Buffers, high-voltage monitoring circuit, and +5/HV indicators.

2.7.3 Xilinx FPGA

The Xilinx FPGA is programmed to serve as a slave VME64X controller for the LinkXchange VME Optical Switch Card. This also handles the interfaces to the non-volatile configuration memory and the Photonic Switch. All the address decoding and other control logic is embedded in this device.

2.7.4 Non-volatile Configuration Memory

A non-volatile SRAM is included in the design to function as the card configuration registers. This memory is comprised of both SRAM and EEPROM technologies, which provides a non-volatile memory solution.

During normal operation, only the SRAM side is utilized. However, during a low-voltage condition, when the power supply falls below 4.0V, the contents of the SRAM will automatically be saved to the EEPROM side within 10ms. This ensures that no information is lost.

When power is restored, the original contents of the card configuration registers will be restored. If the COB bit is set in the Setup register, the stored photonic configuration will be enabled. This is especially useful for automatically restoring the switch connections.

2.7.5 VME Buffers

To isolate and provide the necessary drive, a set of buffer circuits are included between the FPGA and the VME bus.

2.7.6 High Voltage Monitoring Circuit

A high-voltage monitoring circuit is included as part of the design of the card to ensure that the high voltage of the optical switch remains within tolerance. If the high voltage is out of tolerance, the appropriate bit will be set (either HV-H or HV-L) in the alarm register and the HV LED will turn from green to red.

2.7.7 +5/HV Indicators

Two status indicators are included on the front panel of the LinkXchange VME Optical Switch Card; +5V and HV (See Figure 2-7).

When the VME backplane is supplying +5 V to the card and the power circuitry is working properly, the +5 green LED will light up. If this is not on, power to the card should be investigated.

When the high voltage to the Photonic Switch is within tolerance, the HV LED will be green. However, if the high voltage is out of tolerance and +5V is being supplied to the card, the indicator will glow red. If this is the case and +12V (powers the high voltage circuit) is okay, the high-voltage power circuit may be at fault and should be inspected by qualified personnel.

2.7.8 8x8 Photonic Switch

The 8x8 Optical Switch is a MEMS device that provides non-blocking Photonic Switching between the optical planes A and B. Each plane possesses eight ports, where any one port of Plane A may be connected to any one port of plane B. The optical switch is only capable of point-to-point connections through the switch. Control of the switch configuration is accomplished by setting certain bits in the Setup and Switch Read/Write registers.

2.7.9 LC Front Panel Interface

On the VME front panel are sixteen LC connectors that provide interface to the optical switch. Eight are for Plane A and eight are for Plane B (See Figure 2-7).

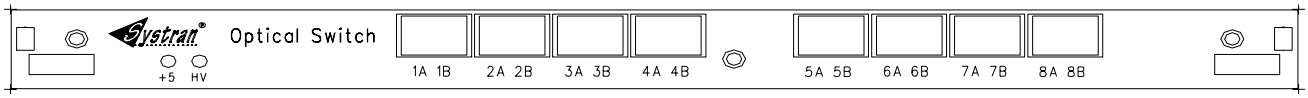


Figure 2-7 Front Panel Faceplate

2.7.10 Voltage Regulation

There are several regulated voltages on the LinkXchange VME Optical Switch described in the following paragraphs.

+5V TO +3.0V PRECISION REGULATORS

The +3.0 V precision regulator provides voltage to the comparator used to monitor the high voltage.

+12 V

The +12 V is used for powering the +130 V circuit for the Photonic Switch.

+130 V

The Photonic Switch requires +130 V ±2% to power the internal mirrors used to switch between the ports. The high side of the +12 V signal is fed directly into an unregulated DC-DC power converter. On the low side of the converter are a 39-Ohm resistor and an NMOS transistor used to turn the circuit on or off.

2.8 System Requirements

The LinkXchange VME Optical Switch cards require only one slot on the host computer backplane, and at least two singlemode LC fiber-optic cable connections (one for Plane A and one for Plane B).

3. INSTALLATION

3.1 Overview

This chapter covers the following:

- Unpacking the switch
- Inspecting the switch
- Configuring the switch
- Installing the switch
- Connecting the cables

3.2 Unpack the Switch



CAUTION: Exercise care regarding the static environment. Use an anti-static mat connected to a wristband when handling or installing the LinkXchange VME Optical Switch. Failure to do this may cause permanent damage to the components on the card.

Follow the steps below to unpack the card:

1. Put on the wristband attached to an anti-static mat.
2. Remove the card and anti-static bag from the carton.
3. Place the bag on the anti-static mat.
4. Open the anti-static bag and remove the card.
5. Retain the original shipping materials in the unlikely event that you should need to return your LinkXchange VME Optical Switch card.

Any optional equipment is shipped in separate cartons.

3.3 Inspect the Switch

If the switch was damaged in shipping, immediately notify Systran Corporation or your supplier.

3.4 Configure the Switch

There are five jumpers on the LinkXchange VME Optical Switch Card as described below.

VME ADDRESS SPACE

The LinkXchange VME Optical Switch card only resides in the A16 address space. The card may reside in any 2048 byte block in the A16 address space.

VME BASE ADDRESS JUMPERS

These jumpers select the VME base address for the LinkXchange VME Optical Switch internal control and status registers. The setting of the VME Address Space determines the definition of these jumpers. The base address jumpers shown in Figure 3-1, labeled J1

through J5, are defined in Table 3-1, where “Not Installed” represents a binary ‘1.’ For example, to set the base address of the board at 0xF000, only jumper J1 must be installed.

Table 3-1 Jumper Definition

Jumper	A16 Space Name	Default Setting
J1	VME_A11	Not installed
J2	VME_A12	Not installed
J3	VME_A13	Not installed
J4	VME_A14	Not installed
J5	VME_A15	Not installed

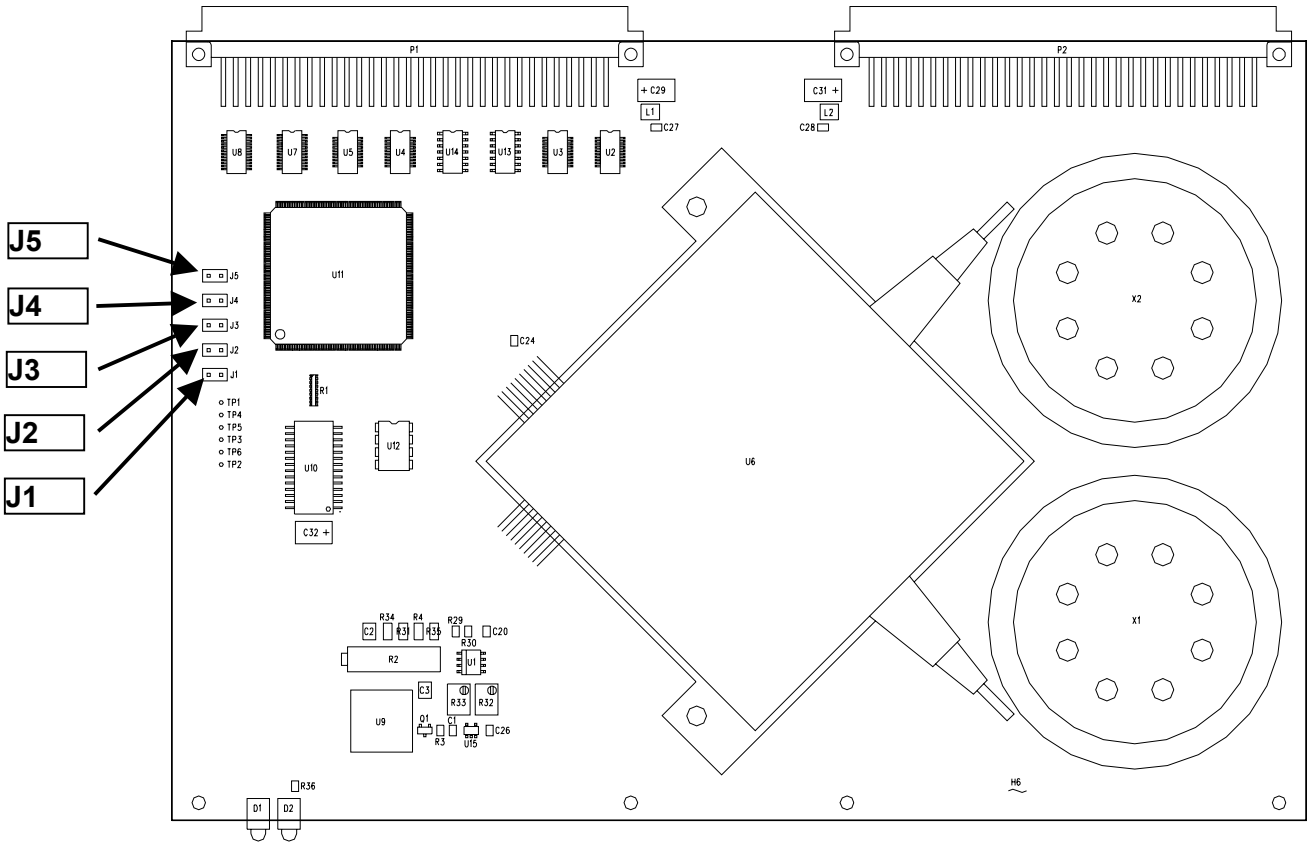


Figure 3-1 LinkXchange VME Optical Switch

3.5 Install the Switch

The LinkXchange VME Optical Switch card occupies one single 6U width VME slot. It is installed as any other VME card would be installed. Ensure that the backplane connectors are fully seated and tighten the screws located at the top and bottom of the front panel.

3.6 Connect the Cables

The typical network communication architecture consists of LinkXchange VME Optical Switch cards connected by fiber-optic cable.

NOTE: The VME Optical Switch is passive. Therefore, the maximum distance between nodes depends on the power budget.

The optional fiber-optic cables may be shipped in a separate carton. Remove the protective caps on the fiber-optic connectors as well as the ones on the fiber-optic cables. These protective caps should be replaced when cables are not in use or in the event the node must be returned to the factory. Attach the fiber-optic cables to the connectors on the LinkXchange VME Optical Switch card. Figure 3-2 and Figure 3-3 depict the types of fiber-optic connectors needed for the LinkXchange VME Optical Switch card.

CAUTION: **Fiber-optic Cable Precautions**

1. Fiber-optic cables that are part of the LinkXchange VME Optical Switch hardware are made of glass and may break if crushed or bent in a loop with a radius of 1 inch or less.
2. Look at the cable ends closely before inserting them into the LC connector. If debris is inserted into the connector, it may not be possible to clean the connector. Hair, dirt, and dust can interfere with the light signal transmission.
3. Use an alcohol-base wipe to clean the cable ends.

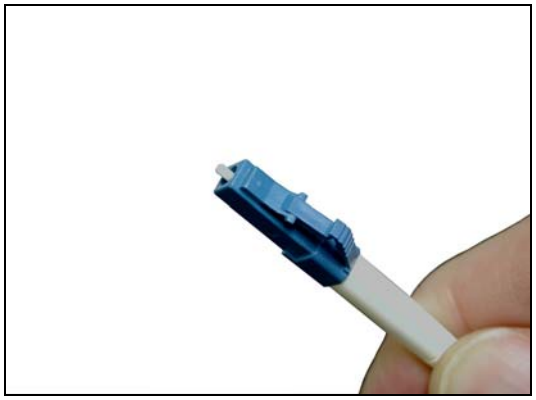


Figure 3-2 Fiber-optic Simplex LC Connector



Figure 3-3 Fiber-optic Duplex LC Connector

3.7 Troubleshooting

If the system does not boot correctly, power-down the system, reseat the card and double-check cable connections. If problems persist, call Systran Customer Support at **(800) 252-5601** for assistance.

Please be prepared to supply the following information:

Host Machine: _____
OS Name: _____
OS Version: _____
Bus Interface: _____
LinkXchange VME Optical Switch S/N: _____
Error Messages: _____
The last action you performed: _____

4. OPERATION

4.1 Overview

This chapter describes how to operate the LinkXchange VME Optical Switch.

4.2 Mode of Operation

The LinkXchange VME Optical Switch card functions as a non-blocking 8x8 crosspoint switch. Configuration of the various registers allows you to switch any one of eight ports on one optical plane to any one of eight ports on the other optical plane. Only a small amount of optical power is lost through the card (less than 3dB).

The Photonic Switch interfaces with the outside world via a set of LC connectors. Labeling for the connectors is such that Port 1 of Plane A would be labeled 1A, Port 4 of Plane B, would be labeled 4B, etc. See Figure 2-7.

4.2.1 Control Interface

Configuration and control of the LinkXchange VME Optical Switch is accomplished via the VME backplane using A16 addressing and DO[8] data modes. Eighteen internal registers are accessible on the LinkXchange VME Optical Switch, which include the Setup (1 Byte), (Optical) Switch Write (8 x 1 byte), Switch Read (8 x 1 byte), and alarm (1 byte).

The switch may be simply accessed either by using a VME debugger or by writing an application for the switch. Some VME system controller cards come with a debugger that is capable of reading and writing to various memory locations in the VME address space and is well suited to control the card.

The other method would be to write a software application, using the information in this section to properly access the card.

4.2.2 VME Access

The LinkXchange VME Optical Switch recognizes the A[16] addressing mode. Any other modes will be ignored. The DO[8] data mode is utilized, where the data bits are placed on D7 down to D0 only. Figure 4-1 shows the relative placement (offsets) of the configuration and control registers of the card.

The card resides in a 2048 bit block in the A[16] address space. Jumpers J1-J5 control where the card can be placed in the address space. See the "VME Base Address Jumpers" section for further details.

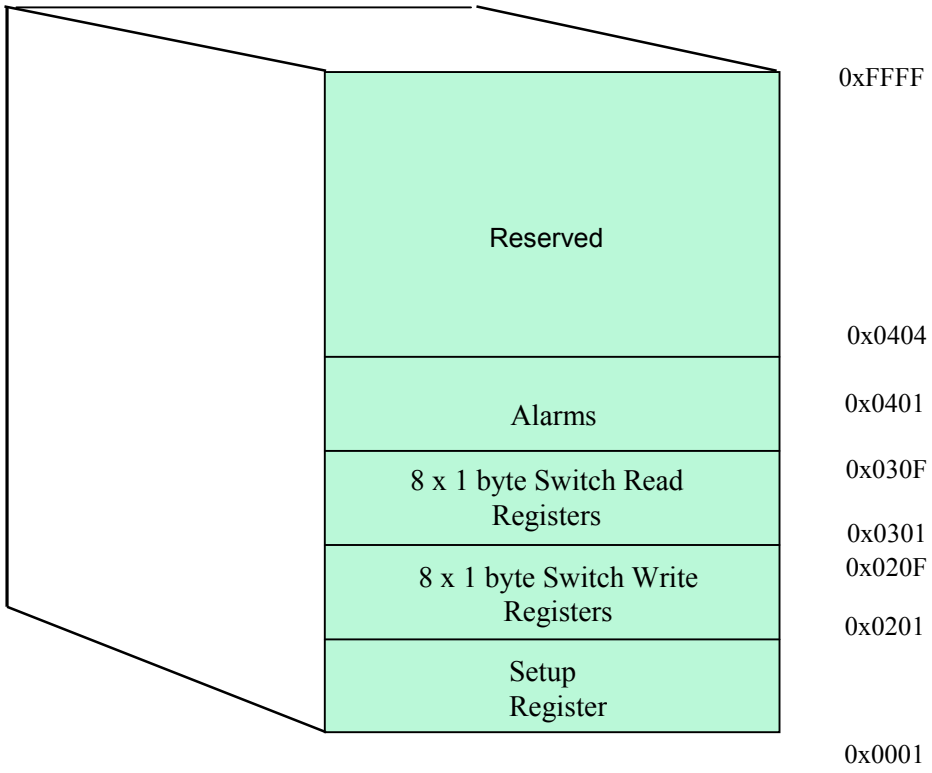


Figure 4-1 A[16] Register Offsets

4.3 Registers

Table 4-1 describes the various configuration registers in the LinkXchange VME Optical Switch card.

4.3.1 LinkXchange VME Optical Switch Register Configuration Terms

COB (Configure Optical Switch on Boot): If this bit is set, the optical switch will load the saved configuration in the NVSRAM after receiving a reset or on power up.

HV-H (High Voltage High): This active high signal indicates that the 130 VDC power source for the Optical Switch is above the maximum.

HV-L (High Voltage Low): This active high signal indicates that the 130 VDC power source for the Optical Switch is below the minimum.

IRQx (Interrupt Request X): These set the appropriate VME interrupt level when an alarm is indicated. A setting of "000" will disable this function.

OEN (Optical Switch Enable): When set, this signal will enable the configuration that has been loaded in the optical switch. Internally, this signal will reset itself to logic zero upon loading the new configuration into the optical switch.

OINV (Optical Switch Configuration is Invalid): When set, this signal indicates that an invalid configuration has been loaded into the switch. Sending an OEN signal while this alarm is active will have no affect.

OSW ("Photonic" Optical Switch)

4.3.2 Setup Register

The Setup register configures several items relating to the IRQ levels and when a switch configuration is enabled. Bits 7-5 control which IRQ level is activated when an alarm is triggered on the card. These correspond to the binary representation of the desired IRQ level. For example, if the IRQ level 3 is desired, the binary bits "011" would be placed in the positions 7-5. If no interrupt request is desired, then write "000" in the register.

When Configure-On-Boot (COB) (bit 3) is set, the stored switch configuration is enabled when the card is reset. The current switch configuration is automatically stored in a non-volatile memory (NVSRAM) when the +5 V power signal drops below +4.0 V for any reason.

When normal power is regained, the stored contents of the Setup and Switch (Read/Write) registers are restored automatically. After the VME reset signal is released, the contents of the Switch Write registers will be serially shifted into the Photonic switch. If the COB bit is set, the switch configuration will be enabled in less than 11ms after the VME reset signal goes high.

When a logic one is written to the Optical Switch Enable Now (OEN) bit in the Setup register, the current switch configuration held in the Switch WriteX registers will be immediately loaded into the switch and enabled. This method would be used during normal operation to enable a new switch configuration.

4.3.3 Switch Write Registers

There are eight 1-byte, Switch Write registers used to load new configurations into the serial shift register, which loads the configuration into the Photonic Switch. The table

relates each of the Switch Write registers to the OSW bits. Refer to Figure 4-2 to see how to connect ports of Plane A to Plane B.

4.3.4 Switch Read Registers

Analogous to the Switch Write registers, are the Switch Read registers. These allow the contents of the internal Switch Write registers to be read.

4.3.5 Alarm Register

An alarm register indicates several different types of internal errors on the card. The HV-H and HV-L are part of the HV level detection circuitry. The High Voltage High (HV-H) signal, when set indicates that the HV is above the acceptable limit. This is also true for the HV-L (High Voltage Low), except that a voltage below the limit is detected. If the VME backplane is providing acceptable +5 V and +12 V power levels, it is advisable to contact Systran Customer Support for assistance (Possible Photonic Switch damage could result from improper +130 V levels).

The OINV (Optical Switch Configuration Invalid) bit, when set, indicates that an invalid configuration has been written to the Photonic Switch. This will not be enabled since it is an invalid configuration. The proper configuration needs to be loaded into the Switch Write registers and then enabled to clear this bit.

Table 4-1 LinkXchange VME Optical Switch Register Configuration

Register	R/W	Offset	7	6	5	4	3	2	1	0
Setup	R/W	0001h	irq2	irq1	irq0	xxxx	COB	xxxx	xxxx	OEN
Switch Write0	W	0201h	Optical Switch Configuration Byte 0						(OSW* Bits 1-8)	
Switch Write1	W	0203h	Optical Switch Configuration Byte 1						(OSW Bits 9-16)	
Switch Write2	W	0205h	Optical Switch Configuration Byte 2						(OSW Bits 17-24)	
Switch Write3	W	0207h	Optical Switch Configuration Byte 3						(OSW Bits 25-32)	
Switch Write4	W	0209h	Optical Switch Configuration Byte 4						(OSW Bits 33-40)	
Switch Write5	W	020Bh	Optical Switch Configuration Byte 5						(OSW Bits 41-48)	
Switch Write6	W	020Dh	Optical Switch Configuration Byte 6						(OSW Bits 49-56)	
Switch Write7	W	020Fh	Optical Switch Configuration Byte 7						(OSW Bits 57-64)	
Switch Read0	R	0301h	Optical Switch Configuration Byte 0						(OSW Bits 1-8)	
Switch Read1	R	0303h	Optical Switch Configuration Byte 1						(OSW Bits 9-16)	
Switch Read2	R	0305h	Optical Switch Configuration Byte 2						(OSW Bits 17-24)	
Switch Read3	R	0307h	Optical Switch Configuration Byte 3						(OSW Bits 25-32)	
Switch Read4	R	0309h	Optical Switch Configuration Byte 4						(OSW Bits 33-40)	
Switch Read5	R	030Bh	Optical Switch Configuration Byte 5						(OSW Bits 41-48)	
Switch Read6	R	030Dh	Optical Switch Configuration Byte 6						(OSW Bits 49-56)	
Switch Read7	R	030Fh	Optical Switch Configuration Byte 7						(OSW Bits 57-64)	
Alarms	R	0401h	HV-H	HV-L	X	X	X	X	OINV	X

* OSW = Optical Switch Module



NOTE: There is no A0 bit In VME. Offsets shown where A0=1 are accessed in VME by setting the proper levels on DS1, DS0, and LWORD.

4.4 Data Format for Switch Register

In order to connect a particular port of Plane A to a port of Plane B, a certain mirror must be actuated. This is accomplished by referring to Figure 4-2. The figure shows the channels 1 through 8 for each of the optical planes. The gold colored (OSW Bit) section indicates what OSW bit should be turned on (logic one) to connect a port of Plane A to a port of Plane B.

For example, to connect channel 1A to 4B, bit 14 must be set to logic one. Thus the Switch Write Register 1 (Offset 0x0203) must have the value 0x04 loaded into it and the Setup Register must have the value 0x01 written to it.

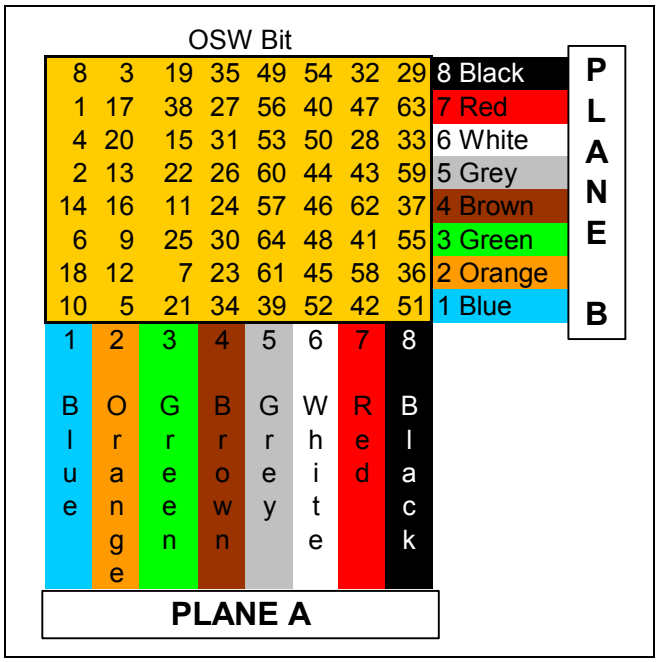


Figure 4-2 OSW Data Bit Matrix

4.5 VME IRQ Response

The LinkXchange VME Optical Switch is capable of generating VME IRQs to indicate that an alarm condition has been detected.

If the Setup register is configured to generate a VME IRQ (See section 4.3.2 for information on how to configure the Setup register), the corresponding interrupt will be placed on the VME bus when an alarm condition has been detected.

When the VME interrupt handler is ready to service the interrupt, it will place the corresponding levels to the IRQ on the lower three address bits (A3-A1). At which time, the LinkXchange VME Optical Switch will place the contents of the alarm register on the data bus. When the data bus has been read, the interrupt handler will release the bus, thus ending the cycle.

4.6 Troubleshooting

Problem	Solutions
No +5 V Light	Check +5 V power to card. If power ok, contact Systran Customer Support.
No HV Light	Check +12 V power to card. If power ok, contact Systran Customer Support.
Red HV Light, HV-H Alarm, or HV-L Alarm	This indicates that the High Voltage circuitry is not functioning. To reduce the chance of damage to the Photonic Switch, immediately remove power and contact Systran Customer Support.
OINV Alarm	This indicates that an attempt to enable an invalid switch configuration occurred. Write a valid configuration to the card and enable.
Cannot Update Switch Configuration	Check if there is an OINV alarm. If so, clear it. Otherwise, call Systran Customer Support.
No signal	Check for power to the card (Is +5 V Green?). Check if the HV LED is green. If not call Systran Customer Support. Check for OINV alarm. If so, clear it. Attempt to switch through another port. If so, a broken fiber or switch is possible. Call Systran Customer Support in either case.
No IRQ activated when an alarm occurs	Check Setup register bits 7-5. If set to “000”, write proper level. Otherwise, call Systran Customer Support.

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APPENDIX A

SPECIFICATIONS

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A.2 Card Dimensions..... A-2

A.1 Hardware Specifications

Hardware Compatibility: .....ANSI/VITA 1-1994 American National Standard for VME64 (supersedes VME Specification Revision C.1, IEEE 1014-1987)
VITA 1.1-199x VME64 Extensions Draft Standard (Draft 2.0)
Product Data Sheet for the OMM8x8 Photonic Switching Subsystem (Proprietary)

Physical Dimensions:.....6.69 x 10.32 inches (169.9 x 262.1 mm) (See Figure A-1)

Weight:.....approximately 1lb 4 oz

Electrical Requirements:.....+5 VDC, 330 mA, 1.650 Watts
+12VDC, 210 mA, 2.520 Watts

Storage Temperature Range:.....-40° to +85°C

Operating Temperature Range:.....+0° to +70°C

Storage Humidity Range:.....0% to 95% (noncondensing)

Operating Humidity Range:.....5% to 90% (noncondensing)

Long Wavelength Range……1290 nm to 1610 nm singlemode

Average Insertion Loss (LC to LC):…..< 3dB

Connector……...Simplex LC

Cable:…….9/125 µm singlemode fiber optic

Mean Time Between Failure (MTBF)	**MIL-HDBK-217F**	**BELLCORE 332**
	221,947 hours	482,828 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

A.2 Card Dimensions

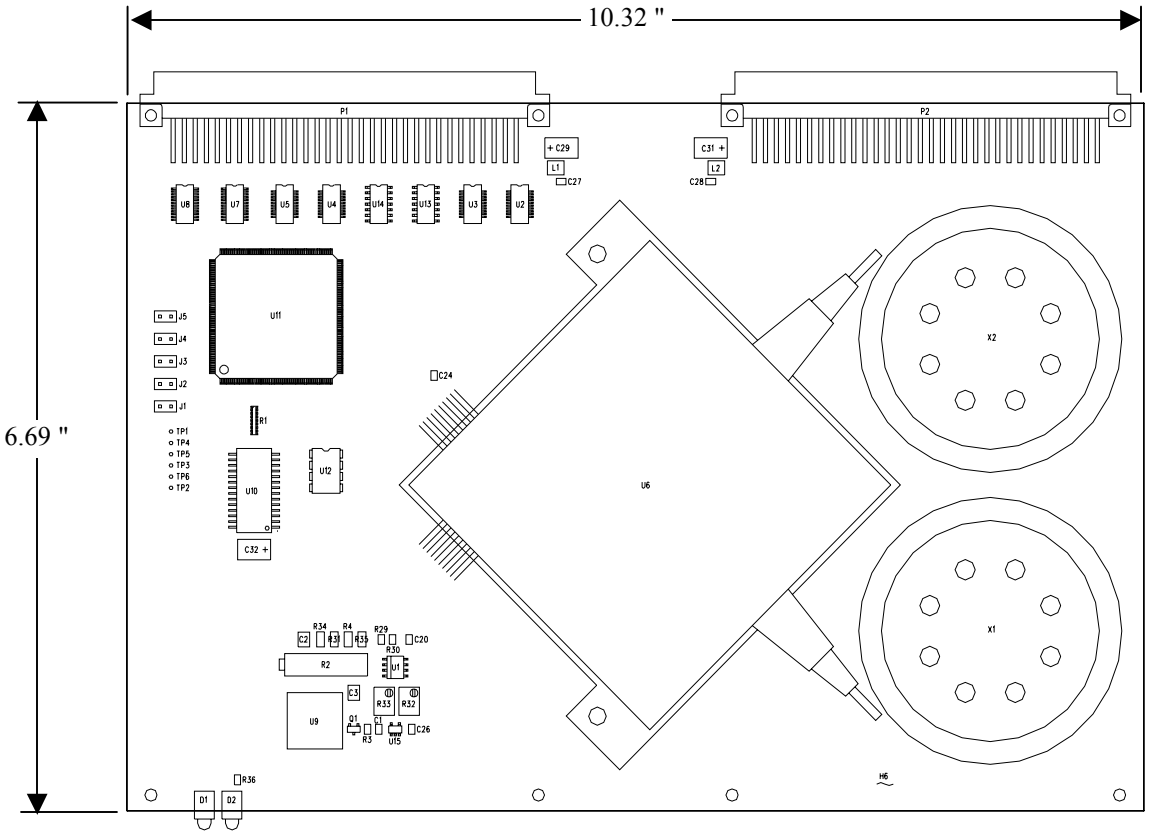


Figure A-1 LinkXchange VME Optical Switch Dimensions

GLOSSARY

1x3 ----------A 3-pin connector for use with copper media.

8B/10B ----------A data-encoding scheme developed by IBM for translating byte-wide data to an encoded 10-bit format.

AAL5----------ATM Adaptation Layer for computer data.

active ----------A term used to denote a port that is receiving a signal.

AL ----------Arbitrated Loop. Fibre Channel topology where L_Ports use arbitration to establish a point-to-point circuit without hubs or switches.

ALPA ----------Arbitrated Loop Physical Address.

ANSI ----------American National Standards Institute.

AP----------Access Point.

API ----------Applications Program Interface.

APID ----------Access Point Identification Number. A number ranging between 0 and 65535 that is assigned by the user to identify a process. All APID's attached to a single FX board must be unique.

ASIC ----------Application Specific Integrated Circuit. An integrated circuit designed to perform a specific function. ASICs are typically made up of several interconnected building blocks and can be quite large and complex.

ATM ----------Asynchronous Transfer Mode. A network technology that transfers data in small 53-byte packets and permits transmission over long distances. Proposed speeds range from 25 Mbps to 622 Mbps.

Auto-Speed Negotiation---------Automatic detection and switching to the appropriate transfer rate. Alternatively, device speed may be fixed at 2Gb/s or 1Gb/s, or configurable through utility.

bandwidth ----------The amount of data that can be transmitted over a channel.

baud ----------A unit of speed in data transmission, usually equal to one bit per second.

Bi-Directional card----------A FibreXtreme Simplex Link card with both source and destination capabilities.

BIOS ----------Basic Input/Output System.

bps ----------bits per second.

broadcast ----------Sending a transmission to all nodes on a network.

BSP ----------Board Support Package. A set of software routines written by the OS vendor or SBC vendor that provides support for a particular SBC.

burst transfers----------Messages are transmitted in a format that includes the initial address followed by all the data. Burst transfers eliminate the need for repeated addresses for each data block, permitting higher throughput.

channel ----------A point-to-point link that transports data from one point to another at the highest speed with the least delay, performing simple error correction in hardware. Channels are hardware intensive and have lower overhead than networks. Channels do not have the burden of station management.

channel network ----------Combines the best attributes of both channel and network, giving high bandwidth, low latency I/O for client server. Performance is measured in transactions per second instead of packets per second.

circuit ----------Bi-directional path allowing communications between two L_Ports.

circuit-switched mode ----------Data transfer through a dedicated connection (Class 1).

CMC ----------Common Mezzanine Card.

communications protocol-------A special sequence of control characters that are exchanged between a computer and a remote terminal in order to establish synchronous communication.

CRC ----------Cyclic Redundancy Check. A code used to check for errors in Fibre Channel.

datagram----------Type of data transfer for Class 3 service. Transfer has no confirmation of receipt and rapid data transmission.

dBm ----------decibels relative to one milliwatt.

destination only card ----------A FibreXtreme Simplex Link card that is only capable of receiving data.

direct connect links ----------An actual physical, dedicated connection between two devices with the entire bandwidth available to serve each direct link. Direct links provide a fast and reliable medium for sending large volumes of data.

DMA ----------Direct Memory Access.

DMA write ----------The DMA engine on the bus controller writes the data from the host computer to the SRAM buffer, freeing the host CPU for other tasks. (FibreXpress board becomes a master for the bus.)

E_Port ----------Element Port. Used to connect fabric elements together.

ECL ----------Emitter Coupled Logic.

ethernet----------A widely used shared networking technology.

exchange ----------One or more sequences for a single operation that are not concurrent, but are grouped together.

F_Port ----------Fabric Port. The access point of the fabric for physically connecting the user's N_Port.

fabric----------A self-managed, active, intelligent switching mechanism that handles routing in Fibre Channel Networks.

fabric elements ----------Another name for ports.

FC----------Fibre Channel.

FC-AL ----------Fibre Channel Arbitrated Loop. Provides a low-cost way to attach multiple ports in a loop without hubs and switches.

FCP----------Fibre Channel Protocol. The mapping of the SCSI communication protocol over Fibre Channel.

FC-PH ----------Fibre Channel Physical interface. Fibre Channel Physical standard, consisting of the three lower levels, FC-0, FC-1, and FC-2.

FCSI----------Fibre Channel Systems Initiative is made up of IBM, Hewlett-Packard and Sun Microsystems. This group strives to advance Fibre Channel as an affordable, high-speed interconnection standard.

FC-SW----------Fibre Channel Switch Fabric standard. Formerly known as FC-XS: Fibre Channel Xpoint Switch. The crosspoint-switched fabric topology is the

highest-performance Fibre Channel fabric, providing a choice of multiple path routings between pairs of F_ports.

Fibre Channel ----------Fibre Channel (FC) is a serial data transfer interface technology operating at speeds up to 1 Gbps. It is defined as an open standard by ANSI. It operates over copper and fiber-optic cabling at distances of up to 10 kilometers. Supported topologies include point-to-point, arbitrated-loop, and fabric switches.

FibreXpress ----------A Systran trademark name for the Fibre Channel family of products.

FibreXtreme ----------A Systran trademark name for the Simplex Link family of products.

FibreXtreme Simplex Link ----A high-speed, point-to-point, communication network capable of transfers in excess of 100 MB/s.

FIFO ----------first in first out

Firmware ----------Microprocessor executable code, typically for embedded type processors.

Flash ----------A type of Electrical Erasable Programmable Read Only Memory (EEPROM). Erased and written to in blocks vs. bytes.

FL_Port ----------Fabric Loop Port. Joins an arbitrated loop to the fabric.

FPDP----------Front Panel Data Port.

frame----------A linear set of transmitted bits that define a basic transport element. A frame is the smallest indivisible packet of data that is sent on the FC.

frame-switched mode----------Data transfer is connectionless (Classes 2 and 3) and data transmission is in frames. The bandwidth is allocated on a link-by-link basis. Frames from same port are independently switched and may take different paths.

FTP application ----------A test application for transferring files from one computer to another.

FX----------FibreXpress.

G_Port----------A port which can function as either an F_Port or an E_Port. Its function is defined at login.

Gbps----------Gigabits per second.

gigabit----------One billion bits, or one thousand megabits.

GLM ----------Gigabit per second Link Module. A Link Module that can be used for optical or copper media.

HANDLE ----------Abstraction for the *Handle* in Windows and *file descriptor* in Unix.

HBA ----------Host Bus Adapter.

HIPPI ----------High Performance Parallel Interface. An 800 Mbps interface to supercomputer networks (previously called high-speed channel) developed by ANSI.

HSSDC2----------High Speed Serial Data Connectors and Cable Assemblies. A type of high-speed interconnect system which allows for transmission of data rates greater than 2.125 Gbps and up to 15 meters.

hunt group----------A group of lines that are linked so that one call to the group will find the line that is free. This provides the ability for more than one port to respond to the same alias address.

I/O ----------Input/Output.

IOCB----------I/O Control Block. A block of information stored in system memory, usually of fixed length, which contains control codes and data. The IOCB is created by a host computer and sent to some other computer. The IOCB contains command/instructions, data, and memory pointers intended to direct the other computer to perform some function.

inactive ----------A term used to denote a port that is not receiving a signal.

intermix ----------A Fibre-Channel-defined mode of service that reserves the full Fibre Channel bandwidth for a dedicated (Class 1) connection, but also allows connectionless (Class 2) traffic to share the link if the bandwidth is available.

IP----------Internet Protocol is a data communications protocol.

IPI ----------Intelligent Peripheral Interface.

insertion delay----------The amount of time the data is delayed for the insertion of FXSL framing protocol. It is measured from when the data becomes available at the FIFO to when the data is actually transmitted on the link. The actual values are either 188 ns in Mode-0 or Mode-1 (with no CRC), or 226 ns in Mode-2 or Mode-3 (with CRC).

KB ----------Kilobytes (binary = 1,024).

kB----------Kilobytes (decimal = 1,000).

L_Port ----------Loop Port. Either an FL_Port or an NL_Port that supports the arbitrated loop topology.

LAN ----------Local Area Network, typically less than 5 kilometers. Transmissions within a LAN are mostly digital, carrying data at rates above 1 Mbps.

latency ----------The delay between the initiation of data transmission and the receipt of data at its destination.

LCF----------Link_Control Facility. Provides logical interface between nodes and the rest of Fibre Channel.

Link Module ----------A mezzanine board mounted on the board to interface between the board and the network.

longword----------32-bit or 4-byte word.

LP----------Lightweight Protocol.

LX1500 ----------LinkXchange LX1500 Crossbar Switch.

LX2500 ----------LinkXchange LX2500 Crossbar Switch.

Mbps ----------Megabits per second.

MBps----------MegaBytes per second.

MB----------MegaBytes.

media----------Means of connecting nodes; either fibre optics, coaxial cable or unshielded twisted pair.

monitor----------An application program used to display the status and change the configuration of the driver.

multicast ----------A single transmission is sent to multiple destination N_ports.

N_Port ----------Node Port. A Fibre-Channel-defined entity at the node end of a link that connects to the fabric via an F-Port.

network----------Connects a group of nodes, providing the protocol that supports interaction among these nodes. Networks are software intensive, and have high overhead. Networks also operate in an environment of unanticipated connections. Networks have a limited ability to provide the I/O bandwidth required by today's applications and client/server architectures.

NL_Port----------Node Loop Port. Joins nodes on an arbitrated loop.

node ----------A host computer and interface board. Each processor, disk array, workstation or any computing device is called a node. Connects to FC through a node port (N_Port).

normal write ----------A host CPU writes data to the SRAM buffer through the bus and bus controller (FibreXpress board operates as a slave of the bus).

ns ----------nanoseconds.

NVRAM----------Non-Volatile Random Access Memory. Generic term for memory that retains its contents when power is turned off.

OFC ----------Open Fibre Control. A safety interlock system used on some FC shortwave links.

operation----------One of Fibre Channel's building blocks composed of one or more exchanges.

out-of-band control ----------On the LinkXchange products, a method of issuing switch commands that does not use any bandwidth of the 32 switch ports.

OSW----------LinkXchange VME Optical Switch module.

PCI----------Peripheral Component Interface.

PIO ----------Programmed Input/Output.

PMC----------PCI Mezzanine Card. Everything that is true for PCI cards is true for PMC except there is a footprint or card format change.

port ----------A physical element through which information passes. It is an electrical or optical interface with a pair of wires or fibers—one each for incoming and outgoing data.

profiles----------Subsets of Fibre Channel standards that improve interoperability and simplify implementation. It is like a cross-section of FC, providing guidelines for implementing a particular application.

protocols ----------Data transmission conventions encompassing timing, control, formatting, and data representation. This set of hardware and software interfaces in a terminal or computer allow it to transmit over a communication network, and these conventions collectively form a communications language.

RISC ----------Reduced Instruction Set Computer. A type of microprocessor that executes a limited number of instructions that typically allows it to run faster than a Complex Instruction Set Computer (CISC).

SAP ----------Service Access Point.

SBC----------Single Board Computer.

SCSI ----------Small Computer System Interface.

sequence----------The unit of transfer, made up of one or more related frames for a single operation.

SFP ----------Small Form-factor Pluggable transceiver modules.

shared connect links ----------The ability to send and receive data without establishing a dedicated physical connection so that other devices can also use the medium. This shared link is more efficient for smaller data transmissions because the overhead of direct connect link is avoided.

SRAM----------Static Random Access Memory.

SRAM Transfer----------Process in which the data is transferred from the host computer to the SRAM buffer by normal or by DMA write.

STP ----------Shielded Twisted Pair. A type of cable media.

striping ----------To multiply bandwidth by using multiple ports in parallel.

switched fabric ----------(see the definition for "fabric").

SYNC ----------FibreXtreme Simplex Link primitive used to synchronize the source and destination cards.

SYNC with DVALID ----------A special case of the SYNC primitive occurring in the middle of a buffer of data.

source only card----------A FibreXtreme Simplex Link card that is only capable of sending data.

TCP----------Transmission Control Protocol.

terminal application ----------A test application that sends characters received from the keyboard and displays received characters.

throughput application ---------An application that tests the throughput for the given system.

time-out----------The time allotted for a native message to travel the network ring and return. If this time is exceeded, an automatic retransmission of the native message occurs.

topology ----------Refers to the order of information flow due to logical and physical arrangement of stations on a network.

ULP----------Upper Level Protocol.

VHDL----------Very high-speed integrated circuit Hardware Description Language.

VME ----------Acronym for VERSA-module Europe: a bus architecture used in some computers.

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