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FibreXtreme

SL100/SL240 Multi-Channel PCIe User Guide

Document No. F-T-MU-S2PCIENF-A-0-A3

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1 FOREWORD

FibreXtreme®

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SL100/SL240 Dual-Port Memory FIFO U.S. Patent #6,259,648.

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4/11/17	Changed references to PCIe lane scaling. PCN 1195	4-3&4-4	A3

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1.1 EMI Statement

EMI Statement

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

This information technology product is not compliant with applicable European Union directives for Information Technology equipment.

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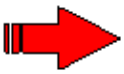
2 INTRODUCTION

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2.1 How to Use This Manual

Purpose

This manual introduces the FibreXtreme SL240 PCI-Express (PCIe) card. It provides guidance through the process of unpacking, setting up, and programming the cards.



NOTE: Both the FibreXtreme SL100 and SL240 hardware are referred to throughout this manual as SL240. The software that supports both the SL100 and SL240 hardware is referred to as SL240, including the driver and API. Anything that is exclusive to the SL100 or the SL240 is described as such.

Scope

This manual contains the following information:

- An introduction to FibreXtreme SL240 PCIe.
- Applications and topologies for SL240 PCIe cards.
- Instructions for installing and configuring the card.
- An operational overview of the product.
- General card specifications.
- Register set information.
- Programming information.
- Summary of the protocol used by the SL240 PCIe cards.
- Ordering information for all products mentioned in this manual.
- A brief introduction to the Front Panel Data Port (FPDP) interface.
- Definitions of words, phrases, and terms used in this manual.
- List of key words referenced in this manual.

The information in this manual is intended for information systems personnel, system coordinators, or highly skilled network users with at least a systems-level understanding of general computer processing, memory, and hardware operation.

Style Conventions

- Called functions are italicized. For example, OpenConnect().
- Data types are italicized. For example, int.
- Function parameters are bolded. For example, Action.
- Path names are italicized. For example, utility/sw/cfg.
- File names are bolded. For example, config.c.
- Path file names are italicized and bolded. For example, utility/sw/cfg/config.c.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7e.
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/). For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
C:\>ls
 file1                file2                    file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

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2.2 Related Information

- *ANSI Z136.2-1988 American National Standard for the Safe Use of Optical Fiber Communication Systems Using Laser Diode and LED Sources*.
- *Draft Standard for a Common Mezzanine Card Family*: CMC; IEEE P1386, Draft 2.0, April 4, 1995.
- *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards*: PMC, IEEE P1386.1, Draft 2.0, April 4, 1995.
- *Fibre Channel Association Product Information Bulletin Revision*, December 9, 1994.
- *Fibre Channel Physical and Signaling Interface (FC-PH)*, Revision 4.3, June 1, 1994; Produced by the ANSI X3T9.3 standards group.
- *Fibre Channel Physical and Signaling Interface-2 (FC-PH-2)*, Revision 7.3, January 5, 1996; Produced by the ANSI X3T11 standards group.
- *Fibre Channel Physical and Signaling Interface-3 (FC-PH-3)*, Revision 8.6, April, 1996; Produced by the ANSI X3T11 standards group.
- *Front Panel Data Port Specifications, ANSI/VITA 17-1998*, Revision 1.0; February 11, 1999. Produced by the VITA Standards Organization.
- *IEC 825-1984 Radiation Safety of Laser Products, Equipment Classification, Requirements, and User's Guide, 2 parts*, 1993.
- *FibreXtreme SL100/SL240 Serial FPDP PCIe NSL Software and API Guide (Doc. No. F-T-ML-S2APINSL-A-0).*
- *LinkXchange GLX4000 Physical Layer Switch Hardware Reference Manual* (Doc. No. F-T-MR-L5XL144#-A-0), Curtiss-Wright.
- *LinkXchange LX2500 Physical Layer Switch Hardware Reference Manual* (Doc. No. F-T-MR-LX2500), Curtiss-Wright.
- *PCI Local Bus Specification*, Revision 2.1, June 1, 1995; PCI Special Interest Group.
- *CompactPCI Specification*, Revision 3.0, October 1, 1999; PICMG 2.0; CompactPCI Power Interface Specification, Revision 1.0, October 1, 1999; PICMG 2.11; Keying of CompactPCI Boards and Backplanes, Revision 1.0, October 1, 1999; PICMG 2.10.
- *American National Standard for XMC PCI Express Protocol Layer Standard, ANSI/ VITA 42.3-2006, http://www.vita.com*
- Small Form-factor Pluggable (SFP) MultiSource Agreement (MSA), September 14, 2000, FO Transceiver Industry
- Curtiss-Wright – http://www.cwcdefense.com/.
- VITA – http://www.vita.com/.

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Curtiss-Wright's policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Curtiss-Wright's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

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- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Curtiss-Wright's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Curtiss-Wright's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's biannual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

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3 TECHNICAL SUPPORT

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Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

While we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

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· Fax: (937) 252-1465
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3.1 Ordering Process

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4 PRODUCT OVERVIEW

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4.1 Overview

The SL240 PCIe is a low cost, highly scalable, point-to-point, serial I/O interconnect that maintains complete software compatibility with PCI. It transfers data at 5 Gbps per lane (2.5 Gbps for Gen 1), per direction, and will scale proportionately for performance by adding lanes to the link.

The PCIe basic transmission unit consists of two pairs of wires, called a "lane." Each pair allows for unidirectional data transmission at 2.5 Gbps, so the two pairs combined provide 5 Gbps full duplex communication, without the risk of transmission collision.

Lanes can be concatenated to provide scalable performance; so for example, combining two lanes will yield 10 Gbps throughput.

The SL240 PCIe is an 8 lane (x8) board with a maximum of 1 Gigabyte per second of throughput per transmit and receive directions. It incorporates many of the advanced protocol features in PCI Express such as Automatic Lane Reversal.

The SL240 PCIe can interoperate with Curtiss-Wright's existing FibreXtreme family of products. These products include PCI, PCI Mezzanine (PMC), and a rehostable Common Mezzanine Card (CMC).

The PCI, and PMC versions provide this link via the PCI bus. However, the SL240 PCIe utilizes the PCIe bus for very high serial bandwidth and throughput applications where parallel-type buses are no longer feasible. All of these variations interoperate completely on the link interface, providing seamless integration between diverse platforms.



Figure 2-1 SL240 PCIe 100 MHz Card

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4.2 SL240 PCIe Features

SL240 PCIe provides reliable highly scalable point-to-point serial I/O interconnects between systems, with minimal overhead and very low latency. The protocol involved for this transport is based on Fibre Channel, though it is not Fibre Channel compliant.

The SL240 PCIe cards incorporate the functionality of four independent Serial FPDP 5 Gbps channels on a single Host Bus Adapter (HBA). This compact design minimizes the number of required host computer slots, while providing the performance of two separate x4 HBAs. As a result, an efficient Serial FPDP system is established using only a minimal number of PCI express slots.

The physical media interface of the SL240 PCIe is the Small Form-factor Pluggable (SFP) Optical Transceiver. The SFP transceivers can be plugged into the card and are removable.

- The major SL240 PCIe features are listed below:
- x8 Link.
- Full-duplex PCI Express lanes; 5 Gbps each.
- Automatic lane reversal.
- 8b/10b encoding.
- Link training (auto-negotiate to smallest link width).
- 256 byte maximum payload size.
- End-to-end CRC and data poisoning.
- Advanced error reporting.
- Link management.
- Advanced flow control.
- Turn off unused lanes for power reduction.

Additional SL240 PCIe Features are:

- Contains four independent Serial FPDP channels.
- Minimizes implementation cost and enhances throughput by using a simple protocol.
- Provides built-in data synchronization with very little reduction in throughput.
- Integrated interrupt controller to report link failure, transaction completion, or buffer space request.
- Status LEDs that reports link stability for each PCIe lane
- Loop operation with out-of-band arbitration or point-to-point operation.
- Provides a register set designed for easy programming and status retrieval.
- Small Form-factor Pluggable (SFP) short wavelength laser media.
- 256 MB Receive FIFO (shared by all 4 channel).
- 1 KB Transmit FIFO (per channel).

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4.2.1 SFP Media

The SL240 PCIe card supplies four short wavelength (850 nm) SFP optical transceivers for the physical media interface. Each short wavelength transceiver provides a solution for short reach intersystem connections (< 300 m), such as connecting between cards on the same backplane.

The SFP transceivers accept a fiber-optic cable terminated with a Duplex LC style connector, available from most major cable manufacturers. For details concerning these connectors, contact Curtiss-Wright Controls, Inc., Technical Support.



Figure 5- 1

4.3 Applications

SL240 PCIe cards are used in a variety of topologies for a variety of applications. The following sections detail typical topologies used and some applications. Many other applications are possible in these configurations. The SL240's applications can be further expanded with the use of additional Curtiss-Wright equipment whose features are also covered in this section.

4.3.1 Typical Digital Signal Processing (DSP) Imaging System

With the support for a 2.5 Gbps link transmission rate between interconnected subsystems, the SL240 PCIe is ideal for use in many of today's high-throughput data transfer applications. Figure 2-2 shows one example. This figure shows the SL240 PCIe's usable data throughput rate.

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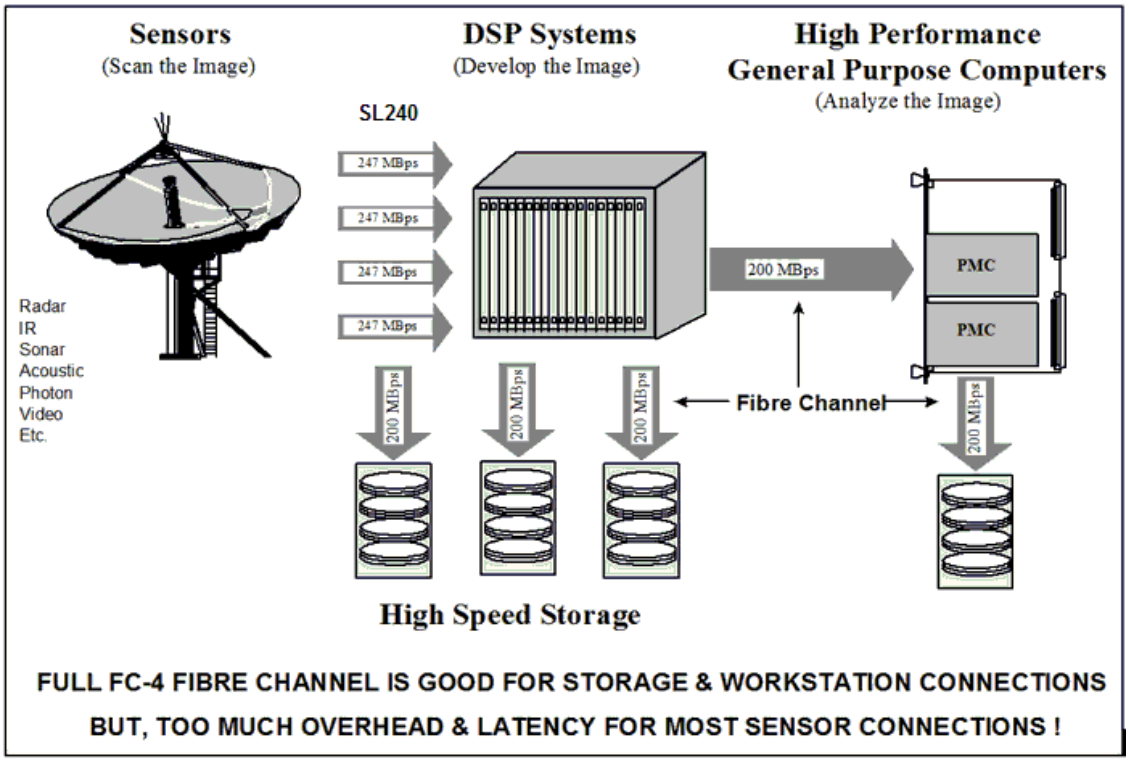


Figure 2-2 Typical Applications of FibreXtreme SL240 PCIe in Advanced DSP Systems

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4.3.2 Extending FPDP

The maximum allowable length for FPDP cables ranges from 1 m to 5 m depending upon its configuration. The FibreXtreme SL240 PCIe system provides a communication link that extends the reach of FPDP while retaining simplicity, high bandwidth, and reliability. This concept is shown in Figure 2-3. The type of transceiver used determines the distance the FPDP cards can be separated. See section 2.2.1, Media Options, for details on transceivers. Using fiber optics provides electrical isolation.

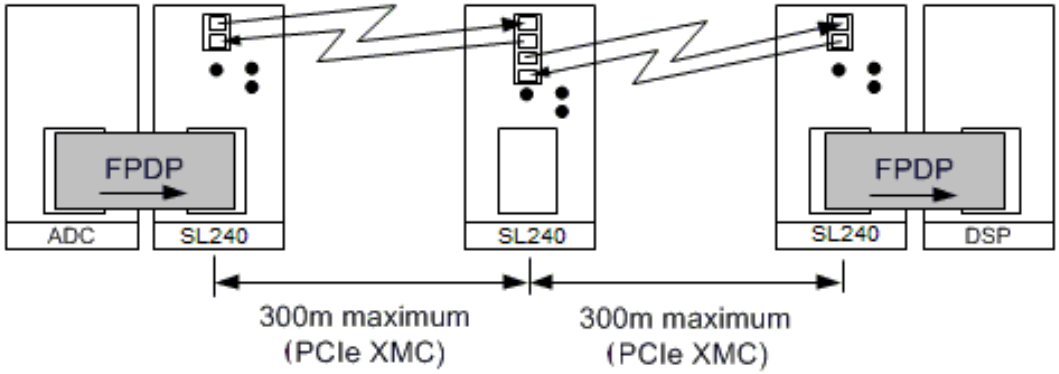


Figure 2-3 FibreXtreme SL240 PCIe Extending FPDP

4.4 Topologies

4.4.1 Typical Topologies

There are four typical topologies for the SL240 PCIe card. These topologies should cover most customer applications, if another topology is desired contact Curtiss-Wright Technical Support to see if it is possible. The topologies are:

- Point-to-point
- Chained
- Single Master Loop
- Multiple Master Loop

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4.4.2 Point-to-point

The point-to-point topology is the native mode for the SL240 PCIe card. One user option available in this mode is whether flow control is used or not. If flow control is used, the transmitter on each end will not transmit when the remote receiver is telling it to back off or the receive fiber is missing. In this mode, the maximum amount of data that can be transferred is 247 MB/s per direction (in this case, both cards are receiving and transmitting 247 MB/s at the same time). The maximum distance between the nodes is 26 km.

There are many applications for the point-to-point topology—as long as it involves only two nodes, this topology covers it. One advantage that point-to-point has over the other topologies is the ability to do simultaneous bi-directional traffic.

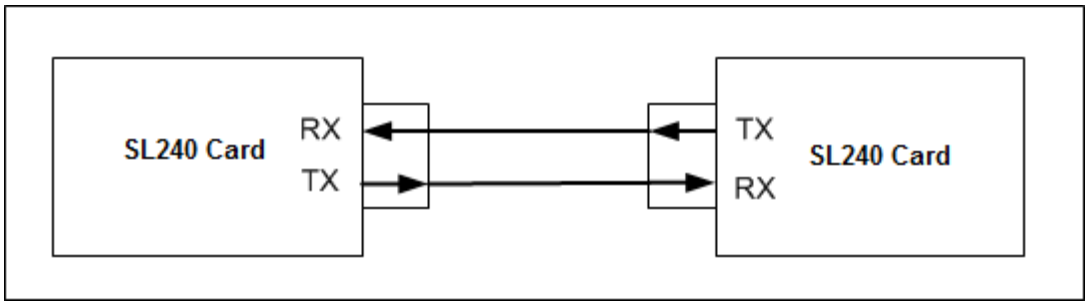


Figure 2-4 Point-to-Point Topology

4.4.3 Chained

This topology is a single transmitter on the end of a long string of receivers. No flow control is available in this topology, and the distance between the nodes is limited only by the transceivers used (10 km typical, 26 km maximum).

This topology is good for broadcasting data to multiple destinations where late data is of no use, such as video transmission applications.

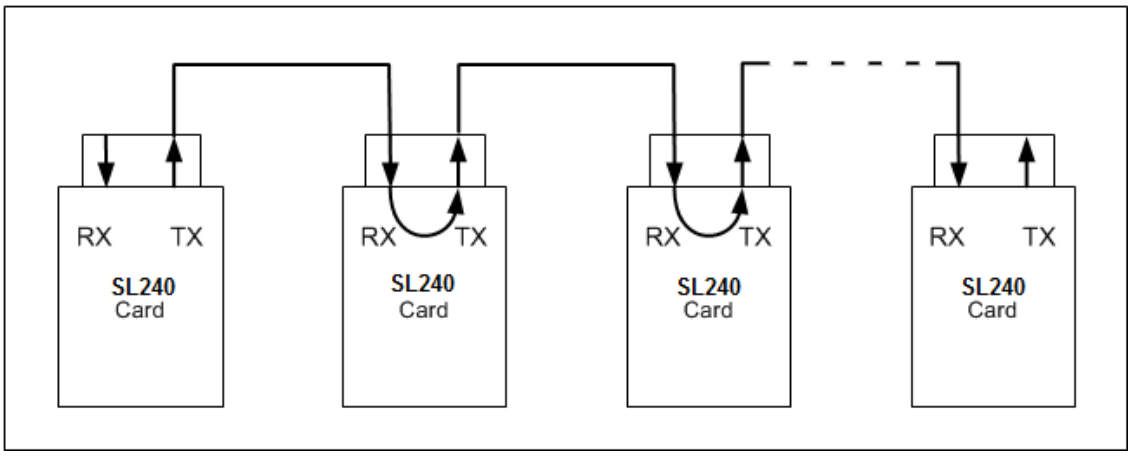


Figure 2-5 Chained Topology

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4.4.4 Single Master Ring

This is one of the most useful topologies for the SL240 PCIe card. This topology allows a single transmitter to send data to a group of destinations with flow control from all of the destinations. This flow control is a single flag to the master—it can send or it cannot send data. This means that if one destination has a failure and stops removing data from its receive FIFO, it should be switched out to avoid bringing down the loop. A switch suitable for this purpose is the LinkXchange GLX4000 Physical Layer Switch, available from Curtiss-Wright Software controls mastership switching of the ring. There are rules associated with master switching listed in the "Programming Interface" section. The flow control used in this case is similar to a multi-drop FPDP bus, where any receiver can back the transmitter off.

This is the typical configuration for record-playback systems, where you have multiple signal processors and data storage elements present on the network and there is only one node (the data source or the recorder playing the data back) transmitting at a time.

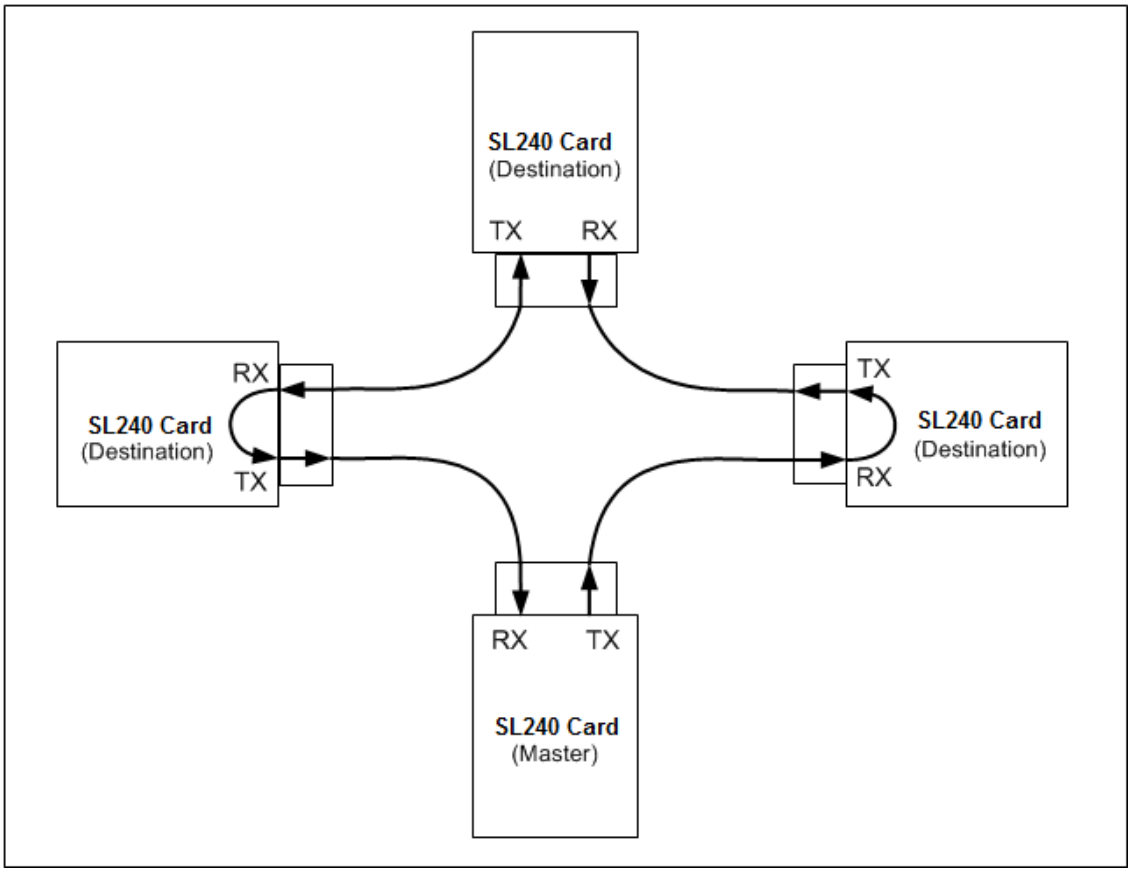


Figure 2-6 Single Master Ring

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4.4.5 Multiple Master Ring

This is another form of ring topology, where there are multiple masters on the ring, and these masters have to receive data as well as transmit data to the next master. In the most complex case, each node is a master, which means that it receives data from the previous master and sends data to the next master. Flow control is not allowed in this topology for rings above two nodes, and the data cannot be passed through masters unless control guarantees that there is at least one source-only node on the ring and that no two masters will transmit at the same time. Single master rings should temporarily become multiple master rings when switching loop masters.

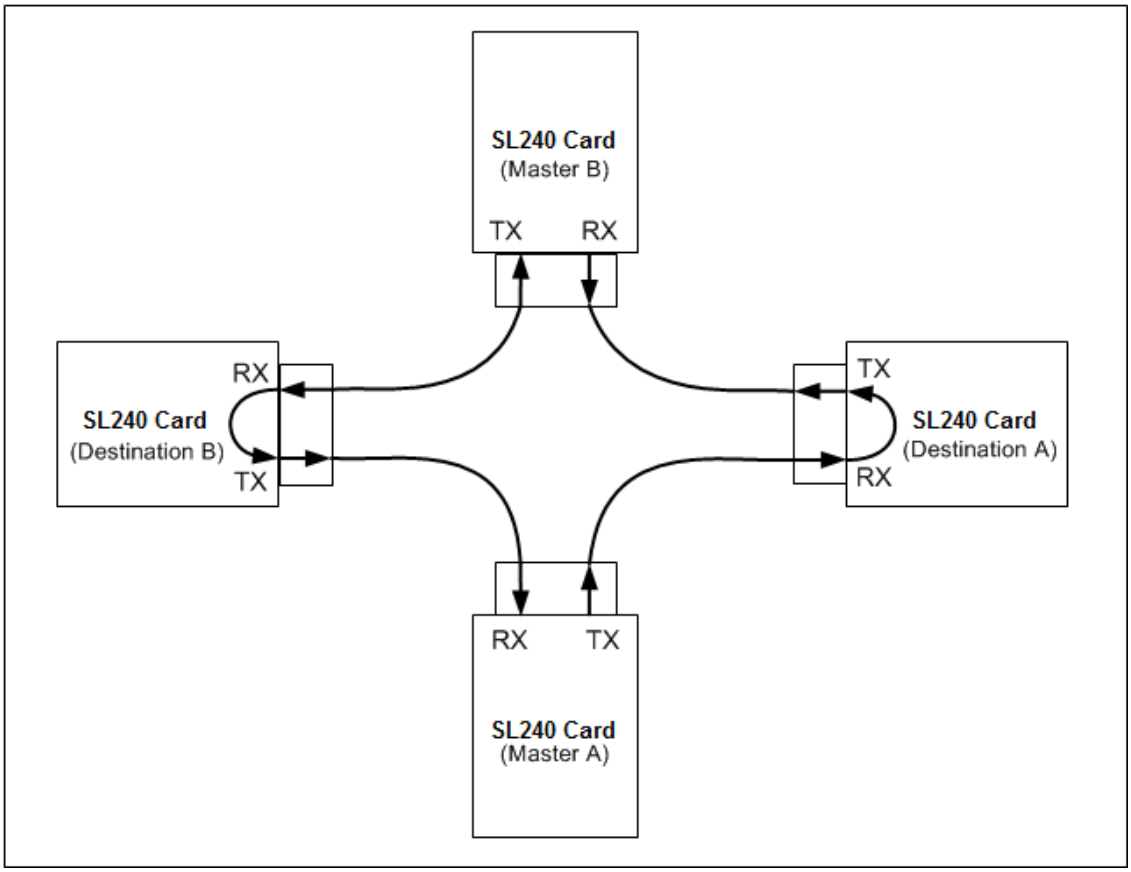


Figure 2-7 Multiple Master Ring

4.5 Status Link Up LED

The Link Up LEDs indicate a signal is present on the receiver. These LEDs gives no indication of the validity of the signal, only that a signal is present. A Link Up LED is present for each Channel. The Link Up LEDs are on the same side of the board as the transceivers near the front panel.

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5 INSTALLATION

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5.1 Overview

SL240 PCIe cards require only one slot on the host computer backplane and interface directly to a fiber-optic cable.

To install an SL240 PCIe card, follow the steps below:

1. Unpack the card.
2. Inspect the card.
3. Install the card.
4. Connect the cables.

5.2 Unpack the Cards



CAUTION: Exercise care regarding the static environment. Use an anti-static mat connected to a wristband when handling or installing the SL240 PCIe card. Failure to do this may cause permanent damage to the components on the card.

Follow the steps below to unpack the card:

1. Put on the wristband attached to an anti-static mat.
2. Remove the card and anti-static bag from the carton.
3. Place the bag on the anti-static mat.
4. Open the anti-static bag and remove the card.
5. In the unlikely event that you should need to return your SL240 PCIe card, please keep the original shipping materials for this purpose.

Any optional equipment is shipped in separate cartons.

5.3 Inspect the Cards

The SL240 PCIe card consists of a single card with a built-in link interface. If the card was damaged in shipping, notify Curtiss-Wright, or your supplier immediately.

5.4 Install the SL240 PCIe Card

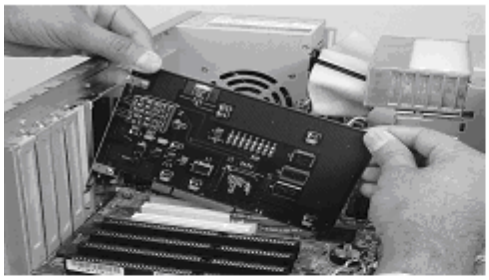


WARNING: Turn off all power to your operating system before attempting to install the SL240 PCIe Card.

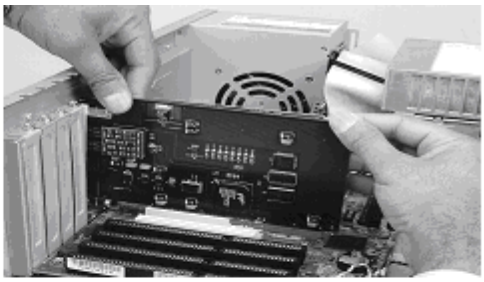
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To install the SL240 PCIe card, push the card into an available X8, X16, or x32 PCIe slot on the motherboard as shown in Figure 5-1 step 1 and 2, until it is firmly seated. Install the mounting screw as shown in step 3.

NOTE: The SL240 PCIe requires an x8 PCIe bus slot for proper operation. The board cannot be installed in an x4, x2, or x1 PCIe bus slot.



Step 1



Step 2



Step 3

Figure 5-2 SL240 PCIe Card Installation

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5.5 Connect the Cables

5.5.1 Transmission Media

For short wavelength laser modules, either a 50 µm or 62.5 µm core diameter cable should be used. For distances up to 300 meters 62.5 µm can be used. 50 µm cable allows distances up to 500 meters.

5.5.2 Fiber-Optic Cables

The two factors to consider when connecting the cables are the topology and the transmission media used. The cards can be connected in several different topologies depending on your application. See section 2.4, Topologies, for detailed examples.

Fiber-optic Cable Precautions

CAUTION: Fiber-optic cables are made of glass and may break if crushed or bent in a loop with less than a 2-inch radius.

Look at the cable ends closely before inserting them into the connector. If debris is inserted into the transmitter/receiver connector, it may not be possible to clean the connector out and could result in damage to the transmitter or receiver lens. Hair, dirt, and dust can interfere with the light signal transmission.

Use an alcohol-based wipe to clean the cable ends.

For short wavelength laser modules, either a 50 µm or 62.5 µm core diameter cable should be used. For distances up to 300 meters 62.5 µm can be used. 50 µm cable allows distances up to 500 meters.

The optional fiber-optic cables may be shipped in a separate carton. Remove the rubber boots on the fiber-optic transmitters and receivers as well as the ones on the fiber-optic cables. Replace these rubber boots when cables are not in use or if the node must be returned to the factory. Attach the fiber-optic cables to the connectors on the SL240 PCIe card.

Figure 3-2 and Figure 3-3 depict the types of fiber-optic connectors needed for the SL240 PCIe card.

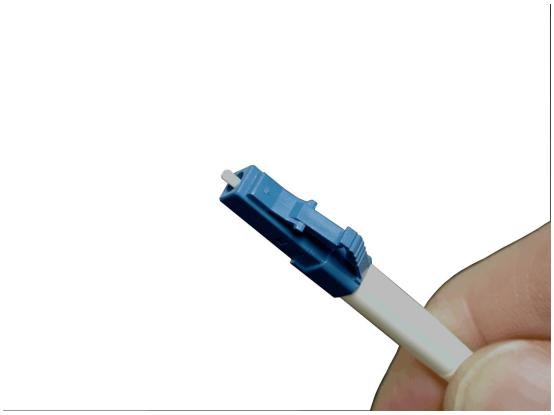


Figure 3-2 Fiber-optic Simplex LC Connector



Figure 3-3 Fiber-optic Duplex LC Connector

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5.6 Troubleshooting

If the system does not boot correctly, power down the machine, reseat the card, double-check cable connections, and turn the system back on. If problems persist, contact Curtiss-Wright, Defense Solutions., Technical Support at **(800) 252-5601** or **DTN_support@ curtisswright.com** for assistance.

Please be prepared to supply the following information:

Machine: _____
OS Name: _____
OS Version: _____
Card Type: _____
Card Serial #: _____
Software Part #: _____
Software S/N: _____
Problem Reproducibility: _____
Problem Description: _____

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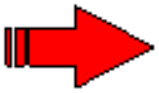
6 OPERATION

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6.1 Overview

SL240 PCIe cards move data with very low latency between a host interface and a 5 Gbps link. The SL100 PCIe version uses 1G SFP optical transceivers and operates in environments where a lower system throughput is acceptable. Both cards must be installed in an x8, x16, or x32 PCIe bus slot.



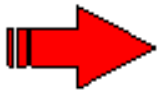
NOTE: It is not possible for SL100 and SL240 PCIe cards to communicate with one another on the link because the link speeds are not compatible.



CAUTION: Do **not** break the link between two SL240 PCIe cards. The unpredictable results may affect your system. While the FPGA can recover from link break scenarios, the corresponding link and data errors caused by disruption of the link must be adequately addressed by the host interface.

6.2 Theory of Operation

The operation of SL240 PCIe cards is simple—take data from the host bus interface and transmit it across a link, or take data from the link and pass it to the host bus interface. The link protocol involved is kept minimal to reduce the latency and improve throughput, while still providing a set of useful features with which to customize your applications. The hardware offers many different features for advanced applications, while maintaining a simple interface to the most commonly used features.



NOTE: For further explanation of terms used in this chapter, refer to the FPDP Primer in Appendix D.

6.2.1 Receive Operation

The SL240 PCIe has several options for receiving data. The most basic option is no-loop operation with data-receive enabled. In this case, data is:

1. Received from the link.
2. Decoded by the card.
3. Placed in the receive FIFO.

If a receive DMA is started, the data is automatically moved into the PCIe address given by the DMA transaction. If a DMA is not started, the data waits in the receive FIFO until the host either PIOs the data out or sets up the DMA transaction to remove it.

FPDP signals are embedded into the control words of a frame. The FPDP signals transported across are: /NRDY, /DIR, /SYNC, PIO1 and PIO2. A /SUSPEND signal is synthesized by the transmit state machine in response to how full the receive FIFO is—this is not the /SUSPEND from an FPDP port.

All FPDP signals, with the exclusion of /SYNC, are passed around the receive FIFO, and are not synchronized with the data stream. The FPDP signals can be read from a register once they are received from the link.

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6.2.2 Transmit Operation

The transmit operation must first collect data in the transmit FIFO for transmission. This means that either data is PIO'd into the Transmit FIFO or a DMA transaction is set up to fill the FIFO. Once a data word is in the FIFO, transmission can begin. The framing-state machine first checks that there is no data in the retransmit FIFO and that the remote node is not telling this node to back off. If it is clear to send, after it transmits the next SOF it will begin filling the data frame as full as possible (up to 2048 bytes). The data is then encoded and sent out across the link. If there is data in the Retransmit FIFO or the card is being backed off from the destination, then the card waits until both conditions are clear before it starts transmission. Note that SYNC and SWDV can also be transmitted by the link logic and these two types of synchronization primitives are handled by the Transmit FIFO and transmit control logic in a similar method as standard data. Specifically, they are written to the link logic through the same interface, passed through the same internal link logic path, and are used in the assembly of link frames in a similar fashion, although the maximum frame size does differ for these types of associated Serial FPDP frames.

All FPDP signals, with the exclusion of /SYNC, are passed around the transmit FIFO, and are not synchronized with the data stream. The FPDP signals can be written to a register and then transmitted across the link.

6.2.3 Loop Operation

Loop operation with the SL240 PCIe acts like a virtual FPDP bus where one source (the loop master) can transmit to any number of receive nodes. The link protocol is the same for this operation, except any node in the loop may assert a suspend request embedded in this data stream. This implies that if one node on the loop is not ready to receive data, the source is backed off for all nodes. This is the same way that multi-drop FPDP busses function.

The fundamental difference between a loop master and a receiving node is the loop master does not have its loop retransmission enabled. Therefore, to the loop master, it appears as if it is still in a point-to-point connection with a single node. Receiving nodes, on the other hand, have knowledge that they are in a loop configuration and must be configured as such. Note that the loop master receives all the data it transmits, so data can either be checked for errors or ignored when it is received. This checking (beyond verification of CRC and 8B/10B decoding validity) is not done in the SL240 PCIe and must be implemented by the system designer.

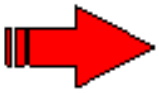
The receivers on the loop can choose to collect the data or ignore it off the loop. If the Receive FIFO is enabled (the node is collecting data), a suspend request may be asserted by this node as the data passes through. If it is not configured to receive the data, it simply passes the data through the Retransmit FIFO without modifying the suspend request.

Serial FPDP supports the DIR, NRDY, PIO1, and PIO2 FPDP signals. These signals do not propagate through the Transmit FIFO or the Receive FIFO and thus cannot be directly associated with the corresponding data. To guarantee a pulse on these signals is propagated to the remote Serial FPDP receiver, the pulse width from the host-bus interface must be equal to or greater than the maximum Serial FPDP frame length (512 words of data with an overhead of nine ordered sets).

The values of PIO1 and PIO2 are retransmitted according to their received link values and the values of DIR and NRDY are used as follows: if the receive interface is enabled, the values transmitted are the received link values logically ORed with the PCIe host-interface values; otherwise, the values are retransmitted according to their received link values. The values of these four signals sent to and received from the link are placed in the register set and then can be accessed by software. These signals are typically used for application-dependent signaling between nodes. The use of DIR and NRDY is consistent with the use of flow control (retransmission of a STOP request) for loop operation. See the VITA 17.1 Serial FPDP specification for additional details.

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Note that NRDY as a Serial FPDP signal has no direct impact on the operation of the link logic. Rather, NRDY is passed through the link logic and its function is dependent on the respective host interface. The Serial FPDP flow control (implemented via suspend requests which are also known as STOP ordered sets) is used by the link logic and does not directly affect the interface between the link logic and host interface.



NOTE: One node on the loop MUST be in non-loop operation in order for loop operation to work correctly. One node needs to remove the data from the loop. When switching masters on the loop, both the previous master and the next master should be in non-loop operation before the previous master switches into loop mode.

6.3 Data Synchronization

The data synchronization primitive SYNC is sent across the link under user control. This primitive synchronizes with the data stream and is written to the transmit FIFO under user control or through the transaction channels. The SYNC may correspond to /SYNC without /DVALID or /SYNC with /DVALID on the FPDP interface depending on the card's configuration.

Unless a non-intelligent device is used, such as a sensor, which cannot insert a periodic SYNC, SYNC should always be used to segment data transfers. It has little impact on system performance and provides a mechanism to synchronize the send and receive operations via the link. This synchronization process is especially useful at application start-up, after error conditions, and is also useful to verify the error-free flow of data during normal operation.

6.4 Configuration Options

The data synchronization primitive SYNC is sent across the link under user control. This primitive synchronizes with the data stream and is written to the transmit FIFO under user control or through the transaction channels. The SYNC may correspond to /SYNC without /DVALID or /SYNC with /DVALID on the FPDP interface depending on the card's configuration.

Unless a non-intelligent device is used, such as a sensor, which cannot insert a periodic SYNC, SYNC should always be used to segment data transfers. It has little impact on system performance and provides a mechanism to synchronize the send and receive operations via the link. This synchronization process is especially useful at application start-up, after error conditions, and is also useful to verify the error-free flow of data during normal operation.

6.4.1 Flow Control

Flow control allows a Serial FPDP receiver to throttle the data stream from a Serial FPDP transmitter. If this option is turned off, the card will continue to send data even when the receiver signals it to stop or when the link is down.

In almost every application, flow control should be enabled. Even if the application must sustain maximum link throughput, it is better to drop the data at the sending source should the system experience a temporary overload condition. In some rare cases, flow control is not desirable. In these cases, very careful system planning is required, which should be confirmed with Curtiss-Wright prior to architectural finalization. One possible exception is for applications that cannot use a duplex fiber-optic link, which means status information (link up and state of flow control) is not available from the remote node. In this circumstance, disable flow control to allow the transmitter to function without the receiver connected normally.

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6.4.2 Loop Enable

The loop-enable option allows the SL240 PCIe card to transmit the received Serial FPDP data stream again. When loop enable is on, it implies that this node is designated as a receiver in the current configuration.

6.4.3 Receiver/Transmitter Enable

The transmitter-enable and receiver-enable settings can turn off the transmit and receive Serial FPDP data streams, respectively. Neither affects the loop operation, so data will still be retransmitted if the loop operation is enabled. This makes these options useful for record/ playback systems where you wish to retransmit merely the data received without processing it. The receive-enable is useful for disabling the receive FIFO for the master in loop operation so that the data sent is not received.

6.4.4 CRC Generation/Checking

The CRC Generation/Checking option allows the SL240 card to detect data transmission errors. The card is not capable of correcting the errors. Error correction is left to application level design.

A single bit controls both generation and checking. CRC should be used in almost all applications. It offers excellent coverage of data errors and has very little impact on link throughput for maximum frame sizes. The option of disabling CRC is only retained for compatibility with older third-party devices. Both nodes on the link (or all nodes in a loop configuration) should be set to a common CRC mode or the resulting mismatch will cause data errors and/or link errors.

6.4.5 Stop on Link Error of/SYNC

There are two DMA stop conditions available to the user—stop on link error and stop on /SYNC. The stop on link error stops the DMA engine from removing data from the receive FIFO when there is a link error, such as the link going down. The stop on /SYNC option allows you to stop data from being received from the receive FIFO when a /SYNC without /DVALID is received on the output.

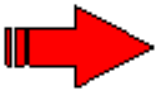
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7 APPENDIX A

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7.1 Specifications



NOTE: "Peak" current specifications are based on measurements taken while the card was transmitting and receiving large buffers of data. All current requirement measurements were taken on a Quad core processor 3.4 GHz system.



CAUTION: Power usage is highly system dependent and varies from system to system.

7.1.1 SL240 PCIe Specifications

Physical Dimensions:	174.6 mm x 106.7 mm (6.87 inches x 4.173 inches)
Weight:	» 0.25 lbs
Operating Voltage: 12 volt supply	 11.75 Volts to 12.25 V
Power Dissipation: 12 Volt Supply	 21.6 Watts Peak @ 12 V
Electrical Requirements: 12 Volt Supply	 1.8 Amps Peak
Temperature Requirements: Storage Operation	 -40° to +85°C 0° to +50°C, with 200 LFM air minimum
Humidity Range : Storage Operating	 0% to 95% (noncondensing) 10% to 90% (noncondensing)
Maximum Node Separation: Standard Fiber	 300 meters
Mean Time Between Failures (MTBF)*: SL240 PCIe, Short wavelength lasers:	 522,521 hours

*These MTBF numbers are based on calculations using MIL-HDBK-217 FN2, Appendix A, Telcordia (Belcore) Method 1 Case 3 for a GB, GC at 30° C.

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7.2 Media Interface Specifications

7.2.1 SL100 PCIe Fibre-Optic Media Interface Specifications

Connector: ..... Duplex LC

850 nm:

Media ..... 50 µm or 62.5 µm multimode fiber

Fiber Channel Formats: ..... 100-M5-SN-1 (1 Gbps, 50 µm fiber)
100-M6-SN-1 (1 Gbps, 62.5 µm fiber)

Maximum Fiber Length: ..... 550 m with 50 µm fiber
300 m with 62.5 µm fiber

Transmit Wavelength: ..... 830 to 860 nm

Transmit Power: ..... -10 to -4 dBm

Receive Wavelength: ..... 770 to 860 nm

Receive Sensitivity: ..... -16 to 0 dBm

7.2.2 SL240 PCIe Fibre-Optic Media Interface Specifications

Connector: ..... Duplex LC

850 nm:

Media ..... 50 µm or 62.5 µm multimode fiber

Maximum Fiber Length: ..... 250 m with 50 µm fiber
125 m with 62.5 µm fiber

Transmit Wavelength: ..... 830 to 860 nm

Transmit Power: ..... -8 to -4 dBm

Receive Wavelength: ..... 770 to 860 nm

Receive Sensitivity: ..... -12 to 0 dBm

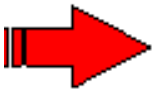
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8 APPENDIX B

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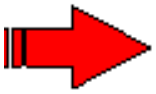
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8.1 Overview



NOTE: The FibreXtreme SL100 and SL240 PCIe Cards will be referred to throughout this appendix as SL240 PCIe. Anything that is exclusive to the SL100 PCIe Cards will be described as such.

The SL240 PCIe Serial FPDP protocol (also known as VITA 17.1) is designed to provide near optimal throughput while maintaining low overhead. The link transfer rate for the SL240 PCIe card is 5 Gbps per lane. Since an 8B/10B encoding scheme is used, this corresponds to a raw data rate of 1000 MBps (1 GBps) for the SL240. Based on the protocol presented here, the usable throughput of each link available to the user is 247 MBps for the SL240. All ordered sets used by this protocol are standard Fibre Channel ordered sets with the exception of positive IDLE, which is allowed for a more flexible receiver interface



NOTE: The protocol referred to throughout this document is the protocol used by the transmitter and accepted by the receiver. The receiver does not have to see the protocol defined here to receive data. Any generic Fibre Channel data stream with an IDLE at least every 4096 words can be used.

8.2 Ordered Sets Used

Fibre Channel denotes a certain mapping of the transmission words in the 8B/10B protocol to be ordered sets, which denote special control information for Fibre Channel. These same ordered sets are used in VITA 17.1, but are assigned different meaning.

There are eighteen ordered sets used by SL240 PCIe to denote different information. Twelve of these ordered sets are used to embed five bits of data—eight start-of-frame (SOF) sets are used to embed three bits at the start of a frame, and four status-end-of-frame (SEOF) sets are used to embed two bits at the end of the frame. The SOF ordered sets embed three FPDP signals - PIO1, PIO2, and DIR.

Note that although the direction signal on FPDP is active low (/DIR), the signal transmitted on the link is active high (DIR).

The four EOF ordered sets embed the FPDP signal NRDY (once again, the inverted version of the FPDP interface's /NRDY) and Transmit FIFO Overflow flag.

There are two additional EOF ordered sets used by SL240 PCIe to denote the actual end of frame. The Mark EOF (MEOF) denotes a frame that has SYNC associated with it, and the Frame EOF (FEOF) denotes a normal data frame. The other four ordered sets are inter-frame padding used to denote flow control information and alternate frame interpretations. Table 6-1 shows the mappings from the Fibre Channel ordered sets onto the VITA 17.1 ordered sets, along with the meaning associated with each ordered set.

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Table 6-1 Mapping Fibre Channel Ordered Sets onto the VITA 17.1 Ordered Sets

Fibre Channel Ordered Set	VITA 17.1 Ordered Set	Description
SOFc1	SOF	Start of Frame: PIO1 = 0, PIO2 = 0, DIR = 0
SOFi1	SOF	Start of Frame: PIO1 = 0, PIO2 = 0, DIR = 1
SOFn1	SOF	Start of Frame: PIO1 = 0, PIO2 = 1, DIR = 0
SOFi2	SOF	Start of Frame: PIO1 = 0, PIO2 = 1, DIR = 1
SOFn2	SOF	Start of Frame: PIO1 = 1, PIO2 = 0, DIR = 0
SOFi3	SOF	Start of Frame: PIO1 = 1, PIO2 = 0, DIR = 1
SOFn3	SOF	Start of Frame: PIO1 = 1, PIO2 = 1, DIR = 0
SOFf	SOF	Start of Frame: PIO1 = 1, PIO2 = 1, DIR = 1
EOFt	SEOF	Status EOF: FIFO Overflow = 0, NRDY = 0
EOFdt	SEOF	Status EOF: FIFO Overflow = 0, NRDY = 1
EOFa	SEOF	Status EOF: FIFO Overflow = 1, NRDY = 0
EOFn	SEOF	Status EOF: FIFO Overflow = 1, NRDY = 1
EOFni	MEOF	Mark EOF: EOF for a SYNC frame
EOFdti	FEOF	Frame EOF: EOF for a normal data frame
R_RDY	SWDV	SYNC with DATA Valid: Says that the next frame will be a SYNC with DATA frame
NOS	STOP	Tells the remote transmitter to stop sending data
CLS	GO	Tells the remote transmitter it can continue to send data
IDLE	IDLE	IDLE character: Used as a padding word to maintain receiver synchronization

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8.3 Frames

There are four basic frame types defined in VITA 17.1 – an IDLE frame, data frame, a SYNC without data frame, and a SYNC with data frame. The data is divided into frames so the FPDP signals are sampled at some minimum interval, and so the receiver is guaranteed to see IDLEs to maintain synchronization. SYNC is used to delimit data streams and maintain host program synchronization. This signal is under user control for PCI-based products, and is the same as the FPDP /SYNC signal for CMC/FPDP based products. Whenever a SYNC appears on the output of the Transmit FIFO, the current frame is terminated and the proper SYNC frame (SYNC with data or SYNC without data) is sent. Figure 6-1 shows the four types of frames and the ordered set placement within those frames.

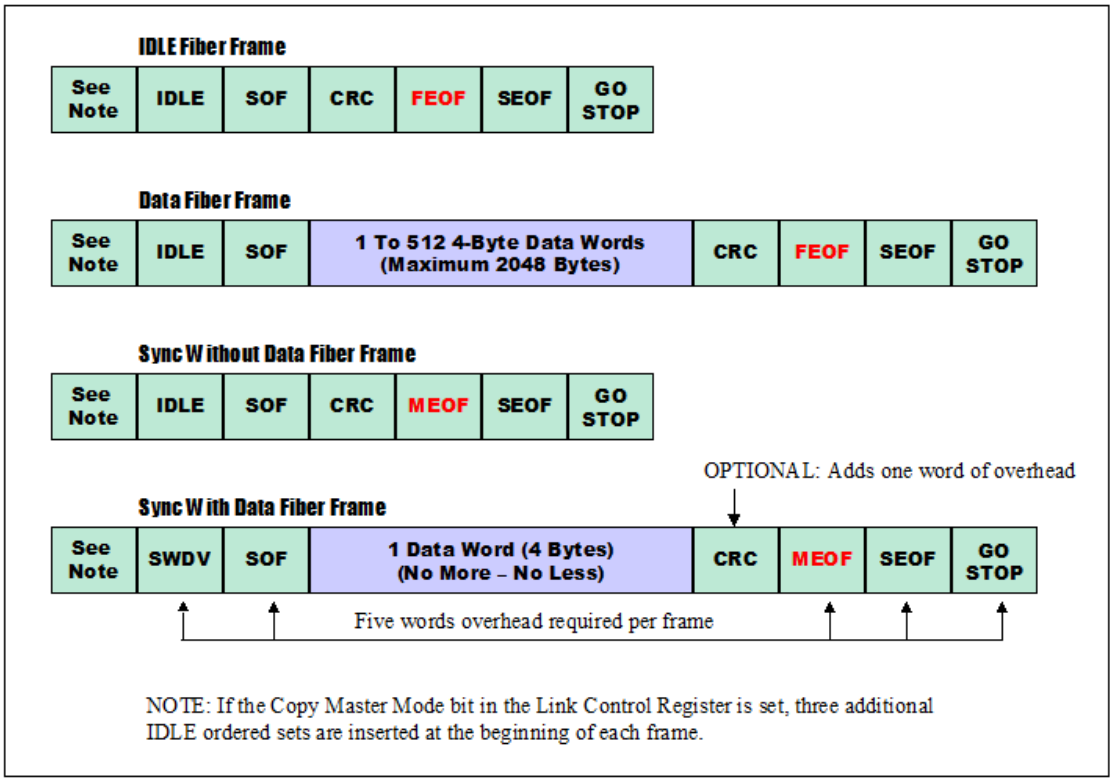


Figure 6-1 VITA 17.1 Framing Protocol

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8.3.1 Link Bandwidth

With CRC disabled and the Copy Mode Master bit clear (‘0’), there is a five-word overhead for every frame transmitted. Since frames can contain up to 512 words of data, this results in an efficiency of 99.03%. With CRC enabled and the Copy Master bit clear, there is a six-word overhead for every frame transmitted. This results in a maximum efficiency of 98.84%. With the Copy Mode Master bit set (‘1’), three additional ordered sets are added per frame. This results in an efficiency of 98.46 percent without CRC and 98.27 percent with CRC. Table 6-2 gives the theoretical maximum sustained throughput based on these numbers.

Table 6-2 Maximum Sustained Throughput per link

Card	With CRC and Copy Mode Master bit = 0	Without CRC and Copy Mode Master bit = 0	With CRC and Copy Mode Master bit = 1	Without CRC and Copy Mode Master bit = 1
SL240	247.10 MB/s	247.58 MB/s	245.68 MB/s	246.15 MB/s

NOTE: The Copy Master Mode is located in the Link Control register.

8.3.2 FPDP Sinnal Sample Rate

The states of the FPDP signals (PIO1, PIO2, DIR, and NRDY) are transmitted across the link at varying rates. The worst-case rate at which these signals are sampled is for CRC checked filled data frames and the Copy Mode Master bit set . In this case, the signals are sampled every 521 words. For CRC checked filled data frames and the Copy Mode Master bit clear, these signals are sampled every 518 words. Table 6-3 summarizes the worst-case sampling frequencies for the different link transmission speeds (SL240).

Table 6-3 Sampling Frequencies

Card	With CRC and Copy Mode Master bit = 0	Without CRC and Copy Mode Master bit = 0	With CRC and Copy Mode Master bit = 1	Without CRC and Copy Mode Master bit = 1
SL240	120.65 KHz	120.89 KHz	119.96 KHz	120.19 KHz

NOTE: The Copy Master Mode is located in the Link Control register.

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8.4 Data Transmission and Flow Control

As SL240 PCIe is seen as a point-to-point link from the transmitter, there is no need to log into the receiver node to begin sending data. SL240 PCIe cards can begin transmission as soon as they are started and data is available in the Transmit FIFO. Using the frames described above, the transmitter sets up a constant stream of frames, into which it inserts data as it becomes available. Data is only inserted if the flow control signal from the remote end is GO—if it is STOP, then the data waits in the Transmit FIFO until the signal changes. Curtiss-Wright' SL240 PCIe cards use the same protocol when transmitting from either end to allow the link to operate bi-directionally. Since these data streams are independent, the maximum throughput on the link would be 494 MB/s (247 MB/s/direction) for SL240.

The receiver should transmit the STOP signal when it has space for the data contained in 20 km of fiber or less left. Assuming 5 µs/km for the speed of light, this gives us 100 µs of data. For SL240, each 32-bit word (40 bits on the link) takes 16 ns, so there are 6250 words stored in 20 km of cable. The first 10 km is reserved for sending the STOP signal to the transmitter, and the second 10 km is for the data already contained in the receive fiber.

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9 APPENDIX C

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9.1 Ordering Information

This appendix contains the order numbers for Curtiss-Wright products mentioned in this manual. For an up to date list, or for inquiries about these products, contact Curtiss-Wright Defense Solutions Center Sales.

9.1.1 SL100/SL240 PCIe Multi-channel Board

Table 7-1 SL100/SL240 PCIe Multi-channel

Order Number	Description
FHB5-PE1MWB04-00	SL100 PCIe, x8 form-factor with one SFP optical transceiver.
FHB5-PE2MWB04-00	SL100 PCIe, x8 form-factor with two SFP optical transceivers.
FHB5-PE4MWB04-00	SL100 PCIe, x8 form-factor with four SFP optical transceivers.
FHB7-PE1MWB04-00	SL240 PCIe, x8 form-factor with one SFP optical transceiver.
FHB7-PE2MWB04-00	SL240 PCIe, x8 form-factor with two SFP optical transceivers.
FHB7-PE4MWB04-00	SL240 PCIe, x8 form-factor with four SFP optical transceivers.

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9.1.2 Short Wavelength Multimode Fibre-Optic Cables

The following table lists the order numbers for the simplex and duplex, 50/125 µm multimode fiber-optic cables, for use with the short wavelength laser media interface.

Table 7-2 LC to LC

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-M1LC3000-00	FHAC-M2LC3000-00	3 meters	LC	LC
FHAC-M1LC5000-00	FHAC-M2LC5000-00	5 meters	LC	LC
FHAC-M1LC1001-00	FHAC-M2LC1001-00	10 meters	LC	LC
FHAC-M1LC2001-00	FHAC-M2LC2001-00	20 meters	LC	LC
FHAC-M1LC3001-00	FHAC-M2LC3001-00	30 meters	LC	LC
FHAC-M1LCxxxx-00	FHAC-M2LCxxxx-00	Custom	LC	LC

Table 7-3 LC to ST

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-M1LCST03-00	FHAC-M2LCST03-00	3 meters	LC	ST
FHAC-M1LCST05-00	FHAC-M2LCST05-00	5 meters	LC	ST
FHAC-M1LCST10-00	FHAC-M2LCST10-00	10 meters	LC	ST
FHAC-M1LCST20-00	FHAC-M2LCST20-00	20 meters	LC	ST
FHAC-M1LCST30-00	FHAC-M2LCST30-00	30 meters	LC	ST
FHAC-M1LCSTxx-00	FHAC-M2LCSTxx-00	Custom	LC	ST

Table 7-4 SC to LC

Simplex Part Number	Duplex Part Number	Length	Cable End 1	Cable End 2
FHAC-M1SCLC01-00	FHAC-M2SCLC01-00	1 meter	SC	LC
FHAC-M1SCLC03-00	FHAC-M2SCLC03-00	3 meters	SC	LC
FHAC-M1SCLC05-00	FHAC-M2SCLC05-00	5 meters	SC	LC
FHAC-M1SCLC10-00	FHAC-M2SCLC10-00	10 meters	SC	LC
FHAC-M1SCLC20-00	FHAC-M2SCLC20-00	20 meters	SC	LC
FHAC-M1SCLC30-00	FHAC-M2SCLC30-00	30 meters	SC	LC
FHAC-M1SCLCxx-00	FHAC-M2SCLCxx-00	Custom	SC	LC

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10 APPENDIX D

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10.1 FPDP Information

This section provides a brief discussion of Front Panel Data Port (FPDP). For more information about FPDP, refer to Front Panel Data Port Specifications, ANSI/VITA 17-1998 or go to the VITA website at: www.vita.com/vso/. The SL240 PCIe cards implement a serial version of FPDP on their link interface, which is standard VITA 17.1. Most of the concepts from the parallel FPDP specification are applicable to the Serial FPDP world, so they are described here.

Many real-time systems require high-speed, low-latency data transfers on a sustained basis. However, the primary bus (for example, VME bus) cannot provide the required bandwidth and latency at all times because of bus contention. The primary bus must also handle other tasks such as system control. The FPDP bus provides a solution to this problem. Using FPDP, two or more cards are connected by a simple, parallel, synchronous interface using 80-conductor ribbon cable running across the cards' front panels or through a 2.5 Gbps serial interface. For parallel FPDP, devices on the FPDP bus must consist of one FPDP Transmit Master (FPDP-TM) and one FPDP Receive Master (FPDP-RM). Multiple FPDP Receiver (FPDP-R) devices may also exist on the bus. For Serial FPDP, there is one master for the bus (which acts as FPDP-TM and FPDP-RM), and one or more receiver nodes. Since only one FPDP-TM can exist on the bus, no bus contention between devices is possible. Figure 8-1 shows an example VME FPDP card interconnection using parallel FPDP.

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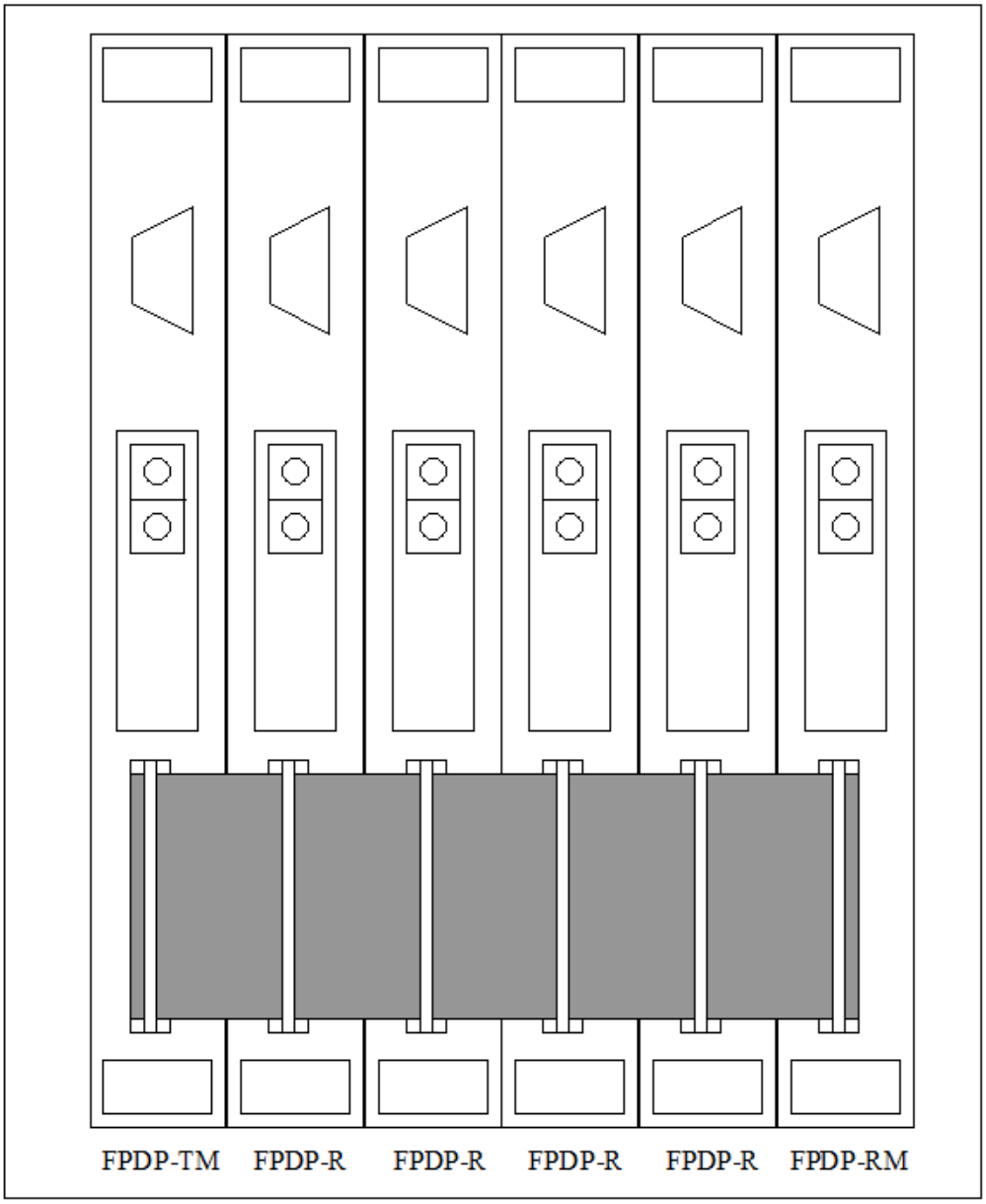


Figure 8-1 Example Configuration With Multiple VME FPDP Cards Connected

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Several advantages of an FPDP interface include:

- Simple hardware is required to interface to FPDP.
- FPDP does not interfere with the normal bus operations—VME or PCI traffic can continue without data transfers wasting bus bandwidth.
- No bus contention is possible because there is only one transmitter.
- No special backplane is required.
- FPDP allows connections from VME chassis to VME chassis.
- Systems may have multiple FPDP buses and thus provides scaleable bandwidth.
- Multiple FPDP busses may coexist in one chassis.
- Throughput can be accurately computed in the design stage.
- Little software development is required to move data between cards.
- Framed or unframed data may be transmitted across the FPDP link.
- Low latency.

Some additional advantages of parallel FPDP are:

- Low cost, 32-bit parallel interface provided through a ribbon cable.
- 160 MBps sustained data rate.

Some additional advantages of Serial FPDP are:

- Noise immune fiber-optic interface.
- Significantly increased transmission distance (10 km).
- Standard cards for parallel FPDP, custom backplanes, PCI (PCI/PMC), and others available.

10.2 Terminology

Some FPDP specific terms are defined below.

FPDP TRANSMIT MASTER (FPDP-TM)

An FPDP-TM is a device that transmits data and timing signals onto the FPDP bus. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-TM may exist on an FPDP bus.

FPDP RECEIVE MASTER (FPDP-RM)

An FPDP-RM is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-RM may exist on an FPDP bus.

FPDP RECEIVER (FPDP-R)

An FPDP-R is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. As opposed to the FPDP-RM, this device does not terminate any bus signals on parallel FPDP. Multiple FPDP-R devices may exist on an FPDP bus.

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10.3 Parallel FPDP Theory of Operation

10.3.1 Clock Signals

A single FPDP-TM generates a free-running clock. This clock frequency determines the maximum transfer rate on the bus. FPDP provides both a PECL (Positive Emitter Coupled Logic) and TTL strobe on the bus, with the PECL clock used for higher frequency (> 20 MHz) transfers. If designing to the CMC card, only an LVTTL clock is generated by the card's FPDP transmitter port, since it is driving to a PCB instead of a long ribbon cable.

An FPDP receiver card (FPDP-R or FPDP-RM) accepts the PECL or TTL clock generated by the transmitter and uses it as the word clock for the data transfers. This clock is generally in the range of 0 to 40 MHz on standard FPDP busses, though the FPDP specification does not state a hard maximum frequency at which the bus may be run. The CMC card has a LVTTL clock input that it uses for the word clock.

10.3.2 Data Framing

The FPDP specification does not allow for the transmission of address information. However, many systems have data coming from several cards or channels. The way to identify data from each channel is through framing. A synchronization pulse signal, /SYNC, was defined for framing purposes. The frame size is defined as the number of data items in the frame. Unframed data may also be transmitted onto the FPDP bus. The four data frame types defined by the FPDP specification are listed and described below.

- Unframed data
- Single frame data
- Fixed size repeating frame data
- Dynamic size repeating frame data

UNFRAMED DATA

- Used when the source and the organization of the data is not important.
- Used when the FPDP receivers do not need to be synchronized to the data stream.
- /SYNC is not required.

When unframed data is transmitted onto the FPDP bus, no synchronization is required. Thus, the FPDP-TM must not generate /SYNC, and the FPDP-RM and FPDP-R devices must not require a /SYNC pulse in order to correctly receive data.

SINGLE FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs between data blocks.
- /SYNC must be asserted before /DVALID is asserted.
- Synchronization occurs infrequently, perhaps only once.

When single frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse before valid data starts being transmitted. Valid data is transmitted when the data valid signal /DVALID is asserted. Thus, a /SYNC pulse must be asserted before /DVALID is asserted when transmitting single frame data. After a /SYNC pulse is asserted, the FPDP-RM and FPDP-R devices should not accept data until the first STROBE period after /DVALID is asserted. The /SYNC pulse does not have to be asserted again until before the start of the next data transmission.

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FIXED SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- All data frames are the same size.

When fixed or dynamic size repeating frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse while /DVALID is already asserted. The /SYNC pulse must be asserted at the same time as the last data item of every frame. The FPDP-RM and FPDP-R devices must recognize that the current data is the last data item in current frame when both /SYNC and /DVALID are asserted. Since /SYNC is asserted at the end of a frame, the first data frame transmitted will not be synchronized. As a result, the system designer may wish to discard this first unsynchronized data frame. All data frames are the same size when fixed size repeating frame data is transmitted.

DYNAMIC SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- Data frames may vary in size.

For dynamic size repeating frame data, the behavior of the /SYNC pulse is the same as for fixed size repeating frame data, with the exception of varying sized frames.

10.4 Serial FPDP Theory of Operation

The protocol and framing for Serial FPDP are listed in Appendix C. Serial FPDP operates similar to parallel FPDP with respect to maintaining data framing with the SYNC signal, but the SYNC signal does not correlate with data frames on the fiber. Any form of data framing listed in section 8.3.2 can be mapped to Serial FPDP, since the data stream and SYNCs are maintained. However, the timing may not be exactly the same as the parallel FPDP version due to link framing overhead and the fact that the link operates asynchronously to the parallel FPDP frequencies.

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10.5 Parallel FPDP Signal Timing

Figure 8-2 shows the timing for several FPDP interface signals. This figure is accurate for all four data framing types. See section 8.3.2 for a discussion of framing. The Data Valid signal, /DVALID, is asserted by the FPDP-TM when valid data is transmitted onto the FPDP bus but not before at least 16 STROBE periods have occurred. The FPDP-TM must de-assert /DVALID when no more data remains in its buffer until valid data is again available. To avoid losing data when the receiver's FIFO is almost full, the receiver (FPDP-RM or FPDP-R) must assert the /SUSPEND signal to hold off the transmitter. The FPDP-TM must de-assert /DVALID within 16 STROBE periods and keep it de-asserted until /SUSPEND is de-asserted. Per the FPDP specification, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least one STROBE period before re-asserting /DVALID. With the FibreXtreme SL240 PCIe card, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least two STROBE periods before re-asserting /DVALID. The /SUSPEND signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

The FPDP-TM must not transmit data onto the FPDP bus until the Not Ready signal, /NRDY, is de-asserted by the FPDP-RM and FPDP-R devices. The FPDP-RM and FPDP-R devices must assert /NRDY when they are not ready to accept data and must de-assert /NRDY otherwise. The /NRDY signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

As required by the *Front Panel Data Port Specifications, ANSI/VITA 17-1998*, the FPDP-TM transmits the Data Direction signal /DIR.FPDP-RM and FPDP-R devices may receive /DIR. The /DIR signal is not given a firm definition of use. Possible uses of this signal include providing a status indication available to be read by software or to allow operation to be inhibited until /DIR is asserted. The /DIR signal may be asynchronous with other FPDP signals. An SL240 PCIe FPDP-R or FPDP-RM inverts and passes this signal from the FPDP interface to the link interface. DIR is an active-high signal on the link interface. /DIR is an active-low signal on the FPDP interface.

Two user-defined Programmable I/O (PIO) signals, PIO1 and PIO2, are reserved in the *Front Panel Data Port Specifications*. These are auxiliary signals, and are not required for core FPDP functions. However, these signals can be user-defined to allow the FPDP-TM, FPDP-RM, and FPDP-R devices to transfer information that is not part of the FPDP specifications. The FPDP-TM, FPDP-RM, and FPDP-R devices must not drive either of the PIO lines immediately at power up of the system. This is to avoid the possibility of two devices driving the same PIO line simultaneously and causing damage to the driver device.

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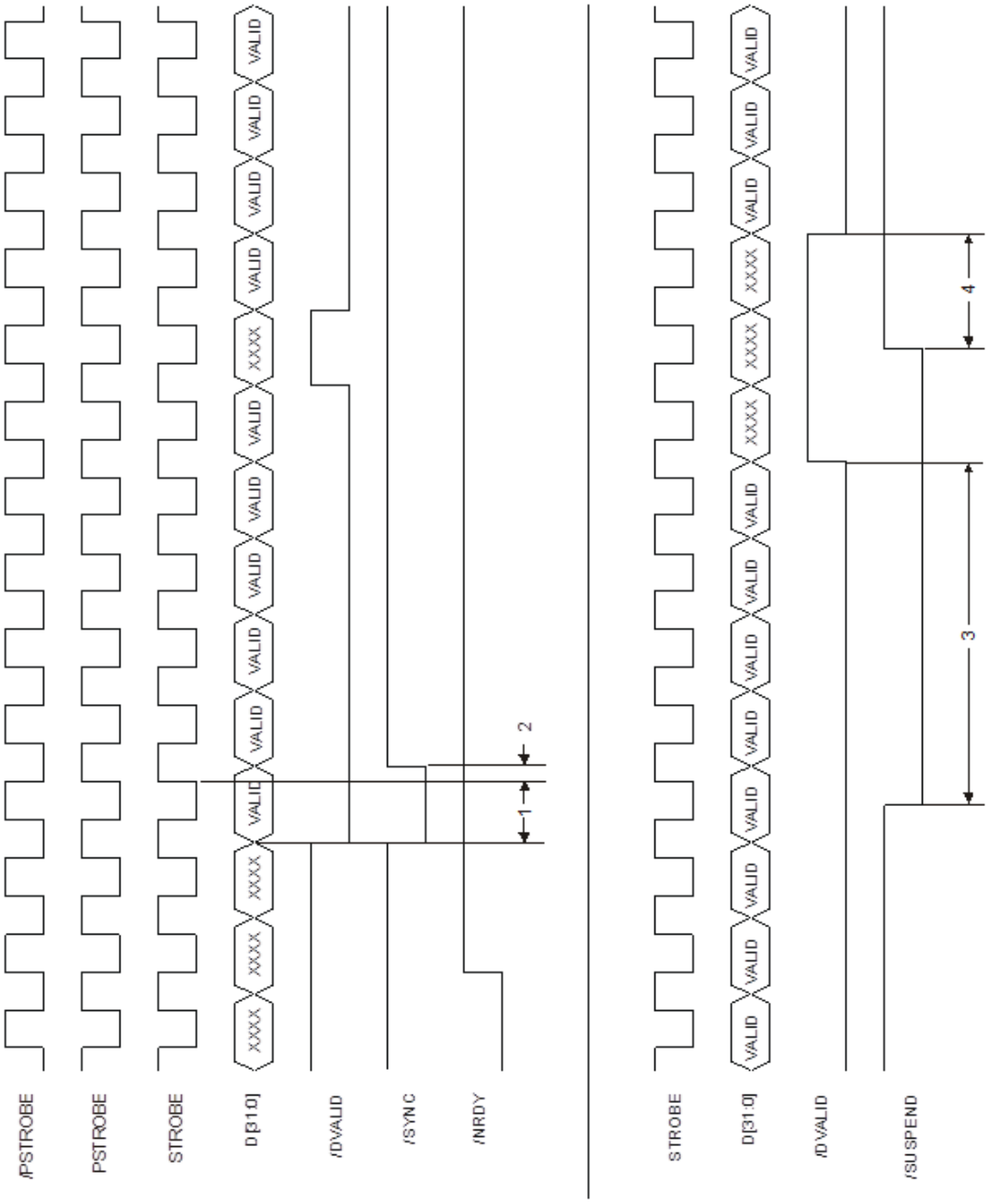


Figure 8-2 Parallel FPDP Interface Timing Diagram

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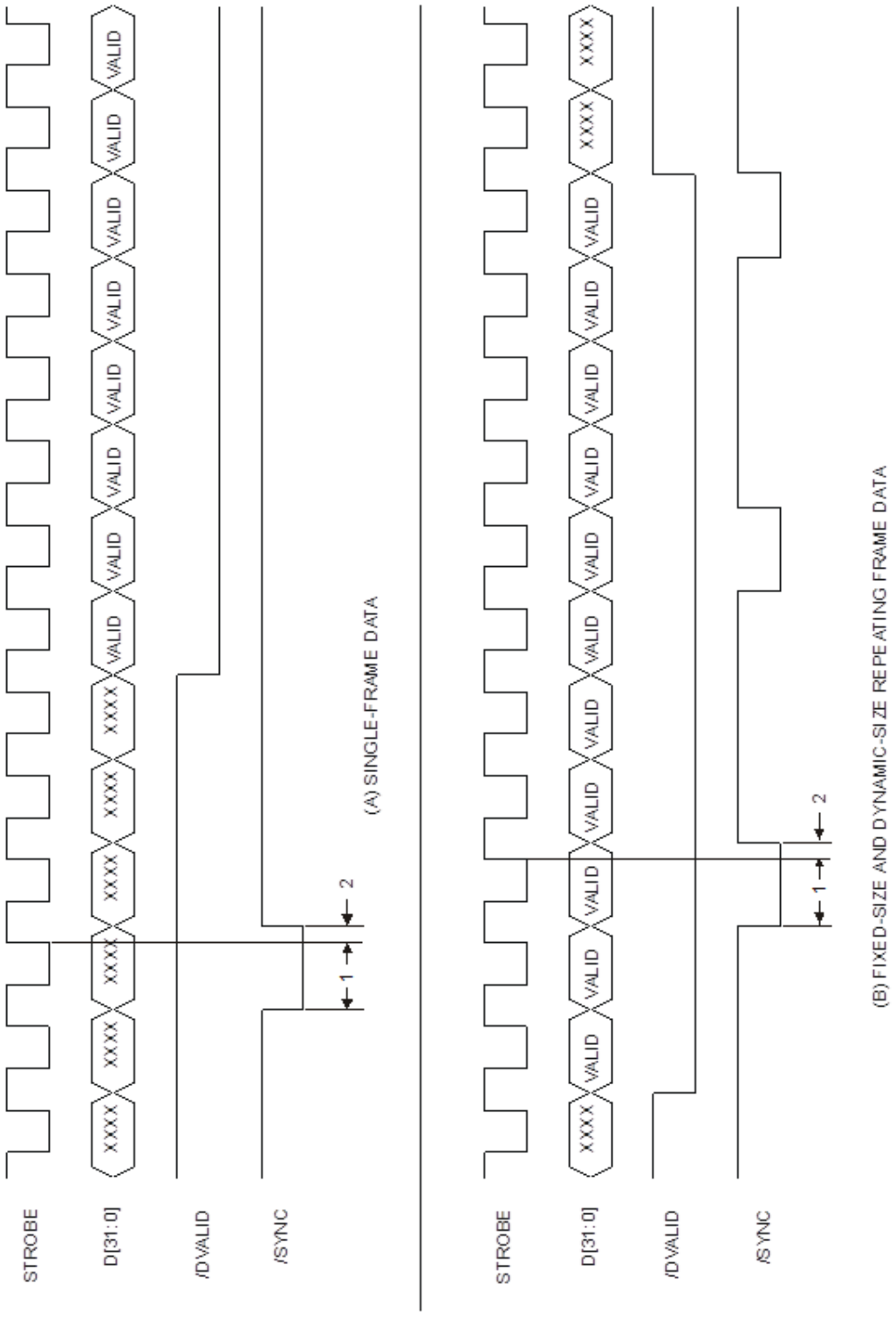


Figure 8-3 FPDP Timing Diagrams Showing the Use of Framing

The timing parameters from Figure 8-2 and D-3 are detailed in Table 8-1 and D-2. These timing specifications are taken from Front Panel Data Port Specifications, ANSI/VITA 17.

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Table 8-1 Parallel FPDP Timing Specifications

Parameter	Description	At Transmitter End of Cable	At Receiver End of Cable	FPDP Clock Used
1	Data, /DVALID, / SYNC setup time	6.0 ns min.	5.0 ns min.	TTL
1	Data, /DVALID, / SYNC setup time	5.5 ns min.	4.5 ns min.	+/- PECL
2	Data, /DVALID, / SYNC hold time	12.8 ns min.	11.8 ns min.	TTL
2	Data, /DVALID, / SYNC hold time	12.0 ns min.	11.0 ns min.	+/- PECL

Table 8-2 FPDP Transmitter Interface Timing Specifications

Parameter	Description	Min	Max
3	/SUSPEND asserted to data stop	---	16 clocks
4	/SUSPEND de-asserted to data started	1 clock	---

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- 3 -

3U 4-3

- 6 -

6U 4-3

- A -

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auto-negotiate 4-4

- B -

bi-directional 4-8
broadcasting 4-8
bus slot 6-3

- C -

clean 5-5
CMC 4-3
CompactPCI 4-3
connector 4-5
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CRC 6-4, 6-6

- D -

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DVALID 6-5

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- F -

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- H -

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- M -

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- N -

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- O -

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- V -

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VITA 17.1 8-3

- W -

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