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ADC128F1

8 Channel, 12-bit, ±10 V Simul-Sampling A/D Converter User Manual

Document No. B-T-MU-ADC128F1-A-0-A2

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SYSTRAN Corporation
4126 Linden Avenue
Dayton, OH 45432-3068
(513) 252-5601

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GLOSSARY

[x:y]. Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte. 8 bits.

byte-lane. 8 bits of a data bus on octal boundaries.

CAE. Computer Aided Engineering.

CVT. Current Value Table consisting of eight current value registers.

DOES. Default Output-Enable State.

doublewide. An IPack module that is twice the size of a standard IndustryPack module.

EPLD. Erasable Programmable Logic Device.

ID PROM. The circuitry that presents the proper data patterns to the lower 8 bits of the IPDbus during the ID (read) transfers.

IndustryPack. Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O. Input/Output.

IPack. Refers to the IndustryPack standard.

IPack logic bus. A synchronous, 4 M transfers/sec, 16- or 32-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6 bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 M words of memory space per IPack module.

IPDbus. IPack Data Bus.

MTBF. Mean Time Between Failures.

ns, µs, ms Nanoseconds, microseconds, and milliseconds respectively.

PC. Personal Computer.

QSOP. Quarter-sized Small Outline Packages.

SAR. Successive Approximation Register. A popular analog-to-digital conversion technique. (e.g. SAR-based ADC technology).

singlewide. An IPack printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL. Very high speed integrated circuit Hardware Description Language.

1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for SYSTRAN's 8-channel, 12-bit, ±10 volt Single-ended Inputs, Simul-sampling Analog to Digital Converter (ADC) IndustryPack (also called IPack) board, referred to in this manual as the ADC128F1 (part number BHAS-ADC128F1).

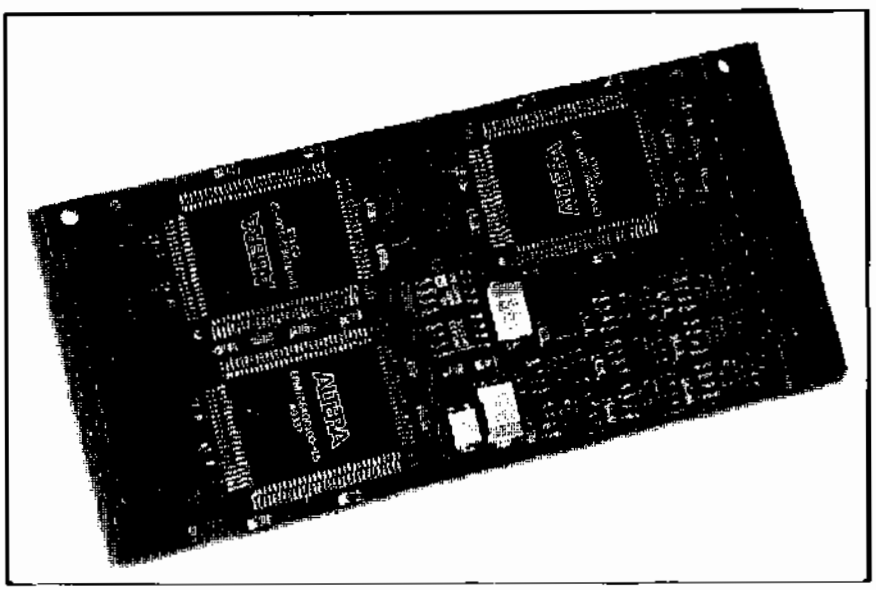


Figure 1-1 ADC128F1 Board

1.2 Scope

This reference manual covers the physical and operational description of the ADC128F1, both from hardware and software perspectives. This manual also contains detailed technical information about the ADC128F1's performance characteristics, and some typical applications. The reader should have a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IPacks on their carrier(s) of choice. Citation of equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The ADC128F1 is a singlewide IPack board, conforming both mechanically and electrically to the *IndustryPack Logic Interface Specification, revision 0.7.1.* For a typical IPack carrier that holds four IPacks, the ADC128F1 can provide up to 32 channels of high-per-

formance ADCs in a single slot on a computer bus backplane, or be mixed with other IPacks for a more customized, modular I/O system solution.

The ADC128F1 is designed to maintain the highest possible accuracy and performance characteristics by minimizing accumulative analog errors in the design by using the best (yet, reasonably affordable) components for the tasks to be accomplished.

1.3.1 The Name

The product name of ADC128F1 consists of several descriptive components. The ADC portion indicates its primary function of performing analog to digital conversions. It has dedicated converters per channel. If it contained a multiplexer feeding a single ADC then its leading field would be "ADM", for analog-to-digital, multiplexed. The next "12" field indicates the number of bits of resolution (not accuracy). The "8" indicates how many analog input channels are available. The last "F1" indicates that the input range is fixed and that the span is ±10 volts.

1.3.2 Features

- Eight independent channels of 12-bit, switched capacitor SAR-based ADCs with all channels tightly-coupled for "true" simultaneous sampling and conversion at a free-run rate of 115,942 samples/second/channel, for a board total of 927,536 samples/second.
- Automatic power-up of all eight ADC channels converting and depositing results simultaneously into a current value table (CVT) every 8.625 µs.
- Modes of operation vary from simply reading the latest results from the CVT through software and hardware handshake interfaces for loosely and tightly coupling multiple ADC128F1 IPacks together for large, ganged simul-sampling applications.
- Elimination of "extra" analog circuitry results in highest accuracy available. Both the relative and differential nonlinearity specifications are guaranteed to ±1 LSB (maximum). Typical accuracy is 11½ bits.
- Real-time digital monitor port on I/O connector allows external access to the CVT contents.
- The single-ended inputs can accept voltage inputs to ±10.000 volts, with an input resistance of 16 KΩ.
- The board operates on the carrier's +5 volt supply only, requiring ≈200 mW of power per channel.
- A buffered +2.500 V reference voltage is supplied to the I/O connector.
- Output data coding is two's complement: 800 *hex* @ -10.000 volts input → FFF *hex* @ ≈ -0.005 volts; 000 *hex* @ 0.000 volts → 7FF *hex* @ +9.995 volts.

- Output data coding is two's complement: 800 *hex* @ -10.000 volts input → FFF *hex* @ ≈ -0.005 volts; 000 *hex* @ 0.000 volts → 7FF *hex* @ +9.995 volts.

1.4 Specifications

MECHANICAL: Singlewide IPack

- Measurements: 1.800" x 3.900" x 0.303" (connectors, above board)
  4.572 x 9.906 x 0.770 cm
  Note: 0.127. (0.323 cm) maximum component height
- Weight: 1.012 oz., 28.68 grams
- Board thickness: 0.062"(0.157 cm) nominally, (4 layer)

ELECTRICAL: Singlewide IPack Transfers

- 8 MHz clock rate
- No WAIT cycles on any transfer types
- HOLD cycles supported on all transfer types supported
- Complete (no partial) address decoding
- I/O transfers: 8- or 16-bit writes, 16-bit reads
- Ten I/O locations:
  - 8 for ADC data values
  - 1 for control
  - 1 for status
  - Maximum read/write rate: 4 MTransfers/second, sustained
  - no zero-fills on IPD[15:12]
- ID Transfers: 8- or 16-bit read (only)
  - Data presented on IPD[7:0]
  - no zero fills on IPD[15:8]
  - Twelve bytes, including CRC
  - SYSTRAN's manufacturer's ID 45 *hex*, E ASCII
  - ADC128F1's model number 6A *hex*, j ASCII
  - Cyclic Redundancy Check value 6A *hex*
  - Maximum read rate: 4 MTransfers/second, sustained
- Memory transfers: not supported
- Interrupt Vector transfers: not supported
- Interrupt requests: none generated
- DMA activity: none supported
- No acknowledgement on unsupported transfer attempts:

- Memory read and write, Interrupt read, ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

- "N_SUPDIS", software update disable, is negated to allow CVT updates to take place
- All ADCs converting with deposition of data into CVT, assuming no hardware connections at "N_HUPDIS" and "RUN", or "N_HUPDIS" is negated high and "RUN" is asserted high
- No accesses permitted or acknowledged during RESET
- Data is not accurate to specification until after 25 ms following application of power

POWER REQUIREMENTS

- Power: +5 Vdc @ 327 mA (typical, no monitor loads, open inputs)
  +12 Vdc @ 0A
  - 12 Vdc @ 0A

PERFORMANCE CHARACTERISTICS

- Timing: Refer to section 5.0 on Performance
- Analog (ADCs):
  - Signal to Noise (distortion) Ratio = 70 dB minimum for 10 KHz Sine wave input
  - Total Harmonic Distortion = -80 dB maximum for 10 KHz Sine wave input
  - Peak Harmonic Distortion = -80 dB maximum for 10 KHz Sine wave input
  - Intermodulation Distortion = -80 dB maximum for both 2nd and 3rd order terms (Fa = 9 KHz and Fb = 9.5 KHz)
  - Minimum resolution = 12 bits with no missing codes, guaranteed
  - Relative accuracy = $\pm \frac{1}{2}$ LSB (typical), ±1 LSB (maximum)
  - Differential nonlinearity = ±1 LSB (typical and maximum)
  - Positive full-scale error = $\pm 1\frac{1}{2}$ LSB (typical), ±3 LSB (maximum)
  - Bipolar zero (offset) error = ±2 LSB (typical), ±4 LSB (maximum)
  - Negative full-scale error = $\pm 1\frac{1}{2}$ LSB (typical), ±3 LSB (maximum)
  - Input voltage range ±10 volts
  - Input resistance 33 KΩ (typical), 16 KΩ (minimum), internally buffered to present a benign, non-changing input current to user's source
  - Reference input current 1μA (maximum) due to internal buffering within the ADC
  - 1 LSB = $20^{volts}/4096 \approx 4.88$ mV

- Analog (Reference)
  - Output voltage +2.500, ±0.010 volts (maximum, over temperature)
  - Output voltage drift = 10 ppm/°C (typical), 25 ppm/°C (maximum) 4.375 mV (maximum, over temperature)
  - Output settling time 25 ms to within 250 µV of final value after application of power

ABSOLUTE MAXIMUM VOLTAGES ‡:

- Supply voltage with respect to ground: -0.3 V (minimum), +7.0 V (maximum)
- Analog inputs: ±17 volts

‡ Stresses above those listed may cause permanent damage to the components on the ADC128F1. Operating the ADC128F1 beyond the recommended ratings for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS:

- Supply voltage: +5.00, ±0.25Volts
- Logic Interface: IndustryPack specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

- Temperature (Operating): 0°C → +70°C
- Temperature (no bias, storage): -40°C → +125°C
- Humidity (non-condensing): 5% → 95%
- Vibration (Operating): 10 G's RMS, 10 → 55 Hz, random
- Shock (Operating): 50 G's maximum, any axis
- Altitude (Operating): 10,000'- maximum

MEAN TIME BETWEEN FAILURES (MTBF):

- 2,923,977 hours per MIL-HDBK-217F

1.5 Related Products

- Software: 'C' library and OS-9 device driver routines with documentation.
- ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

1.6 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp. (This Synopsis is included in this document as Appendix A).
- SYSTRAN I/O Products Technical Note #2001 titled *Programmed Transfer Rate Analysis of the IndustryPack Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001-A-0-A1)
- *IndustryPack Logic Interface Specification Revision 0.7.1* published by Greenspring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.7 Ordering Process

If you wish to learn more aboutr SYSTRAN products or to place an order, the following contacts are available:

- Phone: **(513) 252-5601**
- E-Mail address: **info@systran.com**
- World Wide Web address: **http://www.systran.com/**

1.8 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any and all technical questions that might arise concerning the use of this product. SYSTRAN also publishes and distributes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct questions not satisfactorily answered by this document, or concerns about the functional-fit of this product for your particular application, or programming questions, to the factory at **(513)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance. Our goal is to help you solve your problem.

Refer to Section 7.0 for warranty and repair information.

1.9 Reliability

SYSTRAN Corporate policy is to provide the highest quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

SYSTRAN has developed a Quality System which conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard is the most comprehensive of the conformance standards, in that it addresses all 20 clauses of the ISO quality system requirements.

SYSTRAN's Quality System addresses the following basic quality objectives:

- Achieve, maintain and continually improve the quality of SYSTRAN products.
- Improve the quality of its own operations to meet the needs of SYSTRAN customers and stakeholders.
- Provide confidence internally that quality is being fulfilled, maintained and improved.
- Provide confidence to the customer and other stakeholders that requirements for quality will be achieved in the delivered product.

SYSTRAN's Quality System was assessed by BSI QA, which is the certification division of British Standards Institution, the largest and most respected standardization authority in the world. SYSTRAN's Quality System was found to meet or exceed the international standards in all areas, and Certificate of Registration number FM 31468 was issued to SYSTRAN on May 16, 1995.

The scope of SYSTRAN's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's program of continuing assessment, under which an audit of the quality system is performed by BSI QA every six months. The first such Continuing Assessment was conducted by BSI QA on November 1, 1995.

SYSTRAN Corporate policy is to provide the highest-quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

An integral part of SYSTRAN quality and reliability goals is customer feedback. Customers are encouraged to contact the factory with any questions or suggestions regarding unique quality requirements, or to obtain additional information about our programs. SYSTRAN's commitment to customers includes, but is not limited to:

- Professional and quick response to customer problems utilizing SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

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SYSTRAN provides products and services that meet or exceed the best expectations of our customers.

- All products are tested using an Automatic Test Equipment system, with samplings for all product types taken through extended testing scenarios that include stress testing for voltage and temperature ranges beyond specifications.
- All products receive a predictive reliability rating based upon a calculated MTBF utilizing the MIL-HDBK-217F. Field failures are continuously logged and evaluated for potential failure modes and trends.
- Other environmental parameters are guaranteed by design, and not tested.
- Design reliability is ensured by methodology (top-down CAE design, VHDL, synthesis, extensive all-cases simulation, ALPHA build and test, and BETA testing if required) with full concurrent engineering practices throughout.

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2.0 DESCRIPTION



NOTE: The IPack signal references, transfer and cycle types discussed in this document are explained in detail in the *IndustryPack Logic Interface Specification Synopsis* included as Appendix A.

2.1 Simplified Block Diagram

Figure 2-1 is a simplified block diagram of the ADC128F1.

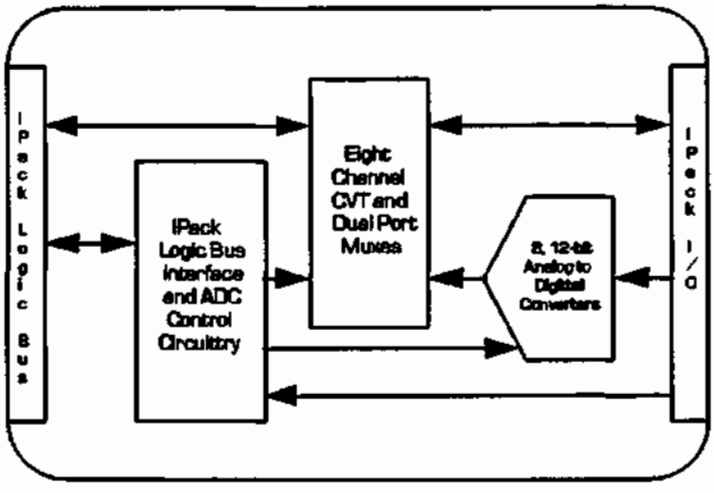


Figure 2-1 ADC128F1 Simplified Block Diagram

2.1.1 Block Descriptions

IPACK LOGIC BUS INTERFACE AND ADC CONTROL CIRCUITRY

On the left side of the diagram is the IPack Logic Bus connector through which all transfers between the IPack carrier and the ADC128F1's registers and data sources are conducted. The block labeled "IPack Logic Bus Interface and ADC Control Circuitry" contains all of the board level control/status registers, the ID PROM data, the main ADC sequence engine, the current value table update and access control logic, and IPack transfer sequence/control and data bus interface logic.

EIGHT CHANNEL CVT AND DUAL PORT MUXES

This block consists of two EPLD devices each implementing support for four analog-to-digital convertors including the serial-to-parallel convertors and current value tables for each, with a pair of data port multiplexers, one for carrier accesses and one for the data monitor port on the user's I/O connector.

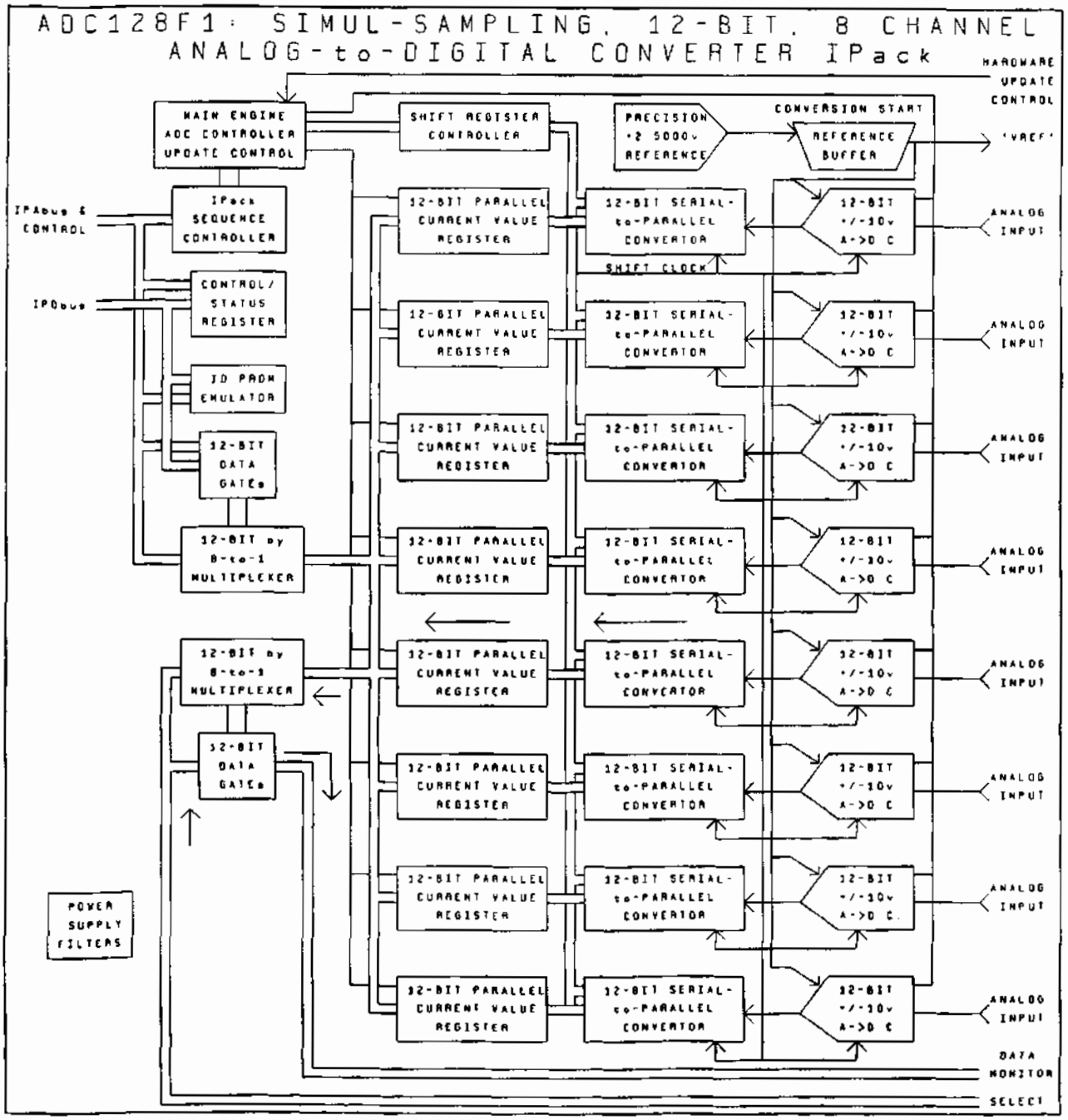


Figure 2-2 ADC128F1 Detailed Block Diagram

8-, 12-BIT ANALOG TO DIGITAL CONVERTERS (ADC)

This block consists of eight separate, tightly-coupled (in time) converters, with their precision voltage reference (not shown) and a buffered reference output. On the right side of the diagram is the ADC128F1 I/O connector, providing eight single-ended inputs to the ADCs, an analog output providing the reference, hardware handshake interface control and status lines, monitor access to any channel's CVT data with select signals; and ample ground connections.

2.2 Detailed Block Diagram

Figure 2-2 is a detailed block diagram of the ADC128F1. As in Figure 2-1, the carrier connections are on the left side, lumped by signal groups of data bus (IPDbus), address and control signals (IPAbus and CONTROL, respectively), and power supply connections (not shown).

2.2.1 Block Descriptions

MAIN ENGINE ADC CONTROLLER UPDATE CONTROL

The block labeled "Main Engine ADC Controller Update Control" (top left) provides all of the proper sequencing circuitry for executing conversions, as directed by both software and hardware handshake interfaces, including the control logic to perform data extraction from all eight ADCs, with subsequent serial-to-parallel conversion on that data. The process ends with a simultaneous updating of all eight current value registers (collectively referred to as the Current Value Table (CVT)).

IPACK SEQUENCE CONTROLLER

The block labeled "IPack Sequence Controller" provides all of the circuitry with responsibilities for:

- Detection of valid I/O and ID transfer operations within their respective fully decoded address ranges, including the support of HOLD cycles when generated by a carrier
- ID PROM data multiplexer and port control signals
- Control/status registers' write and read control signals
- CVT multiplexer and read gate control signals.

CONTROL/STATUS REGISTER

This block consists of a single bit control register with readback, and a 6-bit read gate for monitoring the status of various other important signal states. The "ID PROM Emulator" is the circuitry that presents the proper data patterns to the lower 8-bits of the IPDbus dur-

ing ID transfers. Emulating the never-changing ID information in this way reduces parts count and costs, and increases system reliability and its associated MTBF value.

All of the block elements discussed in this paragraph are contained in the "IPack Logic Bus Interface and ADC Control Circuitry" block in Figure 2-1.

SERIAL-TO-PARALLEL CONVERSION

The majority of the circuitry depicted in Figure 2-2 (primarily in the vertical middle) consists of eight sets of serial-to-parallel convertors feeding eight separate 12-bit parallel registers that all feed two sets of 12-bit wide, eight-to-one data multiplexers. This circuitry, depicted as "Eight Channel CVT and Dual Port Muxes" in Figure 2-1, is housed within two large EPLDs. The actual sectioning of circuitry is accomplished through support of four ADCs each, with four serial-to-parallel convertors, and four 12-bit current value registers feeding two multiplexing port controllers that handle half of the CVT presentation duties. The far right side of Figure 2-2 shows all eight 12-bit ADCs feeding their respective (data) serial-to-parallel convertors.

PRECISION 2.500 VOLT REFERENCE

All eight ADCs operate from a single "Precision 2.500 volt Reference", which also is buffered and presented to the I/O connector.

2.3 Architecture

A short presentation of the rationale behind the architecture of the ADC128F1 may lend some understanding as to why this particular IPack was developed in its current configuration.

2.3.1 Minimum Software Requirement

All too frequently an analog-to-digital converter board is supplied with nearly no value-added logic to make the interface easy to use. For this type of board it generally means that the user must write a lot of software to actually make the board work. Typically, this involves the process of:

- selecting a channel to convert
- implementing a delay mechanism to allow the input signal to settle to its final value
- activating a signal hold operation
- starting the actual conversion
- spin-lock reading the conversion status or waiting on an interrupt to occur indicating that the conversion is complete
- finally fetching the data.

Experience has shown that this requires:

- a significant amount of time (and its associated costs) to develop software and get it working
- usually adding a lot more CPU power to a system to handle these processes, along with its associated costs, etc.

Although all I/O interfaces require some software, SYSTRAN's primary goal for all the I/O products is to minimize the software requirement as much as possible. That philosophy has resulted in the development of the architecture being presented.

2.3.2 Resolution Versus Accuracy

Another note about the ADC128F1 architecture concerns resolution versus accuracy. This one-sentence "sermon" basically states that one should only provide the resolution that indicates real information.

If you are using a voltmeter that can accurately measure only ±1.999 volts (a common 3½ digit display), then no additional information is provided by writing a voltmeter reading as +1.1000 volts. It is simply a false statement.

The same is true for analog-to-digital conversion subsystems. If an analog multiplexer, gain stage amplifiers, anti-aliasing filters, and a separate track/hold amplifier are placed on the front-end of a 12-bit ADC, the real accuracy is typically around 9 bits; certainly no where near the 12 bits being provided as a conversion result.

For the sake of maintaining the maximum conversion accuracy possible, the input signals to be converted by the ADC128F1 are fed directly into their respective ADCs with no other circuitry present to increase noise or decrease accuracy.

2.4 General Description

The ADC128F1 has various levels of user interface capabilities which should be presented before a detailed description of this IPack is undertaken. This top-level presentation should assist the reader/user in understanding why certain features and functions exist on the ADC128F1. The functional spectrum of useability includes "power-up and read" through "tight acquisition control".

2.4.1 Application Descriptions

FREERUN A SINGLE ADC128F1

For those applications where it is not important to know exactly when the last analog-to-digital conversion occurred, within a certainty of less than 8.625 µs, use of the ADC128F1 is as simple as applying power and reading the first eight I/O locations as the application requires. All eight channels on each ADC128F1 are tightly-coupled (to within

a few nanoseconds) and freerun at a sampling and automatic update rate of 927,536 samples per second per ADC128F1 IPack board. The CVT update is automaticlly blocked during a carrier read of any of the first eight I/O locations. Therefore, if new ADC data is ready to be loaded into the CVT during the 250 ns required to complete the I/O read transfer, then the data being read is already [8.625, +0.000, -0.250] µs old. If a subsequent read is performed before another 8.625 µs has elapsed, it too will be from the older sampling.



NOTE: The important functional feature to remember when using the ADC128F1 in this mode of operation is that there is no certainty that multiple-channel readings taken from a single (or multiple) ADC128F1 board(s) occurred from the same simultaneous sampling of the input signals being converted.

This particular mode of operation is presented in the applications section as 6.2: Freerun A Single ADC128F1.

SINGLE ADC128F1 SNAPSHOT

For those applications that require data to be retrieved from the same instance in time from just a single ADC128F1, a software control signal has been provided to accomplish this minimal-channel snapshot operation.

The only software-control bit on the ADC128F1 is used to deliberately block all subsequent current-value update operations when asserted, even though the ADCs continue to perform conversion operations. This is like a manual override of the automatic update block that occurs during a CVT read operation, as described above. The significant difference in the sampled data in this mode of operation is that all of the data retrieved from the ADC128F1 was derived at the same time (within a few nanoseconds), and has been locked into the CVT by the control bit to allow for subsequent data retrieval at any pace without the fear of losing data due to CVT overwrites. Once the data has been retrieved, the control bit can be negated for subsequent automatic updates to the CVT.

This mode of operation is presented in the applications section as 6.3: Single ADC128F1 Snapshot.

MULTI-BOARD LOOSELY-COUPLED SNAPSHOT

For those applications that require data to be retrieved from the same instance in time per ADC128F1 with up to 8.625 µs of uncertainty across multiple ADC128F1 IPacks, a hardware control line has been provided that functions identically to the software control bit function described above.

At the system level, this configuration can be viewed as being a loosely-coupled simultaneous-sampling data acquisition technique. It is loosely coupled because the uncertainty between the data sets from different ADC128F1 IPacks is up to 8.625 µs, even though the data from all eight channels on any one ADC128F1 is obtained at the same time

(within a few nanoseconds). All of the ADC128F1 IPacks that are to be loosely-coupled for simul-sampling can be hard-wire controlled from one digital output line (like from a DIO316I or TRIDO48). When this "Hardware UPdate DISable" line is asserted, all subsequent CVT updates are blocked on all connected ADC128F1 IPacks. Then all the data can be retrieved at any pace and in any sequence with confidence that all data was captured within a 8.625 µs sampling window (preceeding the hardware signal assertion). Once all of the data is retrieved, the hardware control line can then be negated to permit subsequent CVT updates on all of the ADC128F1 IPacks connected together.

This mode of operation is presented in the applications section as 6.4: Multi-board Loosely-Coupled Snapshot.

MULTI-BOARD TIGHTLY-COUPLED SNAPSHOT

For those applications that require a tightly-coupled, simultaneous sampling of more than eight channels (more than one ADC128F1) that can reside on various carriers, even across various physical chassis, a second hardware control line has been provided for maximum control of the data acquisition process.

By using software timing and a simple digital output signal, or an automatic pulse generation scheme by using either a DUAL16CT or a DUAL32CT IPack, the user can force all channels on all connected ADC128F1 boards to start their sampling at the same time. This is accomplished by providing a normally negated (low) state on the digital control line connected to the "RUN" inputs of the ADC128F1's that are coupled together.

When a sample is desired, provide a single high pulse state for 8.625 µs → 14.000 µs. The uncertainty in the sample acquisition times is primarily a function of when each of the individual ADC128F1 boards "see" the rising edge of the "RUN" control line, which can be fine-tuned with equal lengths of connecting wire if necessary. The data is available for retrieval from all of the ADCs' CVTs 8.625 µs following the rising edge of the "RUN" control signal. Note that when "RUN" is negated (low), the connected ADC128F1 boards are NOT sampling and all of their ADC controllers are reset to a known "zero" state.

This mode of operation is presented in the applications section as 6.5: Multi-board Tightly-Coupled Snapshot.

REAL-TIME DATA LOGGING

For those applications that may require real-time data logging from an ADC128F1, refer to application note 6.6 (ADC Data Stream Logging), which also uses the "RUN" control line described above. This application uses a pair of ADC128F1 boards with a TRIDO48 and FIVEFIFO card to stream-record two channels of real-time data for 8.83 ms at a continuous 115,942 samples per second per channel rate.

REAL-TIME MONITORING

For those applications that require externally accessable, on-line, real-time monitoring of actual ADC data for calibration purposes, a powerful monitor interface has been incorporated into the design of the ADC128F1. This circuitry easily lends itself to being built into an automatic test circuit for realtime "health" monitoring and pre-event/post-event calibration verification processes. This particular feature is highlighted in the applications section as 6.7: Real-time Monitoring.

2.5 Detailed Description



NOTE: Refer to the ADC128F1 schematics located in Appendix B while reading this material since individual components are referenced by functional name, schematic reference designators, or industry-standard device part numbers.

The ADC128F1 was developed using VHDL and Synthesis, and targeted to several Altera EPLDs. The design was schematic-captured and integrated to standard interface devices, connectors and discrete components using VIEWLogic CAE tools. This top-down methodology is evident in the schematics and product design material presented in this document.

2.5.1 ADC128F1 Schematics

For those readers not familiar with the top-down methodology used to develop the ADC128F1, the following is a short presentation on the schematics of the ADC128F1. There are five pages that comprise the schematic set.

TOP LEVEL DRAWING, PART I

The first one, labeled ADSC-IADC128F-6A-A1 (sheet 1 of 2) is half of the top-level drawing, which contains all of the digital circuitry with the carrier's Logic Interface connector. This represents the circuitry contained in the three left blocks of Figure 2-1 and most of the three left columns of blocks of Figure 2-2.

TOP LEVEL DRAWING, PART II

The second page of schematics (ADSC-IADC128F-6A-A1, sheet 2 of 2) presents the remaining circuitry, nearly all of which is the analog circuitry with the I/O connector. This represents the circuitry contained in the two right of Figure 2-1 and the right most column of blocks of Figure 2-2.

SIMUL-SAMPLING ADC CONTROLLER

Again referencing the first sheet of schematics, attention is drawn to the three large blocks that identify each of the three EPLD devices used on this product. "Pushing-down" into the block labeled "S_SADCTRL" produces the third page of the schematics.

This drawing is the netlisted "7064" EPLD that is the Simul-sampling ADC ConTRoLler for the ADC128F1. Its reference designator is U1, and is physically located just under and to the left of the J1 Logic connector in the assembly drawing presented in Figure 2-3.

SERIAL AND PARALLEL REGISTRATION DEVICE FOR CHANNELS 1 TO (2) 4

Pushing-down into the block labeled "S_REG124" generates the fourth page of the schematics. This drawing is the netlisted "7128" EPLD that is the serial and parallel REGistration device for channels 1 to (2) 4. Its reference designator is U2, and is physically located just under and to the right of the J1 Logic connector in Figure 2-3.

SERIAL AND PARALLEL REGISTRATION DEVICE FOR CHANNELS 5 TO (2) 8

Pushing-down into the last EPLD device results in the last page of the schematics. This drawing is the netlisted S_REG528 EPLD that contains the serial and parallel REGistration device for channels 5 to (2) 8. Its reference designator is U10, and is physically located just above and to the right of the J2 I/O connector as presented in the assembly drawing in Figure 2-3.

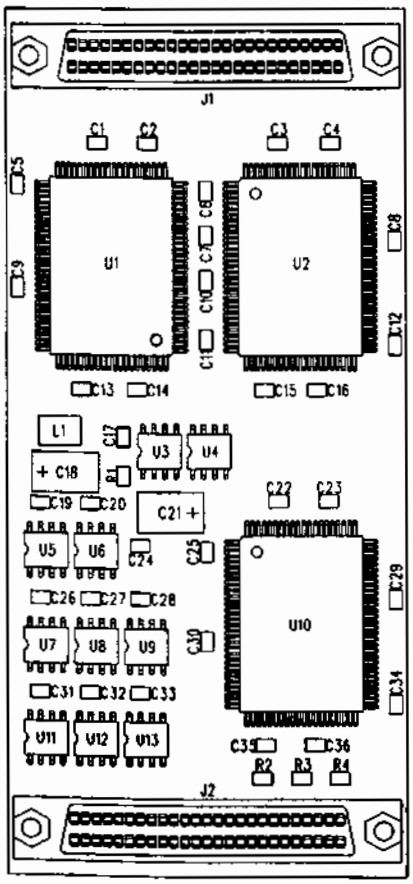


Figure 2-3 ADC128F1 Assembly Diagram

U2 and U10 also contain the dual port multiplexers with gates for presenting CVT information to both the carrier and the I/O connector.

Pushing-down into the three symbols presented on the last three pages of the schematics would reveal hundreds of pages of schematics of synthesized circuitry that are implemented within these three EPLD devices.

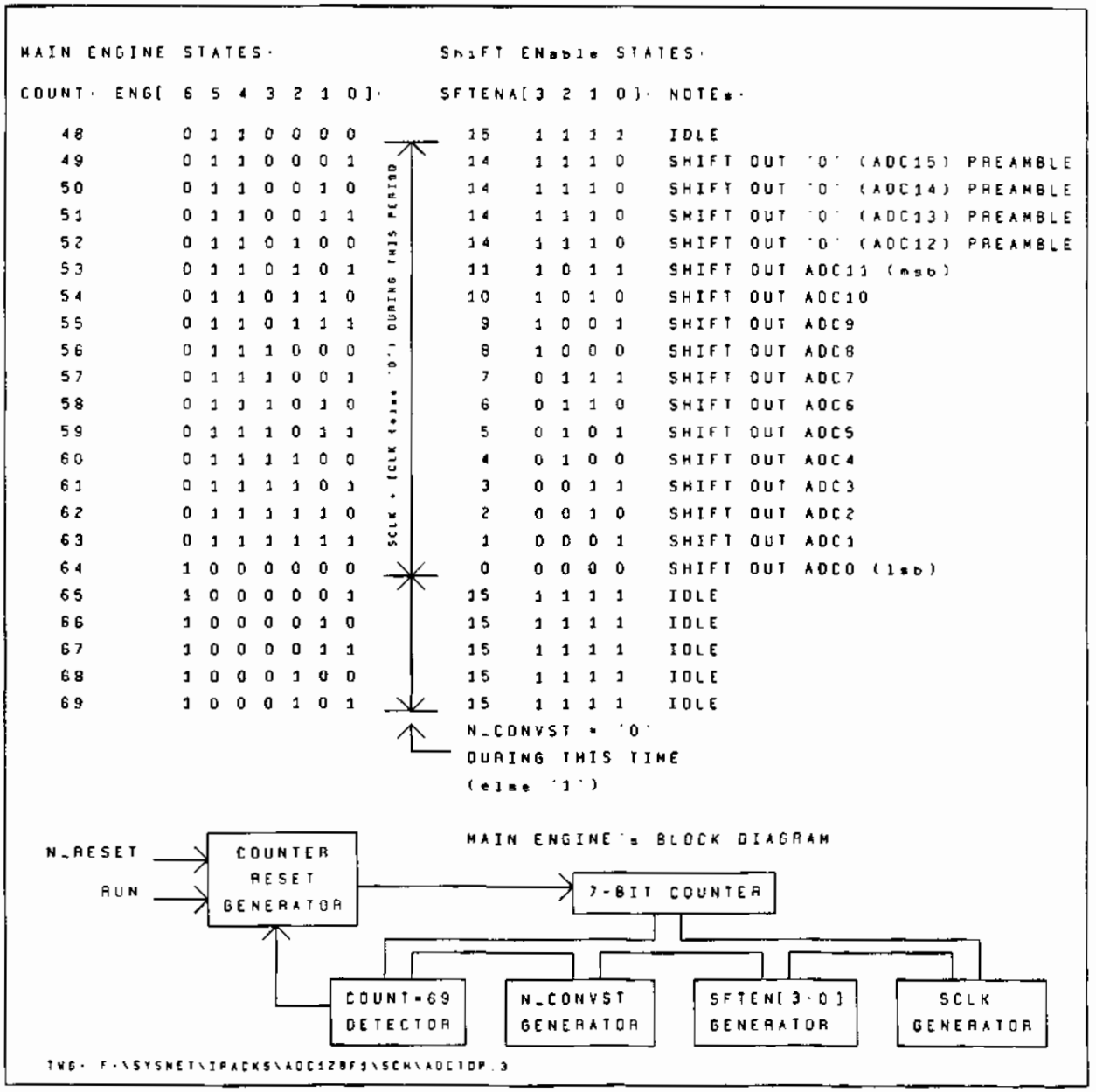


Figure 2-4 ADC128F1 Main Engine Details

2.5.2 Digital Components And Their Functions

All of the discussions in this subsection concern components that are found on the first page of the schematics in Appendix B.

IPACK LOGIC BUS TRANSFERS

All IPack Logic Bus transfers take place across J1, the IPack Logic Connector, located on the left side of all block and schematic diagrams. Refer to Appendix A for details about the signals on this connector. Generally speaking, this IPack does not support DMA or Interrupts, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and (for just one bit) writes to the short, ten location, I/O map.

PRIMARY ACTIVITY CONTROLLER

The ADC128F1's primary activity controller is housed within the "SADCTRL" EPLD at U1. It serves as the primary IPack transfer sequence engine, whose responsibilities include: detection of valid I/O and ID transfer operations within their respective, fully decoded address ranges, including the support of HOLD cycles when generated by a carrier; ID PROM emulation data pattern generation for ID read transfers; and output-enable control signals for use by the other two EPLDs for the proper gating of CVT information onto the IPDbus during I/O read operations from any of the first eight I/O locations.

ADC OPERATION CONTROL

The other primary set of duties performed within SADCTRL is that of controlling all activities related to proper ADC operations. These complex operations are quickly diluted by the subsystem block diagram presented at the bottom of Figure 2-4. Since the ADCs used on the ADC128F1 are small-package, serial-interface devices, the data must be retrieved in an orderly manner with just the right timing to maintain the highest accuracy possible while performing conversions as fast as possible. This is accomplished by a free-running 69-state sequence engine.

The majority of the time, from counts 00 through 48, the activity on the board is minimized to provide a "quiet" time during the actual conversion process. Once the conversion is complete (after 6 µs), the data is extracted from all eight ADCs simultaneously.

The first four bits are leading zeroes and are extracted during the engine's counts of 49 through 52. The next twelve counts shift out real data and are bit-registered by the other two EPLDs as defined by the state of the "SFTENA[3:0]" (Shift Enable) lines, and as clocked out of the ADCs and into the registers by the "SCLK" (Shift Clock) signal. This architecture and technical solution permits the ADC128F1 to actually run at 98.78% of the theoretical maximum capacity for the ADCs selected. Also note that SCLK is a gated ICLK that occurs from counts 49 through 64.

ASSERTED LOW CONVERSION START

The last function performed by SADCTRL for the ADC support is the generation of the N_CONVST (asserted low CONVersion STart) signal which resets the ADCs and starts a new conversion on its rising edge. The external control inputs "RUN" and "N_HUPDIS", with the one software control bit "N_SUPDIS" are used by SADCTRL for state machine control and for the posting of status when required. Additionally, SADCTRL monitors the external control inputs that are used by the other two EPLDs for Monitor Port operations for the sake of posting them as status, when required.

Details concerning the integrated operations between SADCTRL and the ADCs are presented in figures 5-1 through 5-11 of Section 5: PERFORMANCE.

REGISTRATION OPERATIONS

The registration operations contained within the REG124 and REG528 EPLDs are identical for all eight channels. As briefly described above and detailed in timing diagrams in section 5, ADC digital data is serially shifted out of the convertors on the rising edge of SCLK during engine states 49 through 64, and is bit-registered in descending order by the falling edge of SCLK during engine states 53 through 64. The next rising edge of ICLK that starts engine state 65 performs a complete double-buffer parallel registration, of all of the individual 96 data bits captured serially, into the per-channel current value (12-bit) register, collectively called the current value table. This permits the user to gain access to any channel's data at any time regardless of system state without inserting wait-states.

The current value registers within both U2 and U10 are connected to a pair of 12-bit wide bi-channel data multiplexers that are each followed by tristate gate/drivers. One multiplexer and its gates are controlled by SADCTRL for driving CVT information towards the carrier during I/O read operations to the first eight locations, and the other is controlled by four control lines coming from the I/O connector for driving CVT information towards the Monitor Port portion of the I/O connector when applicable.

The eight channel multiplexer that supports the IPDbus is driven by the IPDOE[2:0] and N_IPDOEG signals coming from SADCTRL. Simply, IPDOE[2:0] selects which channel is being accessed and N_IPDOEG asserts low to enable the data onto the IPDbus during the termination cycle of an I/O read from the CVT.

REG124 supplies the data when IPDOE[2:0] = 3 → 0 for channels 4 → 1, respectively.
REG528 supplies the data when IPDOE[2:0] = 7 → 4 for channels 8 → 5, respectively.

The eight channel multiplexer that supports the CVTObus (Current Value Table Output bus) is driven by DATAOE[2:0] and N_DATAOEG signals coming from the I/O connector. Simply stated, DATAOE[2:0] selects which channel is being monitored at the I/O connector and N_DATAOEG is asserted low to enable the data drivers into a low impedance state. This configuration allows many ADC128F1 IPacks to have their monitor ports bussed together, if desired.

REG124 supplies the data to the I/O connector (assuming N_DATAOEG is asserted) when DATAOE[2:0] = 3 → 0 for channels 4 → 1, respectively. Also, REG528 supplies the data when DATAOE[2:0] = 7 → 4 for channels
8 → 5, respectively.

The two different multiplexers are completely independent such that the monitor port can access any channel without being affected by a carrier I/O read at any other channel.

MONITOR PORT APPLICATIONS

The following presents some monitor port application hints concerning its use, and potential abuse.

- Any time a single channel at the I/O connector is being continuously monitored with the ADC128F1 freerunning, then the data will be updated every 8.625 µs and will change as the signal input to the converter changes. If the application calls for externally capturing the data, as is the case in the application note 6.5, then either the low state or the rising edge of N_CONVST at pin 50 of the I/O connector can be used as the clock for both latches and flip-flops since that signal rises only after the CVT has been updated.
- Channel number selections via DATAOE[2:0] and state changes in the output-enable control line N_DATAOEG should not be made asynchronously while free-running the ADC128F1 because the digital "noise" generated during the 6 µs of conversion operations following the rising edge of N_CONVST might couple into the convertors and decrease the accuracy of these ADCs. Except for ICLK, there are no other state changes taking place on the board during conversions, except for any accesses by the carrier.
- Unlike most other IPacks from SYSTRAN, high power buffers were not used for driving information out to the monitor port to further decrease the digitally-induced noise on the board. If multiple channels need to be monitored, it is recommended that the external hardware selecting and gathering data also take control of the board's acquisition sequencing operations, either by asserting N_HUPDIS or negating RUN, to synchronize the data gathering process without affecting the conversion accuracy.

2.5.3 Control

As discussed above, there are several levels of control that can be implemented on the ADC128F1. This subsection is a detailed explanation of those control elements that were explained at the system level in section 2.4: General Description.

N_HUPDIS CONTROL INPUT

The N_HUPDIS control input from pin 49 of the I/O connector is normally negated high by the 10 KΩ resistor designated as R4 located on the right side and just above J2 in Fig-

ure 2-3, page 2-9. CVT updates are disabled when this line is asserted low by an external digital source. The conversion processes continue to run, even when this line is asserted, for only the writes to the parallel registers that are the current value table are blocked by the assertion of this control signal.



NOTE: No more than 128 ADC128F1 IPacks should be controlled from a single digital output from a DIO316l or TRIDO48 to guarantee the low-level assertion state.

RUN CONTROL INPUT

The RUN control input from pin 44 of the I/O connector is normally asserted high by the 10 KΩ resistor designated as R2 located on the right side and just above the I/O connector J2 in Figure 2-3. This control line is typically used for tightly-coupling multiple ADC128F1 IPacks for system level simul-sampling operations. Negating this control line stops all ADC conversion processes and resets the main 69-count engine to a zero state.

N_DATAOEG CONTROL INPUT

The N_DATAOEG control input from pin 48 of the I/O connector is normally negated high by the 10 KΩ resistor designated as R3 located on the right side and just above the I/O connector in Figure 2-3. This control line, when asserted low, places the CVTObus lines in their low impedance states, providing the CVT information for the channel selected by DATAOE[2:0] to the I/O connector for monitoring purposes. When this input is unconnected or driven high, CVTO[11:0] are in their high impedance state.

2.5.4 Analog Components And Their Functions

All of the discussion in this subsection concerns components that are presented on the second page of the schematics in Appendix B.

HIGH PERFORMANCE FILTER

All of the analog circuitry runs off of the carrier's digital 5 volt supply. It is filtered by a 2.7 mH choke designated as L1, and a pair of 33 μF Tantalum capacitors, designated as C18 and C21, configured as a classic π-filter, designed to provide high performance filtering for the ten analog integrated circuits. This filter is on the left side of the board midway between J1 and J2 in Figure 2-3.

ADCS

The eight AD7893AR-10 ADCs, designated as U5 → U9, and U11 → U13 are all 12-bit, ±10 volt single-ended input, serial ADCs with built-in track and hold amplifiers. They have a patented front-end scaling architecture that enables their input voltage range to be four times wider than the power supply voltage that runs the devices. All eight ADCs are controlled by the SADCTRL device (see section 2.5.2 above). The serial data lines

SDATA[4:1] for the first four channels provide conversion data to the REG124 device, while SDATA[8:5] supply the same to the REG528 device. The ADCs have an internal reference buffer that permits all eight ADCs to be run from a single reference. All of the ADCs are located in the bottom left quadrant of Figure 2-3.

Precision Voltage Reference

All eight ADCs are supplied their precision +2.500 volt reference from the AD680JR device located at U4 (in the middle of the board in Figure 2-3). It is based upon bandgap technology and is a very low power device, operating on 250 µA maximum. The inital voltage error is 10 mV maximum, with a temperature coefficient of 25 ppm/°C maximum over the operating range of the ADC128F1. It is important to note that the voltage reference requires about 25 ms to stabilize to within ±0.01% of its final output following application of power. It recommended that this time be accounted for in system designs that may use the ADC128F1 in intermittant power or quick-start-up applications.

Reference Monitor Signal

As can be seen on Schematic #2, the ADC's reference voltage is first buffered by the OP177GS device at U3 (to the left of U4 in Figure 2-3), before being applied to the converters. This signal, called "VREF", is also brought out to pin 18 of the I/O connector for testing purposes.



CAUTION: Under normal operational conditions, pin 18 of the I/O interface cable should have no circuitry attached in order to maintain the high accuracy specifications of this product.

A significant effort has been made to provide very careful signal routing in this analog section of the ADC128F1. All of the digital signals run perpendicular to the analog signals on different printed circuit board planes, with complete ground fills on all layers.

3.0 HARDWARE INSTALLATION

3.1 Unpacking the ADC128F1

The contents of the ADC128F1 shipping packages are listed in Table 3-1:

Table 3-1 Contents of ADC128F1 Shipping Packages

QTY	DESCRIPTION
1	ADC128F1 Printed Circuit Assembly
1	ADC128F1 User Manual *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals up to one per board are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR-ADC128F1).

3.2 Visual Inspection of the ADC128F1

Examine the ADC128F1 to determine if any damage occurred during shipping.

3.3 ADC128F1 Installation



NOTE: The ADC128F1 is an Electrostatic Sensitive Device (ESD), the hardware installation of the ADC128F1 must be conducted on a good anti-static workbench to protect the IPack and carrier boards. The IPack carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the ADC128F1 can be completed.

The ADC128F1 installation requires the following tools:

Table 3-2 ADC128F1 Installation Tools

QTY	DESCRIPTION
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

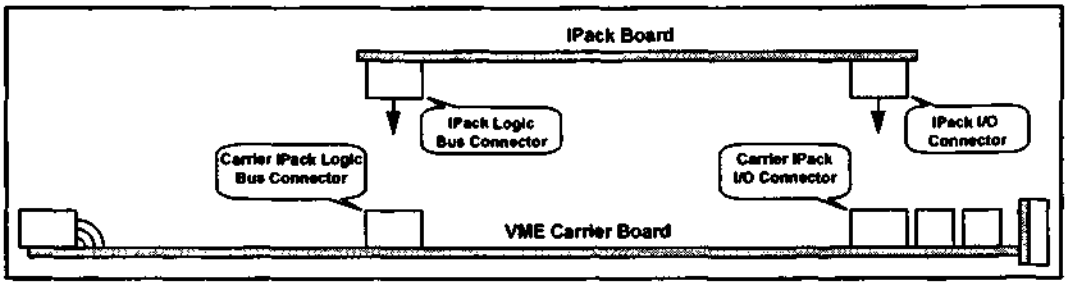


Figure 3-1 Installation of the ADC128F1 on a VME IPack carrier board.

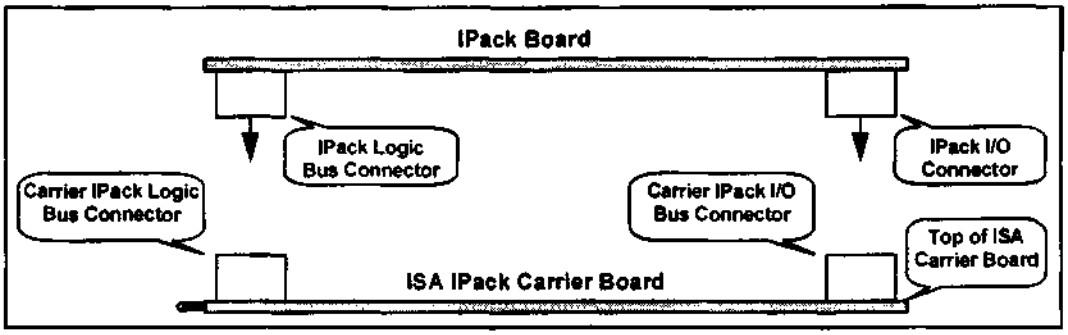


Figure 3-2 Installation of the ADC128F1 on a ISA IPack carrier board.

Figure 3-1 shows how the ADC128F1 is installed on a VME IPack carrier, and Figure 3-2 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IPack Carrier board user's manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IPack carrier and move it to the ESD controlled area where the installation of the ADC128F1 can be made.
3. Remove the ADC128F1 from the shipping package and place it on the ESD bench.
4. Install the ADC128F1 onto the carrier board by applying adequate and equal pressure to the ADC128F1 board at both ends.
* 5. Install four M2x5 mm flat head machine screws onto the IPack carrier's IPack connectors.

This completes the installation of the ADC128F1 to the carrier board.

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Table 3-3 IPack Logic Bus Pin Assignments

Original IPack Signals Names	IPack Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IPack I/O Connector Pin Assignments

IPack I/O Pin #	Signal Name
50	N_CONVERT
49	N_HUPDIS
48	N_DATA0EG
47	DATA0EG
46	DATA0E1
45	DATA0E2
44	RUN
43	CVT00
42	GND
41	CVT01
40	GND
39	CVT02
38	GND
37	CVT03
36	GND
35	CVT04
34	GND
33	CVT05
32	GND
31	CVT06
30	GND
29	GND
28	GND
27	GND
26	GND
25	CVT07
24	CVT08
23	CVT09
22	CVT010
21	CVT011
20	GND
19	GND
18	VREF
17	GND
16	AIN8
15	GND
14	AIN7
13	GND
12	AIN6
11	GND
10	AIN5
9	GND
8	AIN4
7	GND
6	AIN3
5	GND
4	AIN2
3	GND
2	AIN1
1	GND

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4.0 PROGRAMMING GUIDE

4.1 Overview

This section of the manual describes the operation of the ADC128F1 from the software perspective, detailing the ADC128F1 registers and providing programming examples. A more detailed description of the hardware can be found in section 2.0: DESCRIPTION and section 6.0 TYPICAL APPLICATIONS.

4.2 Description

The ADC128F1 is a simple to use IPack card with 8 channels of 12-bit analog to digital convertors. Eight data registers, one per channel, are used to read the input voltages for the channels. In freerun mode (which is the default) these eight data registers are the only registers required for operation of the ADC128F1. The control register allows enabling/disabling the update of the current value table (CVT). The status register indicates the state of the external data monitor port.

4.3 IPack ID PROM Listing

Emulating the ID PROM function is possible due to the never changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IPack to provide "no-wait" read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0C *hex*, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IPack resides.

The IPack ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all ones during valid ID read-only accesses because they remain undriven.

Table 4-1 is the ADC128F1 emulated ID Address Space PROM listing:

Table 4-1 ADC128F1 ID Address Space Listing

IPACK ADDRESS	DESCRIPTION	DATA READ
IPA = 00 *hex*	ASCII "I"	49 *hex*
IPA = 01 *hex*	ASCII "P"	50 hex
IPA = 02 *hex*	ASCII "A"	41 hex
IPA = 03 *hex*	ASCII "C"	43 hex
IPA = 04 *hex*	SYSTRAN's ID	45 hex
IPA = 05 *hex*	ADC128F1's Model Number	6A hex
IPA = 06 *hex*	Revision Level	30 hex
IPA = 07 *hex*	Reserved	00 hex
IPA = 08 *hex*	Low Byte Driver ID	00 hex
IPA = 09 *hex*	High Byte Driver ID	00 hex
IPA = 0A *hex*	Number of Bytes Used	0C hex
IPA = 0B *hex*	CRC	6A hex

4.4 IPack I/O Address Map

The ADC128F1's I/O Address Map was designed with efficiently located data and control/status registers in the IPack I/O space (IPA = 00 → 09 *hex*). The address detector circuitry is fully decoded.



NOTE: Any attempt to access IPA addresses at and above IPA = 0A *hex* will result in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IPack resides.

On power-up, the Control Register Bit 0 = '1' which is 'Run Mode' for the CVT operation and after 25 ms the ADCs will settle out to their connections.

The ADC128F1 has ten 16 bit wide registers; eight data registers, one control register, and one status register. The ADC128F1 supports word (16 bit) reads and writes (some registers are read only, see descriptions below). The registers are described in detail below.

The first eight locations (IPA = 00 → 07 hex) are the read-back data registers 0-7 for the ADC data ports 1 through 8.

The ninth location (IPA = 08 *hex*) is the write and read-back Control Register containing a single bit that is used to enable/disable the updating of the CVT. If this bit is set to a 1, the CVT updates are enabled. If this bit is set to a 0, the CVT updates are disabled. In the CR bits [15:1] are not used.

The tenth location (IPA = 09 *hex*) is the read-back Status Register reflecting the state of the data monitor port signals. In this register bits [15:6] are not used.

Table 4-2 is the ADC128F1 I/O Address Map and contains the data register:

Table 4-2 ADC128F1 I/O Address Map

IPACK ADDRESS	BYTE-LANE 1	BYTE-LANE 0	DESCRIPTION
IPA = 00 *hex*	[XXXX] [11:8]	[7:0]	Data Register 0, 12 bits
IPA = 01 *hex*	[XXXX] [11:8]	[7:0]	Data Register 1, 12 bits
IPA = 02 *hex*	[XXXX] [11:8]	[7:0]	Data Register 2, 12 bits
IPA = 03 *hex*	[XXXX] [11:8]	[7:0]	Data Register 3, 12 bits
IPA = 04 *hex*	[XXXX] [11:8]	[7:0]	Data Register 4, 12 bits
IPA = 05 *hex*	[XXXX] [11:8]	[7:0]	Data Register 5, 12 bits
IPA = 06 *hex*	[XXXX] [11:8]	[7:0]	Data Register 6, 12 bits
IPA = 07 *hex*	[XXXX] [11:8]	[7:0]	Data Register 7, 12 bits
IPA = 08 *hex*	[XXXX,XXXX]	[XXXX,XXX][0]	Control Register, BIT 0 0 = Disable Conversion 1 = Enable Conversion (Run) Bits [15:1] are not used
IPA = 09 *hex*	[XXXX,XXXX]	[XX][5:0]	Status Register Bit 0 = RUN Bit 1 = N_HUPDIS Bit 2 = DATAOE0 Bit 3 = DATAOE1 Bit 4 = DATAOE2 Bit 5 = N_DATAOEG Bits [15:6] are not used

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4.5 Word Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-3 Word Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPACK ADDRESS
BASE + 0	BASE + 0	BASE + 2	IPA = 00 *hex*
BASE + 2	BASE + 2	BASE + 6	IPA = 01 *hex*
BASE + 4	BASE + 4	BASE + A	IPA = 02 *hex*
BASE + 6	BASE + 6	BASE + E	IPA = 03 *hex*
BASE + 8	BASE + 8	BASE + 12	IPA = 04 *hex*
BASE + A	BASE + A	BASE + 16	IPA = 05 *hex*
BASE + C	BASE + C	BASE + 1A	IPA = 06 *hex*
BASE + E	BASE + E	BASE + 1E	IPA = 07 *hex*
BASE + 10	BASE + 10	BASE + 22	IPA = 08 *hex*
BASE + 12	BASE + 12	BASE + 26	IPA = 09 *hex*
BASE + 14	BASE + 14	BASE + 2A	IPA = 0A *hex*
BASE + 16	BASE + 16	BASE + 2E	IPA = 0B *hex*

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4.6 Byte Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for byte accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-4 Byte Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPACK ADDRESS	BYTE-LANE*
BASE + 1	BASE + 0	BASE + 3	IPA = 00 *hex*	0
BASE + 0	BASE + 1	BASE + 2	IPA = 00 *hex*	1
BASE + 3	BASE + 2	BASE + 7	IPA = 01 *hex*	0
BASE + 2	BASE + 3	BASE + 6	IPA = 01 *hex*	1
BASE + 5	BASE + 4	BASE + B	IPA = 02 *hex*	0
BASE + 4	BASE + 5	BASE + A	IPA = 02 *hex*	1
BASE + 7	BASE + 6	BASE + F	IPA = 03 *hex*	0
BASE + 6	BASE + 7	BASE + E	IPA = 03 *hex*	1
BASE + 9	BASE + 8	BASE + 13	IPA = 04 *hex*	0
BASE + 8	BASE + 9	BASE + 12	IPA = 04 *hex*	1
BASE + B	BASE + A	BASE + 17	IPA = 05 *hex*	0
BASE + A	BASE + B	BASE + 16	IPA = 05 *hex*	1
BASE + D	BASE + C	BASE + 1B	IPA = 06 *hex*	0
BASE + C	BASE + D	BASE + 1A	IPA = 06 *hex*	1
BASE + F	BASE + E	BASE + 1F	IPA = 07 *hex*	0
BASE + E	BASE + F	BASE + 1E	IPA = 07 *hex*	1
BASE + 11	BASE + 10	BASE + 23	IPA = 08 *hex*	0
BASE + 10	BASE + 11	BASE + 22	IPA = 08 *hex*	1
BASE + 13	BASE + 12	BASE + 27	IPA = 09 *hex*	0
BASE + 12	BASE + 13	BASE + 26	IPA = 09 *hex*	1
BASE + 15	BASE + 14	BASE + 2B	IPA = 0A *hex*	0
BASE + 14	BASE + 15	BASE + 2A	IPA = 0A *hex*	1
BASE + 17	BASE + 16	BASE + 2F	IPA = 0B *hex*	0
BASE + 16	BASE + 17	BASE + 2E	IPA = 0B *hex*	1

* Byte-lane 1 not applicable for ID space

4.7 Register Descriptions

4.7.1 Data Registers 0-7 Bit Description (IPA = 00 through 07 *hex*)

The eight 16-bit read-only data registers are used to read the input voltage of the eight ADC channels. Data register 0 corresponds to ADC channel 1, register 1 to channel 2, ... register 7 to channel 8.

Table 4-5 Data Registers 0 to 7 Bit Description

Bit #	15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	Not Used	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
R/W	Read as 1's	R	R	R	R	R	R	R	R	R	R	R	R
Power-up State	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D11 - D0 : These bits comprise the 12 bit ADC value.

4.7.2 Control Registers Bit Description (IPA = 08 *hex*)

The Control Register contains a single bit that is used to enable/disable the updating of the CVT. Disabling the CVT before reading of the ADC channels ensures that the readings of all channels represent voltages simultaneously sampled by the parallel ADC's. If this bit is set to a 1, the CVT updates are enabled. If this bit is set to a 0, the CVT updates are disabled.

Table 4-6 Control Register Bit Description

Bit #	15 to 1	0
Bit Name	Not Used	N_UPDIS
R/W	Read as 0's Writes discarded	RW
Power-up State	N/A	1 (Run)

NOTE: N_UPDIS is the CVT update enable/disable bit.

4.7.3 Status Registers Bit Description (IPA = 09 *hex*)

This register reflects the state of the data monitor port signals. The data monitor port can be used to check the operation of the ADC128F1 device without going through the IPack logic interface.

Table 4-7 Status Register Bit Description

Bit #	15 to 12	5	4	3	2	1	0
Bit Name	Not Used	N_DATAOEG	DATAOE2	DATAOE1	DATAOE0	N_HUPDIS	RUN
R/W	Read as 1's	R	R	R	R	R	R
Power-up State	N/A	N/A	N/A	N/A	N/A	N/A	N/A

N_ DATAOEG : This bit indicates the state of the N_DATAOEG signal.

N_ DATAOE2 - N_DATAOE0 : These bits indicate the state of the N_DATAOE2 - N_DATAOE0 signals.

N_ HUPDIS : This bit indicates the state of the N_HUPDIS signal.

RUN : This bit indicates the state of the RUN signal.

4.8 Programming Example

The following example illustrates operation of the ADC128F1 device using the CVT update disable feature. It demonstrates how to temporarily disable the update of the CVT. Since all 8 channels simultaneously sample, disabling update of the CVT while reading multiple channels ensures that all values in the CVT were sampled at the same time.

- Write a '0' to the control register. This disabled the update of the data registers.
- Read data registers 0 to 7 corresponding to AD channels 1 to 8. The eight AD values were all sampled at the same time.
- Write a '1' to the control register. This re-enables the update of the data registers.

5.0 PERFORMANCE

5.1 Overview

Performance specifications for the ADC128F1 IPack fall into two major categories: analog and its subsequent digital representations, and the timing of the actual conversion and data retrieval process. Analog issues are addressed in sections 1 and 2. This section presents information that more clearly depicts the actual conversion process events, various monitor and control techniques with their performance parameters, as well as IPack access timings as they relate to carrier interface activities.

It is important to note that the information provided in this section represents typical measurements, and in no way supplants any related minimum and maximum specifications presented in section 1 of this document. Where possible, data is tabulated with only one response time (actual) performance figure presented to minimize the length of the presentation.

Unlike other related documents published by SYSTRAN Corp. for IPack products, this section does not benefit from having a single system configuration for all of its empirical data measurements. Therefore, as each new set, or sets, of related data is presented, it is preceded by a short description of the system configuration used to gather the information. With this in mind, the following describes the hardware layout used to gather data for sub-section 5.3: Sampler Conversion Time, 5.4: Back-To-Back Conversions, and 5.5: Throughput, as presented in figures 5-1 through 5-11.

5.2 Hardware Configuration

Individual wires 1" long were connected to ADC128F1 #100 for, and at: "SCLK" @ U11 pin 4, "SDATA1" @ U11 pin 5, "SDATA2" @ U7 pin 5, "SDATA3" @ U5 pin 5, "SDATA4" @ U12 pin 5, "SDATA5" @ U8 pin 5, "SDATA6" @ U6 pin 5, "SDATA7" @ U13 pin5, and "SDATA8" @ U9 pin 5.

The IPack was mounted on a MVME162-01 in slot A using an IPack Logic Bus Extender Board (SYSTRAN part number BHAS-IPBE1) under the ADC128F1. A 24" extender cable was connected to an IPack Logic Bus Extender Board where the "ICLK" signal and ground references were made. A 36" I/O cable was connected between the slot A I/O connector on the carrier and a 50-position terminal block where the signal "N_CONVST" ("/CNVRT" in the figures) was monitored. All timing diagrams were captured using an HP 1 GHz Timing Module, Model 16515A, in a 16500A Logic Analysis System chassis.

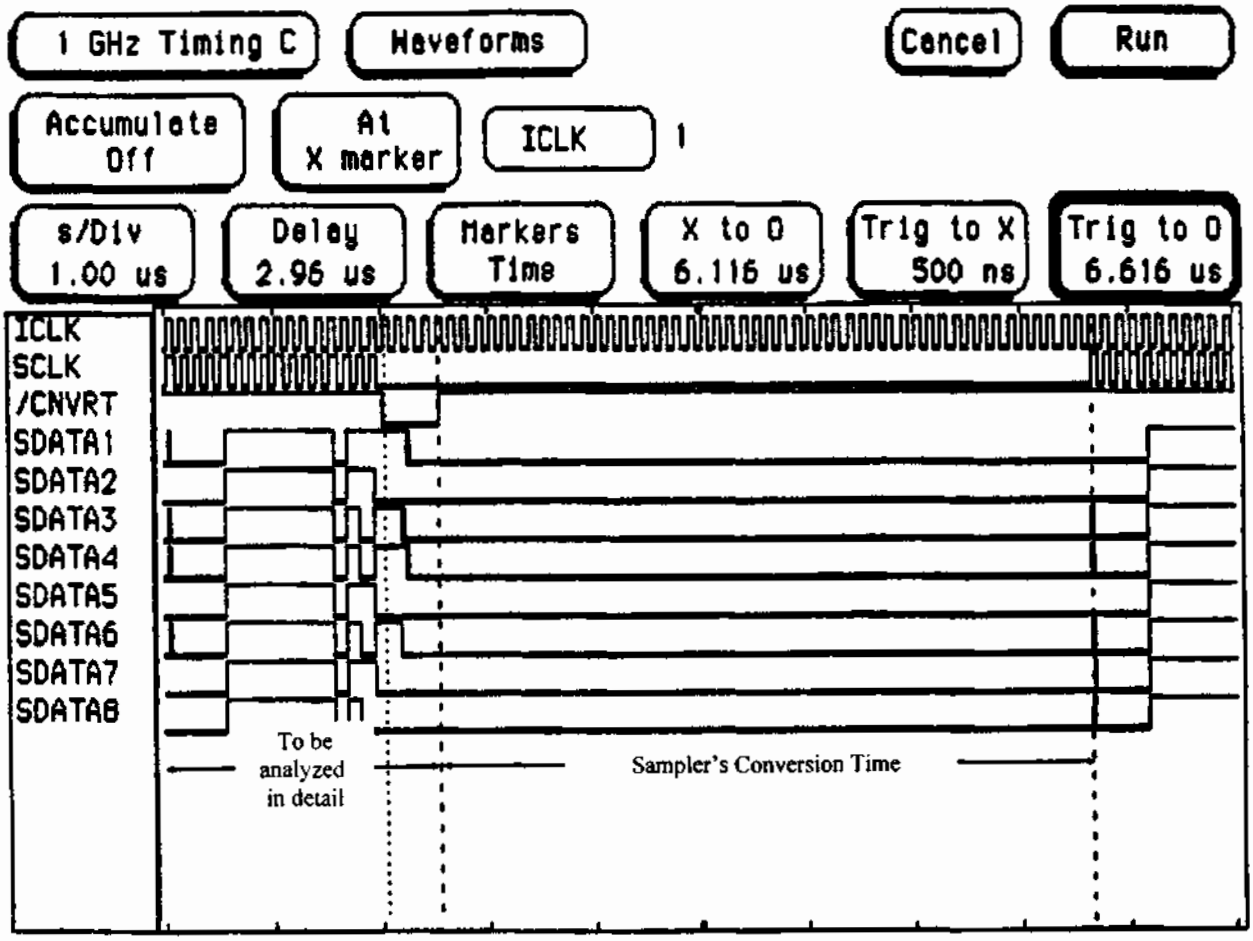


Figure 5-1 Sampler Conversion Time

5.3 Sampler Conversion Time

Data is first available 6 µs after the rising edge of N_CONVST (/CNVRT on the analyzer screen print).

- Measured 6.116 µs
- Theoretical best 6.000 µs (48 ICLK clock periods of 125 ns each)

The 116 µs is due to propagation delays through the components.

The area indicated in Figure 5-1 to be analyzed in greater detail is discussed in Figures 5-2 through 5-10.

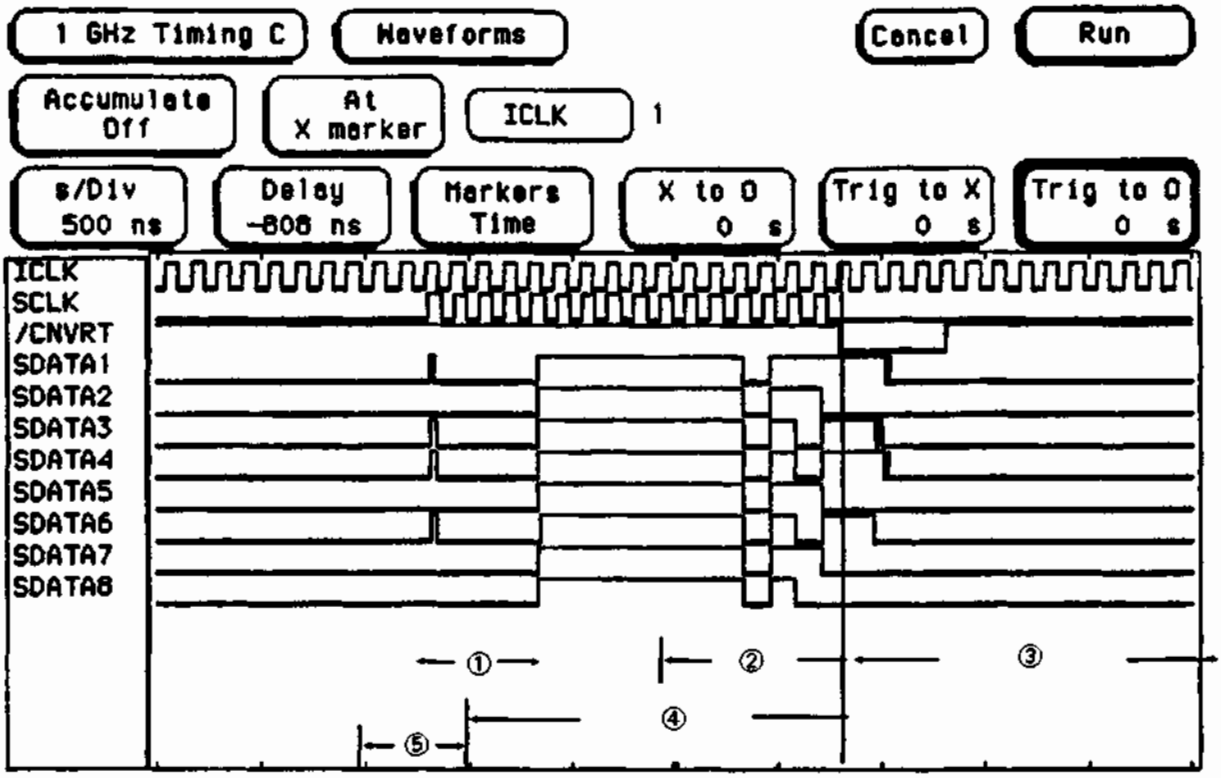


Figure 5-2 Sampling Overview

The overview of the sampling to be analyzed in more detail is discussed using the following analyzer screen prints:

① Figure 5-3

② Figure 5-4

③ Figure 5-5, 5-6

④ Figure 5-7, 5-8

⑤ Figure 5-9, 5-10

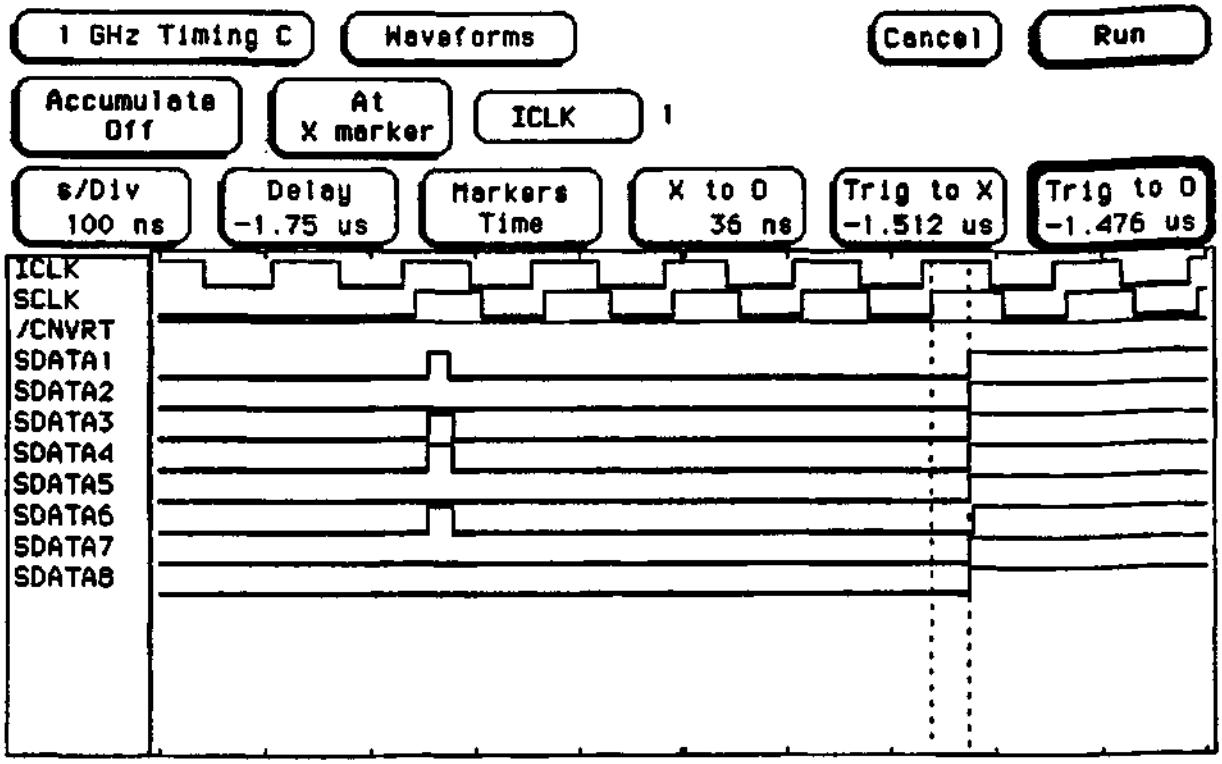


Figure 5-3 Rising Level Data

The rising edge ⌐ of SCLK causes the data to be serially shifted out of the converters about 36 ns later.

The first four ⌐¬ SCLK pulses shown represent the leading nibble of zero. The rising edge causes the converters to shift out a data bit. The falling edge is the data capture clock edge in the serial-to-parallel conversion process.

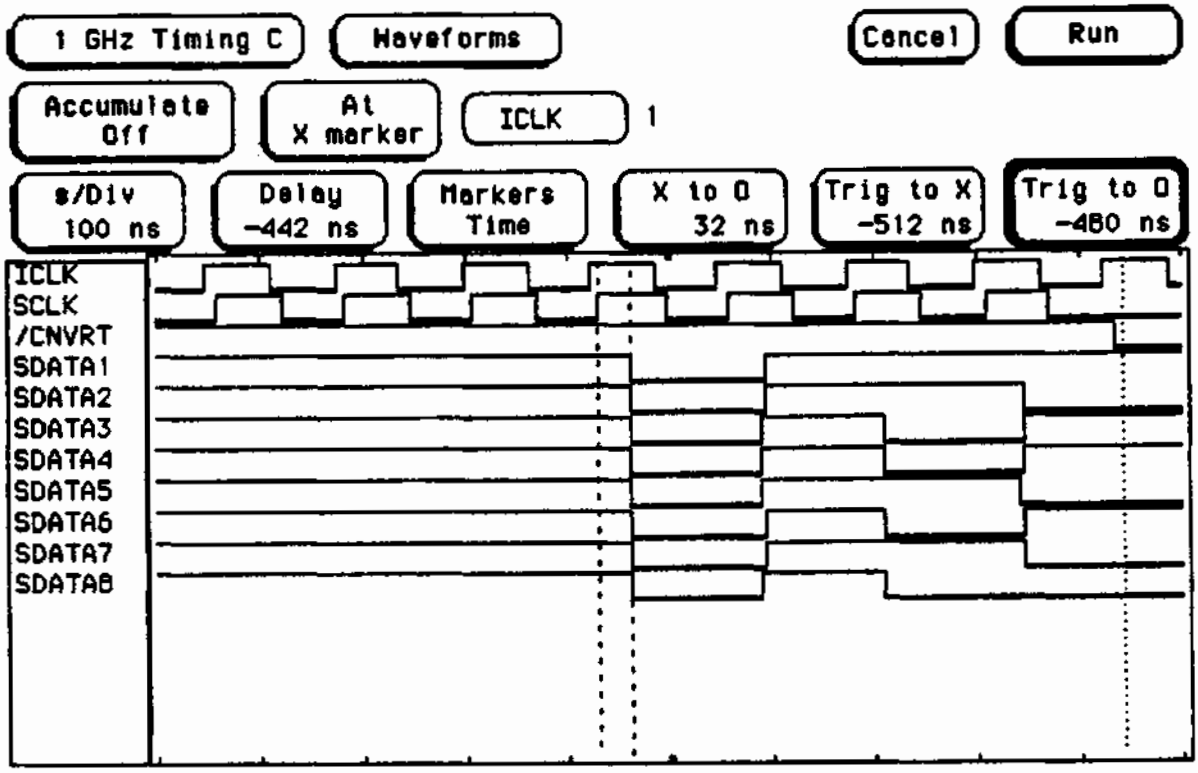


Figure 5-4 Falling Level Data

The rising edge ⌐ of SCLK causes data to be serially shifted out of the converters about 32 ns later.

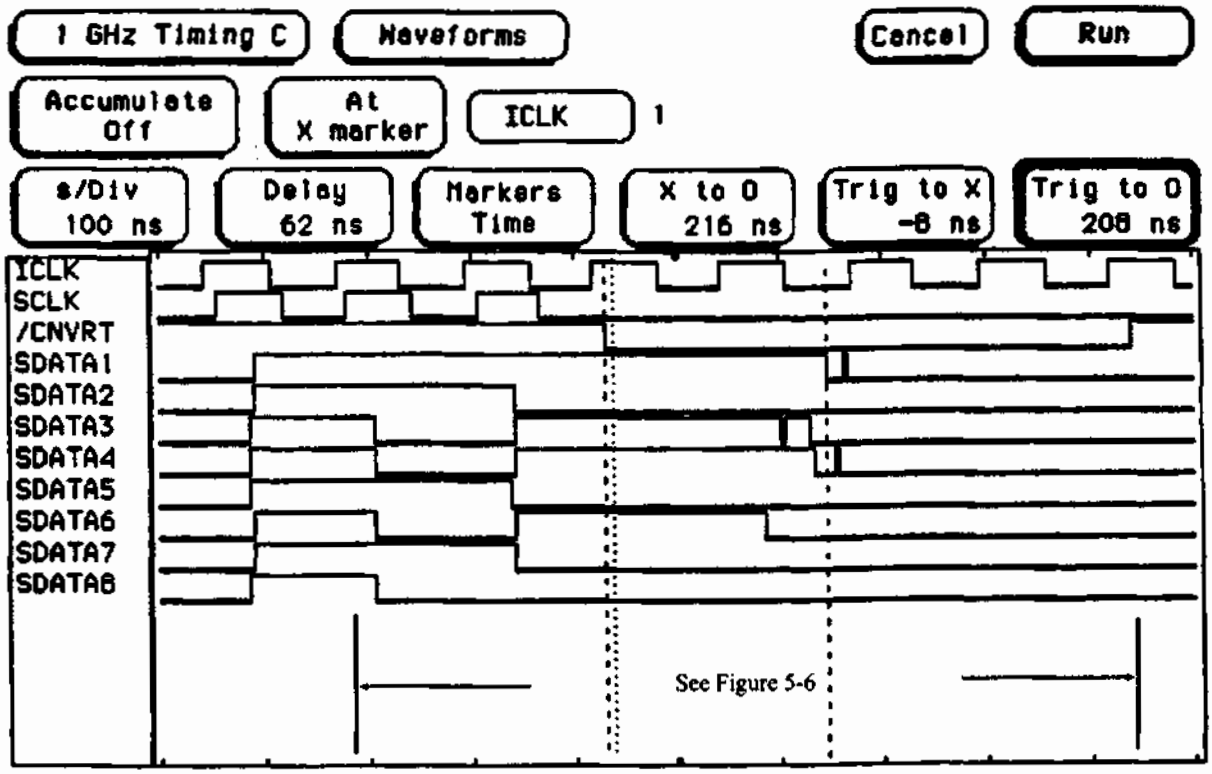


Figure 5-5 Falling Level of N_CONVST

The falling level ⌝ of N_CONVST (/CNVRT) on the analyzer screen), until SDATA is a high impedance state, is between 10 ns and 100 ns according to specification.

This analyzer screen shows about 216 ns because the SDATA lines float low (no pull-up or pull-down resistors to minimize board power requirements).

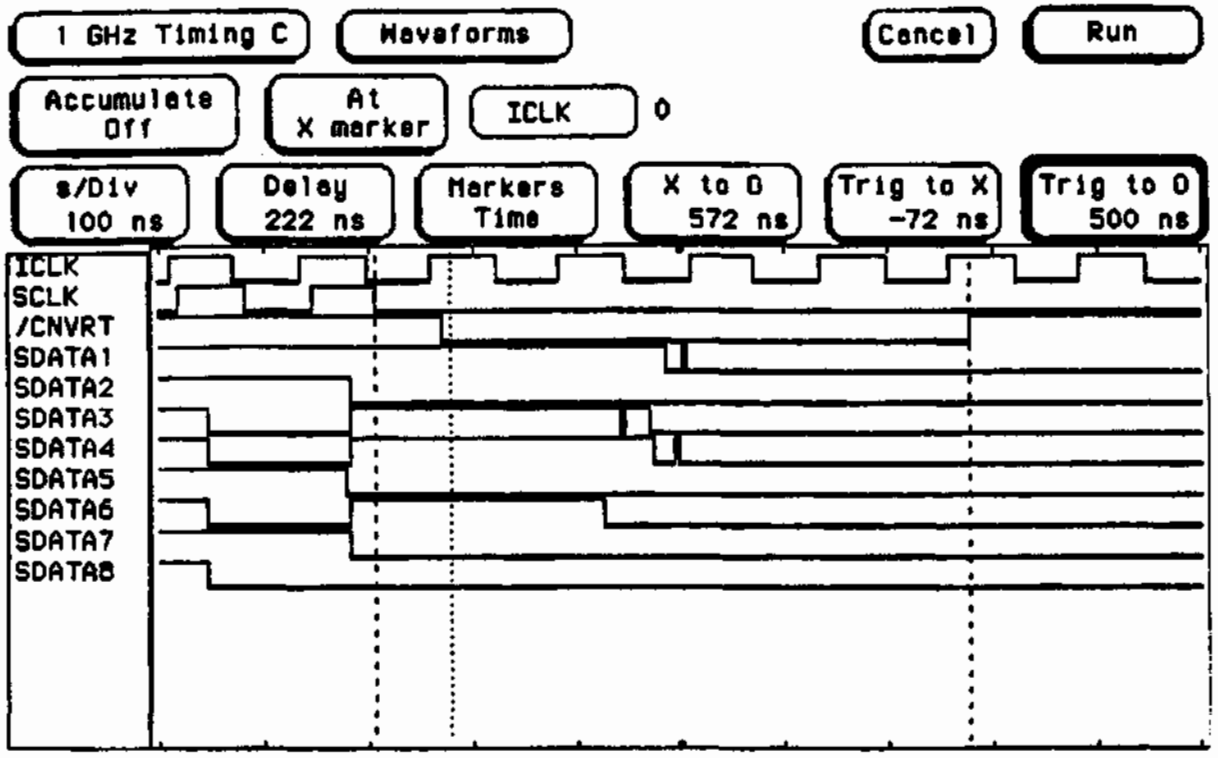


Figure 5-6 Conversion Timing

The elapsed time from the last fall of SCLK to the rising of N_CONVST is supposed to be 600 ns. This requirement is not found in the specification. It is found in the text of ADC's data sheet describing converter details. Portions of this text are quoted below.

"To obtain optimum performance from the part [converter], the read operation should not occur during the conversion* or within 600 ns prior to the next conversion."

[* 6.000 µs from ⌐ N_CONVST until the first _┘ SCLK].

And elsewhere:

"Once the read operation has taken place, a further 600 ns should be allowed before the next rising edge of CONVST [N_CONVST] to optimize the settling of the track/hold amplifier before the next conversion is initiated."

Also:

"The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 1.5 µs."

"At the end of a conversion (6 µs after the rising edge of CONVST [N_CONVST] the part returns to tracking mode."

The results in figure 1-6 of 572 ns violate the text requirement by 28 ns. However, 2.510 µs** of tracking exceeds 1.5 µs specification by nearly 60%.

** See Figure 5-7.

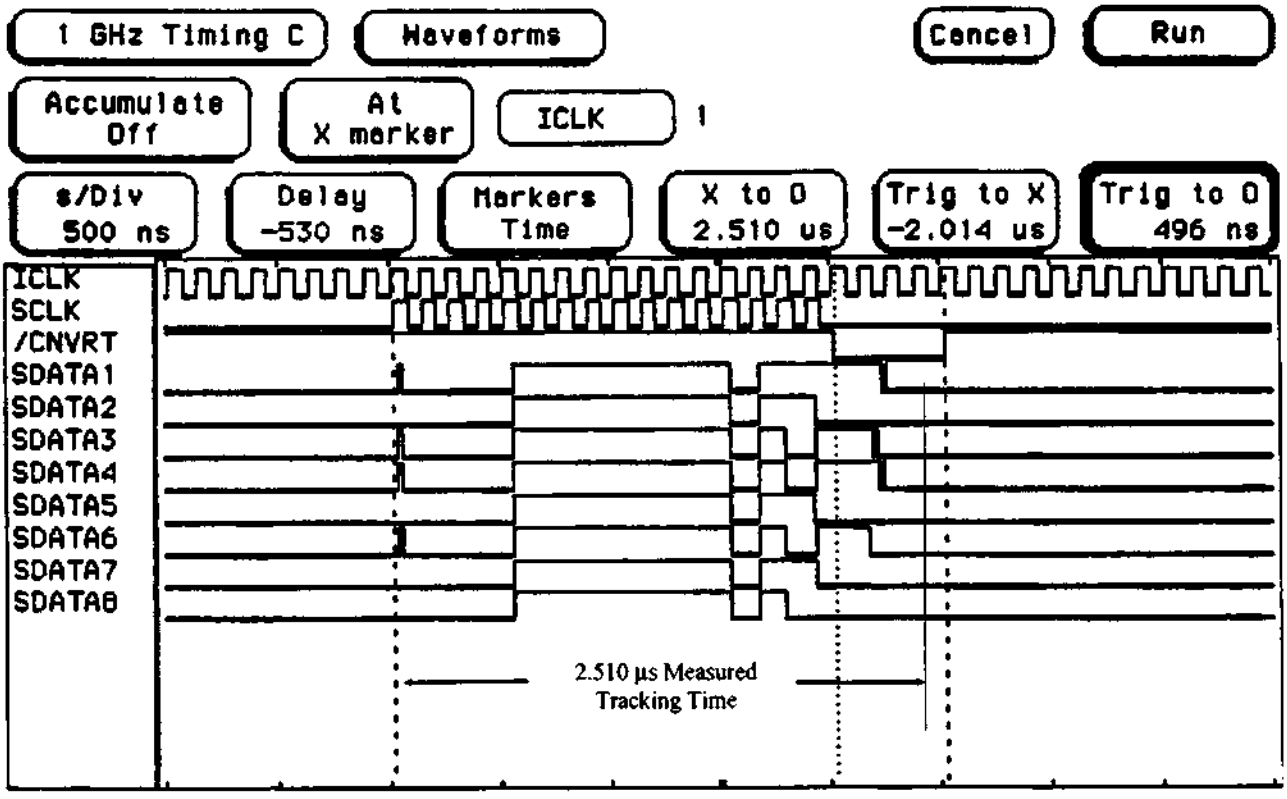


Figure 5-7 Measured Tracking Time

1.5 µs minimum to track to 12-bit accuracy. (See notes for Figure 5-6).

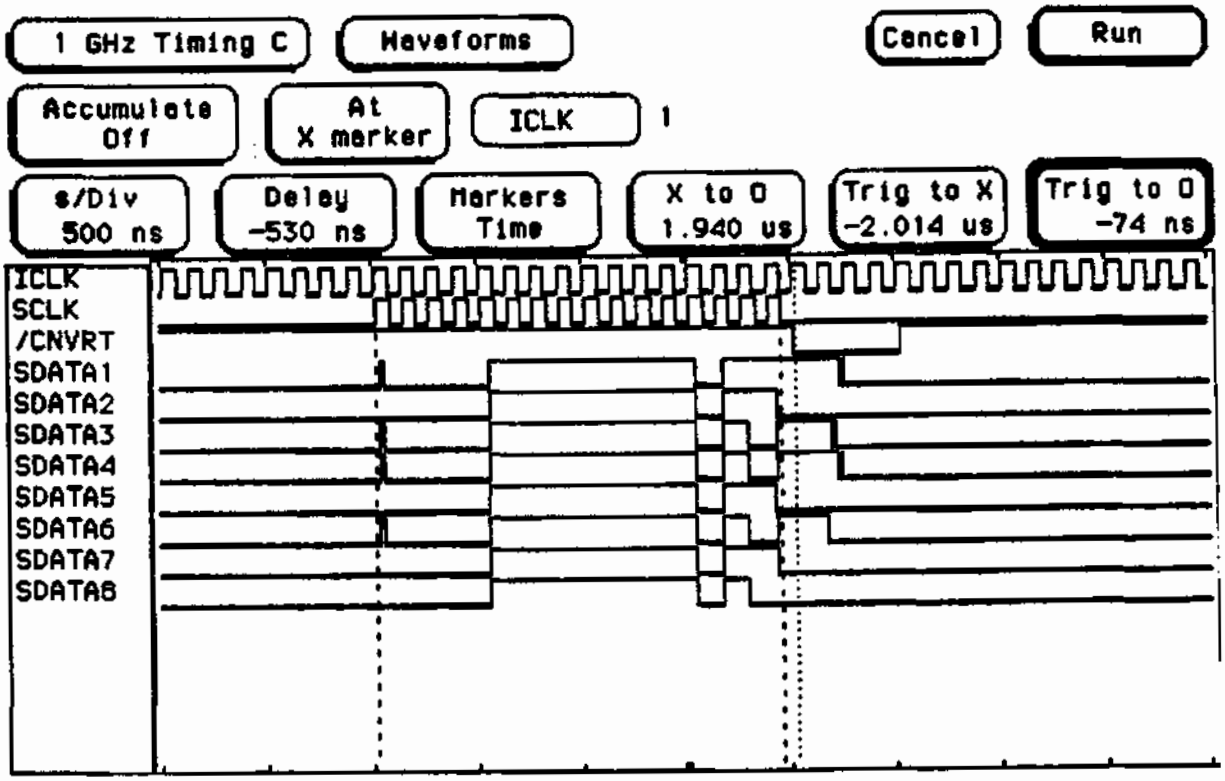


Figure 5-8 Read Operation

Start of read (first ⌐ SCLK) to end of read (last ¬ SCLK) = 1.940 µs

1.92 µs is the fastest read time per specification.

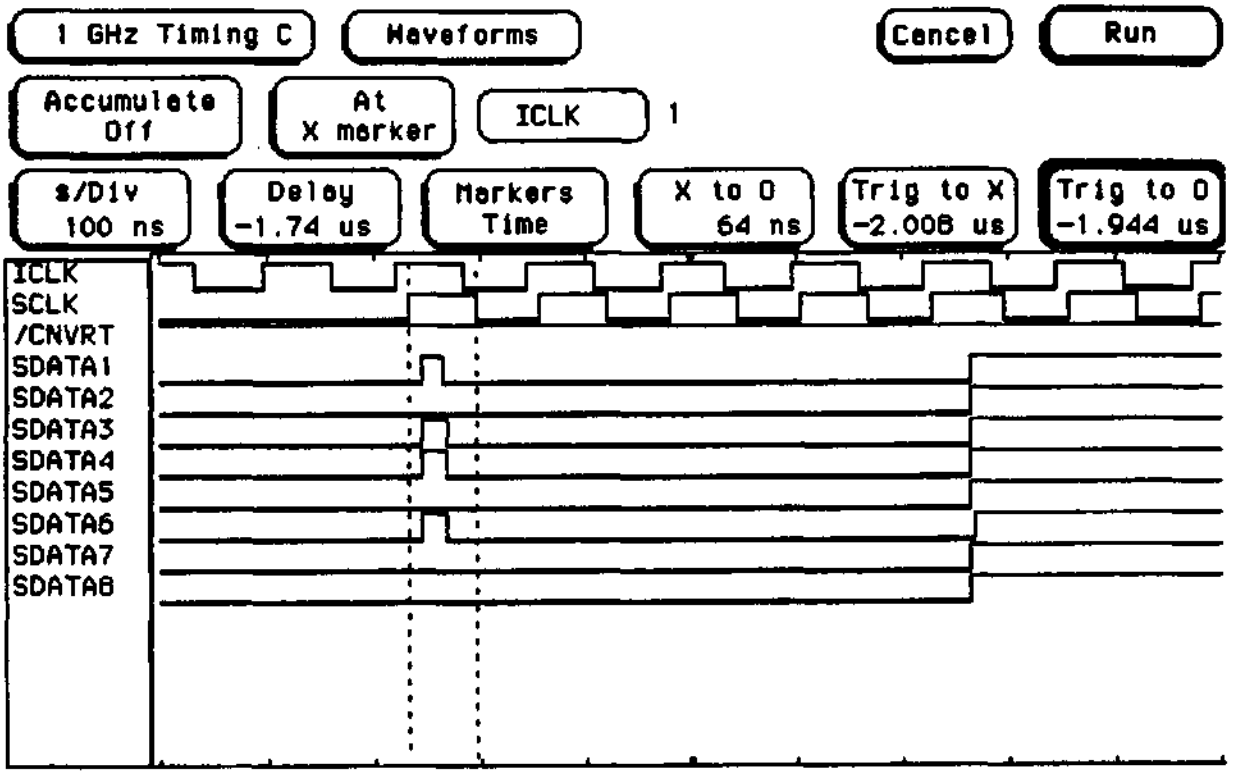


Figure 5-9 SCLK High Pulse Width

SCLK high pulse width = 64 ns measured.

SCLK high pulse width = 60 ns minimum per specification.

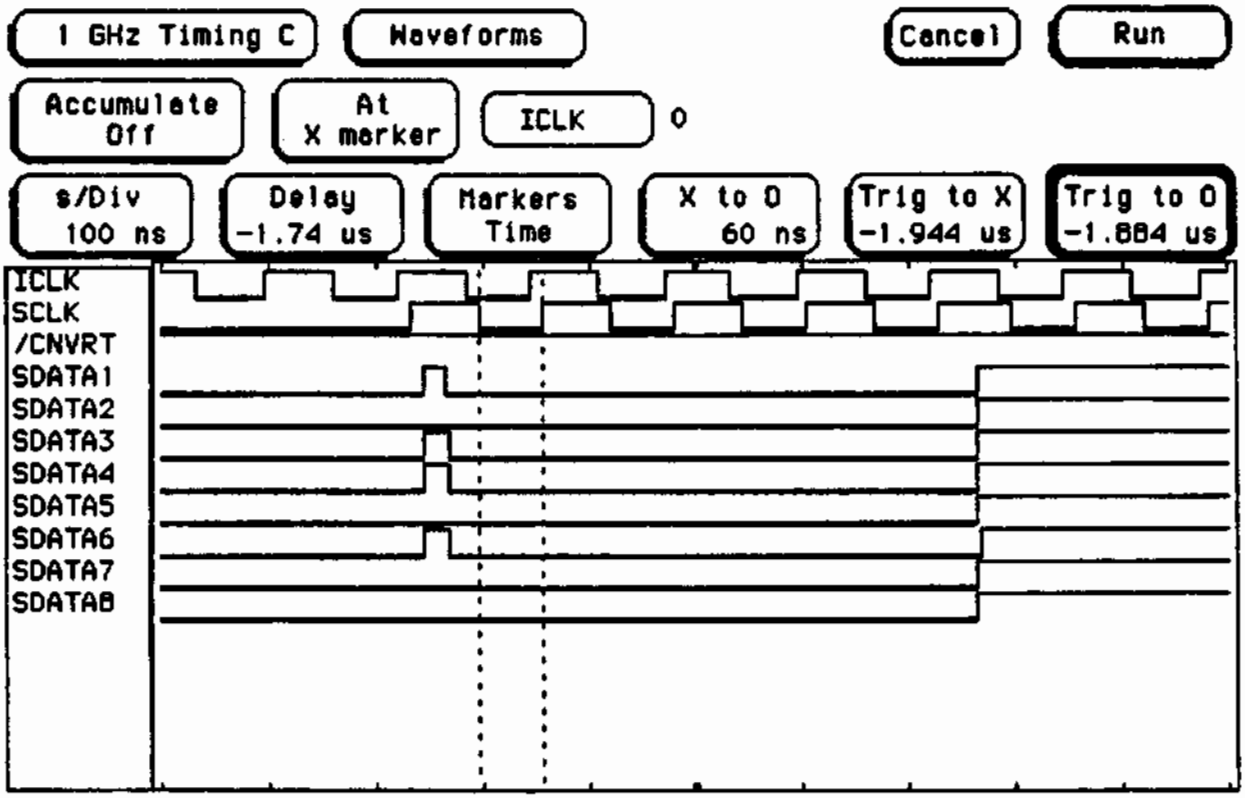


Figure 5-10 SCLK Low Pulse Width

SCLK low pulse width = 60 ns measured.

SCLK low pulse width = 30 ns minimum per specification.

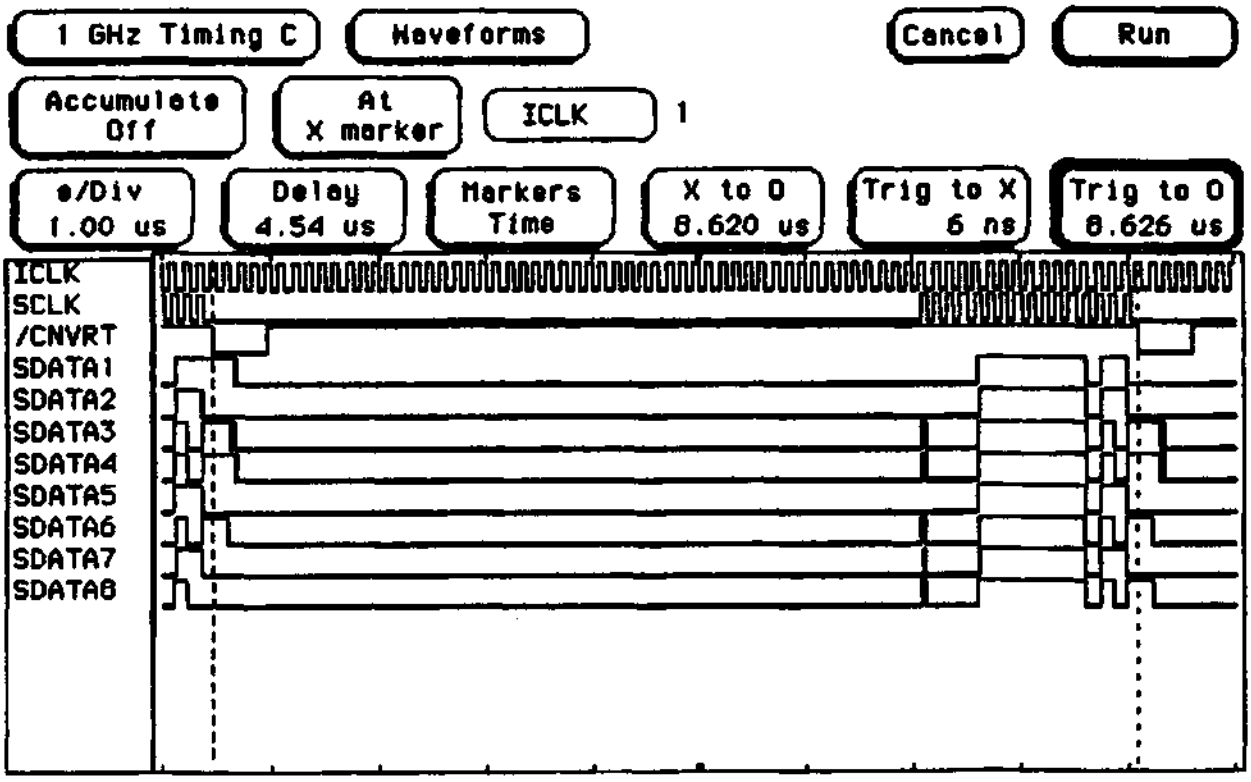


Figure 5-11 Back-to-Back Conversions

5.4 Back-to-Back Conversions

Back-to-back conversions were measured at 8.62 µs. There is a measurement resolution error of 5 ns out of 8.620 ns for 0.58% accuracy.

The theoretical value is 8.625 µs ⇒ 115,942.0289 S/S.

5.5 Throughput

Minimum possible throughput time of 8.52 µs ⇒ 117,370.892 S/S per specification.

This means this IPack card is running at 98.78% of the theoretical maximum.

5.6 Carrier Accesses

This short presentation provides typical timing parameters as they pertain to carrier accesses. The IPack was mounted on a MVME162-01 in slot A using an IPack Logic Bus Extender Board (SYSTRAN part number BHAS-IPBE1) under the ADC128F1. A 24" extender cable was connected to an IPack Logic Bus Breakout Board where all of the connections to signals and ground references were made. All timing diagrams were captured using an HP 1 GHz Timing Module Model 16515A in a 16500A Logic Analysis System chassis. There are four transfer types represented in table 5-1: An I/O write (@ IPA=08, to assert N_SUPDIS), an I/O read from that same control register, an I/O read from the current value table (for the third ADC @ IPA=02), and an ID read (from IPA=01). The two different I/O reads are presented since their timings for the providing of information to the IPDbus is significantly different due to different data sources.

Table 5-1 Carrier Accesses Typical Times

TRANSFER TYPE & WHERE	ICLK UNTIL:	TIME (ns)
I/O Write IPA = 08 *hex*	N_ACK	10
	N_ACK	10
I/O Read IPA = 08 *hex*	N_ACK	10
	IPDbus	13
	N_ACK	10
I/O Read IPA = 01 *hex*	N_ACK	10
	IPDbus	14
	N_ACK	9
I/O Read IPA = 02 *hex*	N_ACK	10
	IPDbus	22
	N_ACK	9

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5.6.1 I/O Write @ IPA = 08 *hex*

Figure 5-12 presents one of the eleven captured timing diagrams used for the development of Table 5-1. This figure presents the I/O write transfer, with the time markers highlighting the time it takes the ADC128F1 to assert N_ACK. Note that the IPDbus has 10 KΩ pull-up resistors on every line, and that it takes a long time for the data lines to float high after being driven low by either the carrier (as in this figure) or by the ADC128F1(or any other) IPack. This is why there is no timing parameter presented that defines the time it takes for the ADC128F1 IPack to release (transfer from low impedance to high impedance states) the IPDbus.

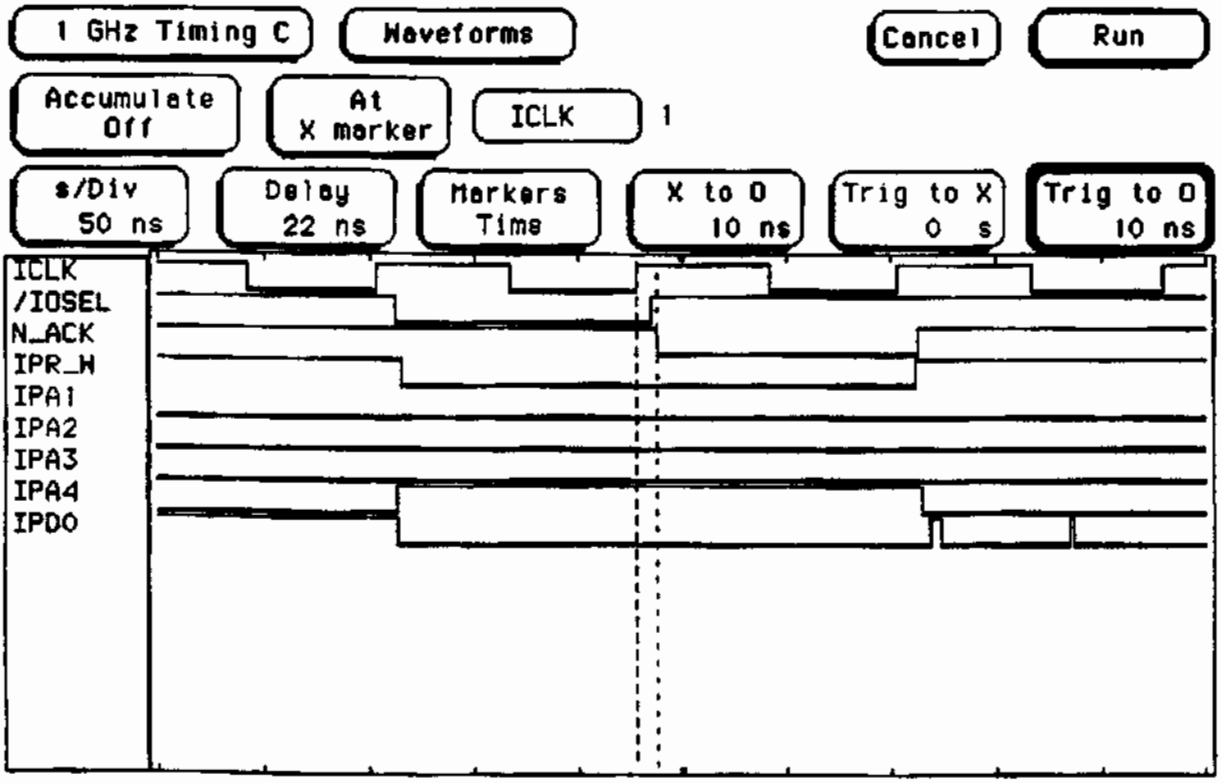


Figure 5-12 I/O Write @ IPA = 08 *hex*

5.7 Monitor Timing

This short subsection presents three diagrams that depict how the hardware-update-disable control line affects the monitor port. In addition, timing data is provided that can be used for data logging/capturing of CVT information from the monitor port.

The system configuration for this subsection consists of a TRIDO48 mounted in slot D, and a single ADC128F1 mounted on slot A of a MVME162-01 board, using an IPack Logic Bus Extender board under the ADC128F1. A 24" extender cable was connected to an IPack Logic Bus Breakout Board where the "ICLK" signal and ground references were made. A pair of 36" I/O cables were connected between the slot A I/O connector on the carrier and a 50-position terminal block where the rest of the I/O signals were monitored, and between the Slot D I/O connector and another 50-position terminal block.

All figures were captured using an HP 1 GHz Timing Module Model 16515A in a 16500A Logic Analysis System chassis. The N_DATAOEG and DATAOE[2:0] inputs were all grounded for the continual presentation of the first ADC's current value on the monitor outputs. The analog inputs were all left open. The lowest nibble of the CVT for the first ADC was the only information captured, and it represents open-input noise. One digital output from the TRIDO48 was connected to the "N_HUPDIS" (HUPDIS in the figures) input to the ADC128F1.

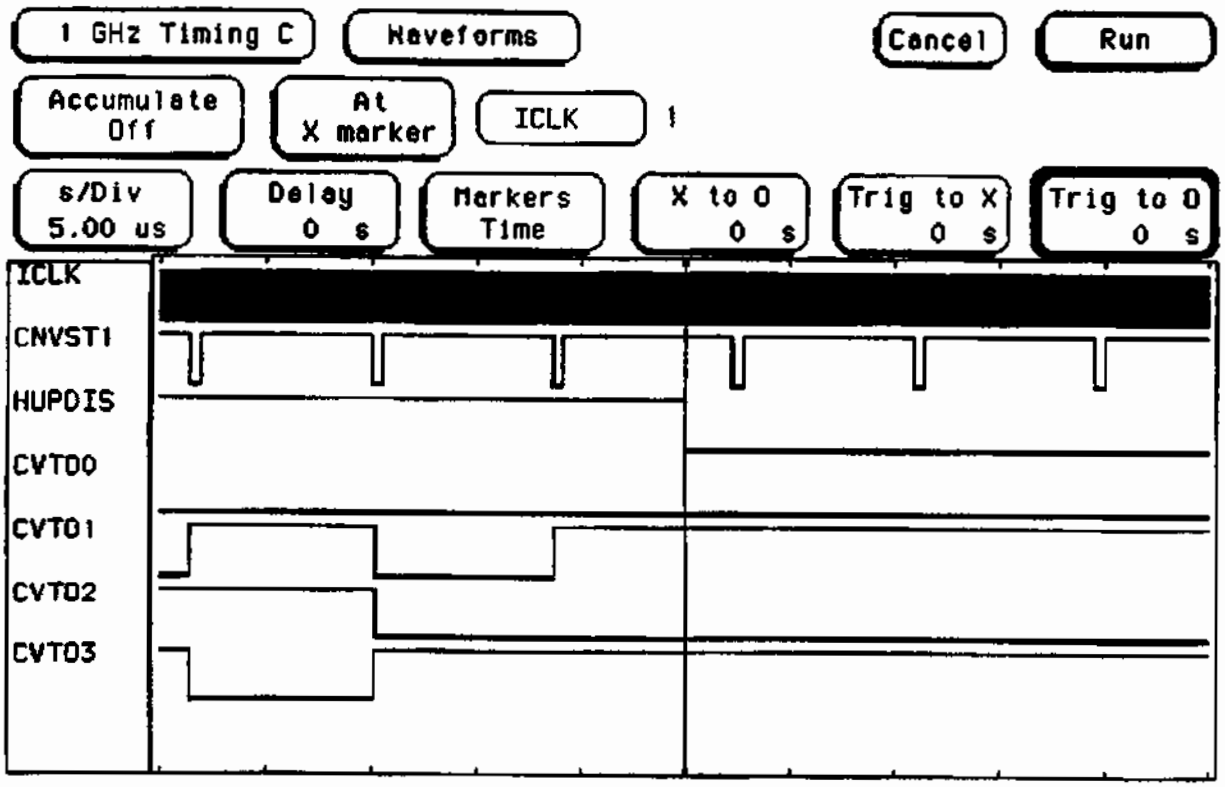


Figure 5-13 Hardware UPdate DISable Assertion

5.7.1 Hardware UPdate DISable Assertion

Figure 5-13 presents the before and after results of the assertion of N_HUPDIS. Note that to the left of the time marker, CVTO data is changing. After N_HUPDIS is asserted low, the current value table is no longer updated, as evidenced by the non-changing CVTO signals.

5.7.2 Hardware UPdate DISable Negation

Figure 5-14 presents the before and after results of the negation of N_HUPDIS. Note that to the left of the time marker, CVTO data is constant. After N_HUPDIS is negated high, the current value table is again being updated, as evidenced by the changing CVTO signals.

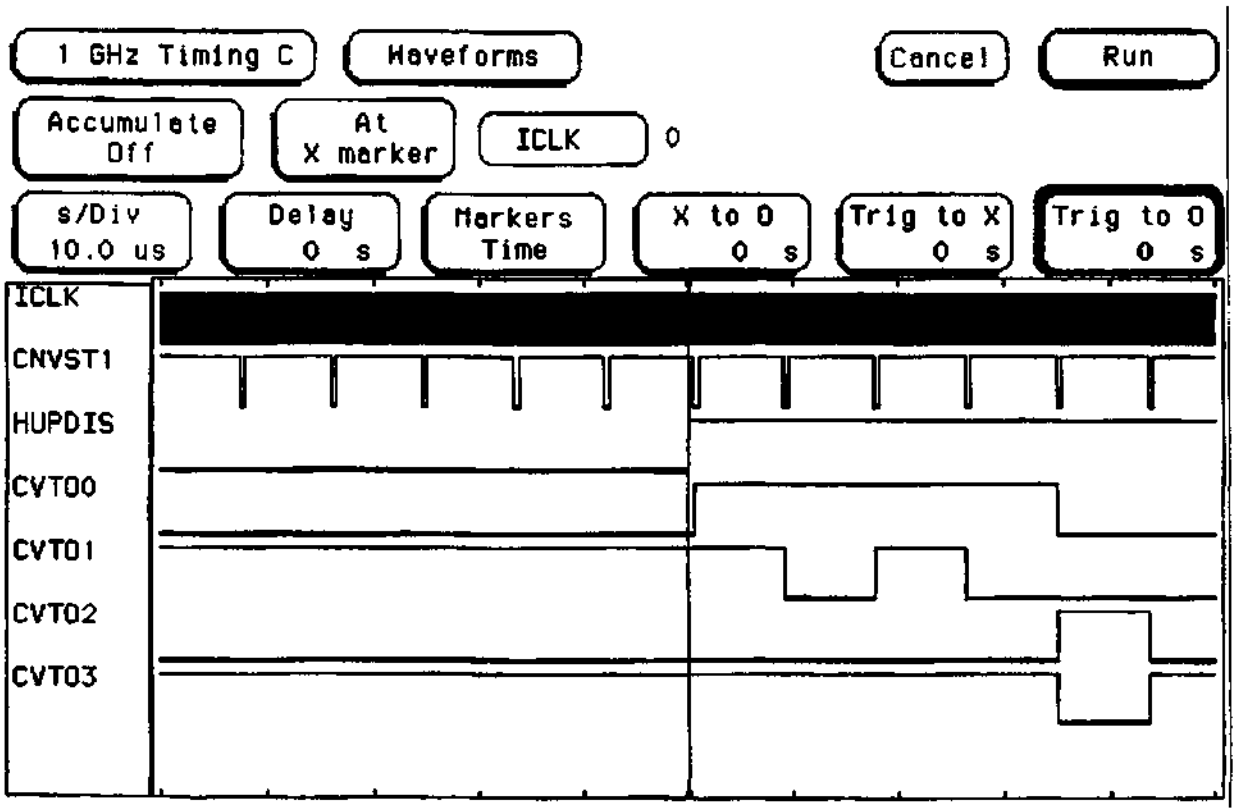


Figure 5-14 Hardware UPdate DISable Negation

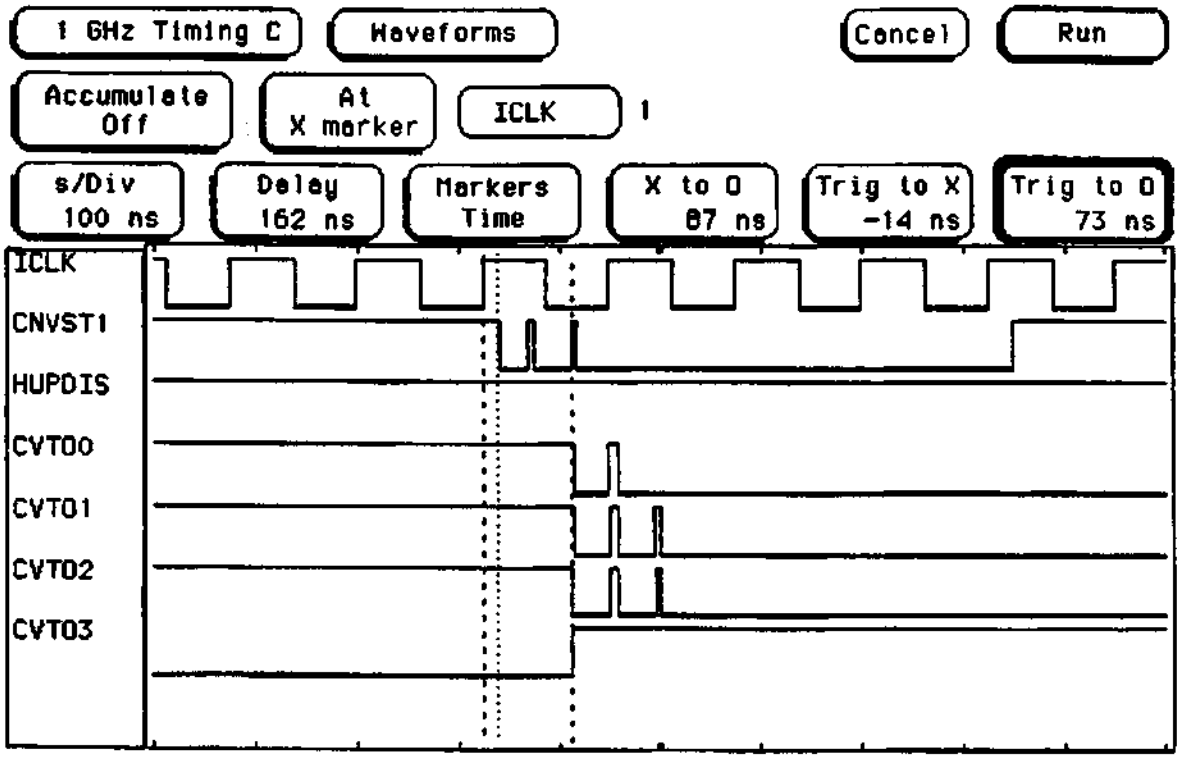


Figure 5-15 CVTO Update Timing

5.7.3 CVTO Update Timing

Figure 5-15 presents the timing relationship between the current value table updates and the "N_CONVST" (CNVST1 in the diagrams). The rising edge of ICLK preceding all other changes actually causes them. It takes about 16 ns for the N_CONVST signal to first reach its low state, while it takes about 87 ns for the changes in the current value table to propagate through the multiplexers and port drivers following their changes that occurred as a result of the actual update process. The ringing on the cables is due to the long, highly-capacitive ribbon cables that are being used unterminated.

Low Pulse Width of N_CONVST

The low pulse width of the N_CONVST signal deserves a short discussion. In various places throughout this document it has been stated that the N_CONVST pulse is 625 ns in width because it is generated from the main ADC engine during five of its machine states. Actually, the pulse width measures to be about 524 ns in width, slightly longer than four ICLK periods. N_CONVST is driven low during machine states 65, 66, 67, 68, and 69. However, as soon as the engine detects the "69" state, it asynchronously resets its main counter to all zeroes. The N_CONVST signal is decoded to be in a high state except for the five cited above. From this one can deduce that it takes the logic a total of 24 ns to detect that the engine is at count 69, reset it to count 00, detect that N_CONVST should then be high, and then drive the signal high.

As can be seen in Figure 5-15, the low state of N_CONVST can be used as a gate for latching the CVTO[11:0] data lines, or its rising edge can be used for registration of the

data (into FlipFlops). The falling edge should not be used due to potential cable ringing, except as a signal that the data is about to change.

5.8 Multi-board Timing

This last subsection presents some typical timing parameters for a pair of ADC128F1 IPacks running, first asynchronously, and then in tightly-coupled mode. As presented in other sections of this document, there are several different ways of using the ADC128F1 individually and coupled with others.

The system configuration for this last group of figures, as described earlier, involves the use of the MVME162-01 as the carrier. On it are placed an ADC128F1 #100 in slot A, an ADC128F1 #108 in slot B, and a TRIDO48 in slot D. The ADC128F1 in slot A is on a bus extender, with a bus breakout board connected at the end of a 24" extender cable. All three boards have 50-position terminal blocks connected to their respective carrier I/O connectors via 72" ribbon cables.

The same logic state analysis equipment cited earlier was used for this test. The "ICLK" signal and ground references were obtained via connections to the bus breakout board. The "N_CONVST" signal from ADC128F1 #100 in slot A (labeled CNVST1 in the figures) was obtained from pin 50 of the I/O terminal block for this board.

The "N_CONVST" signal from ADC128F1 #108 in slot B (labeled CNVST2 in the figures) was obtained from pin 50 of the I/O terminal block for this board. The digital output from the TRIDO48 (port 0 bit 0) at its pin 8 on its I/O terminal block was connected to pin 44 of both of the I/O terminal blocks for the ADC128F1 IPacks. This last connection is to the "RUN" inputs to the ADC128F1's, and was monitored by the analyzer at the TRIDO48's I/O terminal block.

The TRIDO48 was configured so that its outputs would be in a high impedance state on power-up. This permits both of the ADC128F1 IPacks to power-up acquiring data in freerun mode because their respective, pulled-high, RUN inputs present a high state to their respective ADC control engines.

5.8.1 ADC128F1s in Freerun Mode

Figure 5-16 presents a typical "freerun" picture of two ADC128F1's. Even though all of the samples from any one ADC128F1 are all captured simultaneously, the laws of probability indicate that, by chance, there will be a difference between boards. Figure 5-16 indicates that the samples obtained from the ADC128F1 in slot A are leading those from slot B by a skew of 3.241 µs. The reported time from the first occurrence of N_CONVST to the second one on the second ADC128F1 of 8.620 µs is incorrect by 5 ns due to the large sampling window being used.

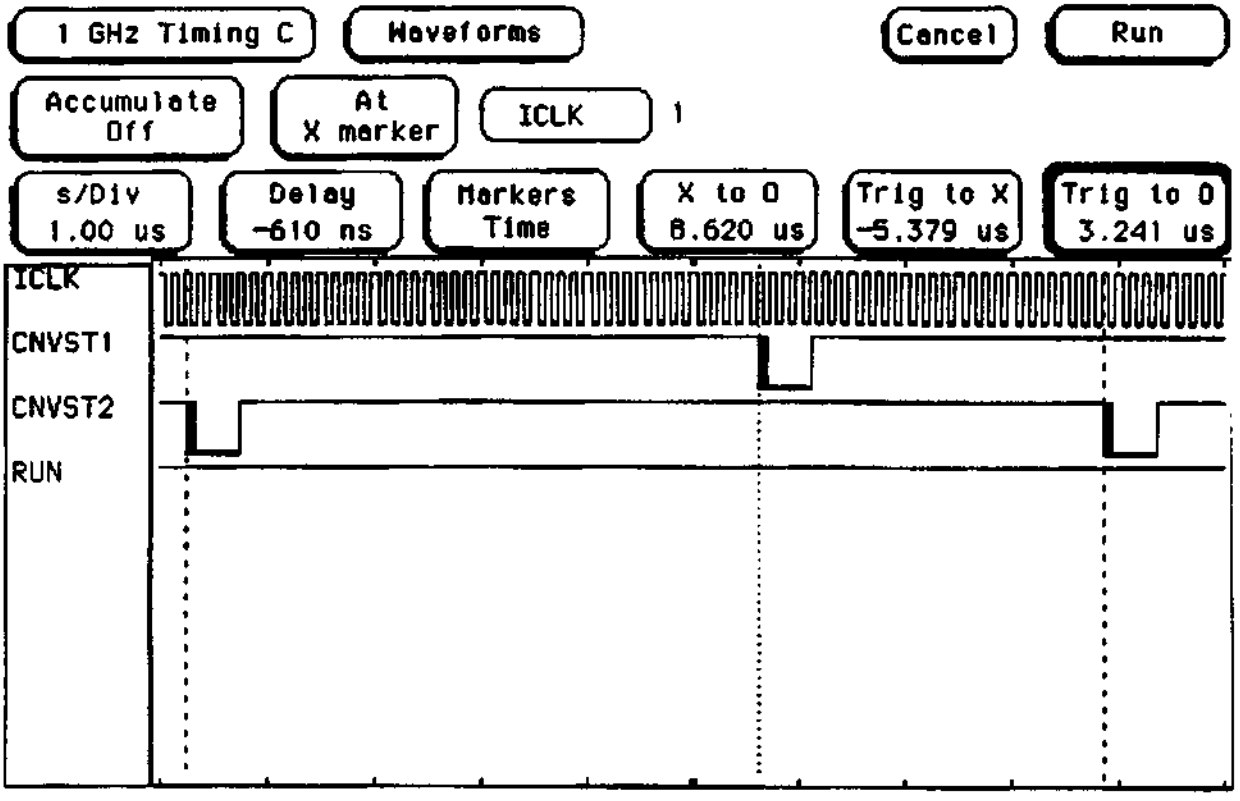


Figure 5-16 ADC128F1s in Freerun Mode

Following the above sampling, the TRIDO48 was configured so that the RUN signal could be manipulated. After enabling its output drivers, the RUN line was negated low (The TRIDO48's data registers default to zeroes on power-up). This, of course, had the effect of stopping both of the ADC128F1's sampling process and resetting their ADC engines to a count of zero.

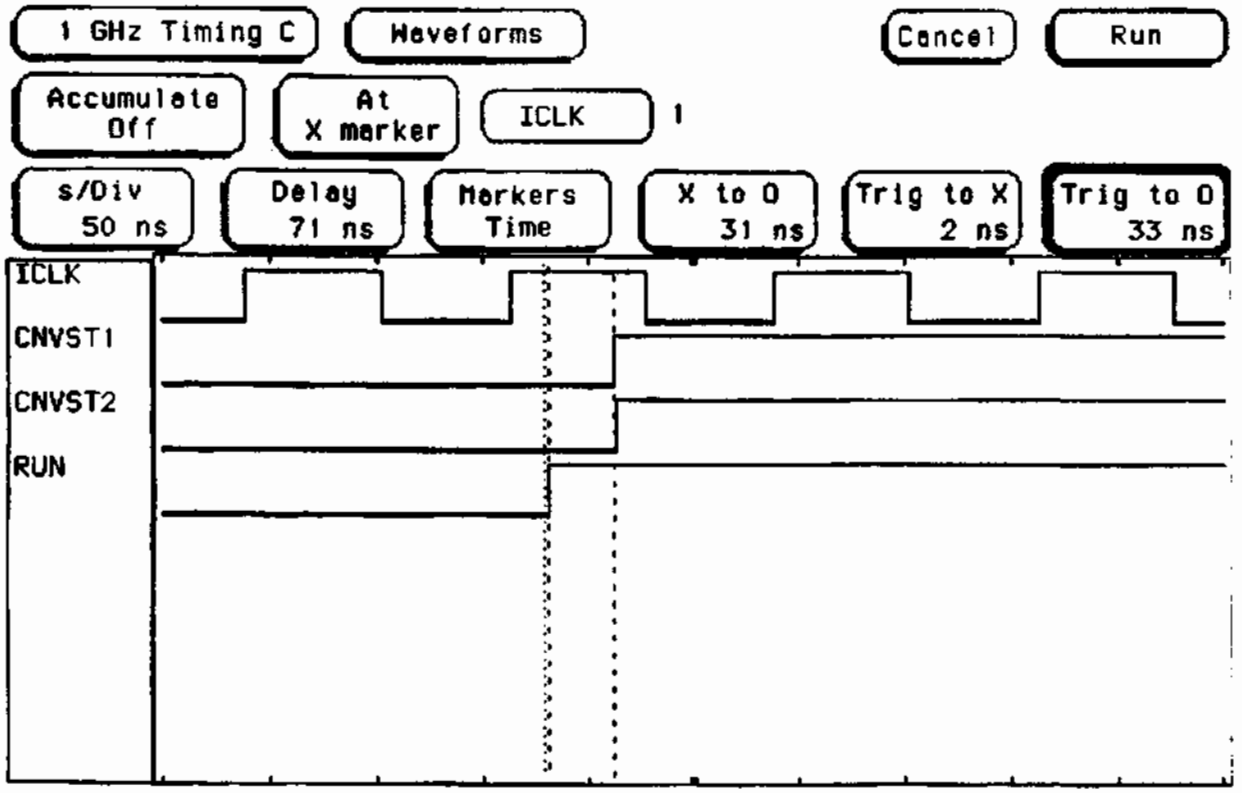


Figure 5-17 ADC128F1s Starting in Tightly-Couple

5.8.2 ADC128F1s in Tightly-Coupled Mode

Figure 5-17 presents what takes place when RUN is asserted on tightly-coupled ADC128F1's. At 31 ns following the rising edge of RUN, both ADC128F1's are driving their respective N_CONVST signals high, simul-sampling 16 channels (in this example). If one were to accept the approximation of 5 ns/meter of propagation delay through the I/O cables, then slightly more than 18 ns (of the 31 ns measured) is non-logic delay timing.

Various samples were taken following the start event depicted in Figure 5-17. After ten minutes of a constantly asserted RUN signal, both ADC128F1 boards were still tightly coupled, as depicted in Figure 5-18. This zero-skew is primarily due to the fact that both ADC128F1's were operating on the same carrier. It is possible that there may be some skew between boards that reside on different carriers within the same chassis, or in different chassis running in tightly-coupled mode. The worst-case skew in such a system configuration is 125 nS, the period of one ADC engine clock cycle with respect to the rising edge of RUN from one ADC128F1 to another.

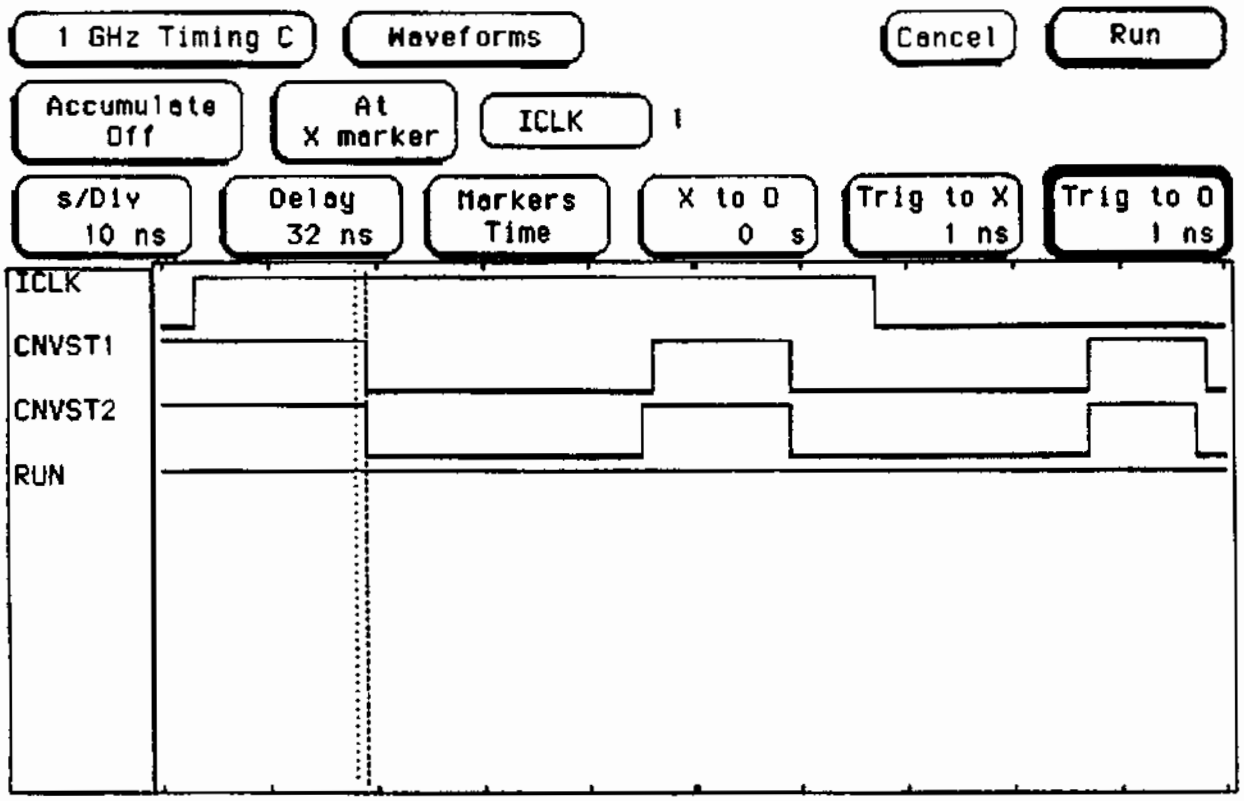


Figure 5-18 After 10 Minutes in Tightly-Coupled

5.8.3 Termination of Tightly-Coupled Mode

This section concludes with the termination of a tightly-coupled mode sampling period. Normally, tightly-coupled operations would only run from a pulse that exists for 8.625 µs → 4.000 µs. This demonstration has shown what happens for boards operating on the same carrier for ten minutes. They are still tightly-coupled (zero skew) having only been synchronized by the rising edge of RUN.

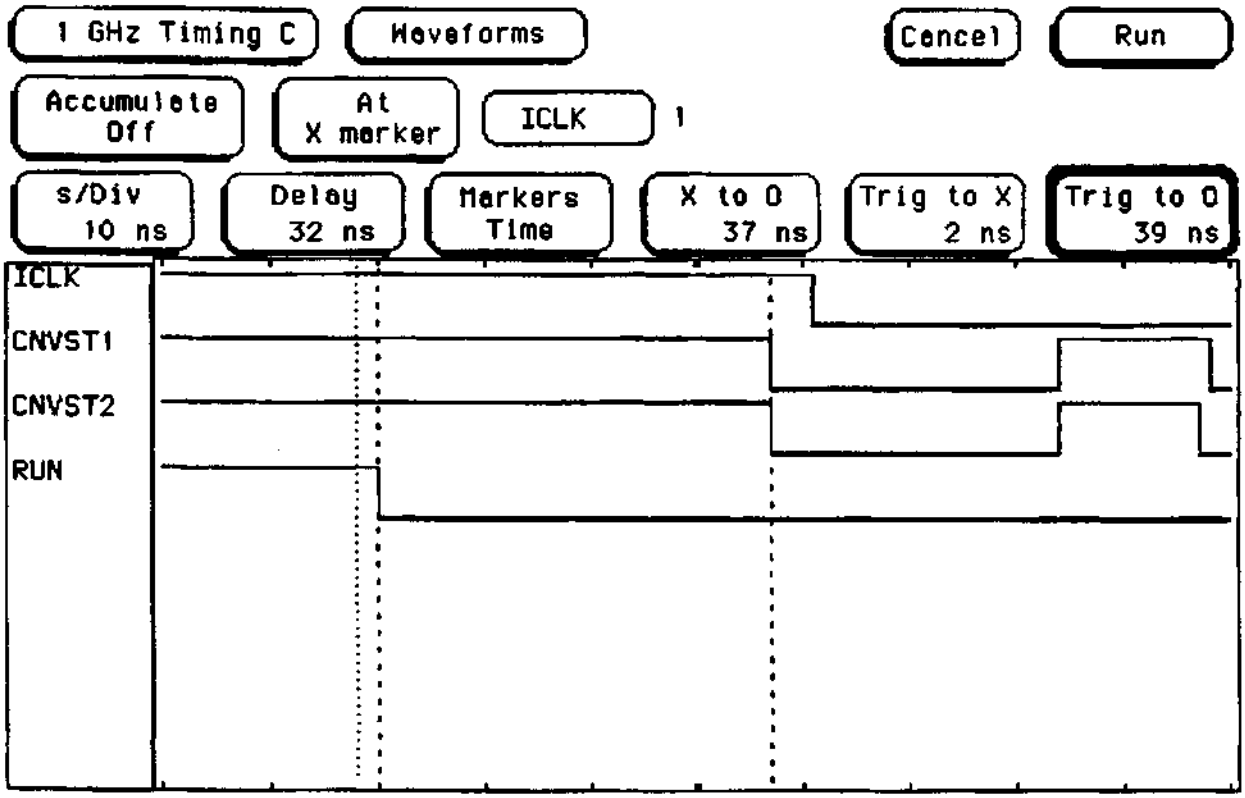


Figure 5-19 Termination of Tightly-Coupled Mode

Figure 5-19 presents the termination of a tightly-coupled sampling, regardless of the RUN signal's pulse width. It took 37 ns from the falling edge of RUN to terminate the sampling operations on both ADC128F1 IPacks. Remember that much of this delay is due to cable propagation delay time.

As these examples may have implied, the timing accuracy that can be achieved when running multiple ADC128F1 IPacks in tightly-coupled mode is quite high. It can be fine-tuned by varying the length of wire that feeds each individual ADC128F1's "RUN" input line if higher accuracy is needed than that which occurs by random cabling of these boards.

6.0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the ADC128F1 IPack to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Submission constitutes permission to publish without additional consent or compensation, and the author reserves the right to modify submissions to provide for more generic appeal, when necessary. Help advance the level of technology by participating with the SYSTRAN team while simultaneously publishing your ideas.

As an example of customer input, note the title "ADC128F1 = EASY POWER" at the top of Figure 6-1. It was provided by a customer who was impressed with how powerful the ADC128F1 is in solving his data acquisition problem while being so easy to use. As described in the following application notes, the ADC128F1 can do far more than the average analog-to-digital conversion product.

Additional information about the various modes of operation presented in this section can be found in section 2, paragraph 2.4: General Description.

6.2 Freerun A Single ADC128F1

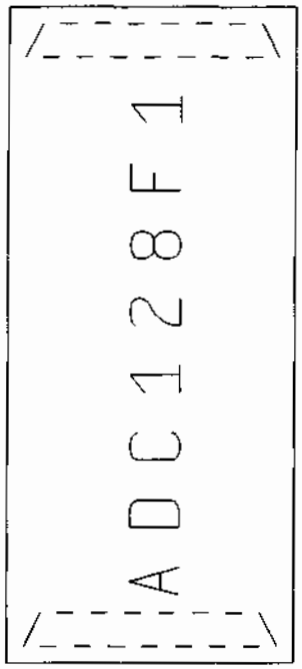
This mode of operation, when applicable for the system requirements, is the simplest usage of the ADC128F1. The ADC128F1 defaults to this mode on power-up with only analog signal inputs and ground connections attached at the I/O connector. Data is retrieved from the current value table (CVT) (any of the first eight I/O locations) when it is needed. The data retrieved from the CVT is never older than 8.625 µs.

If the conversion task involves emulating differential-input sampling by using two separate channels of the ADC128F1 and subtracting their difference, it is recommended that this mode not be used unless the inputs are VERY low in frequency. This is because there is a high probability that the data retrieved from the "+" channel and from the "-" channel will be from different samplings. If this is a problem, then use one of the modes of operation described in the following applications.

ADC128F1 = "EASY POWER"

FREERUN A SINGLE ADC128F1

@ CARRIER:
LOGIC CONNECTION



I/O CONNECTIONS

I/O CONNECTIONS:

PIN:	FUNCTION:
2	ANALOG INPUT, CHANNEL 1
4	ANALOG INPUT, CHANNEL 2
6	ANALOG INPUT, CHANNEL 3
8	ANALOG INPUT, CHANNEL 4
10	ANALOG INPUT, CHANNEL 5
12	ANALOG INPUT, CHANNEL 6
14	ANALOG INPUT, CHANNEL 7
16	ANALOG INPUT, CHANNEL 8
*	GROUND PLANE
44	RUN - LEAVE OPEN OR TIE HIGH
48	N_DATAOEG - LEAVE OPEN OR TIE HIGH
49	N_HUPOIS - LEAVE OPEN OR TIE HIGH

* IT IS RECOMMENDED THAT ALL AVAILABLE GROUND PLANE CONNECTIONS BE USED: PINS 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 20, 26, 27, 28, 29, 30, 32, 34, 36, 38, 40, & 42.

It is also recommended that the DATOE[2:0] inputs, which normally float, be tied high or low if they are not going to be used. DATOE[2:0] = pins 45, 46, & 47, respectively

Typical Usage:

After application of power, start reading data from first eight I/O locations.

For example, if the ADC128F1 is in slot 'A' of a Motorola MVME162-XX, using the 162Bug Debugger Command "MD FFF58000" will result in the display of all eight channels' data being presented on the Monitor's screen. Note that the twelve bits (three nibbles) of significant data is preceded by a leading most significant nibble = "F", which is due to the fact that the IPDbus has pull-up resistors on every line on the carrier, and that the ADC128F1 does not drive IPD[15:12]

TWD: F:\SYSNET\IPACKS\ADC128F1\SCH\APPLICAT 1

Figure 6-1 Freerun A Single ADC128F1

6.3 Single ADC128F1 Snapshot

For applications that must have multiple-channel data from exactly the same sampling, the mode of operation presented in Figure 6.2 is recommended. This is advisable when any or all of the ADCs on any one ADC128F1 are converting high frequency signals or want to maintain valid phase relationships between signals for post-capture data analysis or process control. As in the mode of operation presented in section 6.2 above, the ADC128F1 powers-up free-running.

The snapshot is taken by blocking CVT updates by asserting the one software control bit, "N_SUPDIS", the Software UPdate DISable function. The ADCs continue to freerun but the data in the CVT is frozen for subsequent data retrieval at any pace in any sequence. When the data has been retrieved, the N_SUPDIS bit should be negated to allow for subsequent CVT updates. As in application 6.2, the data retrieved from the CVT is never older than 8.625 μs. The difference is that all of the data retrieved is from exactly the same sampling. The uncertainty between channels of actual sampling times is to within a few nanoseconds, which should be sufficient for most applications.

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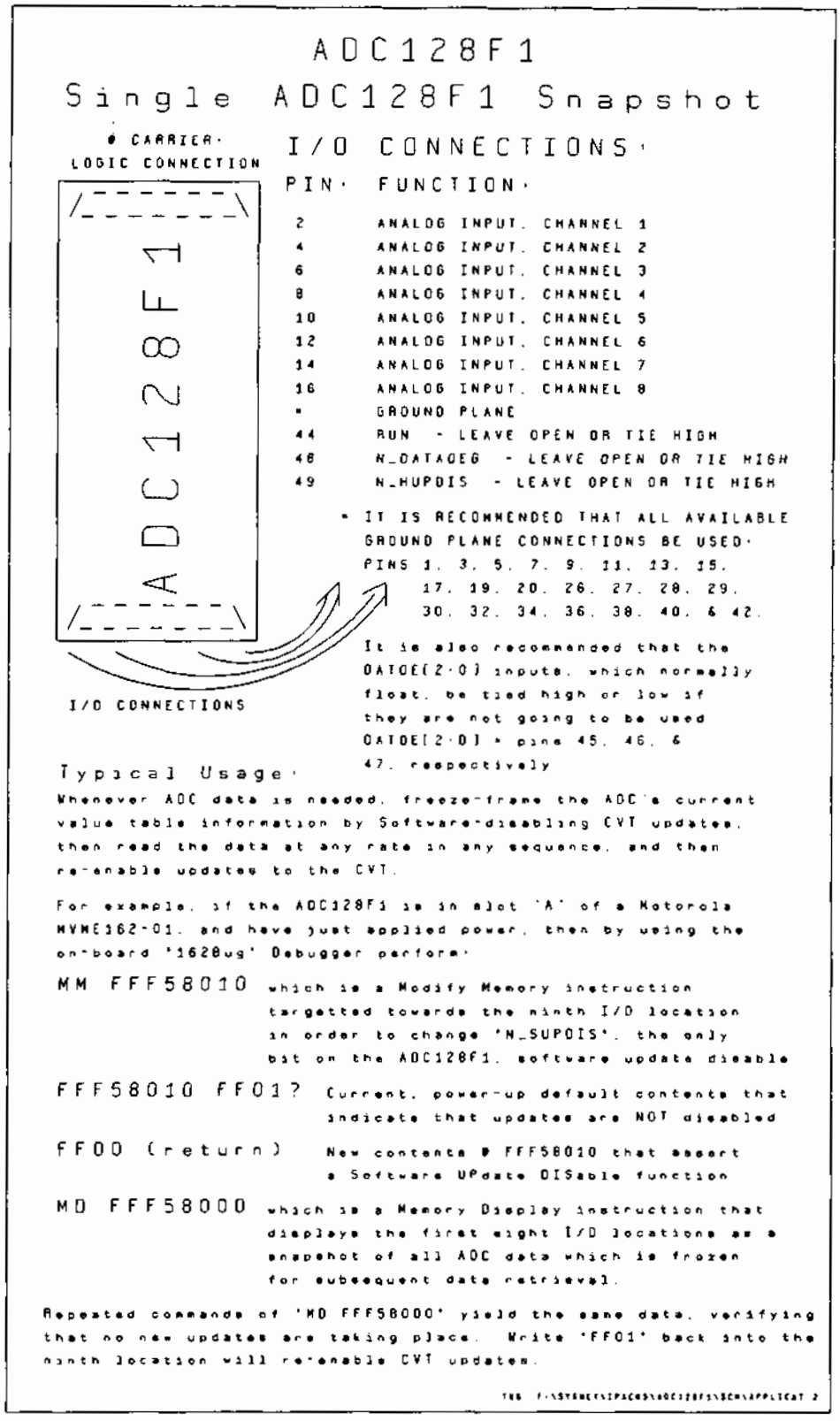


Figure 6-2 Single ADC128F1 Snapshot

6.4 Multi-board Loosely-coupled Snapshot

For applications that want to capture data from multiple ADC128F1's at about the same time, the mode of operation presented in Figure 6-3 is recommended. Basically, it is a multi-board, hardware controlled version of the snapshot technique presented in application 6.3. All of the ADC128F1 boards to be coupled together have their I/O Connector pin 49 wired together, and are controlled by a single digital output line from another IPack (like the TRIDO48 or DIO316I).

There are no special timing constraints for this mode of operation. As before, the snapshot is taken by blocking CVT updates. Instead of asserting the N_SUPDIS bit for a single ADC128F1, the user asserts "low" the digital line that is connected to the ADC128F1's N_HUPDIS control input; the Hardware UPdate DISable function. The ADCs continue to freerun, but the data in the CVTs is frozen for subsequent data retrieval at any pace in any sequence. When the data has been retrieved, and to allow for subsequent CVT updates, the N_HUPDIS control line should be negated by setting high the digital output line controlling the multiple ADC128F1 IPacks. As in all previous application notes, the data retrieved from the multiple CVTs is never older than 8.625 µs. This means that the uncertainty in the actual sampling time from one ADC128F1 to any other is ≤ 8.625 µs, while data retrieved from adjacent channels on any single ADC128F1 is obtained at the same time (to within a few nanoseconds).

Note that the TRIDO48 used in Figure 6-3 has its Default Output-Enable State (DOES) switch in the '1' position to enable its outputs on power-up. Since the data registers on the TRIDO48 are all cleared on power-up, all of the CVT data on all controlled ADC128F1 IPacks is frozen as zeroes because the N_HUPDIS line is asserted low on power-up. If the TRIDO48's DOES switch had been set to '0' to disable its outputs on power-up, then the N_HUPDIS control inputs on the ADC128F1's coupled together would be pulled-high to enable CVT updates.

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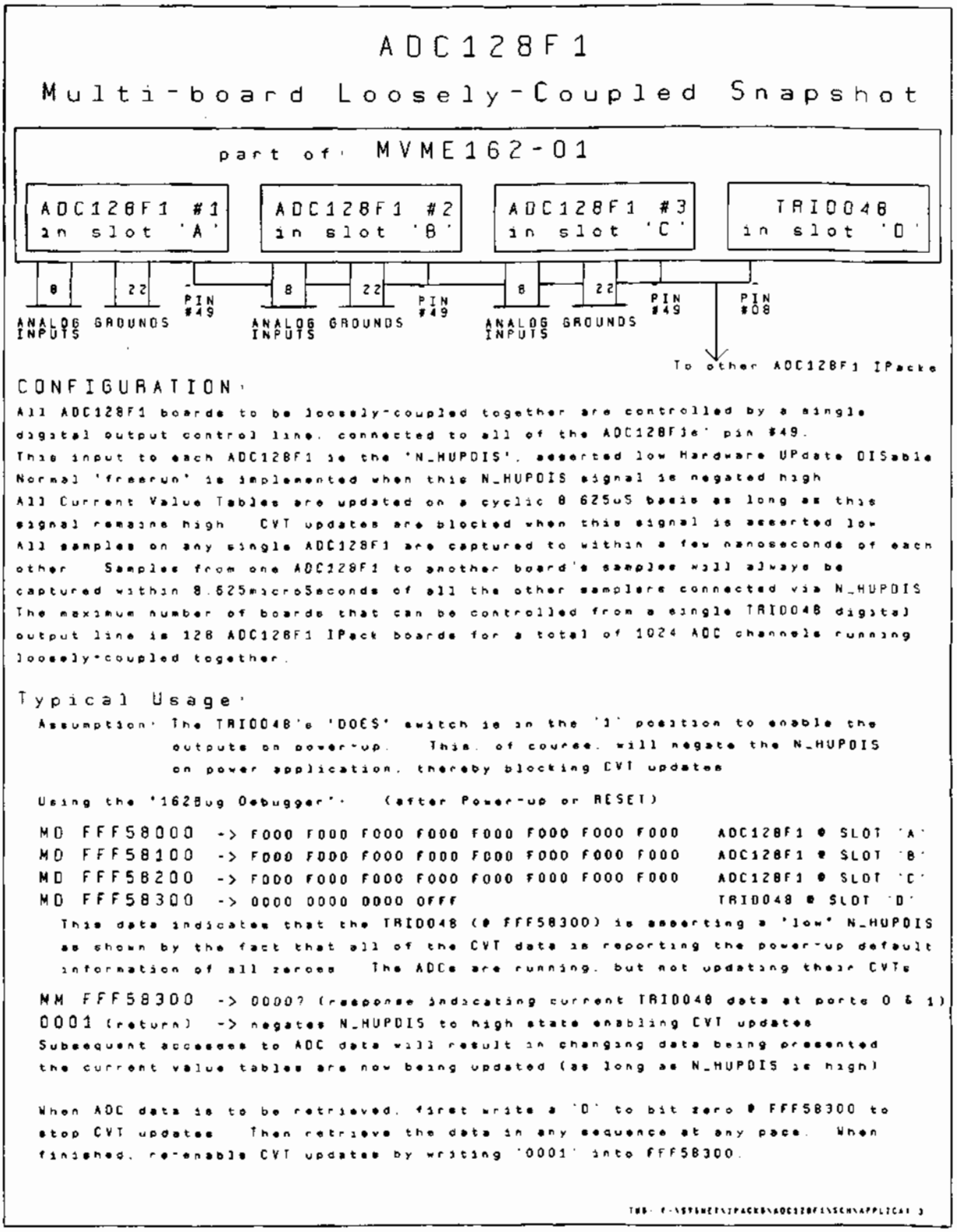


Figure 6-3 Multi-board Loosely-Coupled Snapshot

6.5 Multi-board Tightly-coupled Snapshot

For applications that must have all of the analog signals sampled at exactly the same time across multiple ADC128F1 boards, the mode of operation presented in Figure 6-4 is recommended. There are two basic differences in operation between this mode and that presented in 6.4, the loosely-coupled snapshot (These differences are presented in Figure 6-4):

- The first difference is that the digital control line is connected to the ADC128F1 pin 44 (instead of pin 49) to control the "RUN" line inputs.
- The second is that there is special timing constraints for this mode of operation.

There are two obvious techniques for the development of the "RUN" pulse required for tightly-coupling multiple ADC128F1 IPacks.

- The first one, as presented in Figure 6-4, uses a software controlled technique where a software loop or system real-time clock is used to develop the assertion and negation intervals for setting and clearing the digital line that controls the "RUN" signal.
- A second technique could involve the utilization of an automatic pulse generation signal source like that which could be developed by the DUAL16CT or DUAL32CT IPacks. Besides developing the proper pulse width and cyclic repetition rate for the "RUN" signal, these two IPacks could also signal the processor when it is time to retrieve the ADC data by the assertion of an interrupt on the falling edge of the "RUN" signal.

The ADCs only execute sampling operations when "RUN" is asserted high. They all start their conversion process on the rising edge of "RUN". They automatically start a second sampling and conversion process on the rising edge of N_CONVST after the first sampling has been posted in the CVT. However, the conversion results will not be posted in the CVT, overwriting the first posting, provided the "RUN" signal is negated in the time span presented in Figure 6-4.

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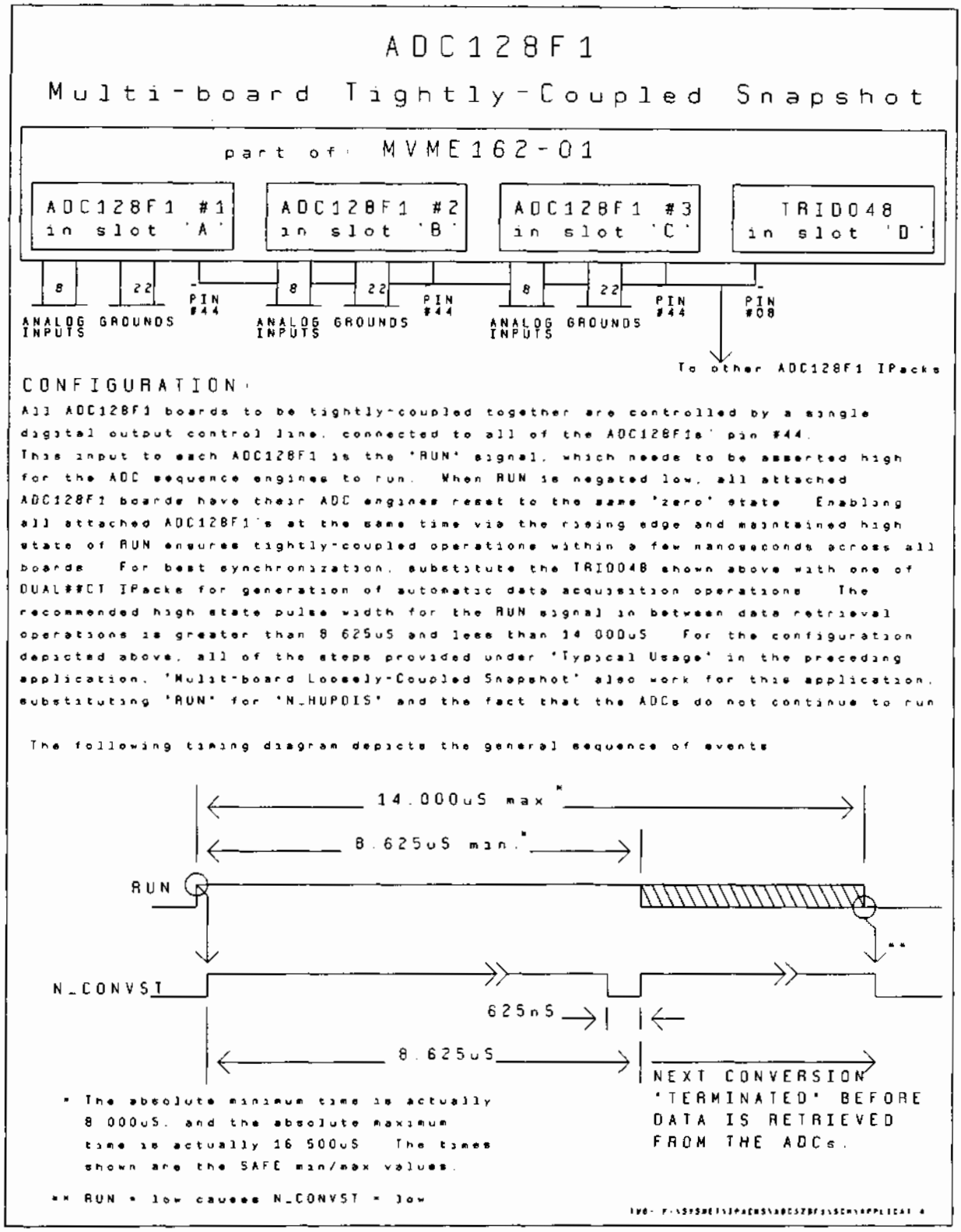


Figure 6-4 Multi-board Tightly-Coupled Snapshot

6.6 ADC Data Stream Logging

This application note presents one of many possible techniques to data-log, in real time, information being presented on the monitor ports of two different ADC128F1 IPacks. The ADC128F1 modes of operation can be any of those presented so far, being primarily dependent on the time relationship requirements of the data being recorded.

Since the channel number is also recorded with the data as an upper-nibble "tag", it is possible to change the information being driven from the TRIDO48 into the ADC128F1's DATAOE[2:0] inputs on-the-fly, provided changes are made at a time to allow for proper data settling before being strobed into their respective FIFOs by their N_CONVST signals.

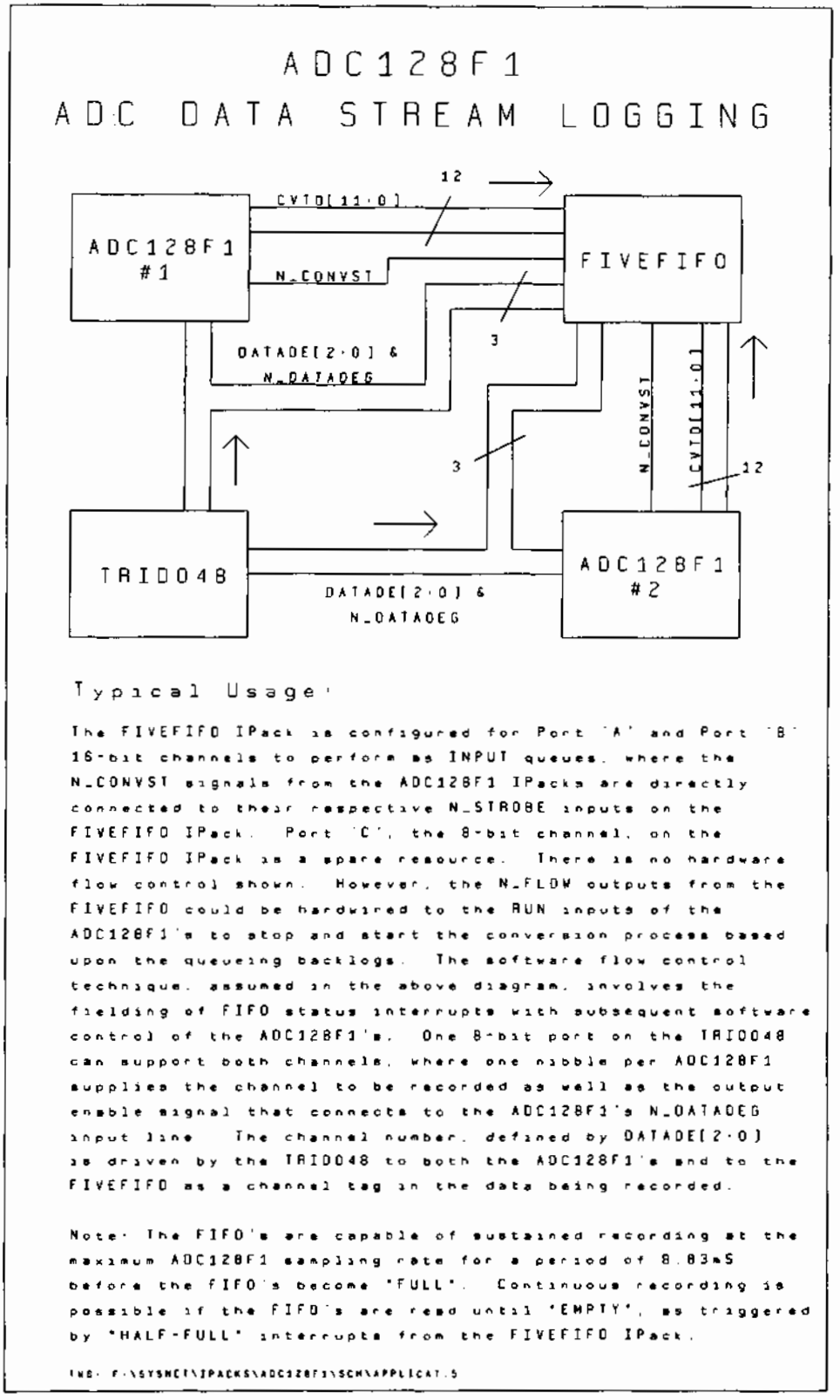


Figure 6-5 ADC Data Stream Logging

6.7 Real-time Monitoring

There are many laboratory and test configurations that require independent (of software) monitoring of ADC information, as a cross-check technique for verifying the accuracy of the conversion process, especially prior to and following special, and often very expensive, test events.

One example, out of many, of this kind of requirement is that of a crash survivability test, where dozens to hundreds of sensors need to be calibrated prior to a test, and confirmed for no shift in accuracy following a test. Often this is done as an independent verification path to ensure that data retrieved via software matches that retrieved at the hardware monitor port, avoiding any issues that may arise from possible software modifications to the retrieved data.

Many times this monitoring technique is tightly-coupled to a sensor-shunt or voltage substitution calibration circuit. Figure 6-6 is a presentation of the latter technique, where a precision (usually traceable) voltage source is injected into the channel being calibrated with the error in conversion being recorded for post-test analysis compensation. Very little additional circuitry is needed to obtain a technique for performing data logging, whether it is used in real-time or not.

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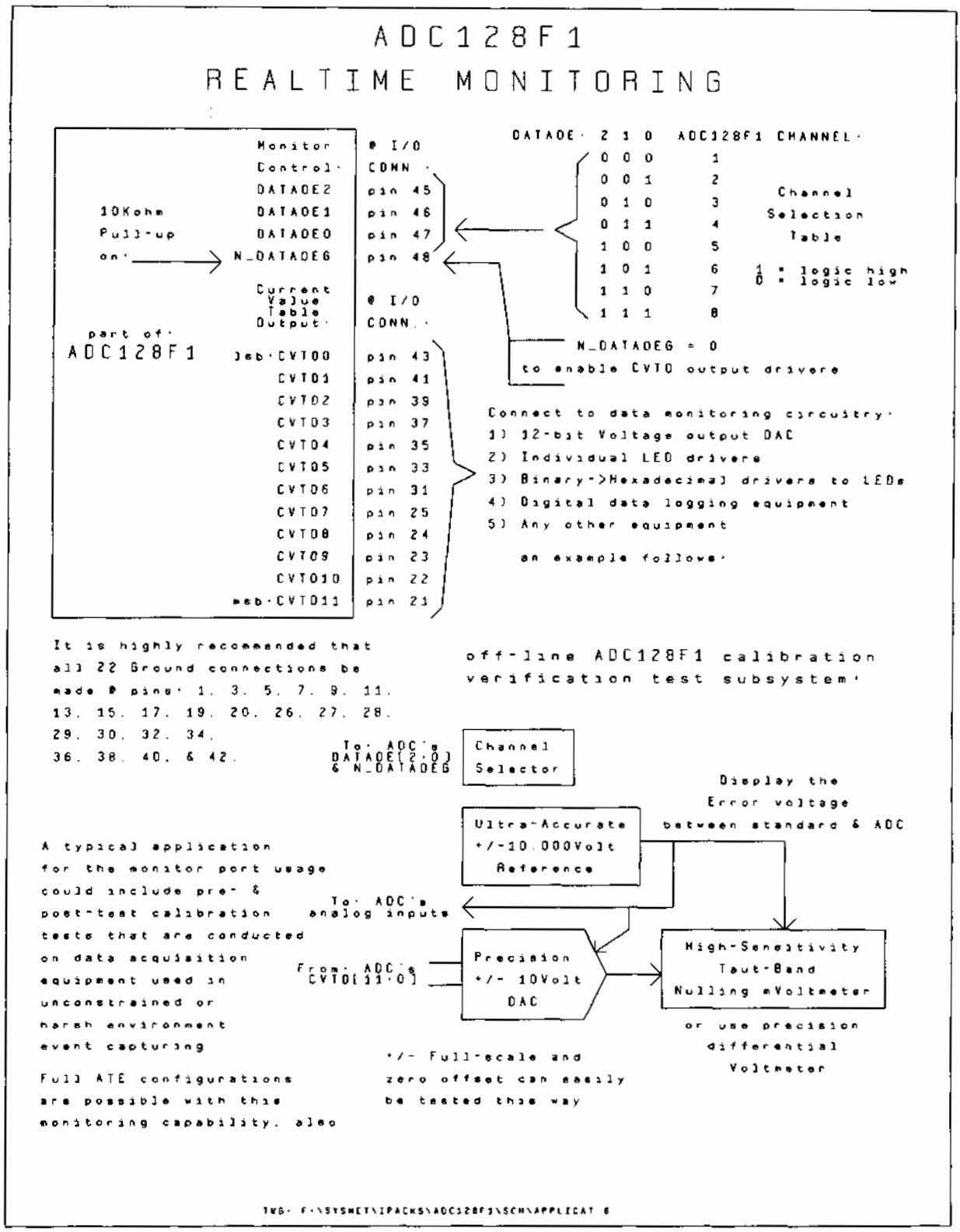


Figure 6-6 Real-time Monitoring

7.0 WARRANTY AND REPAIR

7.1 Warranty Coverage

SYSTRAN makes no warranty of any kind, express or implied, with regard to products, except that SYSTRAN warrants that products delivered will be free from defects in materials or workmanship for a period of three hundred sixty five (365) days from the date of original shipment. During the warranty period, SYSTRAN will provide, free of charge to Buyer, the Warranty Services defined below:

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Hardware Warranty Service consists of factory exchange or repair (at SYSTRAN's sole option) of defective Hardware Products to correct malfunctions which occur during normal use. In the event SYSTRAN decides to replace a failed part or piece of equipment, SYSTRAN shall have the right to replace it with either a new part or piece of equipment, or factory reconditioned part or piece of equipment. Replaced parts or pieces of equipment become the property of SYSTRAN.

Hardware Warranty Services do not include the repair or replacement of equipment or parts which have otherwise become defective, including, but not limited to, damage caused by accidents, modifications or alterations by Buyer, physical abuse or misuse, operation in an environment or conditions outside SYSTRAN's specifications for the Hardware Products, acts of God, and fires. Hardware Warranty Services also exclude labor and material cost of relocation, rearrangement, additions to, and removal of Hardware Products.

Buyer must report hardware malfunction to SYSTRAN Customer Service and obtain a Return Authorization Number. Defective hardware should then be shipped prepaid to SYSTRAN. Repair or replacement will then be returned prepaid upon receipt of the defective item.

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Software Warranty Service consists of update services covering changes to any combination of documentation and software required to maintain Software Products at the revision level most currently released by SYSTRAN. This Software Warranty Service does not include changes or upgrades, or options intended to broaden, enhance or improve the capabilities of the Software Product.

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Also included in the Warranty Services for the covered Products are periodic newsletters announcing new products and applications, and application notes.

THE FOREGOING WARRANTIES ARE IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ANY WARRANTY THAT EQUIPMENT PURCHASED HEREUNDER IS OF MERCHANTABLE QUALITY.

7.2 Additional Paid Services

Should Buyer request services which are beyond the scope of the Hardware, Software or Other Warranty Services specified above, these will be provided by SYSTRAN on a time-and-materials basis at the prices in SYSTRAN's published Price List. Such services will then be undertaken by SYSTRAN after SYSTRAN has given Buyer an estimate of the services required and only after SYSTRAN receives written authorization from Buyer.

7.3 Term

This Warranty is effective for a period of three hundred sixty five (365) days from the date of the original shipment.

7.4 Conditions

Services provided under this Warranty are performed at the SYSTRAN factory, Monday through Friday, 8:00 a.m. through 5:00 p.m. Eastern Standard/Daylight Savings Time, excluding SYSTRAN's holidays. SYSTRAN's performance goal is to ship to Buyer a repaired or replacement Hardware Product within 48 hours of SYSTRAN's receipt of the defective Hardware Product.

7.5 Identification of Covered Products

Products covered by this Agreement shall be identified by their SYSTRAN Serial Numbers which will be affixed on the respective product.

7.6 Shipping

When factory repair services are required, Buyer shall ship or deliver products, freight prepaid, to the SYSTRAN factory. SYSTRAN will return Products, freight prepaid, to Buyer. SYSTRAN reserves the right to select the carrier and shipping method for return shipments. Upon request, Products will be shipped by Buyer's carrier or by a Buyer-specified shipping method for return shipments. Any shipping charges incurred by SYSTRAN for such Buyer-specified shipping will be invoiced separately to Buyer.

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Life support devices or systems are those which support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.

Examples of nuclear facility applications are those (a) in a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing, or disposal of fissionable material or waste products thereof.

SYSTRAN's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages. Buyer uses or sells such products for life support or nuclear facility applications at Buyer's own risk and agrees to defend, indemnify, and hold SYSTRAN Corp. harmless from any and all damages, claims, suits, or expense resulting from such use.

7.8 Communication

Contact SYSTRAN Customer Support by calling (513) 252-5601, or send an E-Mail message to **support@systran.com** for assistance.

APPENDIX A

SYSTRAN CORPORATION's
IP SPECIFICATION SYNOPSIS
of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:

This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small form-factor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general-purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high-speed (32 MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system-level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP", and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8 MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a "doublewide" board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8MHz clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real-world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9" by 1.8" size allows for convenient modular placement of 1, 2, 4, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME-3U, Nubus, VME-6U, ISA, "C" size VXIbus, and VME-9U, as well as stand-alone (embedded processor) carriers of various sizes. A "doublewide" IP is 3.9" by 3.6" in size, and appears mechanically and electrically as two "singlewide" IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:

The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the " I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0 mA (logic low) in parallel with 30 ρF. All signals have a 10 KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK

This signal, ≡ CLK in the specification, is an 8 MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's "logic" connection is via pin 2. The loading is 6.0 mA (logic low) maximum in parallel with 30ρF.

IPA[6:1] (Address bus)

These six lines, ≡ A1...A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for "singlewide" boards, and 32-bit data boundaries for "doublewide" boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as these are defined by individual select lines from the carrier.

IPD[15:0] (Data bus)

These sixteen lines, ≡ D00...D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus ≡ IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For "doublewide" IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but can be any number of bits. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14,

13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET

This signal, ≡ RESET★ in the specification, is the asserted low reset signal. The carrier is required to assert N_RESET for a minimum of 200 ms following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)

This signal, ≡ R/W★ in the specification, is the data direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)

This signal, ≡ ACK★ in the specification, is the asserted low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier-driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)

N_BS1 (high Byte Select)

These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted low byte select lines driven by the carrier to the IP to indicate which byte lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low, or odd byte IPD[7:0], while N_BS1 selects the high, or even byte IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes IPD[15:0] are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)

This signal, ≡ MemSel★ in the specification, is the asserted low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)

This signal, ≡ IOSel★ in the specification, is the asserted low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)

This signal, ≡ IntSel★ in the specification, is the asserted low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. "Doublewide" IPs may respond with a-side only, or b-side only transfers; both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)

This signal, ≡ IDSel★ in the specification, is the asserted low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For "doublewide" IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)

N_INTREQ1 (INTerrupt REQuest #1)

These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are asserted low interrupt requests driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:

The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin

34. Pin 36 is a reserved pin, as is pin 49. DMAEnd* is found at pin 38. Error* is found at pin 40; and Strobe* is found at pin 46.

POWER/GROUND:
+5 volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero volts reference, comes in pins 1, 25, 26, and 50; +12 volts is sourced via pin 23, and, -12 volts comes in pin 22.

CYCLE TYPES:
There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal. A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the first, select cycle. Idle cycles are those between select and terminate cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:
There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:
Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both "singlewide" and "doublewide" IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:
The outside dimensions of a "singlewide" IP are 1.800" by 3.900", +.000/-.020". The outside dimensions of a "doublewide" IP are 3.600" by 3.900", +.000/-.020". There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the "logic" interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8" by 3.188" between the connectors for a "singlewide" IP, and 3.6" by 3.188" for a "doublewide" IP. The maximum height of components on the IP is 0.315", with components exceeding 0.250" in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70°C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40°C up to +85°C.

ADDITIONAL INFORMATION:
The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 1204 O'Brien Drive, Menlo Park, CA 94025.

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MEMORY TRANSFERS - CYCLE TABLES

CYCLE -	MEM WRITE NO HOLDS NO WAITS			MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS					MEM WRITE 1 HOLD 3 WAITS									DRIVEN BY: IPack	DRIVEN BY: CARRIER
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WTGHLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE		
IPA[6-1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15-0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH @ END OF:			◇					◇			◇											◇					

CYCLE -	MEM READ NO HOLDS NO WAITS			MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS					MEM READ 1 HOLD 3 WAITS					DRIVEN BY: IPack	DRIVEN BY: CARRIER
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WTGHLD	WTGHLD	HOLD	TERM	IDLE	SELECT	WTGHLD	WAIT	WAIT	TERM		
IPA[6-1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15-0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND:

- * IPD[15:0] = IPA[22:7] during during the SELECT cycle, and is used for data for all other cycles.
- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE - +5v
- 0 — LOW STATE - GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPack
- ◇ — IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED. IDLE, WAIT & HOLD ARE NOT REQUIRED

IO TRANSFERS - CYCLE TABLES

CYCLE	IO READ NO HOLDS NO WAITS			IO READ NO HOLDS 2 WAITS				IO READ 3 HOLDS NO WAITS					IO READ 1 HOLD 3 WAITS						IO READ 2 HOLDS 2 WAITS					DRIVEN BY: IPack	DRIVEN BY: CARRIER
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WTGHLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WTGHLD	WTGHLD	TERM	IDLE		
IPA[6-1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7-0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1		✓

GENERAL LEGEND:

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE - +5v
- 0 — LOW STATE - GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPac

INT TRANSFERS - CYCLE TABLES

CYCLE	INT READ NO HOLDS NO WAITS			INT READ NO HOLDS 3 WAITS				INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS						INT READ 1 HOLD 2 WAITS					DRIVEN BY: IPack	DRIVEN BY: CARRIER
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WTGHLD	WTGHLD	HOLD	TERM	IDLE	IDLE	SELECT	WTGHLD	WAIT	TERM	IDLE		
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	X	→	→	→	→	X		✓
PD[7-0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	X	Z	Z	Z	←	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

- * IPA1 CAN BE IGNORED IF ONLY ONE INTERRUP IS SUPPORTED (must be at LEVEL 0)
- ** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH

WAITS ARE INVOKED BY THE IPACK

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED. IDLE, WAIT HOLD ARE NOT REQUIRED

I/O TRANSFERS CYCLE TABLES

CYCLE	I/O WRITE NO HOLDS NO WAITS				I/O WRITE NO HOLDS 3 WAITS						I/O WRITE 2 HOLDS NO WAITS						I/O WRITE 3 HOLDS 1 WAIT						DRIVEN BY	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	SELECT	WTRHLD	HOLD	HOLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	→	→	→	→	→	X		✓
IPD[15:0]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	→	→	→	→	→	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	0	0	0	0	0	X		✓
DATA LATCH (beg of)			◇						◇			◇									◇					

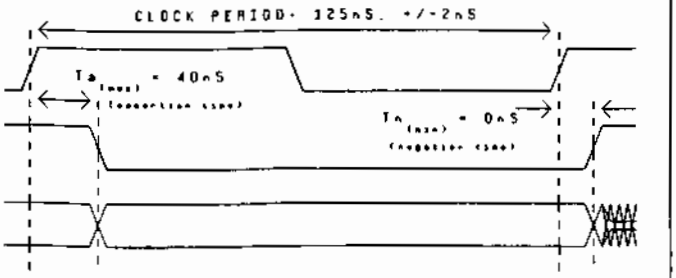
CYCLE	I/O READ NO HOLDS NO WAITS				I/O READ NO HOLDS 2 WAITS						I/O READ 3 HOLDS NO WAITS						I/O READ 2 HOLDS 3 WAITS							I/O READ 3 HOLDS 2 WAITS							DRIVEN BY	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	SELECT	WTRHLD	WTRHLD	WAIT	TERM	IDLE	SELECT	WTRHLD	WTRHLD	HOLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	→		✓	
IPD[15:0]	X	Z	←	X	Z	Z	Z	←	X	Z	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←		✓		
IPR/N_W	X	1	1	X	1	1	1	1	X	1	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1			✓	
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0		✓		
N_IOSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1			✓	

GENERAL LEGEND:

- X = DON'T CARE
- Z = HIGH IMPEDANCE
- 1 = HIGH STATE, +5V
- 0 = LOW STATE, GND
- → = DRIVEN INTO IPack
- ← = DRIVEN OUT OF IPack
- ◇ = IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.
HOLDS ARE INVOKED BY THE CARRIER
SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

VALID TRANSFER SELECTION MATRIX

TRANSFER TYPE: / SIDE: / ASSERTED LOW:	DOUBLEWIDE								SINGLEWIDE				VALID TRANSFER(s):
	N_B_MEMSEL	N_B_IOSEL	N_B_INTSEL	N_B_IOSEL	N_A_MEMSEL	N_A_IOSEL	N_A_INTSEL	N_A_IOSEL	N_MEMSEL	N_IOSEL	N_INTSEL	N_IOSEL	
	1	1	1	1	0	1	1	1	0	1	1	1	MEMORY: A-SIDE ONLY
	0	1	1	1	1	1	1	1					MEMORY: B-SIDE ONLY
	0	1	1	1	0	1	1	1					MEMORY: BOTH SIDES
	1	1	1	1	1	0	1	1	1	0	1	1	I/O: A-SIDE ONLY
	1	0	1	1	1	1	1	1					I/O: B-SIDE ONLY
	1	0	1	1	1	0	1	1					I/O: BOTH SIDES
	1	1	1	1	1	1	0	1	1	1	0	1	INTERRUPT: A-SIDE ONLY
	1	1	0	1	1	1	1	1					INTERRUPT: B-SIDE ONLY
	1	1	1	1	1	1	1	0	1	1	1	0	IO: A-SIDE ONLY

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B-T-SH-IPACKSUM-A-0-A2 (07-15-94)

APPENDIX B

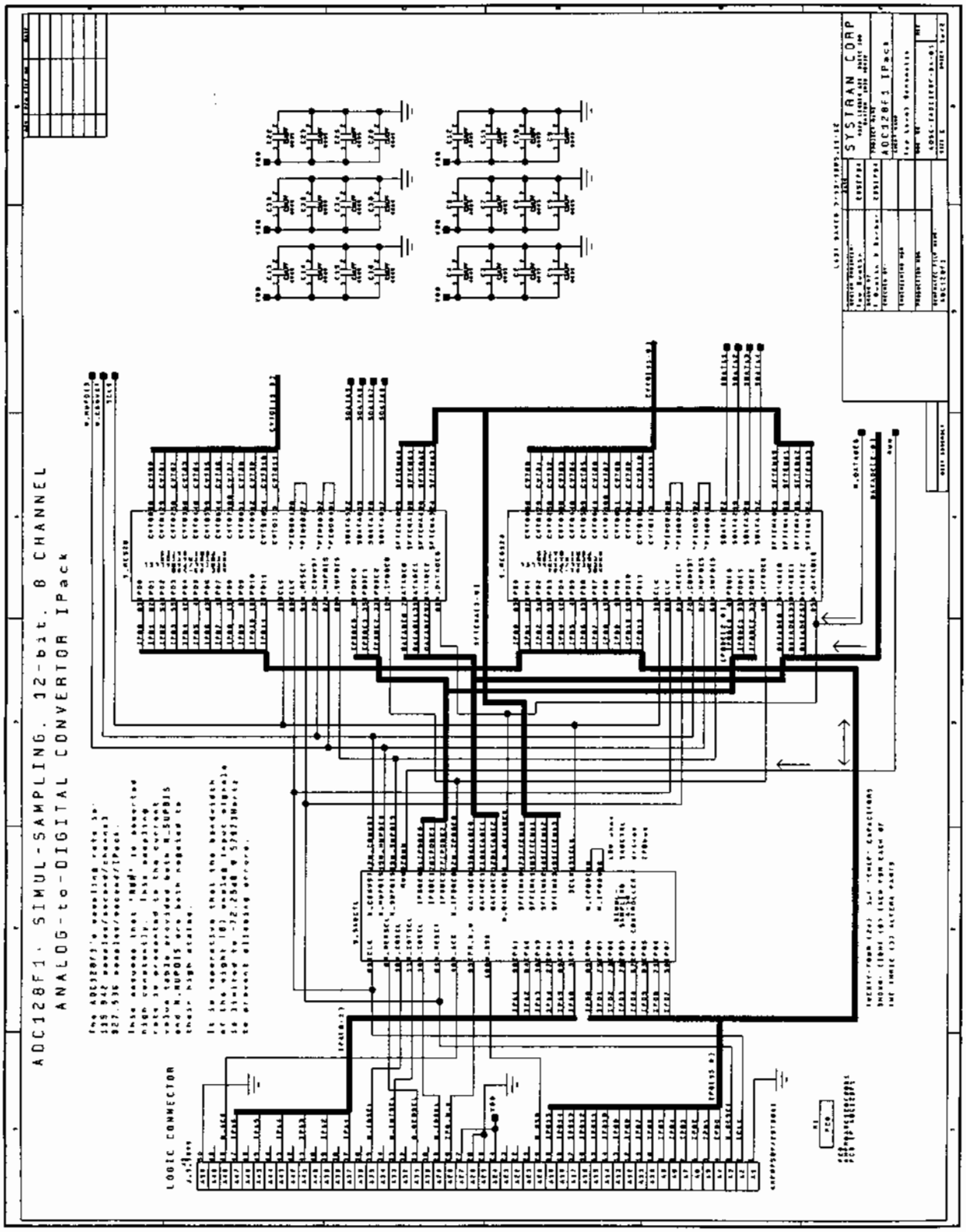


Figure B-1 Schematic #1

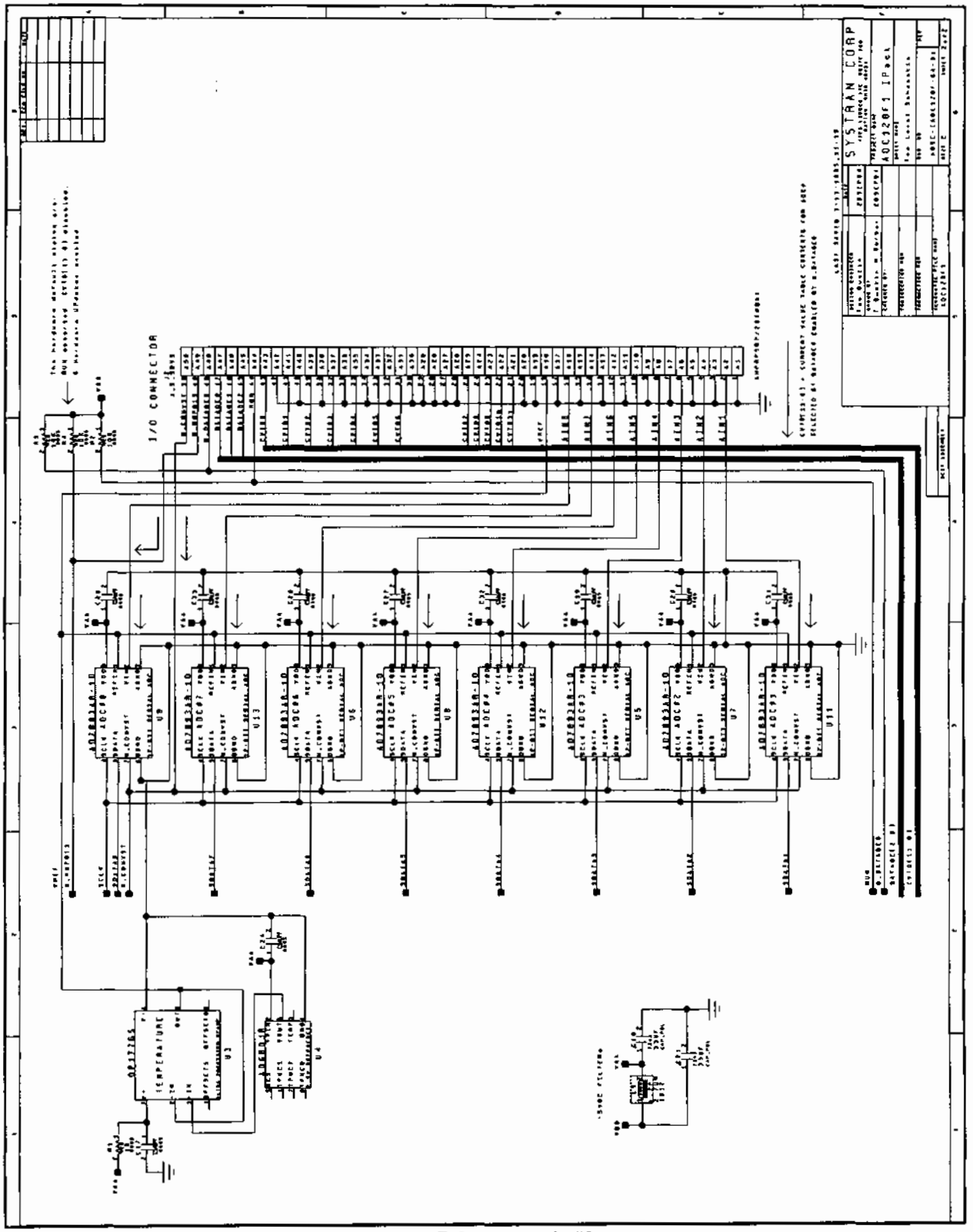


Figure B-2 Schematic #2

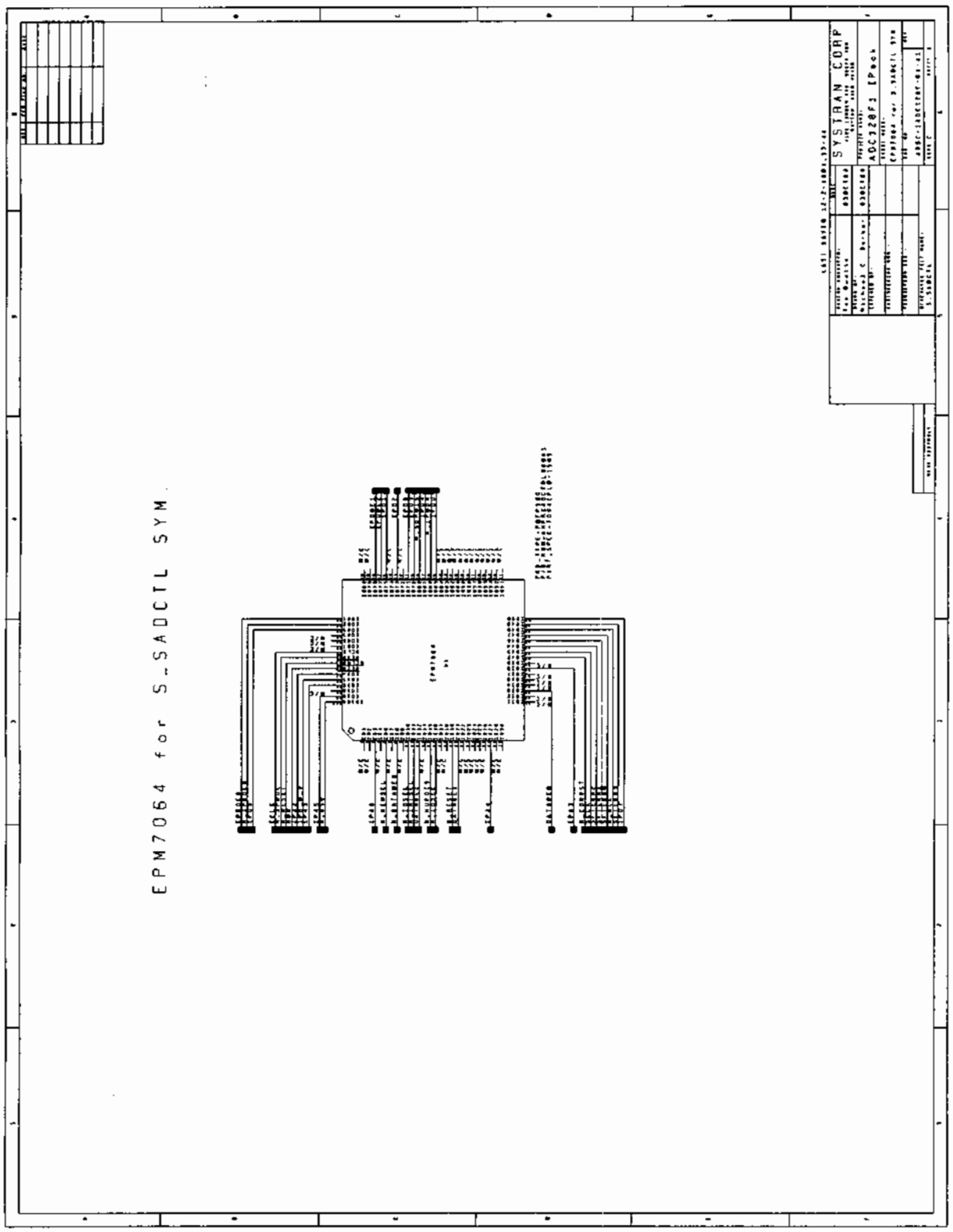


Figure B-3 Schematic #3

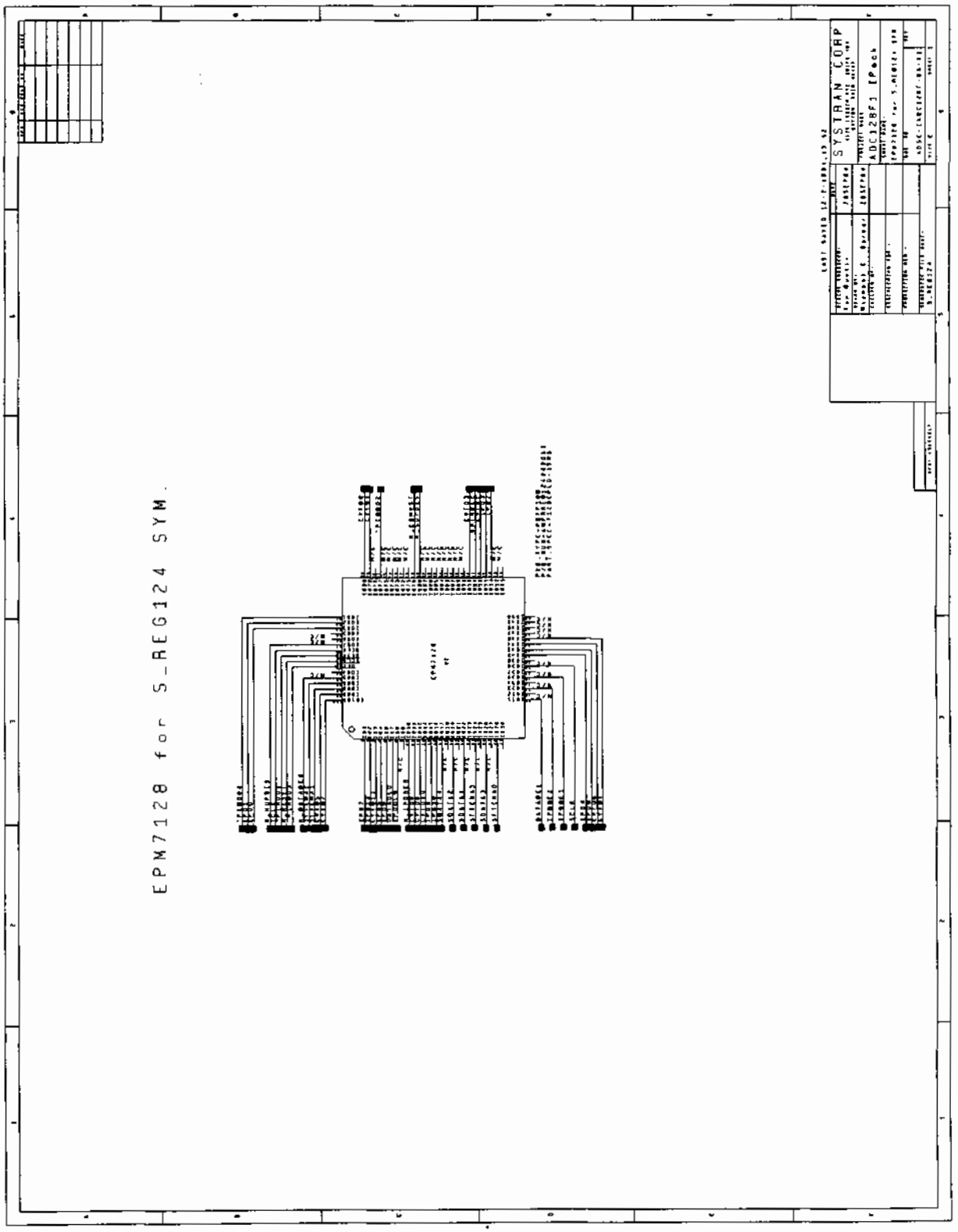


Figure B-4 Schematic #4

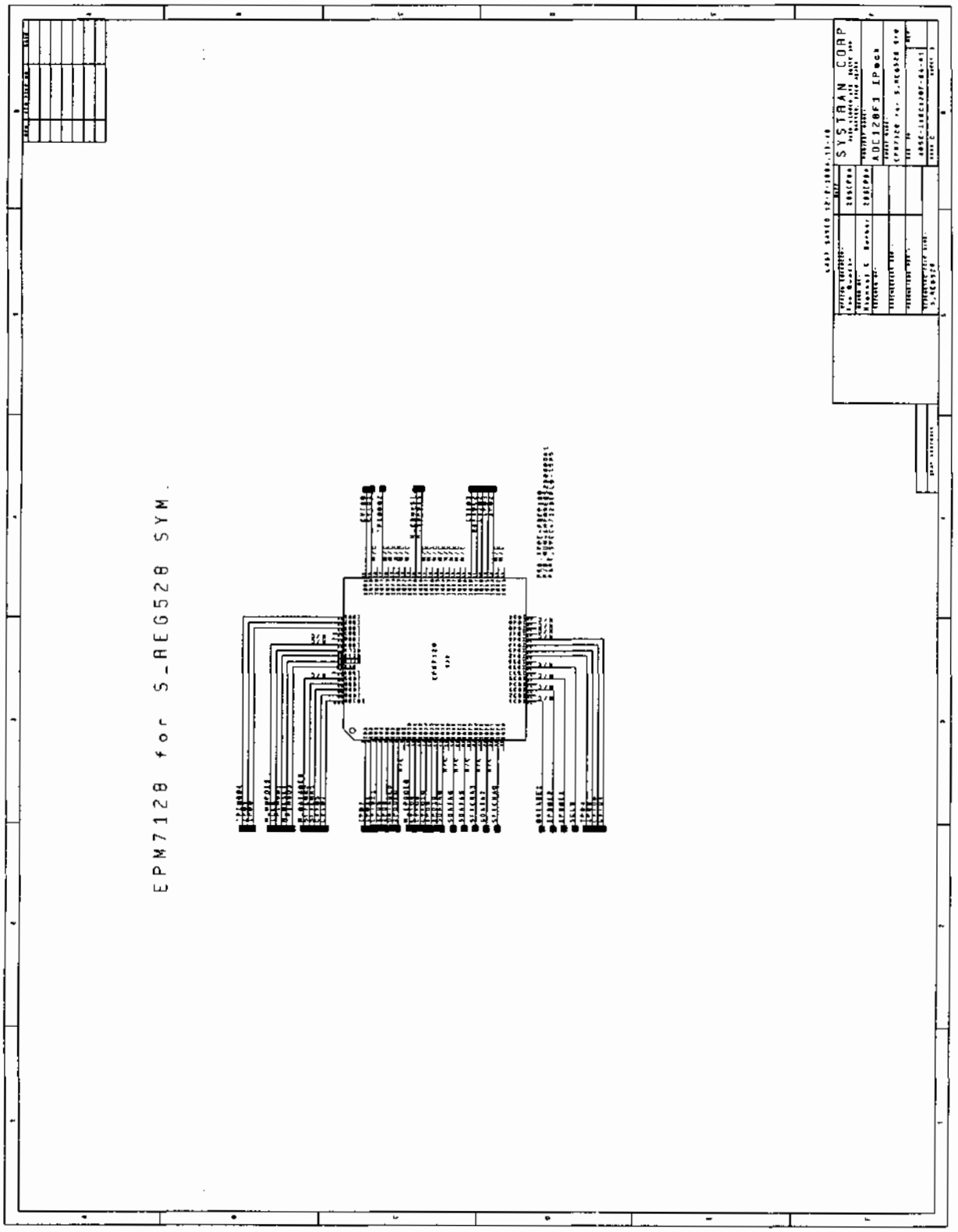


Figure B-5 Schematic #5

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