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ADC128F1

8-Channel, 12-Bit, ±10 V Simul-Sampling A/D Converter Hardware Reference

Document No. B-T-MR-ADC128F1-A-0-A4

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's 8-channel, 12-bit, ±10 V Single-ended Inputs, Simul-sampling Analog-to-Digital Converter (ADC) IP Module board, referred to in this manual as the ADC128F1 (part number BHAS-ADC128F1).

1.1.2 Scope

This reference manual covers the physical and operational description of the ADC128F1, both from hardware and software perspectives. This manual also contains detailed technical information about the ADC128F1's performance characteristics, and some typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Conventions

- A bit-range is designated by [x:y], where "x" is the left-most bit and "y" is the right-most bit. For example, Data bus [7:0] refers to the Least Significant eight bits.
- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2              file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001).

- ANSI/VITA 4-1995 published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA. Phone: 480-951-8866, FAX: 480-951-0720, E-mail: info@vita.com, URL: www.vita.com.
- *ADC128F1 Software Library Manual (OS-9)* (Document No. B-T-ML-ADC128F1).
- *ADC128F1 Software Library Manual for PCI/CPCI IP Carriers Using Windows NT 4.0* (Document No. B-T-ML-NTAAP).
- *DIO316I – DIO316I Tristateable 48-Channel Digital I/O IP Module Hardware Reference* (Document No. B-T-MR-DIO316I).
- *TRIDO48 – Tristateable 48-Channel Digital Output IP Module Hardware Reference* (Document No. B-T-MR-TRIDO48).
- Systran Corporation: www.systran.com.

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Our Quality System addresses the following basic objectives:

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- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

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applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

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2. PRODUCT OVERVIEW

2.1 Overview

The ADC128F1 is a singlewide IP Module board, conforming both mechanically and electrically to the American National Standard for IP Modules (ANSI/VITA 4-1995) specification. For a typical IP Module carrier that holds four IP Modules, the ADC128F1 can provide up to 32 channels of high-performance ADCs in a single slot on a computer bus backplane, or be mixed with other IP Modules for a more customized, modular I/O system solution.

The ADC128F1 maintains the highest possible accuracy and performance characteristics by minimizing accumulative analog errors in the design through the use of the best components for the tasks to be accomplished.

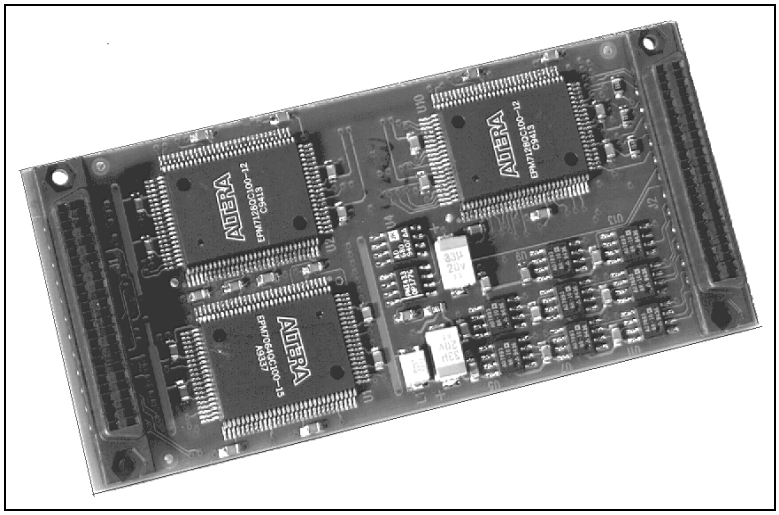


Figure 2-1 ADC128F1 Board

2.2 The Name

The product name of ADC128F1 consists of several descriptive components. The ADC portion indicates its primary function of performing analog-to-digital conversions. It has one dedicated converter per channel. The next "12" field indicates the number of bits of resolution (not accuracy). The "8" indicates how many analog input channels are available. The last "F1" indicates that the input range is fixed and that the span is ±10 V.

2.3 Features

- Eight independent channels of 12-bit, switched capacitor SAR-based ADCs with all channels tightly-coupled for "true" simultaneous sampling and conversion at a free-run rate of 115,942 samples/second/channel, for a board total of 927,536 samples/second.
- Automatic power-up of all eight ADC channels converting and depositing results simultaneously into a current value table (CVT) every 8.625 μs.

- Modes of operation vary from simply reading the latest results from the CVT through software and hardware handshake interfaces for loosely and tightly coupling multiple ADC128F1 IP Modules together for large, ganged simul-sampling applications.
- Elimination of "extra" analog circuitry results in highest accuracy available. Both the relative and differential nonlinearity specifications are guaranteed to ±1 LSB (maximum). Typical accuracy is 11½ bits.
- Real-time digital monitor port on I/O connector allows external access to the CVT contents.
- The single-ended inputs can accept voltage inputs to ±10.000 V, with an input resistance of 16 kΩ.
- The board operates on the carrier's +5 volt supply only, requiring ≈200 mW of power per channel.
- A buffered +2.500 V reference voltage is supplied to the I/O connector.
- Output data coding is two's complement: 0x800 @ -10.000 V input through 0xFFF @ ≈ -0.005 V; 0x000 @ 0.000 V through 0x7FF @ +9.995 V.



NOTE: The IP Module signal references, transfer and cycle types discussed in this document are explained in detail in the ANSI/VITA 4-1995 IP Module specification.

2.4 Simplified Block Diagram

Figure 2-2 is a simplified block diagram of the ADC128F1.

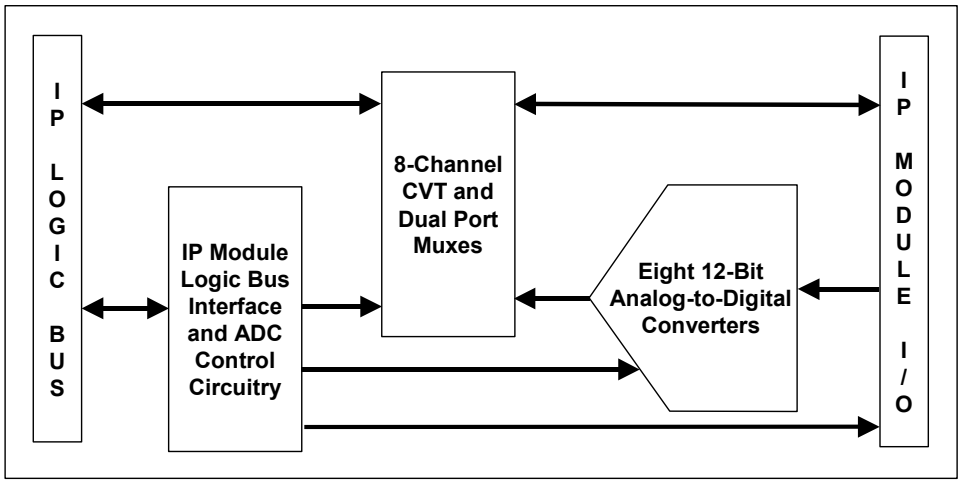


Figure 2-2 ADC128F1 Simplified Block Diagram

2.4.1 Block Descriptions

IP LOGIC BUS INTERFACE AND ADC CONTROL CIRCUITRY

On the left side of the diagram is the IP Logic Bus connector through which all transfers between the IP Module carrier and the ADC128F1's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface and ADC Control Circuitry" contains all of the board-level control/status registers, the ID PROM data, the main ADC sequence engine, the CVT update and access control logic, and IP Module transfer sequence/control and data bus interface logic.

8-CHANNEL CVT AND DUAL PORT MUXES

This block consists of two EPLD devices each implementing support for four analog-to-digital converters including the serial-to-parallel converters and CVTs for each, with a pair of data port multiplexers, one for carrier accesses and one for the data monitor port on the user's I/O connector.

EIGHT, 12-BIT ANALOG-TO-DIGITAL CONVERTERS (ADC)

This block consists of eight separate, tightly-coupled (in time) converters, with their precision voltage reference (not shown) and a buffered reference output. On the right side of the diagram is the ADC128F1 I/O connector, providing eight single-ended inputs to the ADCs, an analog output providing the reference, hardware handshake interface control and status lines, monitor access to any channel's CVT data with select signals and ample ground connections.

2.5 Detailed Block Diagram

Figure 2-3 is a detailed block diagram of the ADC128F1. As in Figure 2-2, the carrier connections are on the left side, lumped by signal groups of data bus (IPDbus), address and control signals (IPAbus and CONTROL, respectively), and power supply connections (not shown).

2.5.1 Block Descriptions

MAIN ENGINE ADC CONTROLLER UPDATE CONTROL

The block labeled "Main Engine ADC Controller Update Control" (top left) provides all of the proper sequencing circuitry for executing conversions, as directed by both software and hardware handshake interfaces, including the control logic to perform data extraction from all eight ADCs, with subsequent serial-to-parallel conversion on that data. The process ends with a simultaneous updating of all eight current value registers (collectively referred to as the CVT).

IP MODULE SEQUENCE CONTROLLER

The block labeled "IP Module Sequence Controller" provides all of the circuitry with responsibilities for:

- Detection of valid I/O and ID transfer operations within their respective fully decoded address ranges, including the support of HOLD cycles when generated by a carrier
- ID PROM data multiplexer and port control signals
- Control/status registers' write and read control signals
- CVT multiplexer and read gate control signals.

CONTROL/STATUS REGISTER

This block consists of a single bit control register with readback, and a 6-bit read gate for monitoring the status of various other important signal states. The "ID PROM Emulator" is the circuitry that presents the proper data patterns to the lower 8-bits of the IPDbus during ID transfers. Emulating the never-changing ID information in this way reduces parts count and costs, and increases system reliability and its associated MTBF value. All of the block elements discussed in this paragraph are contained in the "IP Module Logic Bus Interface and ADC Control Circuitry" block in Figure 2-2.

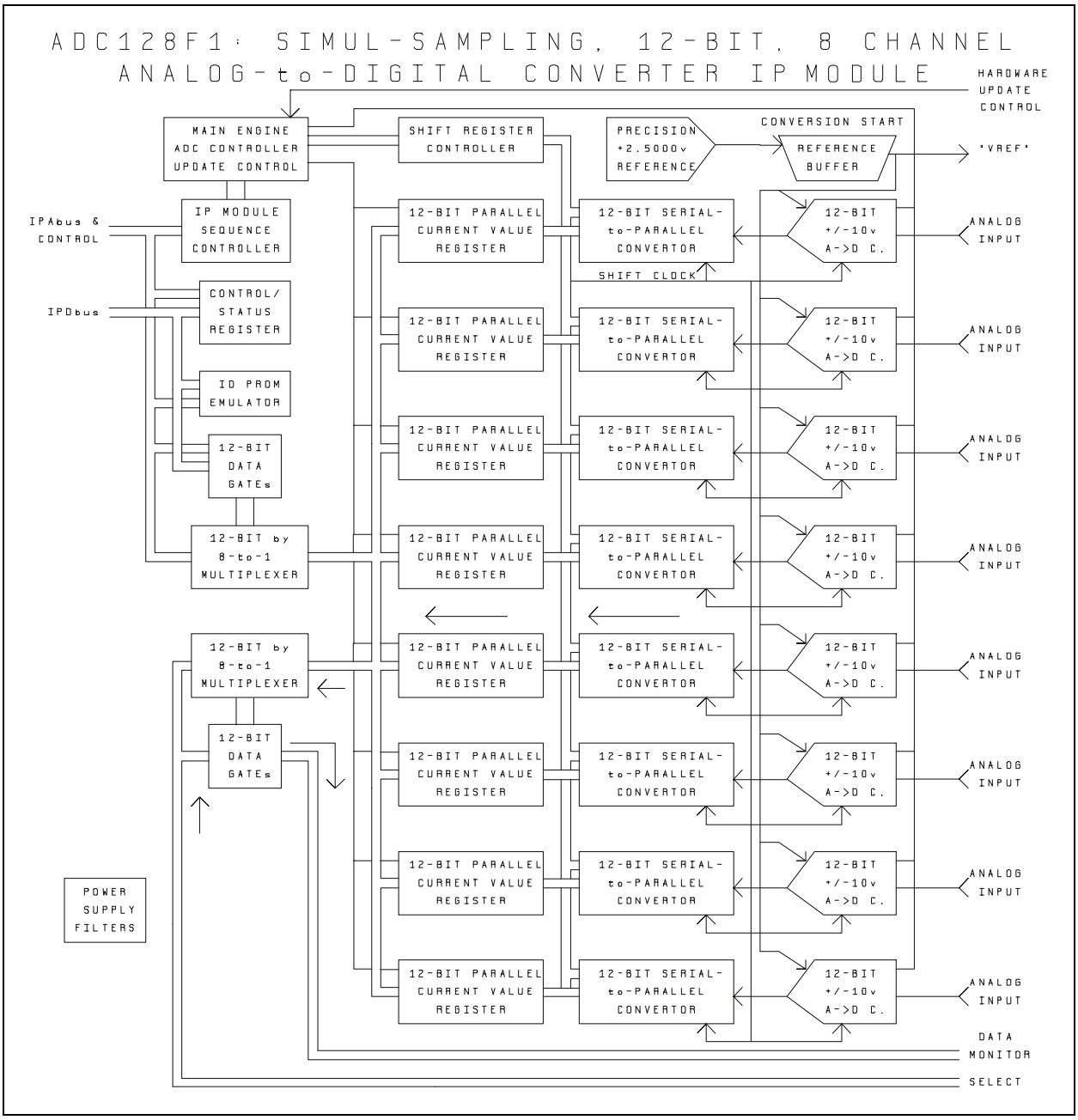


Figure 2-3 ADC128F1 Detailed Block Diagram

SERIAL-TO-PARALLEL CONVERSION

The majority of the circuitry depicted in Figure 2-3 (primarily in the vertical middle) consists of eight sets of serial-to-parallel converters feeding eight separate 12-bit parallel registers that all feed two sets of 12-bit wide, eight-to-one data multiplexers. This circuitry, depicted as “Eight Channel CVT and Dual Port Muxes” in Figure 2-2, is housed within two large EPLDs. The actual sectioning of circuitry is accomplished through support of four ADCs each, with four serial-to-parallel converters, and four 12-bit current value registers feeding two multiplexing port controllers that handle half of the CVT presentation duties. The far right side of Figure 2-3 shows all eight 12-bit ADCs feeding their respective (data) serial-to-parallel converters.

PRECISION 2.500 V REFERENCE

All eight ADCs operate from a single “Precision 2.500 V Reference”, which also is buffered and brought out to pin 18 of the I/O connector as the signal ‘VREF.’

2.6 Architecture

This section explains the rationale behind the architecture of the ADC128F1.

2.6.1 Minimum Software Requirement

Although all I/O interfaces require some software, Systran’s primary goal for all the I/O products is to minimize the software requirement as much as possible. That philosophy has resulted in the development of the architecture being presented.

2.6.2 Resolution Versus Accuracy

The ADC128F1 architecture only provides the resolution that indicates real information.

If you are using a voltmeter that can accurately measure only ±1.999 V (a common 3½ digit display), then no additional information is provided by writing the voltmeter reading as +1.1000 V. It is simply a false statement.

The same is true for analog-to-digital conversion subsystems. If an analog multiplexer, gain stage amplifiers, anti-aliasing filters, and a separate track/hold amplifier are placed on the front-end of a 12-bit ADC, the real accuracy is typically around 9 bits; certainly no where near the 12 bits being provided as a conversion result.

For the sake of maintaining the maximum conversion accuracy possible, the input signals to be converted by the ADC128F1 are fed directly into their respective ADCs with no other circuitry present to increase noise or decrease accuracy.

2.7 General Description

The ADC128F1 has various levels of user-interface capabilities that need to be discussed before a detailed description of this IP Module is undertaken. This top-level presentation explains why certain features and functions exist on the ADC128F1. The functional spectrum of usability includes “power-up and read” through “tight acquisition control.”

2.7.1 Application Descriptions

FREE-RUN A SINGLE ADC128F1

For those applications where it is not important to know exactly when the last analog-to-digital conversion occurred, within a certainty of less than 8.625 µs, use of the ADC128F1 is as simple as applying power and reading the first eight I/O locations as the application requires. All eight channels on each ADC128F1 are tightly coupled (to within a few nanoseconds) and free-run at a sampling and automatic update rate of 927,536 samples per second per ADC128F1 IP Module. The CVT update is automatically blocked during a carrier read of any of the first eight I/O locations. Therefore, if new ADC data is ready to be loaded into the CVT during the 250 ns required to complete the I/O read transfer, then the data being read is already 8.625 [+0.000, -0.250] µs old. If a subsequent read is performed before another 8.625 µs has elapsed, it too will be from the older sampling.



NOTE: When using the ADC128F1 in this mode of operation, there is no certainty that multiple-channel readings taken from a single (or multiple) ADC128F1 board(s) occurred from the same simultaneous sampling of the input signals being converted.

This mode of operation is presented in Appendix B as Section B.2: Free-run A Single ADC128F1.

SINGLE ADC128F1 SNAPSHOT

For those applications that require data to be retrieved from the same instance in time from just a single ADC128F1, a software control signal has been provided to accomplish this minimal-channel snapshot operation.

The only software-control bit on the ADC128F1 is used to deliberately block all subsequent current-value update operations when asserted, even though the ADCs continue to perform conversion operations. This is like a manual override of the automatic update block that occurs during a CVT read operation, as described above. The significant difference in the sampled data in this mode of operation is that all of the data retrieved from the ADC128F1 was derived at the same time (within a few nanoseconds), and has been locked into the CVT by the control bit to allow for subsequent data retrieval at any pace without the fear of losing data due to CVT overwrites. Once the data has been retrieved, the control bit can be negated for subsequent automatic updates to the CVT.

This mode of operation is presented in Appendix B as Section B.3: Single ADC128F1 Snapshot.

MULTI-BOARD LOOSELY-COUPLED SNAPSHOT

For those applications that require data to be retrieved from the same instance in time per ADC128F1 with up to 8.625 μs of uncertainty across multiple ADC128F1 IP Modules, a hardware control line has been provided that functions identically to the software control bit function described above.

At the system level, this configuration can be viewed as being a loosely-coupled simultaneous-sampling data acquisition technique. It is loosely coupled because the uncertainty between the data sets from different ADC128F1 IP Modules is up to 8.625 μs, even though the data from all eight channels on any one ADC128F1 is obtained at the same time (within a few nanoseconds). All of the ADC128F1 IP Modules that are to be loosely-coupled for simul-sampling can be hard-wire controlled from one digital output line (like from a DIO316I* or TRIDO48**). When this “Hardware Update Disable” line is asserted, all subsequent CVT updates are blocked on all connected ADC128F1 IP Modules. Then all the data can be retrieved at any pace and in any sequence with confidence that all data was captured within a 8.625 μs sampling window (preceding the hardware signal assertion). Once all of the data is retrieved, the hardware control line can then be negated to permit subsequent CVT updates on all of the ADC128F1 IP Modules connected together.

This mode of operation is presented in Appendix B as Section B.4: Multi-board Loosely-Coupled Snapshot.

* DIO316I – DIO316I Tristateable 48-Channel Digital I/O IP Module, Systran Corp.
** TRIDO48 – Tristateable 48-Channel Digital Output IP Module, Systran Corp.

MULTI-BOARD TIGHTLY-COUPLED SNAPSHOT

For those applications that require a tightly-coupled, simultaneous sampling of more than eight channels (more than one ADC128F1) that can reside on various carriers, even across various physical chassis, a second hardware control line has been provided for maximum control of the data acquisition process.

By using software timing and a simple digital output signal, or an automatic pulse generation scheme by using either a DUAL16CT or a DUAL32CT IP Module, all channels on all connected ADC128F1 boards can be forced to start their sampling at the same time. This is accomplished by providing a normally negated (low) state on the digital control line connected to the RUN inputs of the ADC128F1's that are coupled together.

When a sample is desired, provide a single high-pulse state between 8.625 µs and 14.000 µs. The uncertainty in the sample acquisition times is primarily a function of when each of the individual ADC128F1 boards "see" the rising edge of the RUN control line, which can be fine-tuned with equal lengths of connecting wire if necessary. The data is available for retrieval from all of the ADCs' CVTs 8.625 µs following the rising edge of the RUN control signal.



NOTE: When RUN is negated (low), the connected ADC128F1 boards are NOT sampling and all of their ADC controllers are reset to a known "zero" state.

This mode of operation is presented in Appendix B as Section B.5: Multi-board Tightly-Coupled Snapshot.

REAL-TIME MONITORING

For those applications that require externally accessible, on-line, real-time monitoring of actual ADC data for calibration purposes, a powerful monitor interface has been incorporated into the design of the ADC128F1. This circuitry easily lends itself to being built into an automatic test circuit for real-time "health" monitoring and pre-event/post-event calibration verification processes. This feature is highlighted in the Appendix B, Section B.6: Real-time Monitoring.

2.8 Detailed Description

The ADC128F1 was developed using VHDL and Synthesis, and targeted to several Altera EPLDs. The design was schematic-captured and integrated to standard interface devices, connectors and discrete components using Innoveda CAE tools.

SIMUL-SAMPLING ADC CONTROLLER

The Simul-Sampling ADC Controller for the ADC128F1, reference designator U1, is physically located to the right of the J1 Logic connector in the assembly drawing presented in Figure 2-4.

SERIAL AND PARALLEL REGISTRATION DEVICE FOR CHANNELS 1 TO 4

The serial and parallel registration device for channels 1 to 4, reference designator U2, is physically located to the right of the J1 Logic connector in Figure 2-4.

SERIAL AND PARALLEL REGISTRATION DEVICE FOR CHANNELS 5 TO 8

The serial and parallel registration device for channels 5 to 8, reference designator U10, is physically located to the left of the J2 I/O connector as shown in the assembly drawing, Figure 2-4. U2 and U10 also contain the dual-port multiplexers with gates for presenting CVT information to both the carrier and the I/O connector.

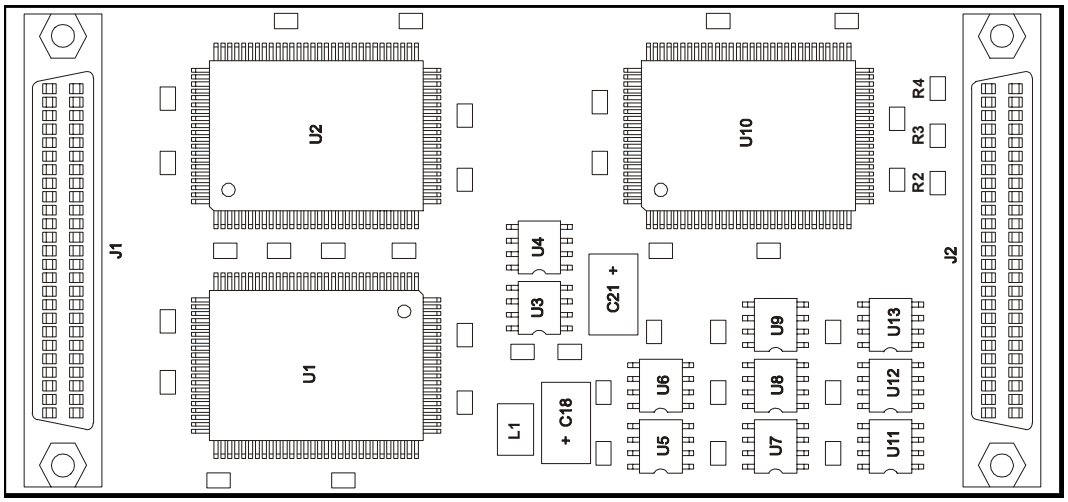


Figure 2-4 ADC128F1 Layout

2.8.1 Digital Components And Their Functions

IP MODULE LOGIC BUS TRANSFERS

All IP Module Logic Bus transfers take place across J1, the IP Module Logic Connector, located on the left side of all block diagrams. This IP Module does not support DMA or Interrupts, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and (for just one bit) writes to the short, ten-location I/O map.

PRIMARY ACTIVITY CONTROLLER

The ADC128F1's primary activity controller is housed within the Simul-Sampling ADC Controller (SADCTRL) EPLD at U1. It is the primary IP Module transfer sequence engine, whose responsibilities include:

- Detection of valid I/O and ID transfer operations within their respective, fully decoded address ranges, including the support of HOLD cycles when generated by a carrier
- ID PROM emulation data pattern generation for ID read transfers; and
- Output-enable control signals for use by the other two EPLDs for the proper gating of CVT information onto the IPDbus during I/O read operations from any of the first eight I/O locations.

ADC OPERATION CONTROL

The other primary set of duties performed within SADCTRL involves controlling all activities related to proper ADC operations. These complex operations are quickly diluted by the subsystem block diagram presented at the bottom of Figure 2-5. Since the ADCs used on the ADC128F1 are small-package, serial-interface devices, the data must be

retrieved in an orderly manner with just the right timing to maintain the highest accuracy possible while performing conversions as fast as possible. This is accomplished by a free-running 69-state sequence engine.

The majority of the time, from counts 00 through 48, the activity on the board is minimized to provide a "quiet" time during the actual conversion process. Once the conversion is complete (after 6 μs), the data is extracted from all eight ADCs simultaneously.

The first four bits are leading zeros and are extracted during the engine's counts of 49 through 52. The next twelve counts shift out real data and are bit-registered by the other two EPLDs as defined by the state of the SFTENA[3:0] (Shift Enable) lines, and as clocked out of the ADCs and into the registers by the SCLK (Shift Clock) signal. This architecture and technical solution permits the ADC128F1 to actually run at 98.78% of the theoretical maximum capacity for the ADCs selected. Also note that SCLK is a gated ICLK that occurs from counts 49 through 64.

ASSERTED LOW CONVERSION START

The last function performed by the Simul-Sampling ADC Controller for the ADC support is the generation of the N_CONVST (asserted low conversion start) signal that resets the ADCs and starts a new conversion on its rising edge. The external control inputs RUN and N_HUPDIS, with the one software control bit N_SUPDIS are used by SADCTRL for state machine control and for the posting of status when required. Additionally, the Simul-Sampling ADC Controller monitors the external control inputs that are used by the other two EPLDs for Monitor Port operations for the sake of posting them as status, when required.

Details concerning the integrated operations between the Simul-Sampling ADC Controller and the ADCs are presented in Chapter 4, PERFORMANCE.

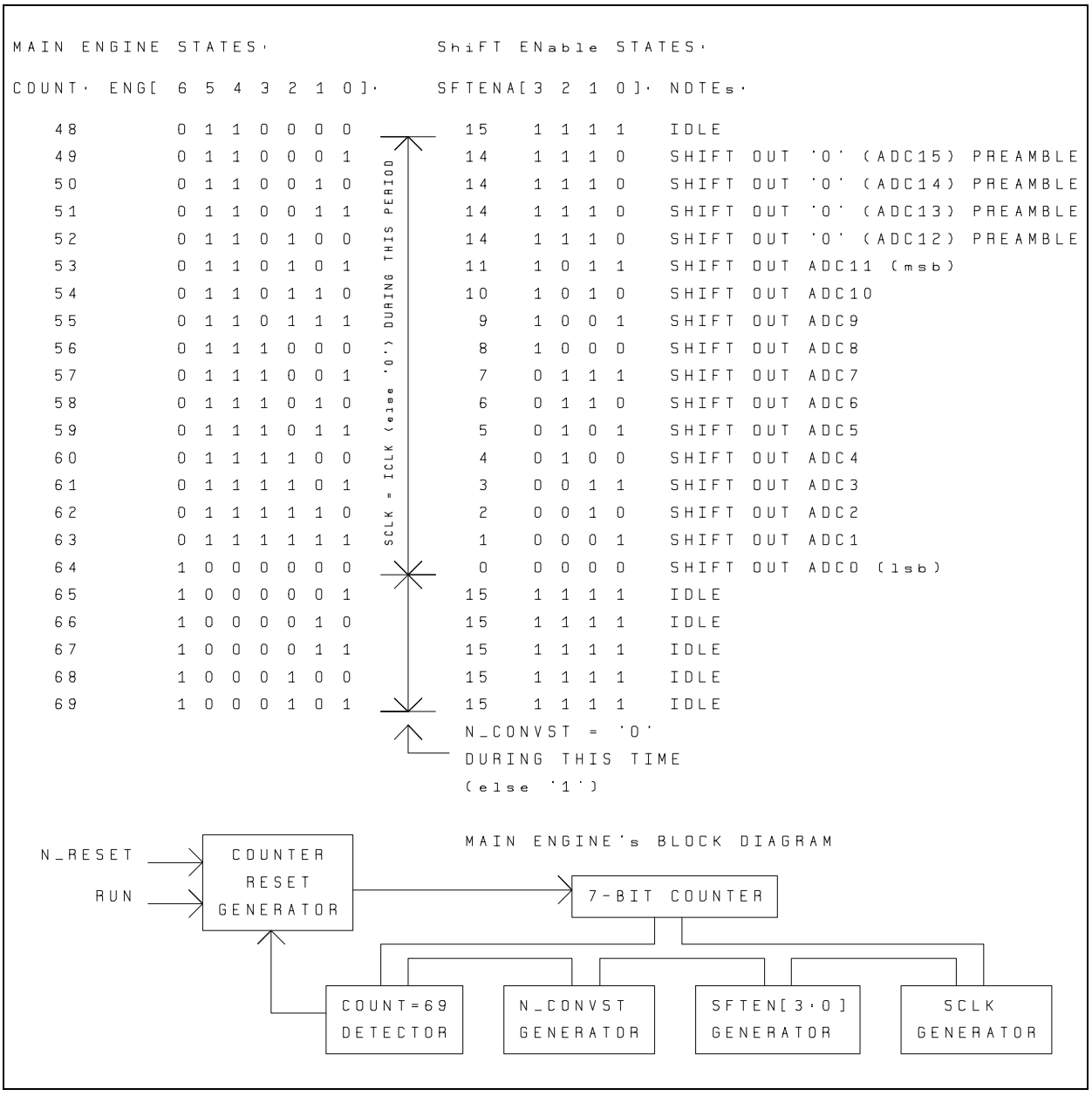


Figure 2-5 ADC128F1 Main Engine Details

REGISTRATION OPERATIONS

The registration operations contained within the REG124 and REG528 EPLDs are identical for all eight channels. As briefly described above and detailed in timing diagrams in Chapter 4, ADC digital data is serially shifted out of the converters on the rising edge of SCLK during engine states 49 through 64, and is bit-registered in descending order by the falling edge of SCLK during engine states 53 through 64. The next rising edge of ICLK that starts engine state 65 performs a complete double-buffer parallel registration of all of the individual 96 data bits captured serially, into the per-channel current value (12-bit) register, collectively called the CVT. This permits the user to gain access to any channel's data at any time regardless of system state without inserting wait states.

The current value registers within both U2 and U10 are connected to a pair of 12-bit wide bi-channel data multiplexers that are each followed by tristate gate/drivers. One multiplexer and its gates are controlled by the Simul-Sampling ADC Controller for driving CVT information towards the carrier during I/O read operations to the first eight locations, and the other is controlled by four control lines coming from the I/O connector for driving CVT information towards the Monitor Port portion of the I/O connector when applicable.

The eight-channel multiplexer that supports the IPDbus is driven by the IPDOE[2:0] and N_IPDOEG signals coming from the Simul-Sampling ADC Controller. Simply, IPDOE[2:0] selects which channel is being accessed and N_IPDOEG asserts low to enable the data onto the IPDbus during the termination cycle of an I/O read from the CVT.

REG124 supplies the data when IPDOE[2:0] = 3 to 0 for channels 4 to 1, respectively. REG528 supplies the data when IPDOE[2:0] = 7 to 4 for channels 8 to 5, respectively.

The eight-channel multiplexer that supports the Current Value Table Output bus (CVTObus) is driven by DATAOE[2:0] and N_DATAOEG signals coming from the I/O connector. Simply stated, DATAOE[2:0] selects which channel is being monitored at the I/O connector and N_DATAOEG is asserted low to enable the data drivers into a low-impedance state. This configuration allows many ADC128F1 IP Modules to have their monitor ports bussed together, if desired.

REG124 supplies the data to the I/O connector (assuming N_DATAOEG is asserted) when IPDOE[2:0] = 3 to 0 for channels 4 to 1, respectively. Also, REG528 supplies the data when IPDOE[2:0] = 7 to 4 for channels 8 to 5, respectively.

The two different multiplexers are completely independent such that the monitor port can access any channel without being affected by a carrier I/O read at any other channel.

MONITOR PORT APPLICATIONS

The following presents some monitor port application hints concerning its use, and potential abuse.

- Any time a single channel at the I/O connector is being continuously monitored with the ADC128F1 free-running, then the data will be updated every 8.625 µs and will change as the signal input to the converter changes. If the application calls for externally capturing the data, as is the case in the sample application in Appendix B, Section B.5, then either the low state or the rising edge of N_CONVST at pin 50 of the I/O connector can be used as the clock for both latches and flipflops since that signal rises only after the CVT has been updated.

- Channel number selections via DATAOE[2:0] and state changes in the output-enable control line N_DATAOEG should not be made asynchronously while free-running the ADC128F1 because the digital "noise" generated during the 6 µs of conversion operations following the rising edge of N_CONVST might couple into the converters and decrease the accuracy of these ADCs. Except for ICLK, there are no other state changes taking place on the board during conversions, except for any accesses by the carrier.
- There are no high-power buffers to drive information out to the monitor port to further decrease the digitally-induced noise on the board. Therefore, if multiple channels need to be monitored, use the external hardware that selects and gathers data to also take control of the board's acquisition sequencing operations; either by asserting N_HUPDIS or negating RUN, to synchronize the data gathering process without affecting the conversion accuracy.

2.8.2 Control

As discussed above, there are several levels of control that can be implemented on the ADC128F1. This subsection is a detailed explanation of those control elements that were explained at the system level in section 2.7: General Description.

N_HUPDIS CONTROL INPUT

The N_HUPDIS control input from pin 49 of the I/O connector is normally negated high by the 10 kΩ resistor designated as R4 located in the upper right-hand corner and just to the left of J2 in Figure 2-4, page 2-8. CVT updates are disabled when this line is asserted low by an external digital source. The conversion processes continue to run, even when this line is asserted, for only the writes to the parallel registers that are the CVT are blocked by the assertion of this control signal.



NOTE: No more than 128 ADC128F1 IP Modules should be controlled from a single digital output from a DIO316I or TRIDO48 to guarantee the low-level assertion state.

RUN CONTROL INPUT

The RUN control input from pin 44 of the I/O connector is normally asserted high by the 10 kΩ resistor designated as R2 located in the upper right-hand corner and just to the left of the I/O connector J2 in Figure 2-4. This control line is typically used for tightly coupling multiple ADC128F1 IP Modules for system level simul-sampling operations. Negating this control line stops all ADC conversion processes and resets the main 69-count engine to a zero state.

N_DATAOEG CONTROL INPUT

The N_DATAOEG control input from pin 48 of the I/O connector is normally negated high by the 10 kΩ resistor designated as R3 located in the upper right-hand corner and just to the left of the I/O connector in Figure 2-4. This control line, when asserted low, places the CVTObus lines in their low-impedance states, providing the CVT information for the channel selected by DATAOE[2:0] to the I/O connector for monitoring purposes. When this input is unconnected or driven high, CVTO[11:0] are in their high-impedance state.

2.8.3 Analog Components and Their Functions

HIGH PERFORMANCE FILTER

All of the analog circuitry runs off of the carrier's digital 5 V supply. It is filtered by a 2.7 mH choke designated as L1, and a pair of 33 µF Tantalum capacitors, designated as C18 and C21, configured as a classic π-filter, designed to provide high performance filtering for the ten analog integrated circuits. This filter is on the bottom edge of the board mid-way between J1 and J2 in Figure 2-4.

ADCS

The eight AD7893AR-10 ADCs, designated as U5 through U9, and U11 through U13 are all 12-bit, ±10 volt single-ended input, serial ADCs with built-in track and hold amplifiers. They have a patented front-end scaling architecture that enables their input voltage range to be four times wider than the power supply voltage that runs the devices. All eight ADCs are controlled by the SADCTRL device (see section 2.8.2 above). The serial data lines SDATA[4:1] for the first four channels provide conversion data to the REG124 device, while SDATA[8:5] supply the same to the REG528 device. The ADCs have an internal reference buffer that permits all eight ADCs to be run from a single reference. All of the ADCs are located in the bottom right quadrant of Figure 2-4.

PRECISION VOLTAGE REFERENCE

All eight ADCs are supplied their precision +2.500 V reference from the AD680JR device located at U4 (in the middle of the board in Figure 2-4). It is based upon band gap technology and is a very low power device, operating on 250 µA maximum. The initial voltage error is 10 mV maximum, with a temperature coefficient of 25 ppm/°C maximum over the operating range of the ADC128F1. It is important to note that the voltage reference requires about 25 ms to stabilize to within ±0.01% of its final output following application of power. It is recommended that this time be accounted for in system designs that may use the ADC128F1 in intermittent power or quick-start-up applications.

REFERENCE MONITOR SIGNAL

The ADC's reference voltage is first buffered by the OP177GS device at U3 (just below U4 in Figure 2-4), before being applied to the converters. This signal, called VREF, is also brought out to pin 18 of the I/O connector for testing purposes.



CAUTION: Under normal operational conditions, pin 18 of the I/O interface cable should have no circuitry attached in order to maintain the high accuracy specifications of this product.



NOTE: A significant effort has been made to provide very careful signal routing in this analog section of the ADC128F1. All of the digital signals run perpendicular to the analog signals on different printed circuit board planes, with complete ground fills on all layers.

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3. INSTALLATION

3.1 Unpack the ADC128F1

The contents of the ADC128F1 shipping packages are listed in Table 3-1:

Table 3-1 Contents of ADC128F1 Shipping Packages

Qty	Description
1	ADC128F1 Printed Circuit Assembly
1	ADC128F1 Hardware Reference Manual *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR-ADC128F1).

3.2 Inspect the ADC128F1

Examine the ADC128F1 to determine if any damage occurred during shipping.

3.3 Install the ADC128F1



NOTE: The ADC128F1 is an Electrostatic Sensitive Device (ESD). Install the ADC128F1 on a good anti-static workbench using good ESD practices to protect the IP Module and its host carrier boards.

The ADC128F1 installation requires the following tools:

Table 3-2 ADC128F1 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

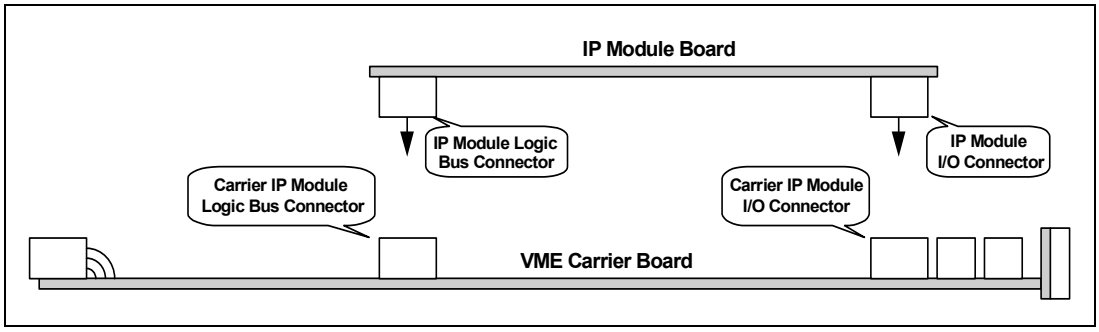


Figure 3-1 Installation of the ADC128F1 on a VME IP Module Carrier Board

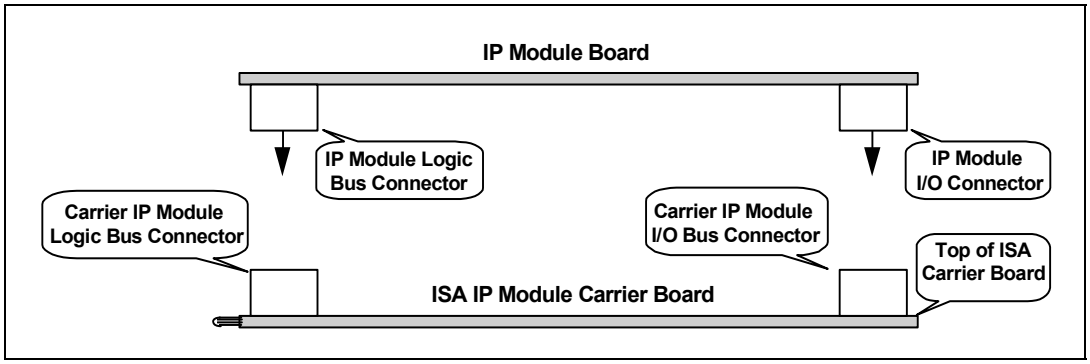


Figure 3-2 Installation of the ADC128F1 on a ISA IP Module Carrier Board

Figure 3-1 shows how the ADC128F1 is installed on a VME IP Module carrier, and Figure 3-2 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board hardware reference manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (∗) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the installation of the ADC128F1 can be made.
3. Remove the ADC128F1 from the shipping package and place it on the ESD bench.
4. Install the ADC128F1 onto the carrier board by applying adequate and equal pressure to the ADC128F1 board at both ends.

*5. Install four M2x5 mm flat head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the ADC128F1 to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signal Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Name
50	N_CONVST
49	N_HUPDIS
48	N_DATAOE0
47	DATAOEG
46	DATAOE1
45	DATAOE2
44	RUN
43	CVT00
42	GND
41	CVT01
40	GND
39	CVT02
38	GND
37	CVT03
36	GND
35	CVT04
34	GND
33	CVT05
32	GND
31	CVT06
30	GND
29	GND
28	GND
27	GND
26	GND
25	CVT07
24	CVT08
23	CVT09
22	CVT010
21	CVT011
20	GND
19	GND
18	VREF
17	GND
16	AIN8
15	GND
14	AIN7
13	GND
12	AIN6
11	GND
10	AIN5
9	GND
8	AIN4
7	GND
6	AIN3
5	GND
4	AIN2
3	GND
2	AIN1
1	GND

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4. PERFORMANCE

4.1 Overview

Performance specifications for the ADC128F1 IP Module fall into two major categories: analog and its subsequent digital representations, and the timing of the actual conversion and data retrieval process. Analog issues are addressed in sections 1 and 2. This section presents information that more clearly depicts the actual conversion process events, various monitor and control techniques with their performance parameters, as well as IP Module access timings as they relate to carrier interface activities.



NOTE: The information provided in this section represents typical measurements, and in no way supplant any related minimum and maximum specifications presented in Appendix A. Where possible, data is tabulated with only one response time (actual) performance figure presented to minimize the length of the presentation.

This section does not have a single system configuration for all of its empirical data measurements. Therefore, as each new set or sets of related data is presented, it is preceded by a short description of the system configuration used to gather the information.

4.2 Hardware Configuration

The following describes the hardware layout used to gather data for sub-section 4.3: Sampler Conversion Time, 4.4: Back-To-Back Conversions, and 4.5: Throughput, as presented in figures 4-1 through 4-11.

Individual wires 1-inch long were connected to ADC128F1 #100 for, and at: SCLK @ U11 pin 4, SDATA1 @ U11 pin 5, SDATA2 @ U7 pin 5, SDATA3 @ U5 pin 5, SDATA4 @ U12 pin 5, SDATA5 @ U8 pin 5, SDATA6 @ U6 pin 5, SDATA7 @ U13 pin5, and SDATA8 @ U9 pin 5.

The IP Module was mounted on a MVME162-01 in slot A using an IP Logic Bus Extender Board (Systran part number BHAS-IPBE1) under the ADC128F1. A 24-inch extender cable was connected to an IP Logic Bus Extender Board where the ICLK signal and ground references were made. A 36-inch I/O cable was connected between the slot A I/O connector on the carrier and a 50-position terminal block where the signal N_CONVST (/CNVRT in the figures) was monitored. All figures were captured using an HP 1 GHz Timing Module, Model 16515A, in a 16500A Logic Analysis System chassis.

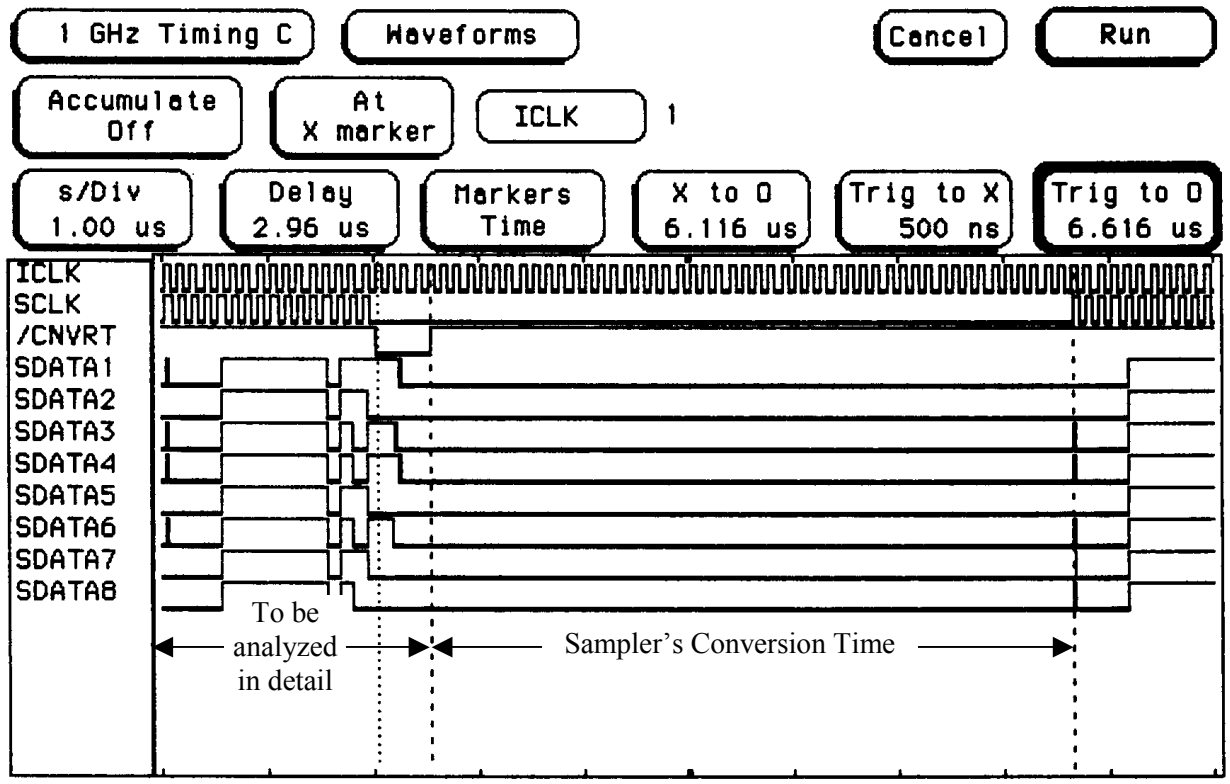


Figure 4-1 Sampler Conversion Time

4.3 Sampler Conversion Time

Data is first available 6 µs after the rising edge of N_CONVST (/CNVRT on the analyzer screen print).

- Measured: 6.116 µs
- Theoretical best: 6.000 µs (48 ICLK clock periods of 125 ns each)

The 116 µs is due to propagation delays through the components.

The area indicated in Figure 4-1 to be analyzed in greater detail is discussed in Figures 4-2 through 4-10.

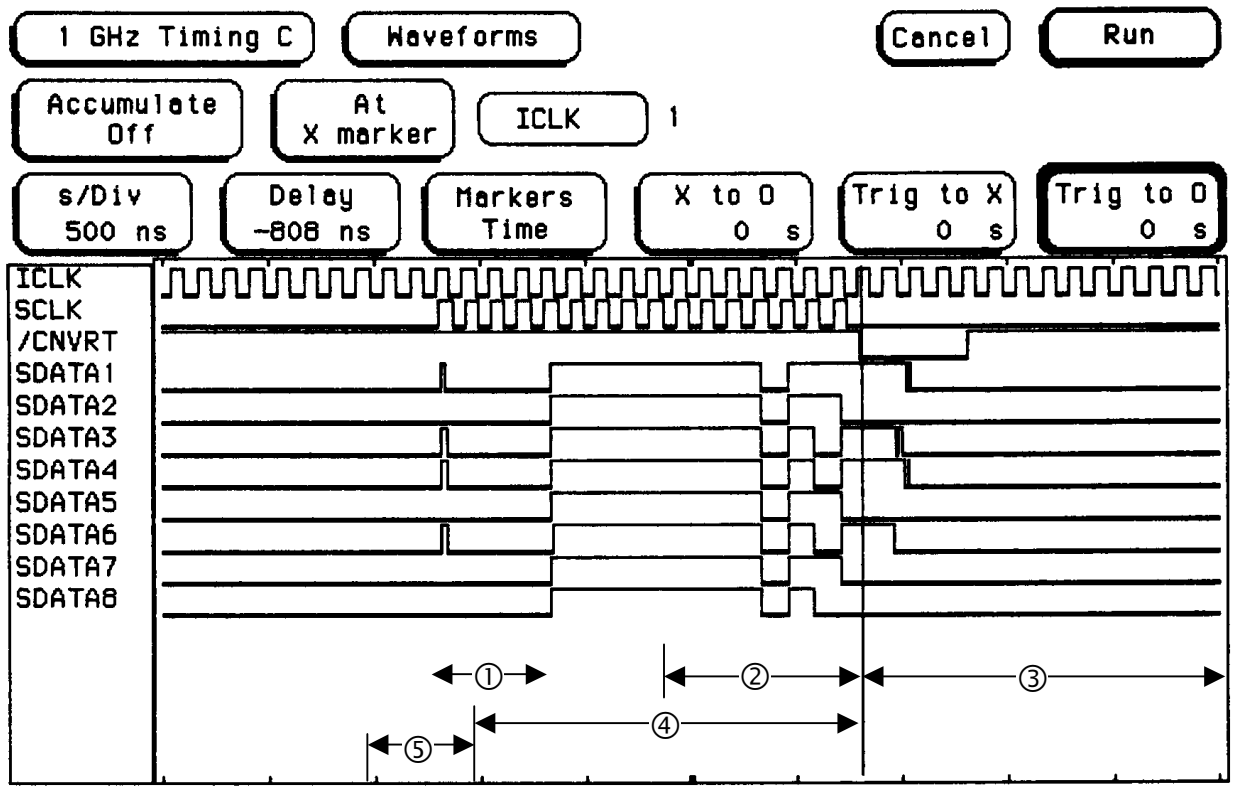


Figure 4-2 Sampling Overview

The overview of the sampling to be analyzed in more detail is discussed using the following analyzer screen prints:

① Figure 4-3
② Figure 4-4
③ Figure 4-5, 4-6
④ Figure 4-7, 4-8
⑤ Figure 4-9, 4-10

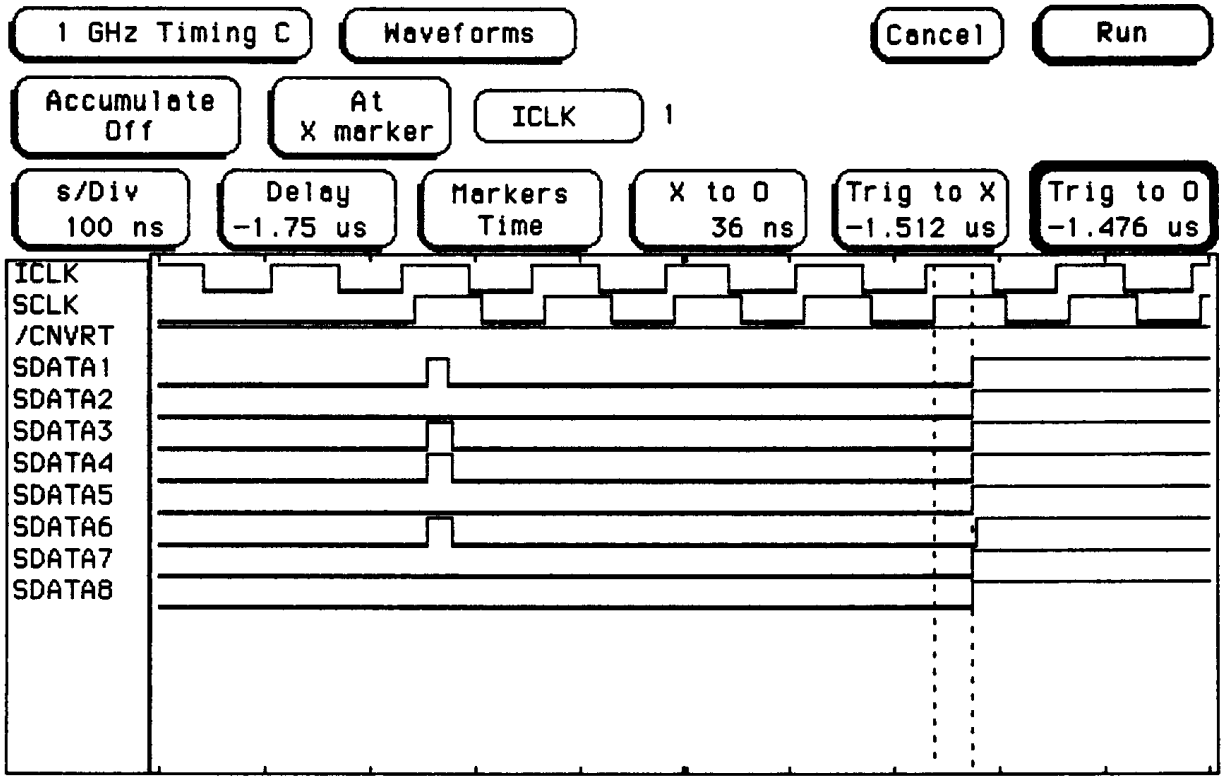


Figure 4-3 Rising Level Data

The rising edge ↑ of SCLK causes the data to be serially shifted out of the converters about 36 ns later.

The first four ↑↓ SCLK pulses shown represent the leading nibble of zero. The rising edge causes the converters to shift out a data bit. The falling edge is the data capture clock edge in the serial-to-parallel conversion process.

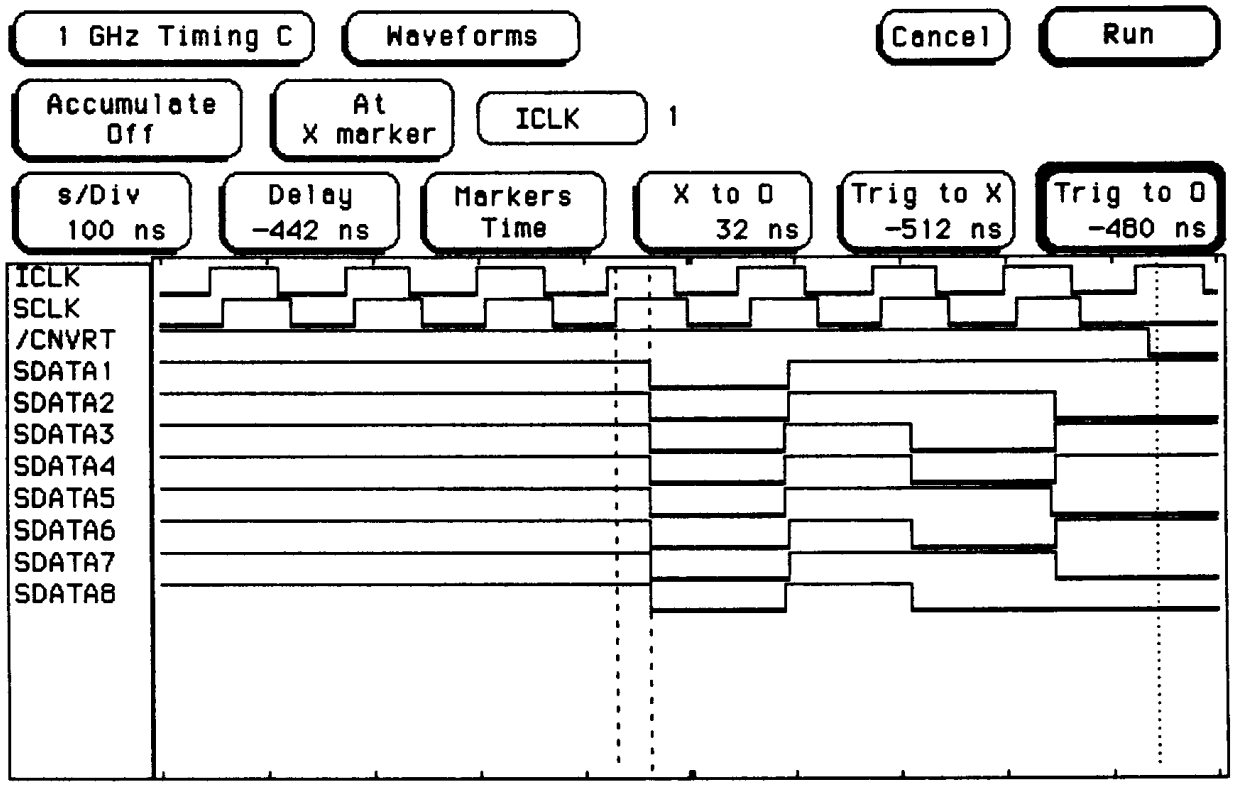


Figure 4-4 Falling Level Data

The rising edge ⎍↑ of SCLK causes data to be serially shifted out of the converters about 32 ns later.

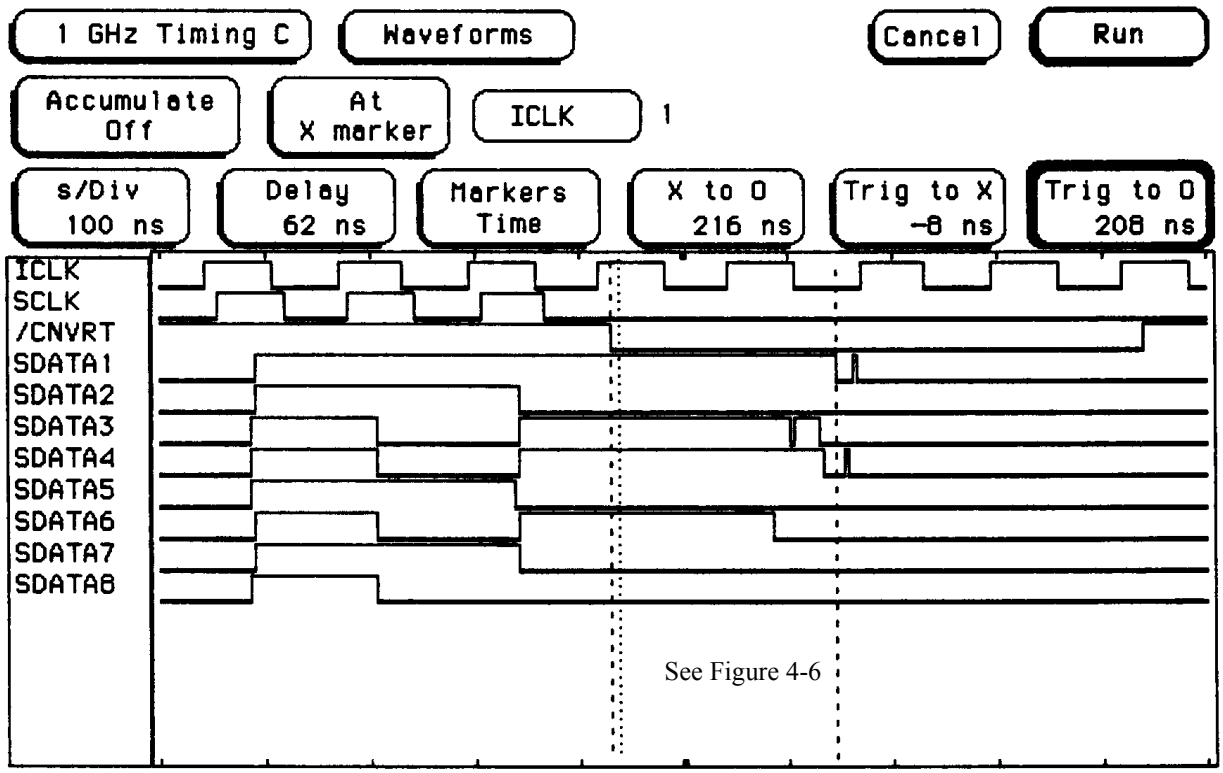


Figure 4-5 Falling Level of N_CONVST

The falling level ↓ of N_CONVST (/CNVRT) on the analyzer screen), until SDATA is a high-impedance state, is between 10 ns and 100 ns according to specification.

This analyzer screen shows about 216 ns because the SDATA lines float low (no pull-up or pull-down resistors to minimize board power requirements).

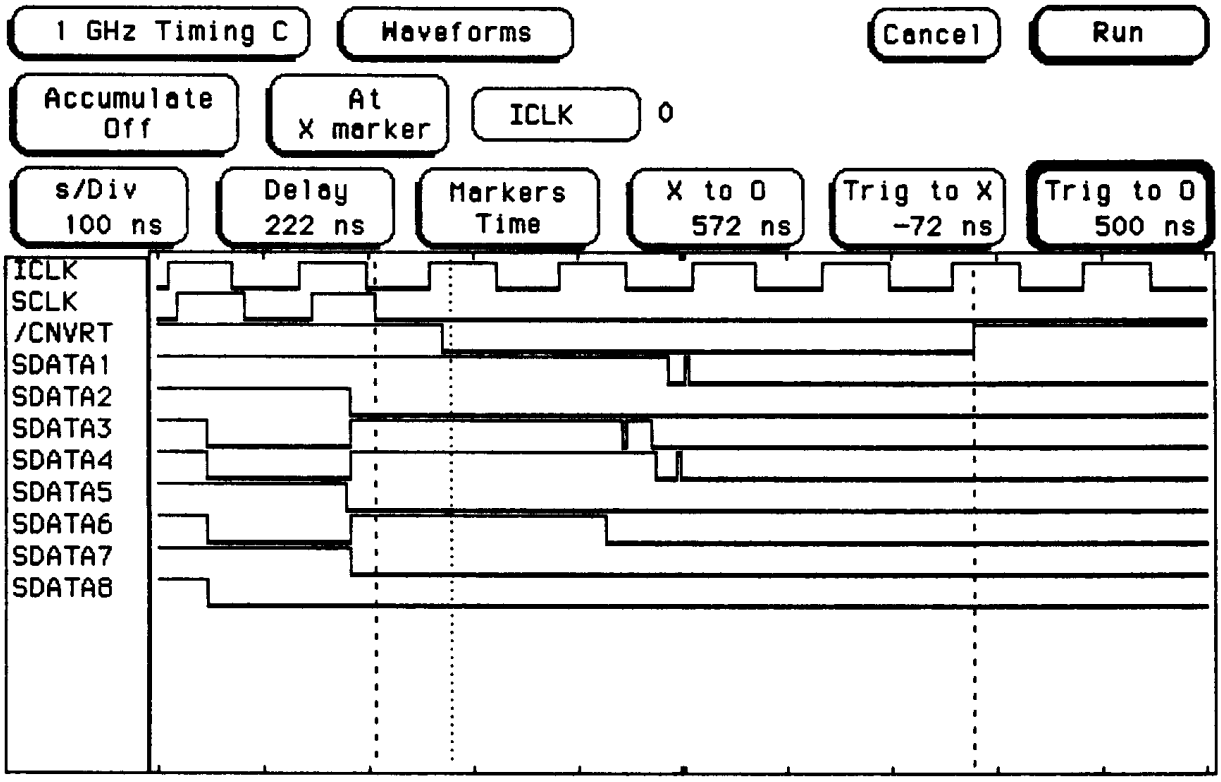


Figure 4-6 Conversion Timing

The elapsed time from the last fall of SCLK to the rising of N_CONVST is supposed to be 600 ns. This requirement is not found in the specification. It is found in the text of ADC's data sheet describing converter details. Portions of this text are quoted below.

"To obtain optimum performance from the part [converter], the read operation should not occur during the conversion* or within 600 ns prior to the next conversion."

And elsewhere:

"Once the read operation has taken place, a further 600 ns should be allowed before the next rising edge of N_CONVST to optimize the settling of the track/hold amplifier before the next conversion is initiated."

Also:

"The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 1.5 µs."

"At the end of a conversion (6 µs after the rising edge of N_CONVST) the part returns to tracking mode."

The results in Figure 4-6 of 572 ns violate the text requirement by 28 ns. However, 2.510 µs** of tracking exceeds 1.5 µs specification by nearly 60%.

* 6.000 µs from ↓ N_CONVST until the first ↑ SCLK

** See Figure 4-7.

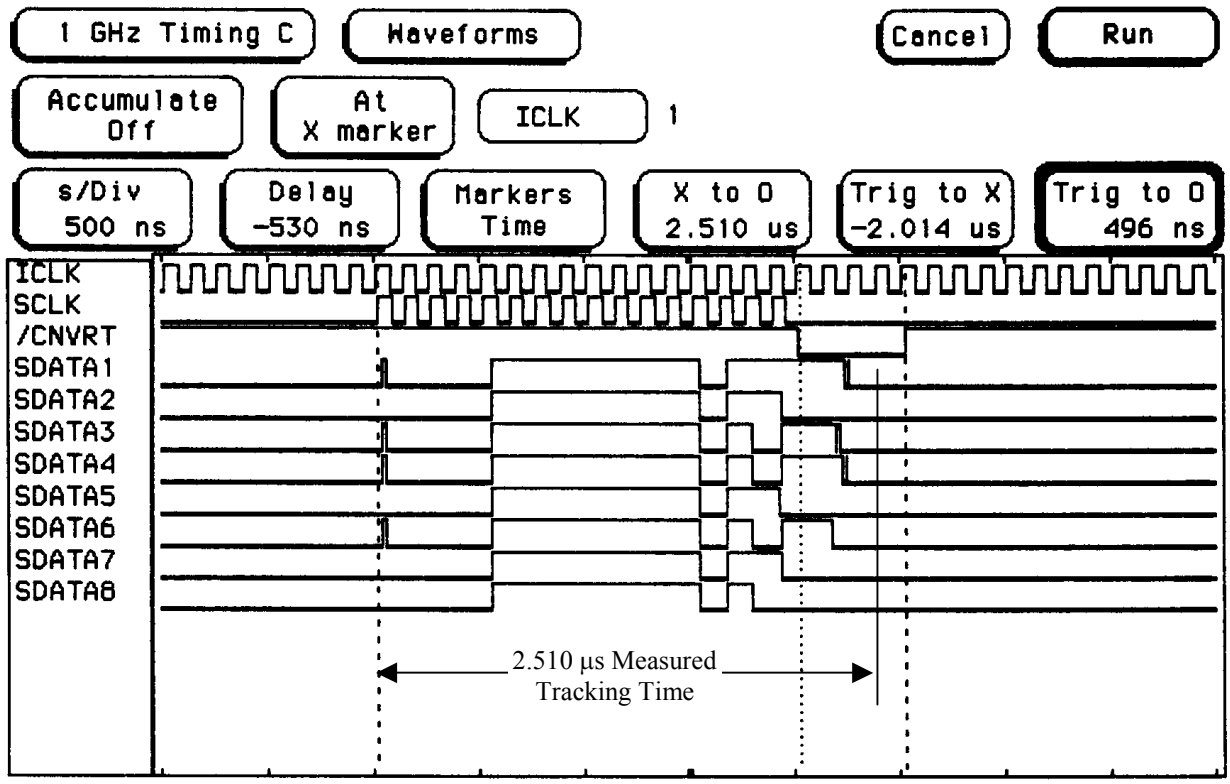


Figure 4-7 Measured Tracking Time

1.5 µs minimum to track to 12-bit accuracy. (See notes for Figure 4-6).

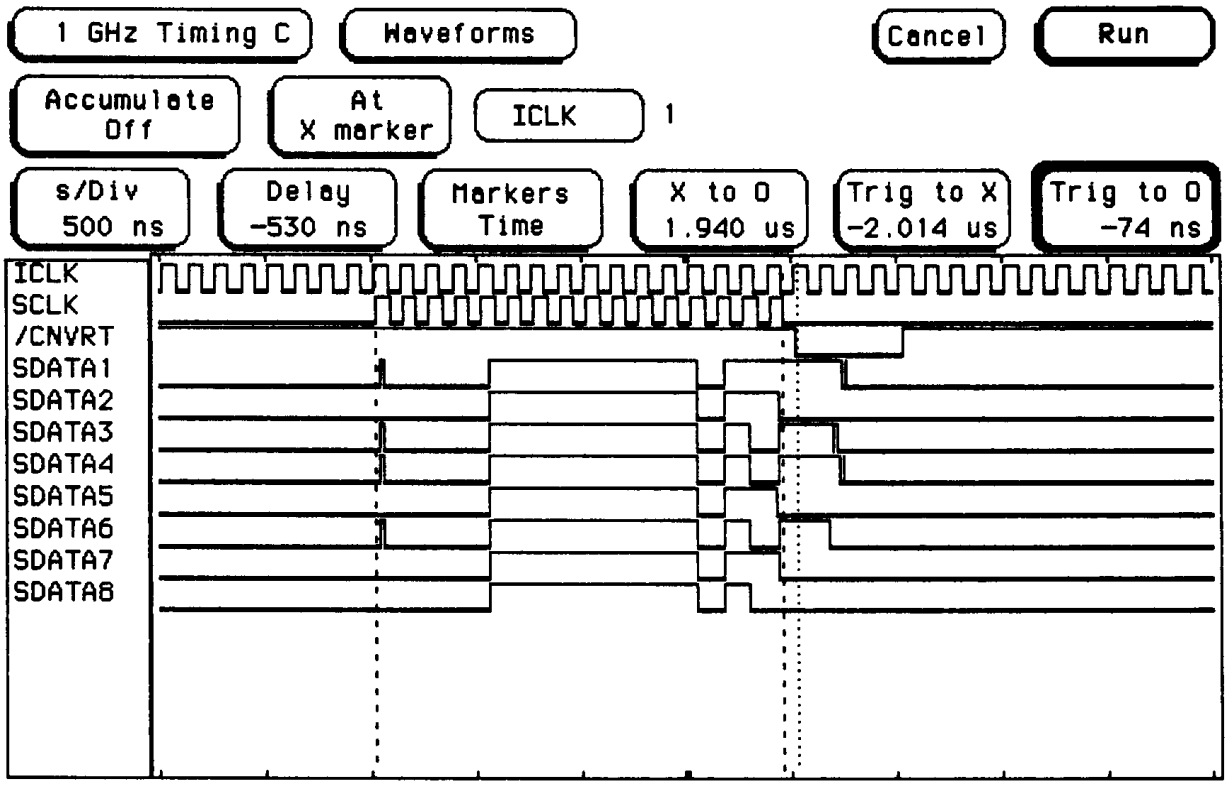


Figure 4-8 Read Operation

Start of read (first ↑ SCLK) to end of read (last ↓ SCLK) = 1.940 µs

1.92 µs is the fastest read time per specification.

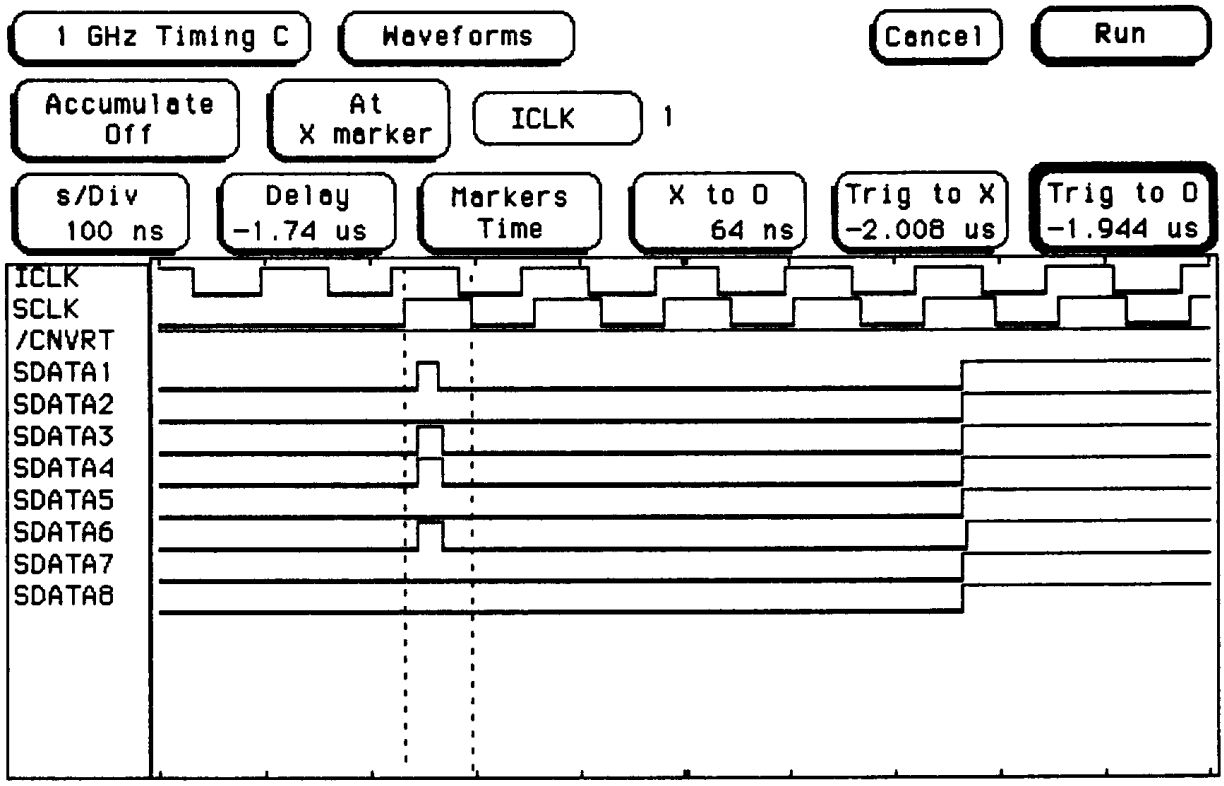


Figure 4-9 SCLK High Pulse Width

SCLK high pulse width = 64 ns measured.
SCLK high pulse width = 60 ns minimum per specification.

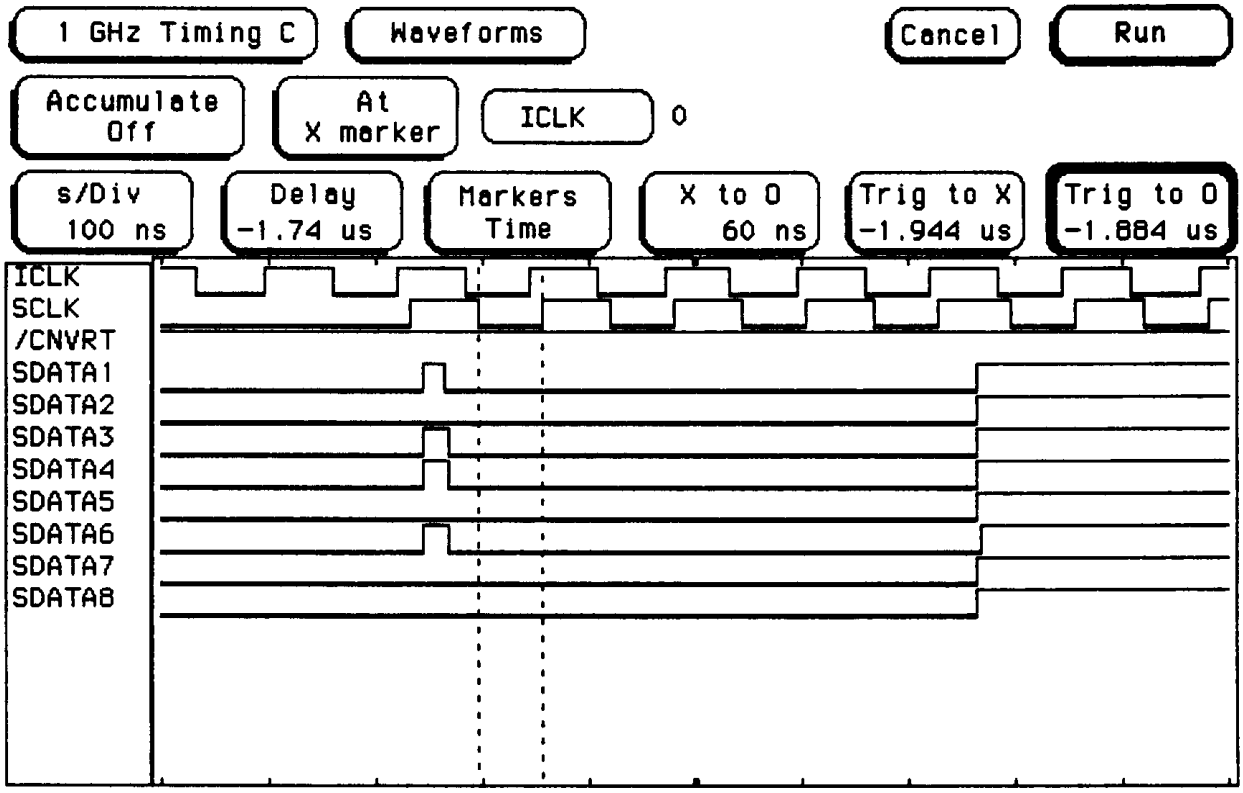


Figure 4-10 SCLK Low Pulse Width

SCLK low pulse width = 60 ns measured.
SCLK low pulse width = 30 ns minimum per specification.

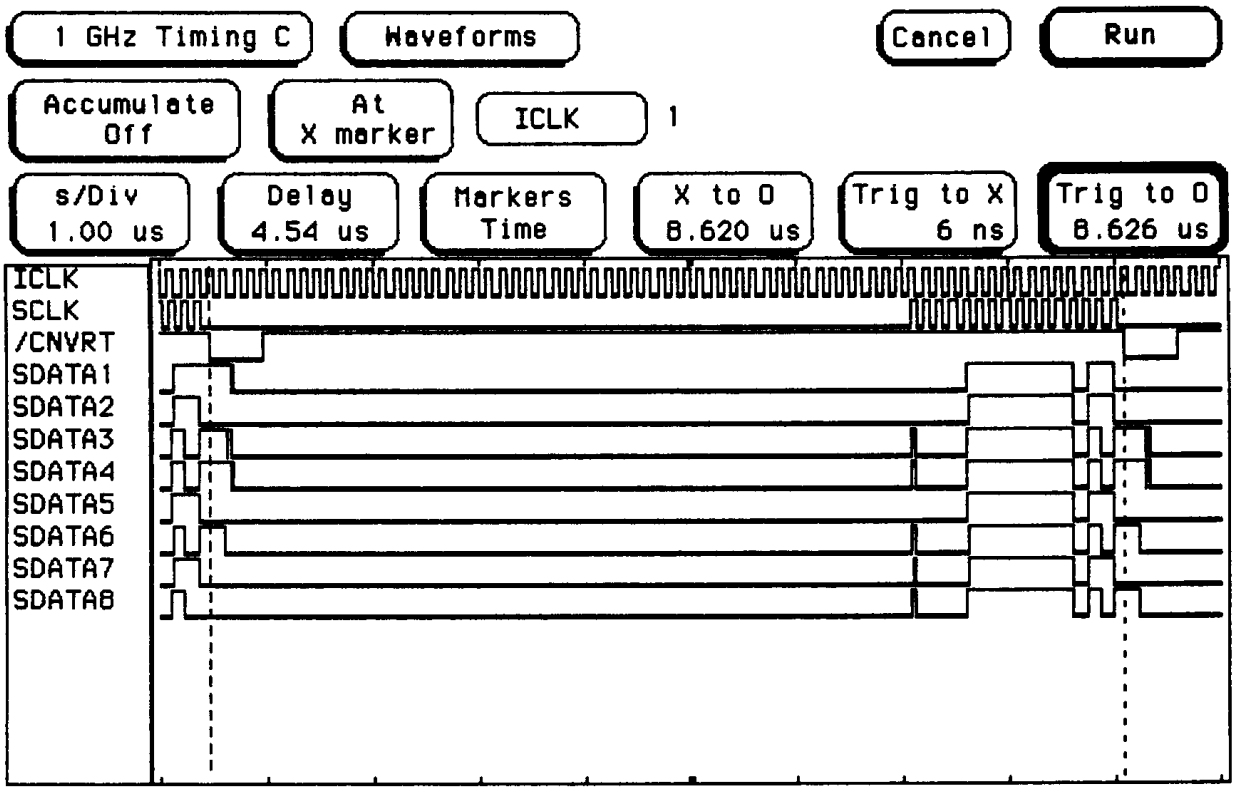


Figure 4-11 Back-to-Back Conversions

4.4 Back-to-Back Conversions

Back-to-back conversions were measured at 8.62 µs. There is a measurement resolution error of 5 ns out of 8.620 ns for 0.58% accuracy.

The theoretical value is 8.625 µs ⇒ 115,942.0289 samples per second.

4.5 Throughput

Minimum possible throughput time of 8.52 µs ⇒117,370.892 samples per second per specification.

This means this IP Module card is running at 98.78% of the theoretical maximum.

4.6 Carrier Accesses

This short presentation provides typical timing parameters as they pertain to carrier accesses. The IP Module was mounted on a MVME162-01 in slot A using an IP Module Logic Bus Extender Board (Systran part number BHAS-IPBE1) under the ADC128F1. A 24-inch extender cable was connected to an IP Module Logic Bus Breakout Board where all of the connections to signals and ground references were made. All figures were captured using an HP 1 GHz Timing Module Model 16515A in a 16500A Logic Analysis System chassis. There are four transfer types represented in Table 4-1: An I/O write (@ IPA=08, to assert N_SUPDIS), an I/O read from that same control register, an I/O read from the current value table (for the third ADC @ IPA=02), and an ID read (from IPA=01). The two different I/O reads are presented since their timings for the providing of information to the IPDbus is significantly different due to different data sources.

Table 4-1 Transfer Types

Transfer Type & Where	ICLK Until:	Time (ns)
I/O Write IPA = 0x08	N_ACK	10
	N_ACK	10
I/O Read IPA = 0x08	N_ACK	10
	IPDbus	13
	N_ACK	10
I/O Read IPA = 0x01	N_ACK	10
	IPDbus	14
	N_ACK	9
I/O Read IPA = 0x02	N_ACK	10
	IPDbus	22
	N_ACK	9

4.6.1 I/O Write @ IPA = 0x08

Figure 4-12 presents one of the eleven captured timing diagrams used for the development of Table 4-1. This figure presents the I/O write transfer, with the time markers highlighting the time it takes the ADC128F1 to assert N_ACK. Note that the IPDbus has 10 kΩ pull-up resistors on every line, and that it takes a long time for the data lines to float high after being driven low by either the carrier (as in this figure) or by the ADC128F1(or any other) IP Module. This is why there is no timing parameter presented that defines the time it takes for the ADC128F1 IP Module to release (transfer from low-impedance to high-impedance states) the IPDbus.

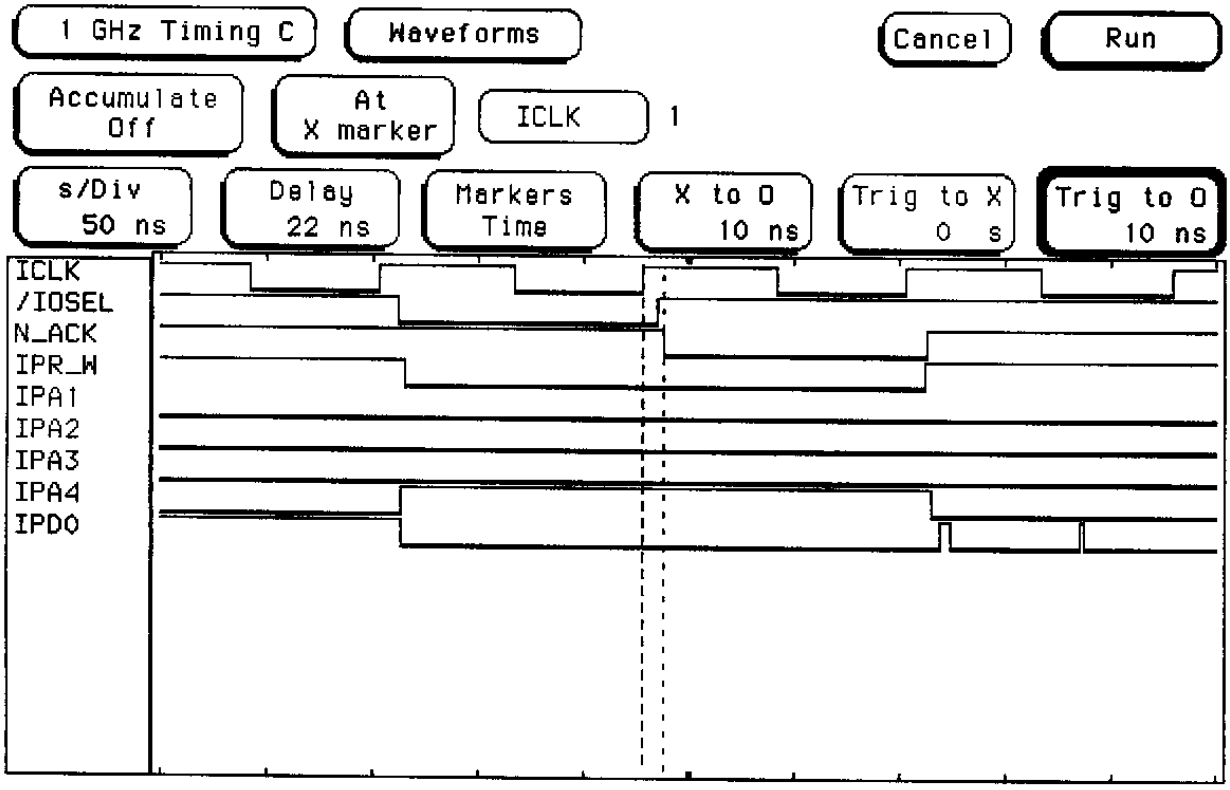


Figure 4-12 I/O Write @ IPA = 0x08

4.7 Monitor Timing

This short subsection presents three figures that depict how the hardware-update-disable control line affects the monitor port. In addition, timing data is provided that can be used for data logging/capturing of CVT information from the monitor port.

The system configuration for this subsection consists of a TRIDO48 mounted in slot D, and a single ADC128F1 mounted on slot A of a MVME162-01 board, using an IP Module Logic Bus Extender board under the ADC128F1. A 24-inch extender cable was connected to an IP Module Logic Bus Breakout Board where the ICLK signal and ground references were made. A pair of 36-inch I/O cables was connected between the slot A I/O connector on the carrier and a 50-position terminal block where the rest of the I/O signals were monitored, and between the Slot D I/O connector and another 50-position terminal block.

All figures were captured using an HP 1 GHz Timing Module Model 16515A in a 16500A Logic Analysis System chassis. The N_DATAOEG and DATAOE[2:0] inputs were all grounded for the continual presentation of the first ADC's current value on the monitor outputs. The analog inputs were all left open. The lowest nibble of the CVT for the first ADC was the only information captured, and it represents open-input noise. One digital output from the TRIDO48 was connected to the N_HUPDIS (HUPDIS in the figures) input to the ADC128F1.

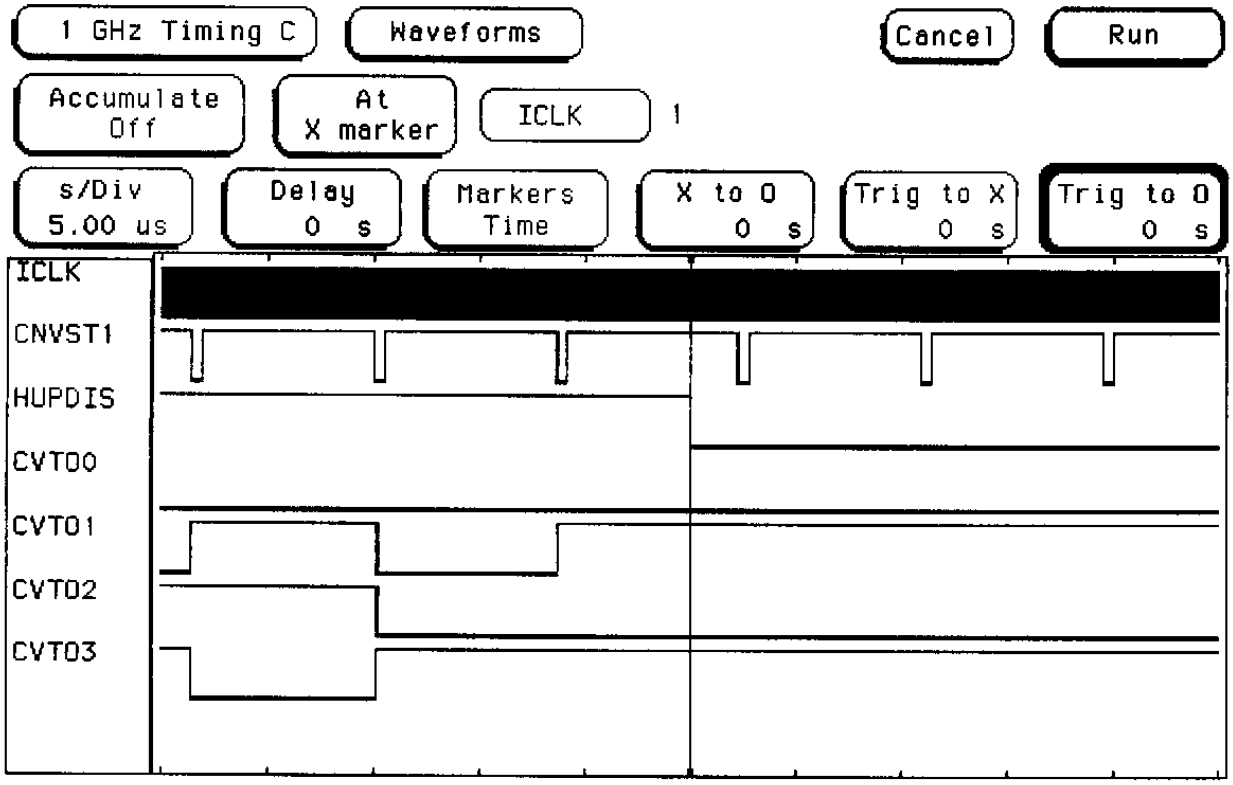


Figure 4-13 Hardware Update Disable (HUPDIS) Assertion

4.7.1 Hardware Update Disable Assertion

Figure 4-13 presents the before and after results of the assertion of N_HUPDIS. Note that to the left of the time marker, CVTO data is changing. After N_HUPDIS is asserted low, the current value table is no longer updated, as evidenced by the non-changing CVTO signals.

4.7.2 Hardware Update Disable Negation

Figure 4-14 presents the before and after results of the negation of N_HUPDIS. Note that to the left of the time marker, CVTO data is constant. After N_HUPDIS is negated high, the current value table is again being updated, as evidenced by the changing CVTO signals.

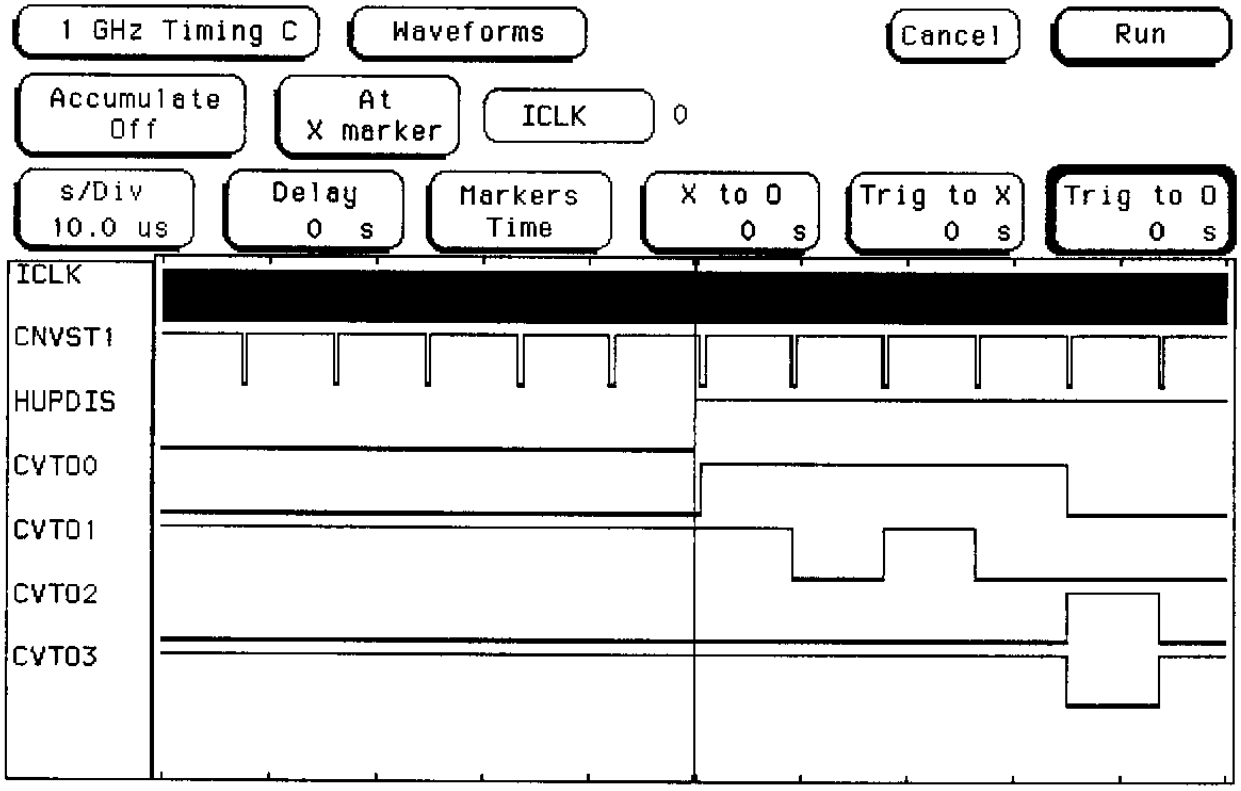


Figure 4-14 Hardware Update Disable (HUPDIS) Negation

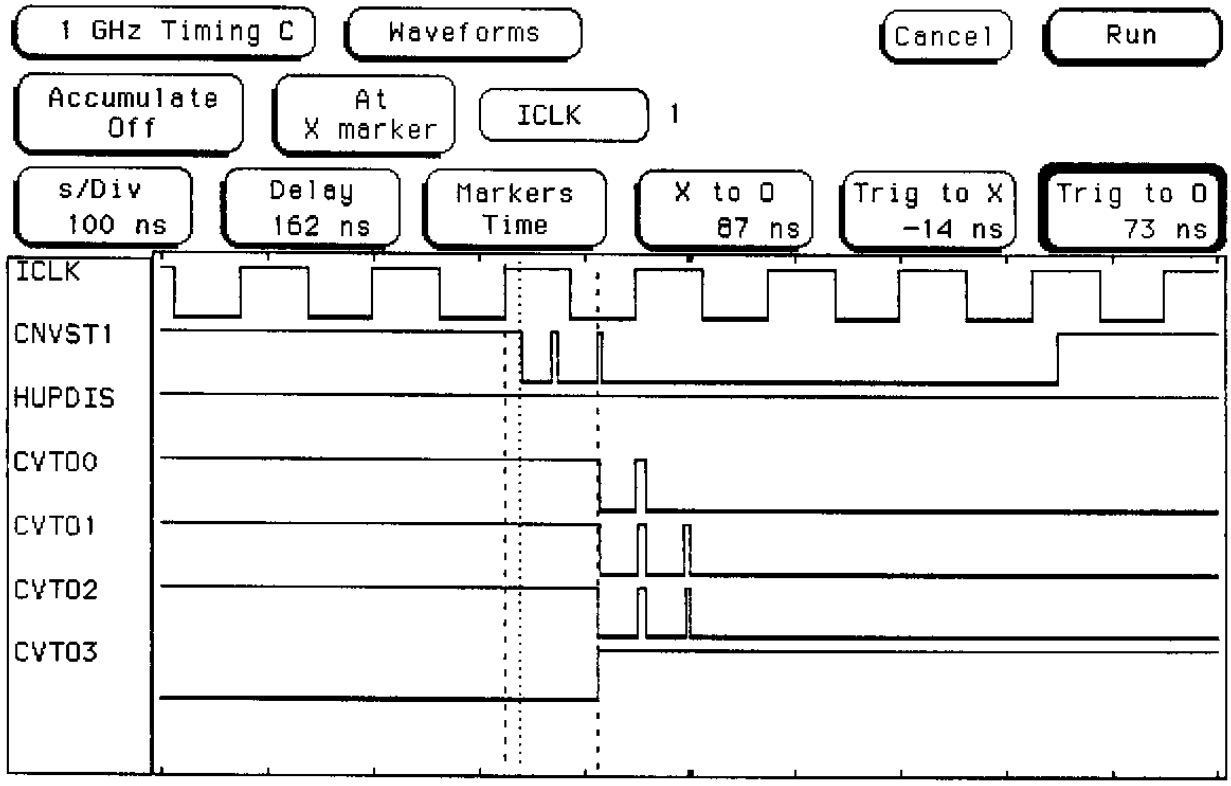


Figure 4-15 CVTO Update Timing

4.7.3 CVTO Update Timing

Figure 4-15 presents the timing relationship between the current value table updates and the N_CONVST (CNVST1 in the diagrams). The rising edge of ICLK preceding all other changes actually causes them. It takes about 16 ns for the N_CONVST signal to first reach its low state, while it takes about 87 ns for the changes in the current value table to propagate through the multiplexers and port drivers following their changes that occurred as a result of the actual update process. The ringing on the cables is due to the long, highly-capacitive ribbon cables that are being used unterminated.

LOW PULSE WIDTH OF N_CONVST

The low pulse width of the N_CONVST signal deserves a short discussion. In various places throughout this document it has been stated that the N_CONVST pulse is 625 ns in width because it is generated from the main ADC engine during five of its machine states. Actually, the pulse width measures to be about 524 ns in width, slightly longer than four ICLK periods. N_CONVST is driven low during machine states 65, 66, 67, 68, and 69. However, as soon as the engine detects the 69th state, it asynchronously resets its main counter to all zeros. The N_CONVST signal is decoded to be in a high state except for the five cited above. From this one can deduce that it takes the logic a total of 24 ns to detect that the engine is at count 69, reset it to count 00, detect that N_CONVST should then be high, and then drive the signal high.

As can be seen in Figure 4-15, the low state of N_CONVST can be used as a gate for latching the CVTO[11:0] data lines, or its rising edge can be used for registration of the data (into FlipFlops). The falling edge should not be used due to potential cable ringing, except as a signal that the data is about to change.

4.8 Multi-Board Timing

This last subsection presents some typical timing parameters for a pair of ADC128F1 IP Modules running, first asynchronously, and then in tightly-coupled mode. As presented in other sections of this document, there are several different ways of using the ADC128F1 individually and coupled with others.

The system configuration for this last group of figures, as described earlier, involves the use of the MVME162-01 as the carrier. On it are placed an ADC128F1 #100 in slot A, an ADC128F1 #108 in slot B, and a TRIDO48 in slot D. The ADC128F1 in slot A is on a bus extender, with a bus breakout board connected at the end of a 24-inch extender cable. All three boards have 50-position terminal blocks connected to their respective carrier I/O connectors via 72-inch ribbon cables.

The same logic state analysis equipment cited earlier was used for this test. The ICLK signal and ground references were obtained via connections to the bus breakout board. The N_CONVST signal from ADC128F1 #100 in slot A (labeled CNVST1 in the figures) was obtained from pin 50 of the I/O terminal block for this board.

The N_CONVST signal from ADC128F1 #108 in slot B (labeled CNVST2 in the figures) was obtained from pin 50 of the I/O terminal block for this board. The digital output from the TRIDO48 (port 0 bit 0) at its pin 8 on its I/O terminal block was connected to pin 44 of both of the I/O terminal blocks for the ADC128F1 IP Modules. This last connection is to the RUN inputs to the ADC128F1's, and was monitored by the analyzer at the TRIDO48's I/O terminal block.

The TRIDO48 was configured so that its outputs would be in a high-impedance state on power-up. This permits both of the ADC128F1 IP Modules to power-up acquiring data in free-run mode because their respective, pulled-high, RUN inputs present a high state to their respective ADC control engines.

4.8.1 ADC128F1s in Free-run Mode

Figure 4-16 presents a typical "free-run" picture of two ADC128F1's. Even though all of the samples from any one ADC128F1 are all captured simultaneously, the laws of probability indicate that, by chance, there will be a difference between boards. This figure indicates that the samples obtained from the ADC128F1 in slot A are leading those from slot B by a skew of 3.241 μs. The reported time from the first occurrence of N_CONVST to the second one on the second ADC128F1 of 8.620 μs is incorrect by 5 ns due to the large sampling window being used.

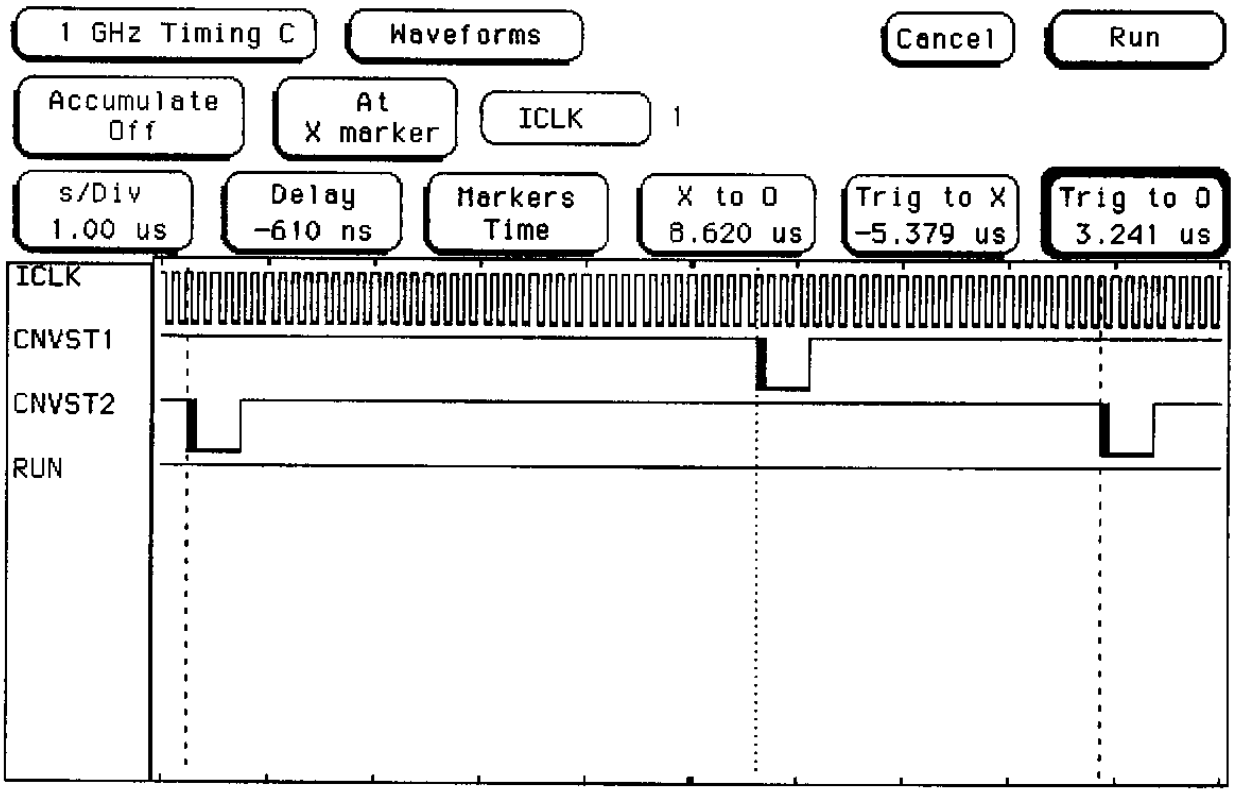


Figure 4-16 ADC128F1s in Free-run Mode

Following the above sampling, the TRIDO48 was configured so that the RUN signal could be manipulated. After enabling its output drivers, the RUN line was negated low (The TRIDO48's data registers default to zeros on power-up). This, of course, had the effect of stopping both of the ADC128F1's sampling process and resetting their ADC engines to a count of zero.

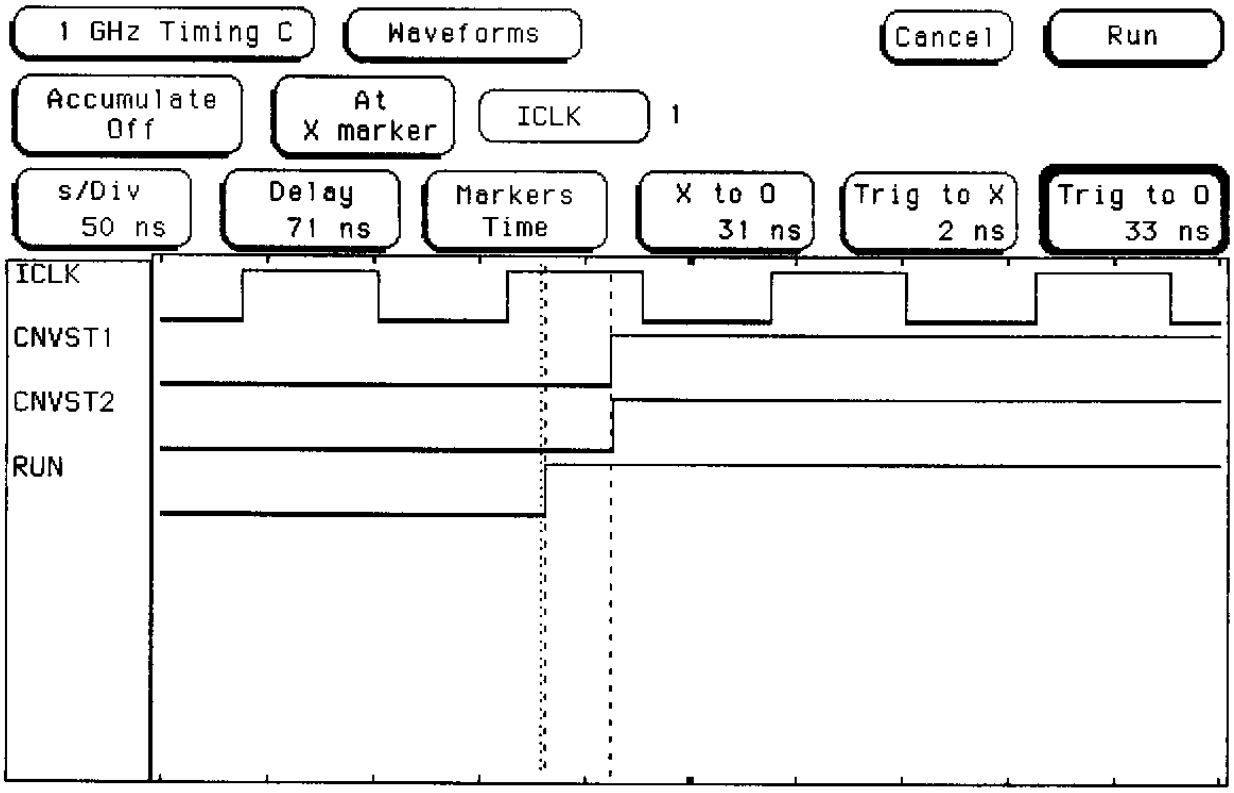


Figure 4-17 ADC128F1s Starting in Tightly Coupled Mode

4.8.2 ADC128F1s in Tightly-Coupled Mode

Figure 4-17 presents what takes place when RUN is asserted on tightly-coupled ADC128F1's. At 31 ns following the rising edge of RUN, both ADC128F1's are driving their respective N_CONVST signals high, simul-sampling 16 channels (in this example). Assuming approximately 5 ns/meter of propagation delay through the I/O cables, then slightly more than 18 ns (of the 31 ns measured) is non-logic delay timing.

Various samples were taken following the start event depicted in Figure 4-17. After ten minutes of a constantly asserted RUN signal, both ADC128F1 boards were still tightly coupled, as depicted in Figure 4-18. This zero-skew is primarily due to the fact that both ADC128F1's were operating on the same carrier. It is possible that there may be some skew between boards that reside on different carriers within the same chassis, or in different chassis running in tightly-coupled mode. The worst-case skew in such a system configuration is 125 ns, the period of one ADC engine clock cycle with respect to the rising edge of RUN from one ADC128F1 to another.

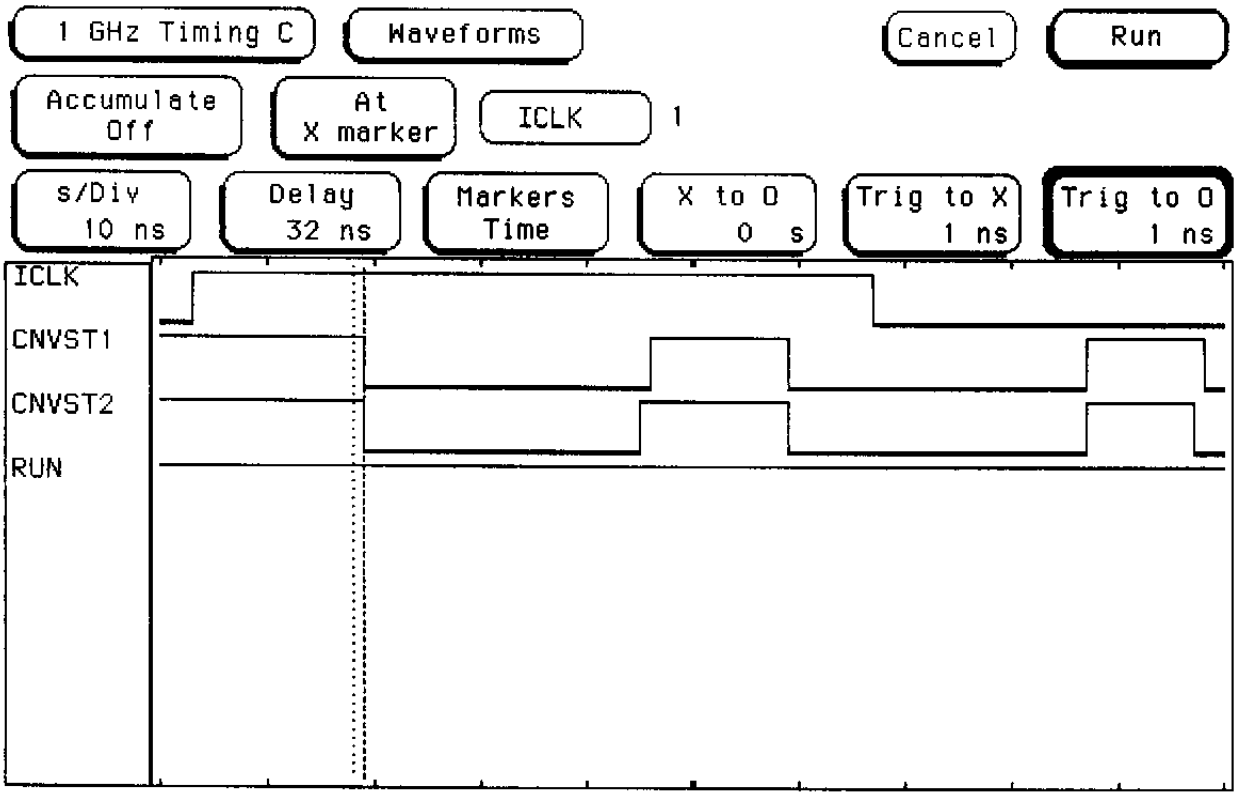


Figure 4-18 After 10 Minutes in Tightly-Coupled Mode

4.8.3 Termination of Tightly-Coupled Mode

This section concludes with the termination of a tightly-coupled mode sampling period. Normally, tightly-coupled operations would only run from a pulse that exists from 8.625 µs to 14.000 µs. This demonstration has shown what happens for boards operating on the same carrier for ten minutes. They are still tightly-coupled (zero skew) having only been synchronized by the rising edge of RUN.

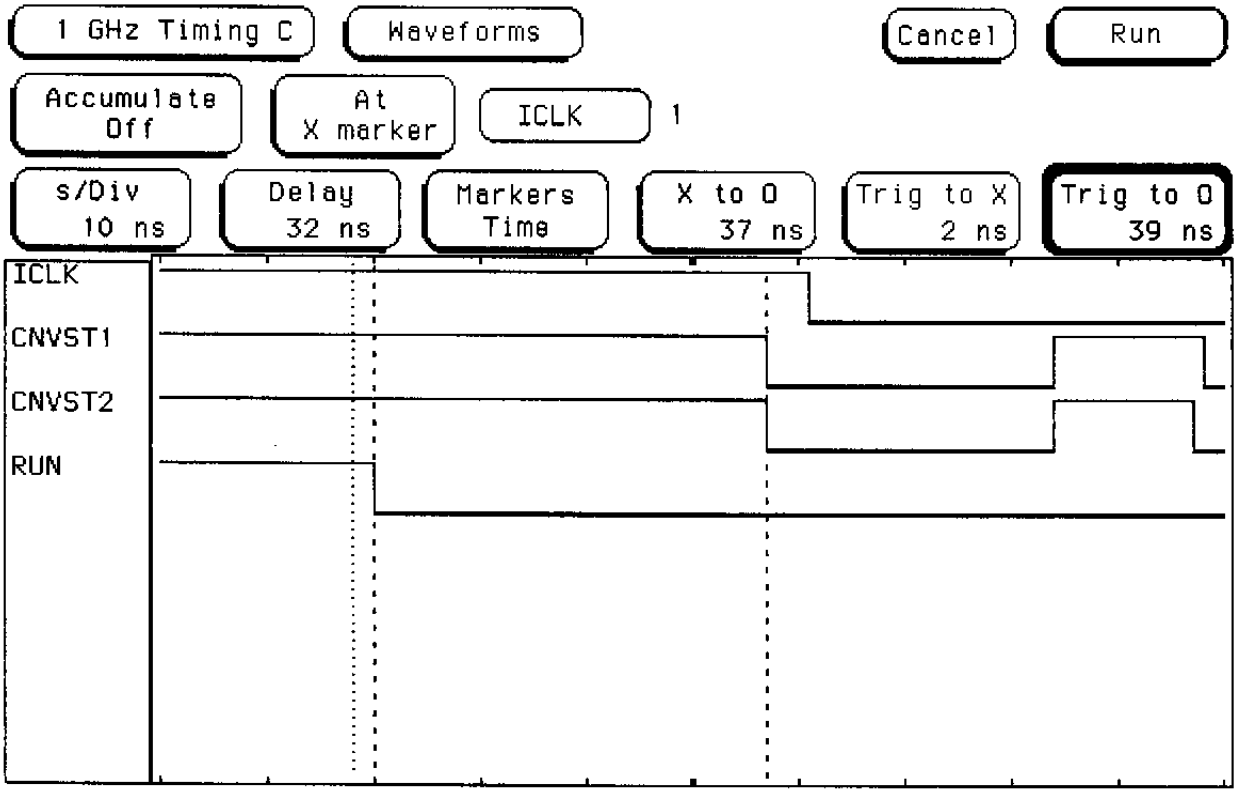


Figure 4-19 Termination of Tightly-Coupled Mode

Figure 4-19 presents the termination of a tightly-coupled sampling, regardless of the RUN signal's pulse width. It took 37 ns from the falling edge of RUN to terminate the sampling operations on both ADC128F1 IP Modules. Remember that much of this delay is due to cable propagation delay time.

As these examples may have implied, the timing accuracy that can be achieved when running multiple ADC128F1 IP Modules in tightly-coupled mode is quite high. It can be fine-tuned by varying the length of wire that feeds each individual ADC128F1's RUN input line if higher accuracy is needed than that which occurs by random cabling of these boards.

APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements	1.800 inches x 3.900 inches x 0.303 inches (above board), 4.572 cm x 9.906 cm x 0.770 cm (Note: 0.127 inches (0.323 cm) max. component height)
Weight	1.012 oz., 28.68 grams
Board thickness	0.062 inches, 0.157 cm, nominally, (4 layer)

PROTOCOL

Clock rate	8 MHz
Wait cycles	None on any transfer types
Hold cycles	Supported on all valid transfer types
Address decoding	Complete (no partial)
I/O transfers	
Writes	8-bit or 16-bit
Reads	16-bit
I/O locations	Ten, 16-bit
ADC Data Values	8
Control	1
Status	1
Maximum read/write rate	4 MTransfers/second, sustained
Zero fills on IPD[15:12]	None
ID transfers	8-bit or 16-bit read (only) data presented on IPD[7:0] No Zero-fills on IPD[15:8] 12 bytes, including CRC
Systran's manufacturer's ID	0x45, E ASCII
ADC128F1 model number	0x6A, j ASCII
CRC value	0x6A
Maximum read rate	4 MTransfers/second, sustained
Memory transfers	Not supported
Interrupt Vector transfers	Not supported
Interrupt requests	None generated
DMA activity	Not supported
Acknowledgment on unsupported transfer attempts	None generated

Memory read and write
Interrupt read
ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

- N_SUPDIS, software update disable, is set to allow CVT updates to occur.
- All ADCs converting with disposition of data into CVT, assuming no hardware connections at N_HUPDIS and RUN, or N_HUPDIS is negated high and RUN is asserted high.
- No accesses permitted or acknowledged during RESET.

- Data is not accurate to specification until after 25 ms following application of power.

POWER REQUIREMENTS

Power:..... +5 Vdc @ 327 mA (typical, no monitor loads, open inputs)
+12 Vdc @ 0 A
-12 Vdc @ 0 A

PERFORMANCE CHARACTERISTICS

Timing .....Refer to Chapter 4, PERFORMANCE
Analog (ADCs)
- Signal-to-Noise Ratio ..... 70 dB min. for 10 KHz Sine wave input
- Total Harmonic Distortion .....-80 dB max. for 10 KHz Sine wave input
- Peak Harmonic Distortion .....-80 dB max. for 10 KHz Sine wave input
- Intermodulation Distortion .....-80 dB max. for both 2nd and 3rd order terms (Fa = 9 KHz and Fb = 9.5 KHz)
- Minimum Resolution .....12 bits with no missing codes, guaranteed
- Relative Accuracy .....±½ LSB (typical), ±1 LSB (maximum)
- Differential Nonlinearity.....±1 LSB (typical and maximum)
- Positive Full-Scale Error.....±1 ½ LSB (typical), ±3 LSB (maximum)
- Bipolar Zero (offset) Error.....±2 LSB (typical), ±4 LSB (maximum)
- Negative Full-Scale Error .....±1 ½ LSB (typical), ±3 LSB (maximum)
- Input Voltage Range.....±10 V
- Input Resistance.....33 kΩ (typical), 16 kΩ (minimum), internally buffered to present a benign, non-changing input current to user's source.
- Reference Input Current.....1 µA (maximum) due to internal buffering within the ADC.
- 1 LSB .....20 V/4096 ≈ 4.88 mV

Analog (Reference)
- Output Voltage .....+2.500, ±0.010 V (maximum, over temperature)
- Output Voltage Drift .....10 ppm/°C (typical)
  25 ppm/°C (maximum)
  4.375 mV (maximum, over temperature)
- Output Settling Time.....25 ms to within 250 µV of final value after application of power

ABSOLUTE MAXIMUM RATINGS:

Supply voltage with respect to ground:
- Minimum ..... -0.3 V
- Maximum..... +7.0 V

Analog Inputs .....±17.0 V



CAUTION: Stresses above those listed may cause permanent damage to the components on the ADC128F1. Operating the ADC128F1 beyond the recommended ratings for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS:

Supply voltage.....+5.00 V, ±0.25 V
Logic Interface .....ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): .....0°C to +70°C
Temperature (no bias, storage): .....-40°C to +125°C
Humidity (Non-condensing): .....5% to 95%
Vibration (Operating): .....10 G's RMS, 10 to 55 Hz, random
Shock (Operating): .....50 G's maximum, any axis
Altitude (Operating): .....10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MIL-HDBK-217F .....661,203 hours
Bellcore 332, Issue 6 .....2,060,237 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

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APPENDIX B

TYPICAL APPLICATIONS

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B.1 Overview

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the ADC128F1 IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Submission constitutes permission to publish without additional consent or compensation, and the author reserves the right to modify submissions to provide for more generic appeal, when necessary. Help advance the level of technology by participating with the Systran team while simultaneously publishing your ideas.

As an example of customer input, note the title "ADC128F1 = EASY POWER" at the top of Figure B-1. It was provided by a customer who was impressed with how powerful the ADC128F1 is in solving his data acquisition problem while being so easy to use. As described in the following application notes, the ADC128F1 can do far more than the average analog-to-digital conversion product.

Additional information about the various modes of operation presented in this section can be found in Chapter 2, paragraph 2.4, General Description.

B.2 Free-Run A Single ADC128F1

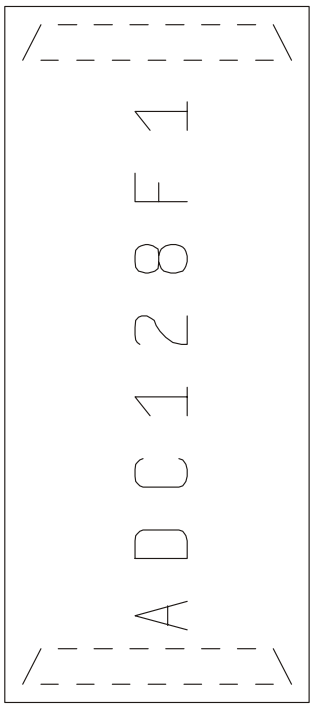
This mode of operation, when applicable for the system requirements, is the simplest usage of the ADC128F1. The ADC128F1 defaults to this mode on power-up with only analog signal inputs and ground connections attached at the I/O connector. Data is retrieved from the CVT (any of the first eight I/O locations) when it is needed. The data retrieved from the CVT is never older than 8.625 μs.

If the conversion task involves emulating differential-input sampling by using two separate channels of the ADC128F1 and subtracting their difference, it is recommended this mode not be used unless the inputs are VERY low in frequency. Because there is a high probability that the data retrieved from the "+" channel and from the "-" channel will be from different samplings. If this is a problem, then use one of the modes of operation described in the following applications.

ADC128F1 = "EASY POWER"

FREE-RUN A SINGLE ADC128F1

@ CARRIER:
LOGIC CONNECTION



I/O CONNECTIONS

I/O CONNECTIONS:

PIN:	FUNCTION:
2	ANALOG INPUT, CHANNEL 1
4	ANALOG INPUT, CHANNEL 2
6	ANALOG INPUT, CHANNEL 3
8	ANALOG INPUT, CHANNEL 4
10	ANALOG INPUT, CHANNEL 5
12	ANALOG INPUT, CHANNEL 6
14	ANALOG INPUT, CHANNEL 7
16	ANALOG INPUT, CHANNEL 8
*	GROUND PLANE
44	RUN - LEAVE OPEN OR TIE HIGH
48	N_DATAOEG - LEAVE OPEN OR TIE HIGH
49	N_HUPDIS - LEAVE OPEN OR TIE HIGH

* IT IS RECOMMENDED THAT ALL AVAILABLE GROUND PLANE CONNECTIONS BE USED: PINS 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 20, 26, 27, 28, 29, 30, 32, 34, 36, 38, 40, & 42.

It is also recommended that the DATOE[2:0] inputs, which normally float, be tied high or low if they are not going to be used. DATOE[2:0] = pins 45, 46, & 47, respectively.

Typical Usage:

After application of power, start reading data from first eight I/O locations.

For example, if the ADC128F1 is in slot 'A' of a Motorola MVME162-XX, using the 162Bug Debugger Command "MD FFF58000" will result in the display of all eight channels' data being presented on the Monitor's screen. Note that the twelve bits (three nibbles) of significant data is preceded by a leading most significant nibble = "F", which is due to the fact that the IPDbus has pull-up resistors on every line on the carrier, and that the ADC128F1 does not drive IPD[15:12].

Figure B-1 Free-run A Single ADC128F1

B.3 Single ADC128F1 Snapshot

For applications that must have multiple-channel data from exactly the same sampling, the mode of operation presented in Figure B-2 is recommended. This is advisable when any or all of the ADCs on any one ADC128F1 are converting high frequency signals or want to maintain valid phase relationships between signals for post-capture data analysis or process control. As in the mode of operation presented in section B.2 above, the ADC128F1 powers-up free-running.

The snapshot is taken by blocking CVT updates by resetting the one software control bit, "N_SUPDIS", the Software Update Disable function. The ADCs continue to free-run but the data in the CVT is frozen for subsequent data retrieval at any pace in any sequence. When the data has been retrieved, the N_SUPDIS bit should be set to allow for subsequent CVT updates. As in application B.2, the data retrieved from the CVT is never older than 8.625 μs. The difference is that all of the data retrieved is from exactly the same sampling. The uncertainty between channels of actual sampling times is to within a few nanoseconds, which should be sufficient for most applications.

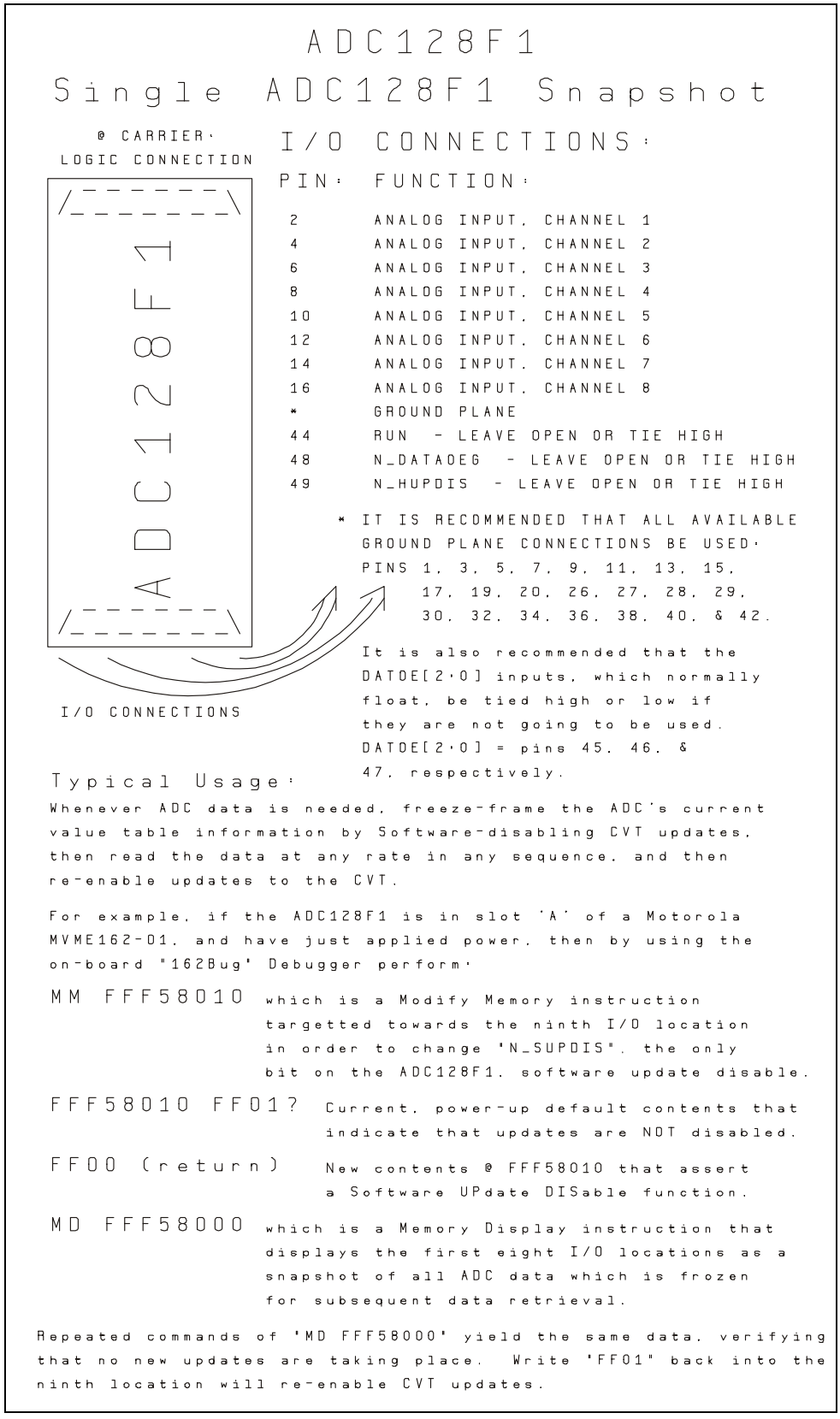


Figure B-2 Single ADC128F1 Snapshot

B.4 Multi-Board Loosely-Coupled Snapshot

For applications that want to capture data from multiple ADC128F1's at about the same time, the mode of operation presented in Figure B-3 is recommended. Basically, it is a multi-board, hardware-controlled version of the snapshot technique presented in application B.3. All of the ADC128F1 boards to be coupled together have their I/O Connector pin 49 wired together, and are controlled by a single digital output line from another IP Module (like the TRIDO48 or DIO316I).

There are no special timing constraints for this mode of operation. As before, the snapshot is taken by blocking CVT updates. Instead of asserting the N_SUPDIS bit for a single ADC128F1, the user asserts "low" the digital line that is connected to the ADC128F1's N_HUPDIS control input, the Hardware Update Disable function. The ADCs continue to free-run, but the data in the CVTs is frozen for subsequent data retrieval at any pace in any sequence. When the data has been retrieved, and to allow for subsequent CVT updates, the N_HUPDIS control line should be negated by setting high the digital output line controlling the multiple ADC128F1 IP Modules. As in all previous applications, the data retrieved from the multiple CVTs is never older than 8.625 µs. This means that the uncertainty in the actual sampling time from one ADC128F1 to any other is ≤ 8.625 µs, while data retrieved from adjacent channels on any single ADC128F1 is obtained at the same time (to within a few nanoseconds).

The TRIDO48 used in Figure B-3 has its Default Output-Enable State (DOES) switch in the '1' position to enable its outputs on power-up. Since the data registers on the TRIDO48 are all cleared on power-up, all of the CVT data on all controlled ADC128F1 IP Modules is frozen as zeroes because the N_HUPDIS line is asserted low on power-up. If the TRIDO48's DOES switch had been set to '0' to disable its outputs on power-up, then the N_HUPDIS control inputs on the ADC128F1's coupled together would be pulled-high to enable CVT updates.

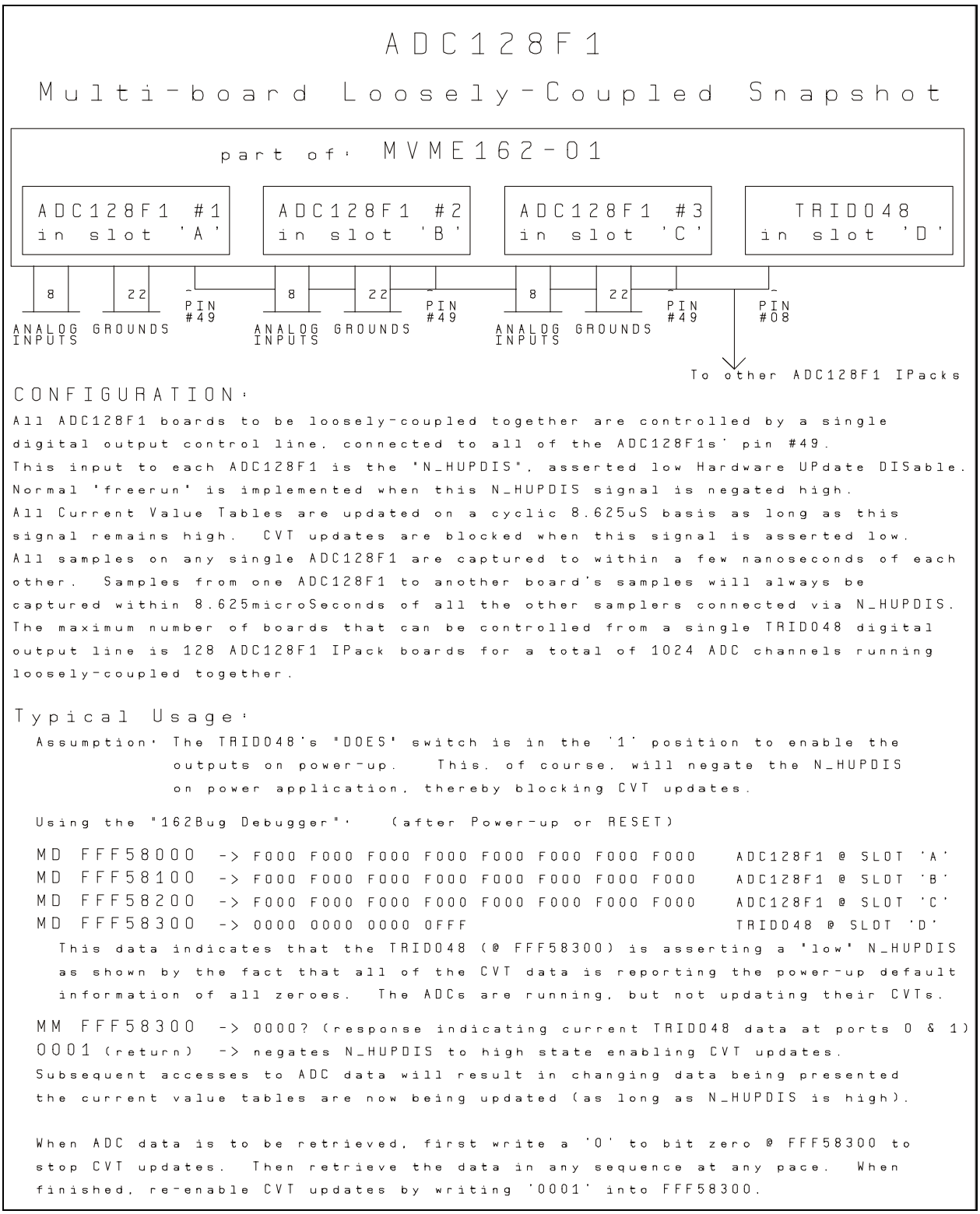


Figure B-3 Multi-Board Loosely-Coupled Snapshot

B.5 Multi-Board Tightly-Coupled Snapshot

For applications that must have all of the analog signals sampled at exactly the same time across multiple ADC128F1 boards, the mode of operation presented in Figure B-4 is recommended. There are two basic differences in operation between this mode and the loosely-coupled snapshot (these differences are presented in Figure B-4):

- The digital control line is connected to the ADC128F1 pin 44 (instead of pin 49) to control the RUN line inputs.
- There are special timing constraints for this mode of operation.

There are two obvious techniques for the development of the RUN pulse required for tightly-coupling multiple ADC128F1 IP Modules.

- A software-controlled technique where a software loop or system real-time clock is used to develop the assertion and negation intervals for setting and clearing the digital line that controls the RUN signal.
- The use of an automatic pulse generation signal source like that which could be developed by the DUAL16CT or DUAL32CT IP Modules. Besides developing the proper pulse width and cyclic repetition rate for the “RUN” signal, these two IP Modules could also signal the processor when it is time to retrieve the ADC data by the assertion of an interrupt on the falling edge of the “RUN” signal.

The ADCs only execute sampling operations when RUN is asserted high. They all start their conversion process on the rising edge of RUN. They automatically start a second sampling and conversion process on the rising edge of N_CONVST after the first sampling has been posted in the CVT. However, the conversion results will not be posted in the CVT, overwriting the first posting, provided the RUN signal is negated in the time span presented in Figure B-4.

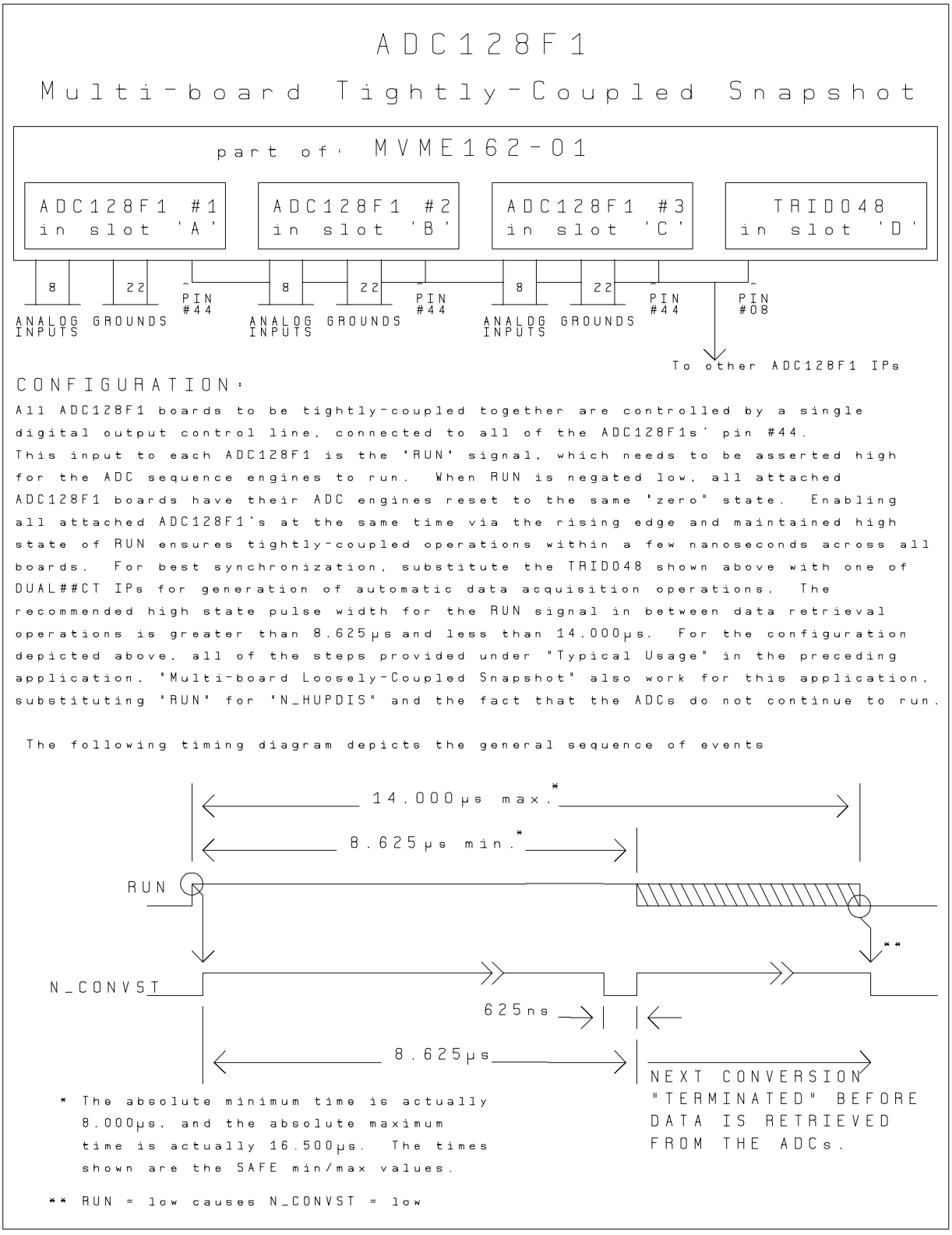


Figure B-4 Multi-Board Tightly-Coupled Snapshot

B.6 Real-time Monitoring

There are many laboratory and test configurations that require independent (of software) monitoring of ADC information, as a crosscheck technique for verifying the accuracy of the conversion process, especially prior to and following special, and often very expensive, test events.

One example, out of many, of this kind of requirement is that of a crash survivability test, where dozens to hundreds of sensors need to be calibrated prior to a test, and confirmed for no shift in accuracy following a test. Often this is done as an independent verification path to ensure that data retrieved via software matches that retrieved at the hardware monitor port, avoiding any issues that may arise from possible software modifications to the retrieved data.

Many times this monitoring technique is tightly coupled to a sensor-shunt or voltage substitution calibration circuit. Figure B-5 is a presentation of the latter technique, where a precision (usually traceable) voltage source is injected into the channel being calibrated with the error in conversion being recorded for post-test analysis compensation. Very little additional circuitry is needed to obtain a technique for performing data logging, whether it is used in real-time or not.

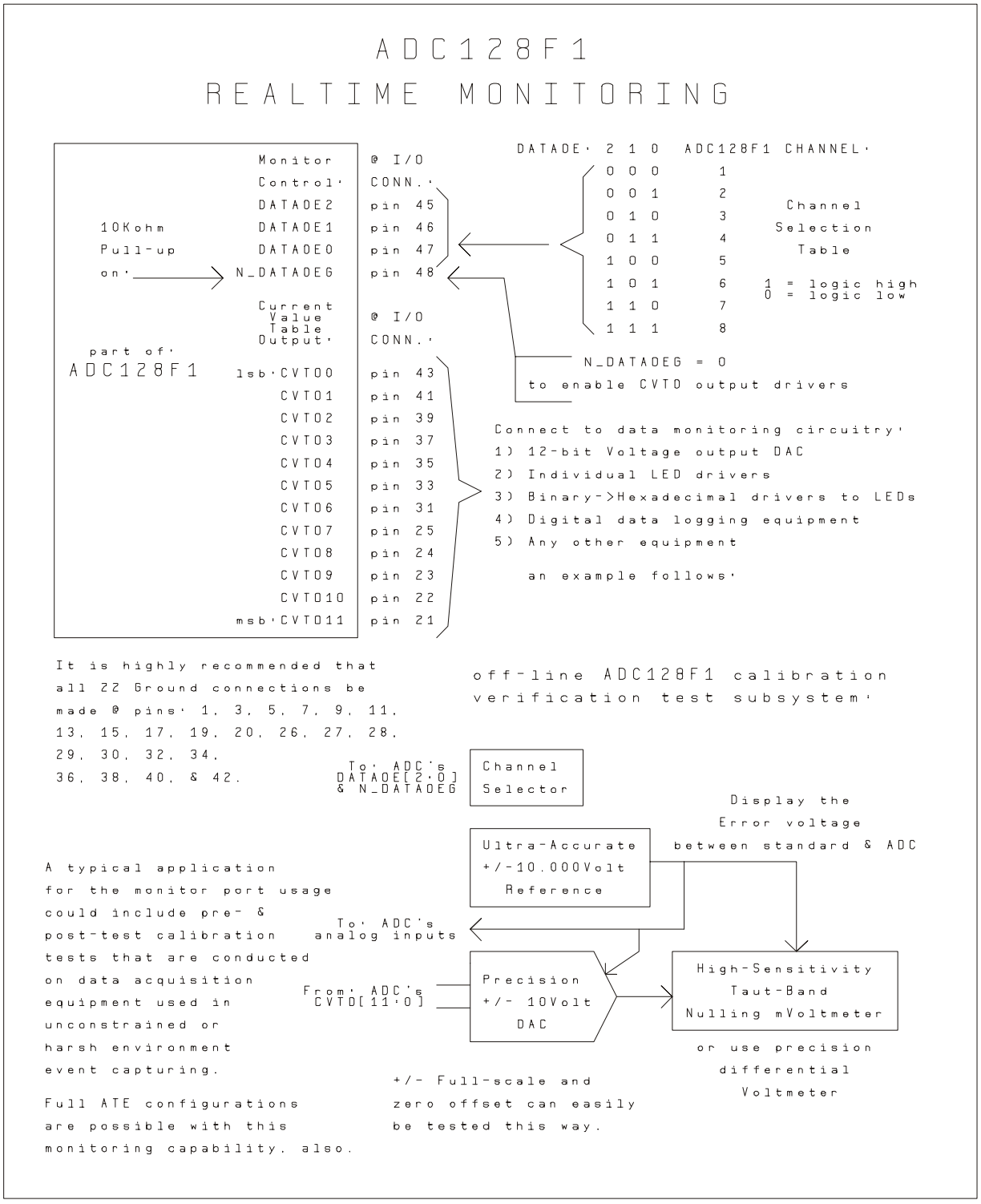


Figure B-5 Real-time Monitoring

APPENDIX C

PROGRAMMING GUIDE

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C.1 Overview

This section of the manual describes the operation of the ADC128F1 from the software perspective, detailing the ADC128F1 registers and providing programming examples. A more detailed description of the hardware can be found in Chapter 2 PRODUCT OVERVIEW and Appendix B, TYPICAL APPLICATIONS.

C.2 Description

The ADC128F1 is an easy-to-use IP Module with 8 channels of 12-bit analog-to-digital converters. Eight data registers, one per channel, are used to read the input voltages for the channels. In free-run mode (which is the default) these eight data registers are the only registers required for operation of the ADC128F1. The control register allows enabling/disabling the update of the CVT. The status register indicates the state of the external data monitor port.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IP Module to provide "no-wait" read accesses of this information. The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IP Module resides.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all ones during valid ID read-only accesses because they remain un-driven.

Table C-1 is the ADC128F1 emulated ID Address Space PROM listing:

Table C-1 ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII “I”	0x49
IPA = 0x01	ASCII “P”	0x50
IPA = 0x02	ASCII “A”	0x41
IPA = 0x03	ASCII “C”	0x43
IPA = 0x04	SYSTRAN’s ID	0x45
IPA = 0x05	DID48’s Model Number	0x6A
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0x6A

C.4 IP Module I/O Address Map

The ADC128F1's I/O Address Map was designed with efficiently located data and control/status registers in the IP Module I/O space (IPA = 0x00 through 0x09). The address detector circuitry is fully decoded.



NOTE: The address detector circuitry is fully decoded. Therefore, any attempt to access IPA addresses at and above IPA = 0x0A will result in no acknowledgment and its subsequent bus time-out error on the IP Module carrier.

On power-up, the Control Register Bit 0 = ‘1’ which is ‘Run Mode’ for the CVT operation and after 25 ms the ADCs will settle out to their connections.

The ADC128F1 has ten 16-bit registers: eight data registers, one control register, and one status register. The ADC128F1 supports word (16-bit) reads and writes (some registers are read only, see descriptions below). The registers are described in detail below.

The first eight locations (IPA = 0x00 through 0x07) are the read-back data registers 0-7 for the ADC data ports 1 through 8.

The ninth location (IPA = 0x08) is the write and read-back Control Register containing a single bit that is used to enable/disable the updating of the CVT. If this bit is set to a ‘1,’ the CVT updates are enabled. If this bit is set to a ‘0,’ the CVT updates are disabled. In the CR bits [15:1] are not used.

The tenth location (IPA = 0x09) is the read-back Status Register reflecting the state of the data monitor port signals. In this register bits [15:6] are not used.

Table C-2 is the ADC128F1 I/O Address Map and contains the data register:

Table C-2 I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	[XXXX] [11:8]	[7:0]	Data Register 0 = 12 bits
IPA = 0x01	[XXXX] [11:8]	[7:0]	Data Register 1 = 12 bits
IPA = 0x02	[XXXX] [11:8]	[7:0]	Data Register 2 = 12 bits
IPA = 0x03	[XXXX] [11:8]	[7:0]	Data Register 3 = 12 bits
IPA = 0x04	[XXXX] [11:8]	[7:0]	Data Register 4 = 12 bits
IPA = 0x05	[XXXX] [11:8]	[7:0]	Data Register 5 = 12 bits
IPA = 0x06	[XXXX] [11:8]	[7:0]	Data Register 6 = 12 bits
IPA = 0x07	[XXXX] [11:8]	[7:0]	Data Register 7 = 12 bits
IPA = 0x08	[XXXX,XXXX]	[XXXX,XXX][0]	Control Register, Bit 0 0 = Disable Conversion 1 = Enable Conversion (Run) Bits [15:1] are not used
IPA = 0x09	[XXXX,XXXX]	[XX][5:0]	Status Register Bit 0 = RUN Bit 1 = N_HUPDIS Bit 2 = DATAOE0 Bit 3 = DATAOE1 Bit 4 = DATAOE2 Bit 5 =N_DATAOEG Bits [15:6] are not used

NOTE: [X] means not used and is read as zero

C.5 Word Access Address Translation

Table C-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VME Bus Address	ISA Bus Address	NuBus Address	IP Module Address
BASE + 0x0	BASE + 0x0	BASE + 0x2	IPA = 0x00
BASE + 0x2	BASE + 0x2	BASE + 0x6	IPA = 0x01
BASE + 0x4	BASE + 0x4	BASE + 0xA	IPA = 0x02
BASE + 0x6	BASE + 0x6	BASE + 0xE	IPA = 0x03
BASE + 0x8	BASE + 0x8	BASE + 0x12	IPA = 0x04
BASE + 0xA	BASE + 0xA	BASE + 0x16	IPA = 0x05
BASE + 0xC	BASE + 0xC	BASE + 0x1A	IPA = 0x06
BASE + 0xE	BASE + 0xE	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B

C.6 Byte Access Address Translation

Table C-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VME bus Address	ISA Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 0x1	BASE + 0x0	BASE + 0x3	IPA = 0x00	0
BASE + 0x0	BASE + 0x1	BASE + 0x2	IPA = 0x00	1
BASE + 0x3	BASE + 0x2	BASE + 0x7	IPA = 0x01	0
BASE + 0x2	BASE + 0x3	BASE + 0x6	IPA = 0x01	1
BASE + 0x5	BASE + 0x4	BASE + 0xB	IPA = 0x02	0
BASE + 0x4	BASE + 0x5	BASE + 0xA	IPA = 0x02	1
BASE + 0x7	BASE + 0x6	BASE + 0xF	IPA = 0x03	0
BASE + 0x6	BASE + 0x7	BASE + 0xE	IPA = 0x03	1
BASE + 0x9	BASE + 0x8	BASE + 0x13	IPA = 0x04	0
BASE + 0x8	BASE + 0x9	BASE + 0x12	IPA = 0x04	1
BASE + 0xB	BASE + 0xA	BASE + 0x17	IPA = 0x05	0
BASE + 0xA	BASE + 0xB	BASE + 0x16	IPA = 0x05	1
BASE + 0xD	BASE + 0xC	BASE + 0x1B	IPA = 0x06	0
BASE + 0xC	BASE + 0xD	BASE + 0x1A	IPA = 0x06	1
BASE + 0xF	BASE + 0xE	BASE + 0x1F	IPA = 0x07	0
BASE + 0xE	BASE + 0xF	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

* Byte-lane 1 not applicable for ID Space

C.7 Register Descriptions

C.7.1 Data Registers 0-7 Bit Description (IPA = 0x00 through 0x07)

The eight 16-bit read-only data registers are used to read the input voltage of the eight ADC channels. Data register 0 corresponds to ADC channel 1, register 1 to channel 2, ... register 7 to channel 8.

Table C-5 Data Register 0 Bit Descriptions

Bit #	15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	Not Used	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
R/W	Read as 1's	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

D11 - D0: These bits comprise the 12-bit ADC value.

C.7.2 Control Register Bit Description (IPA = 0x08)

The Control Register contains a single bit that is used to enable/disable the updating of the CVT. Disabling the CVT before reading of the ADC channels ensures that the readings of all channels represent voltages simultaneously sampled by the parallel ADC's. If this bit is set to a '1,' the CVT updates are enabled. If this bit is set to a '0,' the CVT updates are disabled.

Table C-6 Control Register Bit Description

Bit #	15 to 8	7 to 1	0
Bit Name	Not Used	Not Used	N_SUPDIS
R/W	Read as 1's Writes discarded	Read as 0's Writes discarded	RW
Power-Up State	N/A	N/A	1 = CVT update enabled



NOTE: N_SUPDIS is the CVT update enable/disable bit

C.7.3 Status Register Bit Description (IPA = 0x09)

This register reflects the state of the data monitor port signals. The data monitor port can be used to check the operation of the ADC128F1 device without going through the IP Module logic interface.

Table C-7 Status Register Bit Description

Bit #	15 to 8	7, 6	5	4	3	2	1	0
Bit Name	Not Used	Not Used	N_DATAOEG	DATAOE2	DATAOE1	DATAOE0	N_HUPDIS	RUN
R/W	Read as 1's	Read as 0's	R	R	R	R	R	R
Power-Up State	N/A	N/A	1	0	0	0	1	1

N_ DATAOEG : This bit indicates the state of the N_DATAOEG signal.
DATAOE2 - DATAOE0 : These bits indicate the state of the DATAOE2 - DATAOE0 signals.
N_ HUPDIS : This bit indicates the state of the N_HUPDIS signal.
RUN : This bit indicates the state of the RUN signal.

C.8 Programming Example

The following example illustrates operation of the ADC128F1 device using the CVT update disable feature. It demonstrates how to temporarily disable the update of the CVT. Since all eight channels simultaneously sample, disabling update of the CVT while reading multiple channels ensures that all values in the CVT were sampled at the same time.

- Write a '0' to the control register. This disables the update of the data registers.
- Read data registers 0 to 7 corresponding to ADC channels 1 to 8. The eight ADC values were all sampled at the same time.
- Write a '1' to the control register. This re-enables the update of the data registers.

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GLOSSARY

ADC ----------Analog-to-Digital Converter.

binder----------A routine to allow device driver routines to be called directly from a 'C' language application program.

byte ----------Eight bits.

byte-lane ----------Eight bits of a data bus on octal boundaries.

CAE----------Computer Aided Engineering.

CVT----------Current Value Table consisting of eight current value registers.

DAC ----------Digital to Analog Converters

DOES----------Default Output-Enable State.

doublewide ----------An IP Module that is twice the size of a standard IP Module.

EPLD ----------Erasable Programmable Logic Device.

HUPDIS ----------Hardware UPdate DISable.

ID PROM----------The circuitry that presents the proper data patterns to the lower 8 bits of the IPDbus during the ID (read) transfers.

IP Module ----------Business-card size mezzanine-type subsystem designed with a common digital interface known as the IP bus. The ANSI/VITA 4-1995 standard defines the mechanical and electrical interface to the carrier board.

I/O----------Input/Output.

I/O service call----------Device driver routine call through the operating system

IP logic bus----------A synchronous, 4 M transfers/sec, 16- or 32-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is six bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to four M words of memory space per IP module.

IPDbus ----------IP Module Data Bus.

makefile----------Compiling and linking instructions for the Make utility.

MMU----------Memory Management Unit.

MTBF ----------Mean Time Between Failures.

ns, µs, ms ----------Nanoseconds, microseconds, and milliseconds, respectively.

PC ----------Personal Computer.

QSOP----------Quarter-sized Small Outline Packages.

SAR----------Successive Approximation Register. A popular analog-to-digital conversion technique. (for example, SAR-based ADC technology).

SCF ----------OS-9 Sequential Character File.

singlewide ----------An IP Module printed circuit board (3.9 inches by 1.8 inches). Each module has two 50-pin connectors.

SUPDIS----------Software UPdate DISable.

VHDL ----------Very high-speed integrated circuit Hardware Description Language.

word ----------16 bits

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