

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

ADM1224F

24-Channel, 12-Bit, ±10 V
Differential-Ended-Input, Multiplexed
Analog-to-Digital Converter IP Module
Hardware Reference

Document No. B-T-MR-ADM1224F-A-0-A4

FOREWORD

The information in this document has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Systran reserves the right to make changes without notice.

Systran makes no warranty of any kind with regard to this printed material including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose.

©Copyright 2002 Systran Corporation. All rights reserved.



is a registered trademark of Systran Corporation.
ALTERA® and Altera® are registered trademarks of Altera Corporation.
Excel is a trademark of the Microsoft Corporation.
HP® is a registered trademark of the Hewlett-Packard Corporation.
Motorola® is a registered trademark of the Motorola Corporation.
NuBus™ is a trademark of Texas Instruments, Inc.
OS-9® is a registered trademark of Microware Systems Corporation.
TENMA™ is a trademark of Premier Industrial Corporation.
T-FRAME™ is a trademark of Tracewell Enclosures, Inc.
TRACEWELL® is a registered trademark of Tracewell Enclosures, Inc.
TRI-STATE® is a registered trademark of National Semiconductor Corporation.
VIEWlogic® is a registered trademark of Innoveda, Inc.
Windows NT® is a registered trademark of Microsoft Corporation.

ALTERA: Code © 2002, Systran Corp., All Rights Reserved. The code (programs) contained in this product are proprietary to Systran Corp. and copying or other use of the bit-stream programs, except as expressly authorized by Systran Corp., are expressly prohibited.

Any reference made within this document to equipment from other vendors does not constitute an endorsement of their product(s).

Revised: August 20, 2002

Systran Corporation
4126 Linden Avenue
Dayton, OH 45432-3068 USA
(800) 252-5601 (U.S. only)
(937) 252-5601

FCC

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

As a component part of another system, this information technology product has no direct function and is therefore not subject to applicable European Union directives for Information Technology equipment.

TABLE OF CONTENTS

1. INTRODUCTION 1-1
- 1.1 How to Use This Manual 1-1
  - 1.1.1 Purpose 1-1
  - 1.1.2 Scope 1-1
  - 1.1.3 Conventions 1-1
- 1.2 Related Information 1-1
- 1.3 Quality Assurance 1-2
- 1.4 Technical Support 1-2
- 1.5 Ordering Process 1-3

2. PRODUCT OVERVIEW 2-1
- 2.1 Overview 2-1
  - 2.1.1 The Name 2-1
  - 2.1.2 Features 2-2
- 2.2 Related Products 2-2
- 2.3 Simplified Block Diagram 2-3
  - 2.3.1 Simplified Block Descriptions 2-3
- 2.4 Mid-Level Block Diagram 2-6
  - 2.4.1 Mid-Level Block Descriptions 2-6
- 2.5 Detailed Block Diagram 2-8
  - 2.5.1 Detailed Block Descriptions 2-8
    - 2.5.1.1 Remaining Digital Blocks 2-8
    - 2.5.1.2 Remaining Analog Blocks 2-9
    - 2.5.1.3 Power Filters 2-10
- 2.6 Sampling Details 2-10
  - 2.6.1 Sampling Order 2-10
  - 2.6.2 Sampling Rate 2-10
  - 2.6.3 Sampling Timing 2-11
  - 2.6.4 Deterministic Sampling 2-12
- 2.7 GRAY CODE Engine Details 2-13
- 2.8 Performance Efficiency 2-13
- 2.9 VHDL-Based Activity 2-15

3. INSTALLATION 3-1
- 3.1 Unpacking the ADM1224F 3-1
- 3.2 Visual Inspection 3-1
- 3.3 Jumper Shunts 3-1
- 3.4 Wiring and Jumpering 3-2
  - 3.4.1 Single-ended, Non-inverting Input Channels 3-2
  - 3.4.2 Single-ended, Inverting Input Channels 3-3
  - 3.4.3 Differential-ended, Non-inverting Input Channels 3-3
  - 3.4.4 Differential-ended, Inverting Input Channels 3-3
  - 3.4.5 Unused Inputs 3-4
  - 3.4.6 VREF Connections 3-4
  - 3.4.7 High Shock/Vibration Applications 3-5
- 3.5 ADM1224F Installation 3-5

4. PERFORMANCE 4-1
- 4.1 Overview 4-1
- 4.2 Timing Measurement 4-1
- 4.3 Internal Digital Timing 4-1
  - 4.3.1 Hardware Configuration – GRAY CODE 4-1
  - 4.3.2 GRAY CODE Engine 4-1
  - 4.3.3 Hardware Configuration - ADC Data 4-2
  - 4.3.4 ADC Data Movement 4-3
  - 4.3.5 Converter Control 4-5
- 4.4 Carrier Accesses 4-6

4.4.1 Hardware Configuration – Carrier Accesses 4-6
4.4.2 IP Module Transfers 4-6
4.5 Theoretical Accuracy 4-7
4.6 Typical Empirical Performance 4-11
4.6.1 Test Configuration 4-11
4.6.2 Data Results 4-11

APPENDICES

APPENDIX A – SPECIFICATIONS A-1
APPENDIX B – TYPICAL APPLICATIONS B-1
APPENDIX C – PROGRAMMING GUIDE C-1
GLOSSARY GLOSSARY-1
INDEX INDEX-1

FIGURES

Figure 2-1 ADM1224F Board 2-1
Figure 2-1 ADM1224F Simplified Block Diagram 2-3
Figure 2-2 ADM1224F Mid-Level Block Diagram 2-5
Figure 2-3 ADM1224F Detailed Block Diagram 2-7
Figure 2-4 ADM1224F VHDL Model Block Diagram 2-16
Figure 3-1 ADM1224F Jumpers 3-2
Figure 3-2 ADM1224F Installed on a VME IP Module Carrier 3-5
Figure 3-3 ADM1224F Installed on an ISA IP Module Carrier 3-6
Figure 4-1 GRAY CODE Engine Full Pass 4-2
Figure 4-2 Round-robin Overview 4-4
Figure 4-3 ADC Data Capture Detail 4-4
Figure 4-4 ADC Control Details 4-5
Figure 4-5 Typical I/O Read Timing 4-7
Figure 4-6 Front-end Gain Error Analysis 4-8
Figure 4-7 Overall Gain Error Analysis 4-9
Figure 4-8 Offsets and Total Error Analysis 4-10
Figure 4-9 MIN/Average/MAX of all 24 Channels w/+9.900 Volt Input 4-11
Figure 4-10 Standard Deviation of all 24 Channels w/+9.900 Volt Input 4-12
Figure 4-11 MIN/Average/MAX of all 24 Channels w/0.000 Volt Input 4-12
Figure 4-12 Standard Deviation of all 24 Channels w/0.000 Volt Input 4-13
Figure 4-13 MIN/Average/MAX of all 24 Channels w/-9.900 Volt Input 4-13
Figure 4-14 Standard Deviation of all 24 Channels w/-9.900 Volt Input 4-14

TABLES

Table 2-1 GRAY CODE Sequence Engine Activities 2-14
Table 3-1 Contents of ADM1224F Shipping Packages 3-1
Table 3-2 ADM1224F Installation Tools 3-5
Table 3-3 IP Module Logic Bus Pin Assignments 3-7
Table 3-4 IP Module I/O Connector Pin Assignments 3-8
Table 4-1 Carrier Accesses Typical Times 4-6

This page intentionally left blank

1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's 24-channel, 12-bit, ±10 volt differential-ended-input, multiplexed analog-to-digital converter IP Module board, referred to in this document as the ADM1224F (part number BHAS-ADM1224F).

1.1.2 Scope

This reference manual covers the physical and operational description of the ADM1224F, both from hardware and software perspectives. This manual also contains detailed technical information about the ADM1224F's performance characteristics, and some typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2               file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)

- ANSI/VITA 4-1995 published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA. Phone: 480-951-8866, FAX: 480-951-0720, E-mail: info@vita.com, URL: www.vita.com
- Systran Corporation: www.systran.com

1.3 Quality Assurance

Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to

offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments (including software), contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **support@systran.com**
- Fax: **(937) 252-1349**
- World Wide Web address: www.systran.com

1.5 Ordering Process

To learn more about Systran products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **info@systran.com**
- World Wide Web address: www.systran.com

This page intentionally left blank

2. PRODUCT OVERVIEW

2.1 Overview

The ADM1224F is a singlewide IP Module board, conforming both mechanically and electrically to the *American National Standard for IP Modules (ANSI/VITA 4-1995)*. For a typical (non-Systran) IP Module carrier that holds four IP Modules, the ADM1224F can provide up to 96 channels of high-performance ADCs in a single slot on a computer bus backplane, or be mixed with other IP Modules for a more customized, modular I/O system solution. Using Systran's carriers, up to 120 channels of ADCs may be installed in a single VME slot, or (still more) 144 in a single ISA slot.

The ADM1224F maintains the highest possible accuracy and performance characteristics by minimizing analog errors in the design by using the best (yet, reasonably affordable) components for the tasks to be accomplished. The board level accuracy is also maximized by the inclusion of good ground plane and power filtering design, and by the exclusion of on-board range selectors, gain blocks, offset circuits, anti-aliasing filters, and other special-purpose circuits, thereby providing the user more accuracy for the 12 bits of resolution in the captured and converted data.

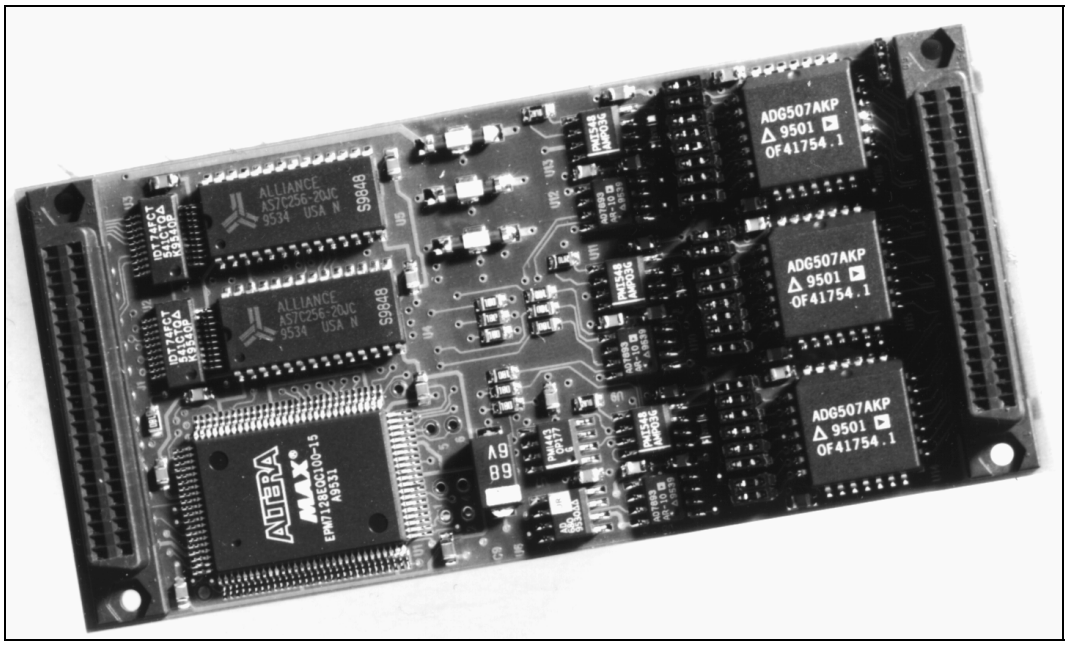


Figure 2-1 ADM1224F Board

2.1.1 The Name

The product name of ADM1224F consists of several descriptive components. The "AD" portion indicates its primary function of performing analog-to-digital conversions. The "M" indicates that this board has a multiplexed, analog front-end design. This means that several channels share an analog-to-digital converter, with their channel-switching function being implemented with an analog multiplexer. If there had been dedicated converters per channel, the leading characters would have been "ADC," as they are on

the ADC128F1 IP Module. The “12” field indicates the number of bits of resolution (not accuracy). The “24” indicates how many analog input channels are available. The “F” indicates that the input range is fixed and that the span is ±10 V. There is no embedded designator for the significant feature of differential-ended-inputs.

2.1.2 Features

- Twenty-four multiplexed channels of switched capacitor SAR-based ADCs with all channels sampling and converting at a free-run and completely deterministic rate of over 14,285 samples/second/channel, with a board total of over 342,857 samples/second.
- All samples provide 12 bits of resolution.
- All twenty-four channels feature true, differential-ended-inputs spanning ±10 V full scale, feeding (gain = 1) instrumentation amplifiers.
- Automatic power-up of all channels sampling and updating the current value table (CVT).
- The CVT provides no-wait, read-on-the-fly IP Module accesses to the latest ADC data.
- 4-bit Frame counter data on top of ADC data in CVT, incremented per pass of 24 channels.
- End-of-frame pulse provided via "N_STROBE" signal on Logic Connector per pass of 24 channels.
- Three sets of multiplexers, instrumentation amplifiers, and ADCs time staggered; one set for every eight channels.
- The ADCs' relative and differential nonlinearities are guaranteed to ±1 LSB (max.).
- Precision +2.500 V ADCs' sampling reference optionally sampled as channel #24.
- Analog (ground) reference jumpers to “inverting” inputs on-board for single-ended inputs for all channels.
- All (on-board filtered) power is obtained from the host carrier.
- Gray Code sequence engines used (where possible) for minimum on-board generated digital noise.
- Embedded analog ground plane for “quiet” operations.
- Theoretical output data coding is two’s complement: 0x800 @ -10.000 V input through 0xFFF @ ≈-0.005 V input; 0x000 @ 0.000 V input through 0x7FF @ +9.995 V input.

2.2 Related Products

- ‘C’ library and OS-9 device driver routines and documentation.
- Windows NT 4.0 library software with documentation.

2.3 Simplified Block Diagram

Figure 2-1 presents the first of three levels of block diagrams for the ADM1224F IP Module.

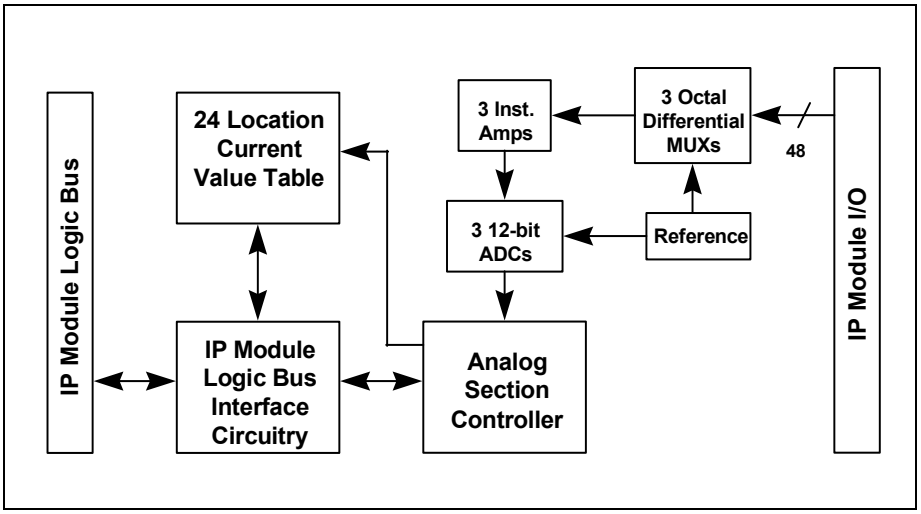


Figure 2-1 ADM1224F Simplified Block Diagram

2.3.1 Simplified Block Descriptions

IP MODULE LOGIC BUS INTERFACE CIRCUITRY

On the left side of the diagram is the IP Module Logic Bus connector through which all transfers between the IP Module Carrier and the ADM1224F's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface Circuitry" contains all of the board level access logic that discriminates between valid and invalid access attempts by the carrier, provides the ID PROM data for identification queries, develops the arbitration and access control logic for the SRAM-based current value table, coordinates activities with the analog section controller, and executes all of the IP Module transfer sequence/control and data bus interface operations.

24 LOCATION CURRENT VALUE TABLE

This block consists of a pair of Static Random Access Memory (SRAM) devices that function as the Current Value Table (CVT). This table consists of 24 consecutive, 16-bit wide locations that contain the latest (most current) conversion results for all 24 input channels. From the IP Module carrier's perspective, these are read-only, 16-bit only, I/O locations that present all ADC and Frame Count data requests with no wait cycles inserted. The analog section controller coordinates with the IP Module Logic Bus Interface Circuitry to perform orderly, error-free deposition of ADC data into the CVT.

ANALOG SECTION CONTROLLER

This block consists of a free-running sequential state machine that controls all of the analog signal selection and conversion activities, data retrieval and serial-to-parallel conversion operations, as well as the writes to the CVT of the conversion results with their appended frame count information. Implied, but not explicitly shown, is a significant connection between the analog section controller and the analog multiplexers.

REFERENCE

The voltage reference is a high-accuracy, buffered source that is the ADCs' conversion analog reference point. This signal is also optionally available as a direct connection into channel #24 for system applications that require continuous monitoring of the voltage reference (hence the connection of the reference to the analog multiplexer's box).

THREE OCTAL DIFFERENTIAL MUXES

This block depicts the analog signal multiplexers that are configured as three separate eight-to-one-by-two analog signal multiplexers whose channel selections are controlled by the analog section controller's state machine. The input channels are grouped as channels 1 through 8, 9 through 16, and 17 through 24.

THREE INSTRUMENTATION AMPS

The differential outputs of the three analog multiplexers drive three separate instrumentation amplifiers that convert the inputs to single-ended, buffered signals for the ADCs. When inputs through the multiplexers are configured as differential-ended inputs, these instrumentation amplifiers remove common-mode (noise, offset errors, etc.) signals.

THREE 12-BIT ADCS

The single-ended outputs of the three instrumentation amplifiers drive the analog inputs to the three 12-bit ADCs. These converters, and their analog signal multiplexers, are time-stagger-controlled by the analog section controller to provide the highest throughput possible with maximum signal settling time (for the highest accuracy possible). The data is retrieved from the ADCs in serial format for eventual deposition of the data into the CVT.

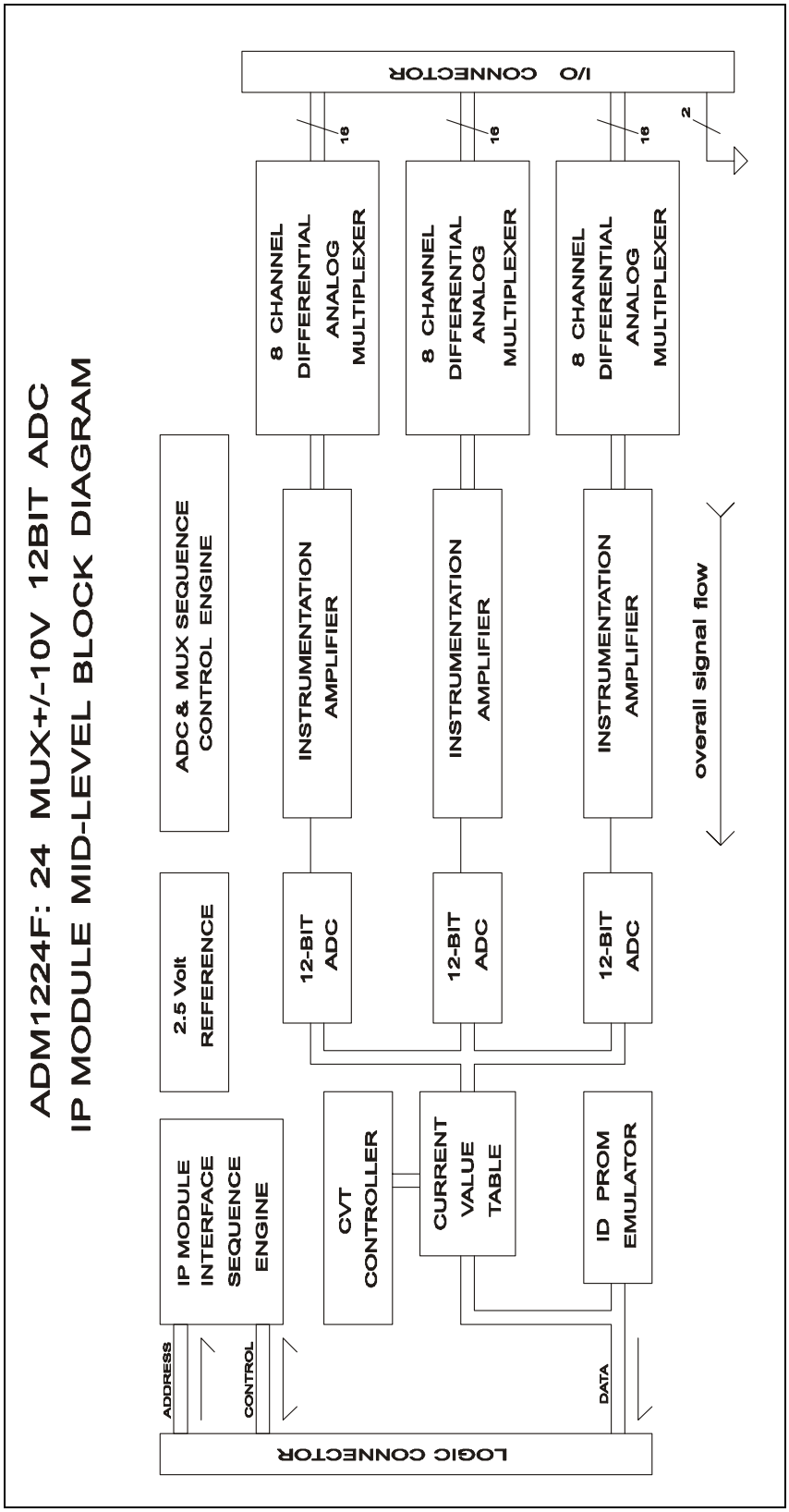


Figure 2-2 ADM1224F Mid-Level Block Diagram

2.4 Mid-Level Block Diagram

Figure 2-2 presents the second, mid-level block diagram of the ADM1224F IP Module.

2.4.1 Mid-Level Block Descriptions

LOGIC CONNECTOR

On the left side of the diagram is the IP Module Logic Bus connection between the ADM1224F and its carrier. The three groups of information signals (not including power and grounds) perform the interface duties. There are six inbound address signals that provide discriminatory information beyond the select (control) signals, accessing both unique ID and I/O data from the ADM1224F's data sources. The normally bi-directional 16-bit data bus is a simplex read-only bus on the ADM1224F since there are only two types of read accesses possible. The normal control lines consist of four select signals, a read/write control line, reset, clock, and the one outbound acknowledgement signal.

ID PROM EMULATOR

This function, included in the IP Module Logic Bus Interface Circuitry block of Figure 2-1, generates the necessary data patterns to emulate an ID PROM during Identification (ID) Transfers from the IP Module to its carrier. Emulating the ID information within the EPLD, instead of providing the data from an actual PROM, is possible due to the never-changing information presented by it. This technique saves board space, lowers costs, improves reliability, and enables this IP Module to provide read accesses to this information without the insertion of wait cycles.

CURRENT VALUE TABLE AND CONTROLLER

These two blocks, included in the 24-Location Current Value Table block of Figure 2-1, separate these functions into their respective physical components. The table itself is actually a pair of 32 KB SRAM devices configured as 32 KWord locations of write (from the ADCs) and read (to the carrier) locations. Only the first 24 locations are used. This registration technique is several orders of magnitude less expensive than any other technique for storing this much information in this small of area.

The CVT controller is contained within the EPLD. All writes and reads to the CVT take place through the EPLD. Not shown in Figure 2-2 is the tight linkage between the CVT Controller and the ADC and MUX Sequence Control Engine, which requests to perform writes to the CVT, and the IP Module Interface Sequence Engine, which requests to perform reads from the CVT. The CVT controller is basically the SRAM's read/write arbiter and timing controller.

ADC AND MUX SEQUENCE CONTROL ENGINE

This block defines the primary functionality of that presented as the analog section controller of Figure 2-1. The core of this engine is a seventy state GRAY CODE counter that is continuously driven by the 8 MHz ICLK from the carrier. It provides orderly sequencing of signal selecting, signal tracking and holding, analog-to-digital converting, retrieving results, serial-to-parallel converting, and assistance in the eventual storing of results.

ANALOG CIRCUITRY

The remainder of Figure 2-2 presents the three sets of analog circuits. For each of eight channels there is a dedicated ADC, which is driven by a dedicated, gain = 1, instrumentation amplifier, which is fed signals from its own 8-channel, differential-input

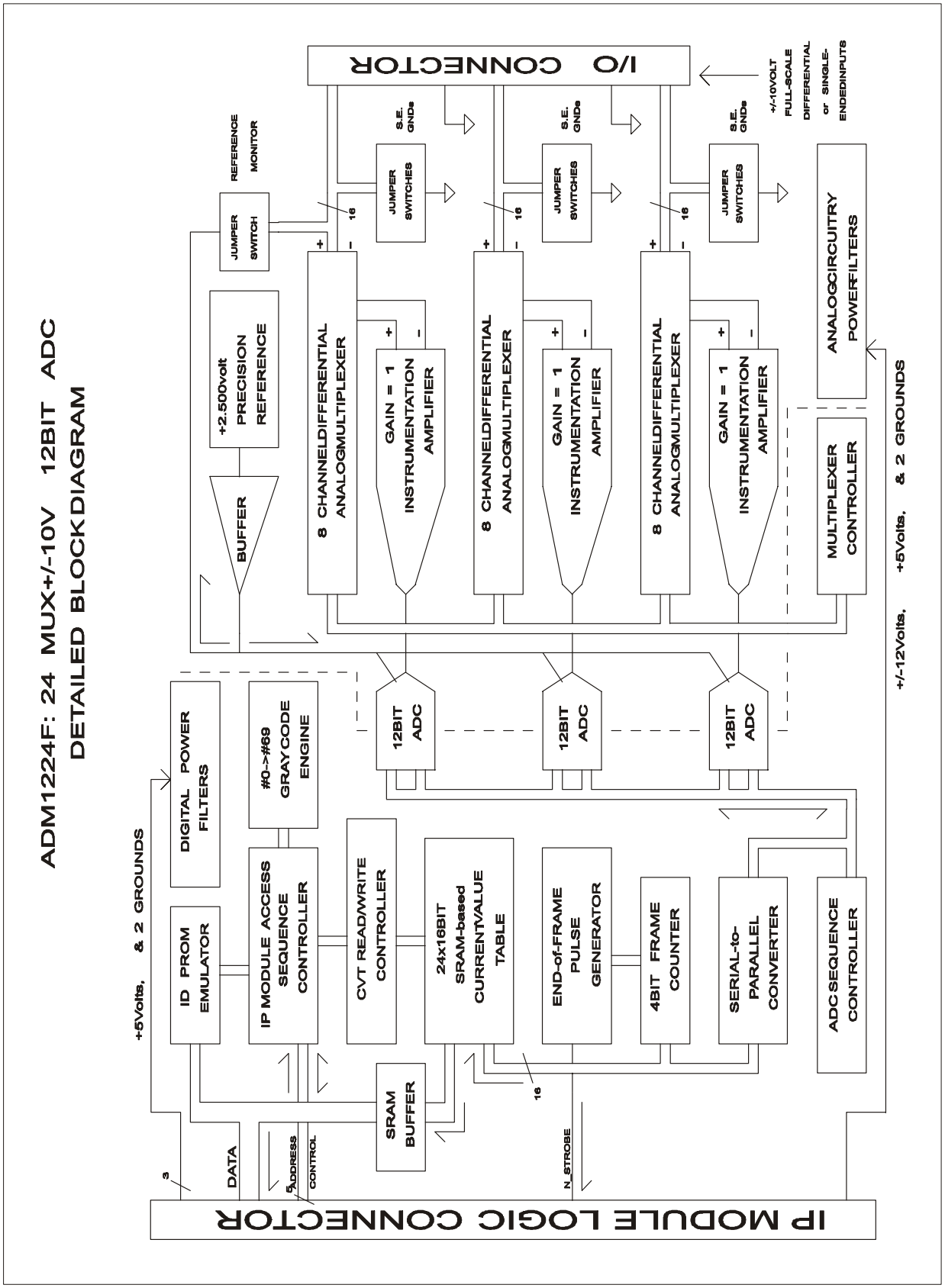


Figure 2-3 ADM1224F Detailed Block Diagram

and differential-output full-scale analog multiplexer. This section of Figure 2-2 expands that which was presented in the upper right corner of Figure 2-1. This diagram still lacks the details necessary to understand all of the features and functions of the ADM1224F IP Module.

2.5 Detailed Block Diagram

Figure 2-3 presents the detailed block diagram of the ADM1224F IP Module.

2.5.1 Detailed Block Descriptions

2.5.1.1 Remaining Digital Blocks

Most of the digital logic (left half of Figure 2-3) has been discussed in the previous figures of this section. The following text provides additional information for a few blocks that Figure 2-3 presents.

DATA MUX

The DATA MUX multiplexes the EPLD internal ID PROM Data and the CVT Data to the IP Bus during ID PROM Reads and CVT (I/O) Reads, respectively.

SERIAL-TO-PARALLEL CONVERTER

As mentioned previously, the three ADCs are serial interface devices. All three share a single, 12-bit, serial-to-parallel converter that captures the digitized data in round-robin fashion. As will be seen in section 2.7, Table 2-1 (page 2-14) the data stream from the ADCs is actually 16 bits in length. The leading nibble of zeroes is discarded. Once the 12 bits of data is assembled in parallel format, the current frame-count value is appended at the highest nibble location, and the 16-bit result is deposited into the current value table by the CVT controller.

4-BIT FRAME COUNTER

A "frame" is defined, for this application, as one complete pass (channel #1 through channel #24) through all 24 channels. The frame counter is provided to enable the user to ascertain an accurate time relationship between the samplings of various channels in any order desired, including at rates slower than the rate at which new data is deposited into the CVT from the ADCs. As with most counters used on the ADM1224F, the frame counter is implemented as a free-running GRAY CODE sequencer, primarily to minimize board level noise (*only one bit changes at a time*). The "frame" count is incremented every 70.0000 µs, ≡ once per pass through all 24 channels. The sequence, in hexadecimal, is:

0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, and 8.

The entire frame count sequence repeats itself every 1.12 ms (70 µs per frame times 16 frames).

END-OF-FRAME PULSE GENERATOR

Every time the frame counter is incremented, a short, ½-ICLK-cycle-width pulse is generated. This low-going pulse occurs every 70 µs on the logic connector's N_STROBE signal line. It can be used for system signaling and synchronization purposes via the carrier's "strobe" connections. One typical use is that of generating an interrupt with the resultant ISR fetching all 24 samples from the CVT.



NOTE: This signal is NOT buffered. Be careful about loading on this line if it is used.

#0 TO #69 GRAY CODE ENGINE

This particular counter is the core of all activity on the ADM1224F IP Module. It is a modified GRAY CODE sequence engine. A minimum of 69 counts was necessary to accomplish all of the control and data retrieval activities. A full-sweep GRAY CODE engine would naturally include 128 counts to encompass the minimum count of 69. A modification in the single-bit changes near the end of the minimum of 69 counts, and the addition of one count to accomplish single-bit changes only, resulted in the 70-state machine design. The non-standard, hexadecimal sequence occurs during the sequence of:

62, 42, 40, 00 instead of 62, 66, 67, 65, … 80, 00.

At one count per ICLK (125 ns per cycle), it takes 8.750 μs per pass through the engine, with eight passes through the engine per frame. Each pass through the engine controls the acquisition and data retrieval processes for one channel each for the three different analog and acquisition paths. The sequencing and associated activities will be covered in greater detail in sections 2.5 and 2.6. For now, it is sufficient to say that for any given pass through this engine, the same multiplexer value is applied to all three analog paths for the conversion process. If the first pass through the engine provides conversion processing for channels 1, 9, and 17; then the fourth pass will provide conversion processing for channels 4, 12, and 20; etc. This topic will be covered in greater detail in sections 2.6 and 2.7.

2.5.1.2 Remaining Analog Blocks

Most of the analog circuitry (right half of Figure 2-3) has been discussed in the previous figures of this section. The following text provides additional information for a few new blocks presented by Figure 2-3.

BUFFER (FOR THE REFERENCE)

This particular (triangular) block is a voltage follower buffer used to provide sufficient drive capability for generating the +2.500 V reference for the three ADCs, and for driving the channel #24 input if that option is exercised.

JUMPER SWITCH (REFERENCE MONITOR)

This is a shunt jumper switch that provides the option of monitoring the +2.500 V ADC reference voltage (defined as VREF ≡ Voltage Reference) for conversion purposes as channel #24 in place of that which would normally be supplied as channel #24 from the I/O connector. It is also possible to couple the buffered reference voltage as an output to the I/O connector if the need exists. This is slightly risky since the ADCs' reference will then be exposed to all noise sources that may exist at the I/O connector and beyond.

JUMPER SWITCHES (S.E. GNDS)

These blocks represent three groups of eight shunt jumper switches, one group per multiplexer. Each switch provides the user the ability to short the inverting differential-ended input to the analog ground reference (AREF) on a per-channel basis for single-ended input applications. It is possible to convert inverted signals using the ADM1224F by driving the desired signal into the inverting input while grounding the non-inverting input. This application, of course, mandates the removal of these single-ended grounding shunts for these channels. An example of this would be the case where an analog input

swings from 0.000 V through -10.000 V but the application needs the data to be represented as if it were changing from 0.000 V through +10.000 V.

2.5.1.3 Power Filters

As can be seen in Figure 2-3, the power distribution and filtering on the ADM1224F IP Module is split between the digital system (upper left area of Figure 2-3) and the analog system (lower portion of Figure 2-3). The IP Module's 50-pin logic connector has two pins reserved for +5 volt power, four pins for ground return, and one each for ±12 V. One +5 V line and two of the ground return lines are dedicated as digital power lines. The digital power filtering consists of eight decoupling (0.1μF) capacitors. The other +5 V line, ±12 V lines, and the remaining two ground return lines (separately defined as AREF ≡ Analog Reference) are dedicated as analog power lines. The analog power filter consists of a 68 μF bulk filter for the +5 V input, three T-type L-C-L filters for the +5 and ±12 V sources, and seventeen decoupling (0.1 μF) capacitors. About two thirds of the board has a solid analog ground plane, under all of the analog circuitry and analog power filters, that connects to AREF (analog ground return). The analog and digital grounds are tied together on the carrier side of the logic connector, as are the two different +5 V power source lines.

2.6 Sampling Details

The ADM1224F IP Module is a fixed-sequence, free-running sampling machine. As described previously, the channels are sectored into three groups of eight channels. Despite its initial appearance, the signal sampling and data conversion process is deterministic and, with the help of the appended frame count values, exact times between any samples can be calculated for samples obtained within a window of 1.12 ms. Channel-to-channel uncertainty is on the order of a few nanoseconds (based upon the stability of the **ICLK** supplied by the carrier).

2.6.1 Sampling Order

The channel number sampling order is: 1, 9, 17, 2, 10, 18, 3, 11, 19, 4, 12, 20, 5, 13, 21, 6, 14, 22, 7, 15, 23, 8, 16, and 24.

2.6.2 Sampling Rate

All channels are tightly controlled in their timings for channel selection, settling times, and when the actual conversion process starts as defined by the transition from "track" mode to "hold" mode. Each channel is repetitively sampled at a fixed cycle time of 70.000 μs, for a fixed sampling rate of 1÷70 μs = 14,285.71429 (over 14,285) samples per second per channel.

Due to the potential access contention to the CVT, the CVT controller will arbitrate the access for a no-WAIT read to the carrier while writes to the CVT of newly acquired data are delayed, as necessary. The window of opportunity for these writes to the CVT is four ICLK cycles long per sampling.



NOTE: This means that if the carrier starts a read of CVT information at exactly the same time that new ADC data is ready to be written into the CVT, the ADM1224F IP Module can support up to a maximum of one carrier-inserted HOLD cycle and still accomplish the write to the CVT. If the carrier inserts more than one HOLD cycle, then the write to the CVT will not take place and the captured data is discarded

There are no built-in limits for the number of HOLD cycles that can be asserted by a carrier during any one transfer. This CVT write activity will be explored when the actual sequence of events is explored in greater detail in section 2.6. The "bottom line" of this immediate discussion is that while the sampling rate is fixed, the write-to-the-CVT rate is not necessarily fixed during times of contention for the usage of the CVT.

There may be applications where a sampling rate of 14,285 samples per second is insufficient for the bandwidth of the signal to be captured. Supercommutation techniques solve this problem nicely. For instance, if a signal has a bandwidth of 5 KHz, then it is recommended that the signal be sampled at least at a 25 KHz rate, more if possible. Applying the same signal to both channels #1 and #5 (first and thirteenth channels to be sampled) will provide evenly spaced acquisitions 35 μs apart for an aggregate sampling rate of over 28,571 samples per second. Evenly spacing the supercommutation of multiple samplings for the same signal applied to three input channels could be accomplished by driving the signal into channels #1, #19, and #14 (first, ninth, and seventeenth channels to be sampled) for an aggregate sampling rate of over 42,857 samples per second. A four-channel sampling applied to channels #1, #3, #5, and #7 (first, seventh, thirteenth, and nineteenth channels to be sampled) yields an aggregate sampling rate of over 57,142 samples per second. At the extreme, applying the same signal to all 24 channels provides an aggregate sampling rate of over 342,857 samples per second.



NOTE: The apparent input impedance drops (to a minimum of ≈ 17 KΩ) as the number of channels is increased in this scheme, thus requiring more drive capability from the signal source.

2.6.3 Sampling Timing

As discussed on page 2-9, three samplings occur per pass of the 70 states of the main GRAY CODE engine, with eight full passes required for a full frame of 24 channels of sampling. Also recall that while only 69 states were required to accomplish the necessary sampling tasks, a seventieth state was added to provide true single-bit transitions in the engine. Thus, every third sampling has an extra ICLK cycle added to its sampling time. The following is a complete list of the sampling time spacing between channels, in the order of sampling.

Using channel #1 as the start of the sampling process:

2.875 μs elapse from the sampling of channel #1 until the sampling of channel #9.
2.875 μs elapse from the sampling of channel #9 until the sampling of channel #17.
3.000 μs elapse from the sampling of channel #17 until the sampling of channel #2.
(Notice the extra 125 ns representing the seventieth state of the GRAY CODE engine.)
2.875 μs elapse from the sampling of channel #2 until the sampling of channel #10.
2.875 μs elapse from the sampling of channel #10 until the sampling of channel #18.
3.000 μs elapse from the sampling of channel #18 until the sampling of channel #3.
2.875 μs elapse from the sampling of channel #3 until the sampling of channel #11.
2.875 μs elapse from the sampling of channel #11 until the sampling of channel #19.
3.000 μs elapse from the sampling of channel #19 until the sampling of channel #4.
2.875 μs elapse from the sampling of channel #4 until the sampling of channel #12.
2.875 μs elapse from the sampling of channel #12 until the sampling of channel #20.
3.000 μs elapse from the sampling of channel #20 until the sampling of channel #5.
2.875 μs elapse from the sampling of channel #5 until the sampling of channel #13.
2.875 μs elapse from the sampling of channel #13 until the sampling of channel #21.
3.000 μs elapse from the sampling of channel #21 until the sampling of channel #6.
2.875 μs elapse from the sampling of channel #6 until the sampling of channel #14.
2.875 μs elapse from the sampling of channel #14 until the sampling of channel #22.

3.000 µs elapse from the sampling of channel #22 until the sampling of channel #7.
2.875 µs elapse from the sampling of channel #7 until the sampling of channel #15.
2.875 µs elapse from the sampling of channel #15 until the sampling of channel #23.
3.000 µs elapse from the sampling of channel #23 until the sampling of channel #8.
2.875 µs elapse from the sampling of channel #8 until the sampling of channel #16.
2.875 µs elapse from the sampling of channel #16 until the sampling of channel #24; and 3.000 µs elapse from the sampling of channel #24 until the next sampling of channel #1 again.

In summary, MUX'A' through MUX'B' channels' samplings occur at a spacing of 2.875 µs; MUX'B' through MUX'C' take 2.875 µs; while transitions from MUX'C' through MUX'A' require 3.000 µs.

2.6.4 Deterministic Sampling

For any given period ≤ 1.12 ms, the exact timing relationship can be determined between any two samples to nanosecond-resolution (± ICLK uncertainty). This is accomplished by adding up the delta-time values between channel numbers as presented above in section 2.6.3, and adding to that value 70 µs per frame count difference between the two samples, as discussed in section 2.3.1.1, "4-bit Frame Counter." A few examples should help clarify any outstanding uncertainties.

Assume that channel #1 is read from the CVT and its high nibble (frame count) value = 0xC, and that channel #1 is subsequently read, in less than 1.12 ms, from the CVT with a new high nibble value = 0xE. Repeating that the frame count sequence is a true GRAY CODE sequence, which yields the path of: …, 4, C, D, F, E, A, …, it can be seen that the elapsed time from the first sampling to the second sampling = 70 µs × 3 = 210.000 µs.

Assume that channel #12 is read and its frame count value = 0x1. Channel #16 is then read and its frame count value = 0x3. The within-frame delta time between channel #12 and channel #16 = 35.000 µs. The frame count sequence encompassing both samples appears as: …, 8, 0, 1, 3, 2, 6, …. Since the samples were in back-to-back frames, only 70.000 µs needs to be added to the value of 35.000 µs for a total time between samplings of 105.000 µs.

Assume that channel #18 is read and its frame count value = 0x6. Then channel #14 is read and its frame count value is 0xB. The within-frame delta time between channels #18 and #14 adds up to 32.125 µs. The frame count sequence that covers both of these samples is …, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9, …. The difference in frame count values yields an additional 70.000 µs × 9 = 630µs. The total time between these two samples = 32.125 µs + 630.000 µs = 662.125 µs.

Assume that channel #8 is read and its frame count value = 0x7. Then channel #17 is read and its frame count value = 0x5. The frame count values are back-to-back as shown by the sequence of …, 2, 6, 7, 5, 4, C, …. Channel #8 is the third-last sampling of frame #7 while channel #17 is the third sampling of the very next frame #5. Therefore, the total time between these two samples = 14.500 µs.

Assume that channel #19 is read and its frame count value = 0x8. Then channel #4 is read and its frame count value = 0x0. The within-frame delta time between channels #19 and #4 is only 3.000 µs since they are consecutive samples. However, the frame counts were different. The frame count sequence that includes both samples is …, B, 9, 8, 0, 1, 3, …. Since the frames are consecutive, only 70.000 µs has to be added for the frame count difference. This brings the time difference between these two samples to a total of 73.000 µs.

There is a timing cross matrix, 24 channels by 24 channels, presented in Appendix B that provides all of the different possibilities for within-frame delta timings (some of which were used as examples above), with directions on how to use it.

2.7 GRAY CODE Engine Details

Table 2-1 provides a complete listing of all of the activities that take place for all seventy states of the primary sequence engine on the ADM1224F IP Module. Every event is fully synchronous to the ICLK's 8 MHz clock; one event every .125 µs. One full sweep through this core engine takes 8.750 µs.



NOTE: States #63, 62, 42, and 40, while single-bit transitions, are not a normal GRAY CODE sequence.

Negating the most significant GRAY CODE bit from state #40 repeats the process back to state #00.

2.8 Performance Efficiency

The maximum throughput for a single ADC used on the ADM1224F is limited by the minimum specification of 8.52 µs for the conversion and fastest data retrieval rates possible. This equates to 68.16 ICLK cycles; a minimum of 69 states; or a minimum of 70 GRAY CODE states. The efficiency rating of the core engine coupled with just one of the ADC's is therefore at 97.37%. The three different ADC's were time-staggered to utilize as much common circuitry as possible for the data retrieval and CVT storage processes, and to maximize the total data acquisition rate of the entire board.

Table 2-1 GRAY CODE Sequence Engine Activities

State	Synchronous Event:
0x00	Drive ADC#A's N_CONVST ⇓ low
0x01	Increment 3-bit counter that drives MUX#C signal selection
0x03	Retrieve ADC#A's leading 0 (bit 15) and discard
0x02	Retrieve ADC#A's leading 0 (bit 14) and discard
0x06	Retrieve ADC#A's leading 0 (bit 13) and discard
0x07	Retrieve ADC#A's leading 0 (bit 12) and discard
0x05	Retrieve ADC#A's bit 11 (msb) and register
0x04	Retrieve ADC#A's bit 10 and register
0x0C	Retrieve ADC#A's bit 9 and register
0x0D	Retrieve ADC#A's bit 8 and register
0x0F	Retrieve ADC#A's bit 7 and register
0x0E	Retrieve ADC#A's bit 6 and register
0x0A	Retrieve ADC#A's bit 5 and register
0x0B	Retrieve ADC#A's bit 4 and register
0x09	Retrieve ADC#A's bit 3 and register
0x08	Retrieve ADC#A's bit 2 and register
0x18	Retrieve ADC#A's bit 1 and register
0x19	Retrieve ADC#A's bit 0 (lsb) and register
0x1B	idle
0x1A	Write ADC#A's data to CVT if carrier not reading CVT
0x1E	Write ADC#A's data to CVT if carrier not reading CVT
0x1F	Write ADC#A's data to CVT if carrier not reading CVT
0x1D	Write ADC#A's data to CVT if carrier not reading CVT
0x1C	Drive ADC#A's N_CONVST ⇑ high (*starts actual conversion*) and Drive ADC#B's N_CONVST ⇓ low
0x14	Increment 3-bit counter that drives MUX#A signal selection
0x15	Retrieve ADC#B's leading 0 (bit 15) and discard
0x17	Retrieve ADC#B's leading 0 (bit 14) and discard
0x16	Retrieve ADC#B's leading 0 (bit 13) and discard
0x12	Retrieve ADC#B's leading 0 (bit 12) and discard
0x13	Retrieve ADC#B's bit 11 (msb) and register
0x11	Retrieve ADC#B's bit 10 and register
0x10	Retrieve ADC#B's bit 9 and register
0x30	Retrieve ADC#B's bit 8 and register
0x31	Retrieve ADC#B's bit 7 and register
0x33	Retrieve ADC#B's bit 6 and register
0x32	Retrieve ADC#B's bit 5 and register
0x36	Retrieve ADC#B's bit 4 and register
0x37	Retrieve ADC#B's bit 3 and register
0x35	Retrieve ADC#B's bit 2 and register
0x34	Retrieve ADC#B's bit 1 and register
0x3C	Retrieve ADC#B's bit 0 (lsb) and register
0x3D	idle

State	Synchronous Event:
0x3F	Write ADC#B's data to CVT if carrier not reading CVT
0x3E	Write ADC#B's data to CVT if carrier not reading CVT
0x3A	Write ADC#B's data to CVT if carrier not reading CVT
0x3B	Write ADC#B's data to CVT if carrier not reading CVT
0x39	Drive ADC#B's N_CONVST ⇑ high (*starts actual conversion*) and Drive ADC#C's N_CONVST ⇓ low
0x38	Increment 3-bit counter that drives MUX#B signal selection
0x28	Retrieve ADC#C's leading 0 (bit 15) and discard
0x29	Retrieve ADC#C's leading 0 (bit 14) and discard
0x2B	Retrieve ADC#C's leading 0 (bit 13) and discard
0x2A	Retrieve ADC#C's leading 0 (bit 12) and discard
0x2E	Retrieve ADC#C's bit 11 (msb) and register
0x2F	Retrieve ADC#C's bit 10 and register
0x2D	Retrieve ADC#C's bit 9 and register
0x2C	Retrieve ADC#C's bit 8 and register
0x24	Retrieve ADC#C's bit 7 and register
0x25	Retrieve ADC#C's bit 6 and register
0x27	Retrieve ADC#C's bit 5 and register
0x26	Retrieve ADC#C's bit 4 and register
0x22	Retrieve ADC#C's bit 3 and register
0x23	Retrieve ADC#C's bit 2 and register
0x21	Retrieve ADC#C's bit 1 and register
0x20	Retrieve ADC#C's bit 0 (lsb) and register
0x60	idle
0x61	Write ADC#C's data to CVT if carrier not reading CVT
0x63	Write ADC#C's data to CVT if carrier not reading CVT
0x62	Write ADC#C's data to CVT if carrier not reading CVT
0x42	Write ADC#C's data to CVT if carrier not reading CVT
0x40	Drive ADC#C's N_CONVST ⇑ high (*starts actual conversion*)

2.9 VHDL-Based Activity

This section concludes with, Figure 2-4, a block diagram for the VHDL model contained within the 7128 EPLD, hopefully pulling together all of the topics described above. As can be seen by the complexity of activity, this section cannot be understood without first reading Section 2.7. Note that there are three (non-GRAY CODE) binary counters contained within this model. They are the multiplexers' address counters for selecting the channels to be converted. Making these GRAY CODE sequencers, while possible and desirable from a noise-reduction viewpoint, would have caused the channel connections at the I/O Connector to appear cumbersome and confusing; hence, the binary sequencing.

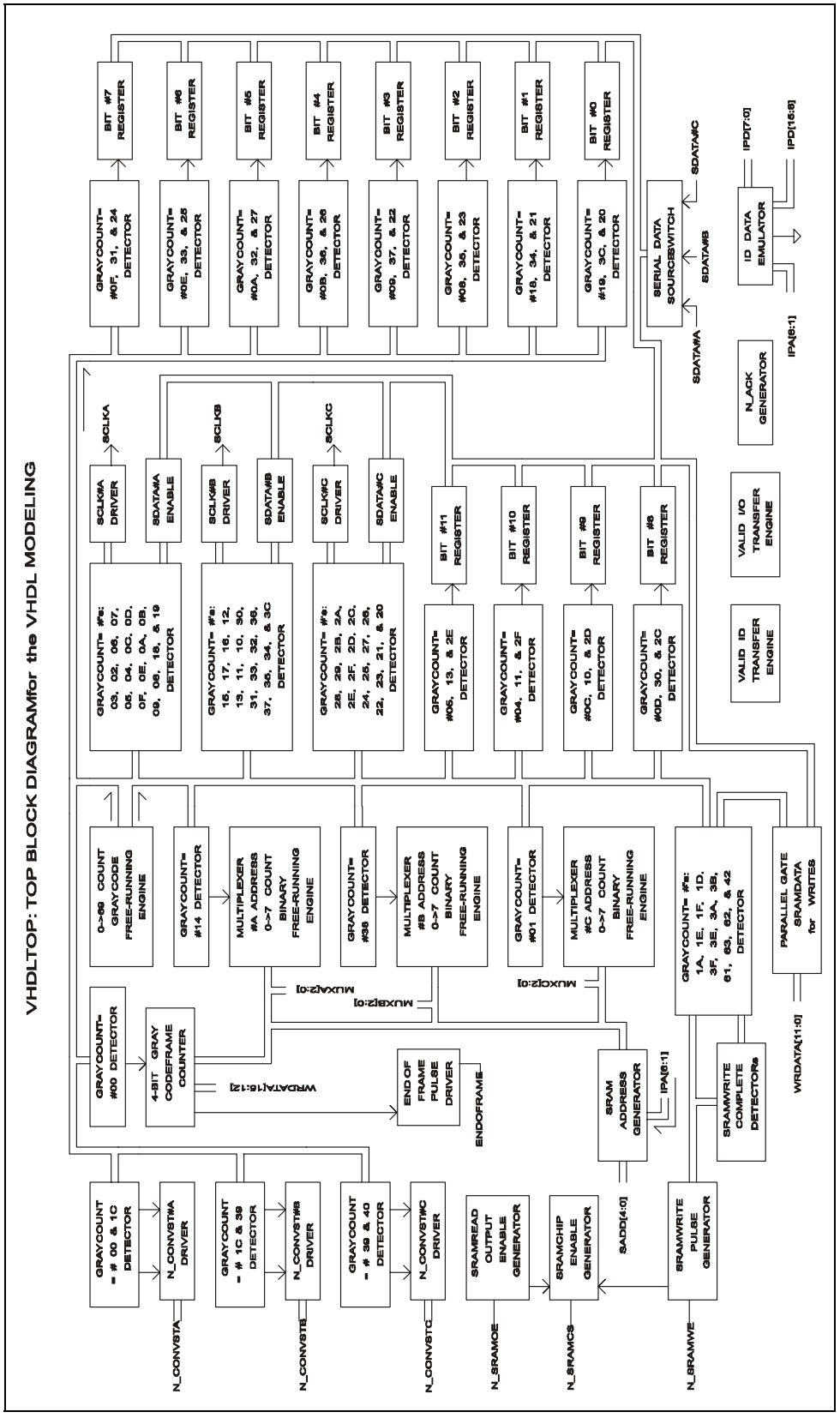


Figure 2-4 ADM1224F VHDL Model Block Diagram

3. INSTALLATION

3.1 Unpacking the ADM1224F

The contents of the ADM1224F shipping packages are listed in Table 3-1.

Table 3-1 Contents of ADM1224F Shipping Packages

Qty	Description
1	ADM1224F Printed Circuit Assembly
1	ADM1224F Hardware Reference*

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Order extra manuals by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR-ADM1224F) to request additional hardware manuals.



NOTE: The ADM1224F is an Electrostatic Sensitive Device (ESD). Install the ADM1224F on an anti-static workbench using good ESD practices to protect the IP Module and its host carrier board.

3.2 Visual Inspection

Immediately inspect the ADM1224F to determine if any damage occurred during shipping. Do **NOT** install a board that appears to be damaged. Contact Systran immediately for return and replacement instructions.

3.3 Jumper Shunts

Refer to Figure 3-1, a partial (not to scale) assembly drawing, for the following discussions. Prior to the installation of the ADM1224F IP Module on its carrier, the as-shipped condition may need to be modified, depending upon the application of this device. The as-shipped configuration has all 24 channels configured as single-ended inputs by the installation of shorting shunts on all 24 jumpers at J3 through J26. Additionally, channel #24 has its non-inverting input configured for a signal source to be applied from the I/O connector by the installation of a shorting shunt at J27, and with no shunt installed at J2.

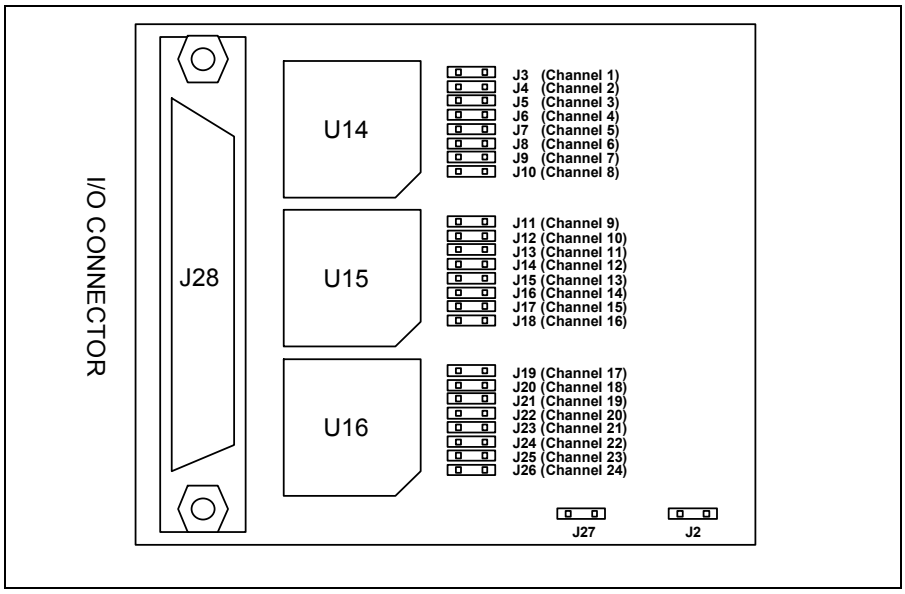


Figure 3-1 ADM1224F Jumpers

NOTE: J2 is not labeled on the ADM1224F board. The silkscreen data was inadvertently left off. J2 is located adjacent to J27 as shown in Figure 3-1.

3.4 Wiring and Jumpering

The ADM1224F performs sequential (not simultaneous) sampling of channels, as described in detail in section 2.6. If there are critical timing relationships between various analog signals that need conversions, then these should be considered when assigning channel numbers and subsequently jumpering and wiring the I/O interfaces for this application. The following are a few example configurations.

3.4.1 Single-ended, Non-inverting Input Channels

Single-ended, Non-inverting Input Channels are the most commonly used configuration for analog-to-digital conversion products. Applications using the ADM1224F IP Module to convert these types of signal sources should:

- Apply these signals to their assigned "**VIN+#**" connections at the I/O connector.
- Leave the corresponding "**VIN-#**" inverting inputs at the I/O connector or tie them externally to pins #25 and #26, providing additional connections to "AREF".
- Install their respective jumper shunts for these channels, providing local, low-impedance connections to "AREF" to the inverting inputs.

EXAMPLE:

If channels #4, #13, and #23 are to be used as single-ended, non-inverting input channels:

- Apply their input signals to I/O pins #30, #14, and #24, respectively.
- Install shorting shunts on jumpers J6, J15, and J25.
- Externally connect the inverting input connections on the I/O connector at pins #29, #13, and #23 to pins #25 and #26 to provide additional external connections to the AREF (analog reference) ground plane.

3.4.2 Single-ended, Inverting Input Channels

If an application requires that a channel must have a single-ended, signal undergo, polarity inversion prior to conversion to digital format, the following technique may be used on the ADM1224F IP Module.

- Apply the signal to the assigned channel's "**VIN-#**" (inverting input)
- Remove or leave off the appropriate shorting shunt for its inverting input jumper, and
- Externally connect the "AREF" to the channel's "**VIN+#**" (non-inverting input).

EXAMPLE:

Assume that channel #12 needs to have its single-ended input signal inverted prior to being converted.

- Apply the inbound signal to the I/O connector pin #37 (inverting input)
- Remove the shorting shunt at J14, and
- Externally connect I/O pin #38 (non-inverting input) to both I/O pins #25 and #26.

3.4.3 Differential-ended, Non-inverting Input Channels

Applications requiring excellent common-mode rejection capabilities can use the following configuration for converting signals using the ADM1224F IP Module. It can be used regardless of whether the signal source is a single-ended driver, or a differential-ended driver. This configuration is ideal for removing deliberate offsets applied in earlier circuitry.

EXAMPLE:

A full-bridge piezo-resistive sensor is excited by a unipolar voltage source (For example, +10 V referenced to ground), which generates a null-state centered at +5 V.

- The non-inverting signal source is applied to the non-inverting input of the ADM1224F
- The shorting shunt is removed from its appropriate jumper; and
- The inverting input receives either the inverting signal from a differential driver, or the remote analog ground reference point.

For best results, use tightly twisted pairs for the inverting and non-inverting signal carriers so that equal amounts of external "noise" are applied to both signal carriers for subsequent removal by the differential amplifiers on the ADM1224F. The pin-out on the I/O connector is designed to work with twisted-pair, IDC cables.

EXAMPLE:

One application of this common configuration is provided for channel #2.

- Apply the non-inverting input signal to I/O pin #28
- Remove the shunt from jumper J4, and
- Connect I/O pin #27 to the signal source's local analog ground reference (or to the inverting output of a differential driver).

3.4.4 Differential-ended, Inverting Input Channels

Applications requiring that a channel must have a differential-ended signal-pair undergo polarity inversion prior to conversion to digital format can use this technique.

A common example of this might be the need for data from an accelerometer to provide positive-going information for forward (+X-axis notation) acceleration, and the in-line gain block is presenting the negation of this goal.

- Apply the non-inverting input signal to the "**VIN-#**" (inverting input)
- Apply the inverting input signal to the "**VIN+#**" (non-inverting input), and
- Remove or leave off the appropriate shorting shunt for its inverting input jumper.

EXAMPLE:

Assume that the analog signals being converted as channels #5 and #22 are differentially driven by inverting drivers, and that they need another analog inversion prior to conversion to digital format to provide analog polarity that represents valid physical events taking place.

- Connect the non-inverting signal for channel #5 to the I/O pin #5 (inverting input).
- Connect the inverting signal for channel #5 to the I/O pin #6 (non-inverting input).
- Connect the non-inverting signal for channel #22 to the I/O pin #47 (inverting input).
- Connect the inverting signal for channel #22 to the I/O pin #48 (non-inverting input).
- Leave off shorting shunts or remove them from both jumpers J7 and J24.

3.4.5 Unused Inputs

Ground both non-inverting and inverting inputs for all unused inputs to AREF to minimize noise in the system, since these channels will be converted anyway. This is accomplished by connecting all of the unused non-inverting inputs to the AREF signals at the I/O connector, and by installing the shorting shunts for the same channels, thereby connecting their inverting inputs to AREF.

EXAMPLE:

The following demonstrates the proper wiring and jumpering scheme for all of the unused channels not cited previously in sections 3.4.1 through 3.4.4:

For channels: #1, #3, #6 through #11, #14 through #21, and #24.

- Connect I/O pins: 2, 4, 32, 8, 34, 10, 36, 12, 40, 16, 42, 18, 44, 20, 46, 22, and 50 to both I/O pins: 25 and 26 to connect all of the unused non-inverting inputs to AREF.
- Install jumpers: 3, 5, 8, 9, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 22, 23, 26, and 27 to connect all unused inverting inputs to AREF.
- Ensure that the shorting shunt is **NOT** installed at jumper J2.
- Installing a shorting shunt at jumper J27 connects the I/O connector's pin #50 to the non-inverting input of analog multiplexer, U16, for channel #24.

3.4.6 VREF Connections

Channel #24 can obtain its analog inputs from either the I/O connector or from the local buffered VREF signal for those applications that require continuous monitoring of the voltage reference in the data set. This is accomplished by removing the shorting shunt at jumper J27 and installing it at jumper J2.

As cited previously in sections 2.3.1.2 and 2.4.2, it is possible (but not recommended) to monitor VREF at pin #50 of the I/O connector. This is accomplished by installing shorting shunts at both jumpers J2 and J27.

In both scenarios, the inverting input to channel #24 needs to be tied to AREF. This is accomplished by installing a shorting shunt at jumper J26.

3.4.7 High Shock/Vibration Applications

For those applications where the ADM1224F will be subjected to high shock and/or vibration environments, it is recommended that the push-on shorting shunts that are supplied with the ADM1224F not be used. Instead, short together the pins of the appropriate jumpers using either wire-wrap techniques, or by soldering wires between posts normally needing the shorting shunts.



NOTE: If wires are soldered onto the jumpers, use low heat to prevent the melting of the jumper posts' plastic holder, and ground the tip to the anti-static equipment to ensure safe soldering on ESD circuits.

3.5 ADM1224F Installation

The tools required for the ADM1224F installation are listed in Table 3-2.

Table 3-2 ADM1224F Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

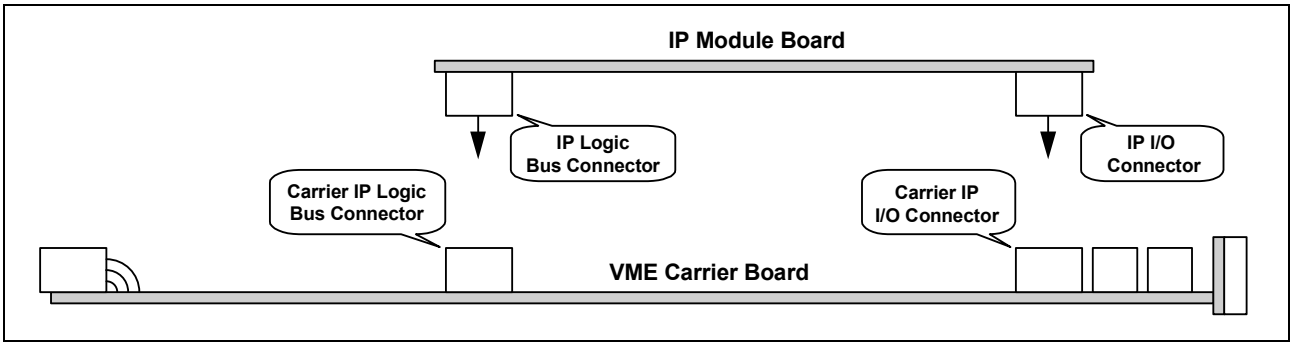


Figure 3-2 ADM1224F Installed on a VME IP Module Carrier

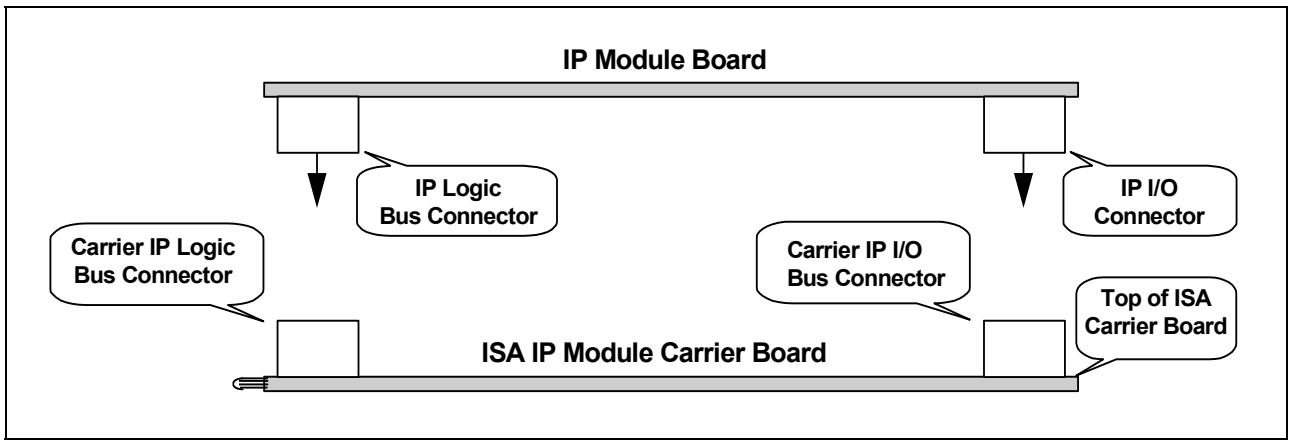


Figure 3-3 ADM1224F Installed on an ISA IP Module Carrier

Figure 3-2 shows the ADM1224F installed on a VME IP Module carrier, and Figure 3-3 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the table are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board user's manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the installation of the ADM1224F can be made.
3. Remove the ADM1224F from the shipping package and place it on the ESD bench.
4. Install the ADM1224F onto the carrier board by applying adequate and equal pressure to the ADM1224F board at both ends.

*5. Install four M2x5 mm flat head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the ADM1224F to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
Intreq1*	44	N_INTREQ1
A4	43	IPA4
intreq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module Logic Bus Pin #	Signal Names
50	VIN+#24
49	VIN-#24
48	VIN+#22
47	VIN-#22
46	VIN+#20
45	VIN-#20
44	VIN+#18
43	VIN-#18
42	VIN+#16
41	VIN-#16
40	VIN+#14
39	VIN-#14
38	VIN+#12
37	VIN-#12
36	VIN+#10
35	VIN-#10
34	VIN+#8
33	VIN-#8
32	VIN+#6
31	VIN-#6
30	VIN+#4
29	VIN-#4
28	VIN+#2
27	VIN-#2
26	GROUND
25	GROUND
24	VIN+#23
23	VIN-#23
22	VIN+#21
21	VIN-#21
20	VIN+#19
19	VIN-#19
18	VIN+#17
17	VIN-#17
16	VIN+#15
15	VIN-#15
14	VIN+#13
13	VIN-#13
12	VIN+#11
11	VIN-#11
10	VIN+#9
9	VIN-#9
8	VIN+#7
7	VIN-#7
6	VIN+#5
5	VIN-#5
4	VIN+#3
3	VIN-#3
2	VIN+#1
1	VIN-#1

4. PERFORMANCE

4.1 Overview

This chapter provides several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Appendix A.

4.2 Timing Measurement

The performance of the ADM1224F can be presented as two major categories:

- Internal and external digital timings, including carrier accesses to information, and
- Those that directly relate to the analog circuitry and its subsequent digital representations of signals passing through this circuitry.

This latter section will be further broken up into two, major subsections:

- An analytical look at what the ADM1224F can accomplish from a worst case perspective, and
- An empirical presentation of typical accuracy and noise values.

Where possible, data is tabulated with only one response time (actual) performance figure presented to minimize the length of the presentation.

There is no single-system configuration for all of its empirical data measurements. Therefore, each new set, or sets, of related data is preceded by a short description of the system configuration used to gather the information.

4.3 Internal Digital Timing

The first group of performance data to be examined includes signals that are internal to the ADM1224F; that is, not visible at its interface connectors. This additional descriptive material supports Chapter 2 of this document. The areas of interest include the sequencing of the GRAY CODE Engine, and the serial extraction of ADC data with subsequent deposition into the CVT.

4.3.1 Hardware Configuration – GRAY CODE

The IP Module under test was specially configured to gain access to the GRAY CODE state counter bits. These bits are not present to the outside world on production units.

4.3.2 GRAY CODE Engine

Sections 2.5.1.1 and 2.7 presented details about the core engine of the ADM1224F, the seventy-state GRAY CODE Engine. Section 2.9 presented a compilation of all of the activities that take place during all of the states of this engine. Figure 5-1 presents a snapshot of slightly more than one full pass through all of the states of this engine. Note that there are only single-edge changes at any given time, the “calling card” of a GRAY CODE counter. Also note that the widths of both “GRAY5” and “GRAY6” are not

proportional to those of the other five, lower significant bits. This phenomenon is a result of the truncated sequence (70 states instead of 128).

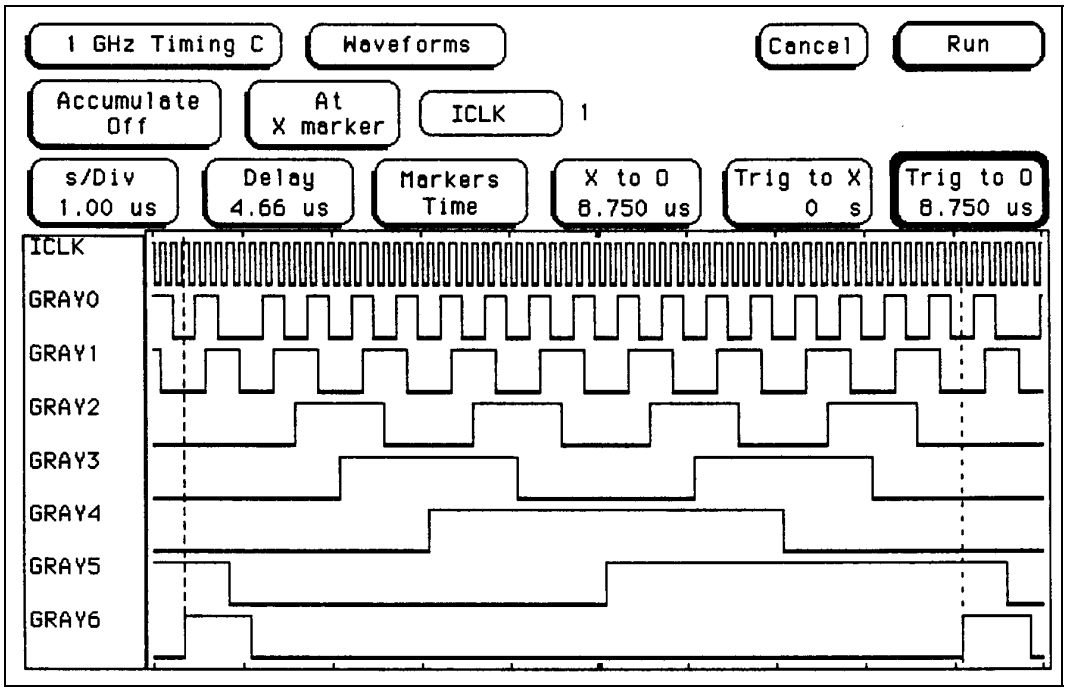


Figure 4-1 GRAY CODE Engine Full Pass

The full pass through all seventy states takes 8.750 µs, and eight passes captures all twenty-four channels in 70 µs. Captured waveforms indicate that all state transitions occurred within 5 ns to 6 ns of the rising edge of ICLK. Being a fully synchronous engine, engine-state-dependent events occur at the end of a count where the system conditions, including the counter's current state, are stable and waiting for the rising edge of the ICLK to perform the next task.

4.3.3 Hardware Configuration - ADC Data

1-inch wires were connected for, and at:

"CLKA"	@ U8 pin 4
"SDA"	@ U8 pin 5
"CTRLA"	@ U8 pin 7
"CLKB"	@ U10 pin 4
"SDB"	@ U10 pin 5
"CLKC"	@ U12 pin 4
"SDC"	@ U12 pin 5
"SRAMD0"	@ U4 pin 11
"SRAMD1"	@ U4 pin 12
"SRAMD2"	@ U4 pin 13
"SRAMD3"	@ U4 pin 15
"SRAMD4"	@ U4 pin 16
"SRAMD5"	@ U4 pin 17
"SRAMD6"	@ U4 pin 18
"SRAMD7"	@ U4 pin 19
"N_SRAMWE"	@ U4 pin 27.

The ADM1224F was remounted as in section 4.3.1 and the same analyzer was connected.

The “CLKA,” “CLKB,” and “CLKC” signals are the serial shift clocks used to extract data from the ADC’s @ U8, U10, and U12, respectively. The “SDA,” “SDB’, and “SDC” signals are the serial data lines from the ADC’s. The “CTRLA” signal is the conversion control line for ADC#A. On the third figure following, it is referred to as “N_CNVS” (N_CONVST). “SRAMD[7:0]” are the data lines that define the low byte of the parallel SRAM data bus that provide the results from the serial-to-parallel conversion process just prior to the writes to the CVT. The asserted low “N_SRAMWE” signal (SRAM write enable) appears on the next two figures as “SRAMWE”.

4.3.4 ADC Data Movement

Sections 2.6.3 and 2.7 textually presented the activities that take place during the seventy states of the GRAY CODE Engine. Most of this activity involves the serial extraction of ADC data with parallel-to-serial conversion and subsequent deposition of data into the CVT in round-robin fashion through all three ADC’s. Figure 4-2 clearly depicts this activity.



NOTE: For readability of Figure 4-2, the leading “F” in parallel data 0xFF3 and parallel data 0xFFB has been omitted.

The left portion of this diagram depicts the serial extraction of data from ADC#B with a CVT write of 0xFF3, followed by the same process for ADC#C with write of 0x000, and the same for ADC#A with a CVT write of 0xFFB. While the leading “F”s are not included in the parallel data being written to the CVT for ADC#B and ADC#A, they are obvious when the serial data streams are examined. The actual write of data occurs on the rising edge of “N_SRAMWE.” Since all three of the writes to the CVT are uncontested, they all occur during their first-opportunity states, during GRAY CODE states 0x3F, 0x61, and 0x1A for converters #B, #C, and #A, respectively. More details are available about these events in section 2.6.2.

Figure 4-3 presents a zoom-in view of the ADC#B’s data capture activity presented in Figure 4-2. Rising edges of ICLK actually capture the serial data present on SDB, with the bit stream of 1, 1, 0, 0, 1, 1 in full view. Notice that the write to the CVT occurs 8 ns following the rising edge of its synchronous clock ICLK.

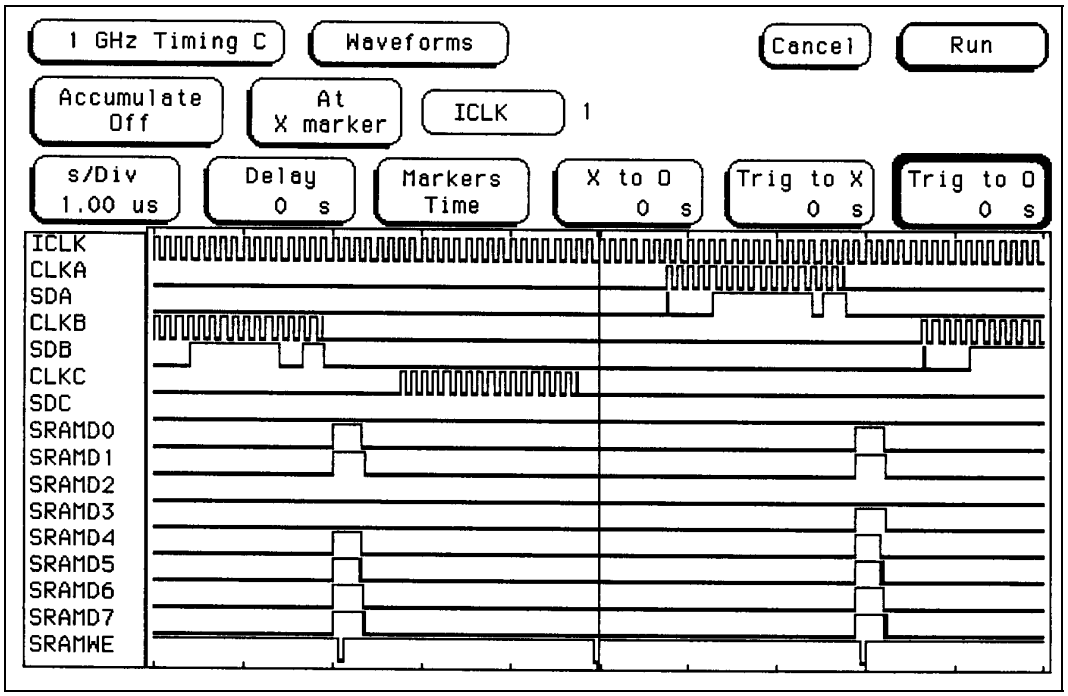


Figure 4-2 Round-robin Overview

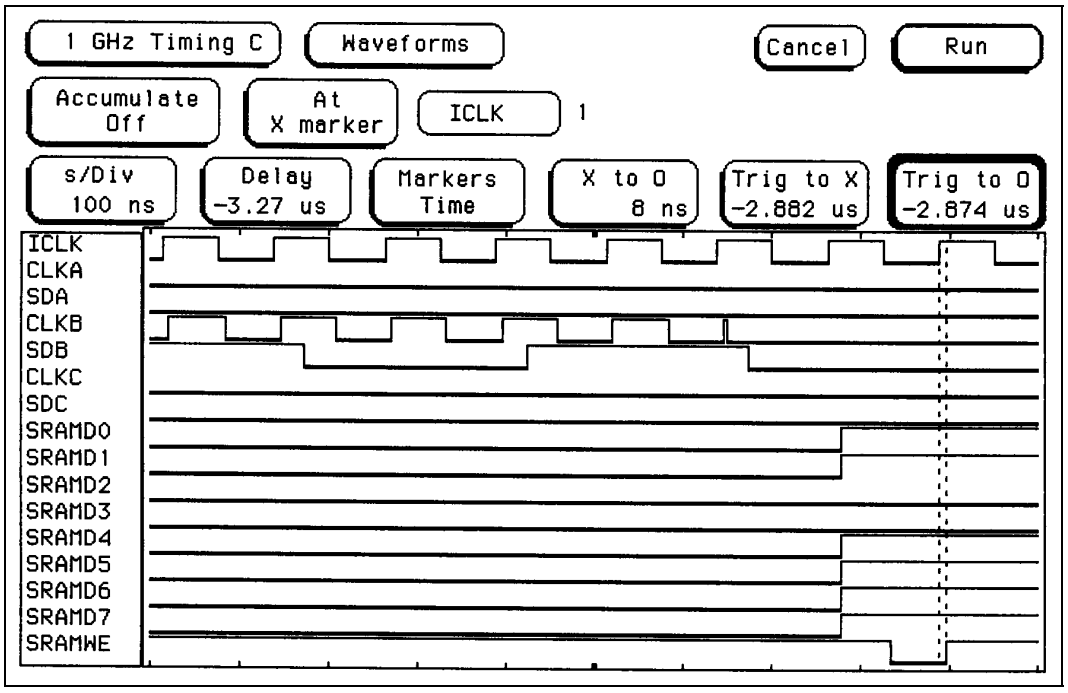


Figure 4-3 ADC Data Capture Detail

4.3.5 Converter Control

Most of the GRAY CODE engine generated activity has been explored to this point. One area that has not been depicted yet is the actual control signals for the ADC's. The hardware configuration was presented in section 4.3.3. Figure 4-4 presents a detailed look at the actual control of ADC#A. Note that the figure's "N_CNVS" is actually the control line "CTRLA," the asserted low conversion start signal.

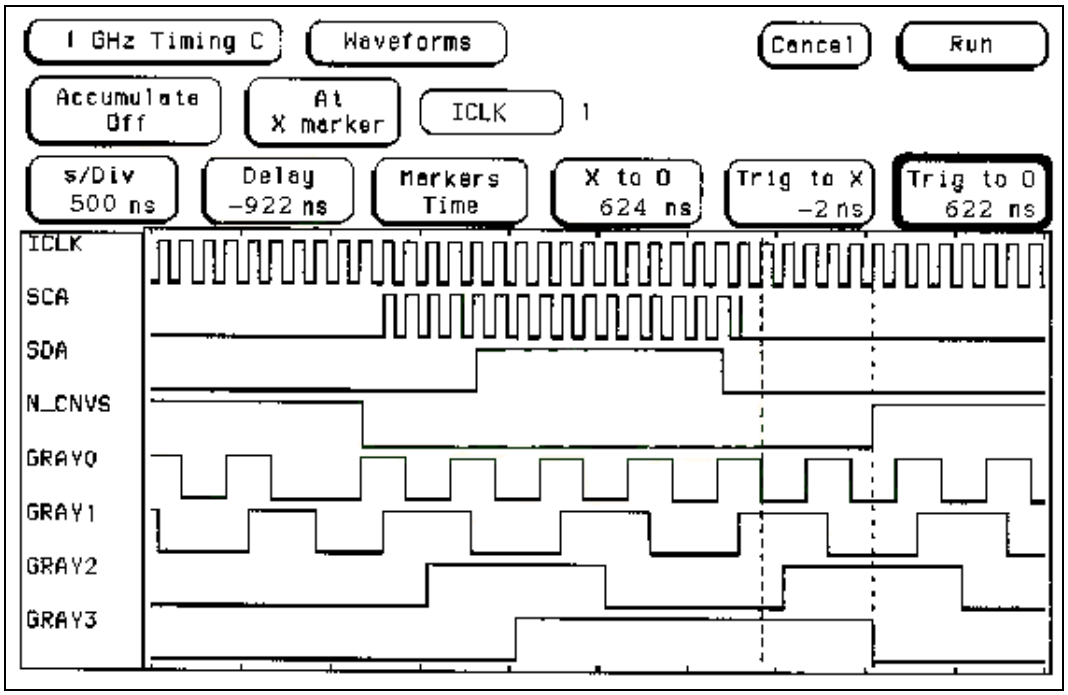


Figure 4-4 ADC Control Details

The ADC's signal acquisition and start of conversion process is controlled by the N_CONVST (CTRLA) signal. The falling edge of this signal resets the ADC's internal counters and registers, while the rising edge changes the front-end analog configuration from track to hold mode and starts the conversion process. The ADC's are self-clocked during the actual conversion process, and they go into track mode automatically following the conversion process, just prior to the first rising edge of SCA in Figure 4-4.

The actual tracking time ≈ 2.75 μs (22 ICLK cycles preceding the rising edge of N_CONVST), while the circuitry acquires the input signal to 12-bit accuracy in less than 1.5 μs. The aperture time (track mode to hold mode) is typically 15 ns.

The depicted width of N_CONVST is 2875 ns, while the ADC's specification calls for a minimum of 600 ns. The four rising edges of ICLK between the markers (X to 0) is where the write to the CVT takes place. It occurs once during this window of opportunity, and on the first rising ICLK edge if no contention to the CVT resources is encountered.

The least significant four bits of the GRAY CODE engine count are included with this figure for comparison purposes with Table 2-1. The GRAY CODE state just prior to the rising edge of the ICLK that causes the fall of N_CONVST is count #0x00. The GRAY CODE state just prior to the rising edge of the ICLK that causes the rise of N_CONVST is count #0x1C. The four counts in between, #0x1A, #0x1E, #0x1F, and #0x1D, are states where the N_SRAMWE pulse can occur. It was triggered to occur by state #1A in Figure 5-3 since the CVT was not being read by the carrier.

4.4 Carrier Accesses

The next group of performance data to be examined includes digital-level signals that interface the ADM1224F to its carrier. This information provides the user with empirical data on how fast the carrier can retrieve I/O and ID data from the ADM1224F.

Simulations have demonstrated that a carrier that has the capability of performing back-to-back transfers with no idle cycles, if such a machine existed, could do so when retrieving data from the ADM1224F.

The following information provides typical access information for I/O reads and ID reads. Actual attempts to write to both regions resulted in the expected non-acknowledgements and their resultant bus timeouts.

4.4.1 Hardware Configuration – Carrier Accesses

ADM1224F#114 was mounted on a VMESC5 (5-slot VME-6U slave carrier) in slot A using a Type 1 IP Module Logic Bus Extender Board under the ADM1224F. The carrier's base address configured the IP Module's I/O addresses for a start at address 0xFFFF2000. A 2-inch extender cable was connected between the extender and an IP Module Logic Bus Breakout Board where all of the connections to signals and ground references were made. All timing information was captured using an HP 1 GHz Timing Module Model 16515A in a 16500A Logic Analysis System chassis.

4.4.2 IP Module Transfers

This short section presents the typical timing data for the only two transfer types that the ADM1224F IP Module supports: I/O reads and ID reads. Table 4-1 tabulates the data and Figure 4-5 presents a typical I/O read (@ IPA = 00, IPD = 003). The I/O read's IPDbus data setup time ≈ 207 ns, while for the ID read it ≈ 116 ns.

Table 4-1 Carrier Accesses Typical Times

Transfer Type	↑ **ICLK until:**	TIME (ns)
I/O Read (IPA = 00)	↓ N_ACK	10
	↑ N_ACK	10
ID Read (IPA = 00)	↓ N_ACK	11
	↑ N_ACK	9

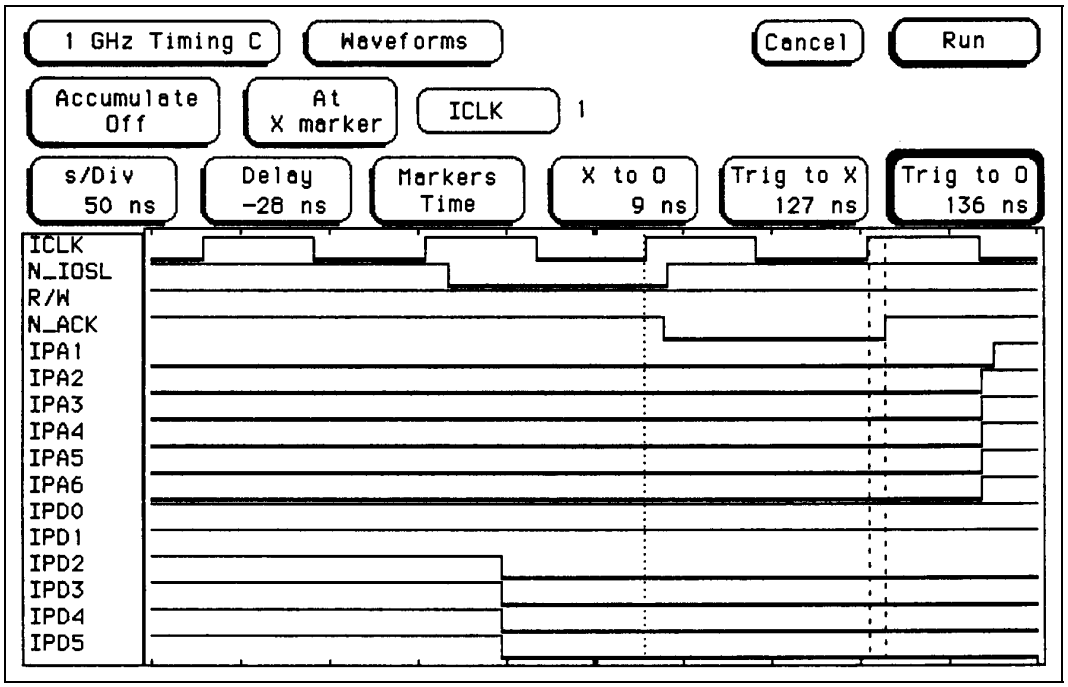


Figure 4-5 Typical I/O Read Timing

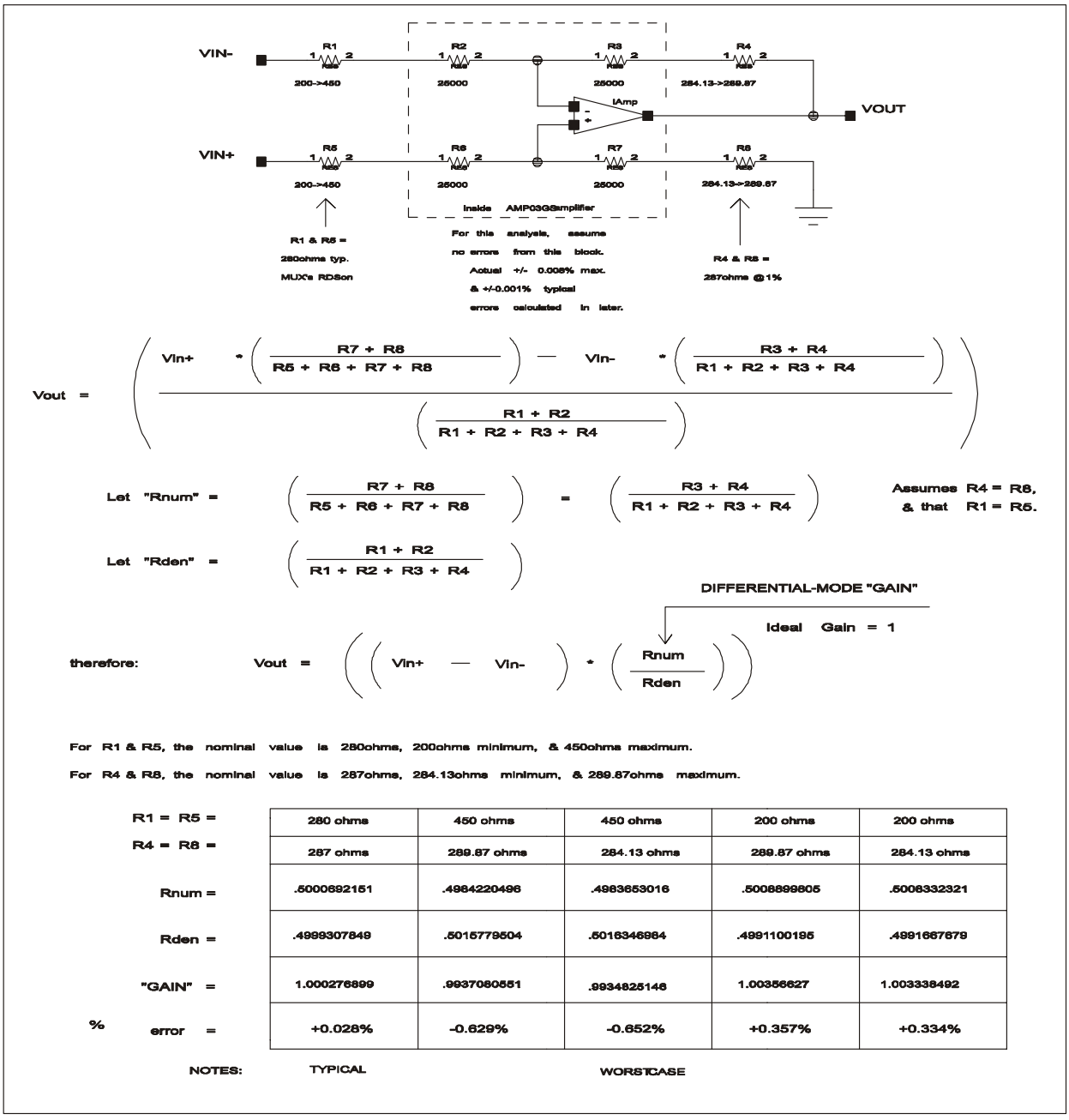
4.5 Theoretical Accuracy

This short subsection attempts to provide an analytical determination of the worst-case errors that could reduce the accuracy of the ADM1224F. It uses the square-root-of-the-sum-of-the-squares technique, and covers both gain and offset contributions to overall inaccuracies. Since these include theoretical worst-case margins for most of the components used in the analog section, the statistical probability of having all components exhibiting worst-case errors is slight.

The analysis is contained within the next three figures. Figure 4-6 and the top half of Figure 4-7 attempt to determine the worst-case gain errors for the analog "front-end" consisting of the analog multiplexers and their associated differential amplifiers. This is conducted in two steps:

- First, the amplifier is assumed to have no gain errors and the error contribution from the multiplexer and two "gain" resistors is determined.
- Then the worst-case specification for the amplifier is factored into the analysis.

The bottom half (below the triple horizontal lines) of Figure 4-7 then includes gain errors from the ADCs and their voltage reference. The result of this gain error analysis is that the worst-case error = 0.769%.



R1 = R5 =	280 ohms	450 ohms	450 ohms	200 ohms	200 ohms
R4 = R8 =	287 ohms	289.87 ohms	284.13 ohms	289.87 ohms	284.13 ohms
Rnum =	.5000692151	.4984220496	.4983653016	.5008899805	.5008332321
Rden =	.4999307849	.5015779504	.5016346984	.4991100195	.4991667679
"GAIN" =	1.000276899	.9937080551	.9934825148	1.00356627	1.003338492
% error =	+0.028%	-0.629%	-0.652%	+0.357%	+0.334%
NOTES:	TYPICAL		WORSTCASE		

Figure 4-6 Front-end Gain Error Analysis

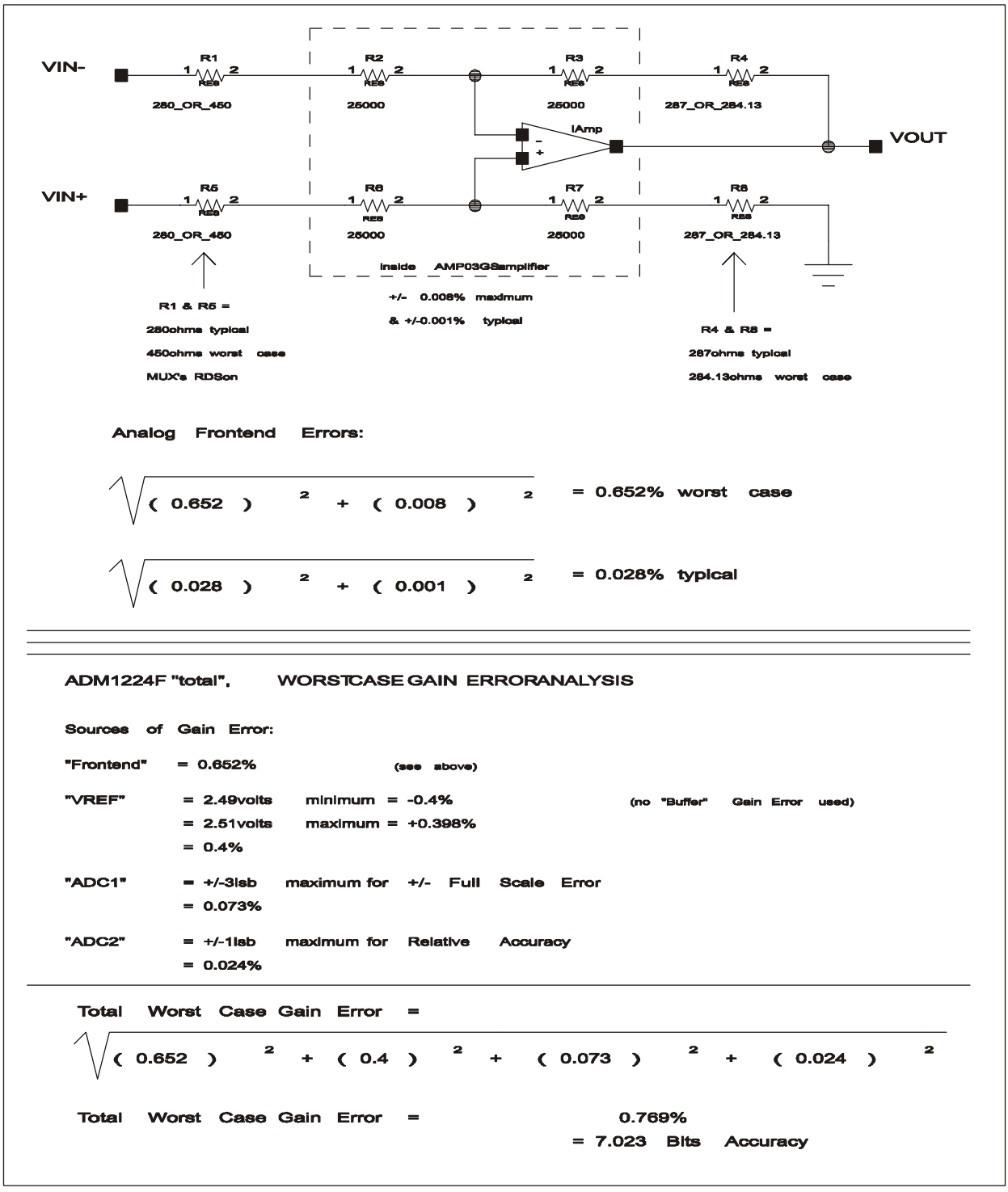


Figure 4-7 Overall Gain Error Analysis

The top half of Figure 4-8 (above the triple horizontal lines) presents a worst-case analysis of significant errors due to offsets. These do not include any offset errors that may be induced due to poor grounding techniques. The bottom half of Figure 4-8 is the final combination of all worst-case gain and offset errors for this analysis. All of the margins and values used in this analysis are data sheet parameters for units operating within voltage specifications and at 25°C.

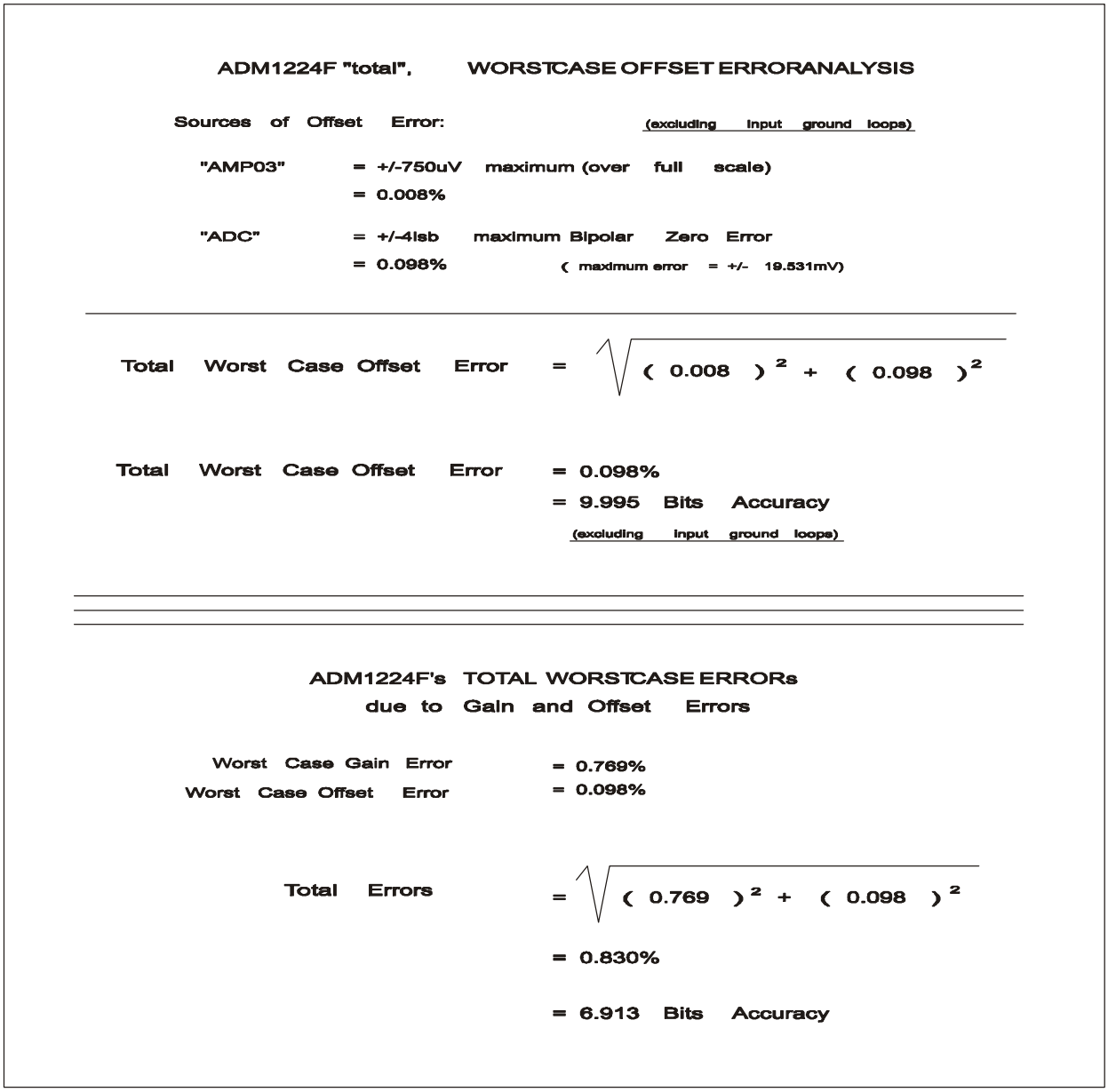


Figure 4-8 Offsets and Total Error Analysis

4.6 Typical Empirical Performance

This section presents data that represents a sampling of the DC accuracy and noise performance of the ADM1224F. The data shown is for one ADM1224F out of five that were tested. The data is however, typical of all five test units.

4.6.1 Test Configuration

The ADM1224F was tested in its single ended (S.E.) configuration using a precision DC voltage source as stimulus. Each input channel was sampled 10,000 times in order to average out noise. Tests were performed with input voltages of +9.900, 0.000, and -9.900 volts. The Maximum (MAX), Average, Minimum (MIN), and Standard Deviation (STD DEV) was computed over 10,000 samples for each input voltage. No corrections were made to the gain and offset errors of the ADM1224F.

4.6.2 Data Results

Figure 4-9 shows the results of the sampled +9.900 input voltage. The first observation that can be made is the error between the actual input versus the sampled voltage. The overall average across all 24 channels is +9.9326 volts. This represents a .33% or 6.7 LSBs (1 LSB = 4.883 mV) error and is attributed to the gain and offset error of the ADM1224F. Channel 11 had the greatest deviation from the group of 24 but was closer to the actual input voltage. This is attributed to the variation in the series ON resistance of each of the MUX input channels. Since the Instrumentation Amp used in the ADM1224F has relatively low input impedance any variation in the input MUX series ON resistance will affect the gain, and therefore accuracy, for that particular channel. As a result, a source that has a relatively high resistance will also affect the accuracy of the ADM1224F. The second observation is the noise represented by the MIN/MAX data and the STD DEV shown in Figure 4-10. The channels with the worst-case peak-to-peak noise were channels 12 and 14. Each had a measured noise of 58.6 mV or ± 6 LSBs. This translates to approximately 2 LSBs rms noise. Channel 17 had the worst case STD DEV of 1.72 LSBs.

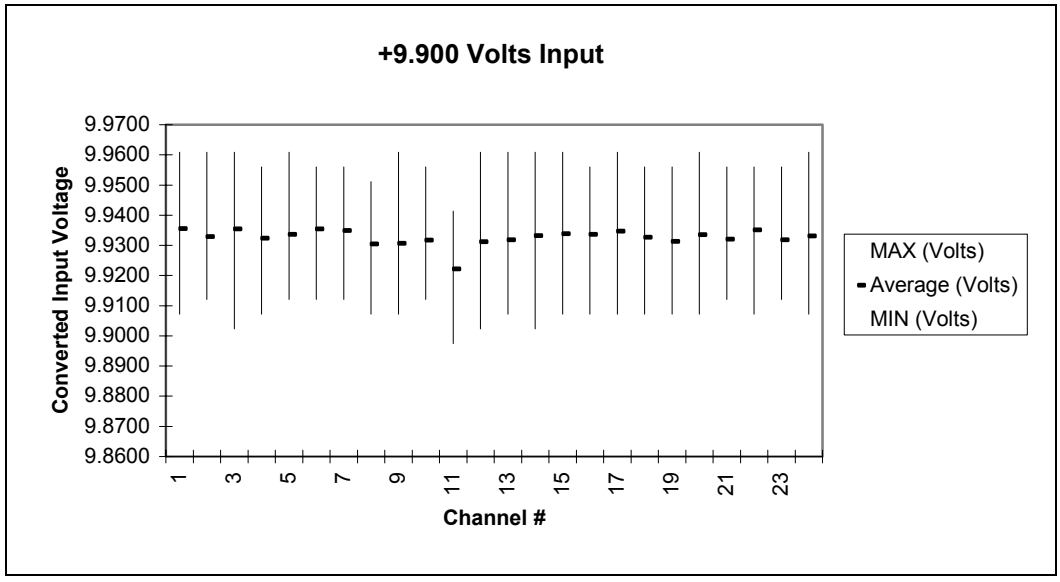


Figure 4-9 MIN/Average/MAX of all 24 Channels w/+9.900 Volt Input

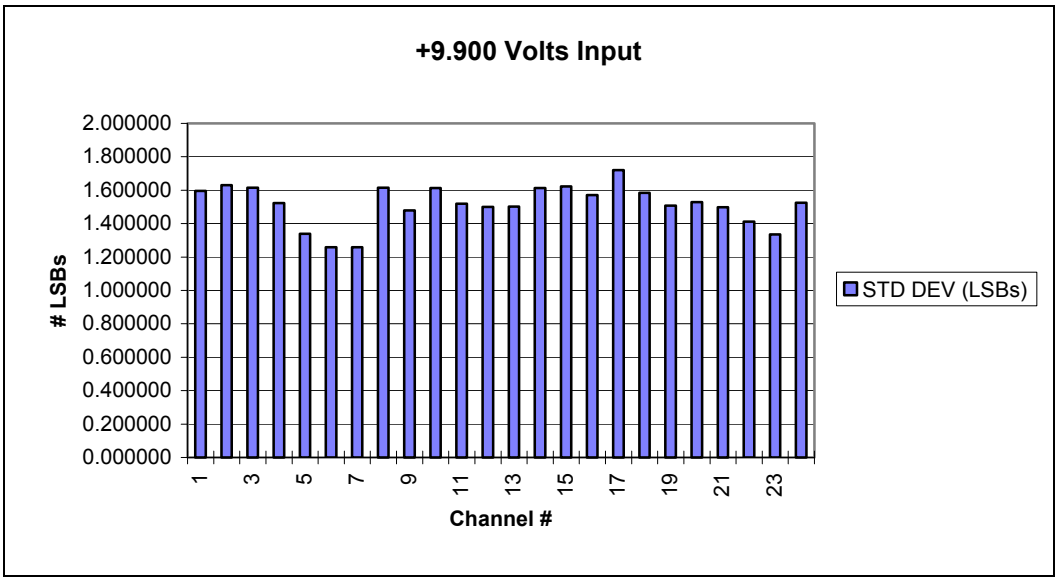


Figure 4-10 Standard Deviation of all 24 Channels w/+9.900 Volt Input

Figure 4-11 shows the MAX/Average/MIN data for a 0.000 V input. The average voltage for all channels is -0.0104 V or approximately -2 LSBs. This is due to the offset voltage of the Instrumentation Amp and the ADCs. As can be seen by the Average values and the STD DEV shown in Figure 4-12 all channels track very close to each other. The maximum STD DEV was 1.14 LSBs for channel 24 and the minimum STD DEV was 0.68 LSBs for channel 8. Measured worst-case noise (appeared on multiple channels) was 39 mV peak-to-peak or ± 4 LSBs that equates to approximately 1.3 LSBs noise rms.

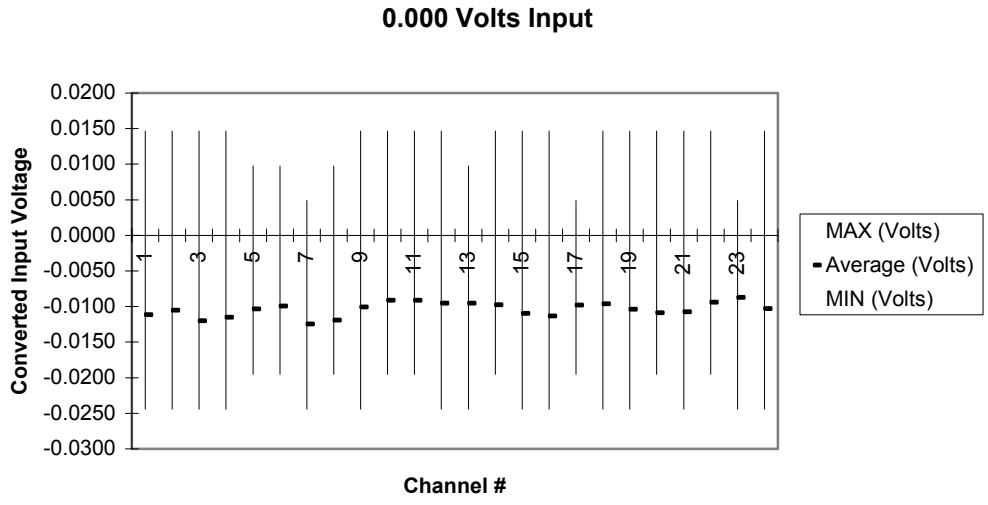


Figure 4-11 MIN/Average/MAX of all 24 Channels w/0.000 Volt Input

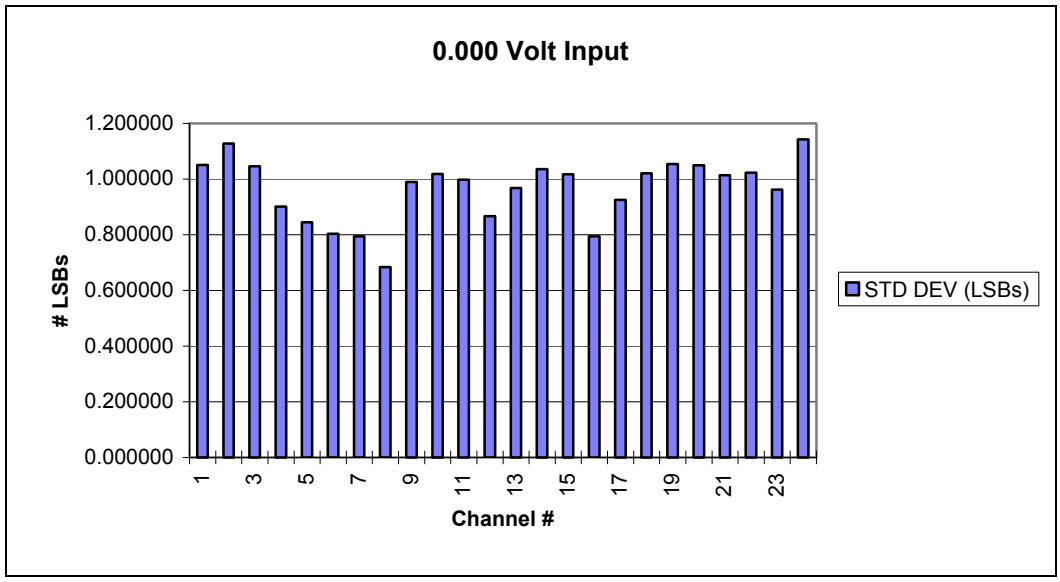


Figure 4-12 Standard Deviation of all 24 Channels w/0.000 Volt Input

Figure 4-13 shows the MAX/Average/MIN data for a -9.900 volt input. The average voltage for all channels is -9.9296 V, which is approximately -.3 % or -6 LSBs error. This is due to the offset voltage and gain error of the ADM1224F. All channels track very close to each other with the exception of channel 11. This is consistent with the data shown for the +9.900 input voltage and is also attributed to the difference in the series ON resistance of the input MUX. The STD DEV, as shown in Figure 4-14, range from 0.78 LSBs on channel 11 to 1.01 LSBs on channel 24. Measured worst-case noise was 34 mV peak-to-peak or ± 3.5 LSBs, which equates to approximately 1.2 LSBs noise rms.

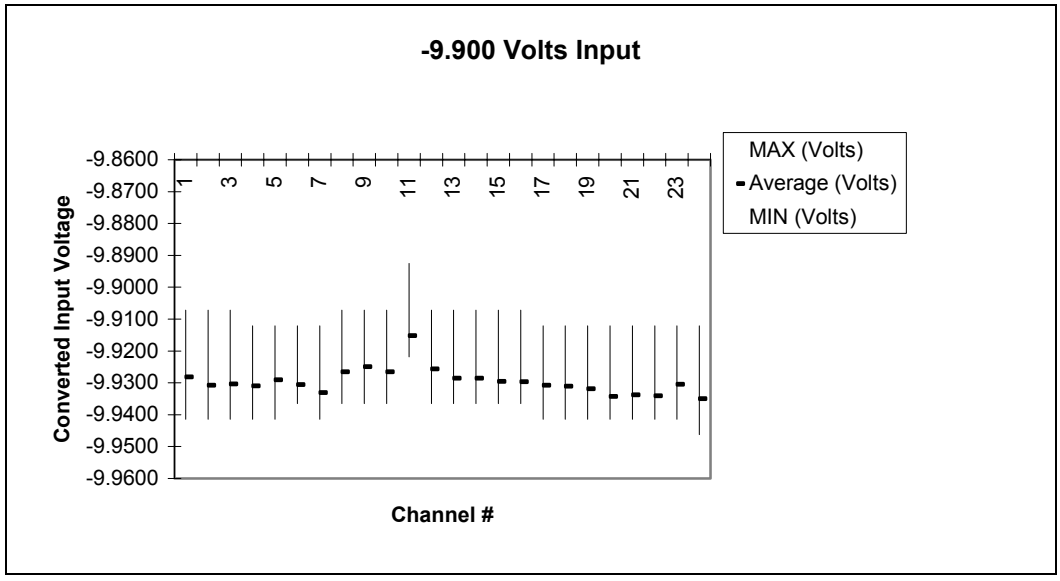


Figure 4-13 MIN/Average/MAX of all 24 Channels w/-9.900 Volt Input

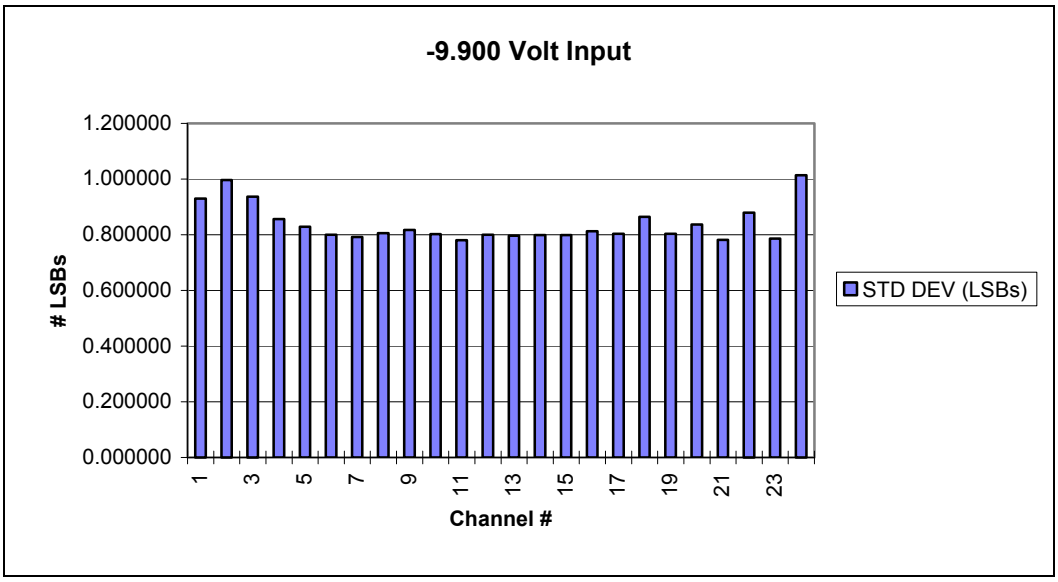


Figure 4-14 Standard Deviation of all 24 Channels w/-9.900 Volt Input

APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements.....1.800 inches x 3.900 inches x 0.303 inches (connectors, above board), 4.572 cm x 9.906 cm x 0.770 cm



NOTE: 0.234″ (0.595 cm) maximum component (non-connector) height.

Weight .....1.104 oz., 31.3 grams
Board thickness .....0.062 inches, 0.157 cm, nominally, (4 layer)

PROTOCOL

Clock rate .....8 MHz
Wait cycles .....None on any transfer types
Hold cycles.....Supported on all valid transfer types



NOTE: A maximum of two hold cycles is supported for updates of the CVT.

Address decoding .....Complete (no partial)
I/O Locations.....24, 16-bit read-only, byte-lane selects ignored
No writes

- ADC data..... IPD[11:0]
- Frame Counter data ..... IPD[15:12]
- Interrupt Control/Status 6
- Maximum read/write rate.....4 MTransfers/second, sustained
- Acknowledgement..... None for IPA≥ 0x18 or for any write attempts

ID Locations.....Twelve, 16-bit read-only, byte-lane selects ignored
No writes

- ID Data ..... IPD[7:0]
- Zero-fill..... IPD[15:8]
- Systran's manufacturer's ID .....0x45 = **E** ASCII
- DIO316I's model number .....0x6F = **o** ASCII
- Cyclic Redundancy Check value 0xCD
- Maximum read rate.....4 MTransfers/second, sustained
- Acknowledgement..... None for IPA ≥ 0x0C or for any write attempts

Memory Transfers .....Not supported, no acknowledgements
Interrupt Vector transfers.....Not supported, no acknowledgements
Interrupt requests.....None generated
DMA activity.....Not supported
End-of-frame: .....≈63 ns pulse every 70 µs at N_STROBE on Logic Connector

Power-up Default Condition

Accesses	None permitted or acknowledged during RESET
Control Logic	frozen, and all counters zeroed, during RESET
Data	Not accurate to specification until after ≈25 ms following application of power



NOTE: First ADC data entries for channels #1, #9 and #17 following the negation of RESET are indeterminate; valid entries for these channels completed 78.750 µs after the negation of RESET.

AS-SHIPPED CONDITION

Channels	All 24 channels configured as single-ended inputs. Channel #24 connected to the I/O Connector; not to the voltage reference

POWER REQUIREMENTS

Carrier Power:	+5 Vdc @ 114 mA (all inputs grounded) +12 Vdc @ 9.10 mA (all inputs grounded) -12 Vdc @ 7.79 mA (all inputs grounded) Total: 204 mW
I/O Connector:	Analog (ground) reference common to all analog circuitry; tied to the digital ground on the carrier side of the Logic Connector only (pins 25 and 50) No other I/O Connector power requirements exist

PERFORMANCE CHARACTERISTICS

Accuracy and Timing	Refer to Chapter 4, PERFORMANCE
Input Impedance (per channel):	Vin+ (Vin- grounded): 50594 Ω, nominal (single-ended configuration) Vin- (Vin+ grounded): 25297 Ω, nominal (inverting single-ended configuration) Differential-ended: 50594 Ω, nominal
MUX (analog):	Analog signal range ±12.000 V
RDS_{ON}	280 Ω (typical @ 25°C), 400 Ω (maximum, over temperature)
RDS_{ON} match	5% (typical)
I_S	0.02 nA (OFF, typical input leakage), 50 nA (maximum, over temperature)
I_D	0.04 nA (OFF, typical input leakage), 100 nA (maximum, over temperature)
I_D	0.04 nA (ON, typical input leakage), 100 nA (maximum, over temperature)
I_{DIFF}	25 nA (maximum, over temperature)
Q_{INJ}	4 ρC (typical @ 25°C)

Maximum continuous current,
Source or drain:.....20 mA (must be externally limited if overvoltage conditions are possible)

IAMP (analog):
Offset voltage.....25 µV (typical @ 25°C), ±2000 µV (maximum, over temperature)
Gain error.....0.001% (typical, full scale, @ 25°C), 0.02% (maximum, full scale, over temperature)
CMR .....80 dB (minimum @ 25°C), 90 dB (typical, over temperature)
Slew Rate .....6 V/µs (minimum @ 25°C), 9.5 V/µs (typical, over temperature)
PSRR.....0.7 µV/V (typical @ 25°C), 15 µV/V (maximum, over temperature)

ADCs (analog):
Signal-to-noise (distortion) Ratio .....70 dB minimum for 10 kHz Sine wave input
Effective Number of Bits.....11.33
Total Harmonic Distortion.....-80 dB maximum for 10 kHz Sine wave input
Peak Harmonic Distortion .....-80 dB maximum for 10 kHz Sine wave input
Intermodulation Distortion .....-80 dB maximum for both 2nd and 3rd order terms (F*a*=9 KHz and F*b*=9.5 KHz)
Minimum resolution .....12 bits with no missing codes, guaranteed
Relative accuracy.....±½ LSB (typical), ±1 LSB (maximum)
Differential nonlinearity.....±1 LSB (typical and maximum)
Positive full-scale error.....±1½ LSB (typical), ±3 LSB (maximum)
Bipolar zero (offset) error.....±2 LSB (typical), ±4 LSB (maximum)
Negative full-scale error .....±1½ LSB (typical), ±3 LSB (maximum)
Input voltage range .....±10 V referenced to "AREF"
Input resistance .....33 KΩ (typical), 16 KΩ (minimum)
1 LSB.....20 V ÷ 4096 ≈ 4.88 mV

REFERENCE (analog):
Output voltage.....+2.500, ±0.010 V (maximum, over temperature)
Output voltage drift.....10 ppm/°C (typical), 25 ppm/°C (maximum)
= 1.75 mV (typical), 4.375 mV (maximum, over temperature)
Output settling time .....25 ms to within 250 µV of final value after application of power

ABSOLUTE MAXIMUM VOLTAGES‡

Carrier power supplies:
+5 Volt supply with respect to ground: -0.3 V (minimum), +7.0 V (maximum)
+12 Volt supply with respect to ground: ≤ +18.0 V
-12 Volt supply with respect to ground: ≥ -18.0 V
VIN± input range:..... ±17 V (maximum if ±18.0 V is supplied by the carrier)

	±12 V (maximum if ±12.0 V is supplied by the carrier)
CMS	±10 V (maximum, over temperature)

‡ *Stresses above those listed may cause permanent damage to the components on the ADM1224F. Operating the ADM1224F beyond the recommended ratings for extended periods of time may affect reliability.*

MAXIMUM INPUT BANDWIDTH

No signal energy ≥ -72 dB in amplitude at frequencies ≥ 7142 Hz to prevent aliasing errors (for single sampling per frame). Signals can be supercommutated using even "time" spacing techniques to acquire higher bandwidth signals, to a limit of a maximum frequency of 171.428 KHz (all 24 channels sampling a single signal source; input impedance ≈ 16,865 Ω)

RECOMMENDED OPERATING CONDITIONS

Carrier Supply Voltages	+5.00, +0.25/-0.125 V, 50 mV maximum peak-to-peak ripple and noise +12.0, +0.60/-0.36 V, 50 mV maximum peak-to-peak ripple and noise -12.0, -0.60/+0.36 V, 50 mV maximum peak-to-peak ripple and noise
Input Signals	±10.000 V 7142 Hz (maximum frequency, fundamental and harmonics)

Recommended carriers: (for "quiet" operations)

- Systran's VME3SC2 for VME-3U
- Systran's VMESC5 for VME-6U
- Systran's ISASC6 for ISA (PC's)
- Systran's CPCISC4 for CPCI
- Systran's PCISC5 for PCI (PC's)

ENVIRONMENTAL SPECIFICATIONS

Temperature (Operating):	0°C to +70°C
Temperature (no bias, storage):	-40°C to +85°C
Humidity (Non-condensing):	5% to 95%
Vibration (Operating):	10 G's RMS, 20→2000 Hz, random (no jumper shunts installed)
Shock (Operating):	50 G's maximum, all axes (no jumper shunts installed)
Altitude (Operating):	10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MTBF	1,013,885 hours per MIL-HDBK-217F

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

TABLE OF CONTENTS

B.1 Overview B-1
B.2 Deterministic Sampling Matrix B-1
B.3 Supercommutation B-5
B.4 Differencing Inputs B-7
B.5 DAC Monitors B-8
B.6 ENDOFRAME strobe B-8

FIGURES

Figure B-1 Sequential Sampling Timing B-2
Figure B-2 Left Half Of Full Timing Matrix B-3
Figure B-3 Right Half Of Full Timing Matrix B-4
Figure B-4 ENDOFRAME “strobe” Pulse B-9

TABLES

Table B-1 Input Impedances by Type and Groupings B-6
Table B-2 Supercommutation Rates/Times B-7
Table B-3 Differencing Results B-8

B.1 Overview

Systran extends an open invitation to all users to freely submit their applications that use the ADM1224F IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 Deterministic Sampling Matrix

Section 2.6.3 provided detailed information about the sequential sampling timing, while section 2.6.4 provided some examples of determining the exact amount of time between any two samples given their channel numbers and the value of the samples' frame-counter nibbles. This subsection provides, in tabular/matrix format, the technical information that was consulted for the development of sections 2.6.3 and 2.6.4.

Figure B-1 diagrammatically presents the information supplied in section 2.6.3. There are eight groups of three channels separated by dashed lines. The first sample of each group is that acquired through the "A" section of circuitry for channels 1 through 8. The second sample of each group is that acquired through the "B" section of circuitry for channels 9 through 16. The third sample of each group is that acquired through the "C" section of circuitry for channels #17 through #24. The delta time between "A" channels and "B" channels is 2.875 µs. The delta time between "B" channels and "C" channels is 2.875 µs. The delta time between "C" channels and "A" channels is 3.000 µs. The extra 125 ns in the latter timing is due to the addition of the seventieth GRAY CODE sequence state to maintain single-bit transitions through the count sequence.

The SADD# column in Figure B-1 provides the "SRAM Address" value of the CVT, in hexadecimal, where the ADC data is stored. These are the same addresses used by the carrier for retrieving CVT data, as driven by IPA[6:1].

The far right column of Figure B-1 provides summation aggregate timing for all channels referenced to channel #1. For example, the elapsed time between the sampling of channel #1 until channel #6 is sampled is 43.750 µs. The time between channel #1's sampling and the capturing of channel #4 in the next frame (as defined by the frame counter values) is 26.250 µs + 70.000 µs for the additional frame. Refer to section 2.6.4 for additional examples.

While Figure B-1 works fine for timings referenced to channel #1, this is not a complete look at all possibilities. A full matrix, of course, would be twenty-four columns wide and twenty-four rows deep. Such a matrix is presented in Figure B-2 and Figure B-3. The reference channel is that defined by the column, as read across the top of the matrix. The second channel's timing with respect to the reference channel is found in the left margin, read from top to bottom.

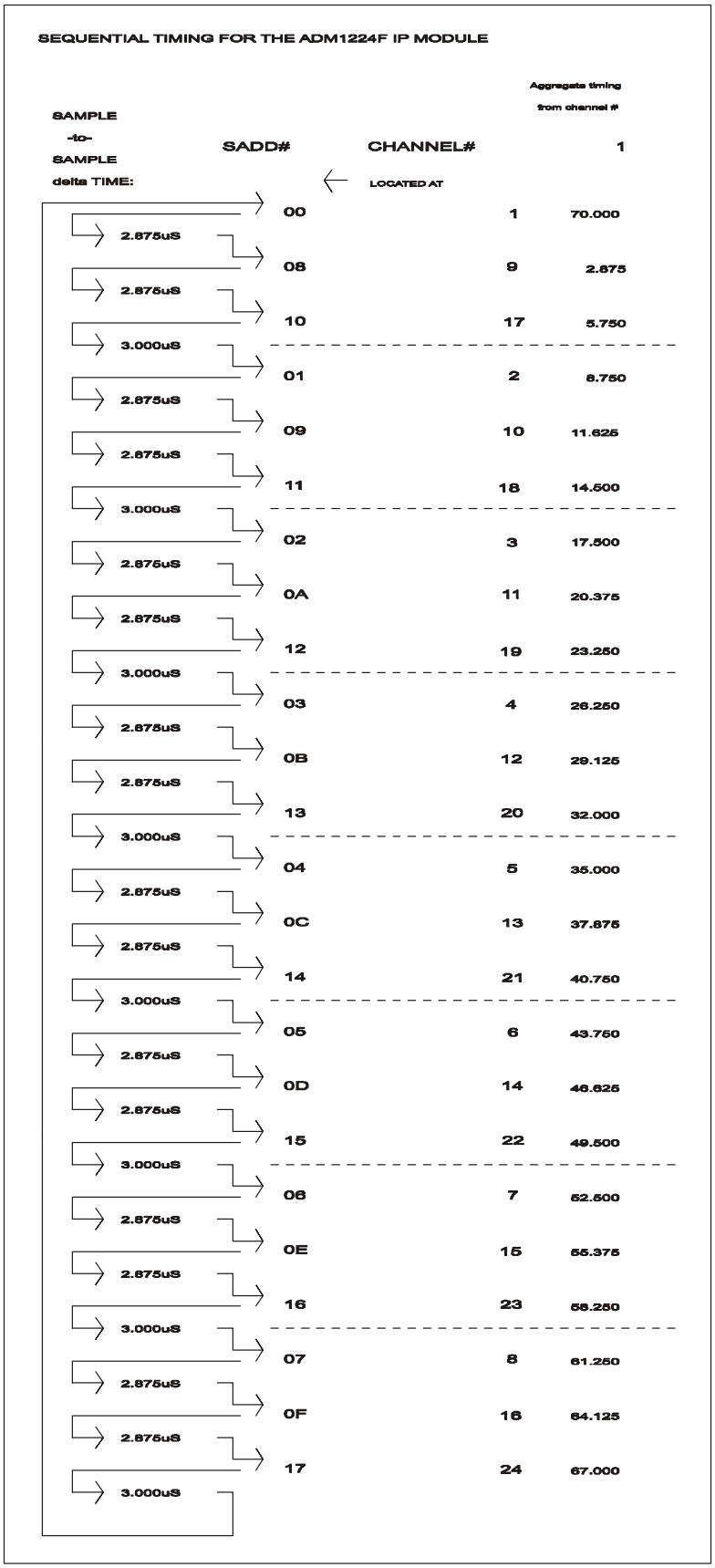


Figure B-1 Sequential Sampling Timing

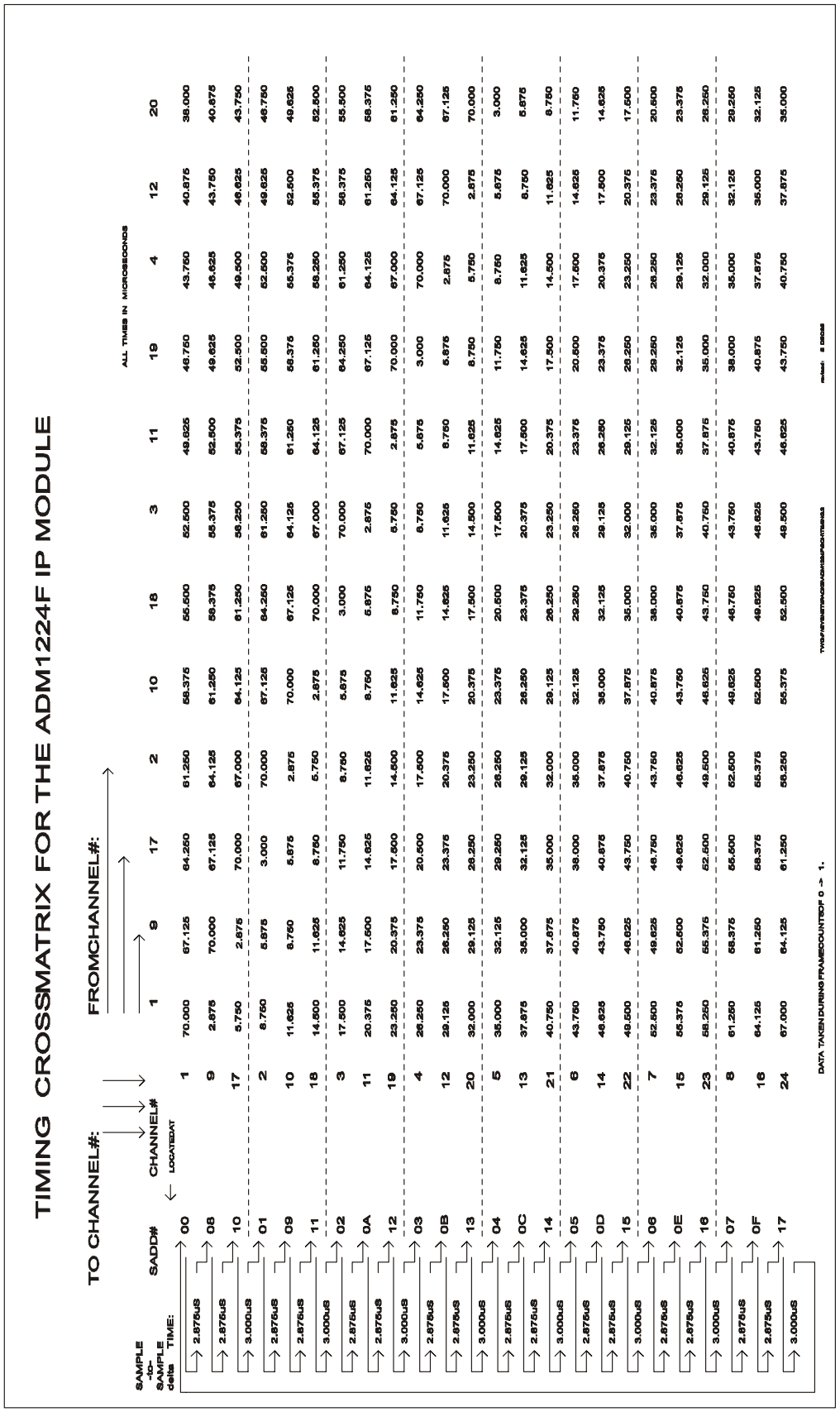


Figure B-2 Left Half Of Full Timing Matrix

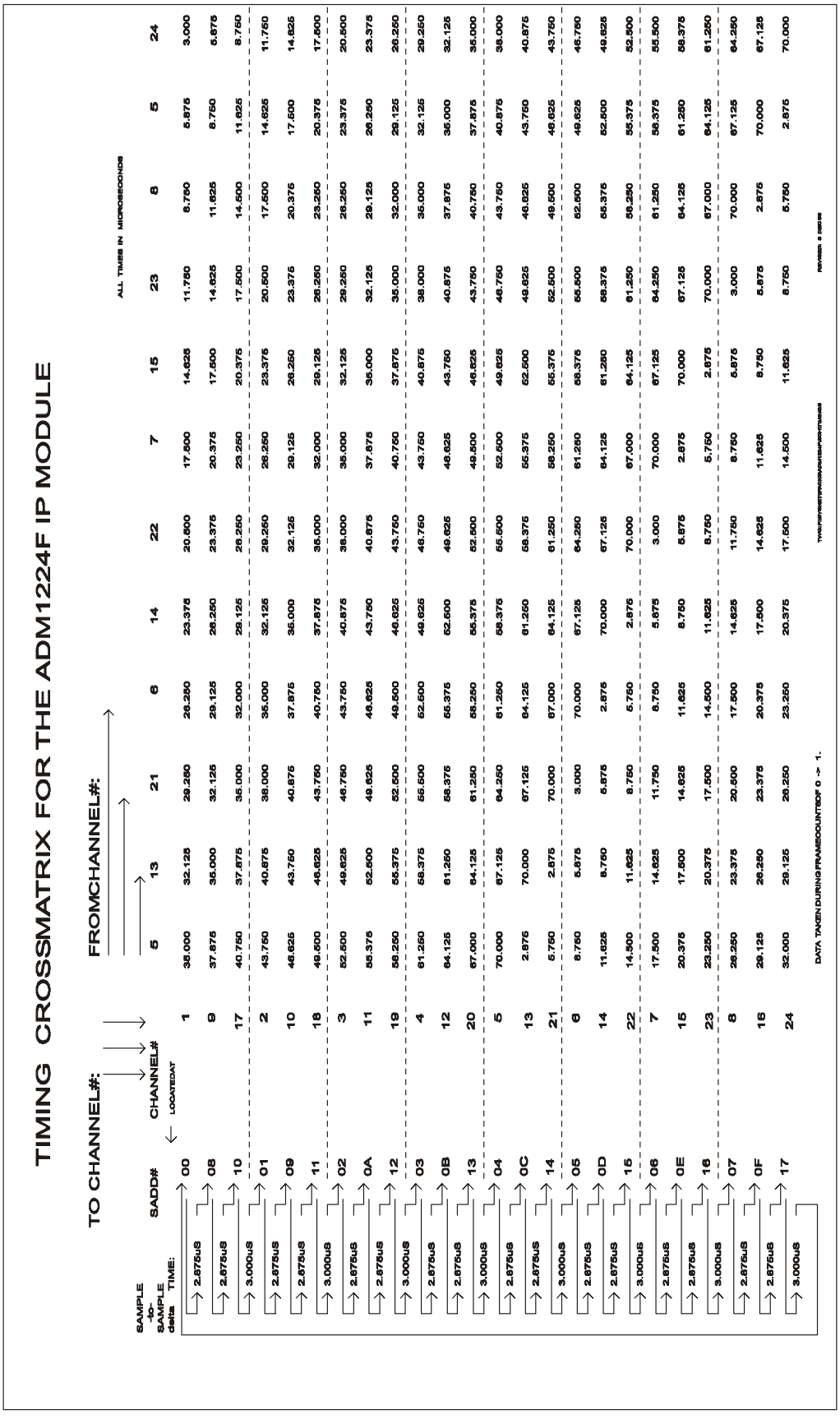


Figure B-3 Right Half Of Full Timing Matrix

Instead of providing detailed steps on how section 2.6.4 was developed, a couple of new examples are provided below for determining exact sampling timing relationships. At this point it is important to reiterate (from section 4.2.5) that the aperture time is typically 15 ns, which is the uncertainty for these timing relationship examples.

Order of sampling is important. The time between sampling channel #18 and then sampling channel #7 is 38.000 µs, while the time between sampling channel #7 and then sampling channel #18 is 32.000 µs. Note that the summation of the two equals a full frame of 70.000 µs. Refer, first, to Figure B-2. Across the top, moving left to right, find the column labeled as channel #18. This is the reference (first) channel. Now move down the list of "TO CHANNEL#" in the left margin until channel #7 is found (first of three channels in the second-last group). At the intersection of column #18 and row #7 is the time of 38.000 (in microseconds). Now refer to Figure B-3. Across the top find channel #7, and down the left side find channel #18. The time that elapses from the sampling of channel #7 until channel #18 is captured is 32.000 µs.

An application's engineer needs to know the timing relationships for data acquired from channels #12, #6, and #23, in that order. Reference Figure B-2 for channel #12. The elapsed time from channel #12 until channel #6 is acquired is 14.625 µs while the time from channel #12 until #23 is captured is 29.125 µs. Reference Figure B-3 and find the column for channel #6. The time that elapses between the sampling of channel #6 and then channel #23 is 14.500 µs. This confirms the above matrix readings above (14.625 µs + 14.5000 µs = 29.125 µs). The time that elapses between the sampling of channel #6 until that of channel #12 (of the next frame) is found to be 55.375 µs. The delta times for channel #12 and #6, referenced to channel #23, are found to be 40.875 µs and 55.500 µs, respectively. Note that the dependent channels actually occur in the next frame with respect to the reference channel #23.

B.3 Supercommutation

The end of section 2.6.2 discusses briefly the concept of supercommutating channels to increase the sampling rate for higher bandwidth input signals. The three figures presented in this section, so far, make it easier to enable even distribution of samplings for a single input by spreading the number of samples out over the full frame in such a manner as to provide approximately equal delta times for the sampling process.

For instance, if a channel needs to be sampled at a rate of ≈110 Ksamples/second, then it is necessary to actually drive the input signal into eight, evenly distributed channels. A full frame time of 70 µs divided by eight yields a sample per 8.75 µs for an aggregate sampling rate of 114,286 samples/second. This can be accomplished by applying the same input signal to all eight channels of any single analog subsection; channels 1 through 8, or channels 9 through 16, or channels 17 through 24.



NOTE: The input impedance is the same as though it were a single input channel since only one analog subsection is being used; 50,594 Ω for differential mode or non-inverting single-ended mode, or 25,297 Ω for inverting single-ended mode with the non-inverting input grounded to AREF.

Table B-1 presents a table of corresponding input impedances as a function of the type of input and the number of analog subsystems being used. An analog subsystem is defined as channels sharing analog circuitry, and are grouped as channels 1 through 8, 9 through 16, and 17 through 24.

Table B-1 Input Impedances by Type and Groupings

Impedance (Ω)	Number of Groups	Type of input
50,594	1	Differential & Noninverting single
25,297	2	Differential & Noninverting single
16,865	3	Differential & Noninverting single
25,297	1	Inverting single-ended
12,649	2	Inverting single-ended
8,432	3	Inverting single-ended

Table B-2 presents a cross tabulation of the number of channels supercommutated, with their corresponding “ideal” delta times for evenly distributed samplings, and their resultant aggregate sampling rates. If the minimum sampling rate is known based upon the bandwidth of the input signal, then the number of input channels needed can be found along with the preferred sampling time spacing. Use Figure B-2 and Figure B-3 to assist in the distribution of the input across channel numbers. Also be alert to the decrease in input impedance as the signal is distributed across channels, as presented in Table B-1, above.

Table B-2 Supercommutation Rates/Times

Number of inputs:	≈ Time between samples (μs):	≈ Aggregate sampling Rate (s/s):
1	70.000	14,286
2	35.000	28,571
3	23.333	42,857
4	17.500	57,143
5	14.000	71,429
6	11.667	85,714
7	10.000	100,000
8	8.750	114,286
9	7.778	128,571
10	7.000	142,857
11	6.364	157,143
12	5.833	171,429
13	5.385	185,714
14	5.000	200,000
15	4.667	214,286
16	4.375	228,571
17	4.118	242,857
18	3.889	257,143
19	3.684	271,429
20	3.500	285,714
21	3.333	300,000
22	3.182	314,286
23	3.043	328,571
24	2.917	342,857

Note: The 2.917 μs approximate delta time between samples for the last entry is really an average of three actual timings of 2.875 μs, 2.875 μs, and 3.000 μs.

B.4 Differencing Inputs

Perhaps the most significant technical advantage of the ADM1224F is its ability to handle differential-ended inputs. The most common purpose for this feature is that of removing common-mode signals for noise reduction purposes. There are often applications where the difference between two analog signals contains significant information. Often these applications involve comparisons between set points and feedback signals, like those that are encountered in servo systems, and status alarm systems.

Table B-3 was generated by the external connection of eight channels of analog outputs from a DAC128F5 driving the differential-ended inputs of the first four channels of an ADM1224F. DAC128F5 #144 was installed on slot B of a MVME162-01, ADM1224F #100 was installed on slot A, and two 3 foot ribbon cables were connected together with

a special "ATE" board. Channel #1 of the DAC128F5 was connected to the non-inverting input to channel #1 of the ADM1224F (pin #2), and channel #2 of the DAC128F5 was connected to the inverting input to channel #1 of the ADM1224F (pin #1). The DAC128F5 voltages cited in the table were measured at the ATE board, while the voltages cited for the ADM1224F were calculated from the difference of the input voltages. The data tabulated is that captured by the manual control screen of the ATE software. Table B-3 is a small subset of the data collected to present a sampling of typical acquired data results for this kind of operation of the ADM1224F.

Table B-3 Differencing Results

Noninverting Voltage:	Inverting Voltage:	ADM1224F's Acquisition Results:	
		DATA:	≡Volts:
+4.99	-4.98	0x7E7	+9.97
+2.500	-4.98	0x5EB	+7.48
-0.018	-4.98	0x3F7	+4.962
-2.492	-4.98	0x1F7	+2.488
+4.99	+4.99	0xFFF	0.000
-4.98	-4.98	0xFFF	0.000
-4.98	-2.491	0xE07	-2.489
-4.98	+0.004	0xC0B	-4.84
-4.98	+2.500	0xA13	-7.48
-4.99	+4.99	0x81A	-9.98

B.5 DAC Monitors

For those systems that require built-in self-testing capability, the ADM1224F is an ideal candidate for providing real-time monitoring of analog outputs in a system. This is true due to the high-density, and ability to configure each input in any of several configurations. The only down side for this application is when a DAC is providing smaller incremental steps than that which can be detected by the ADM1224F. This will occur, for instance, when a 12-bit DAC has a smaller full-scale range than that of ±10 V, or when a DAC can provide full ±10 V outputs but has a higher resolution, like for 14 and 16-bit DACs.

As with any measurement system, probing a signal modifies it, sometimes significantly. The impact of monitoring DACs with the ADM1224F is that it provides a slightly lower load impedance, requiring a little more drive capability from the DACs.

B.6 ENDOFRAME strobe

The Carrier's strobe connection, for the slot on which an ADM1224F resides, provides an output signal that contains significant timing information about the current state of the IP Module in its continuous sequencing through all twenty-four channels. Section 2.3.1.1 discussed this briefly. A short, ½-ICLK-cycle-width pulse, ≈62 ns in duration, occurs every time the frame counter is incremented at the end of every 70 µs period defining a full sweep of all twenty-four channels.
ADM1224F #119 was loaded onto slot B of a VME3SC2 carrier. The "A1" probe of an HP DSO monitored ICLK on the back of the logic connector at pin #2, while the "A2" probe was attached to J5 pin B on the MVE3SC2's strobe connector. Figure B-4 presents

the resultant DSO snapshot. The ENDOFRAME pulse (lower trace) is ≈62 ns in width, lagging the ICLK low state by ≈9.6 ns, with a repetition rate of one pulse per 70 µs.

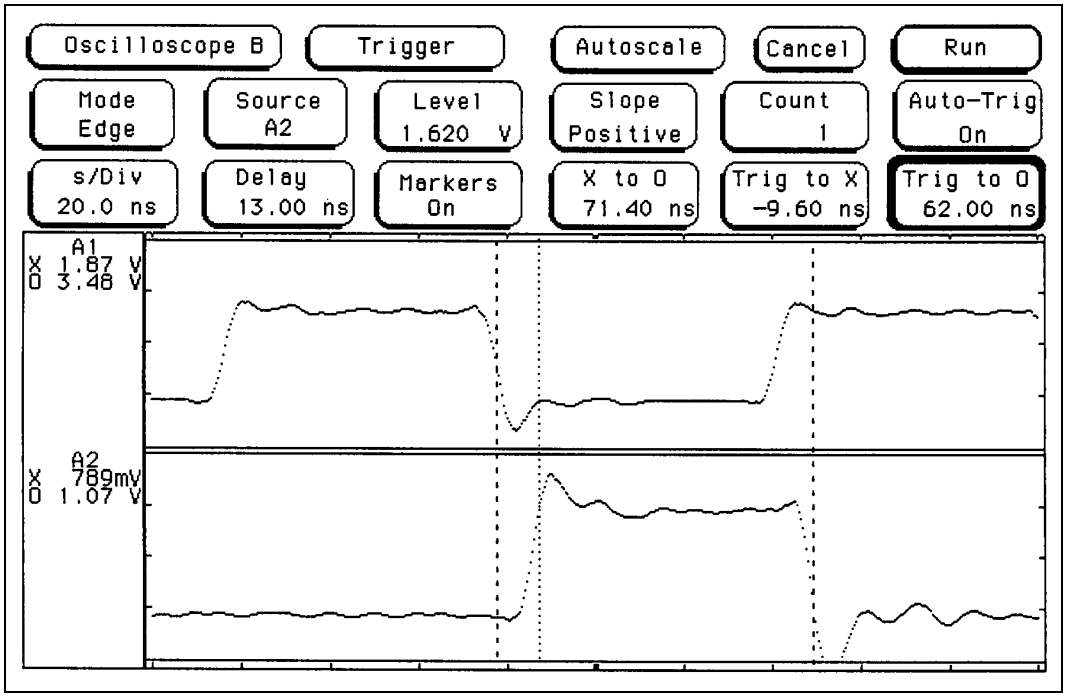


Figure B-4 ENDOFRAME "strobe" Pulse

This pulse is driven directly, through an 30 Ω series termination resistor, by the ALTERA EPLD with no buffer. Minimize the loading on this strobe connection, especially the capacitive loading.

This pulse is ideal for triggering an interrupt to the system that signals a processor to execute an interrupt service routine to read all of the data from the ADM1224F. Be aware that channel #1's data will be overwritten soon after the ENDOFRAME strobe pulse occurs. Therefore its data should be retrieved early in the ISR.

Connecting this strobe signal to a Systran DIO316I IP Module is the preferred way of generating an interrupt. It is recommended that the Systran DID48 IP Module not be used for this purpose since the DID48 will probably interpret this 62 ns pulse as nothing more than noise, and ignore it as a valid input.

This page intentionally left blank

APPENDIX C

PROGRAMMING GUIDE

TABLE OF CONTENTS

C.1 Overview C-1
C.2 Description C-1
C.3 IP Module ID PROM Listing C-1
C.4 IP Module I/O Address Map C-2
C.5 Word Access Address Translation C-3
C.6 Byte Access Address Translation C-4
C.7 Data Registers Bit Description (IPA=0x00 through 0x17) C-6
C.7.1 Data Registers 0 to 17 (IPA=0x00 through 0x17) C-6
C.8 Programming Example C-6
C.9 Integer Register Value to Floating Point Voltage Conversion C-6

TABLES

Table C-1 ADM1224F ID Address Space Listing C-1
Table C-2 ADM1224F I/O Address Space Listing C-2
Table C-3 Word Access Address Translation Table C-3
Table C-4 Byte Access Address Translation Table C-4
Table C-5 Data Register Description C-6

C.1 Overview

This section of the manual describes the operation of the ADM1224F from the software perspective, detailing the ADM1224F registers and providing programming examples. A more detailed description of the hardware can be found in Chapter 2, PRODUCT OVERVIEW and Appendix B, TYPICAL APPLICATIONS.

C.2 Description

The ADM1224F is a simple-to-use 12-bit, 24-channel, ADC (Analog-to-Digital Converter) card. All channels continuously convert and place their data into a current value table. The current values are retrieved by reading the data register for the corresponding channel.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible, due to the never-changing information it presents. It saves space, lowers costs, improves reliability, and enables this IP Module to provide "no-wait" read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) READs as all zeroes during valid ID read-only accesses.

Table C-1 is the ADM1224F emulated ID Address Space PROM listing.

Table C-1 ADM1224F ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII "I"	0x49
IPA = 0x01	ASCII "P"	0x50
IPA = 0x02	ASCII "A"	0x41
IPA = 0x03	ASCII "C"	0x43
IPA = 0x04	Systran's ID	0x45
IPA = 0x05	ADM1224's Model Number	0x6F
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0xCD

C.4 IP Module I/O Address Map

The ADM1224F's I/O Address Map contains 24 registers in the IP Module I/O space (IPA = 0x00 and IPA = 0x17). The address-detector circuitry is fully decoded.



NOTE: Any attempt to access I/O addresses at and above 0x18, or any attempt to WRITE to any I/O space, will result in no acknowledgment and subsequent bus time-out error on the carrier upon which this IP Module resides.

Table C-2 is the ADM1224F I/O Address map and contains the data registers.

Table C-2 ADM1224F I/O Address Space Listing

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	[15:8]	[7:0]	Channel 1 Data Register 16 bits
IPA = 0x01	[15:8]	[7:0]	Channel 2 Data Register 16 bits
IPA = 0x02	[15:8]	[7:0]	Channel 3 Data Register 16 bits
IPA = 0x03	[15:8]	[7:0]	Channel 4 Data Register 16 bits
IPA = 0x04	[15:8]	[7:0]	Channel 5 Data Register 16 bits
IPA = 0x05	[15:8]	[7:0]	Channel 6 Data Register 16 bits
IPA = 0x06	[15:8]	[7:0]	Channel 7 Data Register 16 bits
IPA = 0x07	[15:8]	[7:0]	Channel 8 Data Register 16 bits
IPA = 0x08	[15:8]	[7:0]	Channel 9 Data Register 16 bits
IPA = 0x09	[15:8]	[7:0]	Channel 10 Data Register 16 bits
IPA = 0x0A	[15:8]	[7:0]	Channel 11 Data Register 16 bits
IPA = 0x0B	[15:8]	[7:0]	Channel 12 Data Register 16 bits
IPA = 0x0C	[15:8]	[7:0]	Channel 13 Data Register 16 bits
IPA = 0x0D	[15:8]	[7:0]	Channel 14 Data Register 16 bits
IPA = 0x0E	[15:8]	[7:0]	Channel 15 Data Register 16 bits
IPA = 0x0F	[15:8]	[7:0]	Channel 16 Data Register 16 bits
IPA = 0x10	[15:8]	[7:0]	Channel 17 Data Register 16 bits
IPA = 0x11	[15:8]	[7:0]	Channel 18 Data Register 16 bits
IPA = 0x12	[15:8]	[7:0]	Channel 19 Data Register 16 bits
IPA = 0x13	[15:8]	[7:0]	Channel 20 Data Register 16 bits
IPA = 0x14	[15:8]	[7:0]	Channel 21 Data Register 16 bits
IPA = 0x15	[15:8]	[7:0]	Channel 22 Data Register 16 bits
IPA = 0x16	[15:8]	[7:0]	Channel 23 Data Register 16 bits
IPA = 0x17	[15:8]	[7:0]	Channel 24 Data Register 16 bits

C.5 Word Access Address Translation

Table C-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VME BUS Address	PC-AT BUS Address	NuBus Address	IP Module Address
BASE + 0x00	BASE + 0x00	BASE + 0x02	IPA = 0x00
BASE + 0x02	BASE + 0x02	BASE + 0x06	IPA = 0x01
BASE + 0x04	BASE + 0x04	BASE + 0x0A	IPA = 0x02
BASE + 0x06	BASE + 0x06	BASE + 0x0E	IPA = 0x03
BASE + 0x08	BASE + 0x08	BASE + 0x12	IPA = 0x04
BASE + 0x0A	BASE + 0x0A	BASE + 0x16	IPA = 0x05
BASE + 0x0C	BASE + 0x0C	BASE + 0x1A	IPA = 0x06
BASE + 0x0E	BASE + 0x0E	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B
BASE + 0x18	BASE + 0x18	BASE + 0x32	IPA = 0x0C
BASE + 0x1A	BASE + 0x1A	BASE + 0x36	IPA = 0x0D
BASE + 0x1C	BASE + 0x1C	BASE + 0x3A	IPA = 0x0E
BASE + 0x1E	BASE + 0x1E	BASE + 0x3E	IPA = 0x0F
BASE + 0x20	BASE + 0x20	BASE + 0x42	IPA = 0x10
BASE + 0x22	BASE + 0x22	BASE + 0x46	IPA = 0x11
BASE + 0x24	BASE + 0x24	BASE + 0x4A	IPA = 0x12
BASE + 0x26	BASE + 0x26	BASE + 0x4E	IPA = 0x13
BASE + 0x28	BASE + 0x28	BASE + 0x52	IPA = 0x14
BASE + 0x2A	BASE + 0x2A	BASE + 0x56	IPA = 0x15
BASE + 0x2C	BASE + 0x2C	BASE + 0x5A	IPA = 0x16
BASE + 0x2E	BASE + 0x2E	BASE + 0x5E	IPA = 0x17

C.6 Byte Access Address Translation

Table C-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VME BUS Address	PC-AT BUS Address	NuBus Address	IP Module Address	Byte-Lane *
BASE + 0x01	BASE + 0x00	BASE + 0x03	IPA = 0x00	0
BASE + 0x00	BASE + 0x01	BASE + 0x02	IPA = 0x00	1
BASE + 0x03	BASE + 0x02	BASE + 0x07	IPA = 0x01	0
BASE + 0x02	BASE + 0x03	BASE + 0x06	IPA = 0x01	1
BASE + 0x05	BASE + 0x04	BASE + 0x0B	IPA = 0x02	0
BASE + 0x04	BASE + 0x05	BASE + 0x0A	IPA = 0x02	1
BASE + 0x07	BASE + 0x06	BASE + 0x0F	IPA = 0x03	0
BASE + 0x06	BASE + 0x07	BASE + 0x0E	IPA = 0x03	1
BASE + 0x09	BASE + 0x08	BASE + 0x13	IPA = 0x04	0
BASE + 0x08	BASE + 0x09	BASE + 0x12	IPA = 0x04	1
BASE + 0x0B	BASE + 0x0A	BASE + 0x17	IPA = 0x05	0
BASE + 0x0A	BASE + 0x0B	BASE + 0x16	IPA = 0x05	1
BASE + 0x0D	BASE + 0x0C	BASE + 0x1B	IPA = 0x06	0
BASE + 0x0C	BASE + 0x0D	BASE + 0x1A	IPA = 0x06	1
BASE + 0x0F	BASE + 0x0E	BASE + 0x1F	IPA = 0x07	0
BASE + 0x0E	BASE + 0x0F	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1
BASE + 0x19	BASE + 0x18	BASE + 0x33	IPA = 0x0C	0
BASE + 0x18	BASE + 0x19	BASE + 0x32	IPA = 0x0C	1
BASE + 0x1B	BASE + 0x1A	BASE + 0x37	IPA = 0x0D	0
BASE + 0x1A	BASE + 0x1B	BASE + 0x36	IPA = 0x0D	1
BASE + 0x1D	BASE + 0x1C	BASE + 0x3B	IPA = 0x0E	0
BASE + 0x1C	BASE + 0x1D	BASE + 0x3A	IPA = 0x0E	1
BASE + 0x1F	BASE + 0x1E	BASE + 0x3F	IPA = 0x0F	0
BASE + 0x1E	BASE + 0x1F	BASE + 0x3E	IPA = 0x0F	1

VME BUS Address	PC-AT BUS Address	NuBus Address	IP Module Address	Byte-Lane *
BASE + 0x21	BASE + 0x20	BASE + 0x43	IPA = 0x10	0
BASE + 0x20	BASE + 0x21	BASE + 0x42	IPA = 0x10	1
BASE + 0x23	BASE + 0x22	BASE + 0x47	IPA = 0x11	0
BASE + 0x22	BASE + 0x23	BASE + 0x46	IPA = 0x11	1
BASE + 0x25	BASE + 0x24	BASE + 0x4B	IPA = 0x12	0
BASE + 0x24	BASE + 0x25	BASE + 0x4A	IPA = 0x12	1
BASE + 0x27	BASE + 0x26	BASE + 0x4F	IPA = 0x13	0
BASE + 0x26	BASE + 0x27	BASE + 0x4E	IPA = 0x13	1
BASE + 0x29	BASE + 0x28	BASE + 0x53	IPA = 0x14	0
BASE + 0x28	BASE + 0x29	BASE + 0x52	IPA = 0x14	1
BASE + 0x2B	BASE + 0x2A	BASE + 0x57	IPA = 0x15	0
BASE + 0x2A	BASE + 0x2B	BASE + 0x56	IPA = 0x15	1
BASE + 0x2D	BASE + 0x2C	BASE + 0x5B	IPA = 0x16	0
BASE + 0x2C	BASE + 0x2D	BASE + 0x5A	IPA = 0x16	1
BASE + 0x2F	BASE + 0x2E	BASE + 0x5F	IPA = 0x17	1
BASE + 0x2E	BASE + 0x2F	BASE + 0x5E	IPA = 0x17	1

* Byte-lane 1 not applicable for ID Space

C.7 Data Registers Bit Description (IPA=0x00 through 0x17)

The ADM1224F has 24 16-bit-wide registers, with each register corresponding to an ADC channel. The ADM1224F supports word (16-bit) READs only.

C.7.1 Data Registers 0 to 17 (IPA=0x00 through 0x17)

Table C-5 Data Register Description

Bit#	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	FC 3	FC 2	FC 1	FC 0	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Indeterminate. Real data is present in all registers 78.75 µs after negation of reset.

AD11- AD0: These bits represent the 12-bit two's complement ADC value for the corresponding channel.

FC3-FC0: These bits represent the 4-bit GRAY CODE frame count value for the corresponding channel. A detailed explanation of the frame count GRAY CODE can be found in section 2.3.1 under the heading "4-Bit Frame Counter".

C.8 Programming Example

The following example illustrates how to use the ADM1224F device from a programming perspective.

- At power-up, the ADCs begin converting and placing their data in the current value tables.
- Read ADC channel #1 by reading Data Register 0 at IP Module address 0.
- The ADC value in two's complement binary is extracted by ANDing the register value with 0x0FFF.
- The frame count is extracted by shifting the register value to the right 12 bits and ANDing it with 0x000F.

All of the channels are read in the same manner as the channel #1 example above.

C.9 Integer Register Value to Floating Point Voltage Conversion

The ADM1224F uses a 12-bit two's complement binary representation of the input voltages. The following example illustrates how to convert this integer ADC value to a floating-point volts representation.

CONVERTING THE REGISTER VALUE TO A VOLTAGE

Vin = SignExtendedRegVal * 0.0048828

where:
Vin is the ADC input voltage
SignExtendedRegVal is the sign extended value read from the ADC data register (see explanation below).

SIGN EXTENDING THE 12-BIT REGISTER VALUE

The following example illustrates how to sign extend the 12-bit two's complement ADC value to create a signed 16-bit ADC value:

Read the ADC data register as a 16-bit word.

Test bit 11 (bit numbering starting from 0) of the read value.

```
If bit 11 = 1,
   Then set bits 15 to 12 to 1's (OR it with 0xF000)
Else if bit 11 = 0,
   Then clear bits 15 to 12 0's (AND it with 0x0FFF)
End if
```


NOTE: In either case, the frame count in bits 15 to 12 are overwritten with 1's or 0's. The resulting 16-bit value is a two's complement signed value that can be multiplied by 0.0048828 to obtain the voltage.

This page intentionally left blank

GLOSSARY

[x:y]----------Bit-range designation (in descending decimal), where “x” is the most significant bit down to "y", the least significant bit. (For example, IPD[15:0] refers to the IPD bus where bit 15 is the most significant bit, bit 0 is the least significant bit, and there are 16 bits).

Accuracy ----------*ABSOLUTE*: The error of an ADC at a given output code is the difference between the theoretical and actual analog input voltages required to produce that code.

RELATIVE: The deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

acquire----------The process of selecting and capturing an analog signal for the process of developing its digital representation. A sample/hold or track/hold amplifier usually performs the capturing operation.

active filter ----------A signal filter that uses an amplifier with conventional passive filter elements to provide a desired fixed or tunable pass or rejection characteristic.

ADC ----------Analog-to-Digital Converter. A device that translates continuous analog signals into proportional discrete digital signals.

aliasing error ----------(*over-simplified*) The unrecoverable error in converted data that occurs when sampling an analog signal whose bandwidth is not limited (*by a low-pass filter*) to less than half of the sampling frequency to an amplitude of at least -72 dB for a twelve bit ADC.

analog mux ----------Also known as an analog multiplexer, it provides switching of analog input signals to allow use of a common analog-to-digital converter.

analog signal ----------A nominally continuous electrical signal that varies in amplitude or frequency in response to changes in physical phenomenon, such as sound, light, heat, position, or pressure.

AREF ----------Analog Reference, common or ground.

bipolar mode----------A configuration that an ADC uses to handle signal spans containing both positive and negative signals. Usually it means offsetting half-scale to become analog zero, and accepting the resulting offset binary code or changing it to two's complement coding.

buffer amp----------An operational amplifier used after a critical stage to isolate it from the effects of load impedance variations in subsequent stages.

byte ----------8 contiguous bits on octal boundaries. (For example, IPD[15:8], and IPD[7:0]).

byte-lane ----------Byte position description. (For example, IPD[15:8] is the “*high*” byte-lane, also defined as “*byte-lane ONE*”; whereas IPD[7:0] is the “*low*” byte-lane, also defined as “*byte-lane ZERO*”).

CAD ----------Computer-Aided Design.

CAE ----------Computer-Aided Engineering.

clipper-limiter ----------A device whose output is a function of the instantaneous input amplitude for a range of values lying between two predetermined limits but is approximately constant, at another level, for input values above or below the range.

CMR ----------Common-Mode Rejection. The ability of an amplifier to cancel a common-mode signal while responding to an out-of-phase signal, often through variation of a ground level.

CMRR ----------Common-Mode Rejection Ratio is the ratio of gain for the differential, or normal-mode, signal to the gain for the common-mode signal.

CMS ----------Common-Mode Signal. A signal applied equally to both ungrounded inputs of a balanced amplifier stage or other differential device.

conversion rate ----------The number of complete conversions an analog-to-digital converter can perform per unit time, usually specified in conversions per second per channel.

CRC ----------Cyclic Redundancy Check.

CVT ----------Current Value Table consisting of twenty-four current value registers.

differential----------As in input; a circuit that rejects voltages that are the same at both (+ and -) input terminals and amplifies the voltage difference between the two input terminals.

DNL ----------Differential Nonlinearity (*see nonlinearity*).

doublewide ----------An IP Module that is physically and possibly electrically two side-by-side singlewide IP Modules.

EPLD ----------Erasable Programmable Logic Device.

endoframe ----------Short pulse driven out the N_STROBE logic signal line to the host carrier indicating when channel #24 has just had its ADC and frame count information written to the CVT; also internally increments the frame counter.

ENOB----------Effective Number Of Bits. For a sine wave, the signal-to-noise ratio can be expressed in terms of the number of bits.

$$ENOB = (SNR - 1.76) \div 6.02.$$

frame----------One complete pass through all twenty-four channels.

frame time ----------Time per frame = 70 µs. The reciprocal of this is the sampling rate per channel.

gain error ----------The deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions.

GRAYbus----------Gray Code Engine bus (test points) designated as: GRAY[6:0].

IAMP ----------Instrumentation Amplifier; differential-input, single-ended output. Usually is a closed-loop fixed-gain amplifier, with very high input impedance, low drift, and high common-mode rejection over a wide range of frequencies.

Id----------Drain current of MUX; usually in context with ON and OFF leakage current specifications.

Idiff----------Differential, OFF-state output leakage current for differential multiplexers, where the first channel experiences plus-full-scale on the non-inverting input and minus-full-scale on the inverting input, and the adjacent channel is driven with plus-full-scale on the inverting input and minus-full-scale on the non-inverting input.

ID PROM----------Identification Programmable Read Only Memory, emulated within the EPLD providing the required identification information about the IPack.

INL ----------Integral Nonlinearity (*see nonlinearity*).

I/O ----------Input/Output.

IPAbus----------IP Address bus designated as: IPA[6:1].

IP Module----------Business-card size mezzanine-type boards that provide general and special-purpose input and output functions to and from their host carriers. The ANSI/VITA 4-1995 standard defines the mechanical and electrical interface to the carrier board, which can be a bus converter or a standalone, embedded host.

IPDbus----------IP Data bus designated as: IPD[15:0].

Is ----------Source current of MUX; usually in context with ON and OFF leakage current specifications.

kHz ----------Kilohertz; thousands of cycles per second.

LSB----------Least Significant Bit. Example:

$$20\ V \div 4096\ bits = 4.8828\ mV$$

lowpass filter----------A passive or active filter that transmits alternating current below a given cutoff frequency and substantially attenuates all other currents.

monotonic----------A specification that guarantees no missing codes such that every code combination appears in an increasing sequence as the analog input level is increased.

MTBF----------Mean Time Between Failures.

multiplexer ----------See Analog Mux.

MUXAbus ----------Multiplexer 'A' (address) bus, designated as: MUXA[2:0]. These three signals provide the address that define which of the eight channels, from 1 through 8, that are presented to its subsequent differential amplifier and ADC.

MUXBbus ----------Multiplexer 'B' (address) bus, designated as: MUXB[2:0]. These three signals provide the address that define which of the eight channels, from 9 through 16, that are presented to its subsequent differential amplifier and ADC.

MUXCbus ----------Multiplexer 'C'(address) bus, designated as: MUXC[2:0]. These three signals provide the address that define which of the eight channels, from 17 through 24, that are presented to its subsequent differential amplifier and ADC.

nA----------Nanoamperes, or 10^{-9} amps.

nonlinearity----------*DIFFERENTIAL:* An ideal ADC provides code transitions that are one LSB apart. Differential nonlinearity is the maximum deviation, expressed in LSBs, from this ideal value.

INTEGRAL: The worst-case deviation of a code from a best-fit straight line between "zero" and "full scale".

ns----------Nanoseconds, or 10^{-9} seconds.

offset error ----------The deviation of the actual MSB code change to the ideal of ½LSB below analog common. See "2's complement", below.

ρC----------Picocoulombs, or 10^{-12} coulombs. A unit of electrical charge.

PSRR----------Power Supply Rejection Ratio. Often referred to in amplifier specifications, it is the equivalent change at the input due to variations in the power supply. For an amplifier with a gain of 1, a PSRR of 10 mV/V will provide 10 mV of change on the output for every volt of change on the power supply.

Qinj----------Charge Injection; also charge transfer. In multiplexers, this is the transfer of charge (energy) from the switch driver to the output capacitance after a switch turns off.

QSOP ----------Quarter-sized Small Outline (surface mount) Packages.

RDSon ----------A Multiplexer's series ON-channel resistance measured between the source ("S") input and the drain ("D") output terminals under specified conditions.

SADDbus ----------SRAM's ADDress bus, designated as: SADD[4:0]. These five address lines provide the proper location addressing function for reads from and writes to the SRAM, which is the CVT.

SAR----------Successive Approximation (shift) Register type of ADC.

SNR----------The measured Signal-to-Noise Ratio at the output of the ADC, usually including harmonic distortions, logarithmically expressed in decibels. The ideal is:

$$SNR = (6.02\mathbf{N} + 1.76)\ dB$$

where **N** = bits of resolution.

settling time ----------Also known as the transient response time, the settling time of an ADC is the time required for the ADC to settle to rated accuracy after the application of a full-scale step input in either direction.

single-ended----------As in input; unbalanced and not differential, and one side of the transmission line or circuit is usually referenced to analog common or ground.

singlewide----------The most common size (and smallest) physical IP Module size (3.9 inches by 1.8 inches).

span----------The full scale analog input ranged; = ±10.000 V.

SRAMDbus ----------Static Random Access Memory Data bus designated as: SRAMD[15:0]. The nibble consisting of SRAMD[15:12] contains the frame count information while the 1½ bytes consisting of SRAMD[11:0] contains the ADC information.

switching time ----------The time required for a multiplexer to switch and slew from one analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load.

2's complement----------Output coding: 0x800 @ -10.000 Volts input through 0xFFF @ ≈ -0.005 V input; 0x000 @ 0.000 V input through 0x7FF @ +9.995 V input.

µs----------Microseconds, or 10^{-6} seconds.

VHDL----------Very high-speed integrated circuit hardware description language, used, with synthesis, for EPLD logic development.

VIN+#----------The non-inverting input for differential inputs applied to the ADM1224F IP Module; also the only input for single-ended inputs. # ≡ 1 through 24 channel numbers.

VIN-# ----------The inverting input for differential inputs; or ground (optionally on-board jumpered) for single-ended inputs. # ≡ 1 through 24 channel numbers.

This page intentionally left blank

INDEX

A

access contention 2-10
analog input channels 2-2
analog outputs B-7, B-8
analog signal 2-3, 2-4, 3-2, 3-4, B-7

B

backplane 2-1
bandwidth 2-11, B-5, B-6
base address 4-6, C-3, C-4
binary counters 2-15
bus time-out error C-1, C-2

C

carrier board 1-1, 2-2, 2-3, 2-6, 2-8, 2-10, 2-11, 2-14, 2-15, 3-1, 3-6, 3-7, 4-1, 4-5, 4-6, A-2, A-3, B-1, B-8, C-1, C-2
carrier power A-2
carrier power supplies A-3
clock rate A-1
common-mode signals B-7
connector 2-3, 2-8, 2-9, 2-10, 3-1, 3-2, 3-3, 3-4, 3-5, 3-6, A-1, B-8
control signals 4-5
current value table 2-2, 2-3, 2-4, 2-6, 2-8, 2-10, 2-11, 2-12, 2-13, 2-14, 2-15, 4-1, 4-3, 4-5

D

data acquisition rate 2-13
data bus interface 2-3
data conversion 2-10
data register C-1, C-2, C-6, C-7
distortion A-3
DMA activity A-1

E

Electrostatic Sensitive Device 3-1
emulation 2-6, C-1
EPLD Altera device 2-6, 2-8, 2-15, B-9

F

falling edge 4-5
frame count 2-3, 2-8, 2-10, 2-12
frame counter 2-8

H

hold cycles A-1

I

I/O address map C-2
I/O connector A-2
I/O locations A-1
I/O read 4-6
ID address space C-1
ID locations A-1
ID PROM 2-3, 2-6, 2-8, C-1
ID read 4-6, C-1
impedance 2-11, 3-2, 4-11, B-5, B-6
input signal 3-2, 3-3, 3-4, 4-5, A-4, B-5, B-6
interrupt 2-8, B-9
interrupt requests A-1
interrupt service routine 2-8, B-9
interrupt vector A-1
inverted signals 2-9
IP Module 1-1, 2-1, 2-2, 2-3, 2-6, 2-8, 2-9, 2-10, 2-13, 3-1, 3-2, 3-3, 3-6, 3-7, 3-8, 3-9, 4-1, 4-6, B-1, B-8, B-9, C-1, C-2, C-3, C-4, C-6
singlewide 2-1
IP Module carrier 2-1, 2-3, 3-6, 3-7

J

jumpers 2-2, 3-1, 3-2, 3-4, 3-5

L

load impedance B-8
logic analyzer
snapshot 4-1, B-9

M

manual 1-1, 3-1
measurements A-1
memory transfers A-1
MTBF A-4
multiplexer 2-1, 2-2, 2-3, 2-4, 2-8, 2-9, 2-15, 3-4, 4-7

O

overvoltage A-3

P

piezo-resistive sensor 3-3
pin assignments 3-6
polarity inversion 3-3, 3-4
power-up 2-2, C-6

R

register 2-14, 2-15, C-6
rising edge 4-2, 4-3, 4-5

S

shorting shunt 3-1, 3-3, 3-4, 3-5

signal sampling.....2-10
signal tracking.....2-6
specifications 4-10
state machine.....2-3, 2-4, 2-9
strobe connection B-8, B-9
supercommutation.....2-11

T

thickness.....A-1
timing 2-6, 2-12, 2-13, 3-2, 4-6, B-1, B-5, B-8
tracking time 4-5
tristateable.....1-3

V

VHDL 2-15, 2-16

W

wait cycles.....A-1
weight.....A-1

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP