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CPCISC2

CompactPCI® Slave 2-Slot IP Module Carrier Hardware Reference

Document No. B-T-MR-CPCISC2#-A-0-A5

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Revised: March 18, 2004

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for the Systran CPCISC2 3U CompactPCI Slave 2-slot IP Module Carrier, part number BHAS-CPCISC2. It provides a physical and operational description of the CPCISC2, both from hardware and software perspectives, detailed technical information about CPCISC2 performance characteristics, and a few typical applications.

1.1.2 Scope

This information is intended for applications requiring a carrier interface between IP Modules and CompactPCI system buses. You must have a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IP Modules to effectively use this manual.

- Called functions are italicized: *OpenConnect()*
- Data types are italicized: *int*
- Function parameters are bolded: **Action**
- Path names are italicized: *utility/sw/cfg*
- File names are bolded: **config.c**
- Absolute path file names are italicized and bolded: ***utility/sw/cfg/config.c***
- Hexadecimal values are written with a "0x" prefix: 0xFB001040
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/): /SYNC
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that is bolded represents user input. Text that the computer displays on the screen is not bolded.

```
ls
file1          file2             file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- *PCI Local Bus Specification Rev. 2.1- PCI Special Interest Group*
- *American National Standard for IP Modules, version ANSI/VITA 4-1995* - Published by the VMEbus International Trade Assoc. 7825 E. Gelding Dr. Suite 104, Scottsdale AZ. 85260-0720
- CompactPCI Specification, PICMG 2.0 R2.1, Sept. 1997 by the PCI Industrial Computer Manufacturer's Group

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Our Quality System addresses the following basic objectives:

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- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

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Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: support@systran.com
- Fax: (937) 252-1465
- World Wide Web address: www.systran.com

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To learn more about Systran products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: info@systran.com
- World Wide Web address: www.systran.com

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2. PRODUCT OVERVIEW

2.1 Overview

This section describes the CPCISC2 functions and features.

NOTE: The IP Module signal references, and transfer and cycle types discussed in this document are explained in detail in the *ANSI/VITA 4-1995, American National Standard for IP Modules.*

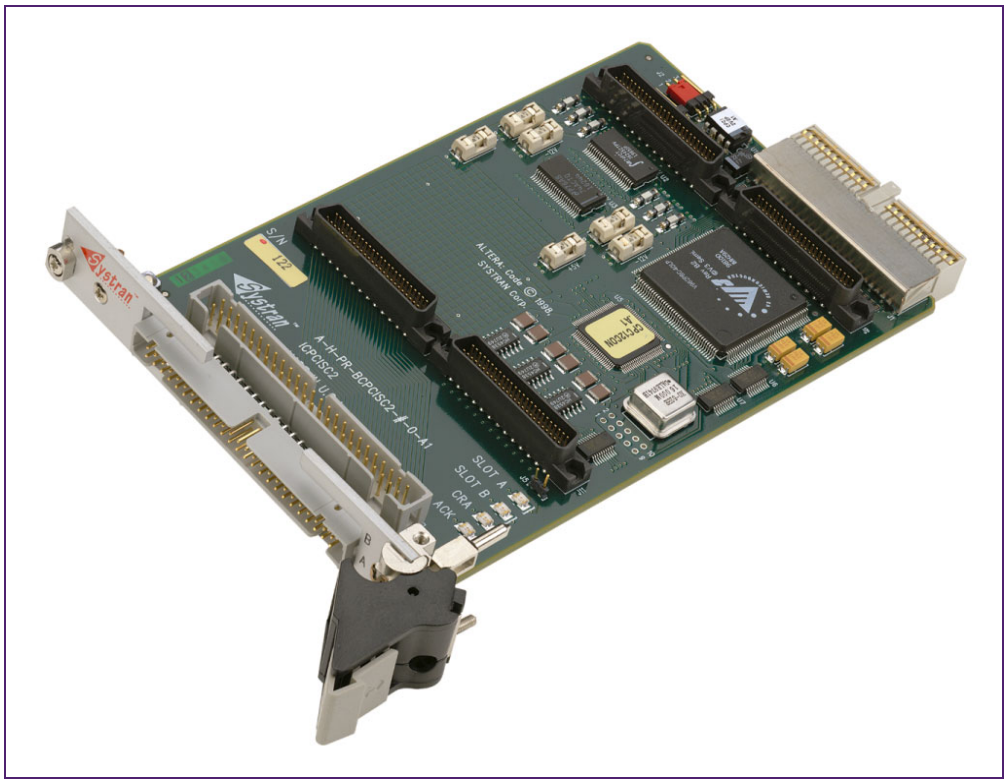


Figure 2-1 CPCISC2 Board

2.2 Functional Description

The Systran CPCISC2 Slave 2-slot IP Module Carrier board (part number BHAS-CPCISC2) is a 3U CompactPCI slave add-in board that supports two singlewide IP Modules or one doublewide IP Module. The CPCISC2 supports 8 MHz IP transfers of ID, I/O, Interrupt Acknowledge and Memory for all slots. The CPCISC2's PCI interface design is compliant with the PCI bus specification V2.1 and the IP interface is designed in accordance with the *IP Module Logic Interface Specification ANSI/VITA 4-1995.*

The bus connector interface and board physical layout are in accordance with the CompactPCI specification PICMG 2.0 R2.1.



NOTE: In this manual CompactPCI will be referred to as CPCI. Also note that the acronym "CPCI" refers to any characteristics of the CPCISC2 that are mechanically based; this includes the J1 connector for interfacing to the host via a backplane. The acronym "PCI" is used when relating to electrical characteristics of the board or relating to signals that are covered in the PCI specification separate from CompactPCI.

The CPCISC2 encompasses a design that does not insert IP hold cycles. This guarantees the highest throughput possible for this PCI-to-IP Module bus-coupling carrier. The CPCISC2 provides up to 100 I/O points (50 per IP) per CPCI slot. LEDs on the CPCISC2 provide diagnostic information on accesses to the IPs, the CPCISC2 local registers, and an IP acknowledgment signal. The CPCISC2 has a very easy-to-use and flexible interrupt capability where the individual interrupts from each IP Module can be programmed to assert a common interrupt request to the PCI bus.

2.2.1 Features

- Up to 100 I/O points in a single, 3U CPCI slot.
- I/O, ID, INT and MEM transfers on all slots with no HOLD cycles inserted.
- CPCISC2 registers and IP Modules mapped into PCI memory space for easy access.
- Board base addresses automatically configured by system BIOS at power-up.
- Supports two singlewide IPs, or one doublewide card.
- Each of four IP interrupt requests (two per IP Module slot) can individually assert a common PCI interrupt.
- Local bus interface time-out can be enabled via software.
- Board is memory mapped via two apertures in the PCI bridge.
- Independent field-replaceable fuses, and 'T'-type filters are used for the +5, +12, and -12 V power feeding each IP.
- Four IP/Carrier Access and IP Acknowledge indicators (with pulse stretchers).
- Posts IP error signals as status.
- Supports writes to ID space.
- Resets individual IP Modules via software.
- One "standard" I/O ribbon cable connection can be made without board removal.
- Supports two "strobe" connections (one per slot).

2.2.2 Memory Mapping Scheme

The mapping scheme for the ID and I/O address spaces on all four IP Modules as well as the carrier's on-board CSRs are all made at fixed addresses relative to the board base address, which is contained in the PCI Configuration Space Registers. These registers are found inside the V962PBC PCI Bridge IC (U4 on the CPCISC2). For more information on these registers, contact QuickLogic at the address below:

QuickLogic
1277 Orleans Drive
Sunnyvale, CA 94089 USA
Telephone: 408.990.4000
Fax: 408.990.4040
www.quicklogic.com

IP Module memory accesses are performed relative to base addresses set within an aperture register in the Configuration Space and on-board address decoding. Memory size as well as base address is controlled by the aperture settings. Chapter 3. and Appendix B. discuss the memory mapping in more detail.

2.2.3 PciCfg Utility

The **PciCfg** Utility facilitates the modification of the PCI configuration EEPROM on up to 16 installed IP Carriers on a single machine. This software allows for quick, easy disabling or enabling of the IP module memory space. If the IP memory space is disabled, the carrier occupies much less PCI memory space. Instructions for installation and use of the **PciCfg** program disk are included in Appendix E. of this manual. The **PciCfg** Utility software is provided with this manual in a sleeve on the inside back cover.

2.3 ID Transfers

IP Module ID transfers are supported as 8-bit or 16-bit local transfers. ID transfers are performed by a byte or word read/write operation of the slot IP Module ID address space from the PCI Bus. The ID ROM values are located every other byte at IP Module odd-byte locations (IP Module byte-lane 0). For 8-bit reads the even byte is discarded. The ID ROM area allows read or write accesses to support future IP Modules requiring writes to the ID address space.

The IP Module data bus has been made big-endian to be compatible with VME. Since PCI is 32-bit little-endian, accesses to the IP Modules occur for PCI even addresses on four byte boundaries only. On PCI, the odd byte is the upper byte (D15 - D8) and the even byte is the lower byte (D0 - D7). For this reason, on 16-bit reads and writes, the IP Module odd byte is transferred on the PCI even byte, and the IP Module even byte is transferred on the PCI odd byte. Single-byte transfers are performed on PCI even addresses only and access the IP Module odd byte.

2.3.1 I/O Transfers

IP Module I/O transfers are supported as 8-bit or 16-bit PCI transfers. I/O transfers are performed by a byte or word read or write operation of the slot IP Module I/O address space from the PCI Bus.

2.3.2 Interrupt Transfers

The IP Module requests interrupts by assertion of N_INTREQ0 or N_INTREQ1. An independent Local-to-PCI interrupt circuit handles each of these IP Module interrupt request lines which asserts the interrupt request line INTA# to the PCI bus. This provides a minimum delay in asserting the interrupt request to the CPU board.

In detail, the hardware and firmware in the CPCISC2 are configured such that any of five interrupts (Intreq0 and Intreq1 from each of two IP Modules and a time-out interrupt) will generate an INTB# input to the on-board PCI bridge which will generate an INTA# to the PCI bus. The INTB# from the IP Interface controller will only be generated if enabled to do so in software. Interrupts are disabled upon power-up to prevent a possible interrupt cycle from occurring until the system becomes stable. Upon completion of power-up, bits in the Control Register on the CPCISC2 can then be set to enable IP and time-out interrupts.

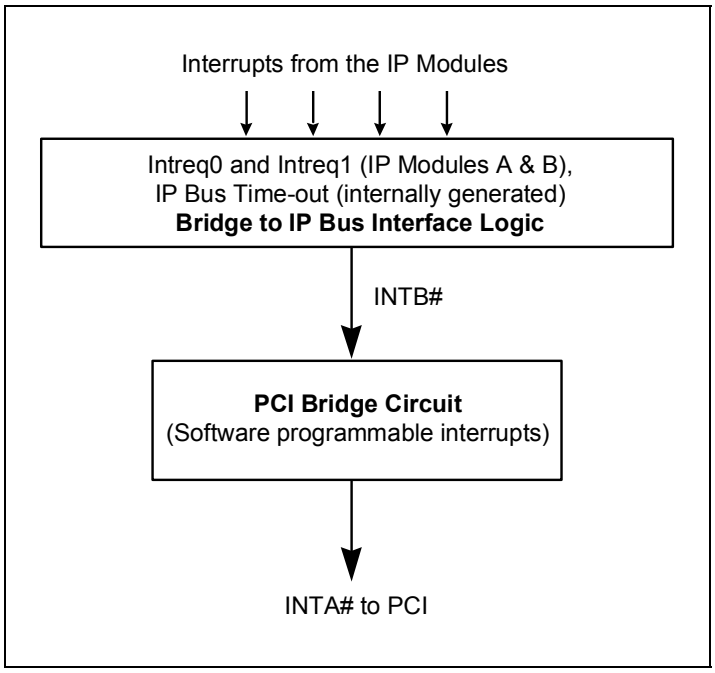


Figure 2-2 Interrupt-Select Tiers

2.3.3 Interrupt Configuration

The interrupt-select tiers in Figure 2-2 show the interrupt "flow" from the IP Modules to the PCI bus.

2.3.4 Diagnostic LEDs

The CPCISC2 has four diagnostic LEDs on the board as shown in Figure 3-6. The LEDs on the board labeled "SLOT A", "SLOT B", and "CRA" indicate when a READ or WRITE transaction is attempted to one of the two IP Modules or a carrier register. The fourth LED, labeled "ACK," indicates an acknowledgment by the IP Module of the attempted access. This scheme provides independent verification of the access and the acknowledgment.

2.3.5 IP Module Reset

Independent or simultaneous resetting of the IP Modules is facilitated through writes to the Reset register. Monitoring of the pulse-stretched reset signals is made possible by reading the Reset register. See Appendix B for a detailed description of this register.

2.3.6 Error Status

Monitoring of the IP Module ERROR signals is made possible by reading the Error Status register. See Appendix B for a detailed description of this register.

2.3.7 Strobe Signals

The IP Module STROBE signals can be connected via a 4-pin header (J4).

2.3.8 Power Supply Filtering

Independent 'T'-type filters are used for the +5, +12, and -12 volt power feeding each IP Module. This arrangement provides superior power supply filtering.

2.3.9 Fuses

Independent field-replaceable fuses are used for the +5, +12, and -12 volt power feeding each IP Module. This provides superior short-circuit protection.



NOTE: Replacement fuses can be purchased directly from Littelfuse, Inc. Phone (708) 829-0400.

1 Amp Fuse Manufacturer's Part Number R451001
2 Amp Fuse Manufacturer's Part Number R451002

2.4 Theory of Operation

2.4.1 Description

The CPCISC2 is an easy-to-use CPCI slave card that holds two singlewide, or one doublewide IP Modules. In addition to providing access to the I/O and ID space of the IP Modules via the CPCI backplane, the CPCISC2 has four locations to perform interrupt acknowledge cycles on the IP Modules, and four on-board control/status registers.

2.4.2 Operation

The signal flow between the CPCI bus backplane, IP Module Logic Bus and the IP Module I/O connectors is schematically shown in Figure 2-3. On the left side of the diagram is the PCI bus connector responsible for all transfers between the backplane and the Bridge registers, CSR registers or IP Modules.

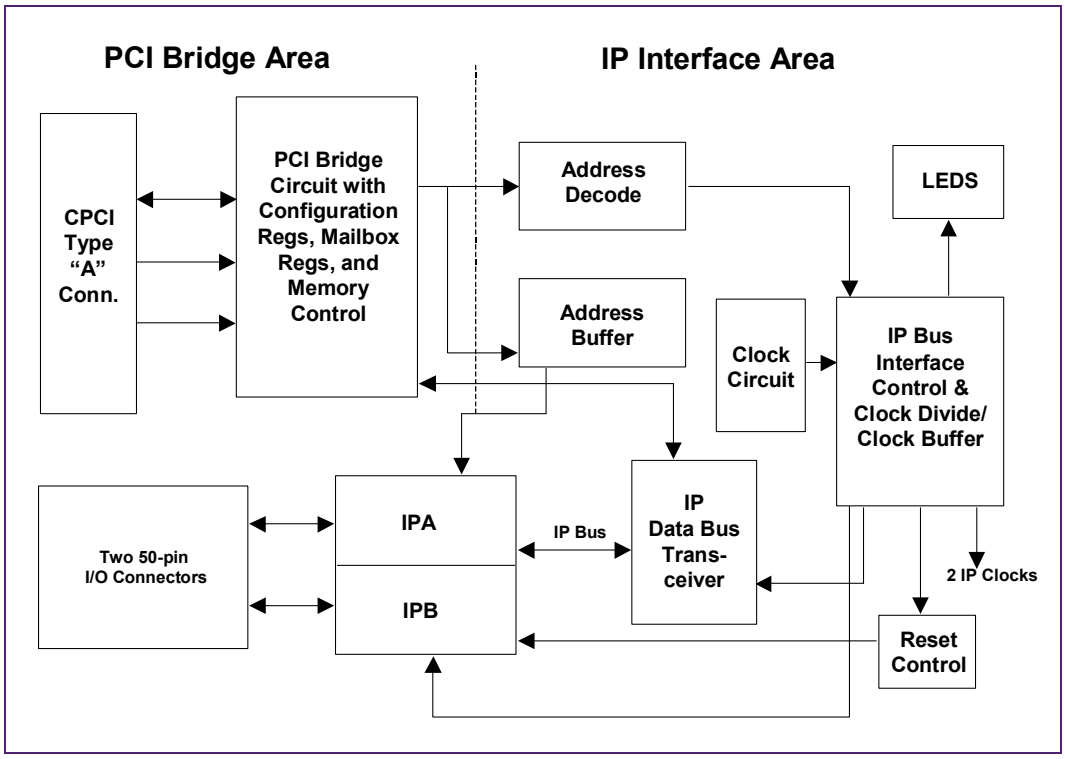


Figure 2-3 CPCISC2 Block Diagram

Other component functions are:

- ADDRESS DECODE: Handles decoding of the aperture address generated from the bridge circuit. This circuit determines which select strobe to generate to a particular IP Module based on the address bits LA25 through LA2.
- ADDRESS BUFFER: Provides the common IP address bits IPA1 through IPA6 to all the IP Modules as well as address bits 7 through 22 during the select cycle for memory transactions.
- IP DATA BUS TRANSCEIVER: Buffers the PCI bridge device from the IP Module data bus.
- IP INTERFACE CONTROL: Provides timing and control of the data flow between the PCI bus bridge and the IP Module bus. It also provides control of the address buffers such that the IP Module data bus will contain an address only during the select cycle of a memory transfer. This block also has a programmable time-out circuit that prevents the local side of the PCI bridge circuit from "hanging." This block will also produce the reset pulses for the IP Modules and the required synchronous select cycles for ID, I/O, Interrupt Acknowledge and Memory transactions.
- RESET CONTROLLER: Block consists of a bank of pulse stretchers that convert the narrow trigger from the reset register in the "IP INTERFACE CONTROL" part to a 200 ms pulse for each of the IP Modules. The wide pulses will then be synchronized to the IP bus clock such that they will be deasserted synchronously.
- LEDS: Contains pulse stretchers and four LEDs to indicate transaction attempts to each of two IP Modules and the on board CSR registers as well as an acknowledge indicator.
- CLOCK CIRCUIT: consists of a 16 MHz oscillator, divider flip-flop and low-skew buffers to allow a separate clock for each IP Module.
- PCI BRIDGE CIRCUIT: Consists of a large-scale IC that provides an interface between the PCI bus backplane and the interface to the IP Module bus.

3. INSTALLATION

3.1 Overview

This chapter describes the installation of the CPCISC2 board. Installation requires the following steps:

- Unpack the board
- Visually inspect the board
- Configure and install the board

3.2 Unpack the CPCISC2

Table 3-1 lists the contents of the CPCISC2 shipping packages.

Table 3-1 Contents of CPCISC2 Shipping Packages

Qty	Description
1	CPCISC2 Printed Circuit Assembly
2	Surface mount spare fuses (one-1 Amp, one-2 Amp)
1	CPCISC2 User Manual *

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR-CPCISC2).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.3 Visually Inspect the CPCISC2

Examine the CPCISC2 to determine if any damage occurred during shipping.

3.4 Configure and Install the CPCISC2



NOTE: The CPCISC2 is an Electrostatic Sensitive Device (ESD). Use an anti-static mat connected to a wristband when handling or installing the board.

The tools required for the CPCISC2 installation are listed in Table 3-2.

Table 3-2 CPCISC2 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver
1	Standard Phillips Screwdriver (Optional)

3.4.1 Jumper and Strobe Header Locations

Figure 3-1 shows the locations of the RESET Mode jumper (J2), the V3 EEPROM Write Protect jumper (J3) and the Strobe header (J4). Each of these items and their settings are described in their respective sections. Refer to this figure as required.

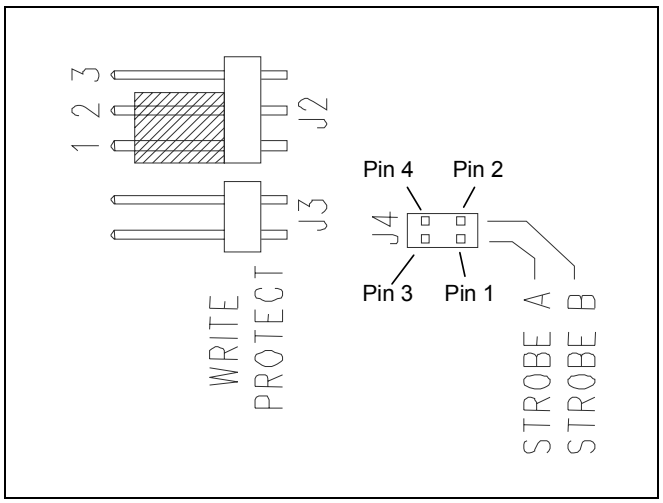


Figure 3-1 Jumper and Strobe Header Locations

RESET MODE JUMPER (J2)

Reset Mode jumper (J2) is a special jumper that is used if the host system exhibits "glitches" on the PCI Reset line that causes the board to not configure itself properly during initialization. Figure 3-1 shows the factory default (normal mode) jumper location for J2 (shunt pins 1 and 2). This jumper location is for systems that do not exhibit the glitch. If your system does not boot properly, then move the jumper shunt to pins 2 and 3. Contact Systran Customer Support for more information.

V3 EEPROM WRITE PROTECT JUMPER (J3)

The V3 EEPROM Write Protect Jumper (J3) enables/disables the write protect for the V3 PCI Bridge chip (U4) configuration EEPROM (U1). This EEPROM contains the information necessary to initialize the V3 chip in the PCI system. The factory setting for J3 is write-protect enabled (no shunt installed). Normally, it will not be necessary to modify the configuration EEPROM. However, the EEPROM may be altered if necessary by installing a shunt to J3 that permits write-access to the EEPROM. Note that this jumper is used in the procedure called out in Appendix E.

CPCISC2 IP MODULE STROBE CONNECTOR (J4)

The IP Module Logic Bus connector has a signal called "$\overline{\text{STROBE_X}}$" and is user-defined by the IP Module Logic Bus Specification. On the CPCISC2, each of the strobe signals is provided through J4 with the IP Module slot "A" strobe signal on pin 1 and slot "B" on pin 2, and pins 3 and 4 connected to ground, as indicated in Table 3-3. Each of the strobe signals on the CPCISC2 is pulled-up to +5 V via 10 KΩ resistors. The strobe connector (J4) is located as shown in Figure 3-1.

Table 3-3 CPCISC2 STROBE Connector Pin Assignments

Pin Number	Signal Name
1	$\overline{\text{STROBE_A}}$
2	$\overline{\text{STROBE_B}}$
3	GROUND
4	GROUND



CAUTION: The silk-screen numbering for the J4 header may be incorrect on your CPCISC2 board. Figure 3-1 shows the correct numbering.

3.4.2 Time-out Jumper (J5)

Although the PCI bus allows a maximum number of clock cycles before a retry, it is still possible for an incorrectly addressed IP Module to "hang" the local side of the bridge IC by not returning an acknowledge signal. Consequently, there is a potential for a wrongly addressed, faulty or missing IP Module to cause an endless string of PCI retries unless the carrier produces its own local time-out to release the bus.

In other cases, it may not be desirable for the carrier to abort a transaction. For example, when used for diagnostic purposes or for use as an IP Module with a very high number of specified wait states. For this reason, the CPCISC2 allows a jumper-selectable enable/disable of the Time-out feature. The enable/disable selection determines the time-out operation for **all** IP Module positions on the CPCISC2—either the time-out feature is enabled for all positions or it is disabled for all positions.

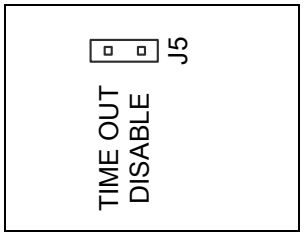


Figure 3-2 Time-out Jumper (shunt removed)

To **enable** the time-out feature, remove the shunt from header J5 (factory default) and set the TO_EN bit in the Carrier Control Register to a '1'. The CPCISC2 will now abort any transaction to an IP Module after a maximum of 29 wait states (slightly less than four microseconds) if the selected IP Module fails to assert an acknowledge. After this time has elapsed, any data returned to the PCI bus is invalid.

To **disable** the time-out feature, place the shunt across both pins on J5 (or leave the shunt for header J5 off and set the TO_EN bit in the Carrier Control Register to a '0'). The CPCISC2 will now allow an indefinite number of IP Module wait states.

NOTE: The CPCISC2 is shipped with the time-out feature **disabled** (since the TO_EN bit in the carrier control register powers up to a '0'). If you choose to enable time-out feature, follow the previous instructions.



If you choose to leave the time-out feature disabled:

1. Verify that an IP Module selected for use on the CPCISC2 produces the correct acknowledge signal before placing it on the carrier.
2. Verify that the software address used for accessing an IP Module on the CPCISC2 agrees with the physical address of the IP Module in the system.



CAUTION: Attempting to access an IP Module that is either not physically present or not correctly addressed on the CPCISC2, or is faulty, may cause an endless string of PCI retries.

3.4.3 Installation of I/O Cables

Installation of I/O cables to the CPCISC2 is similar to procedures for VME-based I/O carriers including Systran's VME35C2. Based on the 3U VME form factor, the CPCISC2 CPCI carrier has two 50-pin IDC headers. Refer to Figure 3-3 for the following discussion.

The IP module B I/O connector (J7) is located on the board behind the front panel. Therefore, you must install the cable before inserting the card into its host chassis. Install the 50-pin ribbon cable by folding the ribbon cable lengthwise in order to insert it into the slot cutout in the front panel. The J7 connector is keyed. However, if the cable being used is not, then line up the pin 1 indicators (usually a small triangle on the connector) and firmly insert the cable connector into the board connector until fully seated. The IP module A I/O connector (J6) is accessible from the front panel without removing the board from the chassis. Simply line up the pin 1 indicators on both connectors and firmly insert into the board connector.

Tagging each cable with a unique code using adhesive labels or permanent ink marker is recommended.

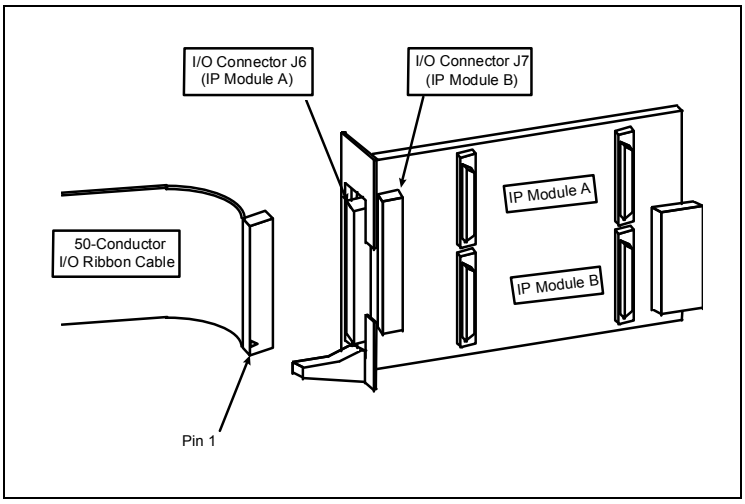


Figure 3-3 I/O Cable Installation

3.4.4 Installing CPCISC2 Into a CompactPCI Chassis

Before installing the CPCISC2 into a CPCI chassis, the IP modules should be installed firmly in place. Then, be sure that the P1 connector in the chassis's backplane has the correct voltage key. The key is a blue plastic insert in the middle of the P1 bottom connector of each slot. The blue key denotes 5-volt operation. The CPCISC2 will not insert correctly into a backplane that has a key color other than blue.

Slide the CPCISC2 into the slot until the guide pin shown in Figure 3-4 slides into the sleeve in the chassis and the connector at the back of the CPCISC2 begins to insert into the backplane connector. With the locking insert in the handle pulled out, push the handle inward toward the front panel of the CPCISC2 until the board rests firmly in the slot. Then push the locking insert in the handle until it snaps in position. Tighten the phillips head screw in the front panel into the chassis if threaded holes have been provided for that purpose.

To remove a CPCISC2 from a chassis, simply loosen the phillips head screws, snap out the locking insert and push the handle gradually yet firmly away from the front panel. When the board pops loose from the backplane connectors, slide it out of the chassis and check to ensure that the voltage key in the J1 connector remains intact.

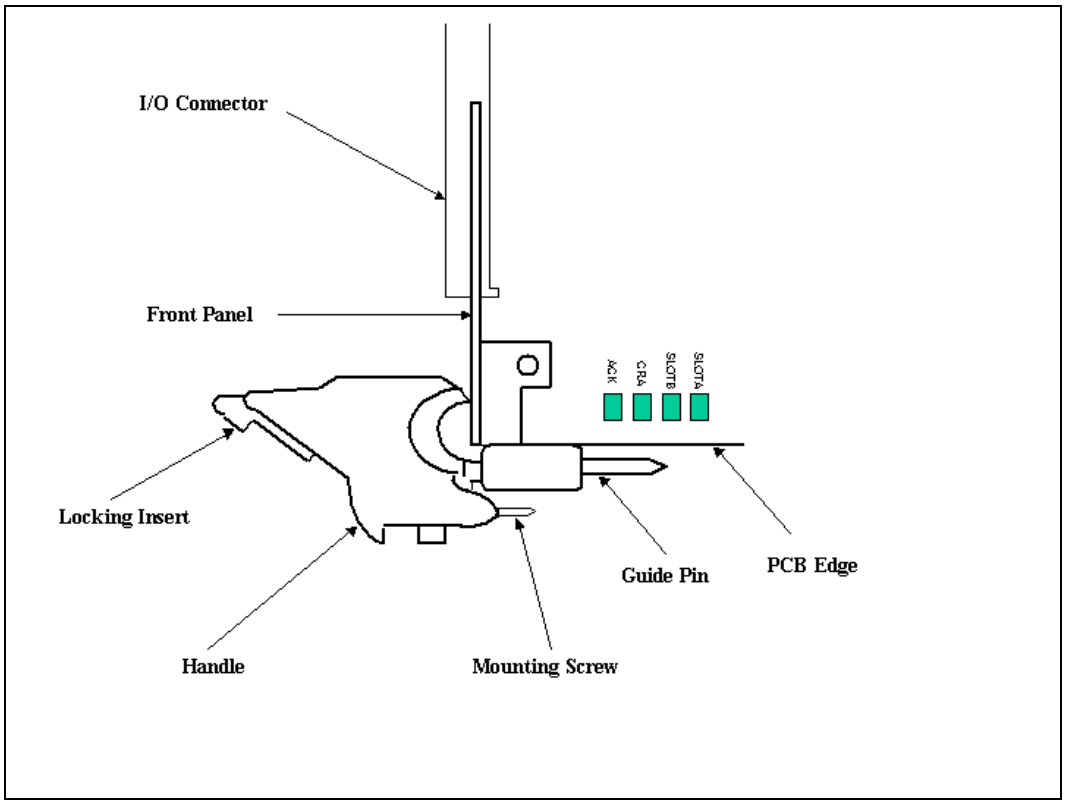


Figure 3-4 Locking Handle Detail

3.4.5 Installation of IP Modules on the CPCISC2

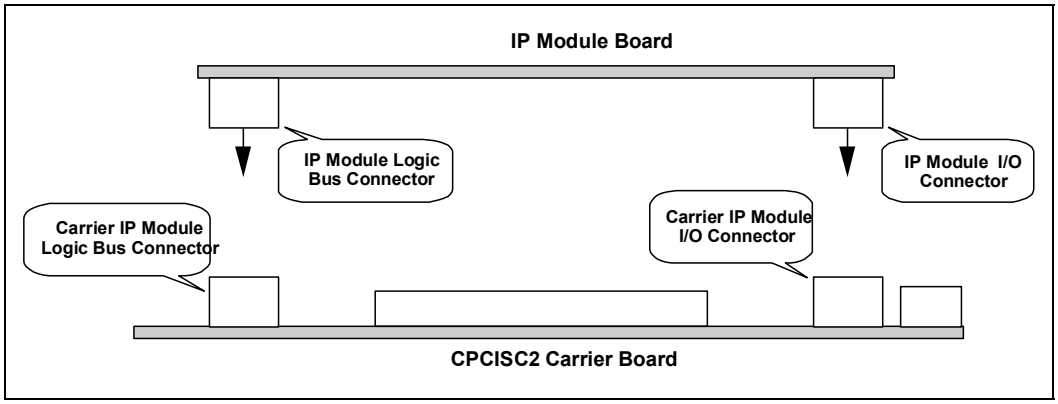


Figure 3-5 Installation of an IP Module on the CPCISC2

Referring to the appropriate figures and table described below, perform the following steps in removing the CPCISC2 from its shipping container (or from an existing installation) and installing IP Modules. The asterisk (*) denotes optional items.

1. Turn off all power to the CPCI backplane.
2. Remove the CPCISC2 from its shipping container and move it to the ESD-controlled area where the installation of the IP Module (s) can be made.

*2a. Remove the CPCISC2 from the CPCI backplane if modifications are necessary, and move it to an ESD-controlled area where the installation or changing of IP Modules can be made.

3. Set the Time-out-disable jumper (J5), the EEPROM Write Protect Jumper (J3), and Reset Mode Jumper (J2) to the desired positions.
4. Install the IP Module (s) onto the carrier board by applying adequate and equal pressure to the IP Module(s) at both ends and on the CPCISC2 board.

*5. Install four M2x5mm flat head machine screws onto the IP Module's connectors.

*6. Install any required I/O cables onto the CPCISC2.

7. Slide the CPCISC2 into a desired peripheral slot of a CPCI backplane while applying enough force to ensure a tight fit into the backplane connector. Note that the J1 connector on the CPCISC2 has a blue colored plastic key guide in the connector's center. This denotes the board as 5 V compatible. If the CPCISC2 does not fit into the chassis, check to make sure the chassis has a 5 V backplane. After insertion, use a standard phillips head screwdriver to secure the CPCISC2 panel onto the frame of the CPCI chassis.

* Optional procedure

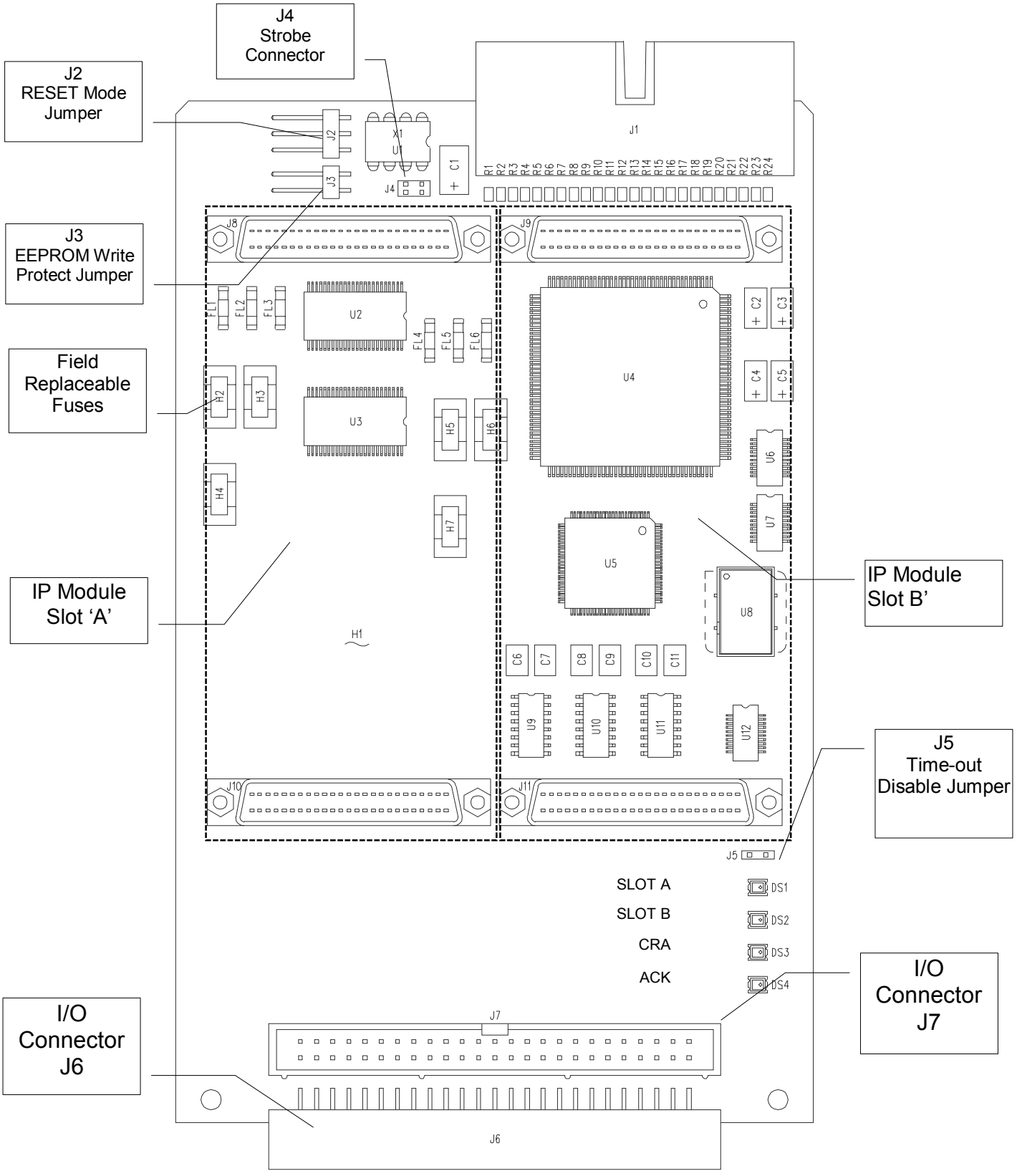


Figure 3-6 CPCISC2 Mechanical Assembly

3.4.6 Connector Pin Assignments

Table 3-4 contains the pin assignments for the PCI signals, power, ground and other pertinent connections made to the J1 connector that interfaces to the CPCI backplane. Note that the J1 connector has six columns of pin positions labeled A through F with column F providing connections for a shield ground. There are twenty-five rows of pins with rows 12 through 14 not used since this area of the connector is designated for the voltage key.

Table 3-4 PCI Bus Pin Assignments

25	5 V	REQ64#	ENUM#	3.3 V	5 V	GND	
24	AD[1]	5 V	V(I/O)	AD[0]	ACK64#	GND	
23	3.3 V	AD[4]	AD[3]	5 V	AD[2]	GND	
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	3.3 V	AD[9]	AD[8]	M66EN	C/BE[0]	GND	
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	J
19	3.3 V	AD[15]	AD[14]	GND	AD[13]	GND	1
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	3.3 V	SDONE	SBO#	GND	PERR#	GND	
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	3.3 V	FRAME#	IRDY#	GND	TRDY#	GND	
12-14	**KEY AREA**						
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	C
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	O
9	C/BC[3]#	IDSEL	AD[23]	GND	AD[22]	GND	N
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	N
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	E
6	REQ#	GND	3.3V	CLK	AD[31]	GND	C
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	T
4	BRSVP1A4	GND	V(1/O)	INTP	INTS	GND	O
3	INTA#	INTB#	INTC#	5V	INTD#	GND	R
2	TCK	5V	TMS	TDO	TDI	GND	
1	5V	-12V	TRST#	+12V	5V	GND	
Pin	**A**	**B**	**C**	**D**	**E**	**F**	

Table 3-5 shows the pin assignments for each IP Module Logic Bus connector. The signals on the left side of the table are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. The upper case "X" in the Systran signal name represents the "A" or "B" mnemonic for each IP Module slot for memory, I/O, ID, or interrupt transfers.

Table 3-5 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names	Bussed or Unique	X = Pulled Up Via 10 KΩ Resistor
GND	50	GND	GND	GND
Reserved	49	RESERVED1	U	X
Ack*	48	$\overline{\text{ACK_X}}$	U	X
A6	47	IPA6	B	
Strobe*	46	$\overline{\text{STROBE_X}}$	U	X
A5	45	IPA5	B	
Intreq1*	44	$\overline{\text{INTREQ_X1}}$	U	X
A4	43	IPA4	B	
Intreq0*	42	$\overline{\text{INTREQ_X0}}$	U	X
A3	41	IPA3	B	
Error*	40	$\overline{\text{ERROR_X}}$	U	X
A2	39	IPA2	B	
DMAEnd*	38	$\overline{\text{DMAEND_X}}$	U	X
A1	37	IPA1	B	
Reserved	36	RESERVED2	U	X
IOSel*	35	$\overline{\text{IOSEL_X}}$	U	
DMAck0*	34	$\overline{\text{DMACK_X}}$	U	X
IntSel*	33	$\overline{\text{INTSEL_X}}$	U	
DMAReq1	32	$\overline{\text{DMAREQ_X1}}$	U	X
MemSel*	31	$\overline{\text{MEMSEL_X}}$	U	
DMAReq0	30	$\overline{\text{DMAREQ_X0}}$	U	X
IDSel*	29	$\overline{\text{IDSEL_X}}$	U	
R/W*	28	R/W_X	B	
+5V	27	+5VDC	+5 Vdc	+5 Vdc
GND	26	GND	GND	GND
GND	25	GND	GND	GND
+5V	24	+5VDC	+5 Vdc	+5 Vdc
+12V	23	+12VDC	+12 Vdc	+12 Vdc
-12V	22	-12VDC	-12 Vdc	-12 Vdc
BS1*	21	$\overline{\text{BS_X1}}$	B	
BS0*	20	$\overline{\text{BS_X0}}$	B	
D15	19	DATA_X15	B	X
D14	18	DATA_X14	B	X
D13	17	DATA_X13	B	X
D12	16	DATA_X12	B	X
D11	15	DATA_X11	B	X

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names	Bussed or Unique	X = Pulled Up Via 10 KΩ Resistor
D10	14	DATA_X10	B	X
D9	13	DATA_X9	B	X
D8	12	DATA_X8	B	X
D7	11	DATA_X7	B	X
D6	10	DATA_X6	B	X
D5	9	DATA_X5	B	X
D4	8	DATA_X4	B	X
D3	7	DATA_X3	B	X
D2	6	DATA_X2	B	X
D1	5	DATA_X1	B	X
D0	4	DATA_X0	B	X
Reset*	3	$\overline{\text{RESET_X}}$	U	
CLK	2	ICLK_X	U	
GND	1	GND	GND	GND



NOTE: The IP Module data bus, usually defined as IPD[15:0] for all of our IP Modules, is a subset of the information that appears on these signal lines. Since carrier register information also uses these signal lines, the bus was defined as the "CPCISC2 Local Data Bus" designated as DATA_X[15:0].

3.5 CPCISC2 PCI Base Address

The CPCISC2 PCI base address space is divided into two sections called apertures. The first aperture set in the board's PCI configuration space is aperture 0 which is set for a total of 1 MB of PCI memory space. This aperture contains the address space for I/O, ID, Interrupt Acknowledge and all of the CSR registers on the carrier itself. The second aperture, aperture 1, is set for 32 MB and is exclusively for memory accesses to the two IP modules. 16 MB is allotted to each IP module since the transactions between the PCI bridge circuit and the IP modules themselves are 32-bit. Note that all accesses to the CPCISC2 will be performed on four byte boundaries.



NOTE: The base address set from the BIOS for aperture 0 is termed Base 1 while the address set for aperture 1 will be termed Base 2.



NOTE: The mapped PCI memory space is controlled by the BIOS on the system board, and is not normally something you can control. Use caution when changing the base address of the CPCISC2 after power-up. The amount of memory space required for the CPCISC2 is provided by the EEPROM upon power-up. You can disable this space if necessary, by using the **PciCfg** utility described in Appendix E.

Refer to Appendix B. for details of PCI accesses to the CPCISC2 on-board registers or IP Modules.

The CPCISC2 memory base addresses are set in hardware for all IP Modules as below:

- PCI Base2 + 0x0000 0000 for the first location of IP A Memory.
- PCI Base2 + 0x0100 0000 for the first location of IP B Memory.

ACCESS EXAMPLE

Let's assume you desire to access the fourth memory location on IP Module B. This would be IP Module address 0x0000 0003 (four byte boundary) on IP Module B. This equates to CPCISC2 Local Bus address 0x0100 0000 + 0x0000 000C or 0x0100 000C being accessed from the host system. If the BIOS system gives the CPCISC2 a base2 address of, say, 0xF800 0000, then the address on PCI when ~FRAME is asserted will be 0xF900 000C. The bridge IC on the CPCISC2 will strip away the PCI base address and present 0100 000C to the IP bus controller. The controller in turn will decode the upper address bits and begin a memory transaction to address 0x0000 0003 on IP Module B.

Accesses to I/O, ID and interrupt acknowledge cycles are done in exactly the same manner. For addresses to these areas, refer to Appendix B.

APPENDIX A

SPECIFICATIONS

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A.1 Specifications

Physical Dimensions	6.30 inches by 3.94 inches (160 mm by 100 mm)
Weight	5.44 oz (154 g) (includes faceplate)
Board Thickness	0.062 inches (0.157 cm), nominally (6 layers)
Power (No IPs installed)[1]	+5 VDC (±5%) @ 211 mA +12 VDC @ 0.0 mA -12 VDC @ 0.0 mA



NOTE: The CPCI bus ground and IP Module ground are not isolated through this board.

Absolute Maximum Ratings

Supply voltage with respect to ground...	Minimum	Maximum
+0.5 VDC	-0.5 VDC	+7.0 VDC
+12.0 VDC	IP Module dependent	
-12.0 VDC	IP Module dependent	

Recommended Operating Conditions

Supply voltage with respect to ground...	+4.75 VDC to + 5.25 VDC
Logic Interface	ANSI/VITA 4-1995 Specification-compliant carrier
Operating Temperature Range	0° to 70° Celsius
Storage Temperature Range (No bias)	-40° to 85° Celsius
Humidity Range	5% to 95% (non-condensing)

Mean Time Between Failure (MTBF)[2]

MIL-HDBK-217F	381,672 hours
Bellcore, Issue 6	864,394 hours

1. The CPCI bus ground and IP Module ground are not isolated through this board.
2. The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

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APPENDIX B

PROGRAMMING GUIDE

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B.1 Overview

This appendix describes the operation of the CPCISC2 from the software perspective, detailing the CPCISC2 registers and the overall mapping and addressing scheme for the board, and provides programming examples. A more detailed description of the hardware is found in Chapter 2. and Chapter 3. Application concepts are discussed in Appendix D.

B.2 Description

The CPCISC2 is an easy-to-use CPCI slave card that holds two singlewide, or one doublewide IP Modules. In addition to providing access to the I/O and ID space of the IP Modules via the CPCI backplane, the CPCISC2 has four locations to perform interrupt acknowledge cycles on the IP Modules, and four on-board control/status registers.

B.3 PCI Configuration Space

The CPCISC2, like all PCI-compliant devices, contains an address space specifically devoted to device identification, as well as memory and I/O configuration. For a comprehensive listing of the configuration register space contents, see the information presented in Table C-1.

B.4 Board Base Address

The CPCISC2 uses a total of 33 Mbytes of PCI memory space. This space is divided into two parts: a 1 MB section for I/O, ID, INT ACK and board registers (starting with Base1) and a 32 MB section for memory transactions to both IP modules (starting with Base2). These different addressable areas are set in two different apertures in the PCI configuration space of the CPCISC2. Other configurations are possible. Contact Systran for information regarding additional setups for memory space other than those mentioned in Appendix E. For more information on the base address, see Chapter 3.

B.5 Address Map

The IP Module I/O and ID, and the carrier's control, status, and general-purpose registers, reside at a fixed relative address from the CPCISC2 Base1 address.

The IP module memory space for both IP modules reside at fixed Base2 address locations relative to the CPCISC2 Base2 address. Table B-1 shows the complete memory map for the board.

Table B-1 CPCISC2 Address Map

Address Space or Register Name	Local Address (relative to board base address)	Size
Base1		
IP Module A I/O	Base1+0x000	128 bytes*
IP Module A ID	Base1+0x100	128 bytes*
IP Module B I/O	Base1+0x200	128 bytes*
IP Module B ID	Base1+0x300	128 bytes*
IP Module Reset Register	Base1+0xA00	2 bits
Error Status Register	Base1+0xA04	2 bits
Carrier Control Register	Base1+0xA08	4 bits
IP Module A IRQ0 Register	Base1+0xB00	8 bits
IP Module A IRQ1 Register	Base1+0xB04	8 bits
IP Module B IRQ0 Register	Base1+0xB08	8 bits
IP Module B IRQ1 Register	Base1+0xB0C	8 bits
Interrupt Steering Register	Base1+0xB28	5 bits
Base2		
IP Module A Memory Base	Base2+0x000 0000	8 MB*
IP Module B Memory Base	Base2+0x100 0000	8 MB*

* This denotes the actual number of bytes used by the respective address space. For each 32-bit memory location, only the lower 16 bits are actually used. The CPCISC2 and any installed IP Modules are typically accessed via 8-bit or 16-bit operations. If 32-bit operations are used, the upper 16-bits are discarded by software.

B.6 Register Descriptions

The CPCISC2 registers are accessed as byte (8-bit) or word (16-bit) values. The unused bits are driven as 0's (or 1's for D15-D8) on reads. All unused bits are discarded on writes. The hexadecimal addresses for the registers shown below are relative to the board base address.

B.7 Word Access Address Translation

The following table shows the relationship between PCI space addresses and the IP Module address for word accesses. In the table, BASE represents the I/O, ID, or memory base address. All addresses are in hexadecimal.



NOTE: By default, the PCI_BASE0 and PCI_BASE1 aperture's byte swapping is disabled by the appropriate bits in the PCI_MAP0 and PCI_MAP1 registers. If these bits are changed to implement byte swapping in the PCI interface, the following table will no longer be correct.

Table B-2 Word Access Address Translation Table

PCI bus Address	IP Module Address
BASE + 0x0	IPA = 0x00
BASE + 0x4	IPA = 0x01
BASE + 0x8	IPA = 0x02
BASE + 0xC	IPA = 0x03
BASE + 0x10	IPA = 0x04
BASE + 0x14	IPA = 0x05
BASE + 0x18	IPA = 0x06
BASE + 0x1C	IPA = 0x07
BASE + 0x20	IPA = 0x08
BASE + 0x24	IPA = 0x09
BASE + 0x28	IPA = 0x0A
...	...
BASE + 0xFC	IPA = 0x3F

B.8

B.9 Byte Access Address Translation

The following table shows the relationship between PCI space addresses and the IP Module address for byte accesses. In the table, BASE represents the I/O, ID, and memory base address. All addresses are in hexadecimal.



NOTE: By default, the PCI_BASE0 and PCI_BASE1 aperture's byte swapping is disabled by the appropriate bits in the PCI_MAP0 and PCI_MAP1 registers. If these bits are changed to implement byte swapping in the PCI interface, the following table will no longer be correct.

Table B-3 Byte Access Address Translation Table

PCI bus Address	IP Module Address	Byte Lane*
BASE + 0x0	IPA = 0x00	0
BASE + 0x1	IPA = 0x00	1
BASE + 0x4	IPA = 0x01	0
BASE + 0x5	IPA = 0x01	1
BASE + 0x8	IPA = 0x02	0
BASE + 0x9	IPA = 0x02	1
BASE + 0xC	IPA = 0x03	0
BASE + 0xD	IPA = 0x03	1
BASE + 0x10	IPA = 0x04	0
BASE + 0x11	IPA = 0x04	1
…	…	…
BASE + 0xFC	IPA = 0x3F	0
BASE + 0xFD	IPA = 0x3F	1

* Byte-lane 1 not applicable for ID Space

B.9.1 Reset Register (0xA00)

Setting one of the bits RES_B and RES_A to '1' asserts the corresponding IP Module's reset line. You can set the bits individually by writing a '1' to that bit or simultaneously with a single write of '0x3.' When set, a one-shot is triggered supplying a minimum 200 ms reset pulse as required by the IP Module specification. When read, these bits return the status of the corresponding IP Module's reset line (a '0' means the IP Module is not being reset, a '1' means it is in a reset condition).

Table B-4 Reset Register Bit Description

Bit #	B15-B8	B7-B2	B1	B0
Bit Name	Not Used	Not Used	RES_B	RES_A
R/W	Reads '1's Writes discarded	Reads '0's Writes discarded	R/W	R/W
Power-up State	N/A	N/A	0	0

NOTE: RES_B-RES_A: Reset bits for IP Module slots B and A.

B.9.2 Error Status Register (0xA04)

These bits indicate the state of the corresponding IP Module ERROR_X signal (pin #40 on a given IP Module). If the ERROR_X signal is asserted (active low) for a particular IP Module, then the corresponding ERR_X bit will be set to a '1'. If the error signal is not asserted, then the corresponding bit will be cleared.

Table B-5 Error Status Register Bit Description

Bit #	B15-B8	B7-B2	B1	B0
Bit Name	Not Used	Not Used	ERR_B	ERR_A
R/W	Reads '1's Writes discarded	Reads '0's Writes discarded	R	R
Power-up State	N/A	N/A	State of IP Module B ERR* Signal	State of IP Module A ERR* Signal

NOTE: ERR_B-ERR_A: Error Status bits for IP Module slots B and A.

B.9.3 Carrier Control Register (0xA08)

This register contains bits that are used to enable interrupts and implement the time-out function on the CPCISC2. Table B-6 shows the bits in the Carrier Control register. A brief description of each bit follows.

- The IP_INT_EN bit must be set to a '1' to enable IP Module interrupt requests to assert a PCI interrupt. This is necessary to prevent interrupts from occurring before the application software has installed an appropriate interrupt service routine.
- The TO_EN bit is used to enable the time-out function. When this bit is set to a '1' and the time-out jumper (J5) is enabled (shunt removed), the carrier completes the local bus transaction after 30 IP Module clock cycles have elapsed from the start of an IP Module access. This time-out feature is used to prevent the local bus of the CPCISC2 from "locking up" if an IP Module access fails.
- The TO_INT_EN bit is used in conjunction with the TO_EN bit to generate a PCI interrupt when a time-out occurs. When this bit is set to a '1' and the time-out jumper (J5) is enabled (shunt removed), the CPISC2 generates a PCI interrupt to alert the software that an IP Module access was unsuccessful.
- The TO_STAT bit indicates if a time-out occurred. This bit is set to a '0' when an IP Module access is successful and it is set to a '1' when a time-out occurs.

Table B-6 Carrier Control Register Bit Description

Bit #	B15-B8	B7-B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	TO_STAT	TO_INT_EN	TO_EN	IPINT_EN
R/W	Reads 1's Writes discarded	Reads 0's Writes discarded	R	R/W	R/W	R/W
Power-up State	N/A	N/A	0	0	0	0



NOTE: Do not enable the time-out feature if using an IP Module that asserts more than 28 wait states.

B.9.4 Interrupt Vector Registers for IP Modules A and B (0xB00 through 0xB08)

The four interrupt vector registers (two per IP Module) are 8-bit, read-only registers. When one of these registers is read, an appropriate interrupt acknowledge cycle is performed on the corresponding IP Module. These registers reflect the vector driven on the IP Module data bus during the appropriate interrupt acknowledge cycle. These registers are useful for IP Modules that have a ROAK (release on acknowledge) interrupt mechanism, as the PCI interrupt cycle is not vectored, unlike some other buses (e.g., VME). This means a ROAK-type IP Module will need to use these registers to clear the interrupt source. Software for RORA (release on register access) IP Modules will typically not use these registers.

Table B-7 Interrupt Vector Registers

Address	Interrupt Vector Register	Address	Interrupt Vector Register
Base + B00	IP Module 'A' Intreq0	Base + B04	IP Module 'A' Intreq1
Base + B08	IP Module 'B' Intreq0	Base + B0C	IP Module 'B' Intreq1

B.9.5 Interrupt Steering Register (0xB28)

The Interrupt Steering Register is a 5-bit register consisting of an interrupt-status bit for each of the two interrupt-request lines for each IP Module, and one local time-out status bit. This register is typically read in the Interrupt Service Routine to determine which interrupt source(s) is (are) being asserted. A table of the bits in the Interrupt Steering Register is shown below. A write to this register will clear a pending time-out-interrupt request.

Table B-8 Interrupt Steering Register

Bit #	B15-B8	B7-B5	B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	TO_INT	IRQ1 B	IRQ0 B	IRQ1 A	IRQ0 A
R/W	Reads '1's Writes discarded	Reads '0's Writes discarded	R/W	R	R	R	R
Power-up State	N/A	N/A	0	0	0	0	0



NOTE: Each bit will be a '1' when the corresponding interrupt is set.

B.10 Programming Examples

The following examples illustrate how to program the CPCISC2 to achieve various operational modes.

B.10.1 Reset Example

This example resets one, then both IP Modules, and then monitors the reset signals to determine when they are de-asserted. Setting a bit in the reset register causes a one-shot to assert the corresponding IP Module reset signal (the one-shot asserts the reset signal for approximately 240 ms). The reset signal can then be monitored by reading the Reset register to determine when it is de-asserted.

- Write '0x01' to the Reset register. This resets the IP Module in slot A by asserting the IP Module A reset signal.

LOOP1:

- Read the Reset register.
- If Bit 0 is set then go to LOOP1.
- Write '0x3' to the Reset register. This resets both IP Modules by asserting their corresponding reset signals.

LOOP2:

- Read the Reset register.
- If any of bits [1:0] are set then go to LOOP2.

B.10.2 Interrupt Initialization Example

The system board in the PCI-based CPCI system senses interrupts at an active-low level with the PCI INTA# interrupt-request line remaining at a logic-low until the system CPU has accessed any necessary registers and removed the interrupt source. On the CPCISC2, interrupts are disabled at power-up and must remain disabled until the entire system is properly initialized. After this, you can enable IP Module and time-out interrupts by writing the appropriate bits to the Control Register on the CPCISC2. The interrupt line from the CPCISC2 (PCI INTA#) is asserted from any one of the five possible sources. Four of the sources are from N_INTREQ0 and N_INTREQ1 from each of the two IP Modules and the fifth source is from a time-out interrupt-status bit that is set in the IP Module interface controller. You can find the status of these interrupt requests by reading the Interrupt Steering Register on the CPCISC2.

An example is given in Appendix D.

APPENDIX C

PERFORMANCE

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C.1 Overview

The purpose of this appendix is to provide several sets of empirical data that represent typical performance parameters beyond those provided in the specification. It is important to note that these are **typical** responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Chapter 2. and Appendix A.

These parameters were taken with the CPCISC2 installed in a typical 166 MHz Pentium , 33 MHz PCI bus PC system. Test software was running in DOS mode. Results from any other system configuration will vary from those shown here. The CPCISC2 hardware and the IP Module bus times (assuming no WAIT states) will remain relatively the same as those shown.

C.2 PCI Data Transfer Performance

Data transfers to three different areas on the CPCISC2 are performed via the PCI bus: Control/Status Register (CSR) area, IP Module (I/O, ID, & Memory) area, and V3 chip register area. Each area has its own unique access time and therefore, performance aspects.

Performance information for the CSR and IP Module is provided in the subsequent subsections. Performance information for the V3 chip register area is included in the discussion on Interrupt Latency in section C.3.

C.2.1 CSR Write/Read Cycles

CSR accesses involve the registers internal to the Altera EPLD. These registers include the Reset Register, the Error Status Register, Carrier Control Register, the IP Module IRQ Registers, and the Interrupt Steering Register (ISR).

WRITE CYCLES

Write-cycle performance is aided by having the Write Posting feature enabled on the V3 chip. This, coupled with the V3's write FIFO, allows for maximum write performance from the PCI bus to the CPCISC2 CSR area. This means that PCI write cycles are acknowledged almost immediately by the V3 chip on the PCI bus. However, the write to the addressed CSR register does not actually take place until an "acknowledge" is generated by the Altera chip on the V3's local bus side. Figure C-1 is a graphical representation of the cycles involved during a CSR Write followed by the times for the cycles involved.

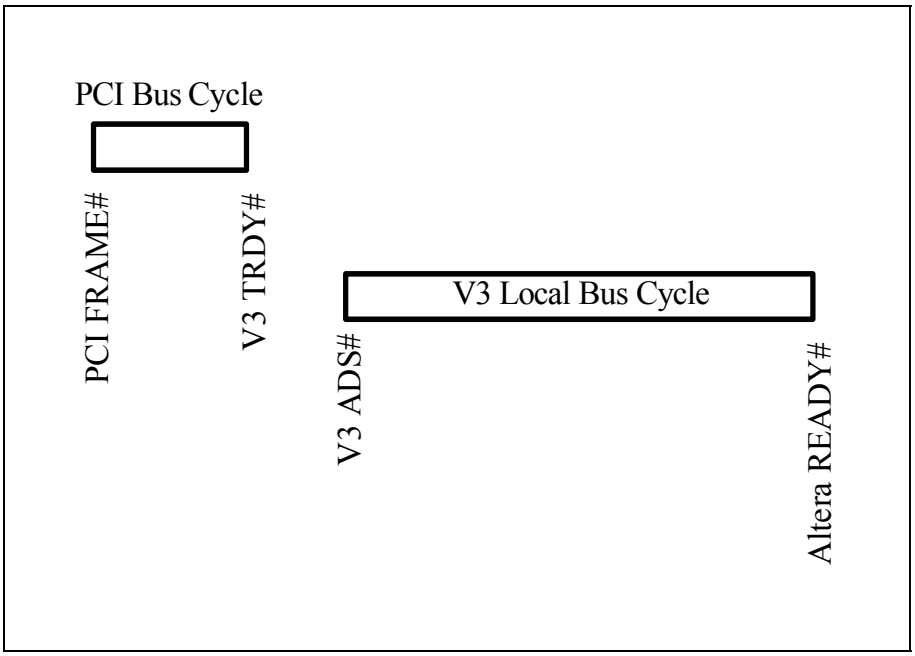


Figure C-1 CSR Write Cycle

PCI bus FRAME# to V3 TRDY# (data Write Posted)	90.0 nsec	*
PCI FRAME # to V3 ADS# (begin local bus cycle)	200.0 nsec	
V3 ADS# to Altera READY# (end local bus cycle)	62.5 nsec	
Total cycle time	262.5 nsec	

* PCI bus is free at this time.

READ CYCLES

Read accesses to these register will be faster than the IP Module areas but not as fast as the V3 register area. Transfers to this area go through the V3 first and then the Altera. Unlike Write Posting, the PCI bus must wait until the read data is ready from the Altera and placed on the bus and the V3 asserts TRDY# before the cycle is finished. Figure C-2 is a graphical representation of the cycles involved during a CSR Read followed by the times for the cycles involved.

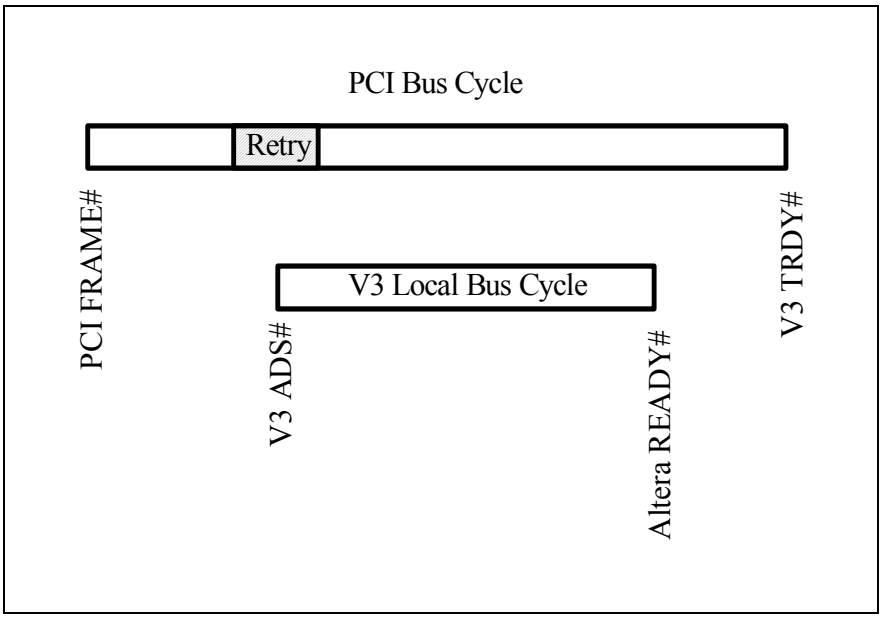


Figure C-2 CSR Read Cycle

PCI bus FRAME# to V3 ADS# (begin local bus cycle)	200 nsec
V3 ADS# to Altera READY# (end local bus cycle)	125 nsec
Altera READY# to V3 TRDY# (end PCI bus cycle)	215 nsec
Total cycle time	540 nsec

C.2.2 I/O, ID, and Memory Write/Read Cycles

IP Module accesses will have the slowest access time of the three areas. This is because any PCI access must go through the V3 chip, the Altera and then to the IP Module bus and wait for the IP Module to generate an acknowledge.

WRITE CYCLES

As stated before, write cycle performance is aided by Write Posting and the V3's write FIFO. However, the write does not actually take place until the addressed IP Module generates an N_ACK to the Altera and, subsequently, the Altera signals the end of the cycle with a READY to the V3 chip. Figure C-3 is a graphical representation of the cycles involved during an IP Module Write followed by the times for the cycles involved.

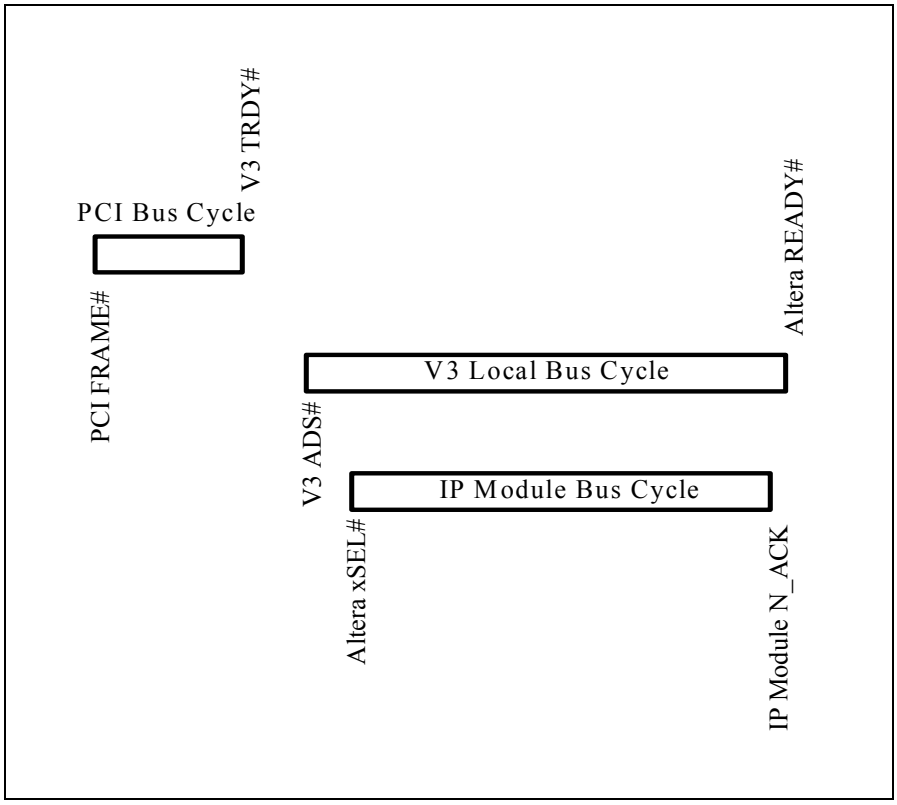


Figure C-3 IP Module Write Cycle

PCI bus FRAME# to V3 TRDY# (data Write Posted)	90 nsec	*
PCI FRAME # to V3 ADS# (begin local bus cycle)	250 nsec	
V3 ADS# to Altera xSEL# (begin IP Module bus cycle)	125 nsec	
Altera xSEL# to IP N_ACK (end IP Module bus cycle)	125 nsec	
IP N_ACK to Altera READY# (end local bus cycle)	62.5 nsec	
Total cycle time	562.5 nsec	

* PCI bus is free at this time.

READ CYCLES

One of the biggest limitations to PCI performance will be the number of PCI bus retries caused by the PCI Target not being ready with the requested data during a Read cycle. In the case of the CPCISC2, this is a function of the speed at which the Local bus is running and the number of IP Module bus WAIT states that are inserted by the IP Module during an IP Module bus cycle. Another factor would be HOLD states inserted by the IP Module carrier into the IP Module bus cycle. The CPCISC2 does not insert any HOLD states. As in the CSR reads, the PCI cycle cannot complete until the data from the addressed device (the IP Module in this case) is placed on the PCI bus and TRDY# is asserted. Figure C-4 is a graphical representation of the cycles involved during an IP Module Read followed by the times for the cycles involved.

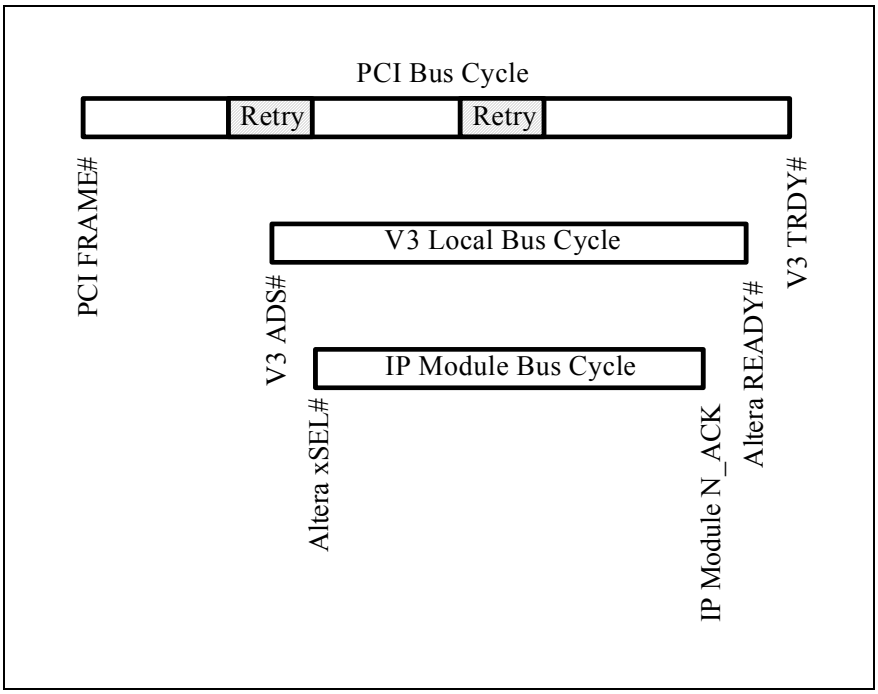


Figure C-4 IP Module Read Cycle

PCI bus FRAME# to V3 ADS# (begin local bus cycle)	187.5 nsec
V3 ADS# to Altera xSEL# (begin IP Module bus cycle)	125.0 nsec
Altera xSEL# to IP N_ACK (end IP Module bus cycle)	125.0 nsec
IP N_ACK to Altera READY# (end local bus cycle)	62.5 nsec
Altera READY# to V3 TRDY# (end PCI bus cycle)	250.0 nsec
Total cycle time	750.0 nsec

C.3 Interrupt Latency

Interrupt latency is a measure of the time that has elapsed from the generation of an interrupt to that interrupt being serviced. For the CPCISC2 the interrupt service includes a read of the Altera's Interrupt Steering Register to determine which interrupt on which IP Module occurred. An additional access to the IP Module is required in order to clear the IP Module interrupt. Also, a read and a write to the V3 chip's internal registers is required in order to clear the PCI interrupt. All register read cycle times include the time for PCI Retries. The interrupting source is from an IP Module. Figure C-5 is a graphical representation of the cycles involved during an Interrupt followed by the times for the cycles involved.



NOTE: The system Interrupt Acknowledge and Interrupt Handler software execution time is part of the overall latency and is highly dependent upon the speed of the system used and the size and efficiency of the Interrupt Handler software. For this reason, in order to quantify just the CPCISC2 hardware latency, a total time is provided with the total system times subtracted out of the total time. Actual system times will vary from those shown here.

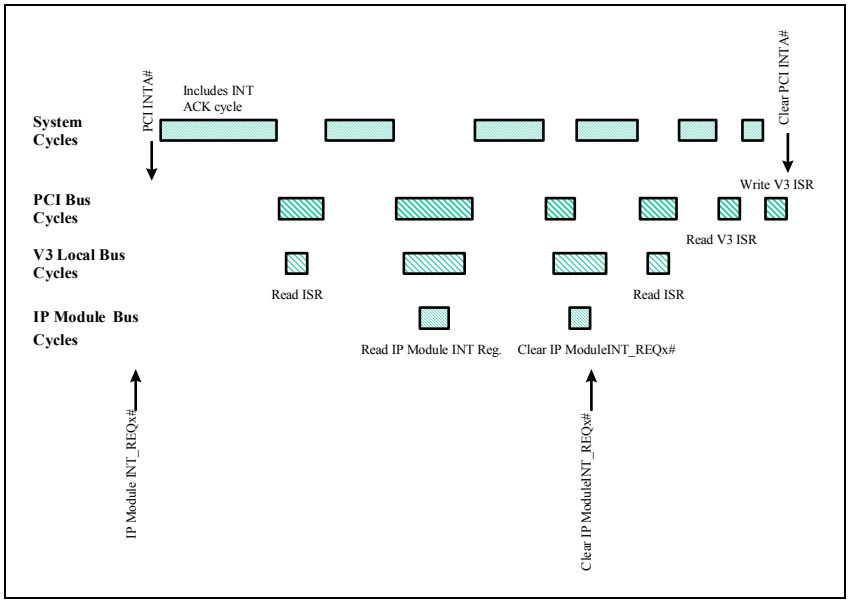


Figure C-5 Interrupt Cycle

IP Module INTx# to PCI INTA# (begin Interrupt cycle)	28.0 nsec
System Cycle (includes INT Acknowledge)	6.8 µsec *
Read INT Steering Register (determine IP INT source)	542.0 nsec
System Cycle	2.2 µsec *
Read IP Module INT Register	993.0 nsec
System Cycle	1.9 µsec *
Write IP INT Register (clears IP Module INT_REQx#)	90.0 nsec
System Cycle	963.0 nsec *
Read INT Steering Register (verify IP INT cleared)	512.0 nsec
System Cycle	512.0 nsec *
Read V3 INT Status Register	120.0 nsec

System Cycle	180.0 nsec *
Write V3 INT Status Register (clears PCI INTA#)	150.0 nsec
Total Time	14.99 µsec
Total System Cycle Time	12.55 µsec *
Total CPCISC2 & IP H/W Time (Total - System)	2.44 µsec

* System Cycles are those times when the PC system is not accessing the Interrupting hardware (CPCISC2 V3, Altera, or Interrupting IP Module registers).

C.4 962PBC Register Map

As mentioned in previous sections, the PCI_IO_BASE, PCI_BASE0, PCI_BASE1, PCI_BPARAM, and PCI_INT_STAT registers in the PBC Configuration space are necessary to access the CPCISC2. Since the above registers represent a small subset of the entire PBC space, Table C-1 provides a complete listing of the PBC registers as initialized by the on-board EEPROM. For a more detailed description of each register, contact QuickLogic at the addresses given below:

QuickLogic
1277 Orleans Drive
Sunnyvale, CA 94089 USA
Telephone: 408.990.4000
Fax: 408.990.4040
www.quicklogic.com

Table C-1 PBC Default Register Values

Name	Width	Offset	Value As Set by EEPROM
PCI_VENDOR	16 bits	0x00	0x1387
PCI_DEVICE	16 bits	0x02	0x4902
PCI_CMD	16 bits	0x04	0x0000
PCI_STAT	16 bits	0x06	0xF080
PCI_CC_REV	32 bits	0x08	0x08800000
PCI_HDR_CFG	32 bits	0x0C	0x00000000
PCI_IO_BASE	32 bits	0x10	0x00000000
PCI_BASE0	32 bits	0x14	0x00000000
PCI_BASE1	32 bits	0x18	0x01000000
PCI_SUB_VENDOR	16 bits	0x2C	0x0000
PCI_SUB_ID	16 bits	0x2E	0x0000
PCI_ROM	32 bits	0x30	0x00000000
PCI_BPARAM	32 bits	0x3C	0x00000100
PCI_MAP0	32 bits	0x40	0x00000003
PCI_MAP1	32 bits	0x44	0x02000053
PCI_INT_STAT	32 bits	0x48	0x00000000
PCI_INT_CFG	32 bits	0x4C	0x00020002
LB_BASE0	32 bits	0x54	0x00000000
LB_BASE1	32 bits	0x58	0x00000000
LB_MAP0	16 bits	0x5E	0x0000
LB_MAP1	16 bits	0x62	0x0000
LB_SIZE	32 bits	0x68	0x00000000
LB_IO_BASE	16 bits	0x6E	0x0000
FIFO_CFG	16 bits	0x70	0x0A00
FIFO_PRIORITY	16 bits	0x72	0x0F0F
FIFO_STAT	16 bits	0x74	0x0000
LB_ISTAT	8 bits	0x76	0x00
LB_IMASK	8 bits	0x77	0x00
SYSTEM	16 bits	0x78	0xC400

APPENDIX D

TYPICAL APPLICATIONS

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D.1 Applications

Systran has an open product application submission policy. You may submit your CPCISC2 Slave Carrier application(s) to us to include in our application library. If we determine the submission will expand the product's functionality, we will revise this section to include the application(s).

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

D.2 Typical Software Considerations in PC Environments



NOTE: The information in this section provides basic information for configuring the CPCISC2 if you choose to write your own driver. Systran has available driver software that automatically configures the CPCISC2. Order part number BSDR-NTASPC1E for Windows NT 4.0, and BSDR-IPWMPCI for Windows 2000 and Windows XP. If you are using this software, you do not need to understand the information in this section.

Using the CPCISC2 may initially appear daunting due to the many options provided by the PCI-interface chip V3 962PBC-B2 (hereafter referred to as "PBC") on the CPCISC2. Fortunately, the on-board EPROM initializes most of the registers and/or the BIOS on the system board and are consequently transparent to the user. Typically, the only PBC registers used by user software are the following: PCI_IO_BASE, PCI_BASE0, PCI_BASE1, PCI_BPARAM, and PCI_INT_STAT. The following examples discuss how to access the CPCISC2 with these registers and handle interrupts appropriately. This description is generic and does not specifically discuss operating system-specific implementation issues.

1. Verify that a PCI compliant BIOS is present on the system board.
2. Verify that at least one CPCISC2 is present in the system. The Device ID and Vendor ID are typically used for this purpose. For each CPCISC2 card found in the system, perform steps 3-6.
3. Perform a 32-bit read of the PCI_IO_BASE register. The result obtained by masking off the lower 8 bits (AND with 0xFFFFFF00) of this value is the base address used to access the PBC's internal registers. For purposes of this discussion, this address will be designated **CPCISC2_Config_Pointer**. This base address is used for all subsequent accesses to the PBC.
4. Perform a 32-bit read of the PCI_BASE0 register (**CPCISC2_Config_Pointer** + 0x14). The result obtained by masking off the lower 8 bits (AND with 0xFFFFFF00) of this value is the base1 address used to access the CPCISC2 registers and the IP Modules (see Appendix B. for the entire address map). For the discussion that follows, this address will be designated **CPCISC2_IP_Space_Pointer**. This base address is used for I/O, ID, Interrupt Acknowledge and carrier register accesses. It is not used for memory accesses.
5. Perform a 32-bit read of the PCI_BASE1 register (**CPCISC2_Config_Pointer** + 0x18). The result obtained by masking off the lower 8 bits (AND with 0xFFFFFF00) of this value is the base 2 address used to access the CPCISC2 IP Modules for memory transactions (see Appendix B. for the entire address map).

This address will be designated **CPCISC2_MEM_Space_Pointer** and is used for IP memory accesses only.

6. Perform a 32-bit read of the PCI_BPARAM register(**CPCISC2_Config_Pointer** + 0x3C). The lower eight bits of this value denote the interrupt line that will be used by the CPCISC2 during interrupts. For an x86-based computer, a valid interrupt line will be in the range 0 though 15. Use this value when installing an Interrupt Service Routine because the system has been configured to generate this level of interrupt to the microprocessor when the CPCISC2 asserts its interrupt request.
7. IP Modules or CPCISC2 internal registers can now be accessed as appropriate by using appropriate offsets from the board Base1 or Base2 address (**CPCISC2_IP_Space_Pointer** or **CPCISC2_MEM_Space_Pointer)**, as listed in Appendix B.



NOTE: Steps 1 though 3 are platform and/or operating-system specific. For instance, BIOS calls (or higher-level API) may be used to perform steps 1-3. After determining the **CPCISC2_Config_Pointer** in step 3, do not continue to use BIOS calls to access the hardware because they must not be invoked from an Interrupt Service Routine



NOTE: Do not overwrite the values in the PCI_IO_BASE, PCI_BASE0, PCI_BASE1 or PCI_BPARAM registers, as initialized by the BIOS. You cannot simply change these values without having potential effects on the operability of the CPCISC2 due to the "plug-and-play" nature of PCI.

D.3 Typical Interrupt Handling in a PC Environment



NOTE: The information in this section provides basic information for configuring the CPCISC2 if you choose to write your own driver. Systran has available driver software that automatically configures the CPCISC2. Order part number BSDR-NTASPC1E for Windows NT 4.0, and BSDR-IPWMPCI for Windows 2000 and Windows XP. If you are using this software, you do not need to understand the information in this section.

The previous example illustrated how to access the PCI interface chip's internal registers, the CPCISC2's registers, and any installed IP Modules. This example demonstrates how interrupts can be handled using the CPCISC2.

- Upon initialization of program, save the current address of the currently installed Interrupt Service Routine (if any) for applicable interrupt line. The interrupt line used by the CPCISC2 was determined in Step 6 of the previous example.
- Install the desired ISR for the appropriate interrupt line.
- Initialize the applicable programmable interrupt controller (8259A-type device)
- Enter the main loop of program here.
- During program's termination routine, restore the old ISR before exiting.

The following is a suggested ISR for the CPCISC2:

- If applicable for ISR, set the programmable interrupt controller (PIC) to enable higher-priority interrupts to preempt this ISR.

- Read the steering register (**CPCISC2_IP_Space_Pointer** + 0xB28) to verify that the interrupt was asserted from the CPCISC2.
- If not, call the previous ISR at this interrupt line, if any, and exit.
- If one or more interrupts from the CPCISC2, service appropriately.

The following is a typical routine, which prioritizes the IP Module interrupt requests in the following order:

IP Module A Interrupt Request 0 through IP Module B Interrupt Request 1.

```
Read Steering Register
"AND" result with 1Fh
if (non-zero)
      while result non-zero
            if (bit 0 set)
                  handle IPA - IRQ0
                  clear source
            else if (bit 1 set)
                  handle IPA - IRQ1
                  clear source
            .
            .
            .

            else if (bit 3 set)
                  handle IPB - IRQ 1
                  clear source
            reread the steering register and "AND" result with 1Fh
      Perform 32-bit read of PCI_INT_STAT (CPCISC2_Config_Pointer)
      Write this value back to PCI_INT_STAT to clear interrupt from PBC

      Issue "end-of-interrupt" command to PIC
else
      call previous ISR if exists
return from exception
```



NOTE: When processing of the interrupt(s) source(s) is complete, read the PCI_INT_STAT register and write this value immediately back to the register to clear the interrupt from the PCI interface chip. Disable the Compiler optimization to avoid removal of this code.

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APPENDIX E

PCICFG UTILITY FOR PCI-BASED CARRIERS

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Figure E-1 Application Main Window E-2

E.1 Overview

PCs are continuing to become popular IP module carrier platforms. PCI is currently the primary PC local bus standard and is widely used as slots on a PC motherboard or as the CompactPCI form factor. One reason for such popularity is the "plug-and-play" nature of PCI BIOS. However, the way PC BIOS systems map add-in card memory tends to differ from one system to another and in some cases can be problematic. Some add-in boards can be ignored or can cause a system to "hang" if they require a greater amount of memory to operate than the particular BIOS allows.

E.2 Purpose

The **PciCfg** utility allows quick and easy modification of the PCI configuration EEPROM. The modification entails an enable or disable of the memory space of the IP carrier. When memory space is disabled, only one megabyte of system space is required to place the carrier which allows proper operation in systems with a "memory sensitive" BIOS. However, if memory space is necessary, it can be enabled, which will require an additional 32 MB to 128 MB depending on which PCI-based carrier is in use.

E.3 Product Coverage

This software was designed for use with the following Systran PCI-based IP module carriers:

- BHAS-PCISC5
- BHAS-PCISC3
- BHAS-CPCISC2
- BHAS-CPCISC4
- BHAS-CPCISC4-BP, RP

This software operates under Windows NT 4.0. We did not design it to operate from another version of Windows or from DOS.



NOTE: This software is not intended for use with Systran's VME-based IP carriers or with any competitor's carrier.

E.4 Hardware Installation

The **PciCfg** utility supports up to 16 installed IP Module carrier cards on a single machine. Simply insert the cards you want to configure into any available PCI or CPCI slots on the host system. Once you install the software, you may insert or remove cards and the software will automatically identify changes when you reboot.

Install a jumper plug across the header connected to the write-protect-disable function on the carrier's EEPROM. The location of the jumper header for each carrier is listed below:

BHAS-PCISC5	Install a plug across J17 located next to the EEPROM in the upper-left end of the board with the mounting bracket facing left.
BHAS-PCISC3	Install a plug across J9 located next to the EEPROM in the upper-right end of the board with the mounting bracket facing left.

BHAS-CPCISC4	Install a plug across J3 located above the EEPROM in the lower-left end of the board with the panel and I/O connectors facing away.
BHAS-CPCISC4-BP, RP	Locate the board programming dipswitch (S1) in the upper right end of the board near the J1 CPCI bus connector. Set switch # 3 to the "up" position away from the "wpd" lettering on the board.
BHAS-CPCISC2	Install the plug across both pins on J3 located in the lower-right end of the board with the panel and I/O connectors facing away.



NOTE: The **PciCfg** program will be blocked from re-programming the EEPROM if the jumper or switch setting is not properly installed.

E.5 Software Installation

We distribute the **PciCfg** utility a standard 3.5" diskette. Insert the diskette into the host computer's removable-diskette drive. Select "Run" from the Windows NT "Start" menu and type `a:setup` in the Open edit box. The **PciCfg** installation utility will guide you through the setup process. After you install the software, reboot your system and **PciCfg** is then ready for operation.

E.6 Software Operation

To run **PciCfg**, select the appropriate icon in the **PciCfg** group of the Windows NT start menu. This brings up the main application window as shown in Figure E-1.

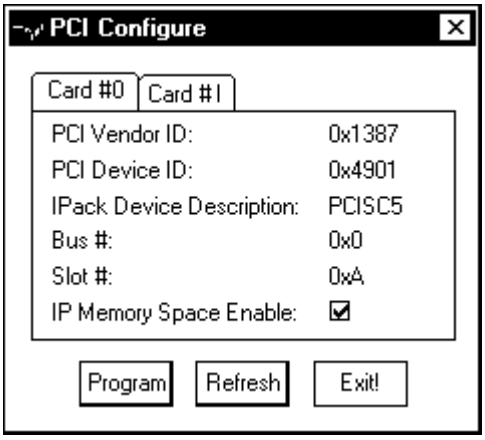


Figure E-1 Application Main Window

The main window displays the information for the first Systran IP Module carrier card found on the system. To display other devices installed on the system, simply select the appropriate "Card #" tab at the top of the window.

Various device characteristics are displayed for the selected card including PCI vendor and device ID, Systran IP Carrier model number as well as the PCI bus and slot numbers.

In addition to the general PCI information, a selection checkbox is provided to turn off the IP Memory Space. To disable, de-select the checkbox and press the **Program** button.

This reconfigures the PCI EEPROM on the selected device, effectively disabling the IP Memory Space. After you make any changes, power down your system and reboot for the new settings to take effect.

The **Refresh** button on the main display window re-reads the selected devices EEPROM and refreshes the display. The **Exit** button closes **PciCfg**.

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GLOSSARY

[x:y] ----------Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (For example: Data bus [7:0] refers to the Least Significant eight bits).

aperture ----------A region or set of addresses.

byte-lane ----------8 bits of a data bus on octal boundaries.

CSR ----------Control and Status Register.

doublewide----------An IP Module that is twice the size of the singlewide board.

interrupt latency ----------A measure of the time that has elapsed from the generation of an interrupt to that interrupt being serviced

IP Module logic bus ----------A synchronous, 4 MTransfers/sec, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

IP Module----------Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP ----------(see IP Module)

ISR ----------Interrupt Service Routine, Interrupt Status Register, or Interrupt Steering Register.

ns, µs, ms----------Nanoseconds, microseconds, and milliseconds, respectively.

singlewide----------An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

system cycles ----------Those times when the PC system is not accessing the interrupting hardware.

VHDL----------Very high-speed integrated circuit Hardware Description Language.

word ----------16 bits.

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