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DAC128F5

8-Channel 12-bit, ±5 V
Digital-to-Analog Converter
IP Module User Manual

Document No. B-T-MU-DAC128F5-A-0-A4

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GLOSSARY

[x:y]---------- Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the least significant eight bits).

Byte---------- 8 bits.

byte-lane ---------- 8 bits of a data bus on octal boundaries.

differential linearity error ---- The analog voltage error for 1 LSB input code change normalized to the full scale.

Doublewide---------- An IP Module that is twice the size of the singlewide board.

DSO ---------- Digital Storage Oscilloscope.

EPLD ---------- Erasable Programmable Logic Device.

gain error ---------- The error, including the internal reference, is the error in the slope of the transfer characteristic, often referred to as scale-factor error.

gain matching---------- The largest difference in gain error between any two DACs in a single packaged device.

ID PROM ---------- The circuitry that presents the proper data patterns to the lower 8 bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

integral linearity error --------- The maximum deviation of the actual DAC output, for any input code, from the ideal analog output as defined by a straight line from +4.9976 V → -5.000 V. This is specified as being ±1 LSB (typical, over temperature).

I/O ---------- Input/Output.

IPDbus---------- IP Module Data Bus.

IP Module---------- Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP Module logic bus---------- A synchronous, 4 MTransfers/sec, 16-bit-wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6 bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4Mwords of memory space per IP Module.

ISR---------- Interrupt Service Routine.

LSB ---------- Least Significant Bit.

Monotonic ---------- Over the full operating temperature, the ouput either increases or remains constant for increasing input codes such that the output will always be a non-decreasing function of input.

MTBF ---------- Mean Time Between Failures.

ns, µs, ms ---------- Nanoseconds, microseconds, and milliseconds, respectively.

offset error ---------- This error is applicable to all input codes equally, where it is a linear shift from the ideal.

offset matching ---------- The largest difference in offset values between any two DACs in a single packaged device.

PC ---------- Personal Computer.

scale-factor error ---------- See description under **gain error**.

Singlewide ---------- A standard IP Module printed circuit board (3.9" by 1.8") with two 50-pin connectors.

slew rate ---------- The rate of change in analog output in terms of volts/time.

VHDL ---------- Very high speed integrated circuit Hardware Description Language.

zero error ---------- The error in analog value when the input code calls for analog zero, and it is a function of both offset error and gain error.

1. 0 INTRODUCTION

1.1 Purpose

This is a reference manual for SYSTRAN's 8-channel, 12-bit, ±5 V Digital-to-Analog Converter (DAC) IP Module board, referred to in this document as the DAC128F5 (part number BHAS-DAC128F5).

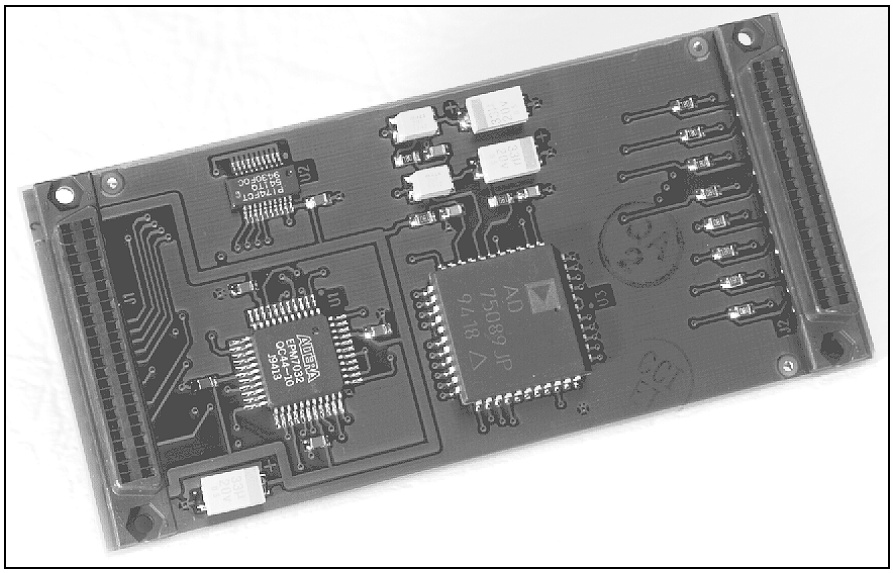


Figure 1-1 DAC128F5 Board

1.2 Scope

This reference manual covers the physical and operational description of the DAC128F5, both from hardware and software perspectives. This manual also contains detailed technical information about the DAC128F5's performance characteristics, and some typical applications. The reader should have a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IP Modules on their carrier(s) of choice. Citing equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The DAC128F5 is a singlewide IP Module board, conforming both mechanically and electrically to the ANSI/VITA 4-1995 IO Module Interface specification. Designed for a typical IP Module carrier that holds four IP Modules, the DAC128F5 can provide up to 32 channels of DACs for a single slot on a computer bus backplane, or can be mixed with other IP Modules for a more customized, modular I/O system solution.

The DAC128F5 maintains the highest possible accuracy and minimizes the cumulative error because the board's design uses the best (yet, reasonably affordable) parts for the tasks to be accomplished.

1.4 Features

- Eight integrated channels of 12-bit resolution, laser-trimmed R-2R SAR-based DACs providing ±5 V outputs with no-wait write and read-back accesses.
- Automatic power-up of all eight channels to code '000' ⇒ -5.000 V outputs.
- Completely monolithic analog section, including an imbedded precision voltage reference, for good channel-to-channel tracking over temperature.
- The fully monotonic -5.000 V to +4.9976 V short-protected (25 mA typical, 50 mA maximum, per channel) outputs can supply ±2 mA (minimum) to a load up to a maximum capacitance of 500 ρF, with an adjacent-channel crosstalk of -90 dB (typical), and digital transient crosstalk of 60 dB.
- The total overall gain error, including the internal reference of +5.000±0.004 V, is typically +4 → -7 LSB, with a noise level of 150±15 µV RMS from 0.1 Hz to 2 MHz bandwidth.
- For a 5 KΩ and 500 ρF load, the settling time to ±½ LSB for a full-scale jump in either direction is 7±2 µs, with a typical slew rate of 3.0±0.3 V/µs.
- Digital coding is offset binary, where FFF *hex* → +4.9976 V output, 800 *hex* → 0.0000 V output, and 000 ⇒ -5.000 V output.

1.5 Specifications

MECHANICAL: Singlewide IP Module

- Measurements: 1.800 x 3.900 x 0.303 inches (connectors, above board)
  4.572 x 9.906 x 0.770 cm (connectors, above board)
  NOTE: 0.175 inches or 0.444 cm maximum components above board
- Weight: 0.992 oz. or 28.12 grams
- Board thickness: 0.062 inches or 0.157 cm, nominally, (4 layers)

ELECTRICAL: Singlewide IP Module Transfers

- 8 MHz clock rate
- No wait cycles on any transfer types
- Hold cycles supported on all valid transfer types
- Complete (no partial) address decoding
- I/O transfers: 16-bit writes, 16-bit reads
  - Eight, 16-bit I/O locations for 8 ports
  - Maximum read/write rate: 4 MTransfers/second, sustained
  - Upper nibble floats (Reads as 'Fxxx')
- ID transfers: 8-bit reads (only)
  - Zero-fill on upper byte
  - Twelve bytes, including Cyclic Redundancy Check (CRC)
  - SYSTRAN's manufacturer's ID = **45** *hex*, **E** *ASCII*
  - DAC128F5's model number = **65** *hex*, **e** *ASCII*
  - Cyclic Redundancy Check value = **83** *hex*
  - Maximum read rate: 4 MTransfers/second, sustained
- Memory transfers: Not supported
- Interrupt vector transfers: Not supported
- Interrupt requests: None generated
- DMA activity: None supported

- No acknowledgement on unsupported transfer attempts:
  - Memory read and write
  - Interrupt read
  - ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

- All data registers power up to '000' ⇒ -5.000 V on outputs
- No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS

- Power: +5 Vdc @ 24 mA (typical, no loads on outputs)
  +12 Vdc @ 17 mA (typical, no loads on outputs)
  -12 Vdc @ 15 mA (typical, no loads on outputs)

PERFORMANCE CHARACTERISTICS

- Electrical characteristics: Refer to Section 5.0: PERFORMANCE

ABSOLUTE MAXIMUM RATINGS

- Supply voltage with respect to ground:
  - -0.3 V (minimum), +7.0 V (maximum) for digital
  - ±13.2 V (maximum) for analog

RECOMMENDED OPERATING CONDITIONS

- Supply voltage: +4.75 V → +5.25 V for digital
  ±11.4 V → ±12.6 V for analog
- Logic Interface: IP Module specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS

- Temperature (Operating): 0°C → +70°C
- Temperature (No bias, storage): -40°C → +90°C
- Humidity (Non-condensing): 5% → 95%
- Vibration (Operating): 10 G's RMS (10 → 55 Hz)
- Shock (Operating): 50 G's (maximum, any axis)
- Altitude (Operating): 10,000 feet, maximum

MEAN TIME BETWEEN FAILURE (MTBF):

- 1,302,423 hours per MIL-HDBK-217F

1.6 Related Product

- Software: 'C' library and OS-9 device-driver routines with documentation.

1.7 Related Publications

- SYSTRAN I/O Solutions Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Module Bus Using the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001).
- American National Standard for IP Modules (ANSI/VITA 4 - 1995) published by the VMEbus International Trade Association 7825 Gelding Dr., Suite 104, Scottsdale, AZ 85260

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SYSTRAN Corporate policy is to provide the highest quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

SYSTRAN has developed a Quality System which conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard is the most comprehensive of the conformance standards, in that it addresses all 20 clauses of the ISO quality system requirements.

SYSTRAN's Quality System addresses the following basic quality objectives:

- Achieve, maintain and continually improve the quality of SYSTRAN products
- Improve the quality of its own operations to meet the needs of SYSTRAN customers and stakeholders
- Provide confidence internally that quality is being fulfilled, maintained and improved
- Provide confidence to the customer and other stakeholders that requirements for quality will be achieved in the delivered product.

SYSTRAN's Quality System was assessed by BSI QA, which is the certification division of British Standards Institution, the largest and most respected standardization authority in the world. SYSTRAN's Quality System was found to meet or exceed the international standards in all areas, and Certificate of Registration number FM 31468 was issued to SYSTRAN on May 16, 1995.

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- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

1.9 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct questions not satisfactorily answered by this document, or concerns about the functional-fit of this product for your particular application, or programming questions, to the factory at **(937) 252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance. Our goal is to help solve your problem.

1.10 Ordering Process

To learn more about SYSTRAN products or to place an order, the following contacts are available:

- Phone: **(937) 252-5601**
- E-mail address: **info@systran.com**
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2. 0 DESCRIPTION

NOTE: The IP Module signal references, transfer and cycle types discussed in this document are explained in detail in the ANSI/VITA 4-1995 IP Module specification.

2.1 Block Diagram Description

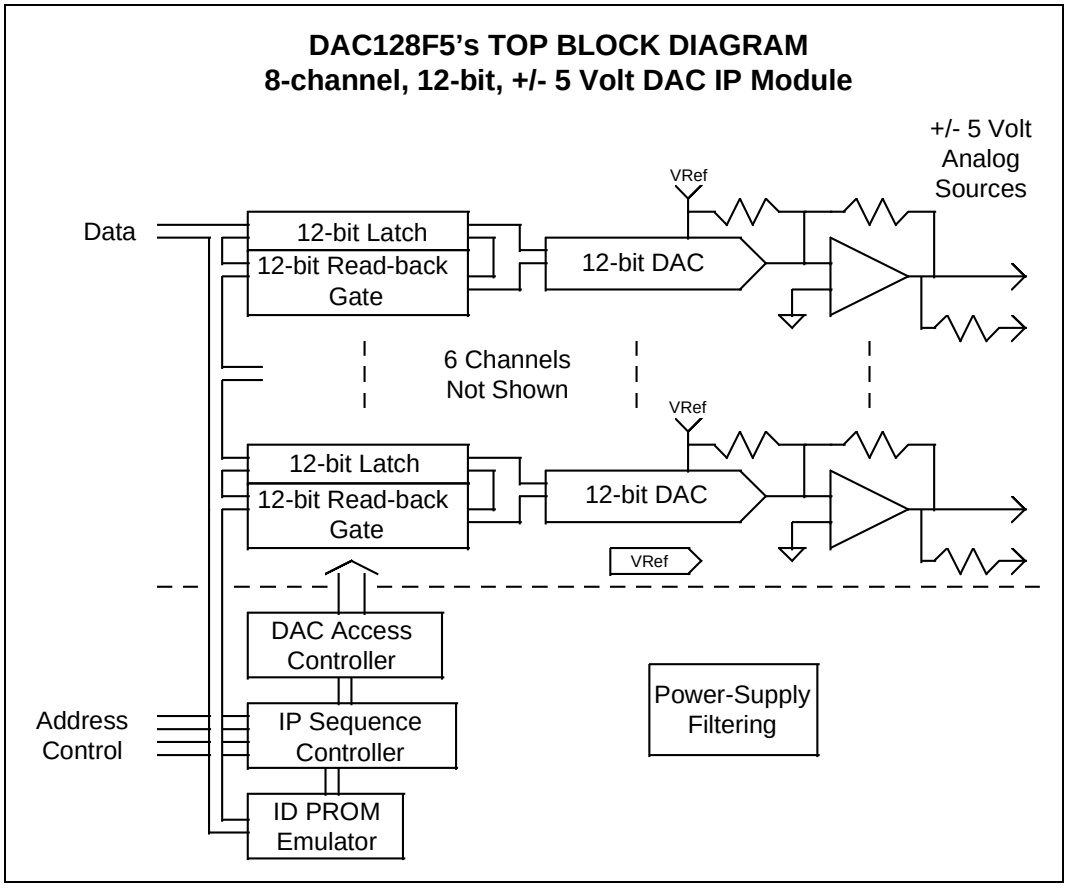


Figure 2-1 DAC128F5 Block Diagram

Figure 2-1 presents a block diagram of the DAC128F5. On the left side is the IP Module's logic interface, consisting of the IPDbus (labeled "DATA"), the IPAbus (labeled "ADDRESS"), and the transfer control signals (labeled "CONTROL").

On the right side are the IP Module's I/O connections, consisting of eight direct DAC connections, eight series-terminated DAC connections, and thirty-four ground connections (not shown).

The circuitry presented above the horizontal dashed line, except for the series-termination resistors, is all contained within a single integrated circuit, the AD75089JP. As depicted, the majority of the digital and all of the analog circuitry for this IP Module is completely self-contained, including the DAC's precision voltage reference source.

The three blocks in the lower left-hand quadrant are contained within the small EPLD device that controls this board. The "Power Supply Filtering" consists of both decoupling and ripple filters for digital and analog circuits on this IP Module.

The DAC128F5 has the following features:

- An intuitive I/O register map
- No switches or options
- Power from just the carrier of choice
- No software control driver requirements

These features reflect the simplicity and elegance of this IP Module.

2.2 Theory of Operation



NOTE: Refer to the DAC128F5 schematics located in Appendix A while reading this material since individual components are referred to by function name, schematic reference designator, or industry-standard device part number.

The DAC128F5 was developed using VHDL and synthesis, targeted to an Altera EPLD, schematic captured and integrated to standard integrated circuits, connectors, and discrete components using Viewlogic's ViewDraw and associated packages. This top-down design approach is evident in the schematics in Appendix A.

2.3 Schematics

The following is a short travel-map through the schematics of the DAC128F5 which emphasizes the top-down design methodology used. Two pages comprise the schematic set in Appendix A.

SCHEMATIC #1

The first page of the schematic, labeled Schematic #1, is the top-level drawing. This drawing is composed of the following:

- IP Module Logic and the user's I/O connectors
- The access controller EPLD (labeled S_DA128)
- An AD75089JP digital-to-analog converter IC
- One 74FCT541 buffer to drive all zeros on the upper byte-lane of the IPD bus during ID read cycles
- Three analog filters for each power supply voltage
- Various decoupling capacitors
- A symbol for the circuit board itself.

If you were to "push-down" into the controller block "S_DA128" on the first sheet, you would arrive at schematic #2 in Appendix A.

SCHEMATIC #2

Schematic #2 in Appendix A is the netlisted Altera EPM7032QC44 EPLD that controls the operations of the IP Module, including the emulation of the ID PROM.

As indicated above, the core of this IP Module is contained within a single integrated circuit, the AD75089JP. It is the largest IC on this IP Module, designated as U3 on the schematics and on the assembly drawing in Figure 2-2. This IC contains eight complete 12-bit, ±5 V output digital-to-analog converters.

Each DAC is based upon laser-trimmed thin-film resistor R-2R SAR-based current DAC architecture, with inverting-buffer output stages, all referenced to the IP Module's ground plane connections at the I/O connector. The internal reference is buffered so that it can serve all eight DACs. The completely monolithic nature of the entire analog section provides excellent temperature tracking and overall accuracy for the entire operational temperature range of this IP Module.

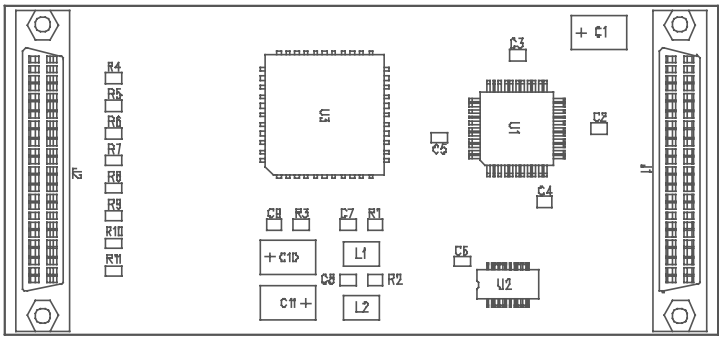


Figure 2-2 DAC128F5 Physical Assembly

2.4 Specifications

The following information is provided as a system design guide to assist in determining expected performance results for typical applications that use the DAC128F5 IP Module. This information is a combination, with exceptions, of the published specification for the AD75089 device by the manufacturer, and of test results from up to 100 samples of the DAC device used for qualifying the part for manufacture and for verifying the published specifications. We have found that most of the devices operate better than advertised by the manufacturer.

2.4.1 Analog Output

For a full scale value of 10 volts ÷ 2^{12} steps → 2.4414 mV/bit. The analog output, therefore, ranges: -5.0000 V → +4.9976 V, with code inputs ranging: 000 *hex* ⇒ FFF *hex*, with 0.0000 V output occurring with a code input of 800 *hex.*

Of significant interest to the user is the current drive capability of the DACs' output buffers. The published specifications indicate that each channel can source and sink up to 2 mA (minimum), with up to 500 ρF load capacitance with no effect on stability.

The capacitance issue will be explored first. For a typical, 0.050″ on-centers Insulation Displacement (flat ribbon) Cable, the typical unbalanced capacitance is 14.1 ρF/foot, which yields a maximum cable length of 35′ before the DAC's output amplifier could become unstable. Since many applications require the ability to link the DAC to its destination at distances greater than 35′, the DAC128F5 series-terminated outputs should be used instead of the direct outputs. The series resistance is 18 Ω , which is much lower than the characteristic impedance of the typical ribbon cable (≈105 Ω). This resistance was deliberately selected low to minimize accuracy errors for heavy DAC loads. For a maximum current of 2 mA, 36 mV will be dropped across the series-termination resistor. Therefore, for applications using long distance cabling, reduce the load current as much as possible and use the series-terminated DAC outputs for stable operations. These series resistors are designated as R4→ R11 in the schematics, and are just to the right of J2 connector in Figure 2-2.

The minimum output current of 2 mA is a very conservative specification. The typical per-channel short-circuit current is 25 mA, with 50 mA being the specified maximum short-circuit current. From the manufacturer's testing of its 100 qualification samples, the minimum short-circuit current was 21.87 mA, and the maximum was 47.26 mA. Additionally, a tabulation of measured maximum currents with the effects of attempting to exceed these limits is presented in this document in Section 5.0 PERFORMANCE.

2.4.2 Voltage Reference

The integrated voltage reference was used, instead of an external source, so that the maximum accuracy possible could be attained due to the tight thermal tracking inherent in a fully monolithic component. The published specifications for the reference provide for a voltage of +4.95 V (minimum) ⇒ +5.05 V (maximum). This equates to a reference error band of ±20 bits. From the manufacturer's testing of its 100 qualification samples, the minimum reference voltage was +4.9962 V, the maximum reference voltage was +5.0038 V, and the average reference voltage was +4.9998 V, with a standard deviation of 2 mV. This data indicates that the reference error is actually ≈ ±2 bits, which is significantly better than specified.

The specification indicates that the reference's temperature coefficient is ±15 ppm/°C, or ±75 µV/°C. For the specified temperature range of 0°C through 70°C, this equates to a worst case error of 5.25 mV, or ±2 bits error. As in most cases, the specification is extremely conservative compared to actual performance data. From the manufacturer's testing of 27 qualification samples, the minimum temperature coefficient was 1.26 ppm/°C, the maximum was 13.73 ppm/°C, and the average was 7.08 ppm/°C, with a standard deviation of 3.02. The average equates to ≈1 bit variation over temperature.

2.4.3 DC Accuracy

There are many different facets of accuracy to be explored. The first, and most important, is the fact that the DACs are all guaranteed to be monotonic over the full operating temperature. This means that the output either increases or remains constant for increasing input codes such that the output will always be a non-decreasing function of input.

Integral linearity error is the maximum deviation of the actual DAC output, for any input code, from the ideal analog output as defined by a straight line from + 4.9976 V → -5.000 V. This is specified as being ±1 LSB (typical, over temperature). From the manufacturer's testing of its 100 qualification samples, the minimum deviation was

-0.881 LSB, the maximum was 1.369 LSB, and the average was 0.501 LSB, with a standard deviation of 0.420. The qualification table recommendation for the specification of ±1½ LSB (min/max) error over temperature was not transmitted to the specification sheet.

Differential linearity error is the analog voltage error for 1 LSB input code change normalized to the full scale. An example of this will complete the explanation. If the differential linearity error is 0.128 LSB, this equates to an error of 2.4414 mV × 0.128 = 312.5 µV. If the input code changes by one bit, and the output changes by 2.129 mV (2.4414 mV - 312.5 µV), then a differential linearity error of 0.128 LSB has occurred. The specified differential linearity error is ±½ LSB (typical, over temperature). From the manufacturer's testing of its 100 qualification samples, the minimum deviation was 0.016 LSB, the maximum was 0.342 LSB, and the average was 0.128 LSB (as used in our example, above), with a standard deviation of 0.054 LSB. The qualification table recommendation for the specification of ±¾ LSB (min/max) error-over-temperature was not transmitted to the specification sheet.

Gain error, including the internal reference, is the error in the slope of the transfer characteristic, often referred to a scale-factor error. In other words, it is the difference between the output span of an ideal DAC and the actual DAC. As an example, if the ideal positive full-scale output is supposed to be +4.9976 V, but it actually measures +4.9927 V, then the gain error of 4.8828 mV yields a specification of -2 LSB. The paragraph on VOLTAGE REFERENCE covered some of the errors involved with the internal reference, which contributes directly to the overall gain error for this product. The specified gain error is ±8 LSB, with a minimum value of -15 LSB, and a maximum value of +15 LSB, giving a worst case specified gain error of ±36.6 mV over the full operating temperature range. From the manufacturer's testing of its 100 qualification samples, the minimum gain error was -6.670 LSB, the maximum was +3.200 LSB, and the average was -2.381 LSB, with a standard deviation of 1.710 LSB. This equates to a typical gain error of -5.813 mV for the 10 V full-scale range of this device.

The last significant accuracy parameter to consider is that of mid-scale error, which is quantified in the qualification information, but is not identified in the specification by definition or by parameter. Typical errors in this related category are identified as "offset error" and "zero error". Offset error is equally applicable to all input codes, where the error is a linear shift from the ideal. Zero error is a function of both offset error and gain error and is defined as the error in analog value when the input code calls for analog zero. The qualified information on mid-scale error appears to be the equivalence of the offset error. From the manufacturer's testing of its 100 qualification samples, the minimum mid-scale error is -1.672 LSB, the maximum is +2.902 LSB, and the average is +0.980 LSB, with a standard deviation of 0.842 LSB. The average mid-scale error, therefore, is ≈+2.393 mV over temperature.

Figure 2-3 is a simple diagram depicting the differences between gain error, offset error, and zero error, compared against the ideal. This figure does not present linearity or differential nonlinearity error examples.

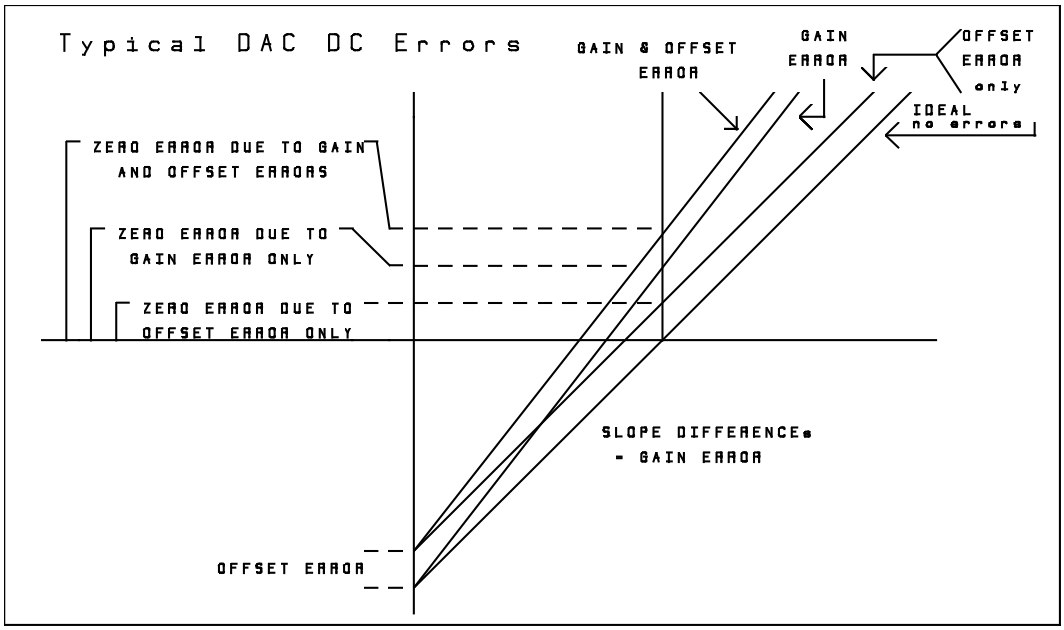


Figure 2-3 DAC DC Errors

2.4.4 Matching Performance

To identify how well all of the DACs within a single device track together, two parameters are used:

- Gain matching
- Offset matching

These parameters are primarily a function of the manufacturing process and the materials used.

Gain matching is defined as the largest difference in gain error between any two DACs in a single packaged device. The published specifications for this parameter are ±2.5 LSB (typical), and ±5 LSB (min/max). From the manufacturer's testing of its 100 qualification samples, the minimum gain error matching value was 0.91 LSB, the maximum was 4.97 LSB, and the average was 3.04 LSB, with a standard deviation of 1.044 LSB. This equates to a typical worst-case gain-matching error of 7.424 mV.

Offset matching is defined as the largest difference in offset values between any two DACs in a single packaged device. The published specifications for this parameter are ±2 LSB (typical), and ±4 LSB (min/max). From the manufacturer's testing of its 100 qualification samples, the minimum (mid-scale) offset-error matching value was 0.70 LSB, the maximum was 3.31 LSB, and the average was 1.65 LSB, with a standard deviation of 0.448 LSB. This equates to a typical worst-case offset- or, mid-scale-matching error of 4.031 mV.

2.4.5 Dynamic Performance

To define how well a DAC responds with an analog-output change as a result of an input-code change, two parameters are used:

- Settling time
- Slew rate

Both of these parameters define what the maximum update rate can be since the analog response to changes is much slower than the IP Module interface circuitry. As an example, if the DAC takes 5 µs to go from its minimum full-scale value to its maximum full-scale value while the input code can be changed once every 250 ns, then the actual update rate is once every 5 µs for the DAC interface.

Settling time is the most important parameter to be considered. The settling time of a DAC is defined as the time taken for the output to move to, and to remain within, a specified error band after the digital input has changed. Settling time includes a worst-case allowance for different transitioning rates depending on the direction of the change (does it slew up faster than it slews down?). The settling time also includes other sub-parameters that are normally lumped into the settling time parameter, like dead time, slew time, recovery time, and sometimes linear-settling time. For a load of 5 KΩ in parallel with 500 ρF, the published specification for the settling time for a full-scale jump in either direction to ±½ LSB is 8 µs (typical). From the manufacturer's testing of 20 qualification samples, the minimum settling time was 4.57 µs, the maximum was 8.97 µs, and the average was 7.15 µs, with a standard deviation of 1.230 µs. The SYSTRAN published specification of 7±2 µs was derived from this data. Actual slew time measurements, presented in section 5.5, show actual times between 2.3 and 2.7 µs.

Slew rate is a subset of settling time. Defined as the rate of change in analog output in terms of volts per unit time, slew rate is the point on the "curve" that has the steepest slope. Slew rate occurs between the dead time (the delay from the rising edge of ICLK during an I/O transfer's termination cycle until the first changes in the analog signal), and the ringing section consisting of the recovery and linear-settling times. For a load of 5 KΩ in parallel with 500 ρF, the published slew rate is 3 V/µS (typical). From the manufacturer's testing of 24 qualification samples, the minimum slew rate was 2.93 V/µs, the maximum was 3.28 V/µs, and the average was 3.09 V/µs, with a standard deviation of 0.080 V/µs. The SYSTRAN published specification of 3±0.3 V/µs was derived from this data.

If the typical values are used for slew rate and settling time, then 10 V÷3 V/µs yields a slew time of 3.333 µs, which means that 3.666 µs is spent in the other settling-time regions of dead time, recovery time, and linear-settling time.

2.5 IP Module Interface

All IP Module Logic Bus transfers take place across J1 (the IP Module Logic Connector) which is located on the left side of the first sheet of the schematics, implicitly on the block diagram presented in Figure 2-1, and on the right side of Figure 2-2. See Appendix A for details about the signals on this connector.

Generally speaking, this IP Module does not support DMA or interrupts, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and writes to a short, 8-location, I/O map.

The DAC128F5's primary activity controller is contained within the EPM7032LC44-10 EPLD located at U1 (just to the left of J1 in Figure 2-2, and to the right of J1 on page B-1 of the schematics). This controller serves as the IP Module transfer engine, with responsibilities that include the following:

- Detection of valid I/O and ID transfer operations within their respective, fully-decoded address ranges, including the support of HOLD cycles when generated by a carrier.
- Generation of ID PROM emulation data pattern for ID read transfers.
- Generation of DAC chip select, reset, and read/write control signal for I/O reads and (16-bit only) writes.
- Enabling of the upper byte zero-fill logic during ID read transfers.

The last integrated circuit on this IP Module is a simple tristateable gate that grounds the upper byte-lane of the IPDbus during ID read transfers, as controlled by U1 (see above). This gate is located at U2 in the schematics, and below U1 to the left of J1 on Figure 2-2.

The remaining discrete components are the power supply filter and decoupling capacitors.

See Section 5.0 PERFORMANCE for timing information that depicts the performance characteristics of the IP Module interface.

2.6 The Ground

As with most DAC-based I/O interfaces, especially those attempting to maintain higher accuracy (10 bits and higher), it is imperative that good grounding practices be implemented. ALL of the 34 ground lines on the I/O connector (J2) should be tied to the analog ground point of the system. These 34 connections are directly tied to the multiple ground planes of this IP Module, which is not isolated from the carrier's ground reference at the logic connector.

2.7 Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol. Do NOT use gasoline or thinner solvents on this product.

3. 0 INSTALLATION

3.1 Unpack the DAC128F5

The contents of the DAC128F5 shipping packages are listed in Table 3-1.

Table 3-1 Contents of DAC128F5 Shipping Packages

Qty	Description
1	DAC128F5 Printed Circuit Assembly
1	DAC128F5 User Manual *

* One manual is shipped with each board ordered unless additional manuals are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR-DAC128F5).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Inspect the DAC128F5

Examine the DAC128F5 to determine if any damage occurred during shipping.

3.3 Install the DAC128F5



NOTE: The DAC128F5 is an Electrostatic Sensitive Device (ESD). Install the DAC128F5 hardware using a good anti-static workbench to protect the IP Module and carrier boards. The IP Module carrier board must be removed from the host system using good ESD practices and moved to an ESD-controlled area where the DAC128F5 can be installed.

The tools required for the DAC128F5 installation are listed in Table 3-2.

Table 3-2 DAC128F5 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat-Head Screwdriver (Optional)

Figures 3-1 and 3-2 show the DAC128F5 installed on a VME IP Module carrier and on an ISA carrier, respectively.

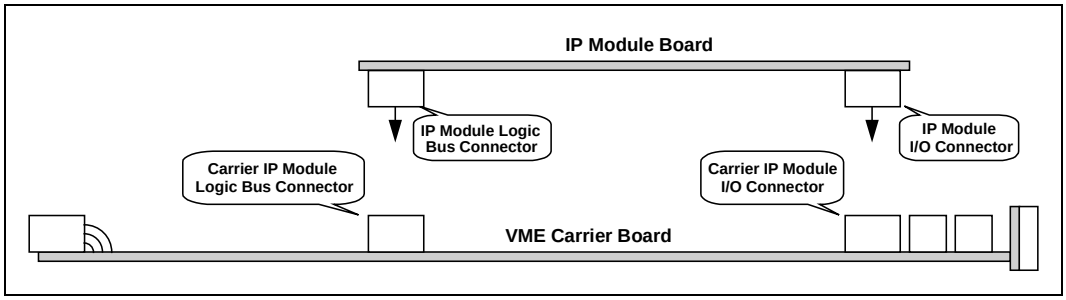


Figure 3-1 DAC128F5 Installed on a VME IP Module Carrier

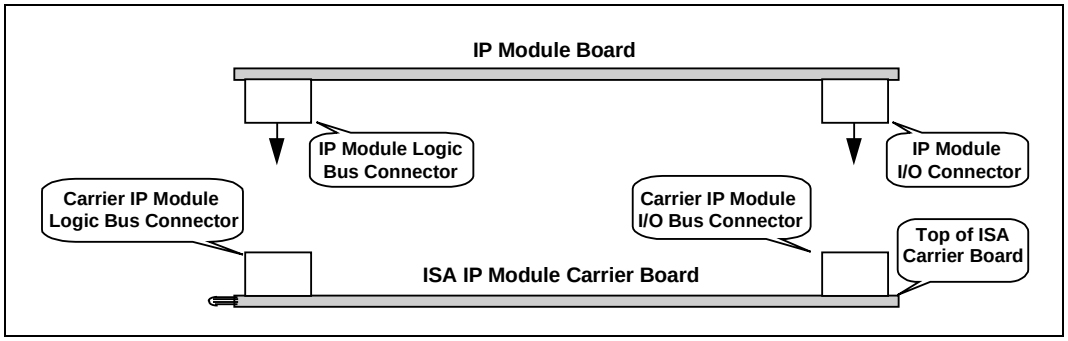


Figure 3-2 DAC128F5 Installed on an ISA IP Module Carrier

The pin assignments for the IP Module Logic Bus connector are shown in Table 3-3. The signals in the left column are the original IP Module signal nomenclature, and the signals in the right column are those used by SYSTRAN Corp.

Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module carrier board *User Manual* for more information.

Referring to the appropriate figures and table described above, perform the following steps to install the DAC128F5. The asterisk (*) denotes optional items.

1. Turn OFF all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD-controlled area where the DAC128F5 can be installed.
3. Remove the DAC128F5 from the shipping package and place it on the ESD bench.
4. Install the DAC128F5 onto the carrier board by applying adequate and equal pressure to the DAC128F5 board at both ends.

*5. Install four M2x5mm flat-head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the DAC128F5 to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signal Names	IP Module Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
Intreq1*	44	N_INTREQ1
A4	43	IPA4
Intreq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Names
50	GND
49	GND
48	GND
47	GND
46	GND
45	GND
44	GND
43	GND
42	GND
41	GND
40	GND
39	GND
38	GND
37	GND
36	GND
35	GND
34	GND
33	GND
32	GND
31	GND
30	GND
29	GND
28	GND
27	GND
26	GND
25	2DAC08R
24	DAC08
23	GND
22	2DAC07R
21	DAC07
20	GND
19	2DAC06R
18	DAC06
17	GND
16	2DAC05R
15	DAC05
14	GND
13	2DAC04R
12	DAC04
11	GND
10	2DAC03R
9	DAC03
8	GND
7	2DAC02R
6	DAC02
5	GND
4	2DAC01R
3	DAC01
2	GND
1	GND

4. 0 PROGRAMMING GUIDE

4.1 Overview

This section of the manual describes the operation of the DAC128F5 from the software perspective, detailing the DAC128F5 registers and providing programming examples. A more detailed description of the hardware can be found in Sections 2.0 DESCRIPTION and 6.0 TYPICAL APPLICATIONS.

4.2 Description

The DAC128F5 is an 8-channel digital-to-analog card. The DAC128F5 has eight 16-bit-wide registers, each corresponding to a DAC channel. The DAC128F5 supports word (16-bit) reads and writes. On power-up, all data registers are set to '000' *hex* (all channels at their minimum range of -5.0 volts). The data registers are viewed as eight 16-bit registers with the twelve bits of each DAC corresponding to the IPD[11:0] bits (with the IPD[15:12] not driven and 'float' to all ones). During ID reads, the upper byte of the IPDbus (bits [15:8]) is driven as zeros.

4.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by this function. This emulation saves space, lowers costs, improves reliability, and enables this IP Module to provide "no-wait" read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0C **hex**, or any attempt to write to ID space results in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeros during valid ID read-only accesses.

Table 4-1 is the DAC128F5 emulated ID Address Space PROM listing.

Table 4-1 DAC128F5 ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 00 *hex*	ASCII 'I'	49 *hex*
IPA = 01 *hex*	ASCII 'P'	50 *hex*
IPA = 02 *hex*	ASCII 'A'	41 *hex*
IPA = 03 *hex*	ASCII 'C'	43 *hex*
IPA = 04 *hex*	SYSTRAN's ID	45 *hex*
IPA = 05 *hex*	DAC128F5 Model Number	65 *hex*
IPA = 06 *hex*	Revision Level	30 *hex*
IPA = 07 *hex*	Reserved	00 *hex*
IPA = 08 *hex*	Low Byte Driver ID	00 *hex*
IPA = 09 *hex*	High Byte Driver ID	00 *hex*
IPA = 0A *hex*	Number of Bytes Used	0C *hex*
IPA = 0B *hex*	CRC	83 *hex*

4.4 IP Module I/O Address Map

The DAC128F5's I/O Address Map was designed with efficiently located data registers in the IP Module I/O space (IPA = 00 ⇒ 07 *hex*).



NOTE: The address detector circuitry is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 08 *hex* will result in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The first location (IPA = 00 *hex*) is the write-and-read-back Data Register 0 for the DAC output channel #1. Valid accesses to and from this location include: 16-bit writes, and 16-bit reads. All of the subsequent locations (IPA = 01 ⇒ 07 *hex*) correspond to the DAC channels #2 through #8, respectively (i.e. IPA = 01 for channel #2 through IPA = 07 for channel #8).

Table 4-2 is the DAC128F5 I/O Address Map and contains the data register.

Table 4-2 DAC128F5 I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 00 *hex*	[XXXX] [11:8]	[7:0]	Data Register 0, Channel 1, 12 bits
IPA = 01 *hex*	[XXXX] [11:8]	[7:0]	Data Register 1, Channel 2, 12 bits
IPA = 02 *hex*	[XXXX] [11:8]	[7:0]	Data Register 2, Channel 3, 12 bits
IPA = 03 *hex*	[XXXX] [11:8]	[7:0]	Data Register 3, Channel 4, 12 bits
IPA = 04 *hex*	[XXXX] [11:8]	[7:0]	Data Register 4, Channel 5, 12 bits
IPA = 05 *hex*	[XXXX] [11:8]	[7:0]	Data Register 5, Channel 6, 12 bits
IPA = 06 *hex*	[XXXX] [11:8]	[7:0]	Data Register 6, Channel 7, 12 bits
IPA = 07 *hex*	[XXXX] [11:8]	[7:0]	Data Register 7, Channel 8, 12 bits

NOTE: [X] means not used and is read as one.

4.5 Word Access Address Translation

Table 4-3 shows the relationship between VME, ISA, and NuBus local bus addresses, and the IP Module address for word accesses.

In the table, the word BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-3 Word Access Address Translation Table

VMEbus Address	ISA Bus Address	NuBus Address	IP Module Address
BASE + 0	BASE + 0	BASE + 2	IPA = 00 *hex*
BASE + 2	BASE + 2	BASE + 6	IPA = 01 *hex*
BASE + 4	BASE + 4	BASE + A	IPA = 02 *hex*
BASE + 6	BASE + 6	BASE + E	IPA = 03 *hex*
BASE + 8	BASE + 8	BASE + 12	IPA = 04 *hex*
BASE + A	BASE + A	BASE + 16	IPA = 05 *hex*
BASE + C	BASE + C	BASE + 1A	IPA = 06 *hex*
BASE + E	BASE + E	BASE + 1E	IPA = 07 *hex*
BASE + 10	BASE + 10	BASE + 22	IPA = 08 *hex*
BASE + 12	BASE + 12	BASE + 26	IPA = 09 *hex*
BASE + 14	BASE + 14	BASE + 2A	IPA = 0A *hex*
BASE + 16	BASE + 16	BASE + 2E	IPA = 0B *hex*

4.6 Byte Access Address Translation

Table 4-4 shows the relationship between VME, ISA, and NuBus local bus addresses, and the IP Module address for byte accesses.

In the table, the word BASE represents the ID* base address. For the DAC128F5, byte accesses are valid only for ID accesses. All addresses are in hexadecimal.

Table 4-4 Byte Access Address Translation Table

VMEbus Address	ISA Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 1	BASE + 0	BASE + 3	IPA = 00 *hex*	0
BASE + 0	BASE + 1	BASE + 2	IPA = 00 *hex*	1
BASE + 3	BASE + 2	BASE + 7	IPA = 01 *hex*	0
BASE + 2	BASE + 3	BASE + 6	IPA = 01 *hex*	1
BASE + 5	BASE + 4	BASE + B	IPA = 02 *hex*	0
BASE + 4	BASE + 5	BASE + A	IPA = 02 *hex*	1
BASE + 7	BASE + 6	BASE + F	IPA = 03 *hex*	0
BASE + 6	BASE + 7	BASE + E	IPA = 03 *hex*	1
BASE + 9	BASE + 8	BASE + 13	IPA = 04 *hex*	0
BASE + 8	BASE + 9	BASE + 12	IPA = 04 *hex*	1
BASE + B	BASE + A	BASE + 17	IPA = 05 *hex*	0
BASE + A	BASE + B	BASE + 16	IPA = 05 *hex*	1
BASE + D	BASE + C	BASE + 1B	IPA = 06 *hex*	0
BASE + C	BASE + D	BASE + 1A	IPA = 06 *hex*	1
BASE + F	BASE + E	BASE + 1F	IPA = 07 *hex*	0
BASE + E	BASE + F	BASE + 1E	IPA = 07 *hex*	1
BASE + 11	BASE + 10	BASE + 23	IPA = 08 *hex*	0
BASE + 10	BASE + 11	BASE + 22	IPA = 08 *hex*	1
BASE + 13	BASE + 12	BASE + 27	IPA = 09 *hex*	0
BASE + 12	BASE + 13	BASE + 26	IPA = 09 *hex*	1
BASE + 15	BASE + 14	BASE + 2B	IPA = 0A *hex*	0
BASE + 14	BASE + 15	BASE + 2A	IPA = 0A *hex*	1
BASE + 17	BASE + 16	BASE + 2F	IPA = 0B *hex*	0
BASE + 16	BASE + 17	BASE + 2E	IPA = 0B *hex*	1

* Byte-lane 1 not applicable for ID Space

4.7 Data Registers 0 to 7 Bit Description (IPA = 00 ⇒ 07 *hex*)

The DAC128F5 has eight 16-bit-wide registers, each corresponding to a DAC channel, and supports word (16-bit) reads and writes. During writes, the upper 4 bits are discarded and are read back as ones. The eight 16-bit read/write data registers set the output voltage of the eight DAC channels. Data register 0 corresponds to DAC channel 1, register 1 to channel 2, ... , register 7 to channel 8. On power-up, all data registers are set to '000' *hex.*

Table 4-5 Data Registers 0 to 7 Bit Descriptions

Bit #	15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	Not Used	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R/W	Read as 1's Writes discarded	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-up State	N/A	0	0	0	0	0	0	0	0	0	0	0	0

D11 - D0 : These bits make up the 12-bit DAC value.

4.8 Programming Example

The following example illustrates how to program the DAC128F5 device. The power-up state sets all of the channels to their minimum range. This example only interacts with channel 1; however, all the channels operate the same way.

- At power-up, all the data registers values are cleared, corresponding to -5.0 volts.
- Write '0FFF' *hex* to data register 0.
- The DAC channel 1 voltage output should now be +4.9976 volts.
- Write '0800' *hex* to data register 0.
- The DAC channel 1 voltage output should now be 0.0 volts.
- Write '0000' *hex* to data register 0 (DAC channel 1's data register).
- The DAC channel 1 voltage output should now be -5.0 volts.

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5. 0 PERFORMANCE

5.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in section 1.0: INTRODUCTION. Where possible, data is tabulated with only one response time (actual) performance figure presented in order to minimize the length of the presentation.

5.2 Timing Measurements

Timing measurements were conducted on the DAC128F5 using an HP model 16500A Logic Analyzer with a 400 megasamples per second Digitizing Oscilloscope Module, model 16531A, plugged into slot E, and a 1 GHz Timing Master Module, model 16515A in slot C. The DAC128F5 was installed in the IPack slot 'A' of a Motorola MVME-162-01 VME processor IPack carrier board. Figure 5-1 shows the test configuration for the oscilloscope and state timing measurements.

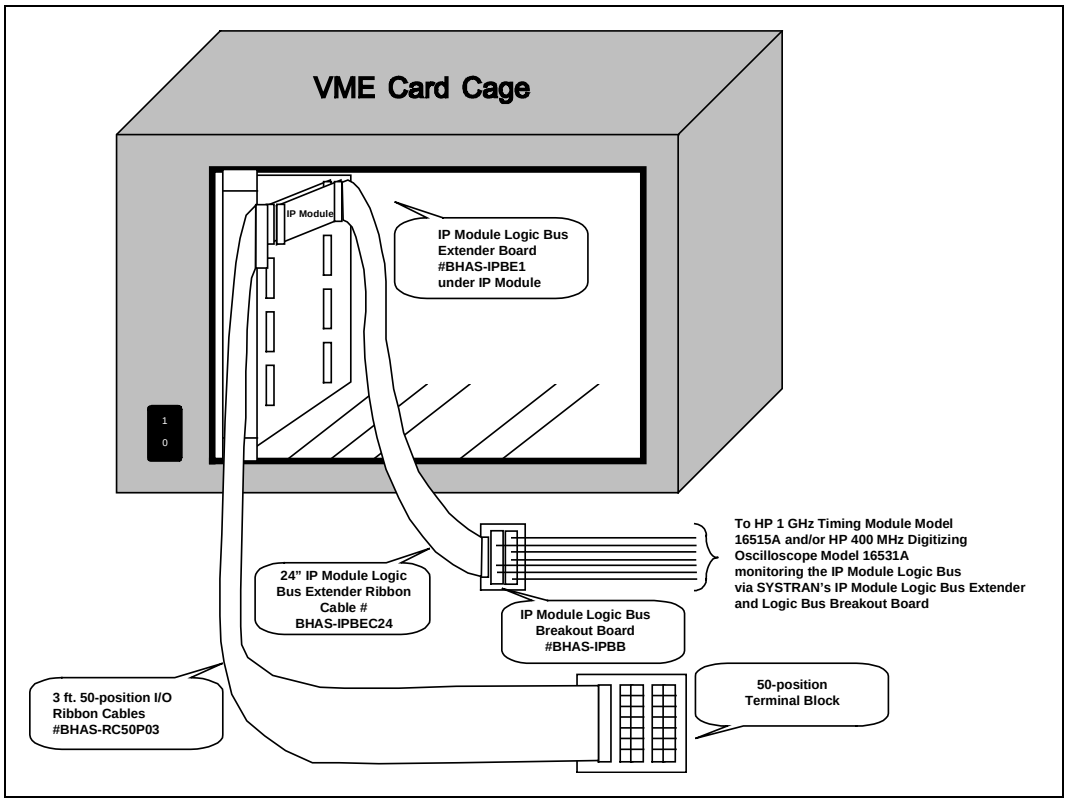


Figure 5-1 Setup for Oscilloscope and State Timing

5.3 IP Module Accesses

There are some parameters that are important when evaluating an IP Module's performance on a specific carrier board. These involve the assertion and negation (or driving to logic state versus high-impedance states) of signals from the IP Module to the carrier, with reference to the rising edge of ICLK. According to specification, these state changes must occur within 40 ns.

Figure 5-2 presents just one of the logic state analysis figures captured for the development of the data in Table 5-1. This depicts an I/O write to the last I/O location (IPA = 07 *hex*) of data whose least significant byte is zero (IPD[7:0] = 0). The important parameter here is that it typically takes 10 ns to negate N_ACK.

Table 5-1 IP Module Typical Access Time

Function/Operation	ICLK Until	Time
I/O READ @ IPA = 00	↓ N_ACK	10 ns
I/O READ @ IPA = 00	↑ N_ACK	11 ns
I/O READ @ IPA = 07	↓ N_ACK	09 ns
I/O READ @ IPA = 07	↑ N_ACK	10 ns
I/O READ @ IPA = 00	IPDbus' HIGH to LOW impedance	06 ns
I/O READ @ IPA = 00	↓ N_ACK	10 ns
I/O READ @ IPA = 00	↑ N_ACK	11 ns

Note that Table 5-1 lacks the usual entry of an I/O READ access typical time to drive the IPDbus to a low-impedance state during the termination cycle (N_ACK asserts low). Unlike nearly all other SYSTRAN IP Modules, the DAC128F5 starts the process of driving the IPDbus during the select cycle (compliant with the specification) instead of waiting for the start of the termination cycle.

The data sheet for the AD75089JP (DAC I.C.) indicates that it takes 150 ns for the data to become valid during a READ access, and 40 ns for the device to release the IPDbus (go to a high-impedance state). The IPDbus is driven during the select cycle to ensure that the data is stable long before the rising edge of ICLK at the end of the termination cycle when the carrier captures the READ data.

Bench tests indicate that the actual attack and release times are 72 ns and 20 ns, respectively (this is about 50% of the data sheet specifications). This means that the data is stable for about 160 ns prior to the end of transfer.

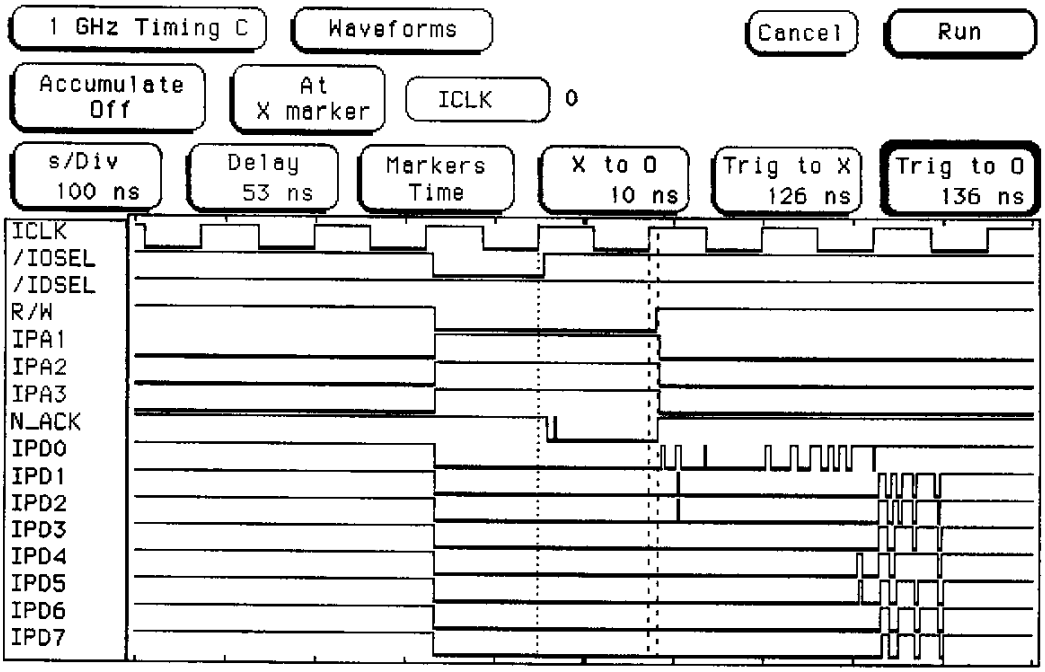


Figure 5-2 I/O Write at IPA = 07

5.4 Maximum Loads (Direct Current)

Paragraph 1.4(Features), page 1-2, indicates that the minimum output current for all channels is ±2 mA, with a typical short-circuit current of ±25 mA, and a maximum load capacitance of 500 pF.

Tables 5-2 through 5-4 present typical direct current load test results for the DAC128F5, unit #101. The system configuration is represented in Figure 5-1.

A variable load connected between pin 1 (ground) and pin 3 for channel #1 testing of typical (low droop) maximum loading was used to develop Table 5-2. For each table entry, a 10 KΩ load was applied to determine a minimum load output voltage. The load resistance was then decreased until the output drooped about 10 mV (about 4 bits of error). At this point, the load resistance was measured and the output current was calculated. Statistical data at the end of the table shows the average current drive capacity is about three times the minimum specification of ±2 mA.

Under heavy loading conditions, errors may be introduced by the series termination resistor in the optional “R” outputs of the DAC when attempting to drive high capacitance loads (e.g. using long ribbon cables).

Table 5-2 Maximum Currents

Code	10 KΩ Load VOUT	Ω @Droop	@VOUT	Calculated Current (mA)
000	-4.99 V	635.0 Ω	@ -4.98 V	7.843
200	-3.74 V	458.0 Ω	@ -3.73 V	8.144
400	-2.497 V	402.0 Ω	@ -2.487 V	6.187
600	-1.249 V	230.1 Ω	@ -1.239 V	MIN 5. 385
700	-0.624 V	107.4 Ω	@ -0.614 V	5.717
100	-4.36 V	418.0 Ω	@ -4.35 V	MAX 10.407
300	-3.122 V	534.0 Ω	@ -3.112 V	5. 828
500	-1.873 V	321.3 Ω	@ -1.863 V	5.798
800	-00.1 Mv	N/A	N/A	N/A
900	+0.623 v	95.1 Ω	@ +0.613 V	6.446
B00	+1.872 v	289.5 Ω	@ +1.862 V	6.432
D00	+3.121 v	486.0 Ω	@ +3.111 V	6.401
F00	+4.37 v	725.0 Ω	@ +4.36 V	6.014
A00	+1.248 v	205.6 Ω	@ +1.238 V	MIN 6.021
C00	+2.497 v	403.0 Ω	@ +2.487 V	6.171
E00	+3.74 v	393.0 Ω	@ +3.73 V	9.491
FFF	+4.99 v	656.0 Ω	@ +4.98 V	MAX 7.591

NOTE: 10 Mv droop ≈ 4 bits error

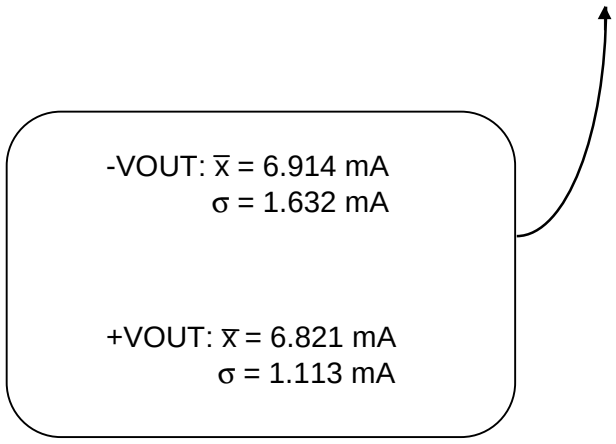


Table 5-3 was developed by placing a fixed load of 469 Ω between pins 1 and 4 of the I/O cable's termination block, and then measuring the error signal across pins 3 and 4 or across the series termination resistor. Note that with this load, the DAC128F5 is sinking and sourcing over 10 mA of current at the full scale settings.

Table 5-3 Heavy Loading Errors

Code	$^{ERROR}V_{(4-3)}$	≈ # Bits Error
000	195.4 mV	80
100	171.0 mV	70
200	146.5 mV	60
300	122.0 mV	50
400	95.5 mV	40
500	73.1 mV	30
600	48.7 mV	20
700	24.4 mV	10
800	00.0	0
900	-24.3 mV	10
A00	-48.7 mV	20
B00	-73.1 mV	30
C00	-97.5 mV	40
D00	-121.9 mV	50
E00	-146.3 mV	60
F00	-170.8 mV	70
FFF	-195.2 mV	80

Table 5-4 (page 5-6) was developed by placing fixed loads of 997 Ω, 467 Ω, 221.6 Ω, and 99.8 Ω between pins 1 and 3 of the I/O cable's termination block, and then measuring the DAC128F5's current drive.



NOTE: Significant droop errors exist at the high voltage outputs for the lower resistance loads.

Table 5-4 Fixed Loads

997 Ω			467 Ω		221.6 Ω		99.8 Ω	
Code	**Voltage**	**Current**	**Voltage**	**Current**	**Voltage**	**Current**	**Voltage**	**Current**
000	-4.98 V	4.995 mA	-4.97 V	10.642 mA	-4.95 V	22.338 mA	-3.37 V	33.768 mA
100	-4.36 V	4.373 mA	-4.35 V	9.315 mA	-4.33 V	19.540 mA	-3.37 V	33.768 mA
200	-3.73 V	3.741 mA	-3.73 V	7.987 mA	-3.71 V	16.742 mA	-3.36 V	33.667 mA
300	-3.11 V	3.119 mA	-3.11 V	6.660 mA	-3.09 V	13.944 mA	-3.06 V	30.661 mA
400	-2.493 V	2.501 mA	-2.488 V	5.328 mA	-2.477 V	11.178 mA	-2.452 V	24.569 mA
500	-1.870 V	7.876 mA	-1.866 V	3.996 mA	-1.858 V	8.384 mA	-1.839 V	18.427 mA
600	-1.247 V	1.251 mA	-1.244 V	2.664 mA	-1.239 V	5.591 mA	-1.226 V	12.285 mA
700	-0.623 V	625.0 mA	-0.622 V	1.332 mA	-0.619 V	2.793 mA	-0.613 V	6.142 mA
800	-00.1 mV	0.1 mA	-00.1 mV	0.2 mA	-00.1 mV	0.5 mA	-00.1 mV	1.0 mA
900	+0.623 V	625.0 mA	+0.621 V	1.330 mA	+0.619 V	2.793 mA	+0.613 V	6.142 mA
A00	+1.247 V	1.251 mA	+1.244 V	2.664 mA	+1.239 V	5.591 mA	+1.228 V	12.305 mA
B00	+1.869 V	1.875 mA	+1.866 V	3.996 mA	+1.858 V	8.384 mA	+1.841 V	18.447 mA
C00	+2.493 V	2.501 mA	+2.488 V	5.328 mA	+2.478 V	11.182 mA	+2.369 V	23.737 mA
D00	+3.116 V	3.125 mA	+3.110 V	6.660 mA	+3.098 V	13.980 mA	+2.369 V	23.737 mA
E00	+3.74 V	3.751 mA	+3.73 V	7.987 mA	+3.71 V	16.742 mA	+2.364 V	23.687 mA
F00	+4.36 V	4.373 mA	+4.35 V	9.315 mA	+4.33 V	19.540 mA	+2.361 V	23.657 mA
FFF	+4.98 V	4.995 mA	+4.97 V	10.642 mA	+4.48 V	20.217 mA	+2.359 V	23.637 mA

5.5 Slew Time Tests

While the specifications presented in paragraphs 1.4 and 2.4 indicate that the DAC128F5 slew rate is 3.0 ± 0.3 V/μs and the settling time for a full scale jump is 7 ± 2 μs for a 5 KΩ and 500 ρF load, actual measurements provide much better performance characteristics.

Figure 5-3 presents one of several Digital Storage Oscilloscope diagrams that were captured for the generation of Table 5-5 Slew Time Tests.

Table 5-5 Slew Time Tests

DAC Change	Load	Connected @	Time (μs)
+ Full Scale	Open & 50 ρF	Pins 1 & 3	2.37
- Full Scale	Open & 50 ρF	Pins 1 & 3	2.32
+ Full Scale	5.00 KΩ & 574 ρF	Pins 1 & 4	2.54
- Full Scale	5.00 KΩ & 574 ρF	Pins 1 & 4	2.66
+ Full Scale	5.00 KΩ & 574 ρF	Pins 1 & 3	2.72
- Full Scale	5.00 KΩ & 574 ρF	Pins 1 & 3	2.62

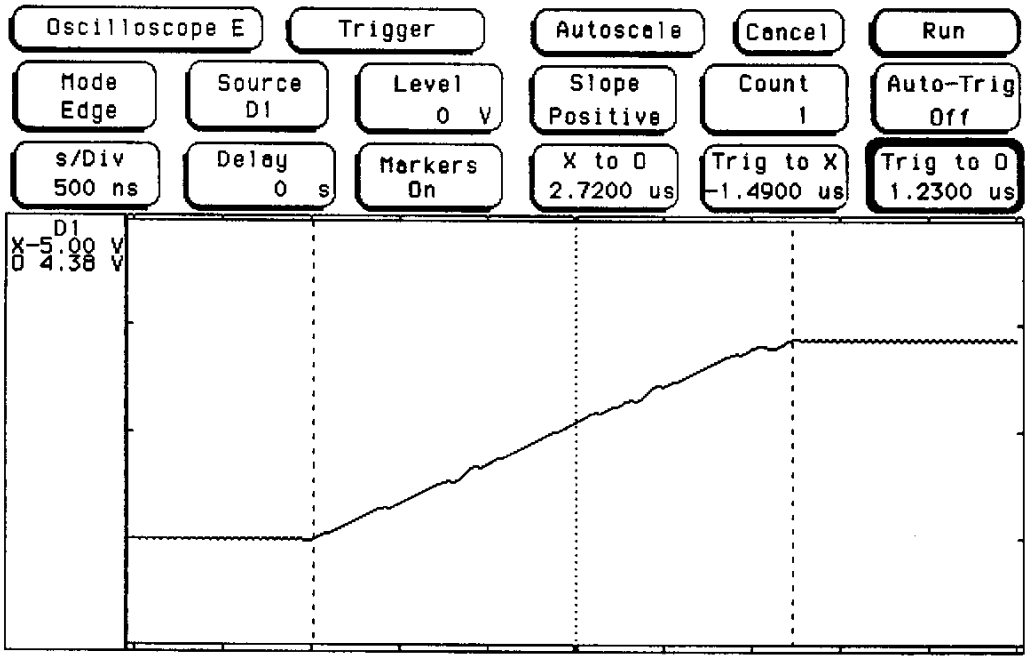


Figure 5-3 Typical Slew Time Waveform

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6. 0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the DAC128F5 IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the SYSTRAN team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and SYSTRAN reserves the right to modify submissions to provide for more generic appeal, when necessary.

6.2 Analog Self-Test

This application uses a single DAC128F5 as a programmable, precision voltage source performing a substitution calibration function as part of an analog subsystem “Built-In Self-Test”. Figure 6-1 presents the overall block diagram, details on switching/wiring, and a logic diagram showing the general connection scheme.

The block diagram (Figure 6-1) shows an extremely simplified, basic implementation of this application. A RELAY16 board is used as an analog switch, providing a multiplexing function to the inputs of a pair of ADC128F1 IP Modules from either 16 input signals that are normally being converted by the ADC128F1’s, or from 8 calibration voltage sources provided by the single DAC128F5. This is only one of many techniques and configurations possible for this type of subsystem. The assumption made for this implementation is that only one ADC128F1 would be checked for calibration at a time. Therefore, each channel of the DAC128F5 is connected to one channel of each of the two ADC128F1’s via proper switching of the individual relays on the RELAY16.

6.2.1 Relay Wiring

The middle section of Figure 6-1 provides a single channel detail of the wiring through one set of Form ‘C’ contacts on the RELAY16. Since the RELAY16 powers-up with all relays in their OFF state (connection is made between the common and the normally closed contacts), the presented configuration allows the ADC128F1’s to power-up sampling the external signal inputs. This configuration was chosen because the calibration mode is the exceptional mode of operation, and because less power is consumed with all of the relays in their OFF state. With all relays OFF (minimum power) the ADC128F1’s are fed the signals that normally need conversions.

6.2.2 Resource Sharing

The bottom of Figure 6-1 presents one-fourth of the system, showing how one DAC channel is feeding two separate relays which in turn feed two different ADC128F1 IP Module boards. As indicated previously, this configuration is completely arbitrary, and should be modified as application requirements dictate.

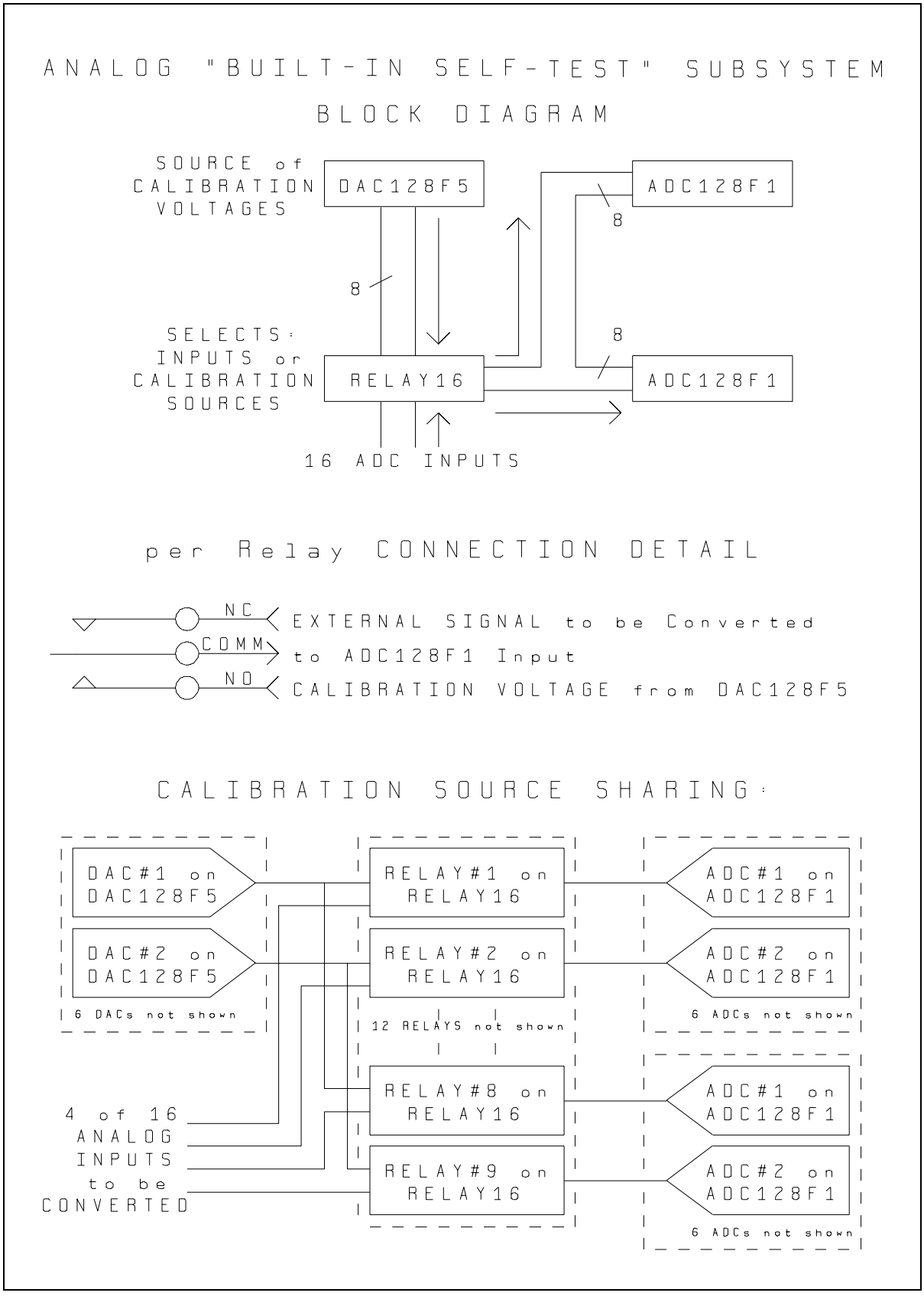


Figure 6-1 Analog Self-Test Application

6.3 Programmable Window Comparator

Figure 6-2 presents a programmable, non-overlapping, hex (6) window comparator. This comparator uses seven of the eight channels on one DAC128F5 to establish the window boundaries, and three (external) quad open-collector voltage comparators. This is only one example of many possible configurations that are primarily dependent upon the number of windows needed for a particular application. Use this presentation for a sorting function or an Automatic Test Equipment application where a signal's presence and general vicinity can be ascertained quickly. When the "real" value is not needed; this approach is "close enough". For instance, if "Vin" should be near ground, then the windows can be set up to determine how close to ground it is by lumped-spectrum indication. This technique is handy if there is noise riding on the average signal energy level making an analog-to-digital conversion too tricky or expensive to justify the information gained.

The Voltage chart in the lower left portion of Figure 6-2 presents the operational story. The assumption in the application is that:
DAC#1's Voltage ≥ DAC#2's Voltage ≥ DAC#3's Voltage ≥ DAC#4's Voltage ≥ DAC#5's Voltage ≥ DAC#6's Voltage ≥ DAC#7's Voltage.
Additionally, since the full-scale output of the DAC128F5 is ±5 V, the comparator outputs will all be zeros if:
Vin ≥ DAC#1's Voltage; or, Vin ≤ DAC#7's Voltage.
There is no requirement to maintain this sequential voltage hierarchy, as some out-of-boundary testing mandate.

For any given pair of comparators bounded by two DAC voltage references, if Vin is greater than the upper DAC's voltage or less than the lower DAC's voltage, the output will be low. However, if Vin falls between both DAC voltages, the output will be high.

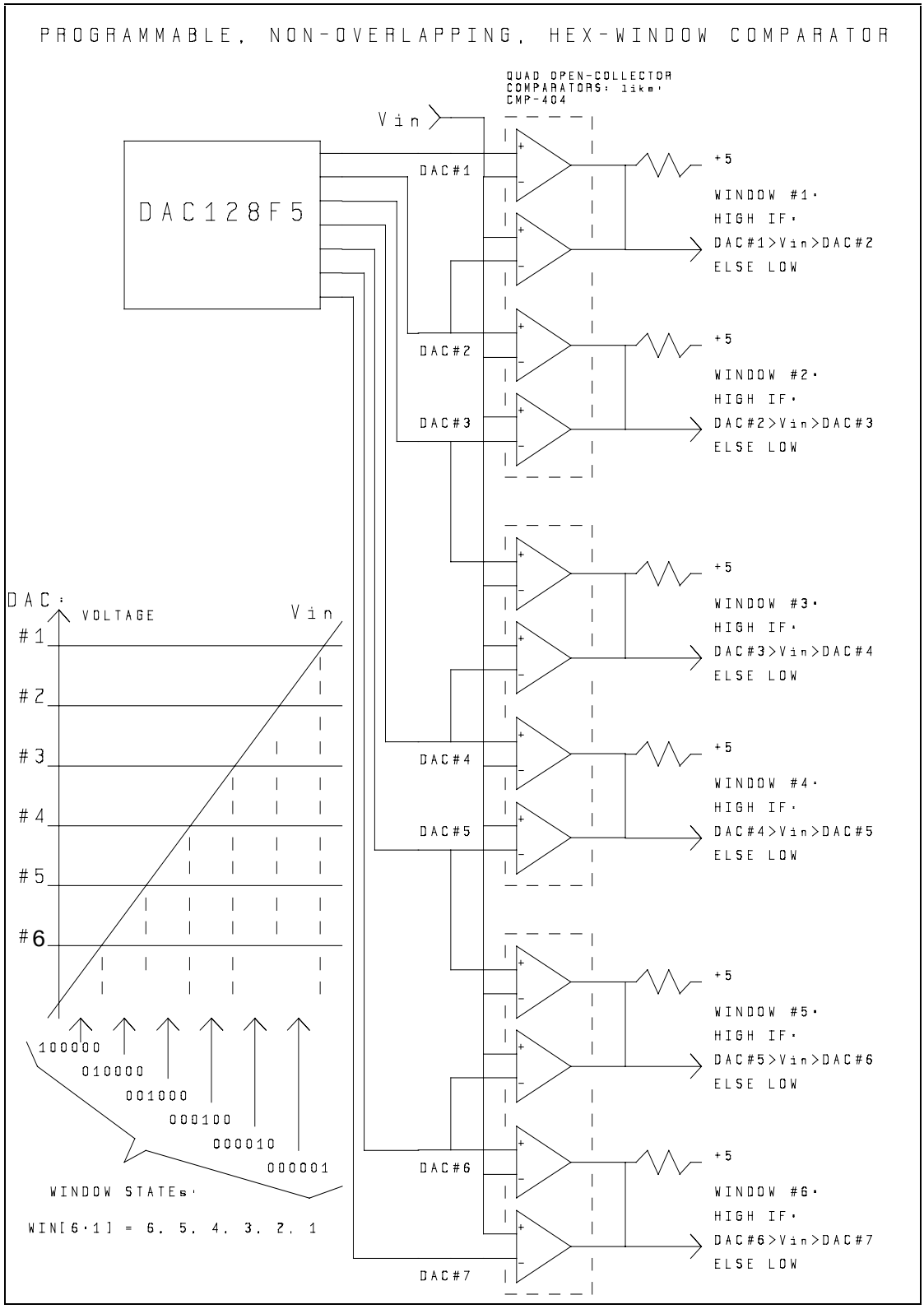


Figure 6-2 Window Comparator Application

APPENDIX A
SCHEMATICS

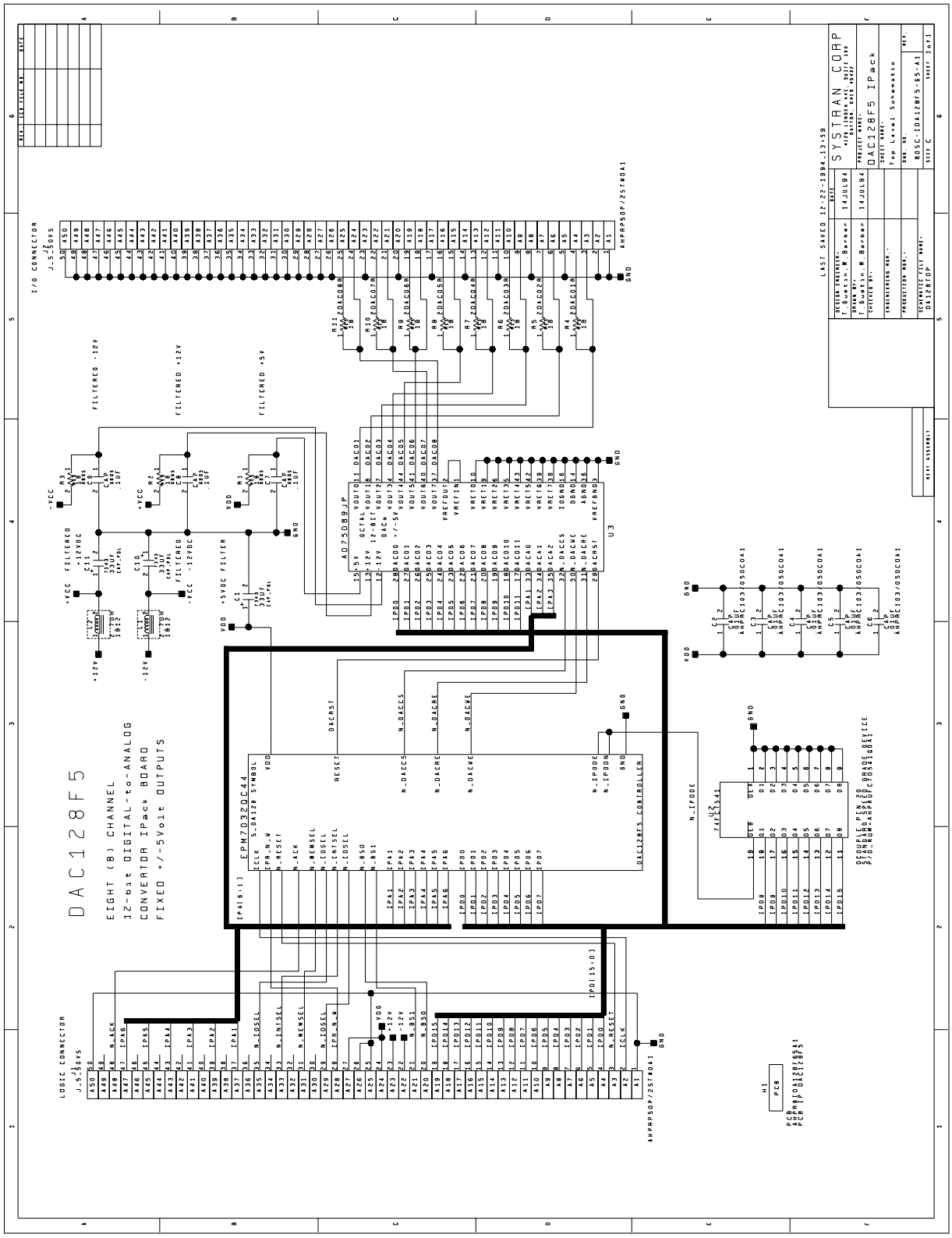


Figure A-1 Schematic #

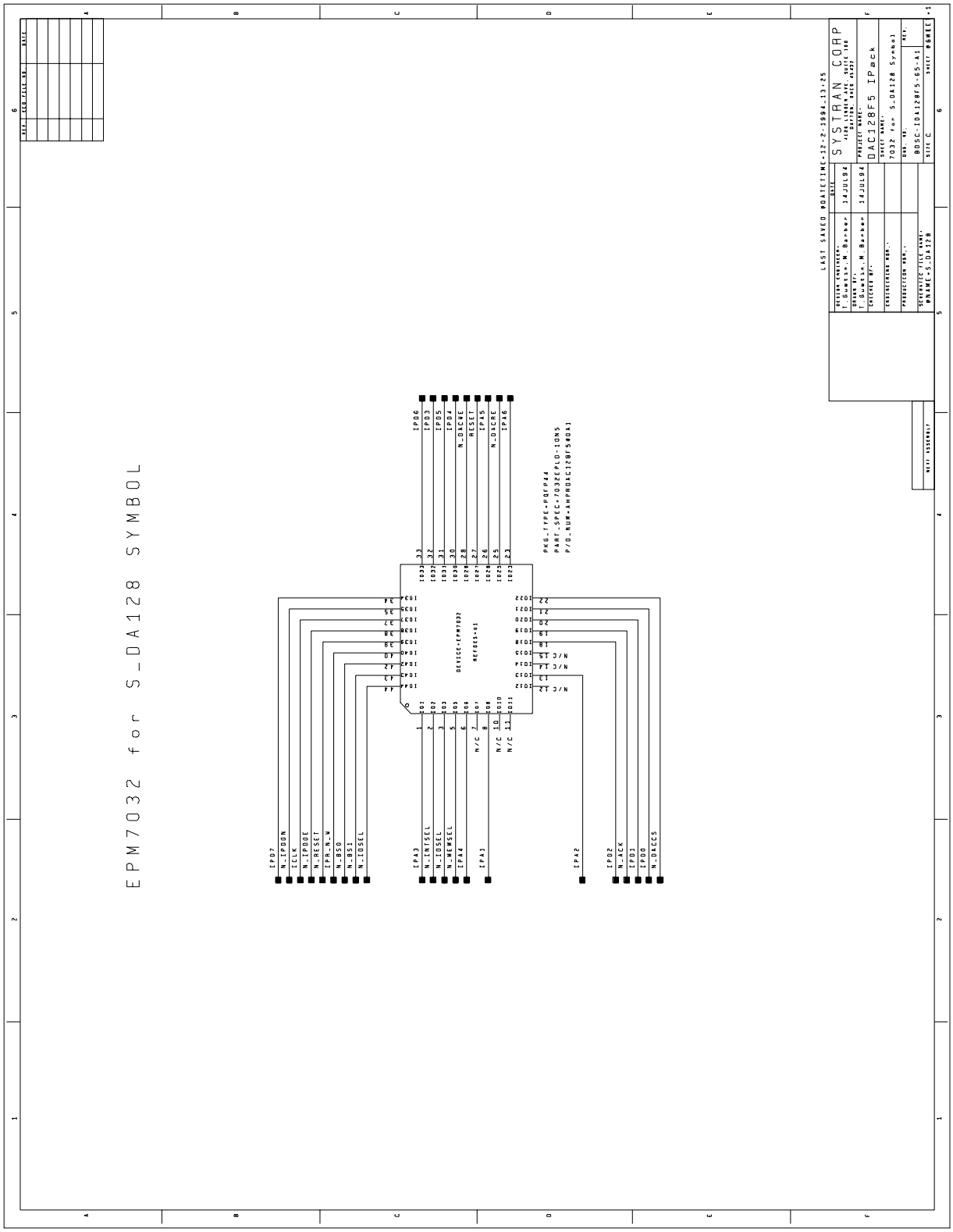


Figure A-2 Schematic #2

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