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OPTDO32

32-Channel Opto-isolated Digital-Output IP Module Hardware Reference

Document No. B-T-MR-OPTDO32#-A-0-A2

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1. INTRODUCTION

1.1 How To Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's 32 channel, opto-isolated, digital-output IP Module, referred to as the OPTDO32 (OPTo-isolated, Digital-output, 32 channels), part number BHAS-OPTDO32.

1.1.2 Scope

This reference manual covers the physical and operational description of the OPTDO32, both from hardware and software perspectives. This manual also contains detailed technical information about the OPTDO32's performance characteristics, and a few typical applications. It is assumed that the reader has a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IP Modules on their carrier(s) of choice.

1.1.3 Style Conventions

- A bit-range is designated by [x:y], where "x" is the left-most bit and "y" is the right-most bit (for example, Data bus [7:0] refers to the least significant eight bits).
- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2               file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- *American National Standard for IP Modules (ANSI/VITA4 - 1995)* published by the VMEbus International Trade Association, 7825 Gelding Dr., Suite 104, Scottsdale, AZ 85260.
- *DID48 48-Channel Debounced Discrete Input Board Hardware Reference* (Doc. No. B-T-MR-DID48).

- *DIO316I Tristateable 48-Channel Digital I/O Board Hardware Reference* (Doc. No. B-T-MR-DIO316I).
- *OPTDO32 Software Library Manual for OS-9 Version 2.4 or Later* (Doc. No. B-T-ML-OPTDO32), Systran Corporation.
- *TRIDO48 Tristateable 48-Channel Digital-output IP Module Hardware* Reference (Doc. No. B-T-MR-TRIDO48).
- Systran Corp. Worldwide Web: www.systran.com.

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2. PRODUCT OVERVIEW

2.1 Overview

The OPTDO32 is a singlewide IP Module, conforming both mechanically and electrically to the *American National Standard for IP Modules (ANSI/VITA 4-1995)*. For a typical quad-IP Module carrier, the OPTDO32 can provide up to 128 opto-isolated digital outputs from any single slot on a computer bus backplane, or can be mixed with other IP Modules for a more customized, modular I/O system solution. Figure 2-1 is a picture of the OPTDO32 board.

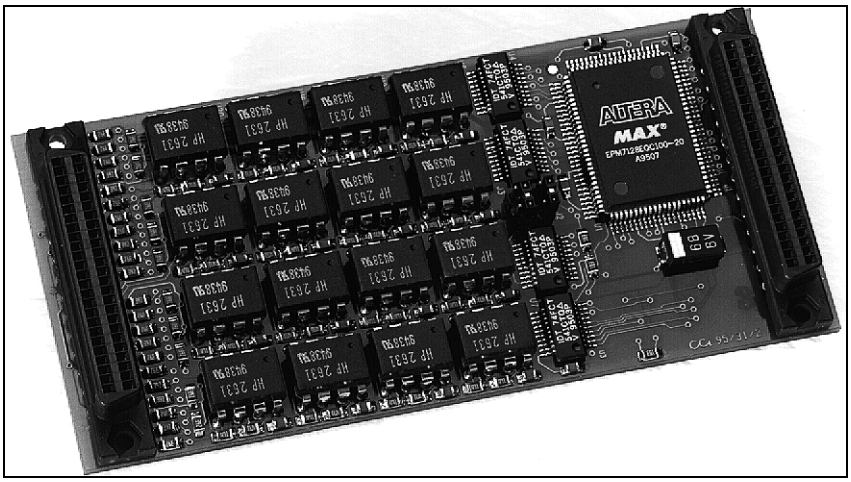


Figure 2-1 OPTDO32 Board

2.1.1 Features

- Four byte-wide ports individually controllable via hardware and/or software.
- Byte-wide grouping of output drivers permits connections to four different power systems, if necessary.
- Board-level hardware status/control:
  - Non-isolated external input to control the “OPEN” versus “ACTIVE”output state conditions on any of the four ports
  - Non-isolated output of status on update of any of the ports
- Switch-selectable power-up default of port “active” versus “open” states
- Switch-selectable logic sense control for “true” versus “inverted” logic
- Open-collector output with per channel sink rating of 13 mA (eight 1.6mA TTL loads) with per-channel built-in pull-up of 3.9 kΩ (≈1.2 mA load); ≡ 10 outputs can be wire-ORed together.
- High-speed coupling with latency ≤ 100 ns.
- Excellent high-voltage electrical insulation specifications.

2.2 Related Product

- Software: 'C' library and OS-9 device-driver routines with documentation.

2.3 Block Diagram Description

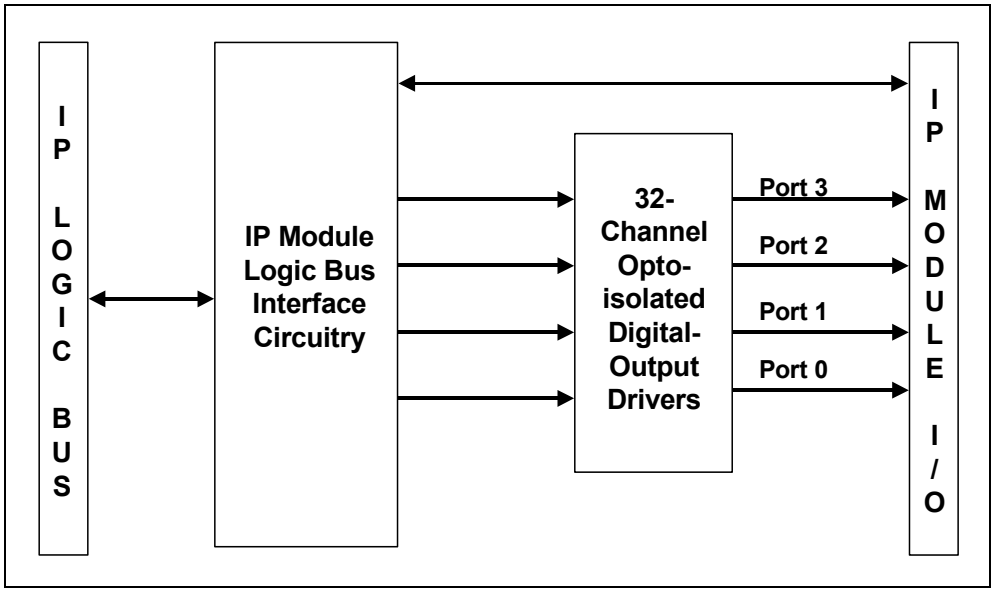


Figure 2-2 OPTDO32 Simplified Block Diagram

Figure 2-2 is a simplified block diagram of the OPTDO32. On the left side of the diagram is the IP Module Logic Bus connector through which all transfers between the IP Module carrier and the OPTDO32's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface Circuitry" contains all of the write/read-back data registers, the ID PROM data, control/status register, external hardware handshake circuitry, port control signal generators, and IP Module transfer sequence/control and data bus interface logic. All of this logic is implemented in a single EPLD device. The block labeled "32-Channel Opto-Isolated Digital-output Drivers" contains 32 LED drivers using buffers, and 16 pairs of dual-opto-couplers. A single wire that is double arrowed, between the EPLD and the I/O connector is the bi-directional Control/Status Input/Output (CSIO) line. On the right side of the diagram is the OPTDO32's I/O connector, providing open-collector sink connections for all 32 drivers, per-byte-lane power and ground connections for the I/O-side of the opto-couplers, a ground reference for the non-isolated CSIO line, as well as CSIO itself.

2.4 Detailed Block Diagram

Figure 2-3 presents a detailed block diagram of the OPTDO32. Again on the left side is the IP Module's Logic Bus connector through which all host carrier transfers take place. The four 8-bit ports are paired-off into two 16-bit registers or "words". Each "word" contains two 8-bit registers, a 16-bit tristateable gate for driving the IP Data bus (IPDbus) during I/O reads, and an invertible 16-bit Light-Emitting Diode (LED) driver port that directly feeds a pair of octal LED low-side drivers. The architecture supports byte-wide writes to either octal register, or to both of them as 16-bit writes. All I/O register reads are performed at the "word" width of 16 bits, only.

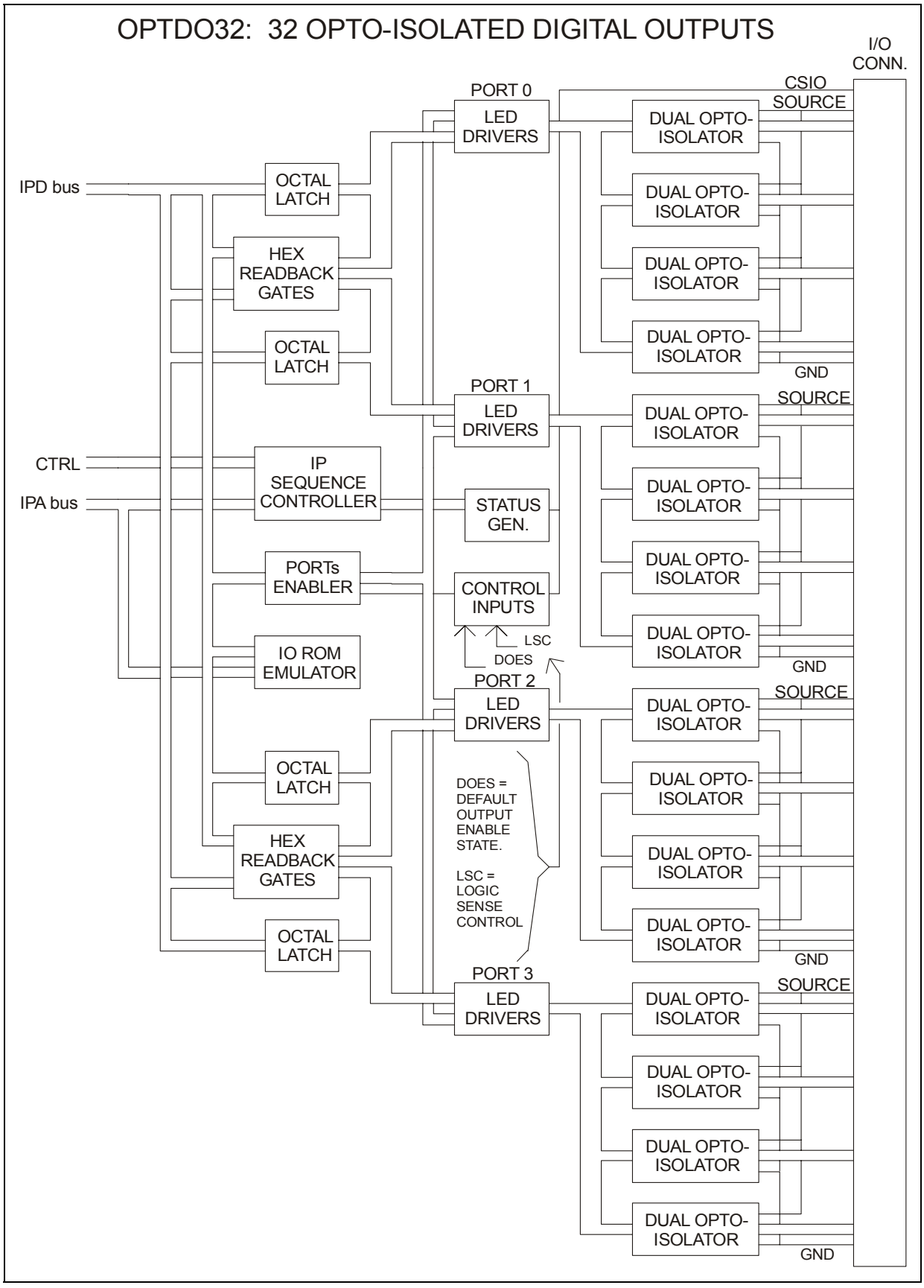


Figure 2-3 OPTDO32 Detailed Block Diagram

2.4.1 Control/Status Register

The control and status register has a similar IP Module carrier interface. This logic is depicted by the blocks labeled “PORTs ENABLER”, “CONTROL INPUTs” and “STATUS GEN.”. The “PORTs ENABLER” consists of a 12-bit write & 16-bit read register as part of the port-enabling logic. The “CONTROL INPUTs” interface handles the power-up initialization circuitry as determined by the state of the Default Output-enable States (DOES) input, the registered data ports' Logic Sense Control (LSC) for “true” or “inverted” logic drive of the ports, and the real-time output enabling and disabling of the ports via the hardware CSIO line, when activated. The “STATUS GEN.” (generator) logic develops the status output portion of the hardware handshake CSIO line, when it is not needed as an input for port-enabling operations. It is important to note that the CSIO line is not opto-isolated, since most handshake applications, whether for control or status, will be conducted at the logic level, often within the same chassis in which the OPTDO32(s) reside(s).

2.4.2 ID PROM Emulator

The ID PROM Emulator is the circuitry that presents the proper data patterns to the lower 8 bits of the IPDbus, with upper-byte zero-fills, during the ID (read) transfers. Emulating the never-changing ID information in this way reduces parts count and costs, and increases system reliability with its associated MTBF value.

2.4.3 Sequence Controller

The IP Module Sequence Controller logic performs orderly transfers between the OPTDO32 and its carrier. Included in this block are the valid select signal detectors, valid address detectors, transfer sequence state machines, including acknowledgement and hold cycle circuits.

2.4.4 Open-collector Port Drivers

The sixteen blocks labeled “DUAL OPTO-ISOLATOR” contain the actual open-collector port drivers. Note that they are functionally and electrically configured as octal groups, so that four separate systems can be interfaced via the OPTDO32 without regard to system grounding requirements. Each group has its own unique supply source input and ground return lines. The port side of the opto-isolators contain logic that must be powered from a five volt power source for the circuitry to perform properly. It is this same power source to which are connected the pull-up resistors for each of its attached open-collector outputs.

2.5 Detailed Description

The OPTDO32 was developed using VHDL and Synthesis, and targeted to an ALTERA EPLD. The design was schematic-captured and integrated to standard logic devices, connectors, and discrete components using Innoveda CAE tools.

2.6 Port Details

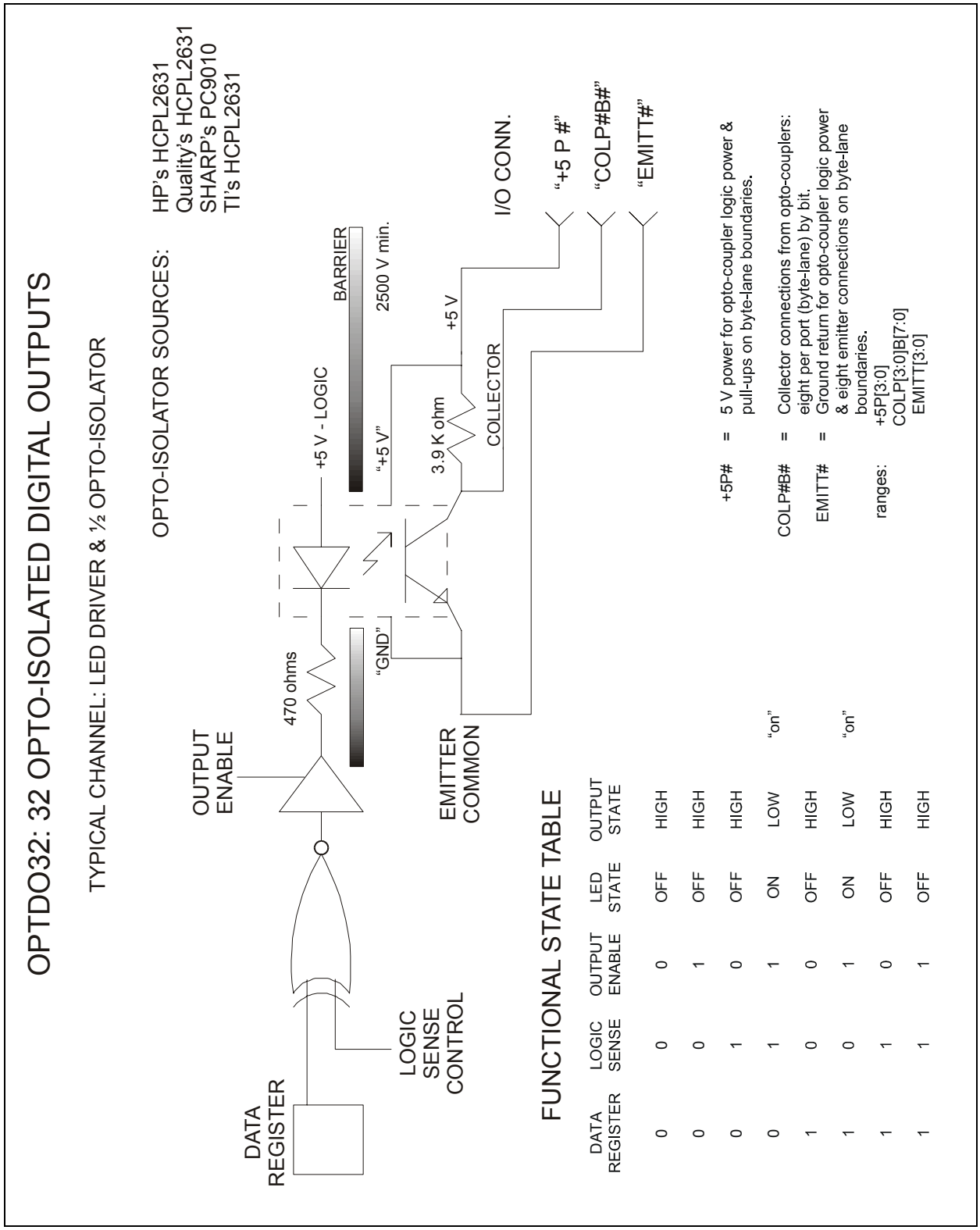
Figure 2-4 presents some detailed logic information for a single channel of the OPTDO32. The functional state table presents the relationship between the data contained within a register as written by the IP Module’s carrier, the LSC switch, and the output-enable control signals as they pertain to the application of sink current for the opto-coupler’s LED, and the resultant logic state at the user’s I/O connected circuitry.

2.7 DOES and LSC Switches

The DOES switch permits powering up of this IP Module with all of the outputs enabled or disabled since the logic state of the DOES switch during the N_RESET determines the initial state of the least significant eight bits in the control/status register. If DOES is high, control/status bits 7 down to 0 (CR[7:0]) are set high; if DOES is low, CR[7:0] are cleared low. These bit states correspond to the software-control states for enabling outputs and disabling outputs, respectively.

The LSC switch controls which logic sense of the data register contents is applied to the LED drivers. If the LSC switch is high, the true data register contents are directly applied to the LED drivers. If the LSC switch is low, the inverted data register contents are applied to the LED drivers.

All of the open-collector outputs on the I/O connector will be ‘ON’ in their low states on power-up (provided the DOES switch is set high to enable the outputs and the LSC is set high for “true” logic) since the data registers power up to zeros. If the DOES switch is low, the LED drivers will all be disabled, preventing sink current to the LEDs and turning “OFF” all the outputs to their high states, regardless of the LSC switch setting.



FUNCTIONAL STATE TABLE

DATA REGISTER	LOGIC SENSE	OUTPUT ENABLE	LED STATE	OUTPUT STATE
0	0	0	OFF	HIGH
0	0	1	OFF	HIGH
0	1	0	OFF	HIGH
0	1	1	ON	LOW "on"
1	0	0	OFF	HIGH
1	0	1	ON	LOW "on"
1	1	0	OFF	HIGH
1	1	1	OFF	HIGH

Figure 2-4 Typical Channel Detail

Table 2-1 presents the state of the OPTDO32 on power-up (data registers power up to zeros), as a function of both of the board's jumper switches: DOES and LSC.

Table 2-1 Power-up State: DOES and LSC

State	DOES:	LSC:	Outputs:
1	LOW	LOW	DISABLED (high)
2	LOW	HIGH	DISABLED (high)
3	HIGH	LOW	ENABLED (high)
4	HIGH	HIGH	ENABLED (low)

In states 1 and 2 the data register contents are disregarded since the DOES = LOW causes the LED drivers to be tristated, thereby turning off the outputs. State 3 outputs are high because the data register contents are all zeros, the LSC switch calls for inverted logic (zeros in the registers provide high-state outputs), and the DOES switch has enabled all of the LED drivers. It is the data register contents that turns off the outputs. State 4 is the only power-up state where all of the outputs are turned ON. The LSC switch requests that "true" logic be invoked, where zeros in the data registers provide low (ON) states on the outputs, and the DOES switch is configured to permit this to happen on power-up.

The OPTDO32's application, of course, will help determine the desired settings. For instance, if "true" logic is being used in the software, and the OPTDO32, by being in its low state, turns on actuators which should not be ON until the software has total control of the system, then the DOES must be configured to disable the outputs on power-up, and the logic sense switch must be set for "true" logic. State 2 accomplishes this. The shipping default for the DOES and LSC jumper switches is state 2. A wired-OR, asserted-low, open-collector bus might use state 3 configuration for its power-up states.

2.7.1 CSIO Line

The CSIO signal line is a multi-function handshake line that acts as either a control-input (power-up default), or as a status-output signal, as determined by CR[12].



NOTE: This I/O connection is not opto-isolated. CSIO is located at pin #49 on the I/O connector, and its logic ground reference is located at pin #50. This ground connects directly to the carrier's ground; it is not isolated.

INPUT

As an input, in conjunction with CR[7:0], the CSIO can selectively control the "active" versus "disabled" states of each of the individual byte-lane ports using selectable sense control. Each byte-lane is assigned two bits of port-state control in the control/status register as described in Table 2-2.

Table 2-2 Port State Control

Port #	Control/Status Register
0	[1:0]
1	[3:2]
2	[5:4]
3	[7:6]

Table 2-3 shows how the CSIO Input line controls the byte-lane port outputs. A bit combination of '00' disables the port just like DOES = LOW on power-up. A bit combination of '11' enables the port just like DOES = HIGH on power-up. A bit combination of '01'permits the CSIO input line to enable the outputs if it is driven high or left unconnected (there is a 10 kΩ pull-up resistor on CSIO), and disable the outputs if it is driven low by external logic. A bit combination of '10' permits the CSIO input line to disable the outputs if it is driven high or left unconnected, and enable the outputs if it is driven low.

Table 2-3 CISO Input Line Controls Port Output

Port X	CSIO Input Line	I/O State
00	--	Outputs disabled
01	HIGH	Enable Outputs
	LOW	Disable Outputs
10	HIGH	Disable Outputs
	LOW	Enable Outputs
11	--	Outputs enabled

OUTPUT

Table 2-4 shows how CSIO performs as an output as determined by the state combination of CR[15:13]. As an output, the CSIO can selectively provide a pulse output when any individual register or all registers are updated with new information, or a steady-state high or low logic state. If CSIO is not needed as an input, as determined by the fact that the bit pairs within CR[7:0] are all '00' or '11' combinations, then (and only then) CSIO can be used as an output status signal by setting CR[12] of the control/status register to '1.'

Table 2-4 CISO Output Driven by CR [15:13]

CR[15]	CR[14]	CR[13]	Function:
0	0	0	Pulse out on port #0 update
0	0	1	Pulse out on port #1 update
0	1	0	Pulse out on port #2 update
0	1	1	Pulse out on port #3 update
1	0	0	Always LOW
1	0	1	Always LOW
1	1	0	Pulse out on any I/O write
1	1	1	Always HIGH

OPERATIONAL HINTS

If CSIO is configured as an output, and a change is made in any of the bits of CR[7:0] that indicate that the CSIO is needed as an input, the logic within the EPLD will automatically clear CR[12] and convert the CSIO line to an input function, whether a deliberate write of a '0' to CR[12] is performed, or not.

Changing the function of CSIO from an input to an output requires two sequential write operations.

- Write of ''11' or '00' bit pairs at CR[7:0] to first clear the need for CSIO as an input; then
- Write of a '1' into CR[12] to turn CSIO into an output status signal.

Table 2-5 illustrates some of the CSIO functions discussed above.

Any other bit combinations for CR[7:0] require CSIO to be an input. Additionally, CR[11:8] are not used, and read-back as zeros. Any attempts to write a '1' to CR[12] of the control register (attempting to make CSIO an output) will be bit-blocked by the EPLD's logic if CSIO is needed as an input for CR[7:0]. Subsequent reads of CR[12] will verify that it remained a logic zero state.

Table 2-5 CSIO Functions

CR[7:6]	CR[5:4]	CR[3:2]	CR[1:0]	FUNCTION
00	00	00	00	All ports disabled; CSIO can be an OUTPUT
00	00	00	11	Port #0 is Enabled; Ports #1, #2, & #3 are Disabled; CSIO can be an OUTPUT
00	00	11	00	Port #1 is Enabled; Ports #0, #2, & #3 are Disabled; CSIO can be an OUTPUT
00	11	00	00	Port #2 is Enabled; Ports #0, #1, & #3 are Disabled; CSIO can be an OUTPUT
11	00	00	00	Port #3 is Enabled; Ports #0, #1, & #2 are Disabled; CSIO can be an OUTPUT
00	00	11	11	Ports #0 & #1 are Enabled; Ports #2 & #3 are Disabled; CSIO can be an OUTPUT
11	11	00	00	Ports #2 & #3 are Enabled; Ports #0 & #1 are Disabled; CSIO can be an OUTPUT
11	00	00	11	Ports #0 & #3 are Enabled; Ports #1 & #2 are Disabled; CSIO can be an OUTPUT
00	11	11	00	Ports #1 & #2 are Enabled; Ports #0 & #3 are Disabled; CSIO can be an OUTPUT
00	11	00	11	Ports #0 & #2 are Enabled; Ports #1 & #3 are Disabled; CSIO can be an OUTPUT
11	00	11	00	Ports #1 & #3 are Enabled; Ports #0 & #2 are Disabled; CSIO can be an OUTPUT
00	11	11	11	Ports #0, #1, & #2 are Enabled; Port #3 is Disabled; CSIO can be an OUTPUT
11	00	11	11	Ports #0, #1, & #3 are Enabled; Port #2 is Disabled; CSIO can be an OUTPUT
11	11	00	11	Ports #0, #2, & #3 are Enabled; Port #1 is Disabled; CSIO can be an OUTPUT
11	11	11	00	Ports #1, #2, & #3 are Enabled; Port #0 is Disabled; CSIO can be an OUTPUT
11	11	11	11	ALL PORTS ENABLED; CSIO can be an OUTPUT

2.7.2 Jumpers

Figure 2-5 presents the physical assembly drawing of the OPTDO32. Jumpers J2 and J3 are the “switches” that define the LSC and DOES functions, respectively.

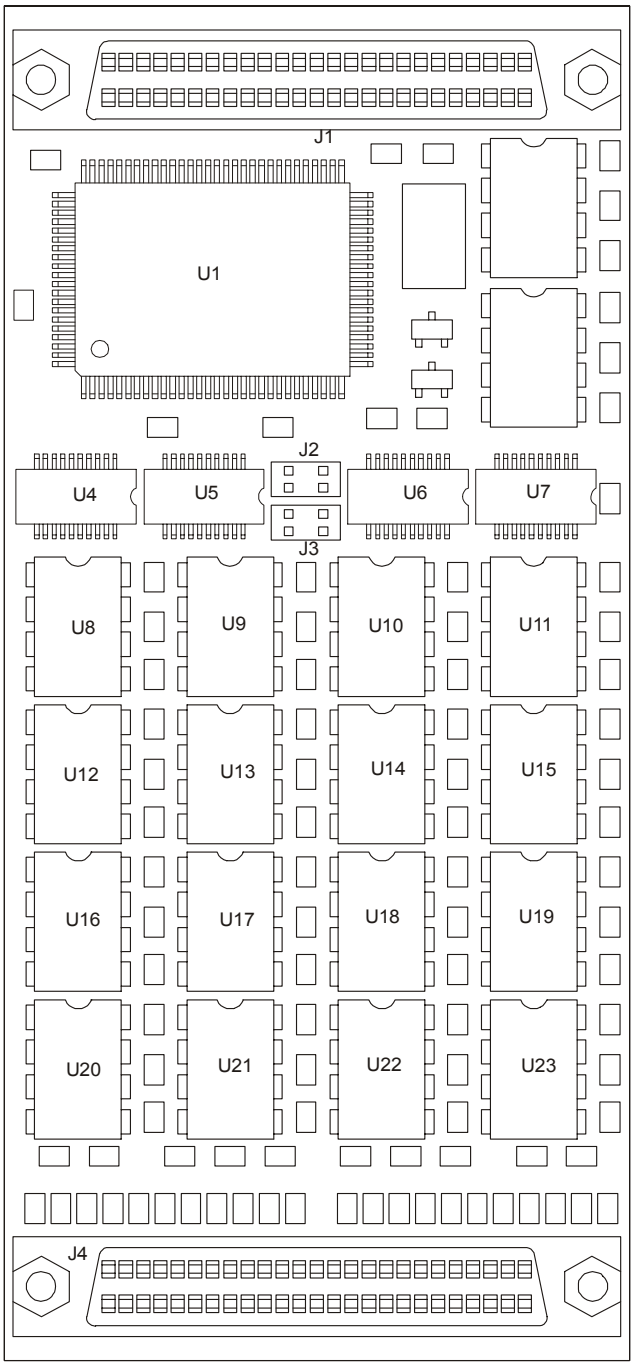


Figure 2-5 OPTDO32 Assembly Drawing

Figure 2-6 is an exploded detail of the switch settings for the LSC and DOES functions. With respect to Figure 2-5, U5 is on the left of Figure 2-6, U6 to the right, and U1 is above. See Table 2-1 for additional detail regarding the DOES and LSC power-up state.

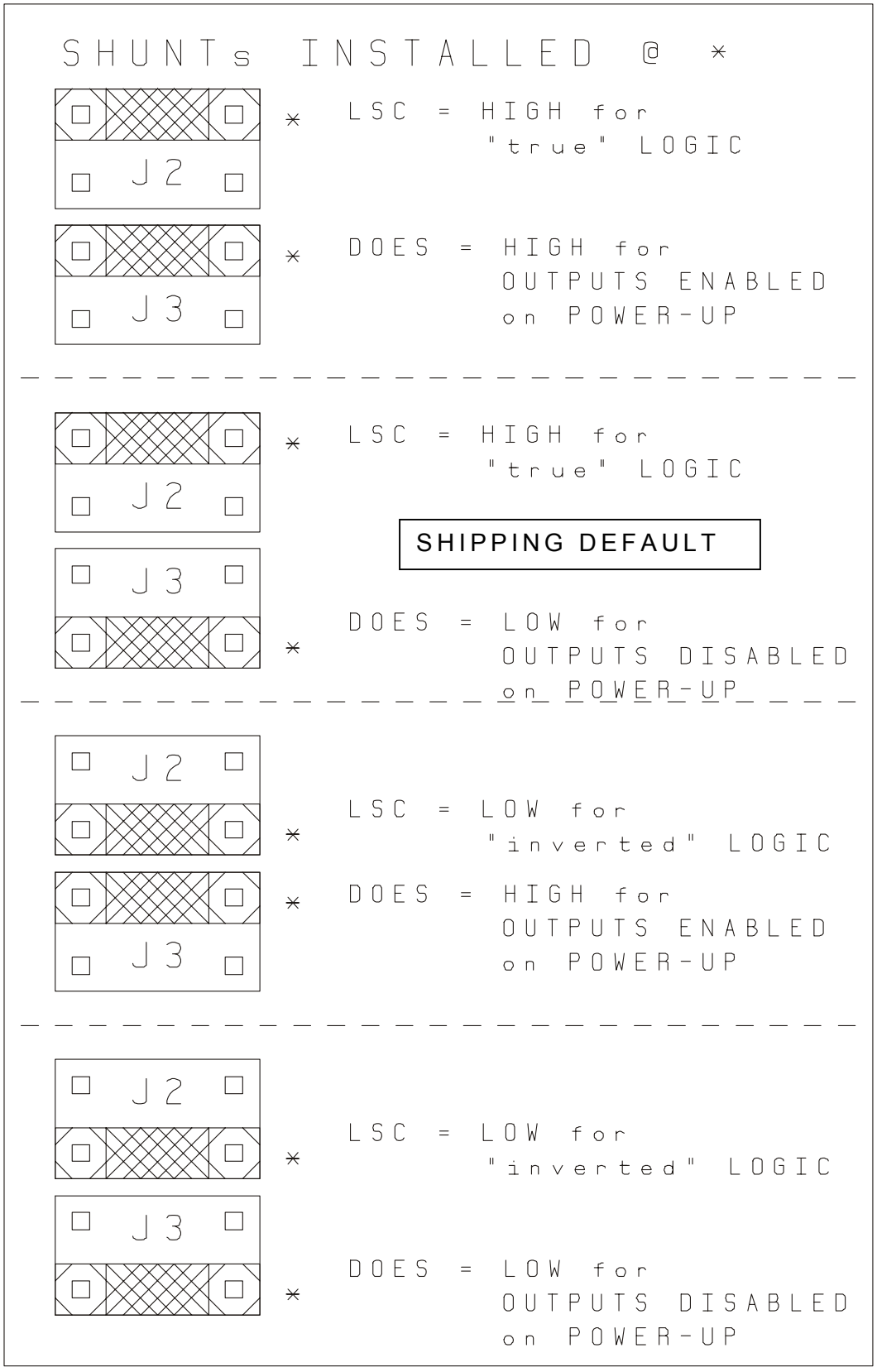


Figure 2-6 OPTD032 "Switches"

2.7.3 Output Characteristics

This short "specification" is a summary and an average of information provided by several sources of the opto-isolators used on the OPTDO32. It is important to note that this data is just for the opto-couplers and does not include delays from preceding and succeeding circuitry, including wiring/cabling. Additionally, the specifications cite test conditions that favor the specification results, and these conditions are not necessarily representative of a typical application of these devices. Additional performance information is provided in chapter 4, PERFORMANCE, using more practical configurations.

- VOL(Low level output voltage) = +0.33 volts typical, +0.6 volts max.
  Vcc = +5.5 V, If = 5 mA, Iol = 13 mA
- tPLH(Propagation delay time, low-to-high level output, from LED input) = 47 ns typical, 75 ns max.
  Vcc = +5.0 V, If = 7.5 mA, Rl = 350 Ω, Cl = 15 pF
- tPHL(Propagation delay time, high-to-low level output, from LED input) = 47 ns typical, 75 ns max.
  Vcc = +5.0 V, If = 7.5 mA, Rl = 350 Ω, Cl = 15 pF
- tr(Rise time) = 25 ns typical, 60 ns max.
  Vcc = +5.0 V, If = 7.5 mA, Rl = 350 Ω, Cl = 15 pF
- tf(Fall time) = 20 ns typical, 60 ns max.
  Vcc = +5.0 V, If = 7.5 mA, Rl = 350 Ω, Cl = 15 pF

Where If ≡ LED's forward current, Iol ≡ low-level (ON-state) output current, Rl ≡ output (Load) pull-up resistor, and Cl ≡ output (Load) capacitance. It is the last parameter that is the most unrealistic test condition for typical IP Module and cabling applications. As will be disclosed in Chapter 4, typical values are on the order of 30 pF.

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3. INSTALLATION

3.1 Unpack the OPTDO32

The OPTDO32 shipping package contains the items listed in Table 3-1.

Table 3-1 OPTDO32 Shipping Package Containers

Qty	Description
1	OPTDO32 Printed Circuit Assembly
1	OPTDO32 User Manual*

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR-OPTDO32).

3.2 Visually Inspect the OPTDO32

Examine the OPTDO32 to determine if any damage occurred during shipping.

3.3 Install the OPTDO32

The OPTDO32 installation requires the tools listed in Table 3-2.



NOTE: The OPTDO32 is an Electrostatic Sensitive Device (ESD). Install the OPTDO32 on an anti-static workbench using good ESD practices to protect the IP Module and its host carrier boards.

Table 3-2 OPTDO32 Installation Tools

Qty	Description
1	ESD static control kit/ground strap/etc.
1	Standard flat-head screwdriver (optional)

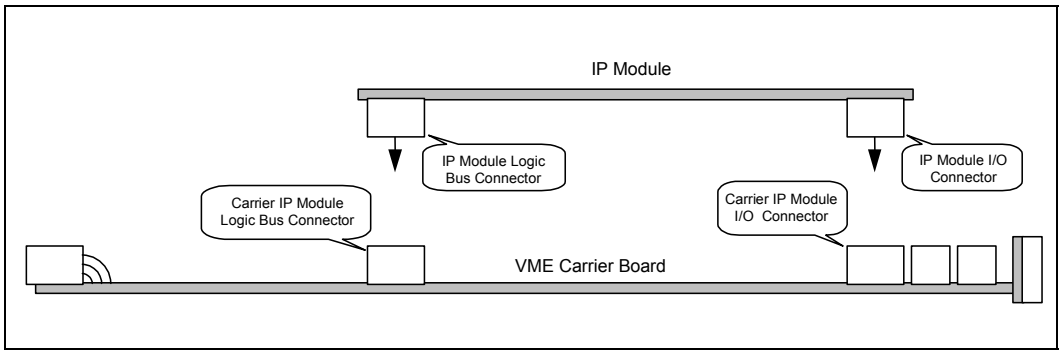


Figure 3-1 OPTDO32 Installed on a VME IP Module Carrier Board

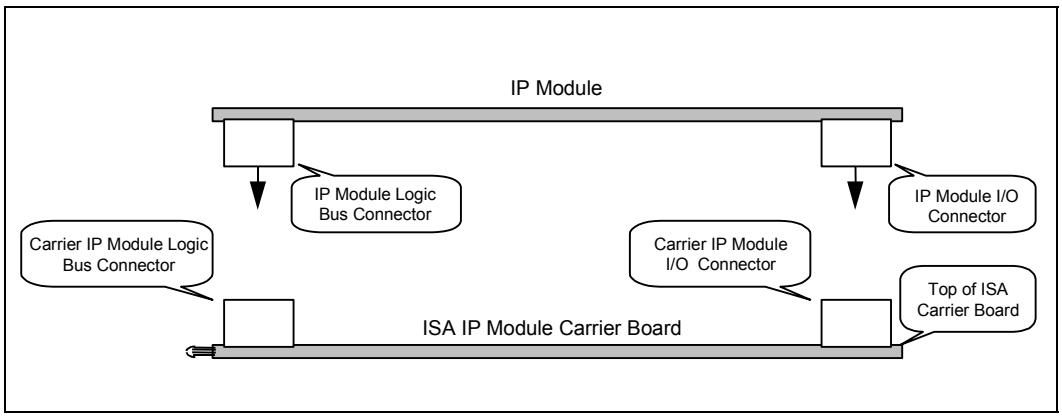


Figure 3-2 OPTDO32 Installed on an ISA IP Module Carrier Board

Figure 3-1 shows how the OPTDO32 is installed on a VME IP Module carrier, and Figure 3-2 shows the board installed on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran.

Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board user's manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the OPTDO32 can be installed.
3. Remove the OPTDO32 from the shipping package and place it on the ESD bench.
4. Install the OPTDO32 onto the carrier board by applying adequate and equal pressure to the OPTDO32 board at both ends.

* 5. Install four M2x5 mm flat-head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the OPTDO32 to the carrier board.

Table 3-3 IP Module Logic bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP I/O Pin #	Signal Name
50	CSIO'S Non-isolating Ground
49	CSIO
48	N/C
47	N/C
46	Port 3, +5 V & pull-up resistor
45	Port 2, +5 V & pull-up resistor
44	Port 1, +5 V & pull-up resistor
43	Port 0, +5 V & pull-up resistor
42	N/C
41	N/C
40	Port 3 Common Emitter
39	Port 2 Common Emitter
38	Port 1 Common Emitter
37	Port 0 Common Emitter
36	N/C
35	N/C
34	N/C
33	N/C
32	PORT 3 BIT 0
31	PORT 3 BIT 1
30	PORT 3 BIT 2
29	PORT 3 BIT 3
28	PORT 3 BIT 4
27	PORT 3 BIT 5
26	PORT 3 BIT 6
25	PORT 3 BIT 7
24	PORT 2 BIT 0
23	PORT 2 BIT 1
22	PORT 2 BIT 2
21	PORT 2 BIT 3
20	PORT 2 BIT 4
19	PORT 2 BIT 5
18	PORT 2 BIT 6
17	PORT 2 BIT 7
16	PORT 1 BIT 0
15	PORT 1 BIT 1
14	PORT 1 BIT 2
13	PORT 1 BIT 3
12	PORT 1 BIT 4
11	PORT 1 BIT 5
10	PORT 1 BIT 6
9	PORT 1 BIT 7
8	PORT 0 BIT 0
7	PORT 0 BIT 1
6	PORT 0 BIT 2
5	PORT 0 BIT 3
4	PORT 0 BIT 4
3	PORT 0 BIT 5
2	PORT 0 BIT 6
1	PORT 0 BIT 7

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4. PERFORMANCE

4.1 Overview

The figures and tables in this section are a collection of typical response times to various system stimuli and IP Module cycles. The tables are summaries of many samples, with representative snapshots for clarification. The intention is to provide a clear understanding of how the OPTDO32 responds under various typical application configurations. This data is reporting "typical" operations at room temperature; the minimum and maximum specifications are presented in the first two sections of this document.

Timing measurements were conducted on the OPTDO32 using an Hewlett Packard model 16500A Logic Analyzer with a 1 GHz Timing Master Module, model 16515A in slot C. The OPTDO32 was installed in the IP Module slot 'A' of a Motorola MVME162-01 VME processor IP Module carrier board, using a Type 1 logic bus extender board with ribbon cable and bus breakout board. Figure 4-1 shows the test configuration for the logic timing measurements. Individual tests identify additional test configuration information, where applicable.

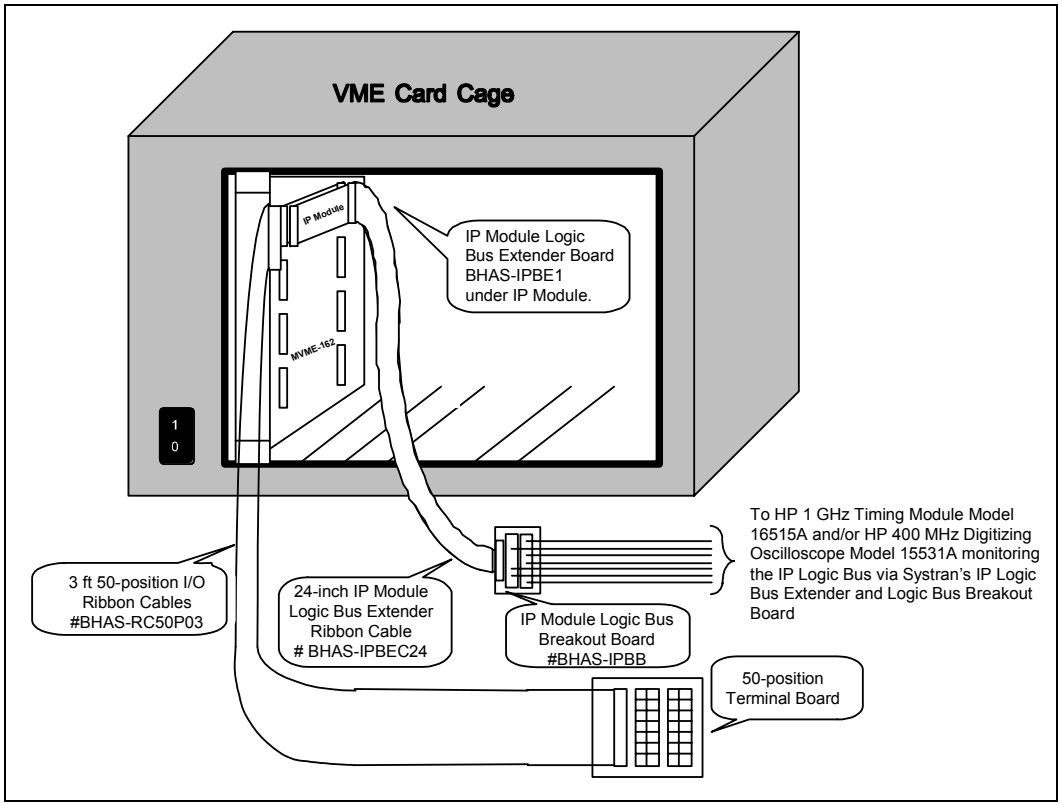


Figure 4-1 IP Module Test Configuration for Logic Timing Measurements

4.2 Carrier Logic Timing

Table 4-1 and Figure 4-2 present information pertaining to the logic interface timing parameters. Specifically, the assertion and negation of the N_ACK signal, and the assertion and release of the IPDbus during read transfers from both ID and I/O space. Table 4-1 presents the minimum, maximum and average timings for each signal event, with an expansion of the IPDbus signal assertions to include the earliest and latest signal events (since there are eight signals being grouped together for these timings). Without exception, all table entries are measured in nanoseconds with respect to the nearest preceding rising edge of ICLK. While statistical analysis was performed to arrive at the "mean" value, the standard deviation, sample size(s) and other related information were omitted for brevity.

Table 4-1 Carrier Logic Timing

Parameter/Event	Minimum	Maximum	Mean
N_ACK assertion	10 ns	12 ns	10.5555 ns
N_ACK negation	9 ns	10 ns	9.2941 ns
IPDbus Earliest assertion	14 ns	17 ns	14.7857 ns
IPDbus Latest assertion	16 ns	19 ns	17.3570 ns
IPDbus Release (tristate)	10 ns	13 ns	10.7000 ns

Figure 4-2 presents, as a typical read transfer, an ID access from IPA = 0x03, where the IPDbus is being driven with 0x43, which corresponds to the header's C ASCII.

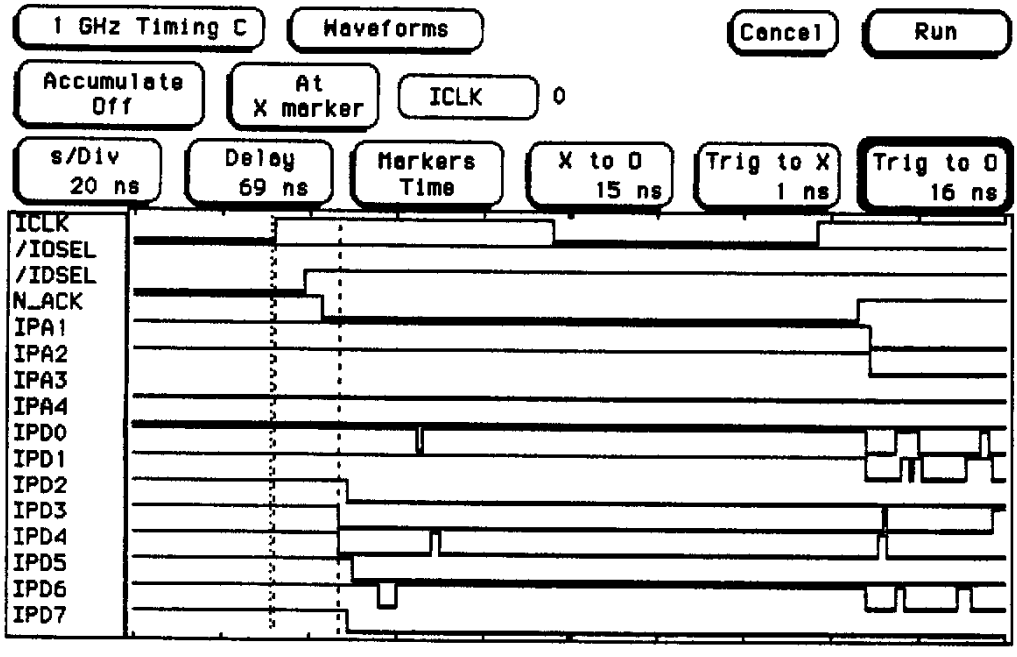


Figure 4-2 Typical ID Read

Inductive coupling and ringing due to the high capacitive cables being used is evident in this waveform. As is often the case for most carriers and IP Modules, the high impedance IPDbus often is driven low for 1 or 2 nanoseconds as it is being released. This is seen by the transitions from IP Module-driven high states during the access to a low state followed immediately by floating high (again) states following the transfer.

4.3 Data-Driven Output Changes

There are several methods for causing changes to take place on the output ports. The most common technique is by changing the actual I/O data values (as opposed to enabling and disabling the ports by hardware and software mechanisms). The timing for transitions on the outputs is highly dependent upon the loading applied to the outputs. Therefore, two sets of data are presented based upon applied loadings; one near the minimum loading as supplied by the on-board pull-up resistors only, and the other near the maximum loading.

It is important to note that these times are valid for the test configuration only. The capacitive loading of ribbon cables contribute significantly to the "turn ON" and "turn OFF" times, especially with long cables. Minimize this additional capacitance by using twisted pair and/or loose wiring instead of the flat-ribbon cables used for these tests. Reduce ringing by using series terminations near the OPTDO32's I/O connection point, and/or using parallel termination schemes near the application receiving circuitry.

In general, the light load resistances have faster turn ON times (defined as transitions from high states to low states) and slower turn OFF times (defined as transitions from low states to high states) than comparable transitions for heavy load (lower value) resistances. The maximum propagation delays cited in the specifications (Appendix A) are based upon the average values published by several sources of the opto-isolators. The "typical" delays presented in these sections include additional delay elements, as well as different loads than the ideal ones used to develop the specifications; hence, the difference in propagation delays.

4.3.1 Heavily-Loaded Timings

The system configuration, presented in Figure 4-1, was modified by the placement of thirteen 330 Ω resistors between the open-collector output connections at pins 1 through 8, and pins 12 through 16, and the system ground for a per-channel equivalent load resistance of 304 Ω. While the low-level output voltage varied based upon the number of outputs driven low, the average voltage resulted in a typical per-channel sink current of ≈12.6 mA. All four byte-lanes of the ports were powered from the same +5 volt supply (even though only two were used for this test), and all emitter connections were tied to the same carrier/system ground. The thirteen output connections correspond to port 0 bits 7 through 0, and port 1, bits 4 through 0, respectively.

The OPTDO32 under test was temporarily removed from its extender board and the capacitance of the terminal block, cabling, and the carrier's and extender's signal paths and connectors were analyzed for typical "load" capacitance. The average capacitance was ≈30 pF for all thirteen channels. Then the OPTDO32 was re-installed.

The power applied to the system measured +4.81 volts, and the fans were turned off to emulate conditions that might exist in a heavily loaded VME system. All of these conditions were used to attempt to perform these tests in a more realistic configuration for typical applications.

Table 4-2 presents measured turn ON and turn OFF delay times for various channel "bit" combinations. The data patterns selected ensured that all bits changed per test. Without exception, all table entries are measured in nanoseconds with respect to the nearest preceding rising edge of ICLK.

Table 4-2 Heavily-Loaded Delay Times

Data From #	To Data #	Earliest Turn Off	Latest Turn Off	Earliest Turn On	Latest Turn On
0x0000	0xFFFF	69	81	N/A	N/A
0xFFFF	0x0000	N/A	N/A	123	127
0x55AA	0xAA55	61	65	76	85
0xAA55	0x55AA	64	75	71	80
0x3C3C	0xC3C3	62	68	66	76
0xC3C3	0x3C3C	62	65	73	80
0x07FC	0x1803	64	66	72	91
0x1803	0x07FC	63	66	67	70

Figure 4-3 presents, as a typical I/O write transfer, the table entry for a write of '0xAA55,' with the "X to O" timing marker high-lighting the latest turn OFF time of 65 ns.

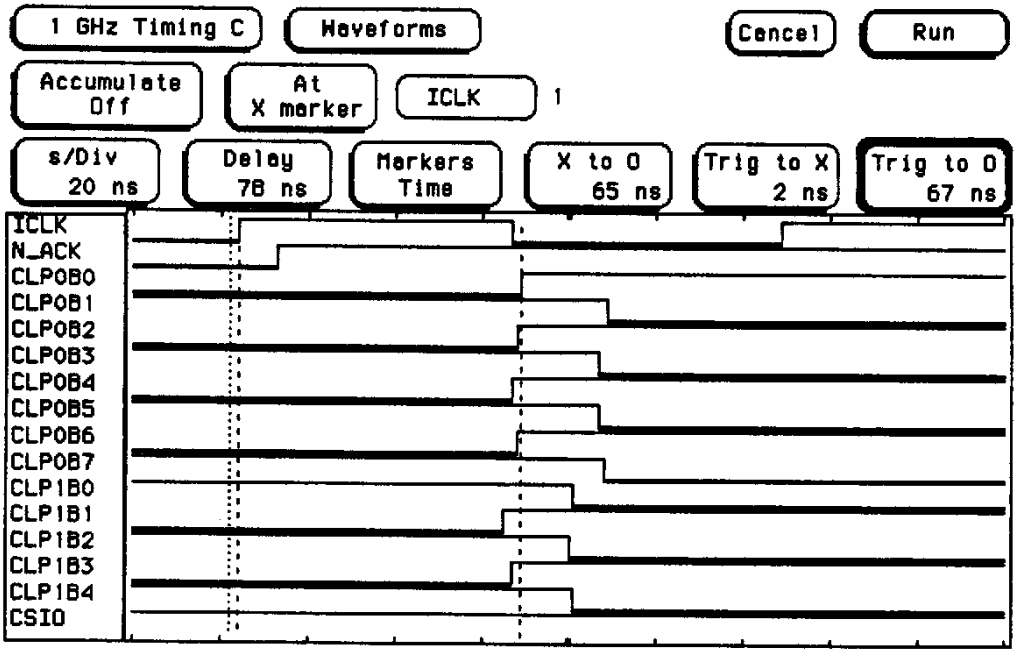


Figure 4-3 Typical Heavily-Loaded Output Delays

4.3.2 Lightly-Loaded Timings

The system configuration for these tests is identical to that presented in section 4.3.1 except that the thirteen (external) 330 Ω resistors were removed. This configuration left only the on-board 3.9 kΩ resistors as loads, with an average typical sink current of ≈1.2 mA. The much-weaker pull-ups have a significant effect on the output ports' transition delays in that they all turned OFF much slower. Table 4-3 presents the measured results for the same test sequence used in section 4.3.1.

Table 4-3 Lightly-Loaded Delay Times

Data From #	To Data #	Earliest Turn Off	Latest Turn Off	Earliest Turn On	Latest Turn On
0x0000	0xFFFF	91	117	N/A	N/A
0xFFFF	0x0000	N/A	N/A	70	89
0x55AA	0xAA55	173	180	66	85
0xAA55	0x55AA	170	304	66	71
0x3C3C	0xC3C3	158	191	63	72
0xC3C3	0x3C3C	159	166	65	83
0x07FC	0x1803	171	204	69	72
0x1803	0x07FC	96	158	64	81

Figure 4-4 presents the same transfer as presented in Figure 4-3 for a write of 0xAA55, with the "X to O" timing marker (again) high-lighting the latest turn OFF time of 180 ns.

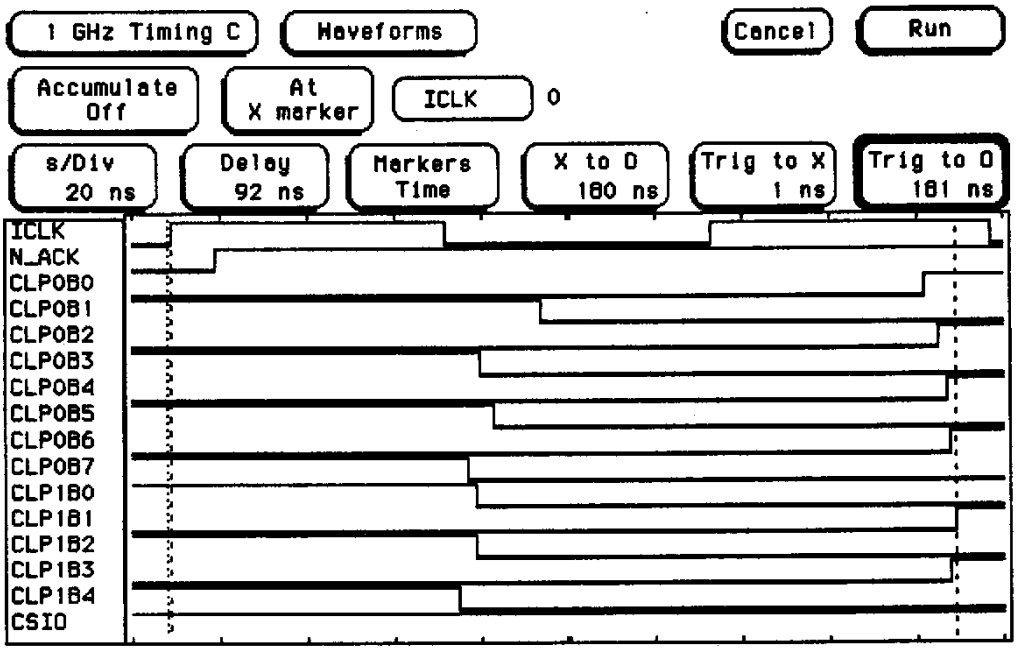


Figure 4-4 Typical Lightly-Loaded Output Delays

4.4 CSIO-Controlled Output Changes

While section 4.3 presented timing information concerning output changes controlled by software changes to the data registers, this section presents information about output changes as they are controlled by the hardware-handshake line CSIO, used as a control input.

The test configuration is similar to that used in section 4.3.2, with the addition of a TRIDO48 card in slot D on the carrier. Pin #8 of the TRIDO48's I/O connector was connected directly to pin #49 of the terminal block attached to the OPTDO32's I/O connector. This connects the TRIDO48's port 0 bit 0 directly to the CSIO line (input) to the OPTDO32. Writing '1's and '0's to address 0xFFF58300 on the MVME162 card drove the OPTDO32's CSIO line HIGH and LOW, respectively (for this test). This test only used the on-board 3.9 kΩ pull-up resistors as loads. Therefore the turn OFF times are slower, and the captured logic analyzer waveform(s) also depicted excessive ringing in the outputs (due to the light loading, improper cable terminations, and high capacitance on the outputs). Table 4-4 presents the measured results for both states of CSIO using both senses for control of the outputs, as described in the notes.

Table 4-4 CSIO-Controlled Output Changes

Time from CSIO going	PORT #?, Turning?	Earliest Time (ns)	Latest Time (ns)	Notes/Comments
HIGH	0, ON	76	89	Control Register = 0xA009 Port 0 enabled if CSIO = 1
HIGH	1, OFF	86*	92*	Port 1 disabled if CSIO = 1
LOW	0, OFF	118**	164**	Control Register = 0xA009 Port 0 disabled if CSIO = 0
LOW	1, ON	72	78	Port 1 enabled if CSIO = 0
LOW	0, ON	76	87	Control Register = 0xA006 Port 0 enabled if CSIO = 0
LOW	1, OFF	122**	130**	Port 1 disabled if CSIO = 0
HIGH	0, OFF	118**	166**	Control Register = 0xA006 Port 0 disabled if CSIO = 1
HIGH	1, ON	73	78	Port 1 enabled if CSIO = 1

* Not including ringing, first OFF ** Sustained, after ringing

The unbalanced table entries were developed so that an approximation could be developed for the turning OFF ringing time. This was accomplished by capturing (on Port 1) the first OFF event in one sampling and the sustained OFF (after ringing) in a different sampling. As a result, and for this test configuration, the ringing time ≈37 ns.

Figure 4-5 presents CSIO going high to turn ON port 0 and turn OFF port 1.

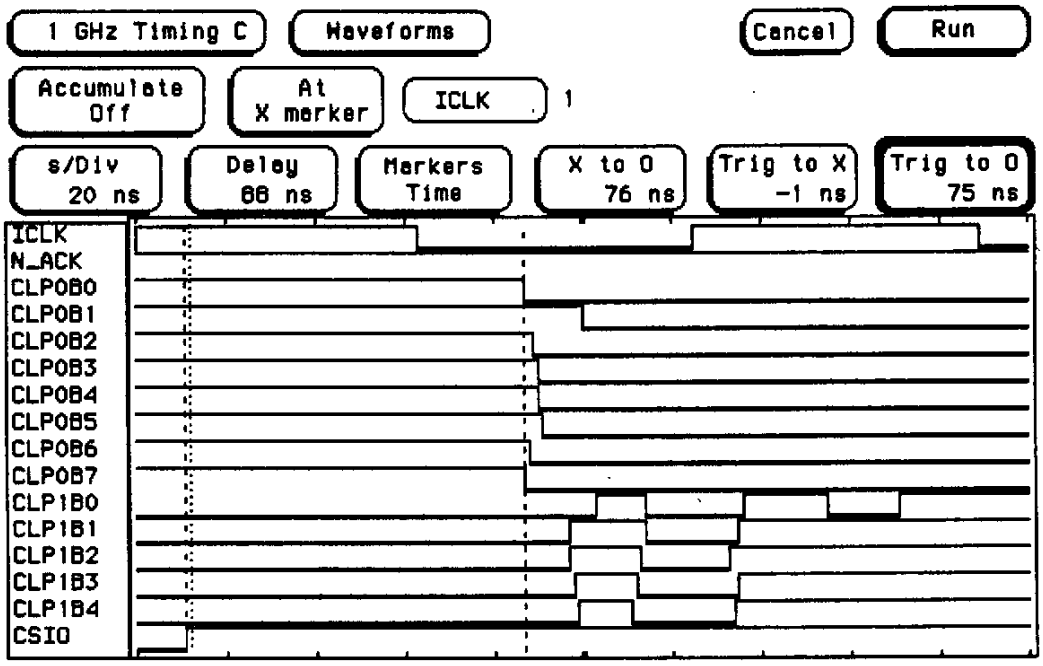


Figure 4-5 CSIO-Controlled Port-Enable/Disable Delays

4.5 CSIO as STATUS OUTPUT

This test was conducted immediately after those described in section 4.4. The sequence is significant in that it verifies what occurs when an application first uses CSIO as a control input, and then changes the mode so that it behaves as a status output signal. Paragraph 2.7.1 describes this process briefly. The actual process used to accomplish this follows:

The data contained within the control register at the end of the last section = '0xA009.' The '9' portion of this data enables Port 0 when CSIO is in a HIGH state (coming in) and enables Port 1 when CSIO is in a LOW state; either port 0 is enabled or port 1 is enabled, but not both (as in an open-collector bus application). When an attempted write to the control register of '0xB000' is made, the data returned from a subsequent read is actually '0xA000'. This is because when the attempt to set bit 12 was made, the data within the control register indicated that the CSIO was being used as an input; therefore, CSIO would not be allowed to be an output. The data of '00' in the low byte cleared the need for CSIO as an input since it disabled (via software) all the ports. A second write to the control port of '0xB000' was successful, as indicated by both a subsequent read of the control register, and by the fact that the CSIO line was driven to a steady-state LOW ('0') within 11 ns following the rising edge of ICLK at the end of the termination cycle.

There are three types of outputs that can now be selected with CSIO running in its "output" mode: constant low, constant high, or pulse on register updates. The first two states represent a single non-isolated "programmed-I/O" digital output. The pulse output, nominally a 125-ns high pulse output, can be used as a handshake line to signal receiving circuitry that a particular port has just been updated.

Figure 4-6 presents a typical pulse output on CSIO. First, the control register had '0x10FF' written into it to enable all of the port outputs and to configure the CSIO

operations to generate a pulse output whenever Port 0 is updated (written to). Then Port 0 was written to with '0xFF.'

CAUTION: Do NOT use CSIO as a latching signal since the transitions on the open-collector outputs vary widely with both the output loading and the cabling capacitance. The CSIO repeatedly started its pulse output within ≈ 8 ns of the rising edge of the ICLK at the end of the termination cycle, while the output ports' changes occurred anywhere from 61 ns to 304 ns, as presented in section 4.3.

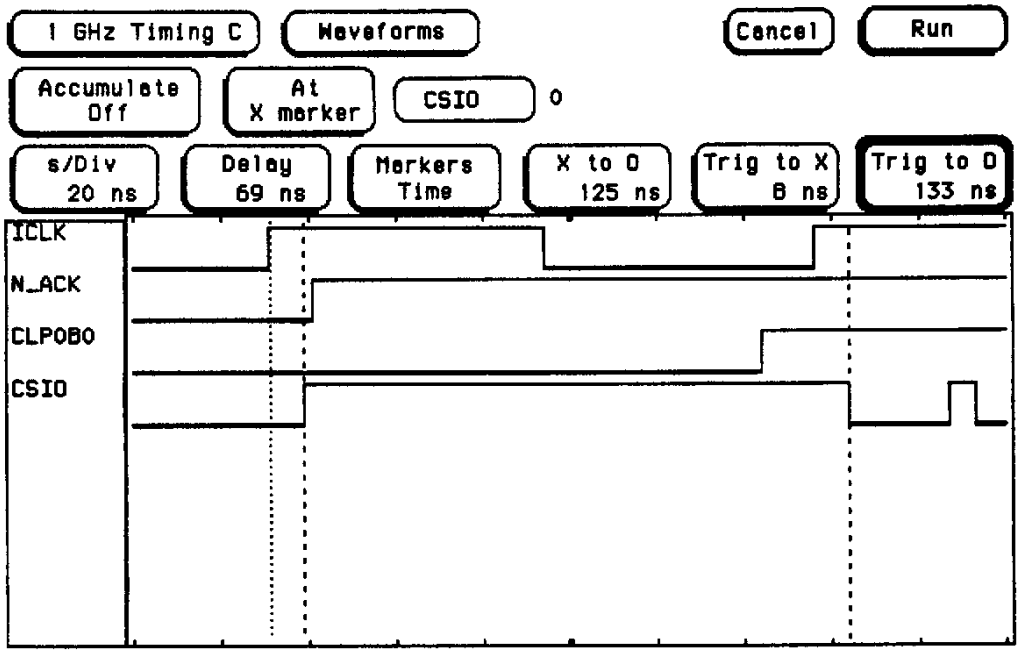


Figure 4-6 CSIO "pulse" Status Output Timing

Figure 4-7 presents one of two nearly identical "programmed-I/O" timing diagrams for CSIO. This particular function was executed by a write to the control register with the value of '0xF0FF.' This places CSIO in a steady-state HIGH 8 ns after the rising edge of ICLK during the cycle following the termination cycle (125 ns + 8 ns = 133 ns). A write of '0x90FF' to the control register resulted in identical timing for the placement of CSIO into a steady-state LOW.

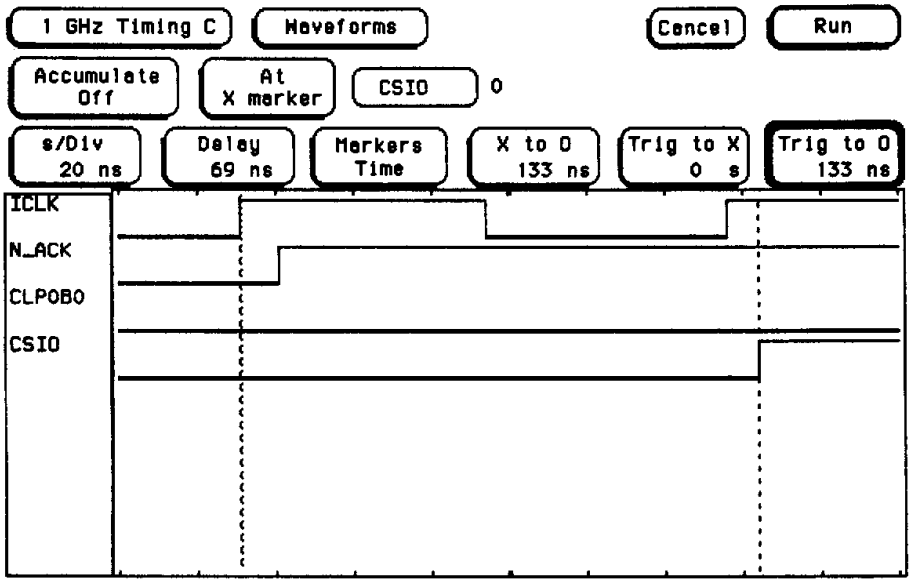


Figure 4-7 CSIO "HIGH" Status Output Timing

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APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements	1.800 inches x 3.900 inches x 0.303 inches (above board), 4.572 cm x 9.906 cm x 0.770 cm
Weight	1.2 oz., 33 grams
Board thickness	0.062 inches, 0.157 cm, nominally, (4 layer)

PROTOCOL

Clock rate	8 MHz
Wait cycles	None on any transfer types
Hold cycles	Supported on all valid transfer types
Address decoding	Complete (no partial)
I/O transfers	
Writes	8-bit or 16-bit
Reads	16-bit
registers	3 16-bit 2 data 1 control/status
Maximum read/write rate	4 Mtransfers/second, sustained
ID transfers	8-bit read (only) Zero-fill on upper byte 12 bytes, including CRC
Systran's manufacturer's ID	0x45, E ASCII
OPTDO32 model number	0x6C, 1 ASCII
CRC value	0x4F
Maximum read rate	4 MTransfers/second, sustained
Memory transfers	Not supported
Interrupt Vector transfers	Not supported
Interrupt requests	None generated
DMA activity	Not supported
Acknowledgment on unsupported transfer attempts:	
Memory read and write	None generated
Interrupt read	None generated
ID write	None generated
Addresses beyond those needed for valid transfers	None generated

POWER REQUIREMENTS

Carrier Power:	
(All channels OFF, no I/O connections)	+5 Vdc @ 133 mA (typical)
(All channels ON, no I/O connections)	+5 Vdc @ 314 mA (typical) ±12 Vdc@ 0 mA
I/O Power	
(All channels OFF, all ports powered)	+5 Vdc @ 111 mA (typical)
(All channels ON, all ports powered)	+5 Vdc @ 174 mA (typical)

(No external loads applied; values with on-board pull-ups only)

ABSOLUTE MAXIMUM RATINGS:

Carrier supply voltage
with respect to ground: .....-0.5 Vdc to +7.0 Vdc
I/O supply voltage "+5VP#"
with respect to "EMITT#":.....+7.0 Vdc maximum
"CSIO" input with respect to ground: .....-2.0 Vdc to +7.0 Vdc
"COLP#B#" per channel output current: ...16mA maximum

RECOMMENDED OPERATING CONDITIONS:

Carrier supply voltage
with respect to ground: .....+4.75 to +5.25 Vdc
I/O supply voltage "+5VP#"
with respect to "EMITT#":.....+4.5 to +5.5 Vdc
"COLP#B#" per channel
output current: .....1.2 mA minimum to 13 mA maximum
(1.2 mA minimum output current maintained by on-board, 3.9 kΩ pull-up resistor)
"CSIO" as input:
- Logic low voltage
with respect to ground: .....-0.3 to +0.8 Vdc
Maximum input current.....10 uA
Maximum input capacitance ....15 pF
- Logic high voltage
with respect to ground: .....+2.0 to Vcc + 0.3 Vdc
Maximum input current.....10 uA
Maximum input capacitance ....15 pF
- Risetime:.....40 ns maximum
- Falltime:.....40 ns maximum

"CSIO" as output:
- Logic low voltage
with respect to ground: .....+0.45 Vdc maximum @ 12 mA
- Logic high voltage
with respect to ground: .....+2.4 Vdc minimum @ -4 mA

"COLP#B#" output voltage: .....+0.23 to +0.4 Vdc typical, +0.6 Vdc maximum
(@ 13 mA load with "+5VP#" = +5.5 Vdc with respect to its associated "EMITT#")
Logic Interface .....ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): .....-40°C to +85°C
Temperature (no bias, storage):.....-55°C to +125°C
Humidity (Non-condensing): .....5% to 95%
Vibration (Operating): .....10 G's RMS, 20 to 2000Hz, random
Shock (Operating): .....50 G's maximum, all axes
Altitude (Operating):.....10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MIL-HDBK-217F .....448,646 hours
Bellcore 332, Issue 6 .....1,070,417 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

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APPENDIX B

TYPICAL APPLICATIONS

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B.1 Overview

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the OPTDO32 IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 Nomenclature

The following nomenclature is used in the application diagrams:

+5VP#	=	+5 volts for ports[3:0]
COLP#B#	=	COLP[3:0]B[7:0] where P = Ports 3 through 0, and B = Bits 7 through 0.
CSIO	=	Control/Status Input/Output line.
EMITT#	=	Common Emitter (ground) for ports 3 through 0.

B.3 Open-Collector Bus

Figure B-1 presents one of many system configurations that are possible using OPTDO32 IP Modules as open-collector data sources on a “custom” bus. Realistically, this open-collector communications bus would actually be implemented using multiple receive channels (only one is shown in Figure B-1). A centralized bus arbiter is depicted, where the TRIDO48 individually enables OPTDO32 boards to drive the bus for all of the receivers. This is accomplished by controlling OPTDO32 CSIO “inputs” with the TRIDO48, and configuring the OPTDO32 control registers with ‘0x55’ or ‘0xAA,’ depending upon whether the asserted CSIO line is to enable its associated OPTDO32 ports with a high level or a low level, respectively (low level is recommended). Due to the built-in 3.9 kΩ pull-up resistor per OPTDO32, and the current limitations it has for sinking current, typically only 10 to 12 OPTDO32 IP Modules can be placed on a single open-collector bus in this fashion.

The CSIO output from the TRIDO48 “controller” IP Module can be configured to generate a pulse output every time there is a change in the enabling operation on the bus to signal the receiver(s) that new data is now being driven onto the bus (by a different OPTDO32).

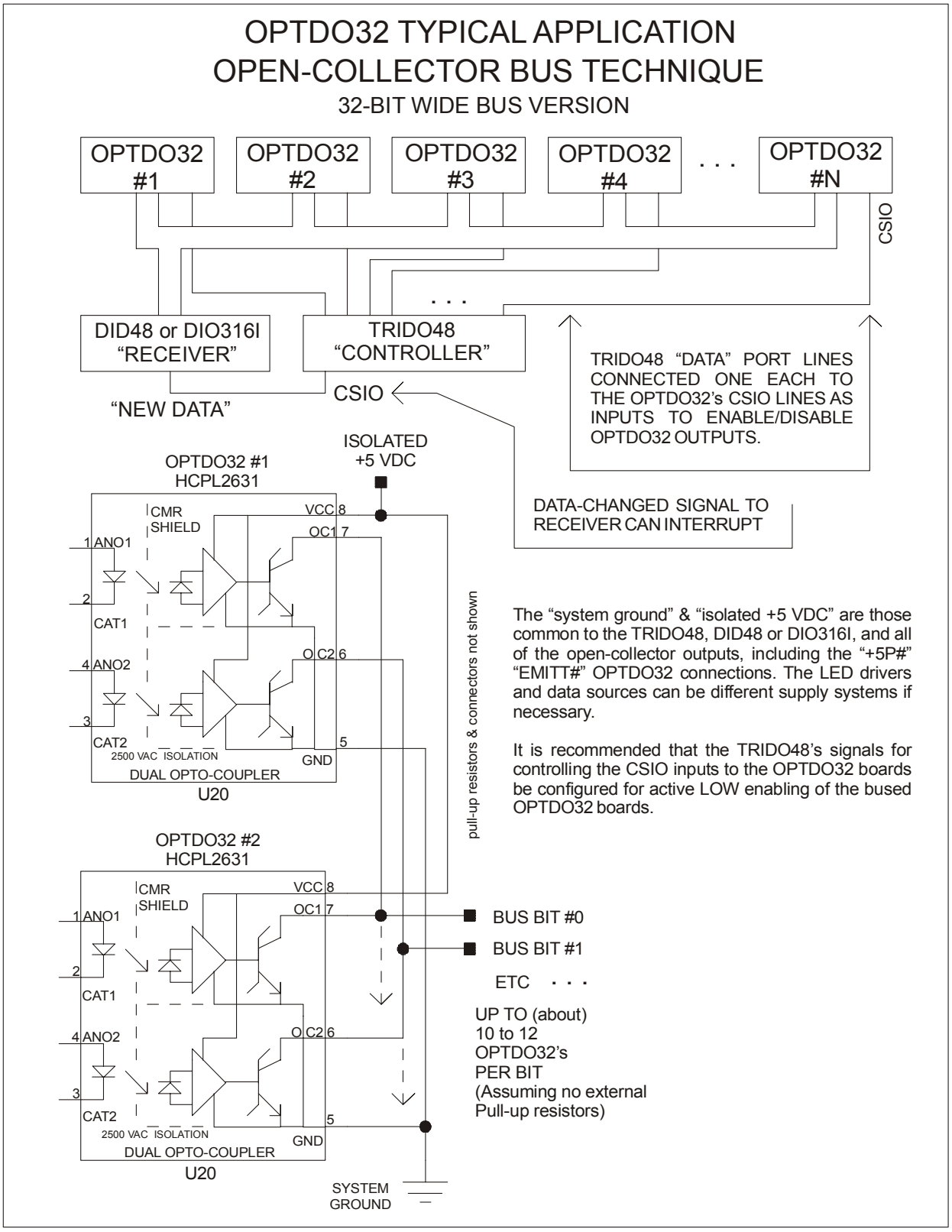


Figure B-1 Open-collector Bus Application

B.4 Isolated Grounds

There are many system applications that require distributed I/O implementations. When physical distances become great enough, system grounding can become a major problem. Losses in ground returns and, therefore, ground differences can be large enough to cause digital-to-digital communications to fail due to shifts in state-detection voltage values. Often these problems are circumvented by using differential transmitter/receiver pairs with sufficient common-mode rejection capabilities to overcome these voltage shifts.

Dangerous voltages can exist between two different “grounds” when they are developed from two different power transformers. If the secondaries are not “tied” to the same ground point, major (and perhaps, lethal) voltages can exist.

In many I/O systems, a “dirty” switcher-supply can generate a significant amount of noise that is coupled to the digital outputs, and therefore to the receivers' inputs.

For all of the above reasons, and many more, the OPTDO32 can be used to isolate systems in a digital communications application. Figure B-2 provides an overview of a system that is operating on five different power systems, with isolation good to several thousand volts, each.

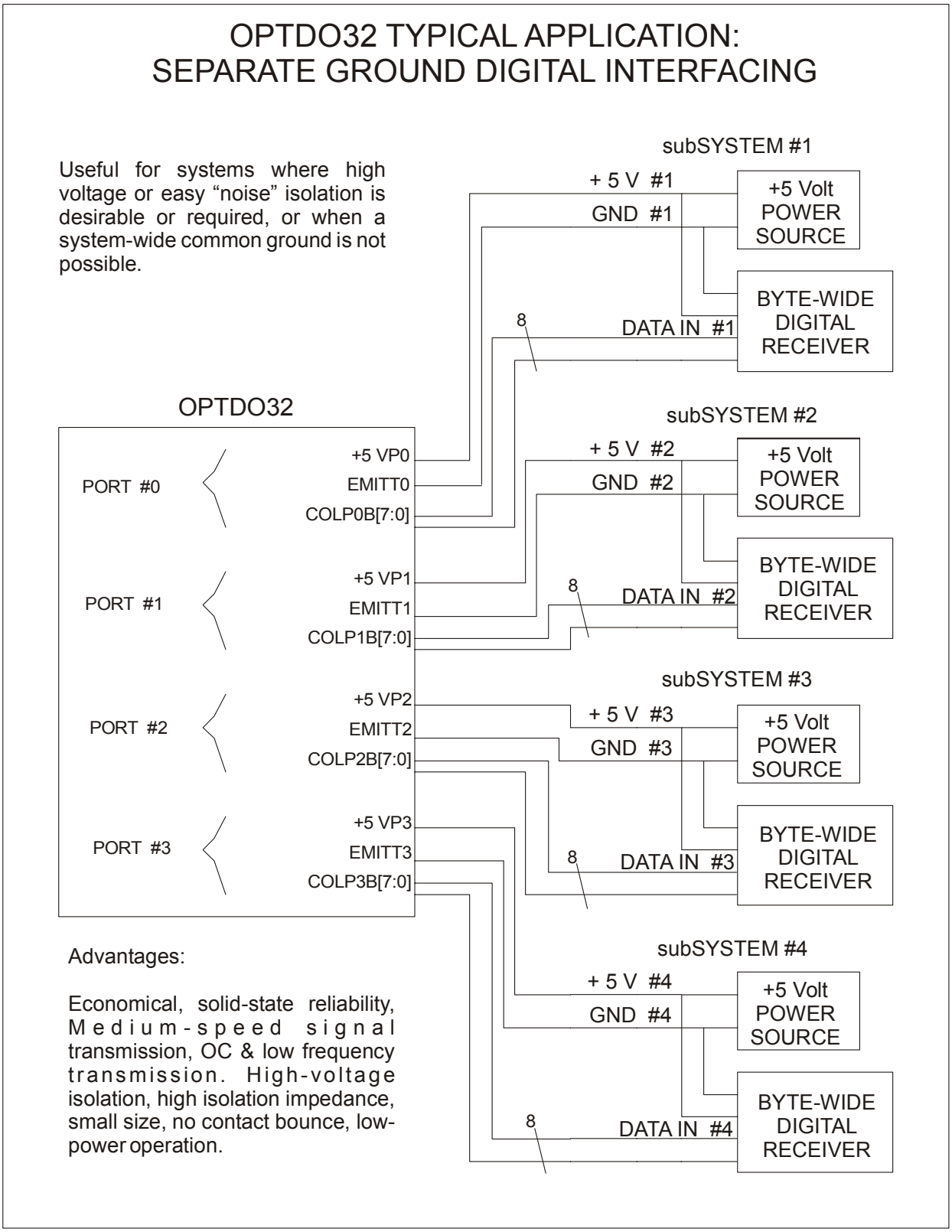


Figure B-2 Isolation Application

B.5 Isolated Analog Outputs

As with the isolated digital communications application presented in section B.4, analog sub-system performance can be significantly improved via isolation (if not for safety reasons, alone). Noisy digital systems can cripple high-resolution analog circuitry. Figure B-3 presents one technique for externally coupling high-resolution digital-to-analog converters to a digital system without coupling the noise. This technique is an absolute requirement in medical-sensing applications, although it is usually deployed in the reverse application of analog-to-digital conversion operations.

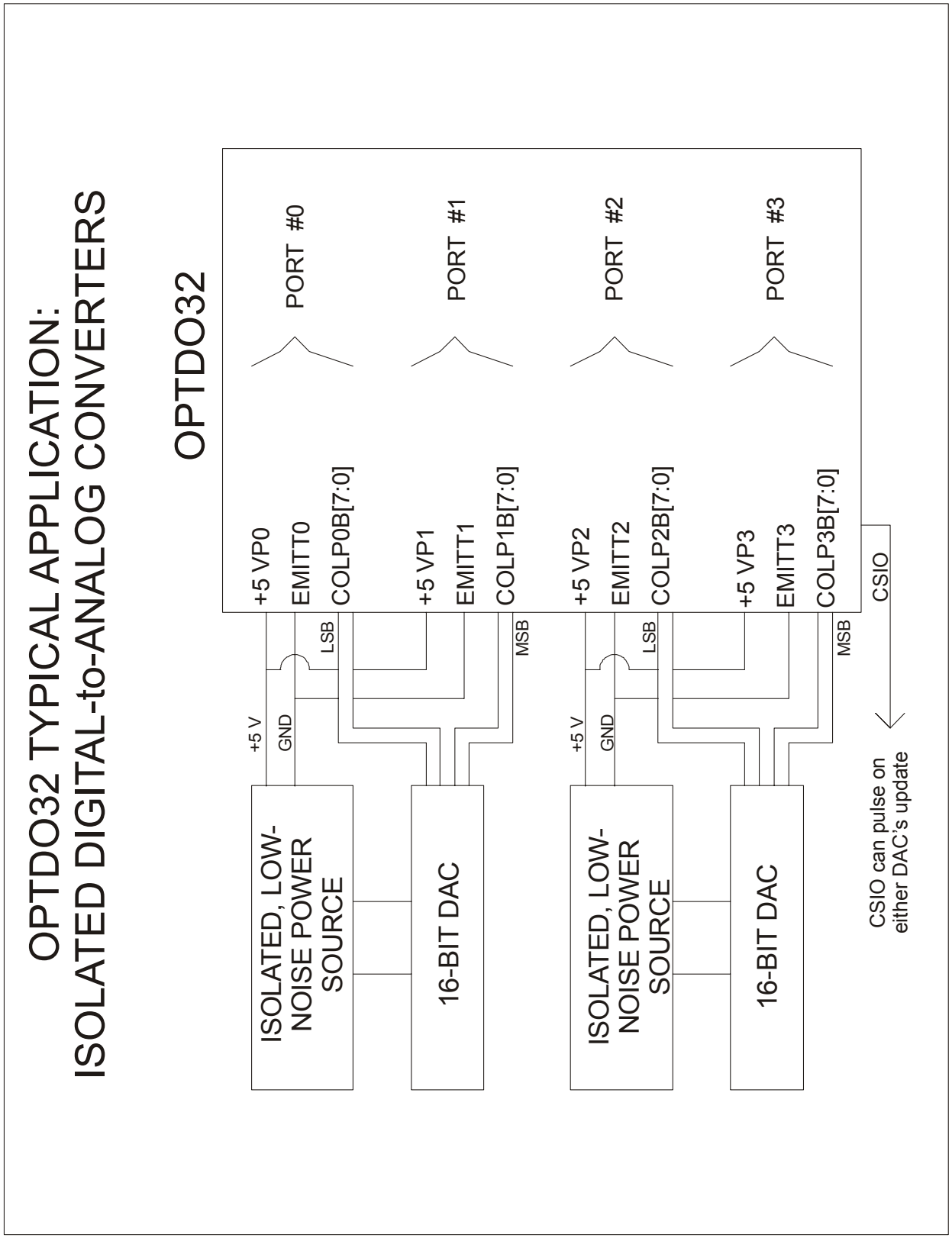


Figure B-3 Isolated Analog Outputs Application

APPENDIC C

PROGRAMMING GUIDE

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C.1 Overview

This section of the manual describes the operation of the OPTDO32 from the software perspective, detailing the OPTDO32 registers and providing programming examples. A more detailed description of the hardware can be found in Chapter 2, Product Overview, and in Appendix B: Typical Applications.

C.2 Description

The OPTDO32 is an opto-isolated, 32-channel, digital-output card. The output-enable can be either software controlled by user-selection on byte boundaries, or hardware controlled via the Control/Status Input/Output (CSIO) signal. If hardware output-enable control is used, the polarity of the CSIO input logic can be further selected. If the CSIO line is not used for output-enable control, it may be configured as an output signal that generates a 125-ns pulse when selected ports are updated. Also, the default output-enable power-up state is switch-selectable.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IP Module to provide "no-wait" read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) results in no acknowledgement, and its subsequent bus-timeout error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

The OPTDO32 emulated ID Address Space PROM listing is shown in Table C-1.

Table C-1 OPTDO32 ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII "I"	0x49
IPA = 0x01	ASCII "P"	0x50
IPA = 0x02	ASCII "A"	0x41
IPA = 0x03	ASCII "C"	0x43
IPA = 0x04	Systran's ID	0x45
IPA = 0x05	OPTDO32's Model Number	0x6C
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0x4F

C.4 IP Module I/O Address Map

The OPTDO32's I/O Address Map (Table C-2) was designed with efficiently located data and control registers in the IP Module I/O space (IPA = 0x00 through 0x02). There are a total of three 16-bit-wide I/O addresses decoded. The first two locations (IPA 0x00 through 0x01) are the data registers 0 and 1, and should be viewed as four 8-bit ports. Data register 0 contains ports 0 and 1 and data register 1 contains ports 2 and 3.

The next address (IPA 0x02) is the control register for the OPTDO32. This control register uses bits 15 through 12 and 7 through 0.

Table C-2 OPTDO32 I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	Data Port 1	Data Port 0	Data Register 0 = Ports 1 and 0, 8 bits each
IPA = 0x01	Data Port 3	Data Port 2	Data Register 1 = Ports 3 and 2, 8 bits each
IPA = 0x02	[15:12][XXXX]	[7:0]	Control Register 0 (CR0) output enables for ports 3 to 0, 8 bits [7:0], CSIO, 1 bit [12], CSIO pulse output configuration, 3 bits [15:13]

NOTE: [X] means not used

C.5 Power-up and System Reset Defaults

All of the data port's registers are cleared to zeros and bits CR[15:12] default to '0x0101' after power-up or system reset. Bits CR[7:0] default to the state of the DOES (default output-enable state) switch after power-up or system reset.

C.6 Word Access Address Translation

Table C-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, the word BASE represents the I/O or ID base address. All addresses are hexadecimal.

Table C-3 Word Access Address Translation Table

VMEbus Address	PC-AT Bus Address	NuBus Address	IP Module Address
BASE +0x00	BASE + 0x00	BASE + 0x02	IPA = 0x00
BASE + 0x02	BASE + 0x02	BASE + 0x06	IPA = 0x01
BASE + 0x04	BASE + 0x04	BASE + 0x0A	IPA = 0x02
BASE + 0x06	BASE + 0x06	BASE + 0x0E	IPA = 0x03
BASE + 0x08	BASE + 0x08	BASE + 0x12	IPA = 0x04
BASE + 0x0A	BASE + 0x0A	BASE + 0x16	IPA = 0x05
BASE + 0x0C	BASE + 0x0C	BASE + 0x1A	IPA = 0x06
BASE + 0x0E	BASE + 0x0E	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B

C.7 Byte Access Address Translation

Table C-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, the word BASE represents the I/O or ID* base address. All addresses are hexadecimal.

Table C-4 Byte Access Address Translation Table

VMEBus Address	PC-AT Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 0x01	BASE + 0x00	BASE + 0x3	IPA = 0x00	0
BASE + 0x00	BASE + 0x01	BASE + 0x2	IPA = 0x00	1
BASE + 0x03	BASE + 0x02	BASE + 0x7	IPA = 0x01	0
BASE + 0x02	BASE + 0x03	BASE + 0x6	IPA = 0x01	1
BASE + 0x05	BASE + 0x04	BASE + 0xB	IPA = 0x02	0
BASE + 0x04	BASE + 0x05	BASE + 0xA	IPA = 0x02	1
BASE + 0x07	BASE + 0x06	BASE + 0xF	IPA = 0x03	0
BASE + 0x06	BASE + 0x07	BASE + 0xE	IPA = 0x03	1
BASE + 0x09	BASE + 0x08	BASE + 0x13	IPA = 0x04	0
BASE + 0x08	BASE + 0x09	BASE + 0x12	IPA = 0x04	1
BASE + 0x0B	BASE + 0x0A	BASE + 0x17	IPA = 0x05	0
BASE + 0x0A	BASE + 0x0B	BASE + 0x16	IPA = 0x05	1
BASE + 0x0D	BASE + 0x0C	BASE + 0x1B	IPA = 0x06	0
BASE + 0x0C	BASE + 0x0D	BASE + 0x1A	IPA = 0x06	1
BASE + 0x0F	BASE + 0x0E	BASE + 0x1F	IPA = 0x07	0
BASE + 0x0E	BASE + 0x0F	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

* Byte-lane 1 is not applicable for ID Space

C.8 Register Definitions

The OPTDO32 has three 16-bit-wide registers: two data, and one general control. The data registers may be viewed as either two 16-bit registers or four 8-bit ports. The general control register allows user selection of output enable and port direction.

Table C-5 lists the registers and gives a short functional description of each. The registers are described in further detail in the following paragraphs.

The Read/Write (R/W) value in the definition table indicates access. “R” indicates read-only access, “W” indicates write-only access, and “RW” indicates both read and write access.

Table C-5 Register Descriptions

Register Name	Register Function	Page
Data Register 0	Data register for output ports 0 and 1	C-7
Data Register 1	Data register for output ports 2 and 3	C-7
Control Register	Selects output-enable control for the CSIO output pulse mode	C-8
	0E1 - 0E0: Output-enable Control Bits	C-8
	I/O: CSIO Input/Output Control Bit	C-8
	OP2 - OP0: CSIO Output Pulse Control Bits	C-9

C.9 Data Register 0 (IPA = 0x00)

This 16-bit read/write register is the data register consisting of the 8-bit-wide output ports 0 and 1. These two 8-bit ports can also be viewed as a single 16-bit register. When this register is written to, it sets the output value of the ports. When read, the register returns the current value of the ports. On power-up, all bits are set to '0'.

Table C-6 Data Register 0 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pn7 - Pn0 : Port n data bits 7 through 0.

C.10 Data Register 1 (IPA = 0x01)

This 16-bit read/write register is the data register consisting of the 8-bit-wide output ports 2 and 3. These two 8-bit ports can also be viewed as a single 16-bit register. When this register is written to, it sets the output value of the ports. When read, the register returns the current value of the ports. On power-up, all bits are set to '0'.

Table C-7 Data Register 1 Bit Description

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

C.11 Control Register (IPA = 0x02)

This 16-bit read/write register selects the output-enable control and the CSIO output pulse mode. The output-enable control can be selected on 8-bit port boundaries. The CSIO line can be used to generate a 125-ns output pulse when a port is updated. This option is available only if CSIO is not being used as an output-enable control gate. The power-up default state of the output-enable bits (OE1-OE0) take on the value of the DOES (default output-enable state) switch.

Table C-8 Control Register Bit Descriptions

Bit #	15	14	13	12	Bits 11 TO 8	7	6	5	4	3	2	1	0
Bit Name	OP2	OP1	OP0	I/O	Not used Read as 0's	P3 OE1	P3 OE0	P2 OE1	P2 OE0	P1 OE1	P1 OE0	P0 OE1	P0 OE0
R/W	RW	RW	RW	RW	Read as 0's Writes Discarded	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	1	0	1	0		DOES	DOES	DOES	DOES	DOES	DOES	DOES	DOES

DOES = Default Output-enable State

Table C-9 0E1 - 0E0: Output-enable Control Bits

OE1	OE0	Output-enable Selection
0	0	Outputs disabled (regardless of CSIO state; that is, software control)
0	1	Outputs enabled if CSIO is high, disabled if CSIO is low
1	0	Outputs enabled if CSIO is low, disabled if CSIO is high
1	1	Outputs enabled (regardless of CSIO state; that is, software control)

Table C-10 I/O: CSIO Input/Output Control bit

I/O	CSIO Input/Output Selection
0	CSIO is an input. It can be used as an output-enable control line.
1	CSIO is an output. This can be selected only if CSIO is not being used as an input for controlling the output enable of a port.

Table C-11 OP2 - OP0: CSIO Output Pulse Control bits

OP2	OP1	OP0	Output Pulse Mode Selection
0	0	0	CSIO pulse out on port 0 update (I/O bit, bit 12, must be high)
0	0	1	CSIO pulse out on port 1 update (I/O bit, bit 12, must be high)
0	1	0	CSIO pulse out on port 2 update (I/O bit, bit 12, must be high)
0	1	1	CSIO pulse out on port 3 update (I/O bit, bit 12, must be high)
1	0	0	CSIO output always low
1	0	1	CSIO output always low
1	1	0	CSIO pulse out on any register update (I/O bit, bit 12, must be high)
1	1	1	CSIO output high (I/O bit, bit 12, must be high)

C.12 OPTDO32 Programming Examples

The following examples illustrate how to program the OPTDO32 to achieve various operational modes.

C.12.1 Software Output-Enable Control Example

This example illustrates software output-enable control. This example uses only port 0; however, the programming concept is the same for all four ports.

- At power-up:
  - LSC switch is set HIGH for “true” logic.
  - The data registers are all cleared (value of ‘0x0000’).
  - Bits CR[15:12] are set to ‘0xA’.
  - Bits CR[7:0] are set corresponding to the DOES switch; ‘00' (LOW) for this example.
- Write ‘0xAA’ to port 0. The outputs will be ‘0xFF’ (HIGH) because the output for port 0 is not enabled.
- Write ‘0x0003’ to the Control Register (software enable). At this point the output of port 0 should be ‘0xAA’ because its output has been enabled.
- Write ‘0x0000’ to the Control Register (software disable). At this point the output of port 0 will be ‘0xFF’(HIGH) again because its output has been disabled.

C.12.2 Hardware Output-Enable Control Example

This example illustrates hardware output-enable control using the CSIO line as an output-enable control input. Only port 0 is used in this example; however, the programming concept is the same for all ports.

- At power-up:
  - LSC switch is set HIGH for "true" logic.
  - The data registers are all cleared (value of '0x0000').
  - Bits CR[15:12] are set to '0xA'.
  - Bits CR[7:0] are set corresponding to the DOES switch.
- Write '0x0002' to the Control Register.
- Write '0xAA' to port 0. At this point the output of port 0 will be '0xAA' if the CSIO input is LOW and '0xFF' if the CSIO input is HIGH.
- Write '0x0001' to the Control Register. At this point the output of port 0 will be 'FF' if the CSIO input is LOW and '0xAA' if the CSIO input is HIGH.
- Write '0x0000' to the Control Register. At this point the outputs will be '0xFF' because all outputs are disabled.

C.12.3 CSIO Output Pulse Example

This example illustrates how to program the OPTDO32 to generate 125-ns output pulses on the CSIO multi-function pin.

- At power-up:
  - The data registers are all cleared (value of '0x0000').
  - Bits CR[15:12] are set to '0xA'.
  - Bits CR[7:0] are set corresponding to the DOES switch.
- Write '0x1000' to the Control Register. At this point the OPTDO32 will generate a 125-ns pulse when port 0 is written to.
- Write '0xD000' to the Control Register. At this point the OPTDO32 will generate a 125-ns pulse when any register is written to.
- Write '0xF000' to the Control Register. At this point the CSIO output of the OPTDO32 is set to HIGH.

GLOSSARY

ATE ----------Automatic Test Equipment.

byte ----------8 bits.

byte-lane ----------8 bits of a data bus on octal boundaries.

CAE----------Computer Aided Engineering.

CASE----------Computer Aided Software Engineering.

CRC----------Cyclic Redundancy Check.

DOES----------Default Output-Enable States.

CSIO----------Control/Status Input/Output Line.

doublewide ----------An IP Module that is twice the size of a singlewide IP Module.

DMA ----------Direct Memory Access.

EPLD ----------Erasable Programmable Logic Device.

ESD ----------Electrostatic Sensitive Device.

GND ----------Ground.

ID PROM----------The circuitry that presents the proper data patterns to the low 8 bits of the IPDbus during the ID (read) transfers.

IP Module----------Credit-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O----------Input/Output.

IP Module logic bus ----------A synchronous, 4M transfers/sec, 16-bit or 32-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6 bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 M words of memory space per IP Module.

IPDbus ----------IP Module Data Bus.

LED----------Light-Emitting Diode.

LSC ----------Logic Sense Control.

MTBF ----------Mean Time Between Failures.

ns, µs, ms ----------Nanoseconds, microseconds, and milliseconds respectively.

Opto-coupler ----------See Opto-isolator.

Opto-isolator ----------A coupling device in which a light-emitting diode, energized by the input signal, is optically coupled to a photo detector such as a light-sensitive output diode, transistor, or silicon-controlled rectifier. Also known as optical coupler, optical isolator, optically-coupled isolator, opto-coupler, opto-electronic isolator, photo-coupler, and photo isolator.

PC ----------Personal Computer.

QSOP----------Quarter-sized Small Outline Packages.

singlewide ----------An IP Module printed circuit board (3.9 inches by 1.8 inches). Each module has two 50-pin connectors.

VHDL ----------Very high-speed integrated circuit Hardware Description Language.

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