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TESTIP

IPack Carrier
Performance Tester
User Manual

Document Nr. B-T-MU-TESTIP##-A-0-A1

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GLOSSARY

[x:y]. Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte. 8 bits.

byte-lane. 8 bits of a data bus on octal boundaries.

CAE. Computer Aided Engineering.

doublewide. An IPack module that is twice the size of a standard IndustryPack module.

EPLD. Erasable Programmable Logic Device.

ID PROM. The circuitry that presents the proper data patterns to the low 8 bits of the IPDbus during the ID (read) transfers.

IndustryPack. Credit-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O. Input/Output.

IPack. Refers to the IndustryPack standard.

IPack logic bus. A synchronous, 4 M transfers/sec, 16- or 32-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6 bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 M words of memory space per IPack module.

IPDbus. IPack Data Bus.

MTBF. Mean Time Between Failures.

ns, µs, ms Nanoseconds, microseconds, and milliseconds respectively.

PC. Personal Computer.

QSOP. Quarter-sized Small Outline Packages.

singlewide. An IPack printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL. Very high speed integrated circuit Hardware Description Language.

1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for SYSTRAN's IndustryPack (IPack) Carrier performance tester, referred to as the TESTIP, part number BHAS-TESTIP. Figure 1-1 is a picture of the TESTIP board.

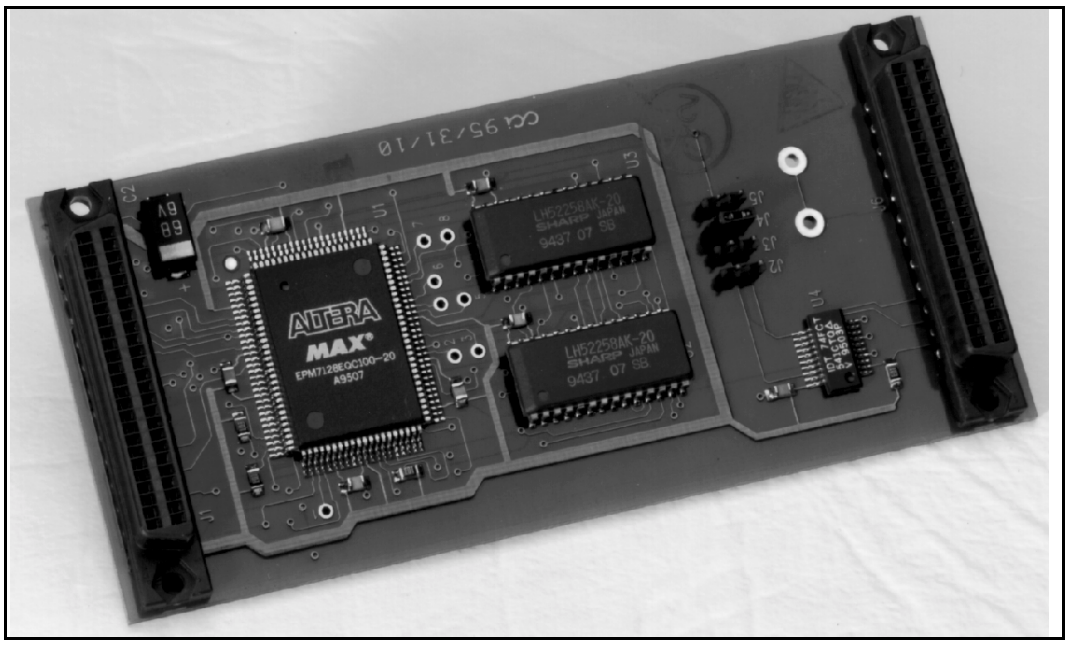


Figure 1-1 **TESTIP Board**

1.2 Scope

This reference manual covers the physical and operational description of the TESTIP, both from hardware and software perspectives. This manual also contains detailed technical information about the TESTIP's performance characteristics, and a few typical applications. It is assumed that the reader has a general understanding of computer processing, hardware and/or software applications experience, and a working knowledge of using IPacks on their carrier(s) of choice. The TESTIP is designed to enhance this carrier performance knowledge base. Citation of equipment from other vendors within this document does not constitute an endorsement of their products.

1.3 Overview

The TESTIP is a singlewide IPack board, conforming both mechanically and electrically to the *IndustryPack Logic Interface Specification Revision 0.7.1*. It can be used singly, or in combination with other TESTIP's to assist in the verification of both functional and performance characteristics of ALL IPack carriers. It can also be used as an operational IPack in systems needing powerful interrupt support, a system-wide time-synchronization scheme, a high-performance timer, a variable-width, software-programmable pulse generator, or additional READ/WRITE (up to 111) “memory” locations for various applications.

1.4 Features

- 22 “memory-transfer” READ/WRITE 16-bit locations over full 8 MByte range
- 57 “I/O-transfer” READ/WRITE 16-bit locations
- 32 “ID-transfer” READ/WRITE 16-bit locations
- 20 “Address-in-Address” READ locations in “ID” range
- 1-of-8 board number identification switches
- Software-controllable 16-bit 1 MHz (READ-on-the-fly) timer
- “N_ERROR” signal generator
- “N_STROBE” status monitor
- Two levels of local interrupt generation support
- System-wide “global” interrupt generation/reception support
- Zero, or pseudo-random 0→7 “wait” cycle insertion generator
- Supports “hold” cycles on all valid transfers

1.5 Specifications

MECHANICAL: Singlewide IPack

- Measurements: 1.800″ x 3.900″ x 0.303″ (above board),
  4.572 x 9.906 x 0.770 cm
- Weight: 0.894 oz., 25.34 grams
- Board thickness: 0.062″, 0.157 cm, nominally, (4 layers)

PROTOCOL: Overall

- Specification Revision = 0.7.1
- Singlewide IPack transfers
- 8 MHz only; no 32 MHz operations
- No “wait” cycles on any transfer types, normally
- Optionally insert 0→7 “wait” cycles on all transfer types, randomly
- Supports carrier-asserted “hold” cycles
- Complete (no partial) address decoding

- No acknowledgement for unsupported transfer types and addresses:
  - Interrupt WRITEs
  - DMA activity (all forms)
  - 4,194,282 of 4,194,304 possible memory “word” locations
- Maximum READ and WRITE transfer rate:
  - 4 MTransfers/second, sustained
- Minimum READ and WRITE transfer rate:
  - 889 KTransfers/second, 7 wait cycles inserted per transfer

PROTOCOL: ID TRANSFERS

- READ 16-bit (byte-lanes ignored) from IPA = 00 → 1F *hex*
  Upper byte (IPD[15:8]) zero-filled
  WRITEs acknowledged with no data changes
- WRITE to and READ from last 32 locations, IPA = 20 → 3F *hex*
  Low byte, high byte, and full-word READs and WRITEs

PROTOCOL: INTERRUPT TRANSFERS

- READ 16-bit (byte-lanes ignored) from IPA = 00 and 01 *hex*
  Upper byte (IPD[15:8]) zero-filled

PROTOCOL: I/O TRANSFERS

- WRITE to and READ from first 57 locations, IPA = 00 → 38 *hex*
  Low byte, high byte, and full-word READs and WRITEs
- READ (on-the-fly) 16-bit (byte-lanes ignored), 1 MHz timer from IPA = 39 *hex*
  WRITE (any data, any width) to reset timer value to ‘0000’
- READ (any width) to stop timer from IPA = 3A *hex* (pseudo-register)
  WRITE (any data, any width) to start timer
- READ 16-bit (byte-lanes ignored) from IPA = 3B → 3F *hex*
  Low byte, and full-word WRITEs
  Unused bits zero-filled:
  IPA = 3B: IPD[15:3]
  IPA = 3C: IPD[15:2]
  IPA = 3D: IPD[15:3]
  IPA = 3E: IPD[15:8]
  IPA = 3F: IPD[15:8]

PROTOCOL: MEMORY TRANSFERS

- Low byte, high byte, and full-word READs and WRITEs
- Only valid addresses defined as a single asserted '1' address line with 21 negated ‘0’ address lines in the field:

  IPD[15:0] ⇒ IPA[22:7] (extended memory address during “select” cycle)
  IPA[6:1] (IPD[15] ⇒ IPA[22] ≡ most significant address bit)

POWER REQUIREMENTS:

- Power: +5 Vdc @ 220 mA (typical, no I/O loads)

±12 Vdc @ 0 mA

- Electrical characteristics: Refer to Section 5.0 PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

- Supply voltage with respect to ground: -0.5Vdc min., +7.0Vdc max.

RECOMMENDED SUPPLY RATINGS:

- Supply voltage with respect to ground: +4.75Vdc → +5.25Vdc

LOGIC INTERFACE:

- IndustryPack specification-compliant carrier

I/O INTERFACE:

- I/O input voltage: ground → supply voltage

  Input current = 5 μA maximum, 2 nA typical (for inputs ground → supply voltage)
  = -320 mA maximum @ -2.5 volts input (heavy negative clamping); must be externally limited to ≤ 20 mA

  Low voltage = 0.8 volts maximum, negative clamp starts @ -1.0 volts

  High voltage = 2.0 volts minimum

  Rise/Fall times: No limit as long as the input is continually rising or falling (no more than 200 mVolts of hysteresis) through the logic threshold region of 0.8 volts → 2.0 volts.

- I/O output voltage:

  Low voltage = 0.55 volts maximum @ 64 mA loading

  High voltage = 2.4 volts minimum @ 15 mA loading

  Short Circuit Current = -60 mA minimum, -225 mA maximum
  No more than one output shorted at a time for ≤ 1 sec.

  No positive clamp: Can power down without disconnecting and de-energizing loads

ENVIRONMENTAL SPECIFICATIONS:

- Temperature: (Operating): -15°C → +85°C
  (Storage): -65°C → +150°C
- Humidity (Noncondensing): 5% → 95%
- Vibration (Operating): 10 G's RMS, 20 Hz→2 KHz, random
- Shock (Operating): 50 G's maximum, all axes
- Altitude (Operating): 10,000 feet maximum

MEAN TIME BETWEEN FAILUREs (MTBF):

- 4,409,171 hours per MIL-HDBK-217F

1.6 Related Products

- Software: 'C' library and OS-9® device driver routines with documentation.

- ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

1.7 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp. (Doc number: B-T-SH-IPACKSUM-A-0-A2 Rev. 7/15/94)
- *IndustryPack Logic Interface Specification Revision 0.7.1* published by GreenSpring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.8 Ordering Process

If you wish to learn more aboutr SYSTRAN products or to place an order, the following contacts are available:

- Phone: **(513) 252-5601**
- E-Mail address: **info@systran.com**
- World Wide Web address: **http://www.systran.com/**

1.9 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes and distributes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct any programming questions, any concerns about the functional-fit of this product for your particular application, or any questions not answered satisfactorily by this document, to the factory at **(513)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance.

Refer to Section 7.0 for warranty and repair information.

1.10 Reliability

SYSTRAN Corporate policy is to provide the highest-quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

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- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

SYSTRAN provides products and services that meet or exceed the best expectations of our customers.

- All products are tested using an Automatic Test Equipment system, with samplings for all product types taken through extended testing scenarios that include stress testing for voltage and temperature ranges beyond specifications.
- All products receive a predictive reliability rating based upon a calculated MTBF utilizing the MIL-HDBK-217F. Field failures are continuously logged and evaluated for potential failure modes and trends.
- Other environmental parameters are guaranteed by design, and not tested.
- Design reliability is ensured by methodology (top-down CAE design, VHDL, synthesis, extensive all-cases simulation, ALPHA build and test, and BETA testing if required) with full concurrent engineering practices throughout.

2.0 DESCRIPTION

2.1 Overview

The purpose of the TESTIP is to provide a wide variety of READ and WRITE access capabilities for exercising and testing any and all IPack carriers in their various modes of operation. With the exception of 32 MHz and DMA operations (which are not yet well defined), the TESTIP provides all of the transfer variations that are possible under the *IndustryPack Logic Interface Specification, Revision 0.7.1*, including a non-rule recommendation, and other features and functions to facilitate the determination of the performance characteristics for various carriers under test. The generic nature and versatility of the TESTIP, along with 111 word-width WRITE/READ-BACK locations, makes it ideal for performing general-purpose I/O support functions when not being used for carrier testing purposes.

2.1.1 I/O Transfers

All of the available I/O addressing space is utilized on the TESTIP. The first 57 word-width locations, consisting of addresses defined as IPA = ‘00’ → ‘38’ *hex*, are WRITE/READ-BACK “registers” that execute storage in and out of a small portion of a 32 KWord SRAM. The last seven I/O locations, consisting of addresses defined as IPA = '39' → '3F' *hex*, are EPLD-based control and status registers for various support features provided by the TESTIP.

2.1.2 ID Transfers

All of the available ID space is utilized on the TESTIP. The first 12, READ-only, locations are the standard fixed identification fields that provide system configuration information, like all other IPacks. The next 20 ID locations, consisting of addresses defined as IPA = ‘0C’ → ‘1F’ *hex*, provide READ-only accesses of information that provide “address-in-address” data, and switch data defining the “board number” for multiple-TESTIP carrier testing. The last 32 locations in the ID space are word-width WRITE/READ-BACK “registers” that operate in and out of a small portion of the 32 KWord SRAM.

2.1.3 Memory Transfers

Since the full-memory map for a singlewide IPack includes 8 MBytes of data, memory transfers are limited in scope to just 22 unique locations—one for each significant address line over the full addressing range. As with the 57 I/O and 32 ID SRAM-based accesses, these 22 MEMORY locations are word-width WRITE/READ-BACK "registers" that complete transfers using a small portion of the 32 KWord SRAM. The only "illegal" transfers that exist for the TESTIP are those for "memory" addresses not specifically encoded for this support.

2.1.4 Interrupt Transfer

The last transfer type of the TESTIP is interrupt support. These features include local and global, software and hardware interrupt generation capabilities (global for ganging boards together), as well as provisions for supplying distinctive interrupt vectors.

2.1.5 Auxiliary Functions

Several auxiliary functions are also included on the TESTIP to further facilitate the testing of various IPack carriers, both for functional and performance purposes:

- A 16-bit, 1 MHz performance counter that can easily be used to ascertain the bandwidth (rate) capacity of any carrier under test for any kind of single or combination of transfer types.
- The ability to insert a random number of (up to seven) wait states.
- The ability to drive the "N_ERROR" line, via software, for testing the carrier's ability to sense and respond to its assertion.
- The TESTIP also provides a software path for monitoring the "N_STROBE" input line from the logic connector for those carriers that provide connection capabilities to this IPack function.

2.1.6 Exceptions

- This IPack is designed to the *IndustryPack Logic Interface Specification Revision 0.7.1*, and therefore does not support DMA or 32 MHz transfers, since these were not defined at this specification level.
- The TESTIP will not respond with an acknowledgement for any memory transfer at addresses not directly defined in its architecture. This will result in a bus time-out event for the carrier's host system.

2.2 Block Diagram Description

Figure 2-1 presents a block diagram for the TESTIP. In the upper left corner of the block diagram are the IPack Logic Bus connections to the IPAbus, the IPDbus, and various (undefined) IPack control signals, through which all transfers between the IPack carrier and the TESTIP's registers and data sources/destinations are conducted.

In the bottom right corner of the block diagram are the IPack I/O connections. There are only three signals, two for interrupts and one indicating the status of the performance counter. Although not shown, these three signals are buffered coming and going. In the upper right corner of the block diagram are a pair of 32 KB SRAM devices that perform WRITE/READ-BACK registration of data for all Memory Transfers, half of the ID Transfers, and 89% of the I/O transfers. The remaining circuitry depicted is housed in a single EPLD device. Not shown are power-filtering

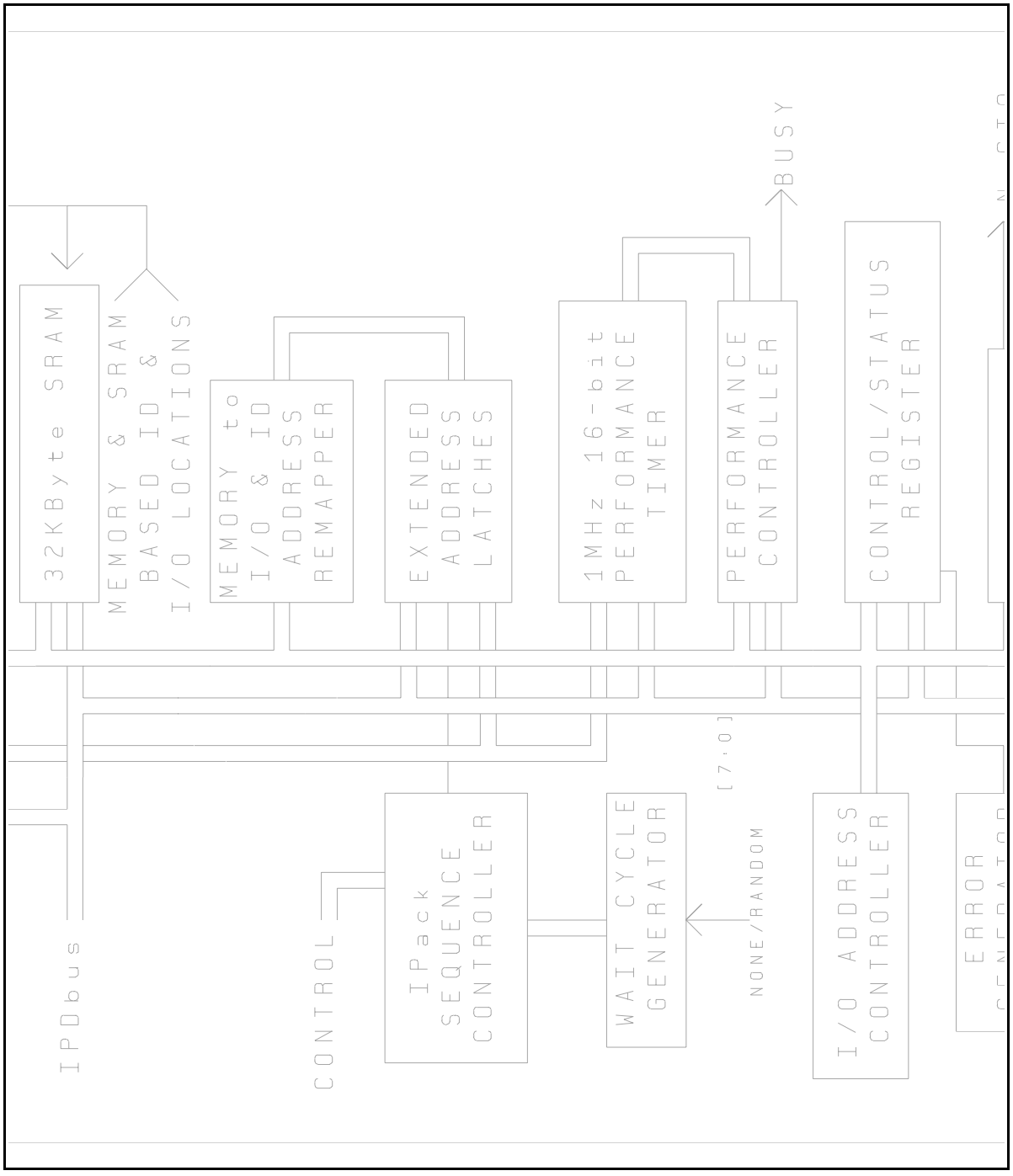


Figure 2-2 **TESTIP Block Diagram**

and by-pass circuits, and a triple jumper switch that appears as a portion of the ID information that presents the board's slot position information on a carrier.

2.2.1 IPack Sequence Controller

This block provides all of the circuitry with responsibilities for: detection of valid I/O, ID, Memory, or Interrupt Vector transfer operations within their respective fully- decoded address ranges; development of internal and external sequence-control signals for each of the supported transfer types, including those for the external 32 KWord SRAM; proper termination cycle sequencing based upon the state of the wait-cycle generator; IPDbus READ-data source multiplexing and tristate gate control for all valid READ transfer operations; and, proper WRITE data capturing and termination cycle sequencing based upon the carrier's "HOLD" cycle insertions, when executed.

2.2.2 Wait Cycle Generator

This block provides all of the circuitry required for implementing a pseudo-random wait-cycle insertion scheme for those carriers needing this test function. It is a 3-bit counter that is normally held at a count of zero unless it is enabled by its control bit. When enabled, it free-runs at the ICLK rate of 8 MHz. The TESTIP will only assert N_ACK when this counter's value is equal to zero. The randomness is due to the indeterminant nature of application software's accesses to and from the TESTIP, and to the variety of different carriers' access techniques and timings.

2.2.3 I/O Address Controller

The primary operations of the logic encompassed by this block include the sectoring of the I/O accesses between SRAM reads and WRITEs, versus accesses to and from the control registers found at the top of the I/O address map, and handled by logic within the TSTCTRL EPLD. Outputs from this logic support the SRAM access-control signal generation logic contained within the IPack Sequence Controller (described above) and the SRAM-address-remapper logic. The first 57 I/O locations (IPA = 00 $\rightarrow$ 38 *hex*) are address- and access-mapped to the low end of the SRAM. The remaining top seven I/O locations (IPA = 39 $\rightarrow$ 3F *hex*) are contained as logic within the TSTCTRL EPLD.

2.2.4 Error Generator

This is a single-bit control/status register that is a subset of the control/status registers within the EPLD. Its function is to allow the application test software to assert and negate the TESTIP's N_ERROR signal for verifying a carrier's ability to post this status, if supported.

2.2.5 Non-Zero IRQ Vector Detectors

This is a pair of 8-bit, zero-value detectors that independently monitor the two top I/O locations where the interrupt vectors for both levels are located. The outputs from these detectors are used by the interrupt engine to block interrupt events. If an interrupt vector is equal to zero (power-up default condition) then this logic will block any attempts to enable and/or execute its respective interrupt request to the carrier. These detectors were installed as a safety measure for systems that have multiple-TESTIP boards that may receive global-interrupt-request inputs prior to the proper initialization of valid interrupt vectors for subsequent Interrupt Service Routine (ISR) support.

2.2.6 ID PROM Emulator

This is a subset of the IPDbus read-data source multiplexing function identified under the IPack Sequence Controller (above). For ID transfers, this logic presents fixed data in the low byte for the first twelve locations that corresponds to the unique information about the TESTIP for system-level configuration purposes. The next twenty ID locations present an “A-in-A” (Address in Address) data field in the lower five data-bit locations (IPD[4:0] ⇐ IPA[5:1]), while the upper three data bits in the lower byte present the board number selected for this particular TESTIP as determined by the three board number jumpers (IPD[7:5] ⇐ BRDN[2:0]). The upper byte READs as all zeroes for all of the lower half, READ-only ID locations. The remaining 32 ID locations are READ/WRITE accessible from/to unique SRAM locations.

2.2.7 Control/Status Registers

These are the locations at the top of the I/O address map that control the functionality and post the status of the TESTIP. These register functions include four locations for interrupt support, a single location for general purpose support, and two locations that provide performance counter support.

PERFORMANCE CONTROLLER

This is the logic that controls the starting, stopping, reading, and resetting of the 16-bit performance counter. It also includes a 3-bit prescalar counter that divides the ICLK down to the frequency required to provide 1 μs resolution required for the counter. And finally, this logic also provides the “BUSY” signal drive that indicates that the counter is running.

1 MHZ 16-BIT PERFORMANCE TIMER

This function consists of a fully synchronous 16-bit counter implemented with two 8-bit counting blocks with a full-look-ahead carry connecting the two groups. Since this counter is incremented by ICLK, full on-the-fly READs are possible without additional latching of the counter contents. There is no terminal count detection and/or stop logic, with rollover counting being feasible.

Interrupt Engine

This logic consists of the functions required to generate two separate interrupt requests to the carrier, using local- and global-request mechanisms. Two of the control/status registers are directly used, along with the interrupt vectors’ non-zero detection logic, to generate and service interrupt requests, as needed.

2.2.8 Extended Address Latches

This logic is necessary for the capturing of the extended address bus (IPA[22:7]) presented by IPD[15:0] during the select cycle for memory transfers. Instead of actually using 16 registers for this function, the address is decoded and remapped for the target SRAM address, which is then latched at the end of the select cycle. This technique reduces the number of registers to seven, for capturing SADD[6:0] (SRAM ADDress bus bits 6 → 0). Figure 2-2 presents an overview of this SRAM address generator.

2.2.9 Memory Address Remapper

This logic performs an address remapping function on the memory transfer addresses such that only 22 locations are used out of the full 8 MBytes of IPack memory space. This remapping provides for a valid, unique, address hit when 1 of the 22 address lines is asserted to a logic ’1’ state, with the other 21 address lines being ’0’. These 22 memory locations then have their addresses converted, in ascending order, to a sequential address list starting at SADD = 40 *hex* and ending with SADD = 55 *hex*. Any other Memory Transfer address values will be ignored as an invalid transfer with no acknowledgement which will result in a bus-time-out error.

2.2.10 32-KB SRAMs

These two blocks provide the READ and WRITE locations necessary to implement half of the ID, most of the I/O and all of the memory transfers for the TESTIP. All accesses are byte-lane controlled. The SRAMs were used for economic reasons, since the implementation of one hundred eleven 16-bit READ/WRITE registers would have been prohibitively expensive by any other technique.

2.3 TESTIP Schematic

There is only a single page schematic for the TESTIP. It is included in Appendix B to this document.

On the left side is the Logic Connector through which all transactions are performed between the TESTIP and its carrier. On the right is U1, the TESTIP Controller EPLD, an ALTERA 7160E device. In the top right portion of the schematic is found two 32 KB SRAM devices, U2 and U3. The bottom right corner contains an octal buffer, 74FCT541, that performs (three channels of) I/O buffering. The I/O connector is on the right side of the schematic. The only other components are passive, board and IC- filtering capacitors and pullup resistors, and four jumper/shunt switches for developing the board number and for automatically self-interrupting during a global-interrupt event.

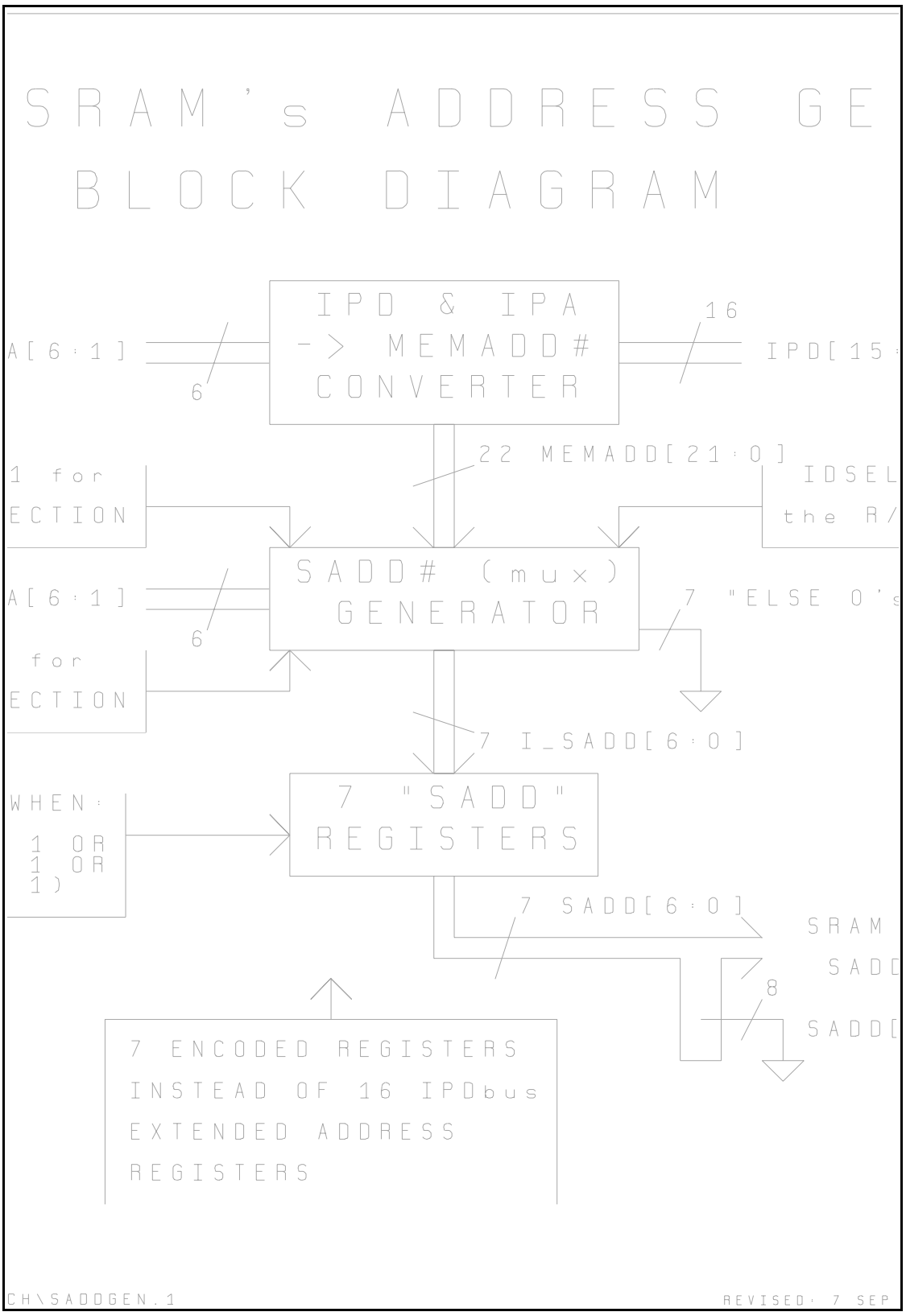


Figure 2-3 **SADDGEN: SRAM's Address Generator Block Diagram**

4 presents the TESTIP's logic diagram. The link between the logic diagram and the schematic clearly partitions components and their functions. The logic connector at the top of 4 is J1 on the schematic. The next block down corresponds to the pair of SRAM devices at U2 and U3. The largest block on 4 depicts U1. The I/O Interface buffer is U4, and the I/O connector is J6.

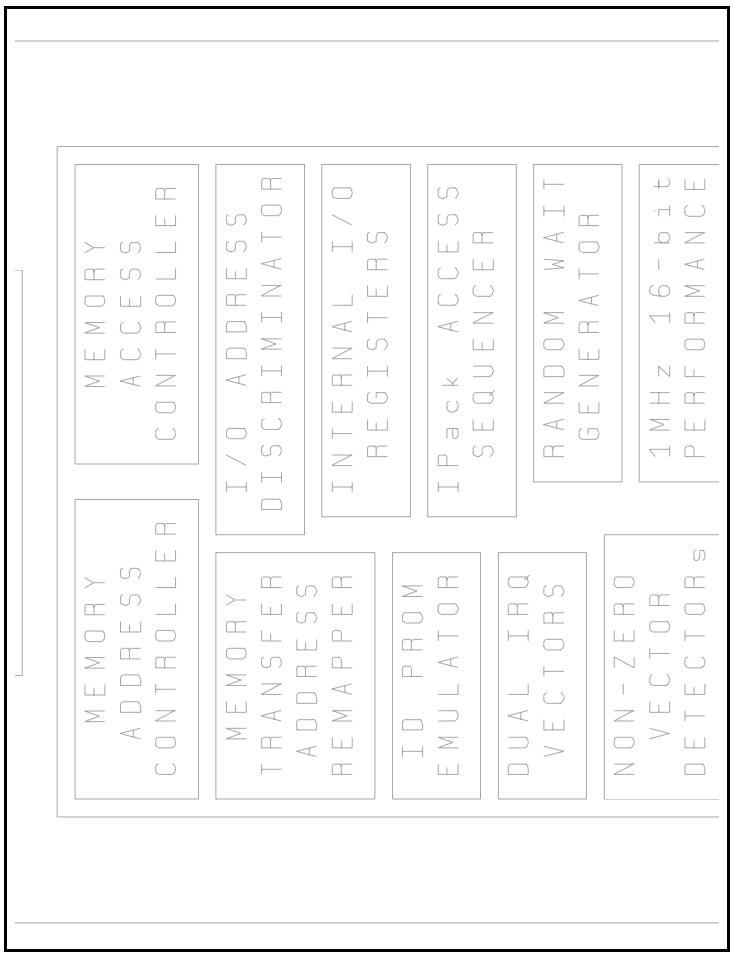


Figure 2-4 **TESTIP's Top Logic Diagram**

2.4 I/O Accesses

There are two major sections to the I/O map of the TESTIP. The first one consists of 57 locations:16-bit wide READ/WRITE “registers” mapped into the first 57 word locations of the on-board SRAM. All accesses to the SRAM (I/O, ID, and Memory) completely obey byte-lane selections for both WRITEs and READs (unlike most other IPacks which typically provide 16-bit READs regardless of byte-lane selections). The first 57 locations correspond to IPA[6:1] addresses of 00 → 38 *hex*, inclusively. On the schematic, these I/O locations directly correspond to SADD[6:0] (SRAM ADDresses) such that the first 57 I/O locations are SADD addresses 00 → 38 *hex*.

The remaining group of seven I/O locations are actual registers and pseudo-registers contained within the EPLD described below:.

2.4.1 I/O Location #1

The first EPLD-based I/O location, corresponding to IPA = 39 *hex*, contains a 16-bit ”timer” that runs at a fixed 1 MHz rate when enabled. Since the timer is completely synchronous and is driven by the ICLK, it can be read at any time, on-the-fly. READ accesses ignore the byte-lane control signals such that READs always present the full 16-bit timer value. Any WRITE to this location, including either byte-lane or full word, using any data value, will reset the timer to zero, whether it is running (reset on-the-fly) or stopped.

2.4.2 I/O Location #2

The second EPLD-based I/O location, corresponding to IPA = 3A *hex*, is a pseudo-register that controls the running of the performance timer. It is a pseudo-register because no real physical registers exist at this location. Any width WRITE access using any data value starts the performance timer. Any width READ access (reads as all zeroes) stops the performance timer. 1 presents the performance timer controller access types with corresponding functional operations:

Table 2-1 **Performance Timer Functions and Access Types**

Timer Function:	Access Location and Type:
STOP TIMER	Any READ @ IPA=3A
READ TIMER	Any READ @ IPA=39
RESET TIMER	Byte/Word WRITE of any data @ IPA=39
START TIMER	Byte/Word WRITE of any data @ IPA=3A
PAUSE/CONTINUE	Any READ & then any WRITE @ IPA=3A

2.4.3 I/O Location #3

The third EPLD-based I/O location, corresponding to IPA = 3B *hex*, is a three-bit, general-purpose control/status register.

- Bit 0, the least significant bit, is the inversion of the N_ERROR signal. When this bit is set to a ‘1’, the EPLD will assert the N_ERROR line to its low state for subsequent reading by carriers that have the ability to post the state of this line. When this bit is cleared to a ‘0’, the EPLD will negate the N_ERROR line to the carrier.
- Bit 1 turns the random-wait-cycle generator on and off. Setting this bit to a ‘1’ enables the insertion of wait cycles for ALL TESTIP accesses, while clearing it to a ‘0’ enables the TESTIP to respond to ALL carrier accesses with no wait cycles.
- Bit 2 is a direct reflection of the logic state of the N_STROBE signal, for those carriers that provide connectivity to this signal.

On power-up, bits 0 and 1 are cleared to zeroes to negate N_ERROR and disable wait cycle insertions, respectively. Valid WRITE accesses to this register are byte-lane-sensitive; low-byte or word accesses work; high-byte-only access attempts will result in an acknowledgement but with no register content changes. READs of this register will provide the registered information for bits 0 and 1, the signal state of N_STROBE for bit 2, and a zero-fill for IPD[15:3].

2.4.4 I/O Location #4

The fourth EPLD-based I/O location, corresponding to IPA = 3C *hex*, is a two-bit interrupt-status register. When bit 0 = ‘1’ it indicates that a level 0 interrupt request is currently being asserted to the carrier via the signal N_INTREQ0. When bit 1 = ‘1’ it indicates that a level 1 interrupt request is currently being asserted to the carrier via the signal N_INTREQ1. When this location is read, bits 0 and 1 indicate the interrupt status, while a zero-fill is applied to IPD[15:2]. Interrupt 0 is cleared by a WRITE of a ‘1’ to bit 0 of this register. The WRITE is fully qualified for data = ‘1’ and for byte-lane 0 select; low-byte or word accesses work; data = ‘0’ or high-byte-only access attempts will result in an acknowledgement but with no register content changes. The same is true for the clearing of interrupt level 1 with a WRITE of a ‘1’ to bit 1 of this register. A subsequent READ of the status bit after a clearing event (WRITE of a ‘1’) will indicate that the interrupt has been cleared by the return of a ‘0’ value (WRITE ‘1’; READ ‘0’). Both of these bits are set to one value by either a valid WRITE to the interrupt control register (local interrupt request), or the application of a global- interrupt input, provided their corresponding interrupt vectors are non-zero values.

2.4.5 I/O Location #5

The fifth EPLD-based I/O location, corresponding to IPA = 3D *hex*, is a three-bit interrupt-control register that is tightly coupled to the interrupt-status register (see above).

- A WRITE of a ‘1’ to bit 0 asserts both the interrupt-status bit 0 and the N_INTREQ0 signal to the carrier, provided the interrupt vector for level 0 is a non-zero value.
- A WRITE of a ‘1’ to bit 1 asserts both the interrupt status bit 1 and the N_INTREQ1 signal to the carrier, provided the interrupt vector for level 1 is a non-zero value.

- A WRITE of a '1' to bit 2 causes a 250 ns low pulse to appear on the global interrupt-output signal N_GIO on the I/O connector, regardless of the values in the interrupt vectors.

Any READ of this register will return values of '1' in bits 0 and 1 when local interrupt requests have been generated, while a zero-fill is applied to IPD[15:2].



NOTE: Bit 2 of the interrupt request register will always read back as a zero. Bits 0 and 1 are cleared by WRITEs to the interrupt-status register (see above).

2.4.6 I/O Locations #6 and #7

The last two EPLD-based I/O locations are a pair of 8-bit interrupt vectors; the next to last I/O location is a vector for interrupt request #0, while the last I/O location provides a vector for interrupt request #1. These locations must be non-zero values for interrupts to be asserted. An in-bound global-interrupt-input and local-interrupt request attempts will be blocked for either or both interrupt requests for zero-value vectors. Global-interrupt inputs can selectively assert interrupt request #0 alone by maintaining vector #1 with a data value of '00'.

2.4.7 EPLD-based I/O Defaults

ALL EPLD-based registers are cleared to zero on power-up. This of course does not apply to the N_STROBE status bit which is hardware signal monitoring only. Figure 2-4 provides a simple summary of the I/O accesses.

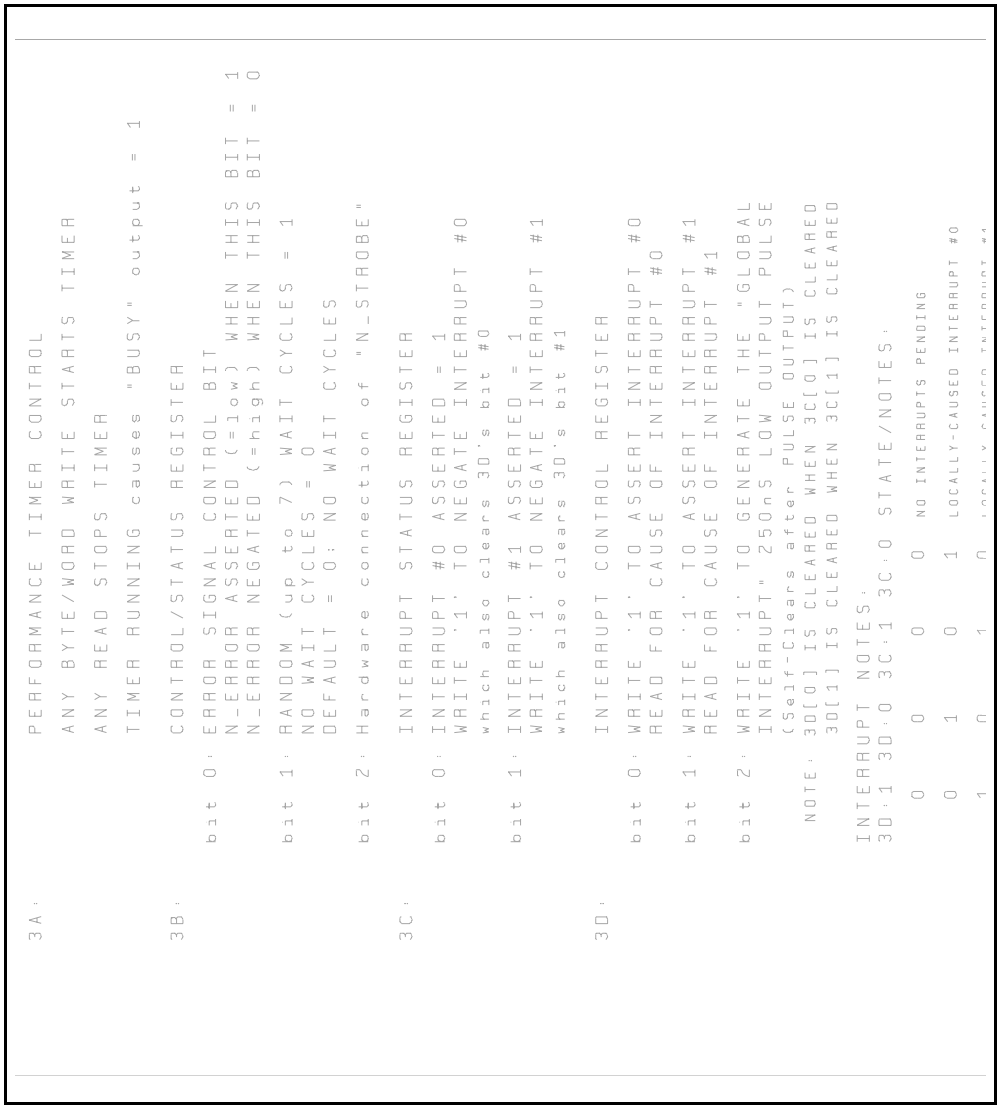


Figure 2-5 **I/O Accesses Summary**

2.5 Memory Accesses

The memory testing support provided by the TESTIP is a fully-decoded, partial-hit memory map consisting of 22 valid memory locations spread over an 8 MB range; best depicted as a bubble-one addresser over the 22 address lines. Figure 2-5 describes the scheme used. Access attempts to any 16-bit location not listed will result in no acknowledgement and its resultant bus time-out. The VMAN[5:0] labels on the far right side of Figure 2-5 correspond to the TESTIP's test points: TP5, TP7, TP8, TP4, TP3, and TP6, respectively. For each of VMAN[4:0] test points, there are only four valid memory-address conditions that will generate a high-state output; and, only two for VMAN[5]. All 22 valid accesses to the SRAM completely obey byte-lane selections for both WRITEs and READs.

2.6 Identification Accesses

The identification (ID) accesses portion of the TESTIP is significantly different than other IPacks from SYSTRAN Corp.

The ID space is divided evenly between READ-only accesses (per specification), and READ/WRITE accesses (per recommendation).

The lower half of Figure 2-6 presents a simple summary of all of the ID space and the associated data fields and accesses.

2.6.1 Configuration ID Space

The first 12 ID locations, IPA = 00 → 0B *hex* contain the standard identification (header) information, typically used for system configuration. These locations are READ-only accesses, with the upper byte set to '00', and the lower byte providing the data depicted in Figure 2-6. These READs are always 16-bits wide as the TSTCTRL EPLD-logic ignores the byte select lines for these accesses. Attempted WRITEs have no effect on the data fields. Acknowledgement is provided for WRITEs for those carriers capable of performing such transfers.

2.6.2 Addressing and Number ID Space

The next 20 ID locations, IPA = 0C → 1F *hex*, contain READ-only variable fields. The lower 5 bits, IPD[4:0], have the address of the location being accessed as defined by IPA[5:1], mapped respectively. This "A-in-A" ("Address-in-Address") function is useful for evaluating the address bus for stuck bits, except for IPA[6].

The upper three bits of the lower byte, IPD[7:5], present the board number as described by section 2.7. These READs are 16-bit widths because the EPLD ignores byte-lane selection for accesses in this area. The upper byte always READs '00'. WRITE attempts, while acknowledged, have no effect on the data in this ID space.

ST IPack MEMORY ADDRE

address) 0	9	8	7	6	5	4	3	2	1	0	IPA 6	5	4	3	2	1	
ent IPA 7	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	PHYSICA ADDRESS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	4
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	8
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	16
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	32
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	64
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	128
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	256
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	512
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1024
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	2048
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	4096
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	8192
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	16384
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	32768
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	65536
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	131072
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	262144
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	524288
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1048576
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2097158
											<-- (binary)						(decimal)

VMAN# = Valid Memory Address Nibble #

Figure 2-6 **Memory Accesses Summary**

2.6.3 SRAM-based ID Mapping

The upper 32 locations of the ID space have full WRITE/READ-BACK capability for those carriers with the ability to address and WRITE to this ID space. Figure 2-6 shows the SRAM-based ID mapping scheme of IPA = 20 →3F *hex* ⇒SADD[6:0] = 60 → 7F *hex*. As with all other SRAM-based transfers, these ID accesses fully comply with byte-lane selections from the carrier.

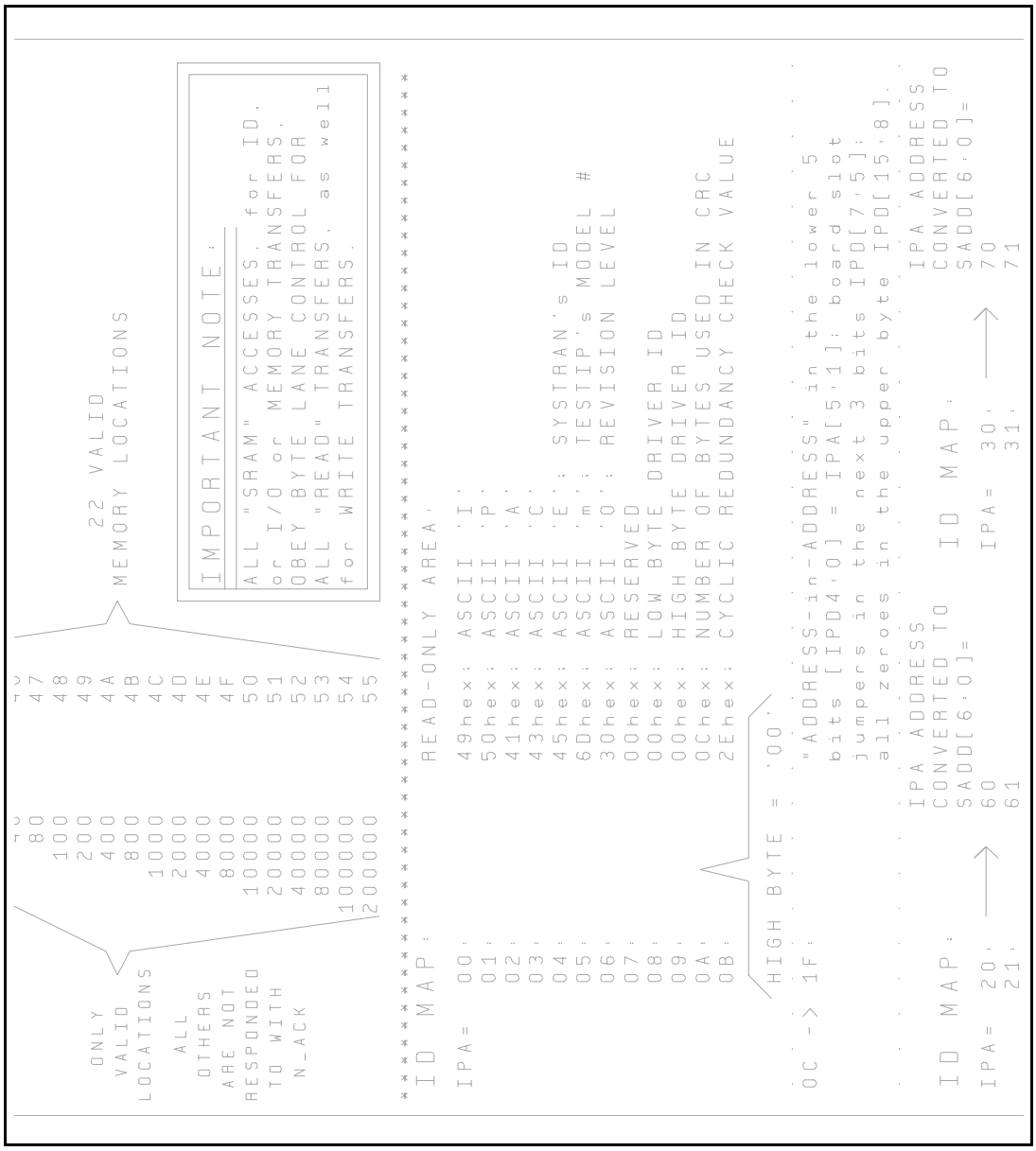


Figure 2-7 **TESTIP: Test IPack SRAM's Address Map**

2.7 Board Number

The TESTIP has built into some of its ID fields (see section 2.6, above) a three-bit field that is jumper selectable for identifying individual TESTIP's in multiple board testing scenarios. This scheme provides the ability to allocate unique board numbers for up to eight different TESTIP's on an embedded carrier under test, five on the VMESC5 carrier, or four (or less) for most standard carriers. Figure 2-7 provides the proper jumper selections for all eight board numbers possible.

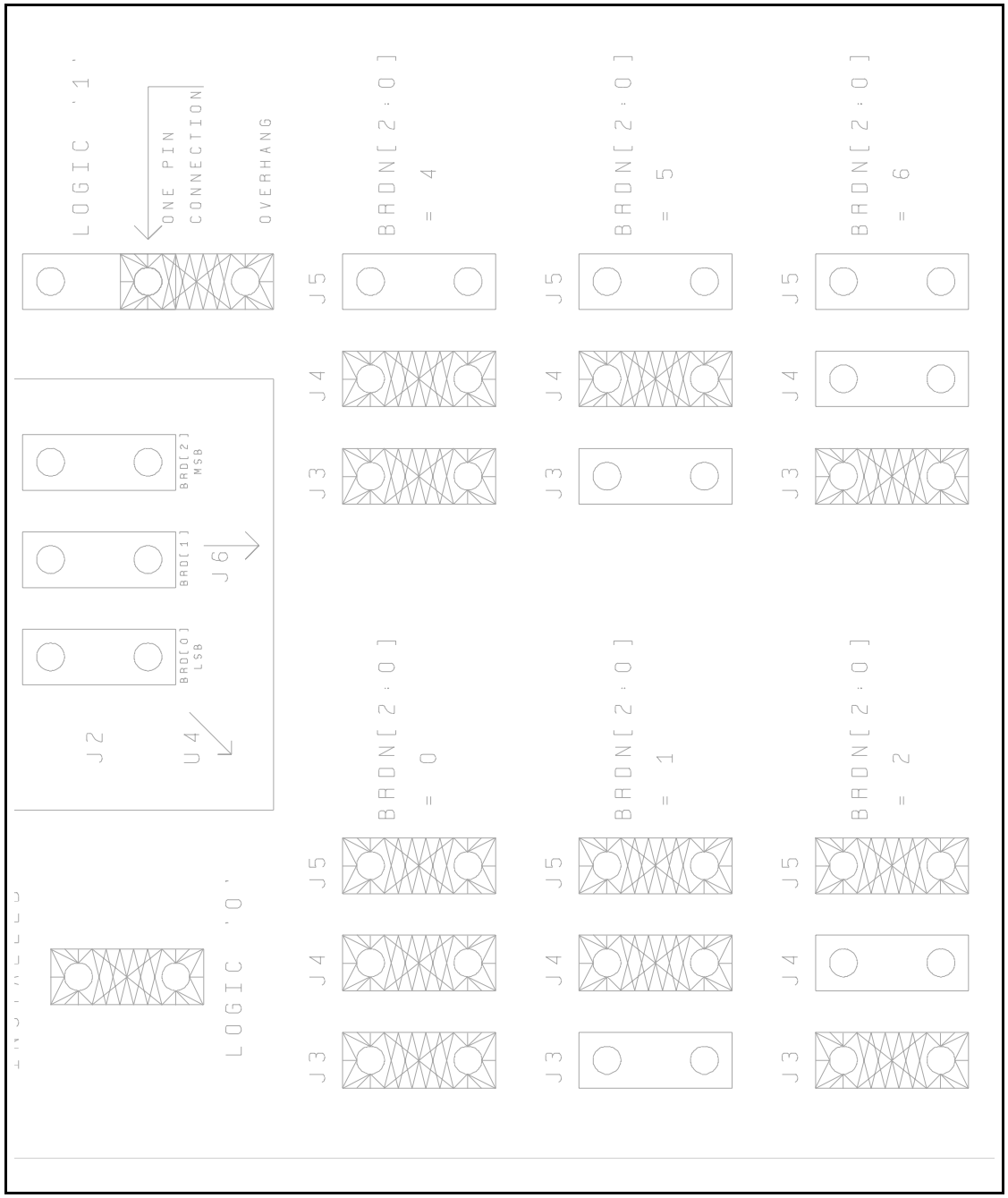


Figure 2-8 **Board Number Jumpers**

2.8 Timing Diagrams

Figures 2-8 through 2-13 present a collection of all of the variations of timing diagrams that are executable by the TESTIP. Most of the variations occur due to WAIT and/or HOLD cycle insertions by the TESTIP and/or Carrier, respectively.

Figure 2-8 presents all of the possible WAIT cycle insertions for all transfer types.

There are two target areas for I/O accesses; the SRAM, and the EPLD-based registers. Figure 2-9 presents all of the possible combinations for the SRAM-based I/O accesses, with variations in READ versus WRITE, with or without wait cycles, and with or without hold cycles. For all three SRAM-based transfer types the “N_CE” signal is the asserted low SRAM chip (select) enable; the “N_OE” signal is the asserted low SRAM output enable that is asserted during READ transfers; the “N_WE” signal is the asserted low SRAM WRITE enable that is asserted during WRITE transfers.



NOTE: The rising edge of “N_WE” performs the actual WRITE This edge precedes the rising edge of ICLK to ensure that data is properly captured.

Figure 2-10 presents all of the possible combinations for the EPLD-based I/O registers and pseudo registers accesses, with variations in READ versus WRITE, with or without hold cycles, and with or without wait cycles.

Figure 2-11 presents the only type of IPack transfer that is READ-only—the interrupt vector. The Interrupt vector READ transfer variations are depicted with or without hold cycles, and with or without wait cycles.

Figure 2-12 demonstrates all of the possible combinations for memory accesses to and from the SRAM, with variations in READ versus WRITE, with or with hold cycles, and with or without wait cycles.

Figure 2-13 presents the 12 different possible timing diagrams for the ID transfers. The READ-only transfers from the lower half of the ID address space is depicted on the left third of Figure 2-13. The SRAM-based WRITE/READ-BACK access combinations for the upper half of the ID space is shown on the right two-thirds of Figure 2-13.

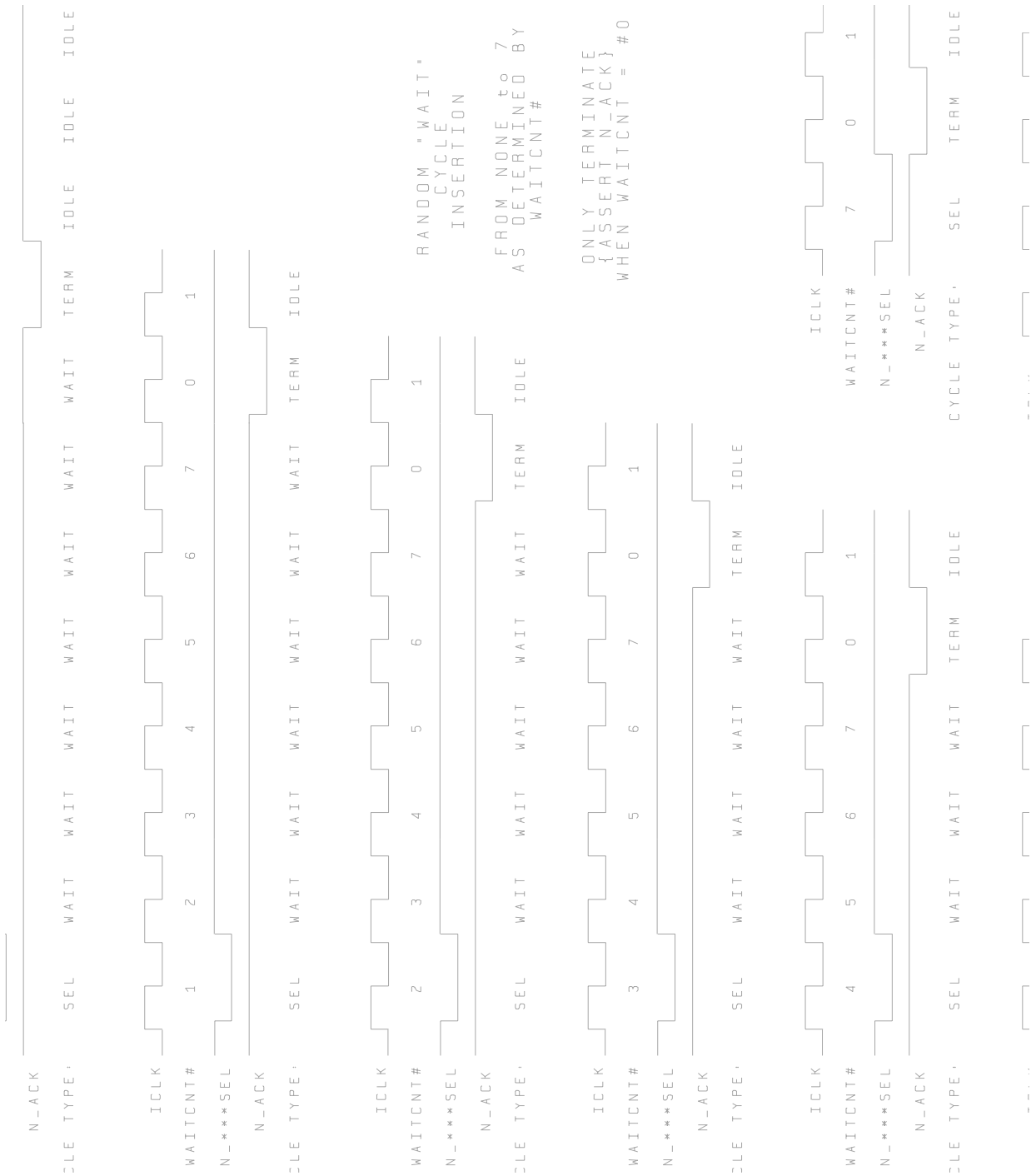


Figure 2-9 **WAIT Cycles Timing Diagrams**

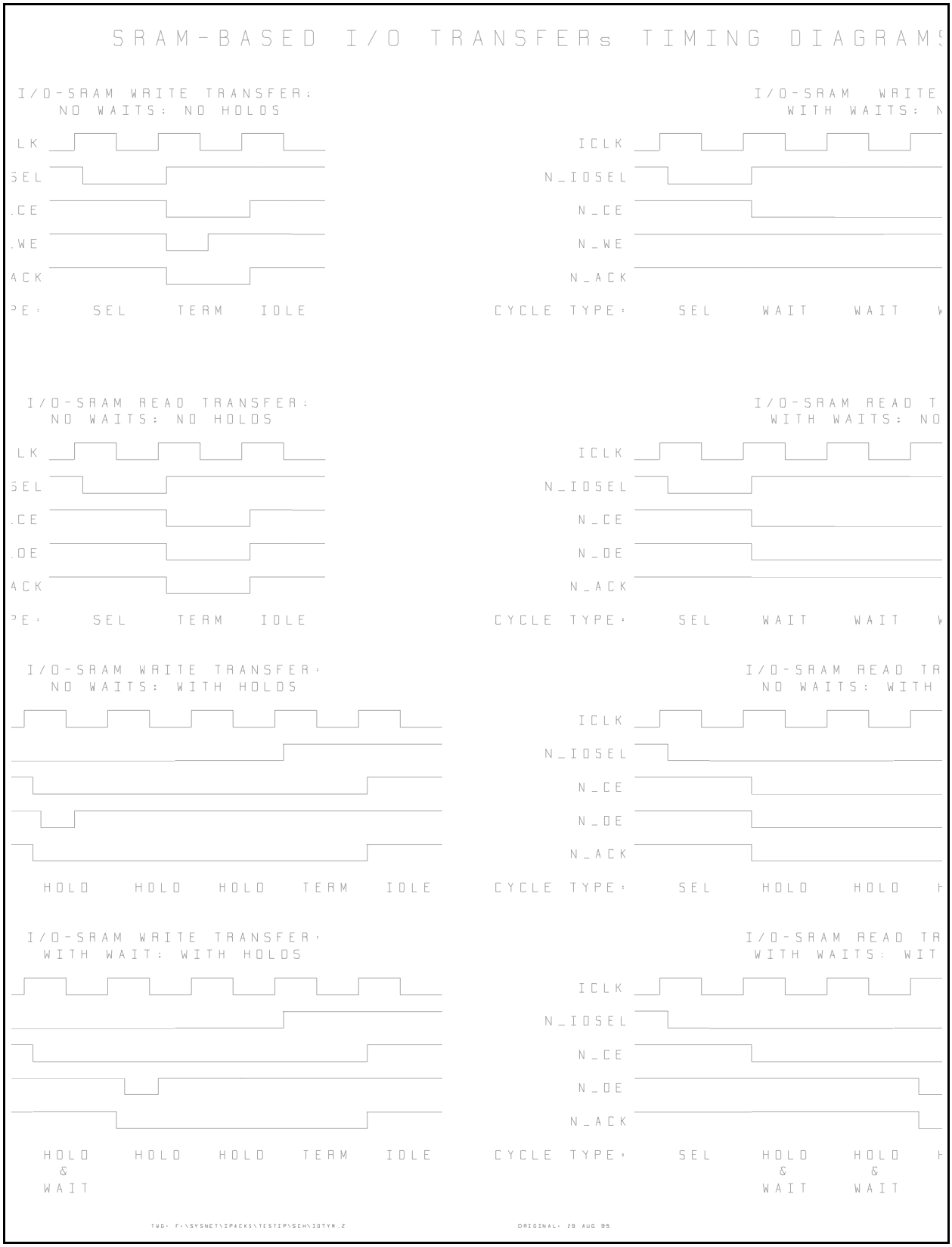


Figure 2-10. **SRAM-based I/O Transfers Timing Diagrams**

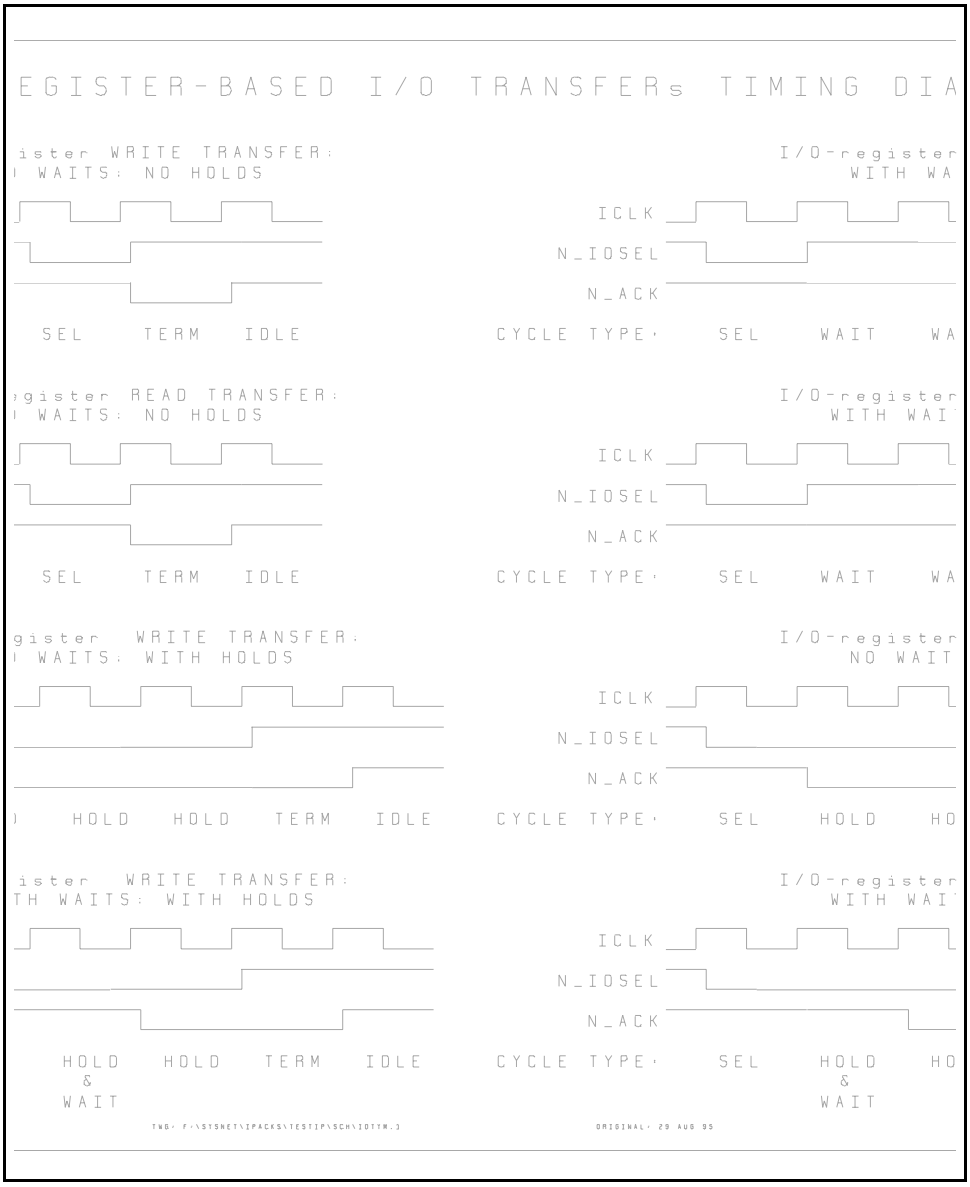


Figure 2-11 **Register-based I/O Transfers Timing Diagrams**

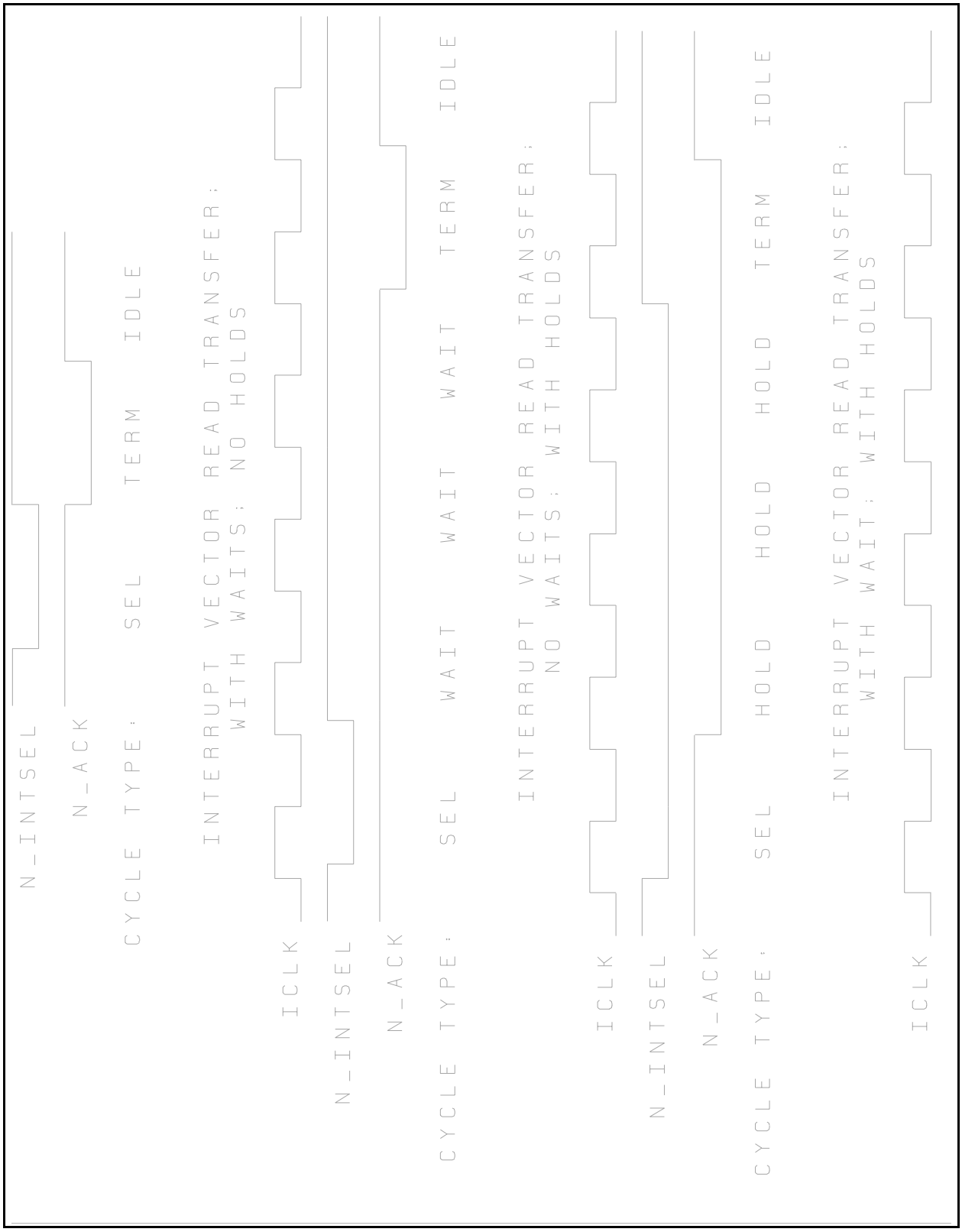


Figure 2-12. **Interrupt Vector READ Transfers Timing Diagrams**



Figure 2-13 **Memory Transfers Timing Diagrams**

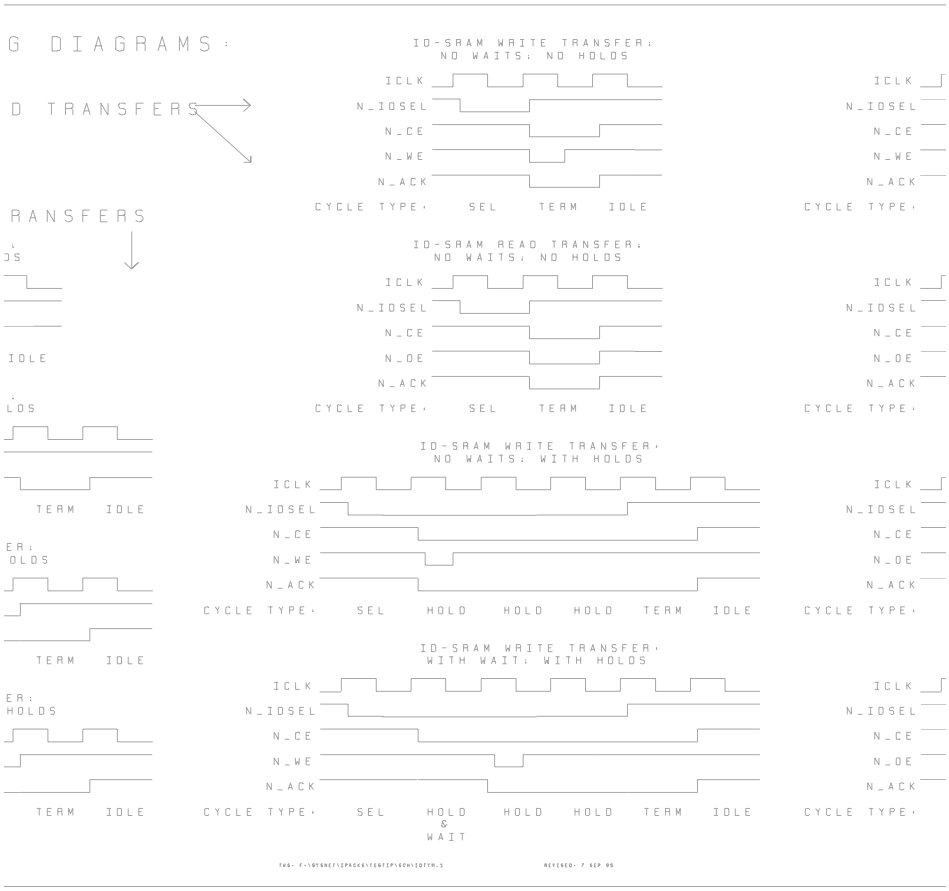


Figure 2-14 **ID Transfers Timing Diagrams**

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3.0 HARDWARE INSTALLATION

3.1 Unpacking the TESTIP

The contents of the TESTIP shipping packages are listed in 2:

Table 3-2 Contents of TESTIP Shipping Packages

QTY	DESCRIPTION
1	TESTIP Printed Circuit Assembly
1	TESTIP User Manual *

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals up to one per board are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix “BTMR-” followed by the product order part number. (e.g. BTMR-TESTIP).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Visual Inspection of the TESTIP

Examine the TESTIP to determine if any damage occurred during shipping.

3.3 TESTIP Installation



NOTE: The TESTIP is an Electrostatic Sensitive Device (ESD). Therefore, the hardware installation of the TESTIP must be conducted on a good anti-static workbench to protect the IPack and carrier boards. The IPack carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the TESTIP can be completed.

The TESTIP installation requires the following tools:

Table 3-3 TESTIP Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

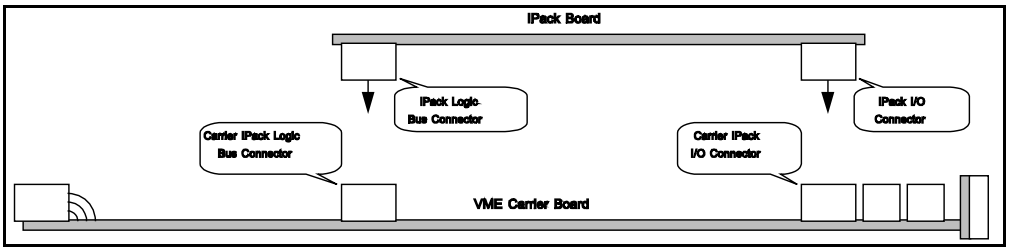


Figure 3-15 **Installation of the TESTIP on a VME IPack carrier board.**

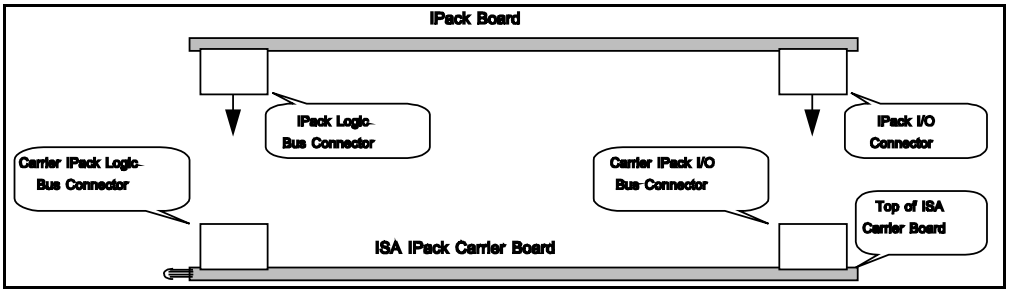


Figure 3-16 **Installation of the TESTIP on a ISA IPack carrier board.**

Reference Figure 3-1 for the diagram of how the TESTIP is installed on a VME IPack carrier, and Figure 3-2 for installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IPack Carrier board user's manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IPack carrier and move it to the ESD controlled area where the installation of the TESTIP can be made.
3. Remove the TESTIP from the shipping package and place it on the ESD bench.
4. If global interrupts are to be daisy-chained using the solder donuts instead of the I/O connection, wire/solder the TESTIP's together at this time.
5. Install the TESTIP onto the carrier board by applying adequate and equal pressure to the TESTIP board at both ends.

* 6. Install four M2x5 mm flat head machine screws onto the IPack carrier's IPack connectors.

This completes the installation of the TESTIP to the carrier board.

Table 3-4 **IPack Logic Bus Pin Assignments**

Original IPack Signals Names	IPack Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-5 **IPack I/O Connector Pin Assignments**

IPack I/O Pin #	Signal Name
50	NO CONNECTION
49	NO CONNECTION
48	NO CONNECTION
47	NO CONNECTION
46	NO CONNECTION
45	NO CONNECTION
44	NO CONNECTION
43	NO CONNECTION
42	NO CONNECTION
41	NO CONNECTION
40	NO CONNECTION
39	NO CONNECTION
38	NO CONNECTION
37	NO CONNECTION
36	NO CONNECTION
35	NO CONNECTION
34	NO CONNECTION
33	NO CONNECTION
32	NO CONNECTION
31	NO CONNECTION
30	NO CONNECTION
29	NO CONNECTION
28	NO CONNECTION
27	NO CONNECTION
26	NO CONNECTION
25	NO CONNECTION
24	NO CONNECTION
23	NO CONNECTION
22	NO CONNECTION
21	NO CONNECTION
20	NO CONNECTION
19	NO CONNECTION
18	NO CONNECTION
17	NO CONNECTION
16	NO CONNECTION
15	NO CONNECTION
14	NO CONNECTION
13	NO CONNECTION
12	NO CONNECTION
11	NO CONNECTION
10	NO CONNECTION
9	NO CONNECTION
8	NO CONNECTION
7	NO CONNECTION
6	GND
5	BUSY
4	GND
3	N_GII
2	GND
1	N_GIO

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4.0 PROGRAMMING GUIDE

This section of the manual describes the operation of the TESTIP from the software perspective, detailing the TESTIP registers and providing programming examples. A more detailed description of the hardware can be found in section 2.0 DESCRIPTION and section 6.0 TYPICAL APPLICATIONS.

4.1 Description

The TESTIP is a general purpose TEST IPack capable of performing all of the well-defined transfer operations for the *Industry Pack Logic Interface Specification Revision 0.7.1.* Its principle function is that of a carrier tester, with provisions for evaluating: the transfer-performance-throughput characteristics, local- and global-interrupt handling capabilities, random-wait-cycle insertions' handling, complete address testing for all transfer types, advanced transfer ability for ID WRITEs, as well as byte-lane selectability for both READ and WRITE transfers for MEMORY, I/O, and ID transactions. Its 16-bit READ-on-the-fly 1 MHz timer and 111 READ/WRITE "memory" locations make it an ideal supplement IPack when not being used as a carrier tester.

4.2 ID PROM Addresses

Table 4-1 shows the TESTIP ID PROM map. The addresses shown are the IPack addresses. To determine the correlation of the local bus to the IPack address, see paragraphs A-4.4: Word Access Address Translation, and A-4.5: Byte Access Address Translation.

Table 4-1 **TESTIP ID Address Space Listing**

IPack Address	Description	Data READ
IPA = 00 *hex*	ASCII 'I'	49 *hex*
IPA = 01 *hex*	ASCII 'P'	50 *hex*
IPA = 02 *hex*	ASCII 'A'	41 *hex*
IPA = 03 *hex*	ASCII'C'	43 *hex*
IPA = 04 *hex*	SYSTRAN's ID	45 *hex*
IPA = 05 *hex*	TESTIP Model Number	6D *hex*
IPA = 06 *hex*	Revision Level	30 *hex*
IPA = 07 *hex*	Reserved	00 *hex*
IPA = 08 *hex*	Low Byte Driver ID	00 *hex*
IPA = 09 *hex*	High Byte Driver ID	00 *hex*
IPA = 0A *hex*	Number of Bytes Used	0C *hex*
IPA = 0B *hex*	CRC	2E *hex*

4.3 IPack I/O Address Map

The TESTIP I/O Address Map was designed with efficiently located data, control and interrupt registers in the IPack I/O address space (IPA = 00->3F *hex*). The address detector circuitry is fully decoded.

The first 57 locations in I/O space are 16 bit READ/WRITE locations. The next location (IPA = 39 *hex*) is the TESTIP 1MHz timer. This timer is reset by performing any byte or word WRITE to the location, a READ gives the current timer value.

IPA 3A *hex* is the Performance Timer Control register. Any byte/word WRITE starts the timer and any READ stops the timer.

The TESTIP Control/Status register is located at the next location, IPA = 3B *hex*. Bit 0 is the TESTIP IPack Error Signal Control bit and bit 1 is the Random Wait Cycles bit.

The TESTIP Interrupt Status register is located at the next location, IPA 3C *hex*. Bit 0 is the assertion flag for interrupt 0, bit 1 is the assertion flag for interrupt 1.

IPA 3D *hex* is the TESTIP Interrupt Control register. Bit 0 is the control bit for interrupt 0, bit 1 is the control bit for interrupt 1.

IPA's 3E and 3F are the Interrupt Vector registers for interrupts 0 and 1, respectively.

Table 4-2 shows the TESTIP register map. The addresses shown are the IPack addresses. To determine the correlation of the local bus to IPack address see paragraphs A.3, Word Access Address Translation and A.4, Byte Access Address Translation.

For further information regarding the TESTIP registers, see section 2.4.

Table 4-2 **TESTIP I/O Address Map**

IPack Address	Bits	Description
IPA = 00 → 38 *hex*	[15:0]	57x16-bit READ/WRITE locations
IPA = 39 *hex*	[15:0]	1 MHz Timer
IPA = 3A *hex*	[15:0]	Performance Timer Control
IPA = 3B *hex*	[XXXX,XXXX][XXXX,X][2.0]	**Control/Status Register** Bit 2: READ Only connection of N_STROBE Bit 1: Random Wait Cycles (0=OFF, 1=ON) Bit 0: Error Signal Control (0=Negated, 1=Asserted
IPA = 3C *hex*	[XXXX,XXXX][XXXX,XX][1.0]	**Interrupt Status Register** Bit 0, 1 = Interrupt 0 Asserted Bit 1, 1 = Interrupt 1 Asserted WRITE 1 to Negate.
IPA = 3D *hex*	[XXXX,XXXX][XXXX,X][2.0]	**Interrupt Control Register** Bit 0, 1 = Interrupt 0 Asserted Bit 1, 1 = Interrupt 1 Asserted Bit 2, 1 = Global Interrupt Pulse Asserted
IPA = 3E *hex*	[XXXX,XXXX] [7.0]	Interrupt Vector 0 (8-bit Register)
IPA = 3F *hex*	[XXXX,XXXX] [7.0]	Interrupt Vector 1 (8-bit Register)

NOTE: X = No WRITE, read as zero.

4.4 Word Access Translation

Table 4-3 shows the relationship between VME, PC-AT, and NBUS local bus addresses and the IPack address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-3 **Word Address Access Translation Table**

VME Bus Address	PC-AT Bus Address	NuBus Address	IPack Address
BASE+0	BASE+0	BASE+2	IPA = 00 *hex*
BASE+2	BASE+2	BASE+6	IPA = 01 *hex*
BASE+4	BASE+4	BASE+A	IPA = 02 *hex*
BASE+6	BASE+6	BASE+E	IPA = 03 *hex*
BASE+8	BASE+8	BASE+12	IPA = 04 *hex*
BASE+A	BASE+A	BASE+16	IPA = 05 *hex*
BASE+C	BASE+C	BASE+1A	IPA = 06 *hex*
BASE+E	BASE+E	BASE+1E	IPA = 07 *hex*
BASE+10	BASE+10	BASE+22	IPA = 08 *hex*
BASE+12	BASE+12	BASE+26	IPA = 09 *hex*
BASE+14	BASE+14	BASE+2A	IPA = 0A *hex*
BASE+16	BASE+16	BASE+2E	IPA = 0B *hex*

4.5 Byte Access Address Translation

Table 4-4 shows the relationship between VME, PC-AT, and NBUS local bus addresses and the IPack address for byte accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-4 **Byte Access Address Translation Table**

VME Bus Address	PC-AT Bus Address	NuBus Address	IPack Address	Byte-lane
BASE+1	BASE+0	BASE+3	IPA = 00 *hex*	0
BASE+0	BASE+1	BASE+2	IPA = 00 *hex*	1
BASE+3	BASE+2	BASE+7	IPA = 01 *hex*	0
BASE+2	BASE+3	BASE+6	IPA = 01 *hex*	1
BASE+5	BASE+4	BASE+B	IPA = 02 *hex*	0
BASE+4	BASE+5	BASE+A	IPA = 02 *hex*	1
BASE+7	BASE+6	BASE+F	IPA = 03 *hex*	0
BASE+6	BASE+7	BASE+E	IPA = 03 *hex*	1
BASE+9	BASE+8	BASE+13	IPA = 04 *hex*	0
BASE+8	BASE+9	BASE+12	IPA = 04 *hex*	1
BASE+B	BASE+A	BASE+17	IPA = 05 *hex*	0
BASE+A	BASE+B	BASE+16	IPA = 05 *hex*	1
BASE+D	BASE+C	BASE+1B	IPA = 06 *hex*	0
BASE+C	BASE+D	BASE+1A	IPA = 06 *hex*	1
BASE+F	BASE+E	BASE+1F	IPA = 07 *hex*	0
BASE+E	BASE+F	BASE+1E	IPA = 07 *hex*	1
BASE+11	BASE+10	BASE+23	IPA = 08 *hex*	0
BASE+10	BASE+11	BASE+22	IPA = 08 *hex*	1
BASE+13	BASE+12	BASE+27	IPA = 09 *hex*	0
BASE+12	BASE+13	BASE+26	IPA = 09 *hex*	1
BASE+15	BASE+14	BASE+2B	IPA = 0A *hex*	0
BASE+14	BASE+15	BASE+2A	IPA = 0A *hex*	1
BASE+17	BASE+16	BASE+2F	IPA = 0B *hex*	0
BASE+16	BASE+17	BASE+2E	IPA = 0B *hex*	1

4.6 Register Descriptions

The TESTIP has sixty-four 16-bit wide registers. The control registers allow user control of hardware functions. The interrupt related registers allow the triggering of interrupts, provide status of the interrupt bits, and programming of the interrupt vectors. Byte WRITEs to any of these registers are non-destructive to adjacent bytes. The registers are described in detail below.

4.7 Registers 00 →38 Description

These 16-bit registers are general READ/WRITE registers. On power-up all bits are in an unknown state.

4.8 1MHz Timer Description

A 1 MHz 16-bit timer. When read, it returns the current value of the timer. When written to, on either a byte or word boundaries, it causes the timer to reset to zero. On power-up the timer value is zero.

4.9 Performance Timer Control Register Description

This 16-bit READ/WRITE register controls both the Error Signal and the Random Wait Cycle features. Bit 0 is the Error Signal Control bit, bit 1 is the Random Wait Cycles Control bit, and bit 2 is a READ-only hardware connection of N_STROBE. On power-up all bits except bit 2 are set to zeros.

Table 4-5 **Interrupt Control Register Bit Descriptions – IP Address = 3B**

Bit#	Bits [15:3]	2	1	0
Bit Name	Not Used read as 0's	N_STROBE	Random Wait Cycles	Error Signal Control
R/W		R	RW	RW
Power-up State		State of N_STROBE Signal	0	0

4.11 Interrupt Status Register Description

This 16-bit wide READ/WRITE register provides the interrupt status for the two TESTIP interrupts. A bit is set in this register if there is an interrupt triggered by the corresponding bit. If a bit is set in this register, it is cleared by writing a '1' to that bit position. The status indication is valid whether the interrupt is enabled or disabled for the bit.

Table 4-6 **Interrupt Status Register Bit Description**

Bit#	Bits [15:2]	1	0
Bit Name	Not Used read as 0's	B1 IS	B0 IS
R/W		RW	RW
Power-up State		0	0

Bit#	**Interrupt Status Per Bit**
0	Input condition not detected for bit
1	Input condition detected for bit

4.12 Interrupt Control Register Description

This 16-bit READ/WRITE register controls both the TESTIP Interrupts. Bit 0 is the Interrupt-bit-0 control bit, bit 1 is the Interrupt-bit-1 control bit, and bit 2 is the Global-Interrupt Control bit. On power-up all bits are set to zeros.

Table 4-7 **Interrupt Status Register Bit Description**

Bit#	Bits [15:2]	2	1	0
Bit Name	Not Used read as 0's	Global Interrupt	Interrupt 1 Control Bit	Interrupt 0 Control Bit
R/W		RW	RW	RW
Power-up State		0	0	0

4.13 Interrupt Vector 0 Register Description

This 16-bit wide READ/WRITE register contains the interrupt vector for interrupt #0. Only the lower 8 bits are used. The upper 8 bits are read as zeros. This vector will be presented on the IPack data bus during an interrupt request transfer.

Table 4-8 **Interrupt Vector 0 Register Bit Descriptions – IP Address = 3E**

Bit#	Bits [15:8]	7	6	5	4	3	2	1	0
Bit Name	Not Used read as 0's	IV 0 B7	IV 0 B6	IV 0 B5	IV 0 B4	IV 0 B3	IV 0 B2	IV 0 B1	IV 0 B0
R/W		RW	RW	RW	RW	RW	RW	RW	RW
Power-up State		0	0	0	0	0	0	0	0

4.14 Interrupt Vector 1 Register Description

This 16-bit wide READ/WRITE register contains the interrupt vector for interrupt #1. Only the lower 8 bits are used. The upper 8 bits are read as zeros. This vector will be presented on the IPack data bus during an interrupt request transfer.

Table 4-9 **Interrupt Vector 0 Register Bit Descriptions – IP Address = 3F**

Bit#	Bits [15:8]	7	6	5	4	3	2	1	0
Bit Name	Not Used read as 0's	IV 1 B7	IV 1 B6	IV 1 B5	IV 1 B4	IV 1 B3	IV 1 B2	IV 1 B1	IV 1 B0
R/W		RW	RW	RW	RW	RW	RW	RW	RW
Power-up State		0	0	0	0	0	0	0	0

4.15 Programming Examples

The following examples show how to control and operate the TESTIP. The five examples demonstrate how to: control the timer, generate interrupts, generate a carrier IPack error signal, and how to generate wait states.

4.15.1 Timer Example

This example illustrates TESTIP Timer control and use.

- At power-up, all bits of the Timer Control register (IPA = 3A *hex*).
- At power-up, the value of the Timer register is '0' *hex*..
- At this point the counter is not running and the BUSY signal is not asserted.
- WRITE any value to IPA 3A *hex*. This enables the counter.
- At this point the counter is free-running and the BUSY signal is asserted.
- READ IPA 39 *hex.* This presents the current timer value while the timer is still running (read-on-the-fly).
- READ IPA 3A *hex*. This disables the counter.
- At this point the counter is not running and the BUSY signal is not asserted. Any READs to IPA 39 *hex* present the final value of the 16 bit timer.
- WRITE any value to IPA 39 *hex*. This clears the Timer value to '0' *hex*.

4.15.2 Interrupt Example

This example illustrates how to generate interrupts using the TESTIP.



NOTE: In order to self-interrupt with the global interrupt bit, the jumper J2 must be installed.



NOTE: This example assumes a suitable ISR (Interrupt Service Routine) exists. An example ISR is shown on page 4-9.

- At power-up, the value of the Interrupt Control register is '0000' *hex*.
- At power-up, the value of the Interrupt Vector registers are '0000' *hex*.
- At this point the TESTIP interrupts are disabled.
- WRITE value of the interrupt vector to IPA 3E *hex*. This assigns a vector to TESTIP interrupt 0. Note the interrupt vector assigned should point to a valid ISR.
- At this point the TESTIP is ready to cause interrupt #0.
- WRITE 0001 to IPA = 3D, the Interrupt Control register, this causes an interrupt on interrupt #0 of the TESTIP.



NOTE: Perform the next two lines in the ISR in order to eliminate the possibility of multiple interruptsfrom occuring with only one trigger.
- READ IPA 3C *hex*. A value of '0001' *hex* should be read. This indicates that an interrupt on interrupt #0 has occurred.
- WRITE '0001' *hex* to IPA 3C *hex*. This will clear the interrupt status bit for interrupt #0 and also clear the corresponding bit of IPA 3D *hex*.

- Repeat the above steps for interrupt 1 of the TESTIP (replacing any occurance of ‘0001’hex with ‘0002’hex).
- At this point both TESTIP Interrupt Vector registers contain valid values.
- WRITE ‘0004’hex to IPA 3D. This causes a global interrupt (both interrupts #0 and #1 are asserted).



NOTE: Perform the next two lines in the ISR in order to eliminate the possibility of multiple interrupts from occuring with only one trigger.
- READ IPA 3C *hex*. A value of ‘0003’ *hex* should be read. This indicates that an interrupts occurred on both interrupts #0 and #1.
- WRITE ‘0003’ *hex* to IPA 3C *hex*. This will clear the interrupt status bit for interrupts #0 and #1 and also clear the corresponding bits in IPA 3D *hex*.

- WRITE ‘0000’ *hex* to IPA’s 3E and 3F.
- At this point the TESTIP interrupts are disabled.

4.15.3 Interrupt Service Routine Example

If the interrupt capability of the TESTIP is used, a suitable ISR must exist. This example describes some steps that the ISR should perform. The host dependent details are left out since they will vary.

ISR ENTRY POINT

- READ the Interrupt Status register. Test the bits to determine which interrupt(s) has(have) occurred.
- The event (interrupt) usually indicates that some event driven action is to be taken. If this is the case, take the action associated with the detected interrupt(s). If the action taken must not be interrupted, disable interrupts while taking the action, then re-enable them.
- Remove the condition that caused the interrupt. If this is not practical to do from the ISR, disable the interrupt by clearing the enable bit for the interrupt in the interrupt enable register, and set a flag indicating that some other process should clear the condition. If the condition is cleared outside the ISR, then the clearing process must also re-enable the interrupt.
- Clear the interrupt status register by writing a ‘1’ to the bit(s) that is (are) set in the status register. This can effectively be accomplished by writing back the same value read from the status register.
- Return from exception.

4.15.4 Error Example

This example illustrates the use of the TESTIP to generate a carrier IPack error signal.

- At power-up, all bits of the Control/Status register (IPA = 3B *hex*) are set to '0', except for bit 2 which is set to the state of the N_STROBE Signal.
- WRITE '0001' to IPA 3B *hex*. This generates an IPack error signal to the carrier.
- WRITE '0000' to IPA 3B *hex*. This clears the error signal to the carrier.
- At this point the carrier IPack error register should reflect that an error occurred in slot A of the carrier.

4.15.5 Wait Example

This example illustrates the use of the TESTIP to generate a carrier IPack error signal.

- At power-up, all bits of the Control/Status register (IPA = 3B *hex*) are set to '0', except for bit 2 which is set to the state of the N_STROBE Signal.
- WRITE '0002' to IPA 3B *hex*. This enables the TESTIP to generate random wait states.
- At this point the TESTIP inserts random wait cycles for all carrier accesses.
- WRITE '0000' to IPA 3B *hex*. This disables the generation of random wait states from the TESTIP.

5.0 PERFORMANCE

5.1 Overview

This section provides several sets of emperical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the minimum and maximum specification envelopes presented in section 1.0: INTRODUCTION. Additionally, they provide the user with actual waveforms that further clarify IPack bus operations, beyond those presented in both section 2.0: DESCRIPTION, and Appendix A: SYSTRAN's IndustryPack Logic Interface Specification Synopsis.

5.2 System Configuration

The performance data for this section was obtained by using two different test configurations as shown in 17. The majority of the data was captured with the TESTIP being used on Slot A of the MVME162 card. The TESTIP was placed on slot A of the VMESC5 carrier for ID WRITE tests since the MVME162 card is not capable of performing these transfers. In both configurations the TESTIP resided on the IPack Logic Bus Extender (IPLBE) connected to the Logic Bus Breakout Board (IPLBB) via an 18″ Logic Bus Extender Ribbon Cable (BHAS-IPBEC18). All of the waveforms were captured using the HP 1 GHz Timing Master Module (16515A). Only

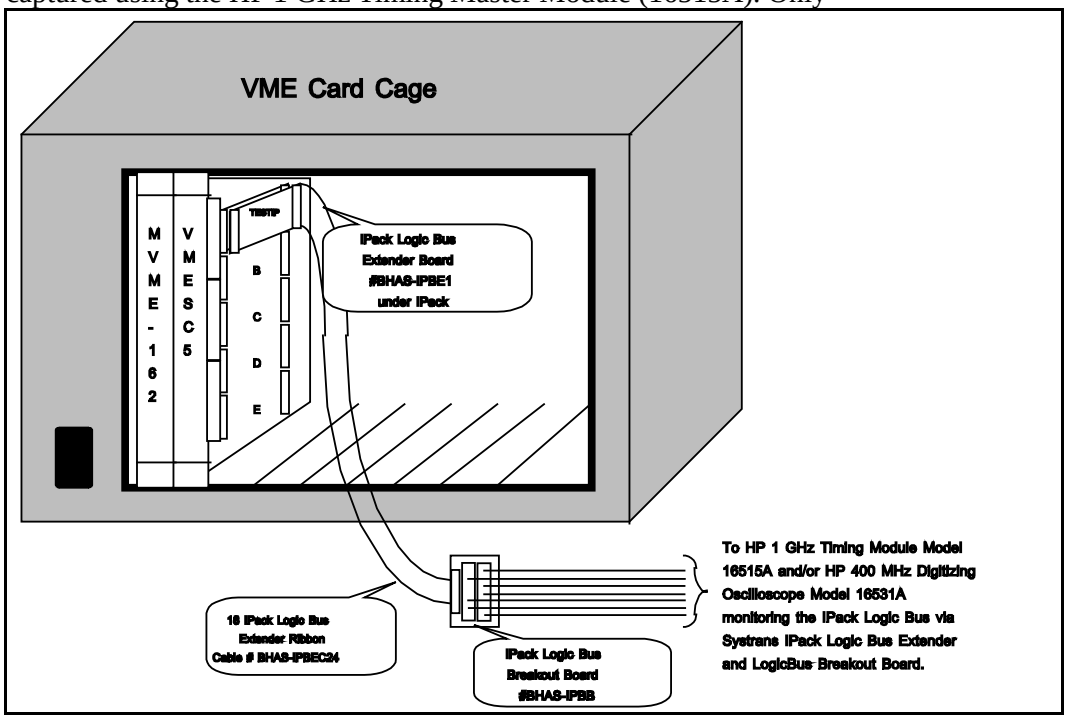


Figure 5-17 **Performance Test Equipment Configuration**

a few of the representative captured waveforms are presented in this section for brevity.

5.3 I/O Transfers

There are four variations of I/O transfers for the TESTIP, not including random-wait cycle insertions. They are: I/O WRITE (low byte, high byte, and full word) to SRAM, I/O READ (low byte, high byte, and full word) from SRAM, I/O WRITE to control registers, and I/O READ from status/control registers. The TESTIP was placed in slot A of the MVME162 card for these tests. 6 presents some typical event times (in nanoseconds), all of which are relative to the immediately-preceding rising edge of the ICLK. 18 presents a typical READ of 55 *hex* from the SRAM.

Table 5-6 **I/O READ From SRAM**

Function/Operation	↑ ICLK until	Time (ns)
I/O WRITE TO SRAM	↓ N_ACK	10
I/O WRITE TO SRAM	↑ N_ACK	9
I/O READ FROM SRAM	↓ N_ACK	11
I/O READ FROM SRAM	IPDbus' HIGH➢LOW Impedance	21
I/O READ FROM SRAM	↑ N_ACK	9
I/O WRITE TO REGISTER	↓ N_ACK	11
I/O WRITE TO REGISTER	↑ N_ACK	9
I/O READ FROM REGISTER	↓ N_ACK	11
I/O READ FROM REGISTER	IPDbus' HIGH➢LOW Impedance	20
I/O READ FROM REGISTER	↑ N_ACK	9
I/O READ FROM REGISTER	IPDbus' LOW➢HIGH Impedance	12

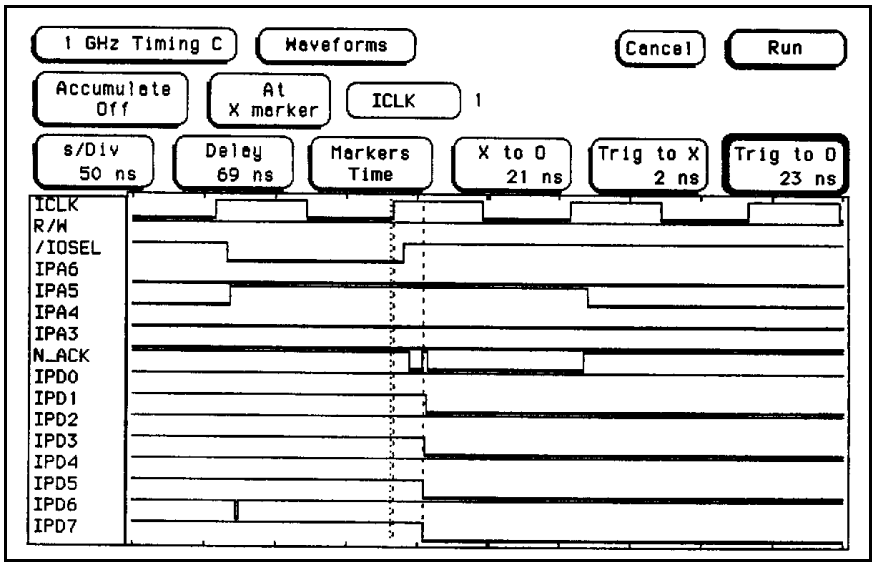


Figure 5-18 **I/O READ From SRAM**

5.4 ID Transfers

There are three variations of ID transfers for the TESTIP, not including random-wait cycle insertions. They are: ID READ (only) in the lower half of the address map, ID WRITE (high byte, low byte, and full word) to SRAM, and ID READ (high byte, low byte, and full word) from SRAM. For the first tests (READ-only section) the TESTIP resided on the MVME162 card; while it was placed on the VMESC5 carrier for accesses to and from SRAM. 7 presents some typical event times (in nanoseconds), all of which are relative to the immediately-preceding rising edge of the ICLK. 18 presents the timing for the first instance of IPDbus transitioning from high impedance to low impedance for a READ of "PROM" data 00 *hex* from the location IPA=08 *hex* (Low byte drive ID). Figure 5-4 presents the timing for an ID WRITE-to-SRAM of 69 *hex* at the IPA=30 location. As a note of interest, the quiescent states for IPA[6:1] on the MVEM162 card are low, while they are high on the VMESC5 carrier.

Table 5-7 **TESTIP Typical ID Access Times**

Function/Operation	↑ ICLK until	Time (ns)
I/D WRITE TO SRAM	↓ N_ACK	11
I/D WRITE TO SRAM	↑ N_ACK	9
I/D READ FROM SRAM	↓ N_ACK	11
I/D READ FROM SRAM	IPDbus' HIGH➢LOW Impedance	20
I/D READ FROM SRAM	↑ N_ACK	9
I/D READ FROM REGISTER	↓ N_ACK	11
I/D READ FROM REGISTER	IPDbus' HIGH➢LOW Impedance	19
I/D READ FROM REGISTER	↑ N_ACK	9

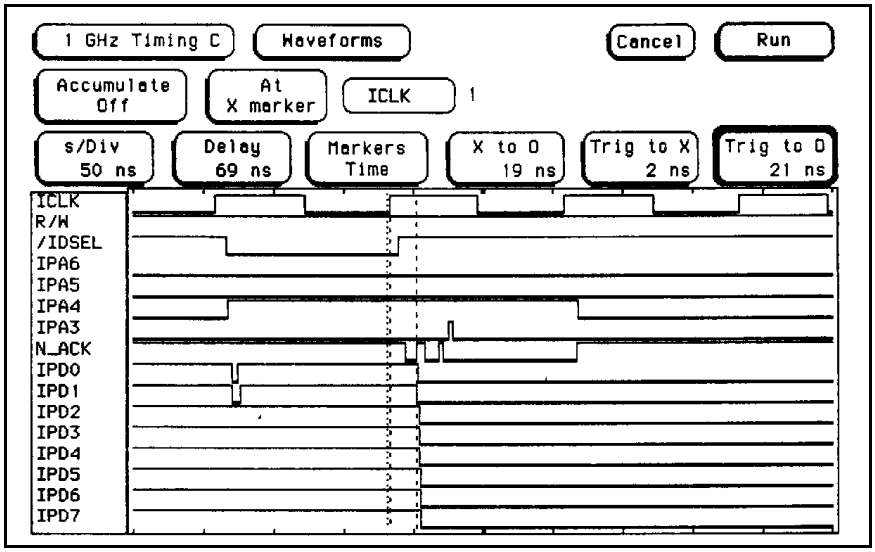


Figure 5-19 **ID "PROM" READ**

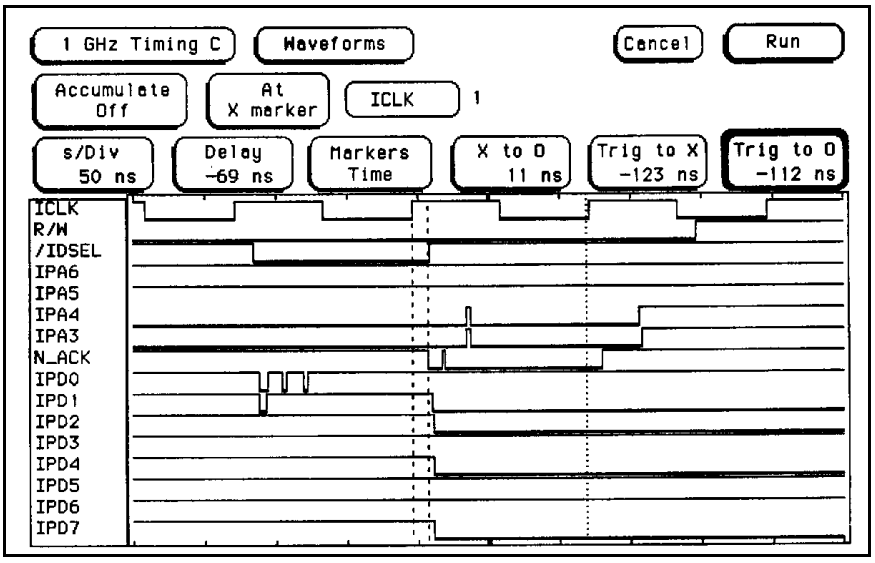


Figure 5-20 **ID WRITE to SRAM**

5.5 Memory Transfers

There are two variations of MEMORY transfers for the TESTIP, not including random-wait cycle insertions. They are: MEMORY WRITE (full word, low byte, and high byte) to SRAM, and MEMORY READ (full word, low byte, and high byte) from SRAM. The TESTIP was placed on slot A of the MVME162 card for these tests. Table 5-3 presents some typical event times (in nanoseconds), all of which are relative to the immediately-preceding rising edge of the ICLK. Figure 5-5 presents the timing for the last instance of IPDbus changing from its high-impedance states to low impedance for a READ of #69 *hex* from the location BASE+000008 *hex*, IPD[15:0]=00 and IPA[6:1]=04 *hex* (IPD[15:0]=IPA[22:7] extended addressing).

Table 5-8 **TESTIP Typical MEMORY Access Times**

Function/Operation	↑ ICLK until	Time (ns)
MEMORY WRITE TO SRAM	↓ N_ACK	11
MEMORY WRITE TO SRAM	↑ N_ACK	9
MEMORY READ FROM SRAM	↓ N_ACK	11
MEMORY READ FROM SRAM	IPDbus' HIGH➢LOW Impedance	23
MEMORY READ FROM SRAM	↑ N_ACK	9

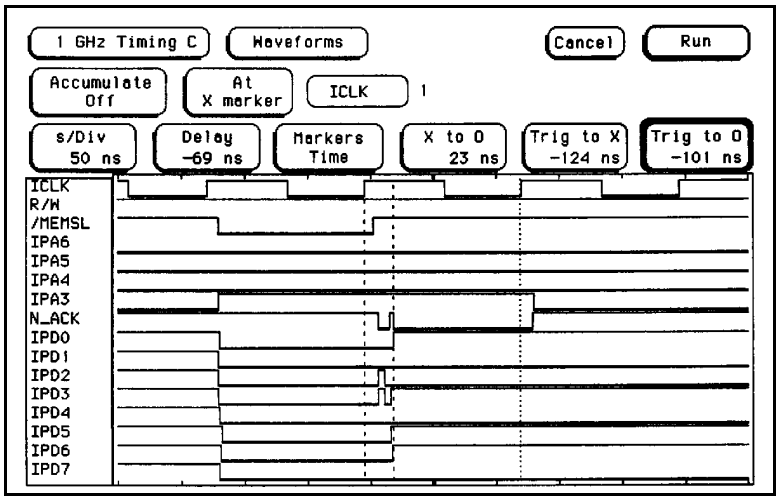


Figure 5-21 **MEMORY READ From SRAM**

5.6 Interrupts, Transfers and Waits

This subsection presents information on three related topics: Interrupt generation and reception, interrupt vector READ transfers, and (due to capturing techniques) wait-cycle insertions. The TESTIP is capable of generating two different “local” interrupt requests; they are generated by software WRITEs to the interrupt-control register in the I/O space via the carrier. The TESTIP can also generate two simultaneous “global” interrupt requests; they are generated by the reception of a low pulse, that spans a rising edge of ICLK, on the I/O connector’s N_GII (asserted low Global-Interrupt Input) line. This global request can be self-generated by a WRITE to the interrupt-control register and the installation of a jumper-shunt on J2, with the signal being passed along to other TESTIP’s or devices needing global synchronization via either of the solder donut holes (M904 or M905), or by pin #1 on the I/O connector.

5.6.1 Requests

The architecture and design of the interrupt engine on the TESTIP ensures that it was fast. Due to the modular approach and synchronous design techniques, the interrupt requests that are generated toward the carrier are very fast, with timing parameters that are independent of request type (local versus global). The timing measurements presented in 9 were conducted with the TESTIP residing on slot A of the MVME162 card, and with a jumper-shunt installed on J2 for the implementation of self-reception of a global-interrupt request. The latter configuration item is the cause for a no-skew global-interrupt-request input with respect to the output. If this TESTIP were a slave to another device in a different chassis generating the global-interrupt-output signal, then the asserted low 250 ns pulse on N_GII could be completely asynchronous to ICLK. As with all tables in this section, the event times are in nanoseconds, relative to the immediately-preceding rising edge of the ICLK.

Table 5-9 **TESTIP Typical Interrupt Request Times**

Function/Operation	↑ ICLK until	Time (ns)
LOCAL REQUEST #0	↓ N_IRQ0	4
IGLOBAL REQUEST #0	↓ N_IRQ0	4
NEGATION OF REQUEST #0	↑ N_IRQ0	4
LOCAL REQUEST #1	↓ N_IRQ1	5
GLOBAL REQUEST #1	↓ N_IRQ1	5
NEGATION OF REQUEST #1	↑ N_IRQ1	4
GLOBAL REQUEST ASSERTION	↓ N_GIO	12
GLOBAL REQUEST NEGATION	↑ N_GIO	10
GLOBAL INTERRUPT PULSE WIDTH	n/a	250

21 presents some of the events in 9. It does not show the individual interrupt request negation events. As indicated above, this snapshot presents a self-generated global-interrupt request.

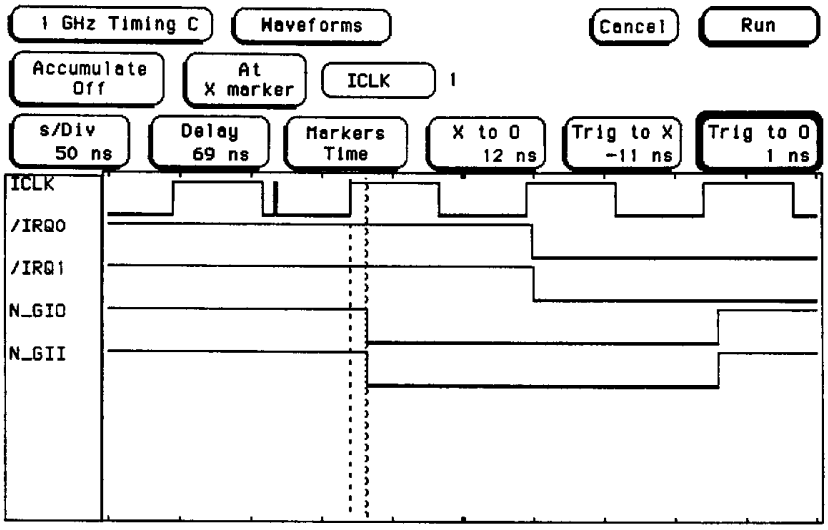


Figure 5-22 **Global Interrupt Requests**

5.6.2 Vector READS

The first event that typically occurs when servicing an interrupt request is the fetch of the interrupt vector. This is the last type of IPack transfer, consisting of a simple (low byte, and full word) READ of one of two locations on the TESTIP. The TESTIP was placed on the VMESC5 carrier for these tests. 10 presents some typical event times (in nanoseconds), all of which are relative to the immediately-preceding rising edge of the ICLK.

Table 5-10 **TESTIP Typical INTERRUPT VECTOR READ Times**

Function/Operation	↑ ICLK until	Time (ns)
INTERRUPT VECTOR READ	↓ N_ACK	12
INTERRUPT VECTOR READ	IPDbus' HIGH➢LOW Impedance	20
INTERRUPT VECTOR READ	↑ N_ACK	11

5.6.3 Wait Cycles

23 presents a single interrupt vector READ transfer (see section 5.6.2) with inserted wait cycles. As with 21, this was captured while using the TESTIP on the VMESC5 carrier. It clearly depicts a typical (interrupt-vector READ) transfer with wait cycles inserted by the IPack; seven (the maximum possible from the TESTIP) of them in this case. This equates to the longest time envelope for a transfer from the TESTIP: 1.125 μs. The number of rising edges of ICLK between the end of the select cycle and before the termination cycle determines the number of inserted wait cycle. Note that the value of 1.124 μs on figure 5-7 for this timing is a resolution error due to the 200 ns/division scale selected for this sampling. The top portion of figure 2-8 provides the user with additional information regarding wait-cycle insertions.

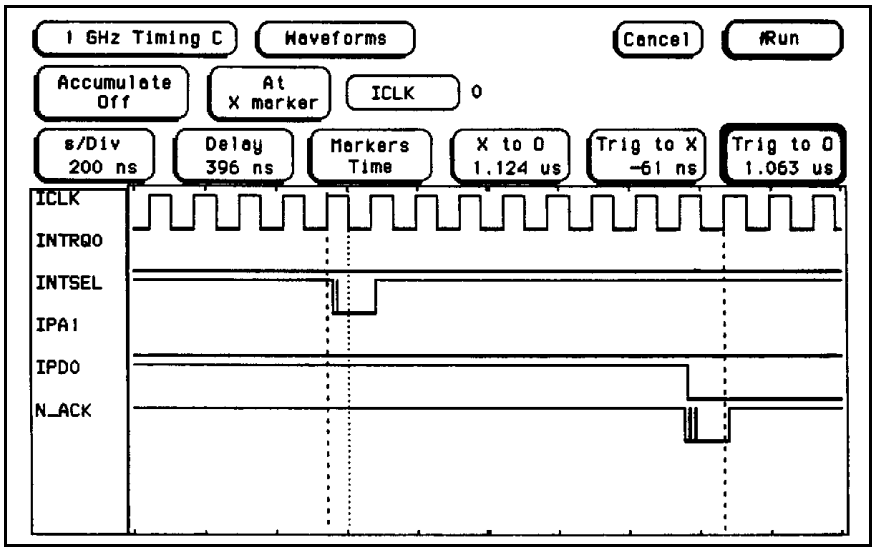


Figure 5-23 **INTERRUPT VECTOR READ with WAIT CYCLES**

5.7 Performance Timer

Several performance timer tests were conducted for the development of table 5-6. The TESTIP was placed in slot A on the MVME162 card for these tests. Note that the last four table entries reflect another “I/O READ” transfer, similar to the last four items in table 5-1. The first table entry was obtained by monitoring the “Carry” signal at test point TP1. This signal is periodic as long as the timer is running. The second entry is a variation on the positive pulse generation application presented in Section 6.3. It was developed using the resident “162BUG” command “MM FFF58074” which performs a WRITE followed by a READ-AND-VERIFY operation which turned on the timer and turned it off again in the time tabulated.

Table 5-11 **TESTIP Typical TIMER Times**

Function/Operation	↑ ICLK until	Time (ns)
TIMER CARRY PULSE WIDTH	n/a	1000
162BUG ⇒ BUSY PULSE WIDTH	n/a	33410
TIMER ON "BUSY" ASSERTED	↑ BUSY	5
TIMER OFF "BUSY" NEGATED	↓ BUSY	6
TIMER* READ FROM REGISTER	↓ N_ACK	11
TIMER* READ FROM REGISTER	IPDbus' HIGH➢LOW Impedance	21
TIMER* READ FROM REGISTER	↑ N_ACK	10
TIMER* READ FROM REGISTER	IPDbus' LOW➢HIGH Impedance	12

* READ-ON-THE-FLY data = D76Ahex.

6.0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the TESTIP to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the SYSTRAN team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and SYSTRAN reserves the right to modify submissions to provide for more generic appeal, when necessary.

While the normal utilization of the TESTIP encompasses various aspects of IPack carrier testing functions, it can also be used in operational systems, as described in the following not-so-obvious applications.

6.2 111 Location Scratchpad

In many data acquisition system applications the need often arises for storage of important parametric and special-event information in a “memory” region that is globally accessible by more than one bus master. Most bus-based CPU boards have more than adequate amounts of on-board private memory for operating system and application program storage, as well as for data manipulation and data storage purposes. Some of them even have shared-memory regions that are bus-wide accessible. If system requirements dictate the need for a small amount of shared data base, the TESTIP can fulfill the requirements, circumventing the costs of adding a bus-based memory board. Actually, 89 locations are available as two separate blocks of “memory” while the remaining 22 locations are scattered throughout a third region of locations.

These 111 locations may or may not all be accessible, depending upon the level of compliance to the IPack specification given by the carrier(s) being used. There are two instances where locations will not be usable as “memory”:

- If a carrier does not support WRITEs via ID transfers, then 32 locations will not be usable.
- If a carrier does not support the seldom-used memory transfer, then 22 locations will not be usable.

Figure 6-1 describes how 79 of the 111 memory locations of the TESTIP may be used on Motorola’s MVME162-xx carriers in slot 4. The 32 ID “memory” locations are not accessible. Figure 6-2 describes how 89 of the 111 memory locations may be used with SYSTRAN’s VMESC5 carrier. The 22 MEMORY-transfer “memory” locations are not accessible when using this carrier since it does not support the seldom-used memory transfers.

```
Memory location interpretation:

  @ FFFFBC004 write 'C000', and
  @ FFFFBC006 write '00000': to establish
      an IPack Memory region with a base
        address @ 'C0000000'.

  @ FFFFBC00C write '7F00': to establish
      an 8MByte memory size for the TESTIP.

  @ FFFFBC018 write '0900': to establish
      16-bit width operations and to enable
        accesses to this region.

  Memory read & write "word" locations @:

  C0000002, C0000004, C0000008, C0000010,
  C0000020, C0000040, C0000080, C0000100,
  C0000200, C0000400, C0000800, C0001000,
  C0002000, C0004000, C0008000, C0010000,
  C0020000, C0040000, C0080000, C0100000,
  C0200000, & C0400000.

    Note: while N_MEMSEL assertions will occur over the
          full addressing range of C0000000 -> C07FFFFE
            the TESTIP will only respond to the addresses
              listed above.

"I/O"-TRANSFER AREA: { 57 locations }

  SLOT A: | SLOT B: | SLOT C: | SLOT D:
          |         |         |
  FFF580000| FFF581000| FFF582000| FFF583000
    through |   through |   through |   through
  FFF580070| FFF581070| FFF582070| FFF583070
          |         |         |

    Note: the EPLD-based I/O registers reside at addresses
          ranging from FFF58x72 -> FFF58x7E.
```

Figure 6-24 **79 Memory Locations on the MVEM162-xx**



Figure 6-25 **89 Memory Locations on the VMESC5**

6.3 Bipolar Pulse Generation

The TESTIP is capable of providing a single line of programmed I/O digital output of a high-current, TTL-level type. Besides fixed low or high states, software can also implement high- or low-pulse outputs. This capability is only available if the built-in performance timer is not being used in the application.

Pin #5 of the TESTIP's I/O connector is designated as the "BUSY" output. It is asserted high when the performance timer is running, and negated low when it is stopped. The starting and stopping of the timer is implemented via WRITEs to and READs from the I/O register controlling the timer (typically addressed as base+074), respectively.

Figure 6-3 presents how a positive, programmable width, pulse can be generated on pin #5 of the I/O connector. It also provides how this may be used as a steady-state output pin. The example provides the specific addressing required for a TESTIP residing on a MVME162-01 board in slot A.

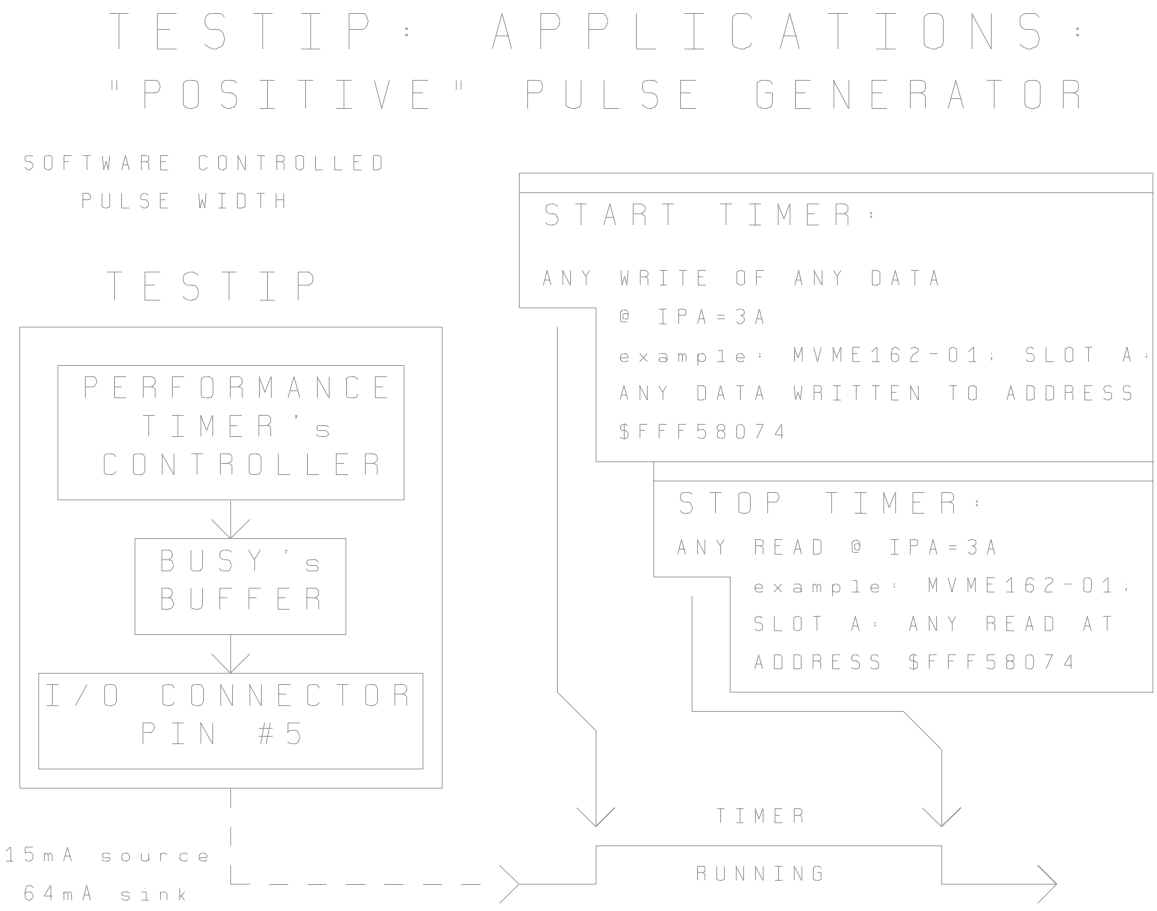


Figure 6-26 **"Positive" Pulse Generation**

Figure 6-4 presents how a negative pulse can be generated on pin #5 of the I/O connector. This method decouples dependency on application software to provide pulse-width-duration control as it becomes simply a function of how fast a particular CPU can perform a “READ/MODIFY/WRITE” operation. This does not preclude the ability to provide software-controllable pulse width for the negative-pulse-generation scheme. By inverting the scheme presented in figure 6-3; by first reading, waiting, and then writing to the timer’s control register, a programmable negative-pulse-width may be obtained on this output.

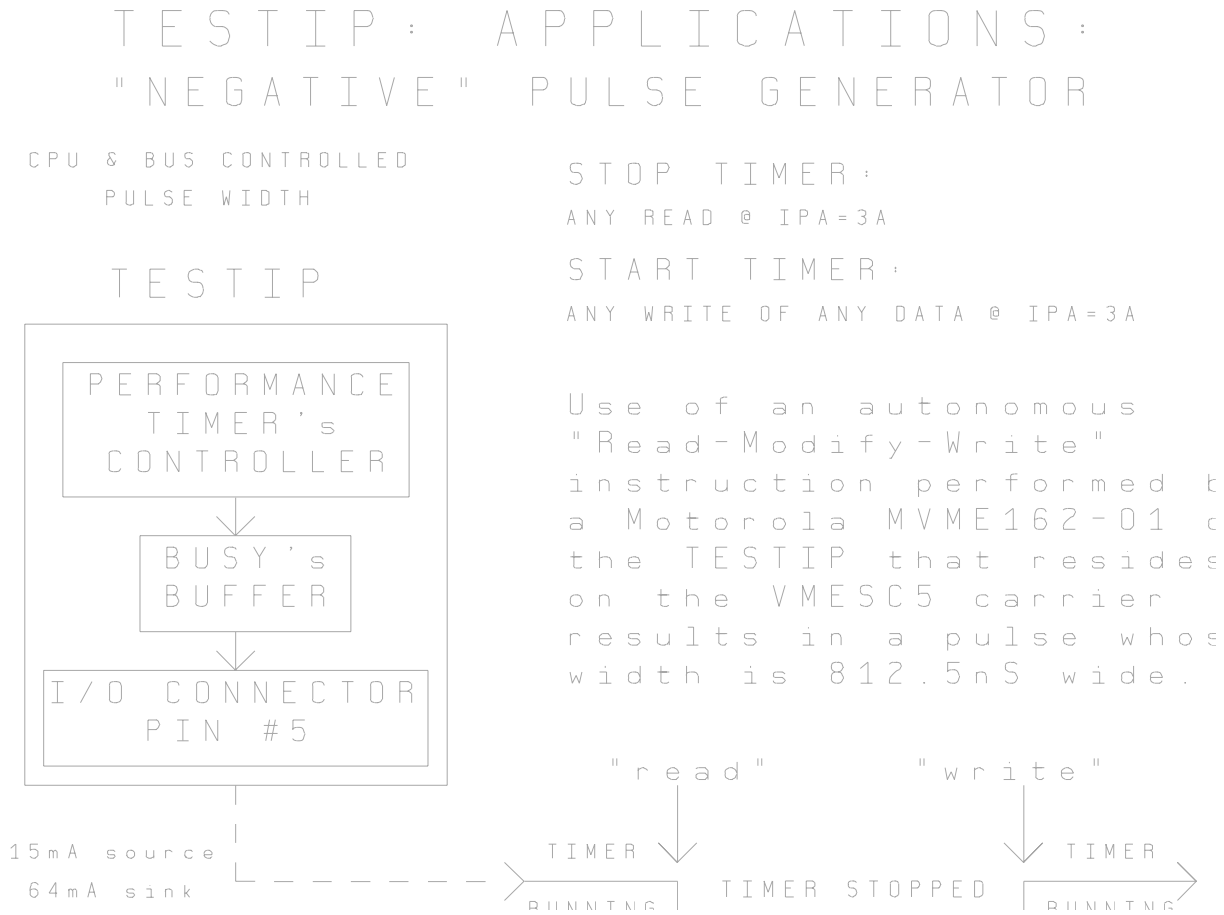


Figure 6-27 **“Negative” Pulse Generation**

6.4 200 Simultaneous Interrupts

When evaluating various CPU boards and/or operating systems for their “real-time” capabilities, one of the more important parameters to consider is the ability to respond quickly to multiple sources of interrupts. Since system architectures are as varied as the number of system developers, it is difficult to create a test scenario that will do all things for all people. For instance, some systems are loaded heavily with many processors sharing I/O resources, while others may have a single CPU supporting a rack full of I/O. Of these two extremes, the latter configuration presents the possibility of a significant number of interrupts to be handled by any single CPU. This application presents a system architecture that is capable of generating two hundred (200) simultaneous (to within a few nanoseconds) interrupts to be handled by a single CPU's interrupt handler. This configuration provides the means to test various pieces of hardware (different CPU cards running the same software) and candidate operating systems (one CPU board running different software packages) for fairly analyzing the best system performer.

Not all IPack carriers are as flexible as the VMESC5. For instance, some carriers only provide the ability to generate a single interrupt level for all interrupt sources on a single carrier. Some require that higher-priority-interrupt sources be placed in specific slots on the carriers. Some carriers provide the user with the ability to change the interrupt level via changes in programmable logic. While these restrictions exist for some carriers, there are no restrictions of any kind when using the VMESC5 carrier.

Of course, the significant advantage of the VMESC5 carrier is that it provides the highest density IPack support possible. What is not obvious is the versatile interrupt support and very high throughput capacity of this carrier. There are ten potential interrupt sources per VMESC5 carrier, two per IPack. The VMESC5 provides the user with the ability to assert any one of the seven valid VME interrupt levels per IPack interrupt source.



NOTE: If all ten interrupt levels on any given VMESC5 were programmed to be the same, then the position of the IPack becomes significant in that the interrupt #0 in slot A is serviced first, followed by #1 in slot A, #0 in slot B, #1 in slot B, in this order to #1 in slot E

The TESTIP was designed to test a carrier’s and a system’s ability to deal with simultaneous interrupts. The physical implementation is depicted in the following two diagrams. Figure 6-5 presents a top view of a VMESC5 carrier with five TESTIP IPacks installed. The significant point concerning this diagram is the daisy-chain wiring of the “global” interrupt. The “Daisy#1” wire is from the bottom IPack of the preceding carrier, while the “Daisy#2 wire goes to the top IPack of the succeeding carrier. Exceptions to this scheme are the first and last carriers in the system. Additionally, the first TESTIP in the daisy-chain will need to have a shorting-header installed at J2 to enable the generation of the global interrupt on the first IPack to itself. After all of the interrupt levels have been programmed (200 locations) in the carrier’s registers, and after all of the TESTIP’s interrupt vectors have been programmed into the last two I/O locations of each TESTIP (200 locations), a single WRITE to the global-interrupt bit at the first TESTIP starts the test.

Figure 6-6 provides a full-chassis view of the system configuration.

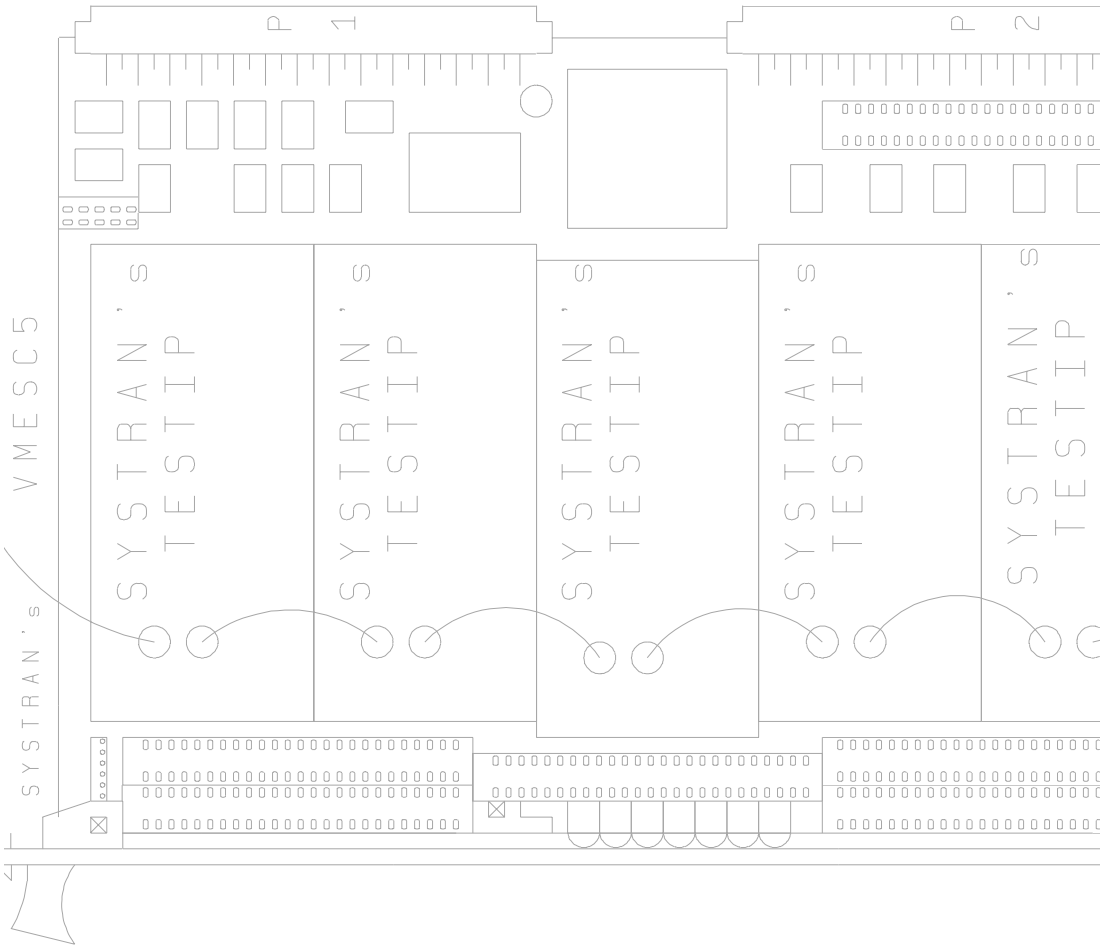


Figure 6-28 **TESTIPs' Global Interrupt Daisy-Chain Detail**



Figure 6-29 **100 TESTIP's on 20 VMESC5 Carriers**

7.0 WARRANTY AND REPAIR

THE FOREGOING WARRANTIES ARE IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ANY WARRANTY THAT EQUIPMENT PURCHASED HEREUNDER IS OF MERCHANTABLE QUALITY.

7.1 Warranty and Repair

SYSTRAN makes no warranty of any kind, express or implied, with regard to products, except that SYSTRAN warrants that products delivered will be free from defects in materials or workmanship for a period of three hundred sixty five (365) days from the date of original shipment. During the warranty period, SYSTRAN will provide, free of charge to Buyer, the Warranty Services defined below:

7.2 Hardware Warranty Service

Hardware Warranty Service consists of factory exchange or repair (at SYSTRAN's sole option) of defective Hardware Products to correct malfunctions which occur during normal use. In the event SYSTRAN decides to replace a failed part or piece of equipment, SYSTRAN shall have the right to replace it with either a new part or piece of equipment, or factory reconditioned part or piece of equipment. Replaced parts or pieces of equipment become the property of SYSTRAN.

Hardware Warranty Services do not include the repair or replacement of equipment or parts which have otherwise become defective, including, but not limited to, damage caused by accidents, modifications or alterations by Buyer, physical abuse or misuse, operation in an environment or conditions outside SYSTRAN's specifications for the Hardware Products, acts of God, and fires. Hardware Warranty Services also exclude labor and material cost of relocation, rearrangement, additions to, and removal of Hardware Products.

Buyer must report hardware malfunction to SYSTRAN Customer Service and obtain a Return Authorization Number. Defective hardware should then be shipped prepaid to SYSTRAN. Repair or replacement will then be returned prepaid upon receipt of the defective item.

7.3 Software Warranty Service

Software Warranty Service consists of update services covering changes to any combination of documentation and software required to maintain Software Products at the revision level most currently released by SYSTRAN. This Software Warranty Service does not include changes or upgrades, or options intended to broaden, enhance or improve the capabilities of the Software Product.

7.4 Other Services

Also included in the Warranty Services for the covered Products are periodic newsletters announcing new products and applications, and application notes.

7.5 Additional Paid Services

Should Buyer request services which are beyond the scope of the Hardware, Software or Other Warranty Services specified above, these will be provided by SYSTRAN on a time-and-materials basis at the prices in SYSTRAN's published Price List. Such services will then be undertaken by SYSTRAN after SYSTRAN has given Buyer an estimate of the services required and only after SYSTRAN receives written authorization from Buyer.

7.6 Term

This Warranty is effective for a period of three hundred sixty five (365) days from the date of the original shipment.

7.7 Condition

Services provided under this Warranty are performed at the SYSTRAN factory, Monday through Friday, 8:00 a.m. through 5:00 p.m. Eastern Standard/Daylight Savings Time, excluding SYSTRAN's holidays. SYSTRAN's performance goal is to ship to Buyer a repaired or replacement Hardware Product within 48 hours of SYSTRAN's receipt of the defective Hardware Product.

7.8 Identification of Covered Products

Products covered by this Agreement shall be identified by their SYSTRAN Serial Numbers which will be affixed on the respective product.

7.9 Shipping

When factory repair services are required, Buyer shall ship or deliver products, freight prepaid, to the SYSTRAN factory. SYSTRAN will return Products, freight prepaid, to Buyer. SYSTRAN reserves the right to select the carrier and shipping method for return shipments. Upon request, Products will be shipped by Buyer's carrier or by a Buyer-specified shipping method for return shipments. Any shipping charges incurred by SYSTRAN for such Buyer-specified shipping will be invoiced separately to Buyer.

7.10 Life Support and Nuclear Policy

SYSTRAN products are not authorized for and should not be used as critical components in life support systems or nuclear facility applications without the specific written consent of SYSTRAN Corp. As used herein:

- Life support devices or systems are those which support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.

- Examples of nuclear facility applications are those (a) in a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing, or disposal of fissionable material or waste products thereof.

SYSTRAN's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages. Buyer uses or sells such products for life support or nuclear facility applications at Buyer's own risk and agrees to defend, indemnify, and hold SYSTRAN Corp. harmless from any and all damages, claims, suits, or expense resulting from such use.

7.11 Communication

Contact SYSTRAN Customer Support by calling (513) 252-5601, or send an E-Mail message to **support@systran.com** for assistance.

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APPENDIX A
IP Specification Synopsis

SYSTRAN CORPORATION'S

IP SPECIFICATION SYNOPSIS

of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:

This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small formfactor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general-purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high-speed (32 MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system-level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP" , and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8 MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a doublewide board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8 MHz-clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9″ by 1.8″ size allows for convenient modular placement of 1, 2, 4, 5, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME3U, Nubus, VME6U, ISA, "C" size VXIbus, and VME9U, as well as stand-alone (embedded processor) carriers of various sizes. A doublewide IP is 3.9″ by 3.6″ in size, and appears mechanically and electrically as two singlewide IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:

The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the "I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted-low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0 mA (logic low) in parallel with 30 ρF. All signals have a 10 KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK

This signal, ≡ CLK in the specification, is an 8 MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's logic connection is via pin 2. The loading is 6.0 mA (logic low) maximum in parallel with 30 ρF.

IPA[6:1] (Address bus)

These six lines, ≡ A1... A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for singlewide boards, and 32-bit data boundaries for doublewide boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as this is defined by individual select lines from the carrier.

IPD[15:0] (Data bus)

These sixteen lines, ≡ D00... D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus = IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For doublewide IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but may use IPD[15:0]. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET
This signal, ≡ RESET★ in the specification, is the asserted-low reset signal. The carrier is required to assert N_RESET for a minimum of 200 ms following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)
This signal, ≡ R/W★ in the specification, is the data-direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)
This signal, ≡ ACK★ in the specification, is the asserted-low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier-driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)
N_BS1 (high Byte Select)
These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted-low byte-select lines driven by the carrier to the IP to indicate which byte-lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low (odd) byte, IPD[7:0], while N_BS1 selects the high (even) byte, IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes, IPD[15:0], are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)
This signal, ≡ MemSel★ in the specification, is the asserted-low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. Doublewide IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)
This signal, ≡ IOSel★ in the specification, is the asserted-low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. Doublewide IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)
This signal, ≡ IntSel★ in the specification, is the asserted-low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. Doublewide IPs may respond with a-side only or b-side only transfers. A transfer involving both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)
This signal, ≡ IDSel★ in the specification, is the asserted-low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For doublewide IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)
N_INTREQ1 (INTerrupt REQuest #1)
These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are the asserted-low interrupt request signals driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:
The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin 34. Pin 36 is a reserved pin, as is pin 49. DMAEnd★ is found at pin 38. Error★ is found at pin 40; and Strobe★ is found at pin 46.

POWER/GROUND:
+5 volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero-volts reference, comes in pins 1, 25, 26, and 50; +12 volts is sourced via pin 23, and, -12 volts comes in pin 22.

CYCLE TYPES:
There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two (in the case of a doublewide IP) select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal(s). A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the (first) select cycle. Idle cycles are those between terminate and select cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:
There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:
Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both singlewide and doublewide IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:
The outside dimensions of a singlewide IP are 1.800″ by 3.900″, +.000/-.020″. The outside dimensions of a doublewide IP are 3.600″ by 3.900″ , +.000/-.020″ . There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the logic interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8″ by 3.188″ between the connectors for a singlewide IP, and 3.6″ by 3.188″ for a doublewide IP. The maximum height of components on the IP is 0.315″ , with components exceeding 0.250″ in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush-cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500 VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high-shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70° C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40° C up to +85° C.

ADDITIONAL INFORMATION:
The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 181 Constitution Drive, Menlo Park, CA 94025.

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MEMORY TRANSFERS: CYCLE TABLES

CYCLE:	MEM WRITE NO HOLDS NO WAITS			MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS						MEM WRITE 1 HOLD 3 WAITS									DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15:0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH @ END OF:			◇					◇			◇											◇					

CYCLE:	MEM READ NO HOLDS NO WAITS			MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS					MEM READ 1 HOLD 3 WAITS						DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15:0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND:

* IPD[15:0] = IPA[22:7] during the SELECT cycle, and is used for data for all other cycles.

X DON'T CARE

Z HIGH IMPEDANCE

1 HIGH STATE, +5v

0 LOW STATE, GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPack

◇ IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

ID TRANSFERS: CYCLE TABLES

CYCLE:	ID READ NO HOLDS NO WAITS			ID READ NO HOLDS 2 WAITS					ID READ 3 HOLDS NO WAITS					ID READ 1 HOLD 3 WAITS						ID READ 2 HOLDS 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7:0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	0	1	✓	
N_IDSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1		✓

GENERAL LEGEND:

X DON'T CARE

Z HIGH IMPEDANCE

1 HIGH STATE, +5v

0 LOW STATE, GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPack

INT TRANSFERS: CYCLE TABLES

CYCLE:	INT READ NO HOLDS NO WAITS			INT READ NO HOLDS 3 WAITS					INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS						INT READ 1 HOLD 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	TERM	IDLE	IPack	CARRIER
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	X		✓
IPD[7:0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	←	X	Z	Z	Z	←	←	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

* IPA1 CAN BE IGNORED IF ONLY ONE INTERRUPT IS SUPPORTED (must be at LEVEL 0).

** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH.

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

I/O TRANSFERS: CYCLE TABLES

CYCLE:	I/O WRITE NO HOLDS NO WAITS				I/O WRITE NO HOLDS 3 WAITS					I/O WRITE 2 HOLDS NO WAITS					I/O WRITE 3 HOLDS 1 WAIT						DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	IDLE	SELECT	WT&HLD	HOLD	HOLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPD[15:0]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
DATA LATCH @ END OF:			◇						◇			◇										◇					

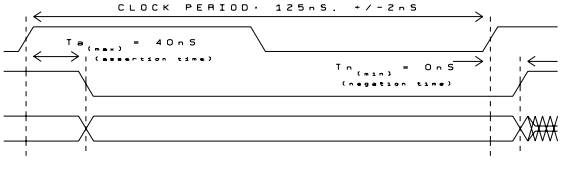
CYCLE:	I/O READ NO HOLDS NO WAITS				I/O READ NO HOLDS 2 WAITS				I/O READ 3 HOLDS NO WAITS					I/O READ 2 HOLDS 3 WAITS					I/O READ 3 HOLDS 2 WAITS						DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WT&HLD	WAIT	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15:0]	X	Z	←	X	Z	Z	Z	←	X	Z	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←	✓	
IPR/N_W	X	1	1	X	1	1	1	1	X	1	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1		✓

GENERAL LEGEND:

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE: +5v
- 0 — LOW STATE: GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPack
- ◇ — IPack LATCHES AT END OF CYCLE

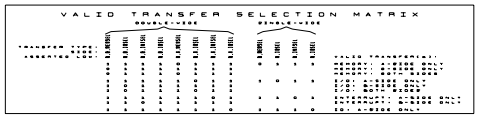
WAITS ARE INVOKED BY THE IPACK.
HOLDS ARE INVOKED BY THE CARRIER
SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

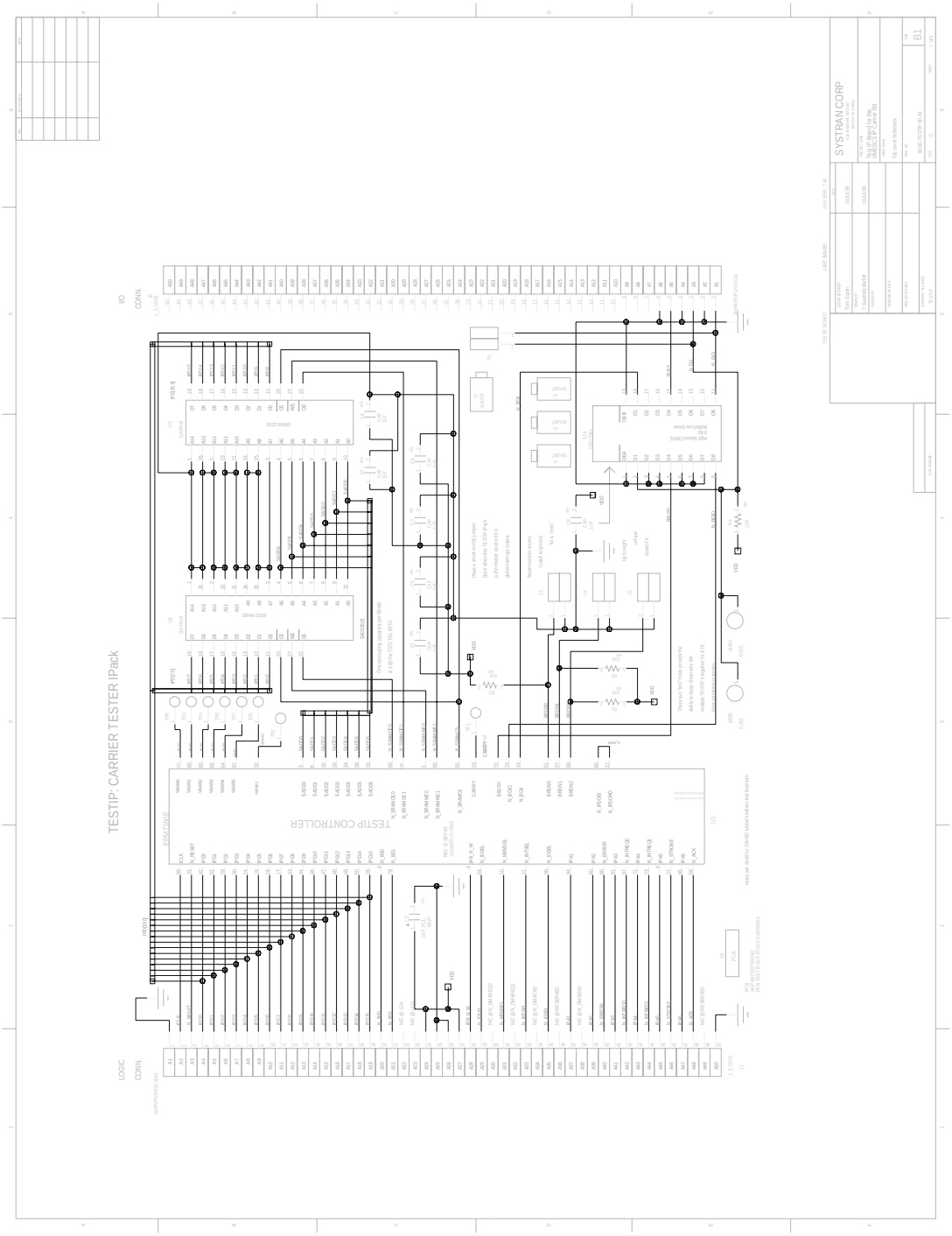
VALID TRANSFER SELECTION MATRIX



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B-T-SH-IPACKSUM-A-0-A3 (11/13/96)

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APPENDIX B
SCHEMATICS


TESTIP: CARRIER TESTER IPack
I/O CONN.
LOGIC CONN.
TESTIP CONTROLLER
SYSTRAN CORP

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