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V64XSC4

VME64 Extensions 6U
Slave 4-Slot IP Module Carrier
Hardware Reference

Document No. B-T-MR-V64XSC4#-A-0-A2

CURTISS WRIGHT Controls, Inc.
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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This reference manual covers the physical, operational, and performance characteristics of Curtiss-Wright Controls' VME64 Extensions 6U 4-Slot Slave IP Module Carrier and Transition Module. The part number of the carrier is BHAS-V64XSC4 and the part number of the transition module is BHAS-V64XT4L. Hereafter, we will refer to the IP Module Carrier as V64XSC4, or simply as the "carrier", and its accompanying transition module as V64XT4L, or as the "transition module." Supporting software information and sample applications are also included.

1.1.2 Scope

This manual describes the board features, overall board layout, data transfer types, and detailed description of the registers. To benefit from the manual you should have a general understanding of computer software and hardware applications and be familiar with IP modules.

1.1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7e.
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/). For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
C:\ls
file1          file2             file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

The following publications provide background information on the V64XSC4 and related topics.

- Curtiss-Wright Controls, Inc. I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)
- *ANSI/VITA 1–1994* published by VMEbus International Trade Association, P.O. Box 19658, Fountain Hills, AZ 85269 USA www.vita.com.
- *ANSI/VITA 4–1995* published by VMEbus International Trade Association, *ANSI/VITA 1.1-1997*
- *ANSI/VITA 4.1-1996*

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2. PRODUCT OVERVIEW

2.1 Overview

The V64XSC4 is a VME64 Extensions 6U Slave board supporting four singlewide, two singlewide and one doublewide, or two doublewide IP Modules. This carrier is limited to 8 MHz IP Modules. The V64XSC4 supports I/O, ID, Interrupt and Memory transfers on all four slots. DMA accesses are not supported.

The high-density carrier is based on a super-synchronous design with an affordable, high-performance, easy-to-use, and intuitive user interface. Since the board does not insert IP Module hold cycles, a very high throughput is achieved.

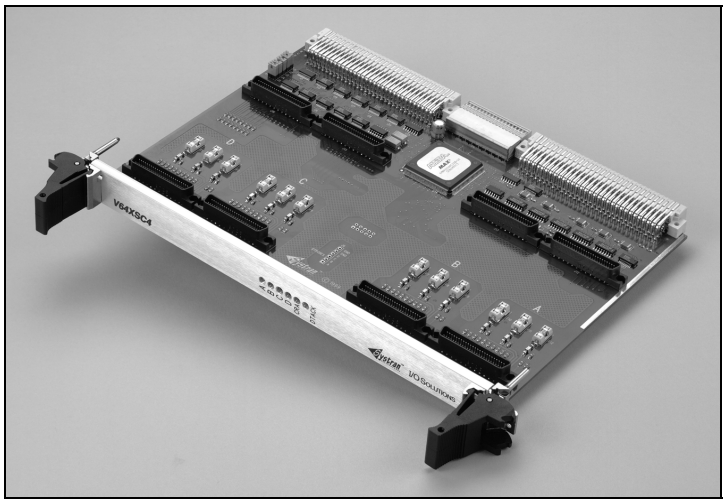


Figure 2-1 V64XSC4 Carrier Board

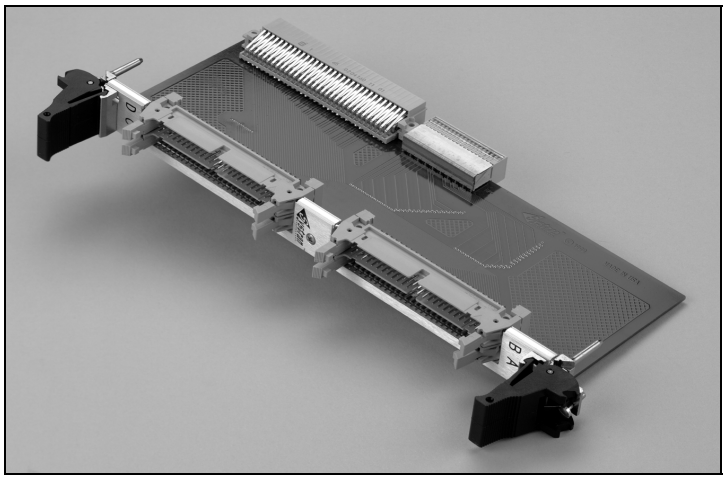
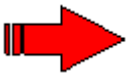


Figure 2-2 V64XT4L Transition Modules

The V64XSC4 provides up to 200 I/O points (50 per IP Module) per VME6U slot in conjunction with the transition module. The entire area under the IP Modules provides a

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solid quiet ground plane for sensitive analog IP Modules. The front panel LEDs give diagnostic information on accesses to the IP Modules, the V64XSC4 local status and control registers, and the VME DTACK. The V64XSC4 has a flexible easy-to-use a VME interrupting capability. Individual interrupts from each IP Module can be programmed to assert any VME interrupt request signal.



NOTE: Physical doublewide IP Modules are supported. However, logical doublewide 32-bit transfers are not supported.

2.1.1 Features

The V64XSC4 has the following features:

- Up to 200 I/O points in a single VME6U slot with Transition Module
- 8 IP Module interrupt requests (2 per IP Module slot)
- 7 VME interrupt levels per IP Module
- Equal level IP Module slot prioritization I/O, ID, INT and memory transfers with no HOLDs. *
- Read-Modify-Write cycles supported to IP Modules and V64XSC4 registers
- +5, +12, and -12 V power to each IP Module with independent field-replaceable fuses, and T-type filters
- IP Module error signals posted in status register
- Software resettable IP Modules.
- Jumper-selectable board base-address
- Quiet IP Module ground planes
- Four singlewide, or two singlewide and one doublewide, or two doublewide IP Modules
- Six front-panel IP Module/Carrier Access and VME DTACK indicators (with pulse stretchers)
- Four 8-bit General-purpose registers
- I/O, ID and INT 8- and 16-bit transfers in A16 space (2 KB block using address modifiers 0x29, 0x2D). Will also support memory transfers in A24 space (1 MB for each IP Module using address modifiers 0x39, 0x3D) or A32 space (8 MB for each IP Module using address modifiers 0x09, 0x0D).
- Supports Writes to ID Space

**ANSI/VITA 4-1995 used*

3. INSTALLATION

3.1 Unpack the V64XSC4 and V64XT4L

Table 3-1 lists the contents of the V64XSC4 shipping package.

Table 3-1 Contents of V64XSC4 Shipping Package

Qty	Description
1	V64XSC4 Printed Circuit Assembly (Carrier)
1	V64XT4L Printed Circuit Assembly (Transition Module)
2	Surface-mount spare fuses (one 1-Amp, one 2-Amp)
1	V64XSC4 Hardware Reference *

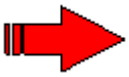
* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Curtiss-Wright Controls, Inc. or by mail. Use the prefix "BTMR-" followed by the product order part number; (for example, BTMR-V64XSC4).

The Printed Circuit Assemblies are enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Inspect the V64XSC4 and V64XT4L

Examine the V64XSC4 Carrier and V64XT4L Transition Module to determine if any damage occurred during shipping.

3.3 Install theV64XSC4 and V64XT4L



NOTE: The V64XSC4 and V64XT4L are Electrostatic Sensitive Devices. The hardware installation of the V64XSC4 and V64XT4L must be conducted on a good anti-static workbench to protect the IP Modules and carrier board.

The tools required for the V64XSC4 and V64XT4L installation are listed in Table 3-2.

Table 3-2 V64XSC4 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

3.3.1 Installation of IP Modules on the V64XSC4

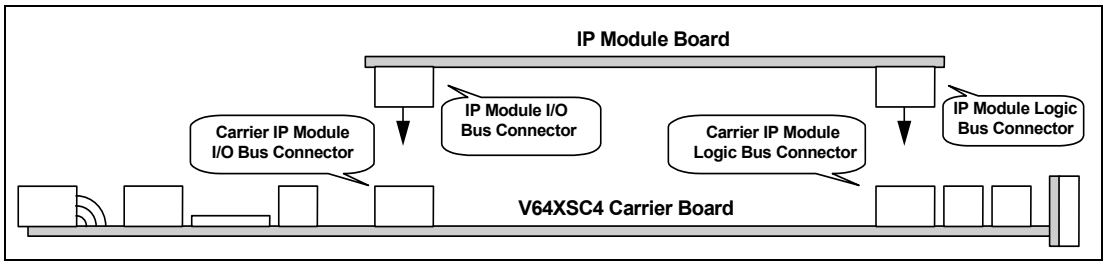


Figure 3-1 Installation of an IP Module on the V64XSC4

Referring to the appropriate figures and table described below, perform the following steps in removing the V64XSC4 from it shipping container (or from an existing installation) and installing IP Modules. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.

2a. Remove the V64XSC4 from it's shipping container, move it to the ESD controlled area, and install the IP Modules.

*2b. Remove the V64XSC4 from the VME card cage, move it to the ESD controlled area, and install the IP Modules.

3. Set the VMEbus base address on the J5-J1 jumpers (see Figure 3-3 and Figure 3-5).

4. Install the IP Module(s) onto the carrier board by applying adequate and equal pressure to the IP Module(s) at both ends and the V64XSC4 board.

*5. Install four M2x5mm flat head machine screws onto the IP Module's connectors.

6. Install the V64XSC4 into desired slot of a VME card cage.

V64XT4L TRANSITION MODULE INSTALLATION

7. Remove the V64XT4L from its shipping container.

8. Install the V64XT4L in the slot directly behind the V64XSC4 Carrier so that the I/O signals from the Carrier will connect to the Transition Module.

9. Install the necessary I/O cables onto V64XT4L.

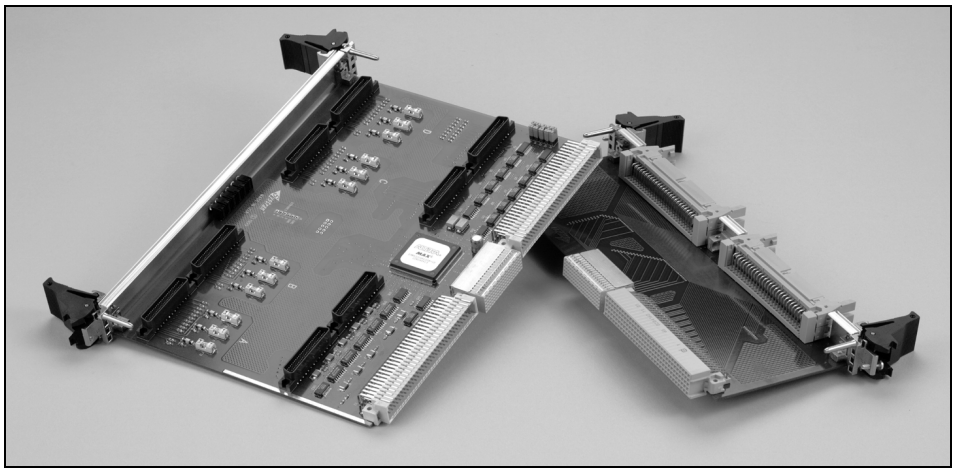


Figure 3-2 V64XSC4 and V64XT4L

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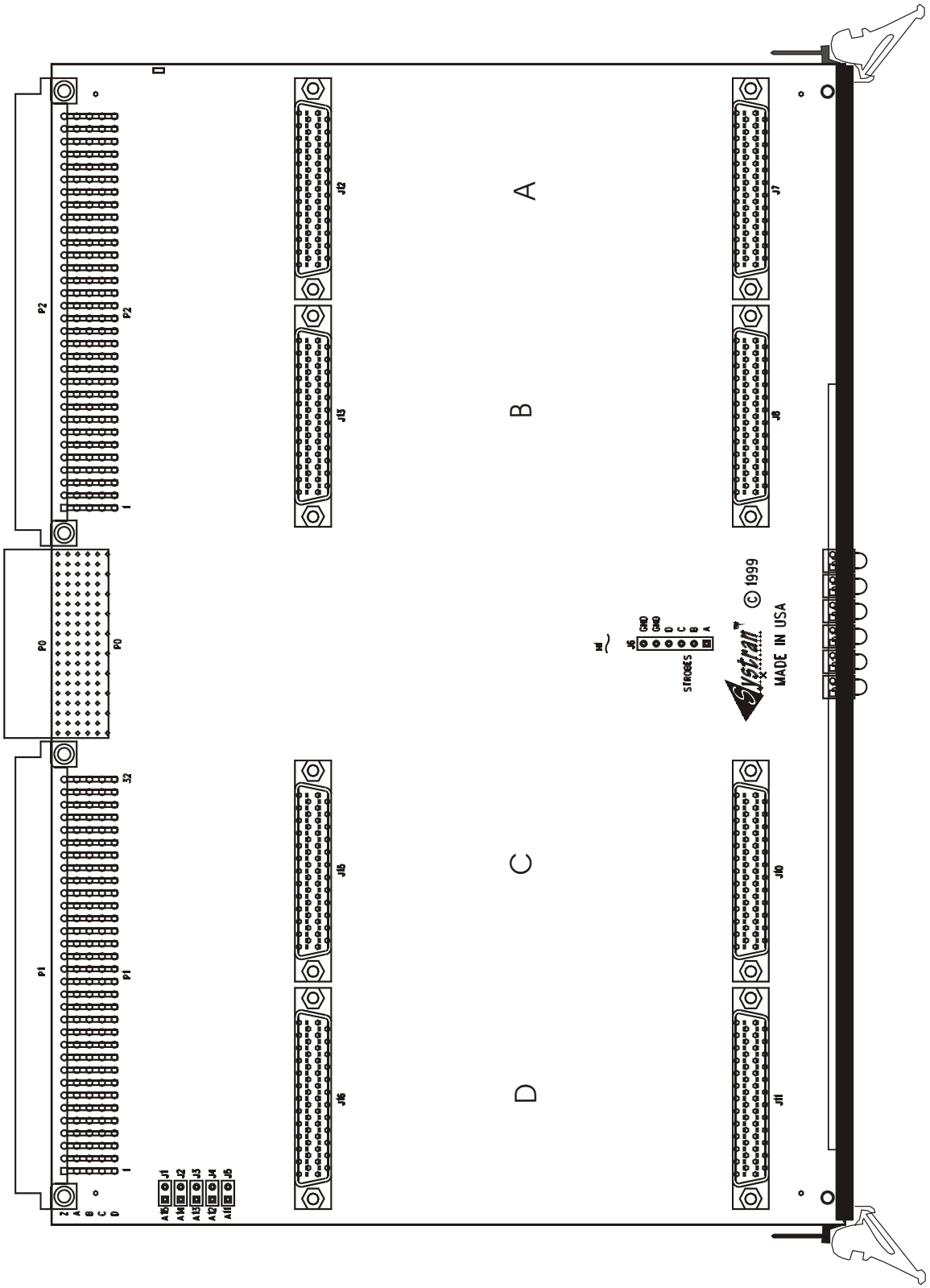


Figure 3-3 V64XSC4 Assembly Drawing

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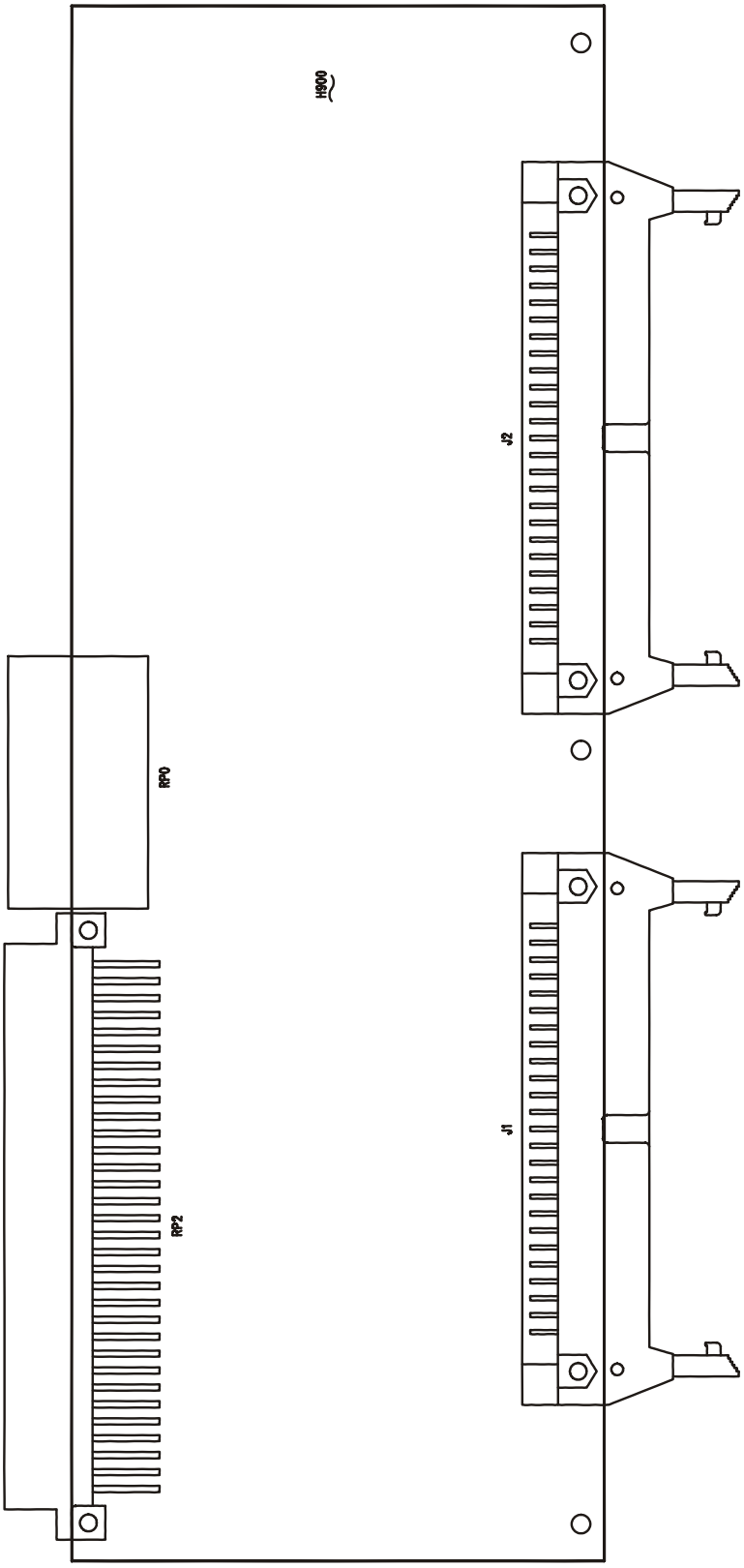


Figure 3-4 V64XT4L Transition Module

3.3.2 V64XSC4 VME Base Address

The V64XSC4 VME board base address is set with five jumpers J1–J5, corresponding to VME address bits A15 to A11, respectively. You can place the board's registers and I/O space at any one of 32 possible base addresses on 2 KB boundaries in the VME short address space.

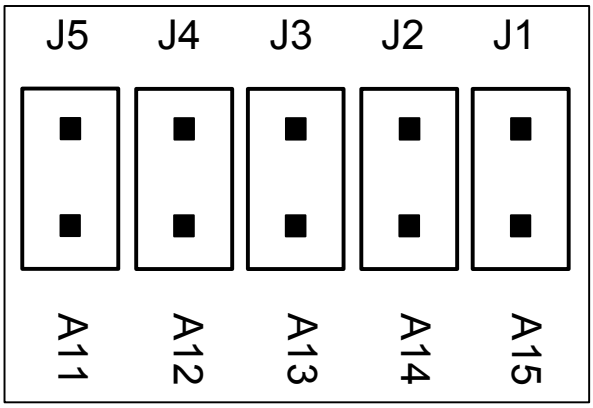


Figure 3-5 V64XSC4 Jumpers J5–J1

Placing a jumper across both posts corresponds to a logic low, or '0', for that address bit. Removing the jumper, or storing it on a single post, corresponds to a logic high, or '1', for that address bit.

NOTE: The V64XSC4 is shipped with all jumpers installed and appears in memory at address 0x0000.

EXAMPLE:

The short I/O space on the MVME162 is located from 0xFFFF0000 to 0xFFFFFFFF, so the V64XSC4 can be placed from 0xFFFF0000 to 0xFFFFF800 on 2 K boundaries.

Table 3-3 indicates all possible jumper settings for board base addressing.

Refer to Appendix B PROGRAMMING GUIDE for details of VME accesses to the V64XSC4 on-board registers or IP Modules.

NOTE: When using the MVME162 with OS-9, OS-9 maps the VMEChip2 GCSRs (Global Control Status Registers) to the beginning of short I/O space. This causes a bus conflict with boards placed at this address. To avoid a bus conflict:

1) Do not put any VME boards at locations 0xFFFF0000 to 0xFFFF0010;
2) Move the GCSR location by changing the Group Select and Board Select values in the VMEChip2 LCSR registers (the 3 bytes starting at 0xFFF4002C); or
3) Disable the map decoder by writing '0xF' to the Board Select value (0xFFF4002E). Refer to the MVME162 manual for more details.

Also, OS-9 probes location 0xFFFF10C0 for a disc controller on power-up. Locating a VME board at this address can cause unpredictable results.

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Table 3-3 V64XSC4 Board Base Address Jumper Selection Table

J1(A15)	J2(A14)	J3(A13)	J4(A12)	J5(A11)	VME Short I/O Address
ON	ON	ON	ON	ON	0x0000
ON	ON	ON	ON	OFF	0x0800
ON	ON	ON	OFF	ON	0x1000
ON	ON	ON	OFF	OFF	0x1800
ON	ON	OFF	ON	ON	0x2000
ON	ON	OFF	ON	OFF	0x2800
ON	ON	OFF	OFF	ON	0x3000
ON	ON	OFF	OFF	OFF	0x3800
ON	OFF	ON	ON	ON	0x4000
ON	OFF	ON	ON	OFF	0x4800
ON	OFF	ON	OFF	ON	0x5000
ON	OFF	ON	OFF	OFF	0x5800
ON	OFF	OFF	ON	ON	0x6000
ON	OFF	OFF	ON	OFF	0x6800
ON	OFF	OFF	OFF	ON	0x7000
ON	OFF	OFF	OFF	OFF	0x7800
OFF	ON	ON	ON	ON	0x8000
OFF	ON	ON	ON	OFF	0x8800
OFF	ON	ON	OFF	ON	0x9000
OFF	ON	ON	OFF	OFF	0x9800
OFF	ON	OFF	ON	ON	0xA000
OFF	ON	OFF	ON	OFF	0xA800
OFF	ON	OFF	OFF	ON	0xB000
OFF	ON	OFF	OFF	OFF	0xB800
OFF	OFF	ON	ON	ON	0xC000
OFF	OFF	ON	ON	OFF	0xC800
OFF	OFF	ON	OFF	ON	0xD000
OFF	OFF	ON	OFF	OFF	0xD800
OFF	OFF	OFF	ON	ON	0xE000
OFF	OFF	OFF	ON	OFF	0xE800
OFF	OFF	OFF	OFF	ON	0xF000
OFF	OFF	OFF	OFF	OFF	0xF800

Where ON = logic ‘0’, OFF = logic ‘1’

3.3.3 IP Module I/O

The V64XT4L provides easy access to all four IP Module I/O connectors. The V64XT4L Transition Module must be installed directly behind the V64XSC4 Carrier as outlined above and shown in Figure 3-6.

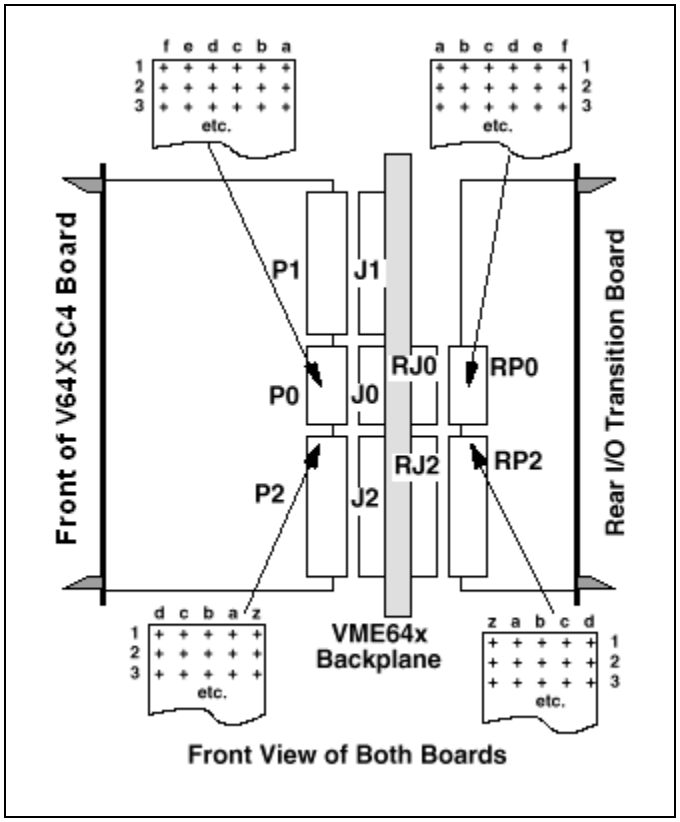


Figure 3-6 V64XSC4 and V64XT4L Board Orientation

NOTE: This drawing is from the *ANSI/VITA 1.1-1997*. VMEbus International Trade Association P.O. Box 19658, Fountain Hills, AZ 85260 USA www.vita.com.

The V64XT4L is a transition module that is necessary to use if I/O is desired. The I/O connectors are located near the front panel of the transition module where standard 50-pin flat cables can be installed by directly plugging into headers protruding through the front panel and securing the tabs behind the cable ends. This allows for easy system integration.

All of the V64XSC4 IP Module I/O connector pin numbers directly correspond to each transition module's I/O connector pinout (that is, a **one-to-one** relationship with **pin 50 connected** to **pin 50** down to **pin 1 connected** to **pin 1**).

3.4 V64XSC4 IP Module STROBE Connector

IP Module Logic Bus connector has a signal called “N_STROBE” and is user defined by the IP Module Logic Bus Specification. On the V64XSC4 each of the strobe signals are provided through J6 with the IP Module slot “A” strobe signal on pin 1 through slot “D” on pin 4 with pin 5 and 6 grounded. Each of the strobe signals on the V64XSC4 are pulled-up to +5 V via 10 KΩ resistors. The strobe connector (J6) is located at the middle left of Figure 3-3 V64XSC4 Assembly Drawing (which is at the front middle of the V64XSC4 when installed).

Table 3-4 V64XSC4 STROBE Connector Pin Assignments

Pin Number	Signal Name
1	GROUND
2	GROUND
3	N_STROBE_D
4	N_STROBE_C
5	N_STROBE_B
6	N_STROBE_A

3.5 VME64 Extensions (VME64x)

Table 3-5 shows the pin assignments for the VME64x P1 connector. The signals on the left side are of the VME64x specification signal nomenclature while the ones on the right are those used by Curtiss-Wright Controls, Inc.

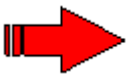
Table 3-5 VME64x P1 Rows a, b, and c Pin Assignment

VME64x P1 Pin #	VME64x ROWa Signal	Curtiss-Wright ROWa Signal	VME64x ROWb Signal	Curtiss-Wright ROWb Signal	VME64x ROWc Signal	Curtiss-Wright ROWc Signal
1	D00	VMED0	BBSY*	N/C	D08	VMED8
2	D01	VMED1	BCLR*	N/C	D09	VMED9
3	D02	VMED2	ACFAIL*	N/C	D10	VMED10
4	D03	VMED3	BG0IN*	V_BG0IN	D11	VMED11
5	D04	VMED4	BG0OUT*	V_BG0OUT	D12	VMED12
6	D05	VMED5	BG1IN*	V_BG1IN	D13	VMED13
7	D06	VMED6	BG1OUT*	V_BG1OUT	D14	VMED14
8	D07	VMED7	BG2IN*	V_BG2IN	D15	VMED15
9	GND	GND	BG2OUT*	V_BG2OUT	GND	GND
10	SYSCLK	SYSCLK_IN	BG3IN*	V_BG3IN	SYSFAIL*	N/C
11	GND	GND	BG3OUT*	V_BG3OUT	BERR*	VME_BERR
12	DS1*	VME_DS1	BR0*	N/C	SYSRESET*	VME_SYSRESET
13	DS0*	VME_DS0	BR1*	N/C	LWORD*	V_LWORD
14	WRITE*	VME_WRITE	BR2*	N/C	AM5	AM5
15	GND	GND	BR3*	N/C	A23	VME_A23
16	DTACK*	V_DTACK	AM0	AM0	A22	VME_A22
17	GND	GND	AM1	AM1	A21	VME_A21
18	AS*	V_AS	AM2	N/C	A20	VME_A20
19	GND	GND	AM3	AM3	A19	VME_A19
20	IACK*	V_IACK	GND	GND	A18	VME_A18
21	IACKIN*	V_IACKIN	SERCLK*	N/C	A17	VME_A17
22	IACKOUT*	V_IACKOUT	SERDAT*	N/C	A16	VME_A16
23	AM4	AM4	GND	GND	A15	VME_A15
24	A07	VME_A7	IRQ7*	V_IRQ7	A14	VME_A14
25	A06	VME_A6	IRQ6*	V_IRQ6	A13	VME_A13
26	A05	VME_A5	IRQ5*	V_IRQ5	A12	VME_A12
27	A04	VME_A4	IRQ4*	V_IRQ4	A11	VME_A11
28	A03	VME_A3	IRQ3*	V_IRQ3	A10	VME_A10
29	A02	VME_A2	IRQ2*	V_IRQ2	A09	VME_A9
30	A01	VME_A1	IRQ1*	V_IRQ1	A08	VME_A8
31	-12V	-12V	+5VSTDBY	N/C	+12V	+12V
32	+5V	VDD	+5V	VDD	+5V	VDD

Table 3-6 shows the pin assignments for the VME64x P1 connector. As with Table 3-5 the signals on the left side are of the VME64x specification signal nomenclature while the ones on the right are those used by Curtiss-Wright Controls, Inc.

Table 3-6 VME64x P1 Rows z and d Pin Assignments

VME64x P1 Pin #	VME64x ROWz Signal	Curtiss-Wright ROWz Signal	VME64x ROWd Signal	Curtiss-Wright ROWd Signal
1	MPR	N/C	VPC	N/C
2	GND	GND	GND	GND
3	MCLK	N/C	+V1	N/C
4	GND	GND	+V2	N/C
5	MSD	N/C	RsvU	N/C
6	GND	GND	-V1	N/C
7	MMD	N/C	-V2	N/C
8	GND	GND	RsvU	N/C
9	MCTL	N/C	GAP*	N/C
10	GND	GND	GA0*	N/C
11	RESP*	N/C	GA1*	N/C
12	GND	GND	+3.3v	N/C
13	RsvBus	N/C	GA2*	N/C
14	GND	GND	+3.3v	N/C
15	RsvBus	N/C	GA3*	N/C
16	GND	GND	+3.3v	N/C
17	RsvBus	N/C	GA4*	N/C
18	GND	GND	+3.3v	N/C
19	RsvBus	N/C	RsvBus	N/C
20	GND	GND	+3.3v	N/C
21	RsvBus	N/C	RsvBus	N/C
22	GND	GND	+3.3v	N/C
23	RsvBus	N/C	RsvBus	N/C
24	GND	GND	+3.3v	N/C
25	RsvBus	N/C	RsvBus	N/C
26	GND	GND	+3.3v	N/C
27	RsvBus	N/C	LI/I*	N/C
28	GND	GND	+3.3v	N/C
29	RsvBus	N/C	LI/O*	N/C
30	GND	GND	+3.3v	N/C
31	RsvBus	N/C	GND	GND
32	GND	GND	VPC	N/C



NOTE: Pins d1, d2, d31, and d32 are MFBL (mate-first-break-last) pins

Table 3-7shows the pin assignments for the VME64x P2 connector. As with Table 3-5, the signals on the left side are of the VME64x specification signal nomenclature while the ones on the right are those used by Curtiss-Wright Controls, Inc.

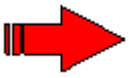
Table 3-7 VME64x P2 Rows a, b and c Pin Assignments

VME64x P2 Pin #	VME64x ROWa Signal	Curtiss-Wright ROWa Signal	VME64x ROWb Signal	Curtiss-Wright ROWb Signal	VME64x ROWc Signal	Curtiss-Wright ROWc Signal
1	B41	B_IO_41	+5 V	VDD	B42	B_IO_42
2	B43	B_IO_43	GND	GND	B44	B_IO_44
3	B45	B_IO_45	Reserved	N/C	B46	B_IO_46
4	B47	B_IO_47	A24	VME_A24	B48	B_IO_48
5	B49	B_IO_49	A25	VME_A25	B50	B_IO_50
6	A1	A_IO_1	A26	VME_A26	A2	A_IO_2
7	A3	A_IO_3	A27	VME_A27	A4	A_IO_4
8	A5	A_IO_5	A28	VME_A28	A6	A_IO_6
9	A7	A_IO_7	A29	VME_A29	A8	A_IO_8
10	A9	A_IO_9	A30	VME_A30	A10	A_IO_10
11	A11	A_IO_11	A31	VME_A31	A12	A_IO_12
12	A13	A_IO_13	GND	GND	A14	A_IO_14
13	A15	A_IO_15	+5 V	VDD	A16	A_IO_16
14	A17	A_IO_17	D16	N/C	A18	A_IO_18
15	A19	A_IO_19	D17	N/C	A20	A_IO_20
16	A21	A_IO_21	D18	N/C	A22	A_IO_22
17	A23	A_IO_23	D19	N/C	A24	A_IO_24
18	A25	A_IO_25	D20	N/C	A26	A_IO_26
19	A27	A_IO_27	D21	N/C	A28	A_IO_28
20	A29	A_IO_29	D22	N/C	A30	A_IO_30
21	A31	A_IO_31	D23	N/C	A32	A_IO_32
22	A33	A_IO_33	GND	GND	A34	A_IO_34
23	A35	A_IO_35	D24	N/C	A36	A_IO_36
24	A37	A_IO_37	D25	N/C	A38	A_IO_38
25	A39	A_IO_39	D26	N/C	A40	A_IO_40
26	A41	A_IO_41	D27	N/C	A42	A_IO_42
27	A43	A_IO_43	D28	N/C	A44	A_IO_44
28	A45	A_IO_45	D29	N/C	A46	A_IO_46
29	A47	A_IO_47	D30	N/C	A48	A_IO_48
30	A49	A_IO_49	D31	N/C	A50	A_IO_50
31	+3.3V	N/C	GND	GND	+3.3V	N/C
32	+5V	VDD	+5V	VDD	+5V	VDD

Table 3-8 shows the pin assignments for the VME64x P2 connector. As with Table 3-5, the signals on the left side are of the VME64x specification signal nomenclature while the ones on the right are those used by Curtiss-Wright Controls, Inc.

Table 3-8 VME64x P2 Rows z and d Pin Assignments

VME64x P2 Pin #	VME64x ROWz Signal	Curtiss-Wright ROWz Signal	VME64x ROWd Signal	Curtiss-Wright ROWd Signal
1	C46	C_IO_46	C47	C_IO_47
2	GND	GND	C48	C_IO_48
3	C49	C_IO_49	C50	C_IO_50
4	GND	GND	B1	B_IO_1
5	B2	B_IO_2	B3	B_IO_3
6	GND	GND	B4	B_IO_4
7	B5	B_IO_5	B6	B_IO_6
8	GND	GND	B7	B_IO_7
9	B8	B_IO_8	B9	B_IO_9
10	GND	GND	B10	B_IO_10
11	B11	B_IO_11	B12	B_IO_12
12	GND	GND	B13	B_IO_13
13	B14	B_IO_14	B15	B_IO_15
14	GND	GND	B16	B_IO_16
15	B17	B_IO_17	B18	B_IO_18
16	GND	GND	B19	B_IO_19
17	B20	B_IO_20	B21	B_IO_21
18	GND	GND	B22	B_IO_22
19	B23	B_IO_23	B24	B_IO_24
20	GND	GND	B25	B_IO_25
21	B26	B_IO_26	B27	B_IO_27
22	GND	GND	B28	B_IO_28
23	B29	B_IO_29	B30	B_IO_30
24	GND	GND	B31	B_IO_31
25	B32	B_IO_32	B33	B_IO_33
26	GND	GND	B34	B_IO_34
27	B35	B_IO_35	B36	B_IO_36
28	GND	GND	B37	B_IO_37
29	B38	B_IO_38	B39	B_IO_39
30	GND	GND	B40	B_IO_40
31	+3.3V	N/C	GND	GND
32	GND	GND	VPC	N/C



NOTE: Pins d1, d2, d31, and d32 are MFBL (mate-first-break-last) pins

Table 3-9 shows the pin assignments for the VME64x P0 connector. As with Table 3-5, the signals on the left side are of the VME64x specification signal nomenclature while the ones on the right are those used by Curtiss-Wright Controls, Inc.

Table 3-9 VME64x P0 Rows a, b and c Pin Assignments

VME64x P0 Pin #	VME64x ROWa Signal	Curtiss-Wright ROWa Signal	VME64x ROWb Signal	Curtiss-Wright ROWb Signal	VME64x ROWc Signal	Curtiss-Wright ROWc Signal
1	D1	D_IO_1	D2	D_IO_2	D3	D_IO_3
2	D6	D_IO_6	D7	D_IO_7	D8	D_IO_8
3	D11	D_IO_11	D12	D_IO_12	D13	D_IO_13
4	D16	D_IO_16	D17	D_IO_17	D18	D_IO_18
5	D21	D_IO_21	D22	D_IO_22	D23	D_IO_23
6	D26	D_IO_26	D27	D_IO_27	D28	D_IO_28
7	D31	D_IO_31	D32	D_IO_32	D33	D_IO_33
8	D36	D_IO_36	D37	D_IO_37	D38	D_IO_38
9	D41	D_IO_41	D42	D_IO_42	D43	D_IO_43
10	D46	D_IO_46	D47	D_IO_47	D48	D_IO_48
11	C1	C_IO_1	C2	C_IO_2	C3	C_IO_3
12	C6	C_IO_6	C7	C_IO_7	C8	C_IO_8
13	C11	C_IO_11	C12	C_IO_12	C13	C_IO_13
14	C16	C_IO_16	C17	C_IO_17	C18	C_IO_18
15	C21	C_IO_21	C22	C_IO_22	C23	C_IO_23
16	C26	C_IO_26	C27	C_IO_27	C28	C_IO_28
17	C31	C_IO_31	C32	C_IO_32	C33	C_IO_33
18	C36	C_IO_36	C37	C_IO_37	C38	C_IO_38
19	C41	C_IO_41	C42	C_IO_42	C43	C_IO_43

Table 3-10 shows the pin assignments for the VME64x P0 connector. As with Table 3-5, the signals on the left side are of the VME64x specification signal nomenclature while the ones on the right are those used by Curtiss-Wright Controls, Inc.

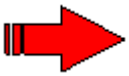
Table 3-10 VME64x P0 Rows d, e and f Pin Assignments

VME64x P0 Pin #	VME64x ROWd Signal	Curtiss-Wright ROWd Signal	VME64x ROWe Signal	Curtiss-Wright ROWe Signal	VME64x ROWf Signal	Curtiss-Wright ROWf Signal
1	D4	D_IO_4	D5	D_IO_5	GND	GND
2	D9	D_IO_9	D10	D_IO_10	GND	N/C
3	D14	D_IO_14	D15	D_IO_15	GND	GND
4	D19	D_IO_19	D20	D_IO_20	GND	N/C
5	D24	D_IO_24	D25	D_IO_25	GND	GND
6	D29	D_IO_29	D30	D_IO_30	GND	N/C
7	D34	D_IO_34	D35	D_IO_35	GND	GND
8	D39	D_IO_39	D40	D_IO_40	GND	N/C
9	D44	D_IO_44	D45	D_IO_45	GND	GND
10	D49	D_IO_49	D50	D_IO_50	GND	N/C
11	C4	C_IO_4	C5	C_IO_5	GND	GND
12	C9	C_IO_9	C10	C_IO_10	GND	N/C
13	C14	C_IO_14	C15	C_IO_15	GND	GND
14	C19	C_IO_19	C20	C_IO_20	GND	N/C
15	C24	C_IO_24	C25	C_IO_25	GND	GND
16	C29	C_IO_29	C30	C_IO_30	GND	N/C
17	C34	C_IO_34	C35	C_IO_35	GND	GND
18	C39	C_IO_39	C40	C_IO_40	GND	N/C
19	C44	C_IO_44	C45	C_IO_45	GND	GND

Table 3-11 shows the pin assignments for each IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by SYSTRAN. The lower case "x" in the SYSTRAN signal name represents the "A", "B", "C", or "D" mnemonic for each IP Module slot.

Table 3-11 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Curtiss-Wright Signal Names	Bussed or Unique	X = Pulled Up Via 10 KΩ Resistor
GND	50	GND	GND	GND
Reserved	49	RESERVED1	Unique	X
Ack*	48	N_IPxACK	Unique	X
A6	47	VMEA6	Bussed	
Strobe*	46	N_STROBE_x	Unique	X
A5	45	VMEA5	Bussed	
Intreq1*	44	N_IPxINTREQ1	Unique	X
A4	43	VMEA4	Bussed	
Intreq0*	42	N_IPxINTREQ0	Unique	X
A3	41	VMEA3	Bussed	
Error*	40	N_IPxERROR	Unique	X
A2	39	VMEA2	Bussed	
DMAEnd*	38	N_DMAEND	Unique	X
A1	37	IPA1	Bussed	
Reserved	36	RESERVED2	Unique	X
IOSel*	35	N_IPxIOSEL	Unique	
DMAck0*	34	N_DMACK0	Unique	X
IntSel*	33	N_IPxINTSEL	Unique	
DMAReq1	32	N_DMAREQ1	Unique	X
MemSel*	31	N_MEMSEL	Unique	
DMAReq0	30	N_DMAREQ0	Unique	X
IDSel*	29	N_IPxIDSEL	Unique	
R/W*	28	V_WRITE	Bussed	
+5V	27	+5VDC	+5 Vdc	+5 Vdc
GND	26	GND	GND	GND
GND	25	GND	GND	GND
+5V	24	+5VDC	+5 Vdc	+5 Vdc
+12V	23	+12VDC	+12 Vdc	+12 Vdc
-12V	22	-12VDC	-12 Vdc	-12 Vdc
BS1*	21	V_BS1	Bussed	
BS0*	20	V_BS0	Bussed	
D15	19	VLD15	Bussed	X
D14	18	VLD14	Bussed	X
D13	17	VLD13	Bussed	X
D12	16	VLD12	Bussed	X
D11	15	VLD11	Bussed	X
D10	14	VLD10	Bussed	X
D9	13	VLD9	Bussed	X
D8	12	VLD8	Bussed	X
D7	11	VLD7	Bussed	X
D6	10	VLD6	Bussed	X
D5	9	VLD5	Bussed	X
D4	8	VLD4	Bussed	X
D3	7	VLD3	Bussed	X
D2	6	VLD2	Bussed	X
D1	5	VLD1	Bussed	X
D0	4	VLD0	Bussed	X
Reset*	3	N_IPxRESET	Unique	
CLK	2	ICLK_x	B	
GND	1	GND	GND	GND



NOTE: The IP Module data bus, usually defined as IPD[15:0] for all of our IP Modules, is a subset of the information that appears on these signal lines. Since carrier register information also uses these signal lines, the bus was defined as the "VME64x Local Data Bus" designated as VLD[15:0].

4. OPERATION

NOTE: The extended implementation of write-transfer capability over the full ID addressing space for this product is over and above that described in the specification.

4.1 Overview

This section details the V64XSC4's features, functionality, and operation.

4.2 Functional Description

4.2.1 VME Memory Mapping Scheme

The V64XSC4 responds to VME supervisory and non-privileged data accesses in all three memory sizes: A16, A24 and A32. The V64XSC4 memory-mapping scheme allows I/O and ID addresses for all four IP Modules in all three addressing modes. This includes access to the carrier's control/status registers in A16 mode at fixed addresses relative to a jumper-selectable board base address. These base addresses can be set on 2 K boundaries throughout the VME short address space.

The V64XSC4 responds to address-modifier codes 29 and 2D (non-privileged and supervisory, respectively) in an A16 transfer. Memory accesses to all four of the IP Modules can be performed in either standard (A24) address mode or in extended (A32) address mode. The V64XSC4 responds to address-modifier codes 39 (standard non-privileged) and 3D (standard supervisory) in an A24 transfer. If you use this addressing mode, you can assign each IP Module a 1 MB section of the A24 memory map within an area defined by address bits A22 and A23. These bits are compared to those programmed into the MEMA24BASE Register to determine whether the V64XSC4 memory space is being hit in a standard data transfer.

The V64XSC4 also responds to address-modifier codes 09 (extended non-privileged) and 0D (extended supervisory) in an A32 transfer. If you use this addressing mode, each IP Module is assigned an 8 MB section of the A32 memory map within an area defined by address bits 31 down to 25. These bits are compared to those programmed into the MEMA32BASE Register to determine whether the V64XSC4 memory space is being hit in an extended data transfer. The MEMA24BASE Register and the MEMA32BASE Register are outlined in table 4-1 in section 4-4.

4.2.2 ID Transfers

The board supports IP Module ID reads and writes as A16/D16/D8 VME transfers. ID reads and writes are performed as word or byte transfers to the IP Module slot ID address space from the VMEbus. The ID PROM values are located at every other byte at odd-byte locations (IP Module byte lane 0). For word-reads the even byte is discarded. The ID PROM area allows read or write accesses to support future IP Modules requiring writes to the ID address space. Read-Modify-Write cycles are supported for ID transfers.

4.2.3 I/O Transfers

The board supports IP Module I/O reads and writes as A16/D16/D8 VME transfers. I/O reads and writes are performed as word or byte transfers to the IP Module slot I/O address space from the VMEbus. Even and odd single-byte reads are supported. Read-Modify-Write cycles are supported for I/O transfers.

4.2.4 Interrupt Transfers

The IP Module requests interrupts by asserting N_INTREQ0 or N_INTREQ1. An independent VME interrupter handles each of these IP Module interrupt request lines and asserts one of the seven prioritized VME interrupt request lines. This provides a minimum delay in asserting the interrupt request to the VMEbus master.

Which line is asserted depends on the interrupt level programmed into the carrier's IP Module slot-specific interrupt register. The four interrupt registers, one per IP Module slot, support independent selection of interrupt levels for both interrupt request signals N_INTREQ0 and N_INTREQ1. The V64XSC4 conducts a D8 transfer of the interrupt vector from the IP Module to the VMEbus after receipt of the interrupt acknowledgment from the VMEbus master. The interrupt request release will depend on the individual IP Module being used.

4.2.5 Interrupt Prioritization

VME systems prioritize interrupts in a two-tier fashion: Interrupt Request Level (IRQ) and relative position. This tier effect is demonstrated in Figure 4-1.

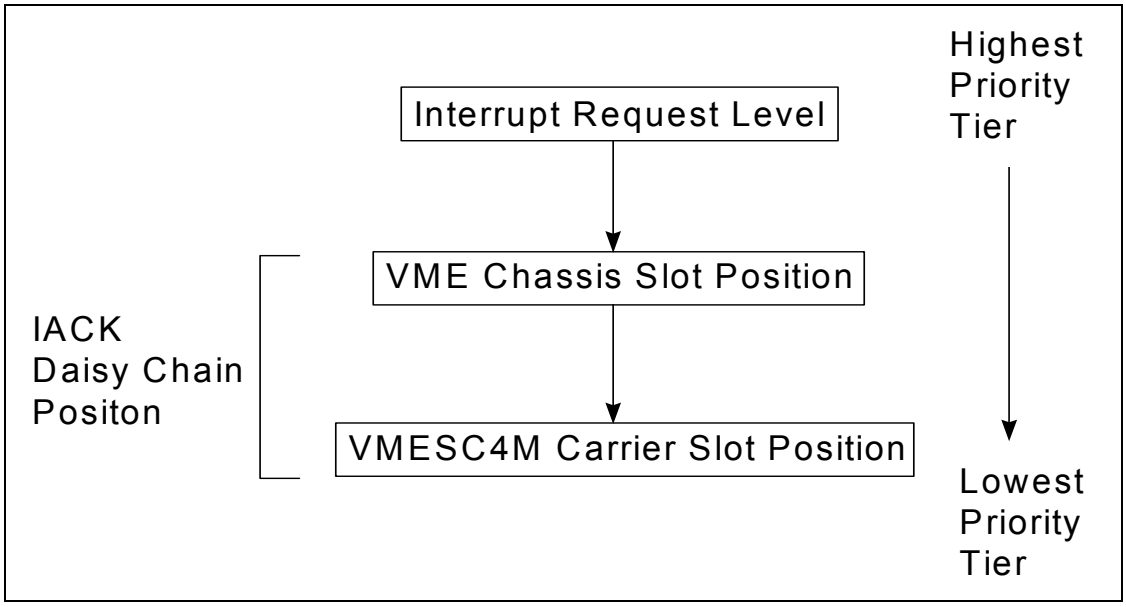


Figure 4-1 Interrupt Priority Tiers

The first tier of prioritization is the interrupt request level, with level 7 being the highest priority and level 1 the lowest as shown in Table 4-1.

Table 4-1 Interrupt Request Level Priorities

Interrupt Request Level	Priority
7	Highest
6	2nd Highest
5	•
4	•
3	•
2	2nd Lowest
1	Lowest

The relative position in the interrupt daisy chain determines the second tier of prioritization. The closer the interrupt requester is to the interrupt handler in the daisy chain, the higher its priority for a given request level. The relative position in the daisy chain is determined by the VME chassis slot location (see Figure 4-2) and the IP Module slot location on the V64XSC4 carrier (see Figure 4-3).

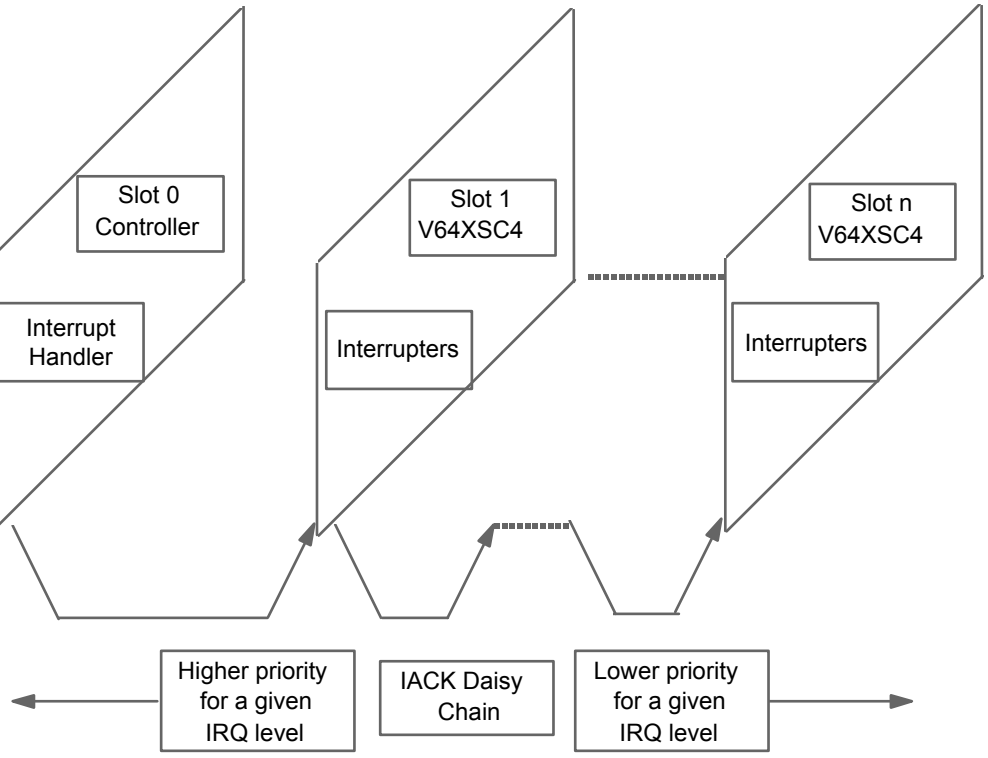


Figure 4-2 VME Chassis Slot Prioritization Through IACK Daisy Chain

The V64XSC4 IP Module slot priority order from highest to lowest is A0, A1, B0, B1, C0, C1, D0, D1.

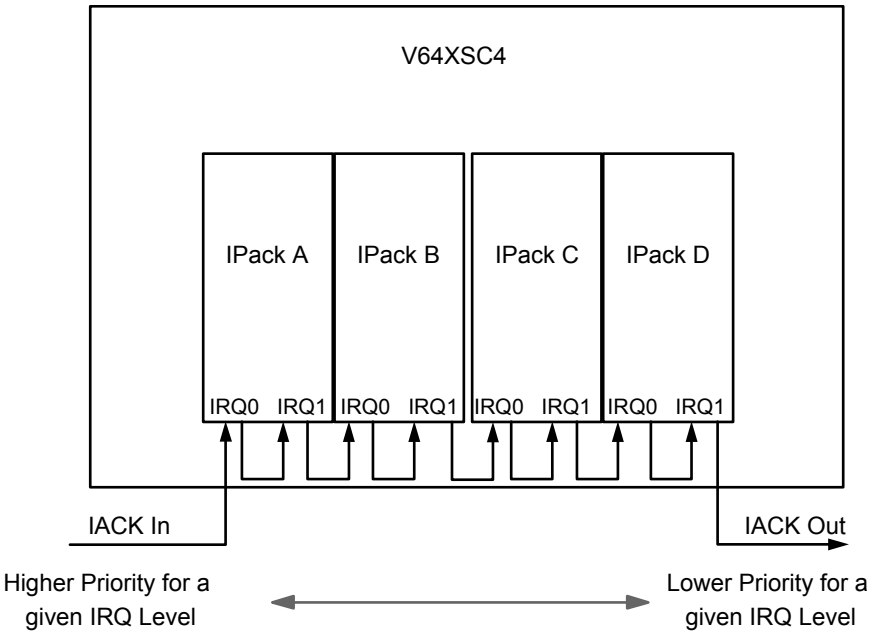


Figure 4-3 IACK Daisy Chain on the Carrier

4.2.6 General-purpose Registers

The board has four 8-bit general purpose user-defined registers, and supports read-Modify-Write cycles for general-purpose register accesses.

4.2.7 Diagnostic LEDs

Six diagnostic LEDs are located on the front panel of the V64XSC4. The five LEDs labeled A, B, C, D, and CRA, indicate when a read or write access is attempted to one of the four IP Module slots or the carrier registers. The sixth LED, labeled DTACK, indicates an acknowledgment by the IP Module or the V64XSC4 of the attempted access. This scheme provides independent verification of the access and the acknowledgment.

4.2.8 IP Module Reset

The board facilitates independent or simultaneous resetting of the IP Modules through writes to the Reset register. Monitoring of the pulse-stretched reset signals is made possible by reading the Reset register. For a detailed description of this register, see Appendix B: Programming Guide.

4.2.9 Error Status

Reading the Error Status register allows IP Module ERROR monitoring. For a detailed description of this register, see Appendix B: Programming Guide.

4.2.10 Strobe Signals

You can connect IP Module STROBE signals via a 6-pin header (J6) located near the front panel.

4.2.11 Power Supply Filtering

The carrier uses independent ‘T’ type filters for the +5, +12, and -12 volt IP module power. This arrangement provides superior power supply filtering.

4.2.12 Fuses

The board uses independent field-replaceable fuses for the +5, +12, and -12 volt IP Module power. These fuses are more expensive than ordinary fuses but they provide superior short-circuit protection.

NOTE: Replacement fuses can be purchased directly from Littelfuse®, Inc. Phone (708) 829-0400.

1. Amp Fuse Manufacturer's Part Number R451001
2. Amp Fuse Manufacturer's Part Number R451002

4.3 Theory of Operation

4.3.1 Block Diagram Description

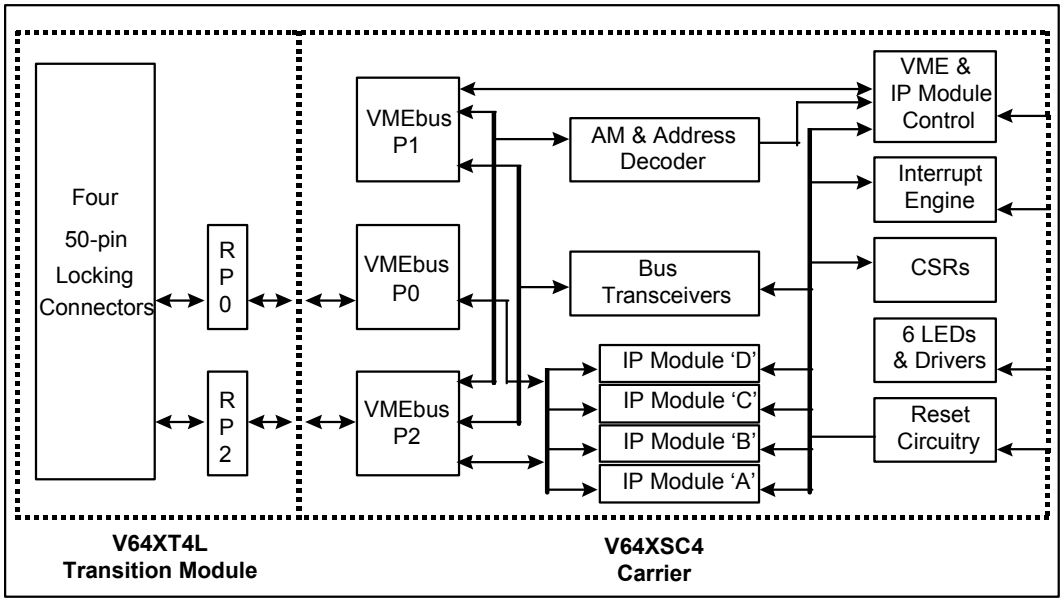


Figure 4-4 V64XSC4 Block Diagram

Figure 4-4 is a simplified block diagram of the V64XSC4 carrier and the V64XT4L transition module. The figure represents the signal flow between the VMEbus, IP Module Logic Bus and the IP Module I/O connectors via the V64XT4L Transition Module. The VMEbus P1, P2 and P0 connectors are located on the diagram's left side. All transfers between the VME host computer and the V64XSC4's registers or IP Modules are conducted through the P1 connectors. The VMEbus transfers **do not** insert any IP Module hold cycles during an access to the IP Modules.

The block labeled "AM & Address Decoder" handles decoding of the VME address and address modifiers. The block labeled "VME & IP Module Control" handles the transfer of data between the VME and both the V64XSC4 CSRs and the IP Modules.

The block labeled "Interrupt Engine" controls the VME Interrupt requests, and prioritizes VME Interrupt Acknowledge cycles. The large block in the center of the diagram represents the four IP Module slots labeled IP Module 'D' down to IP Module 'A'. The IP

Module I/O connectors are directly connected to the backplane via V64XSC4's P2 and P0 connectors. These signals transition from the backplane to the V64XT4L's four front-panel 50-pin I/O connectors with the RP0 and RP2 connector. The 50-pin I/O connectors consist of two sets of clearly labeled 100-pin "stacked" headers. This allows inserting IP slots "A" and "B" I/O cables one directly over the other. This orientation is the same for IP modules "C" and "D" respectively. The last two blocks at the lower right hand corner of the diagram contain the reset circuitry for each IP Module and drivers for each of the six front panel LEDs.

The P1 connector is located on the upper left of the V64XSC4 Assembly Drawing (Figure 4-5). When looking at the "top" or component side of the V64XSC4, the IP Module slots are labeled from left to right for slot 'D' through slot 'A'. All I/O signals are connected through the P0 and P2 connectors located at the top-center and top-right of the drawing.

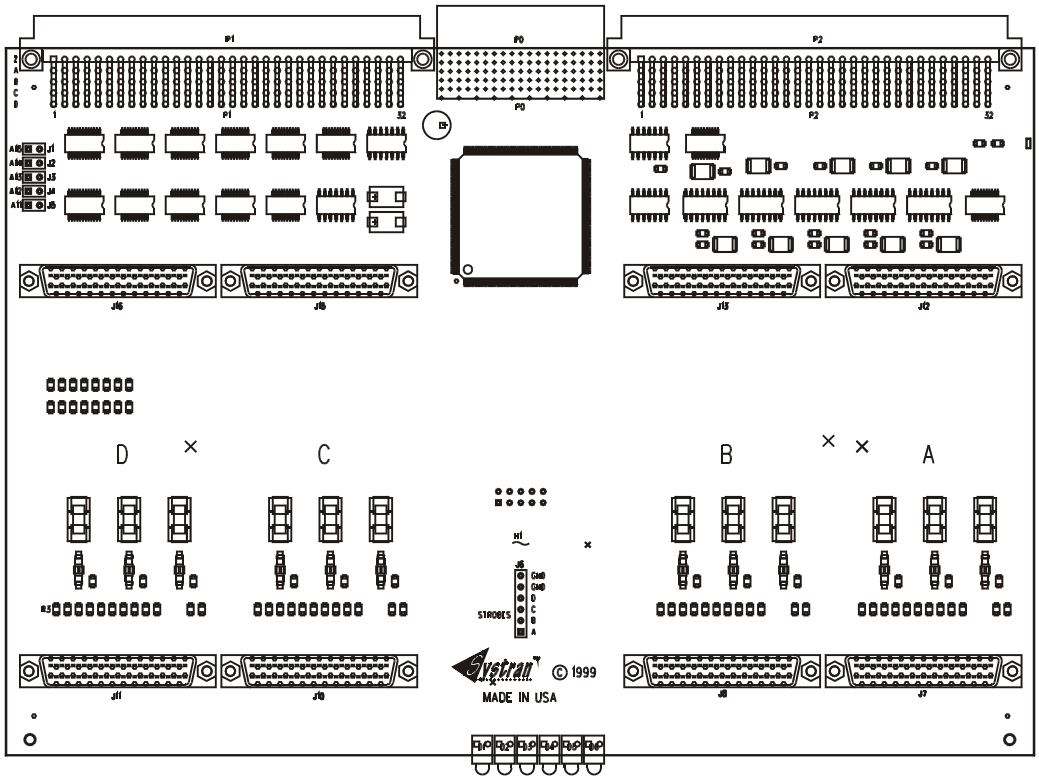


Figure 4-5 V64XSC4 Mechanical Assembly

4.3.2 Functional Logic Module Overview

The address decoding, VME and IP bus interface controllers, interrupt handler, and the reset control and LED driver circuitry are all contained within one functional logic module, VME4CTL, which was created using VHDL modeling techniques. The VME4CTL is programmed into a single Altera 9000 series EPLD and can be sectioned into several functional areas as defined below.

4.3.2.1 Data Transfer Control

VME ADDRESS DECODER

The VME Address Decoder detects VME host accesses to local V64XSC4 Board Registers and IP Module I/O and ID spaces. The decoder asserts an address-detect (hit) signal corresponding to one of these address spaces when it detects a matching address and address modifier (0x29 and 0x2D). This functional area also compares VME address bus values to memory base registers during A24 (standard) or A32 (extended) address cycles. The decoder generates internal memory hit signals when values match.

DATA TRANSFER ENGINE

The DTE block handles data transfers between the VMEbus and IP Modules. It monitors the HIT signals from the address decoders and determines when a transfer takes place. The VME control signals and address lines provide the rest of the transfer information. The DTE asserts the appropriate IP Module ID, I/O, or memory select line and executes an IP Module synchronous transfer. The DTE is implemented using combinational logic and four state machines: The State Machines are:

- VME Read cycles from the local control and status registers
- VME Write cycles to the local control and status registers
- IP Module I/O, ID, and memory Read cycles
- IP Module I/O, ID, and memory Write cycles

The IP Module read and write state machines complete a transfer in three IP Module clock cycles (six VME SYSCLOCK cycles).

REGISTERS

The VME4CTL module contains registers necessary for data transfers and interrupt cycles. The registers are the general-purpose registers, interrupt level registers, reset control register, error status register and the memory-base-address registers.

4.3.2.2 Interrupt Control

VME INTERRUPT ENGINE

The VME Interrupt Engine detects interrupt requests from one or more IP Modules, then asserts and selects VME interrupt request levels. It monitors the VME V_IACKIN and A3-A1 signals and determines if the interrupt being acknowledged is the one it requested. If the level is different than the one requested, the acknowledge signal is passed on via V_IACKOUT daisy chain. If the acknowledge is for this IP Module's interrupt, the DTE asserts an internal interrupt hit signal and transfers the corresponding IP Module's interrupt vector. If more than one IP Module interrupts at the same level and time, the interrupts are processed in a prioritized fashion. IP Module slot A's N_INTREQ0 has the highest priority, then slot A's N_INTREQ1 the second highest, down to the slot D's N_INTREQ1. Refer to section 4.2.5 for a detailed description of interrupt prioritization.

You can implement the interrupt priority scheme by programming a specific level in the interrupt level registers. The Interrupt Engine is implemented using combinational logic and a state machine. The state machine places an interrupt vector on the VMEbus just like a VME read cycle. The IP Module Interrupt Acknowledge Cycle places the interrupt vector on the VMEbus in three IP Module clock cycles (six VME SYSCLOCK cycles). Specifically the IP Module interrupt vector state machine places the vector on the VMEbus after detection of the appropriate IP Module acknowledge signal N_ACK.

4.3.2.3 Access LED/Reset Control

FRONT PANEL LED AND IP MODULE RESET DRIVERS

The VME4CTL module is also responsible for combinationally driving the front panel LEDs from the one-shot drivers, and for logically “ORing” the VME system reset (V_SYSRESET) with the individual IP Module reset one-shot signals for driving each IP Module reset signal

APPENDIX A

SPECIFICATIONS

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FIGURES

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Figure A-2 V64XT4L Dimensions..... A-4

A.1 V64XSC4 Specifications

MECHANICAL

Measurement:	Length: 9.187 inches (23.33 cm) Width: 6.299 inches (15.99 cm)
Weight:	11.06 oz., 313 grams (includes front panel)
Board Thickness:	0.062 inches, 0.157 cm, nominally, (10 layers)
Power (No IPs installed):	(No IP Modules installed): +5 Vdc (+5%) @ 0.3 Amps, +12 Vdc @ 0.0 Amps, - 12 Vdc @ 0.0 Amps

NOTE: The grounds for the VMEbus and IP Module are not isolated through this board.

ABSOLUTE MAXIMUM ELECTRICAL RATINGS

Supply voltage with respect to ground..	Minimum	Maximum
+0.5 VDC	-0.5 VDC	+7.0 VDC
+12.0 VDC	IP Module dependent	
-12.0 VDC	IP Module dependent	

RECOMMENDED OPERATING SUPPLY RATINGS

Supply voltage with respect to ground	+4.75 VDC to + 5.25 VDC
Logic Interface	ANSI/VITA 4-1995 Specification-compliant carrier

ENVIRONMENTAL SPECIFICATIONS

Temperature

Operating Range	0° to +70° C
Storage	-45° to +85°C
Humidity Range	5% to 95% (non-condensing)

MEAN TIME BETWEEN FAILURE (MTBF):

MIL-HDBK-217F	234,042 hours
Bellcore, Issue 6	588,822 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

A.2 V64XSC4 Dimensions

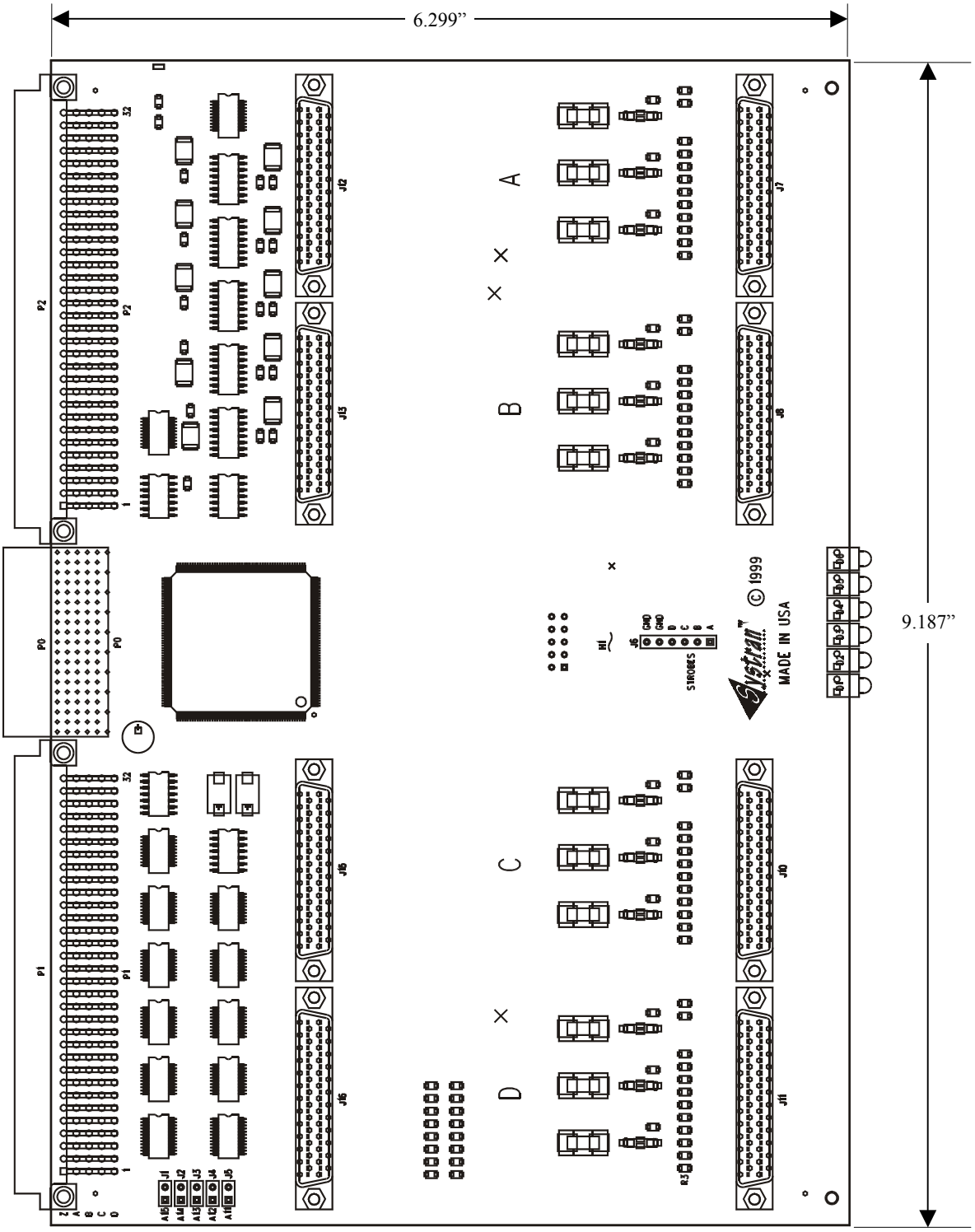


Figure A-1 V64XSC4 Dimensions

A.3 V64XT4L Specifications

MECHANICAL

Measurement	Length: 9.187 inches (23.33 cm) Width: 3.150 inches (8.0 cm)
Weight:.....	7.35 oz., 208 grams (includes front panel)
Board Thickness:	0.062 inches, 0.157 cm, nominally, (8 layers)

ENVIRONMENTAL SPECIFICATIONS

Temperature

Operating Range	0° to +70° C
Storage	-45° to +85°C
Humidity (Noncondensing)	5% to 95% (non-condensing)

MEAN TIME BETWEEN FAILURE (MTBF):

MIL-HDBK-217F	27,177,606 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.

A.4 V64XT4L Dimensions

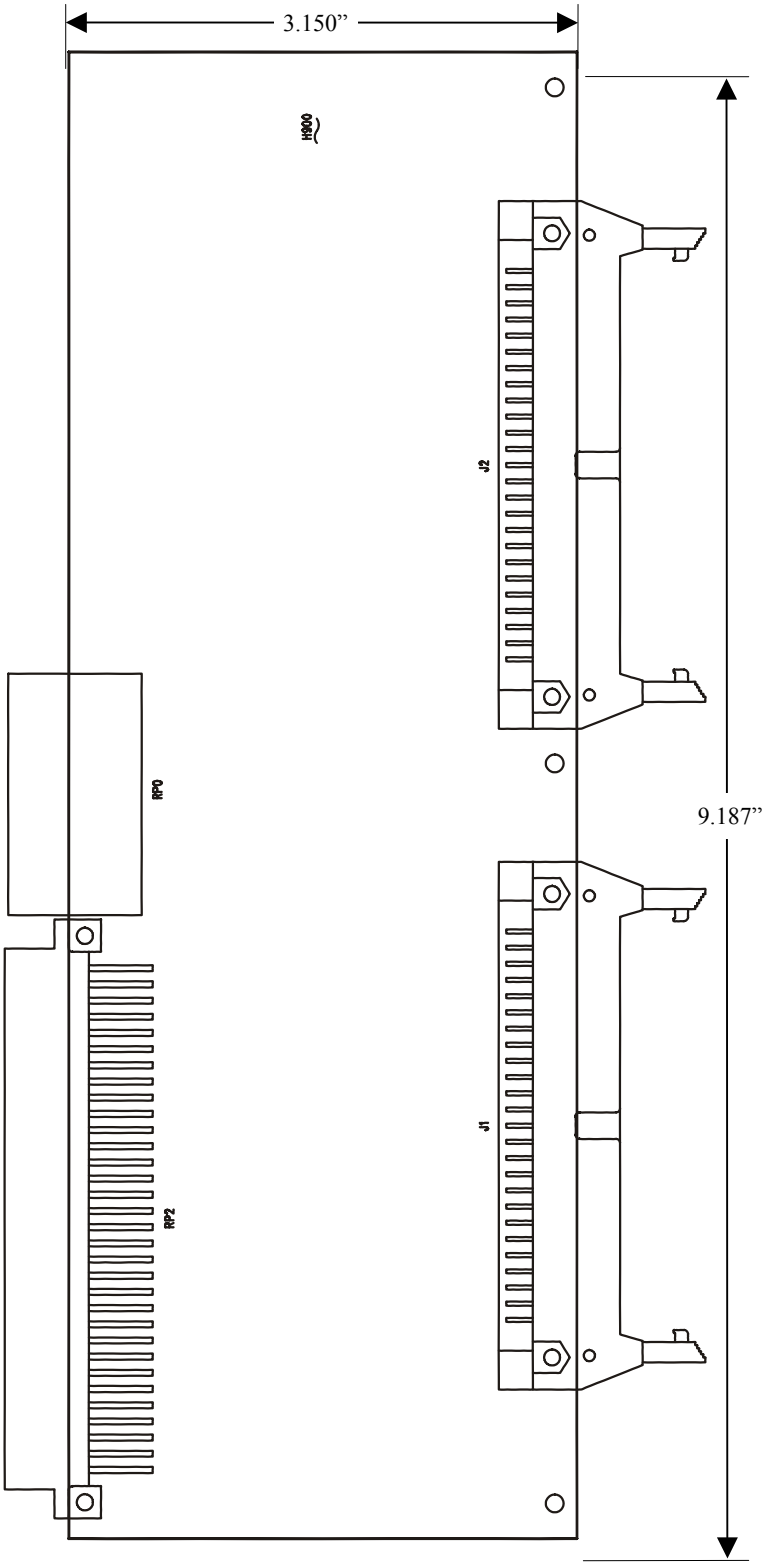


Figure A-2 V64XT4L Dimensions

APPENDIX B

PROGRAMMING GUIDE

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B.1 Overview

This section describes the V64XSC4's software, specifically, the V64XSC4's registers and overall mapping and addressing scheme, and includes programming examples. A more detailed description of the hardware can be found in chapter 2: Product Overview, and application concepts are discussed in Appendix D: Typical Applications.

B.2 Description

The V64XSC4 is an easy-to-use VME6U slave card supporting four singlewide, two singlewide and one doublewide, or two doublewide IP Modules. In addition to providing access to the I/O and ID space of the IP Modules via the VME bus, the V64XSC4 has 12 onboard control/status registers.

B.3 Board Base Address

You can place the V64XSC4 anywhere in the VME short IO space (A16 space address modifier codes 0x29 and 0x2D) on 2 KB boundaries by setting the board base address jumpers. These jumpers, J5 to J1, correspond to address lines A11 to A15 respectively. Section 3.3.2 contains a detailed description of setting the board base address.

B.4 Address Map

The IP Module IO and ID spaces, and the carrier's control and status registers, reside at a fixed relative address from the V64XSC4 base address. Table B-1 shows the complete memory map for the board.

Table B-1 V64XSC4 Address Map

Address Space or Register Name	VME Address (relative to board base address)	Size
IP Module A I/O	Base+0x000	128 bytes
IP Module A ID	Base+0x080	128 bytes
IP Module B I/O	Base+0x100	128 bytes
IP Module B ID	Base+0x180	128 bytes
IP Module C I/O	Base+0x200	128 bytes
IP Module C ID	Base+0x280	128 bytes
IP Module D I/O	Base+0x300	128 bytes
IP Module D ID	Base+0x380	128 bytes
IP Module Reset Register	Base+0x500 - Word Access Base+0x501 - Byte Access	4 bits
Error Status Register	Base+0x502 - Word Access Base+0x503 - Byte Access	4 bits
IP Module A Interrupt Register	Base+0x580 - Word Access Base+0x581 - Byte Access	6 bits
IP Module B Interrupt Register	Base+0x582 - Word Access Base+0x583 - Byte Access	6 bits
IP Module C Interrupt Register	Base+0x584 - Word Access Base+0x585 - Byte Access	6 bits
IP Module D Interrupt Register	Base+0x586 - Word Access Base+0x587 - Byte Access	6 bits
General-purpose Register A	Base+0x600 - Word Access Base+0x601 - Byte Access	8 bits
General-purpose Register B	Base+0x602 - Word Access Base+0x603 - Byte Access	8 bits
General-purpose Register C	Base+0x604 - Word Access Base+0x605 - Byte Access	8 bits
General-purpose Register D	Base+0x606 - Word Access Base+0x607 - Byte Access	8 bits
A24 Memory Base Register	Base+0x680 - Word Access Base+0x681 - Byte Access	2 bits
A32 Memory Base Register	Base+0x682 - Word Access Base+0x683 - Byte Access	7 bits
Memory Enable Register	Base+0x684 - Word Access Base+0x685 - Byte Access	2 bits

B.5 Register Descriptions

The V64XSC4 registers can be accessed as byte (D8) or word (D16) values. When accessed as words, the upper byte is not driven by the carrier and its value is all '1's due to VLD[15:8] pull-up resistors. The unused bits in the lower byte are driven as '0's on reads. All unused bits are discarded on writes. The hexadecimal VME addresses for the registers shown below are relative to the board base address and are in the format (WORD/BYTE) for word and byte accesses respectively.

B.5.1 Reset Register (0x500/0x501)

Writing a '1' to bits RES_D through RES_A, asserts the corresponding IP Module's reset line. The bits can be set individually by writing a '1' to that bit or simultaneously with a single write of '0x0F.' When set, a one-shot is triggered supplying a minimum 200 ms reset pulse as required by the IP Module specification. When read, these bits return the status of the corresponding IP Module's reset line (a '0' means the IP Module is not being reset, a '1' means it is in a reset condition).

Table B-2 Reset Register Bit Description

Bit #	B15-B8	B7-B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	RES_D	RES_C	RES_B	RES_A
R/W	Reads '1's Writes discarded	Read '0's, Writes discarded	R/W	R/W	R/W	R/W
Power up State	N/A	N/A	0	0	0	0

NOTE: RES_D-RES_A: Reset bits for IP Module slots D to A.

B.5.2 Error Status Register (0x502/0x503)

These bits indicate the state of the corresponding IP Module N_xERROR. If the N_xERROR* signal is asserted (active low) for a particular IP Module, then the corresponding ERR_N bit will be set to a '1.' The corresponding bit will be cleared if the error signal is not asserted

Table B-3 Error Status Register Bit Description

Bit #	B15-B8	B7-B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	ERR_D	ERR_C	ERR_B	ERR_A
R/W	Reads '1's Writes discarded	Reads '0's Writes discarded	R	R	R	R
Power up State	N/A	N/A	State of IP Module D ERR* Signal	State of IP Module C ERR* Signal	State of IP Module B ERR* Signal	State of IP Module A ERR* Signal

NOTE: ERR_D-ERR_A: Error Status bits for IP Module slots D to A.

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B.5.3 Interrupt Level Registers A to D (0x580/0x581 to 0x586/0x587)

The three interrupt level bits, IL2-IL0, determine the VME bus interrupt request level when the corresponding IP Module IRQ line is asserted. Valid interrupt levels are 1 to 7. A value of '0'is not a valid interrupt request level and will not assert a VME interrupt request. Therefore, you can write a '0' to these registers to disable interrupts.

The interrupt requests are first prioritized by interrupt request level, then by slot position. Level 7 interrupt requests are the highest priority and level 1 is the lowest. Equal interrupt request levels are serviced in the slot prioritized order A0, A1, B0, ... C1, D0, D1. For more details regarding interrupt prioritization, see chapter 4: Operation.

Table B-4 Interrupt Level Register Bit Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	0	IRQ1 IL2	IRQ1 IL1	IRQ1 IL0	0	IRQ0 IL2	IRQ0 IL1	IRQ0 IL0
R/W	Reads 1's Writes discarded	Read '0' Writes discarded	R/W	R/W	R/W	Read '0' Writes discarded	R/W	R/W	R/W
Power -up State		0	0	0	0	0	0	0	0

NOTE: IRQN IL2-IL0: The interrupt level bits for IRQN.

B.5.4 General-purpose Registers A to D (0x600/0x601 to 0x606/0x607)

You can define general-purpose registers A to D to fit your specific applications. These read/write registers can be used for semaphores, shared memory, etc. For more information regarding these registers, see Appendix D: Typical Applications.

Table B-5 General-purpose Register Bit Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	GPR7	GPR6	GPR5	GPR4	GPR3	GPR2	GPR1	GPR0
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up State		0	0	0	0	0	0	0	0

NOTE: GPR7-GPR0: The General-purpose Register byte value.

B.5.5 A24 Memory Base Register (0x680/0x681)

The VME base address, where memory accesses will initiate memory cycles, are determined when the V64XSC4 carrier is configured to use A24 space (via the Memory Enable Register). In this mode the carrier will occupy 4 MB of A24 space. The first 1 MB will access IP Module A's first 1 MB of memory space. The second 1 MB will access IP Module B's first 1 MB of memory space. This is also true for IP Module C's and IP Module D's memory space in A24 mode. Accesses to an IP Module's memory space above 1 MB are not possible when using A24 address space.

Table B-6 A24 Memory Base Register Description

Bit #	B15-B8	B7	B6	B5-B0
Bit Name	Not Used	A23	A22	0
R/W	Reads '1's Writes discarded	R/W	R/W	Read '0' Writes discarded
Power-up State		0	0	0

NOTE: A23-A22: The A24 memory base used by the carrier to detect accesses to IP Module memory space

B.5.6 A32 Memory Base Register (0x682/0x683)

The VME base address, where memory accesses will initiate memory cycles, are determined when the V64XSC4 carrier is configured to use A32 space (via the Memory Enable Register). The carrier will occupy 32 MB of A32 space. The first 8 MB will access IP Module A's memory space. The second 8 MB region will access IP Module B's 8 MB of memory space. This is also true for IP Module C's and IP Module D's memory space in A32 mode.

Table B-7 A32 Memory Base Register Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	A31	A30	A29	A28	A27	A26	A25	0
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Read '0' Writes discarded
Power-up State		0	0	0	0	0	0	0	0

NOTE: A31-A25: The A32 memory base used by the carrier to detect accesses to IP Module memory space.

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B.5.7 Memory Enable Register (0x684/0x685)

Accesses to IP Module memory space are configured using this register. If the MEM_EN bit is cleared, accesses to the memory spaces of the IP Modules are disabled. If the MEM_EN bit is set to a '1,' accesses to the memory spaces are enabled. If the MEM_EN bit is set to a '1' and the SPACE_SEL is cleared, the IP Modules' memory spaces can be accessed via VME A24 cycles. If the MEM_EN bit and the SPC_SEL bit are both set to a '1,' the IP Modules' memory spaces can be accessed via VME A32 cycles.

Table B-8 Memory Enable Register Description

Bit #	B15-B8	B7-B2	B1	B0
Bit Name	Not Used	0	SPACE_SEL	MEM_EN
R/W	Reads '1's Writes discarded	Read '0' Writes discarded	R/W	R/W
Power-up State		0	0	0

B.6 V64XSC4 Programming Examples

The following examples illustrate how to program the V64XSC4 to achieve various operational modes.

B.6.1 Reset Example

This example resets one, then all four IP Modules, and then monitors the reset signals to determine when they are de-asserted. Setting a bit in the reset register causes a one-shot to assert the corresponding IP Module reset signal (the one-shot asserts the reset signal for approximately 240 ms). Monitor the Reset Register to determine when the reset signal is de-asserted.

- Write '0x0001' to the Reset register. This resets the IP Module in slot A by asserting the IP Module A reset signal.

LOOP1:

- Read the Reset register.
- If Bit 0 is set then go to LOOP1.
- Write '0x000F' to the Reset register. This resets all four IP Module modules by asserting their corresponding reset signals.

LOOP2:

- Read the Reset register.
- If any of the bits [3:0] are set then go to LOOP2.

B.6.2 Interrupt Initialization Example

Interrupts in the VME system are prioritized in a two-tier fashion:

- The first tier of prioritization is the interrupt request level, with level 7 being the highest priority and level 1 the lowest.
- The second tier of prioritization is determined by the relative position in the interrupt daisy chain.

If the interrupt requester is closer to the interrupt handler in the daisy chain, its priority is higher for a given request level. The relative position in the daisy chain is determined by the VME chassis slot location and the IP Module slot location on the V64XSC4 carrier. The V64XSC4 IP Module slot priority order from highest to lowest is A0, A1, B0, ... C1, D0, D1. See section 4 or Appendix D for more details regarding interrupt prioritization. The following examples illustrate several interrupt service priority schemes.

EXAMPLE 1:

In this example, all interrupters are set to the same interrupt request level.

- Write '0x0011' to Interrupt Level register A
- Write '0x0011' to Interrupt Level register B
- Write '0x0011' to Interrupt Level register C
- Write '0x0011' to Interrupt Level register D

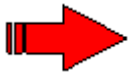
Now all eight interrupt sources are set to interrupt request level 1. If all eight sources assert an interrupt request at the same time, they will be serviced in the following order: A0, A1, B0, B1, C0, C1, D0, D1.

EXAMPLE 2:

In this example, the interrupt request levels are set to different values to illustrate that the interrupt-request-level prioritization takes precedence over the slot prioritization.

- Write '0x0011' to Interrupt Level register A
- Write '0x0022' to Interrupt Level register B
- Write '0x0032' to Interrupt Level register C
- Write '0x0054' to Interrupt Level register D

For this configuration, if all eight sources assert an interrupt request at the same time, they will be serviced in the following order: D1, D0, C1, B0, B1, C0, A0, A1.



NOTE: It is not normally possible to assert simultaneous interrupt requests, except via special IP Modules like the Curtiss-Wright Controls TESTIP.

B.6.3 Memory Space Example

Certain IP Modules use or require memory space for their operation. Examples of such devices include non-volatile storage boards, MIL-STD 1553 IP Modules, or IP Modules that simply require additional address space. The following examples show how to configure the V64XSC4 to allow accesses to the memory space of installed IP Modules.

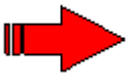
EXAMPLE 1

In this example, the V64XSC4 is programmed to use VME A24 base address location '0x800000' for IP Module memory accesses. Write the appropriate address value to the Memory Base register (table B-6) so the carrier at that address will operate in A24 mode. It is also necessary to write a '1' to the Memory Enable register (table B-8) for operation in A24.

- Write '0x0080' to the A24 Memory Base register
- Write '0x0001' to the Memory Enable register

By writing '0x0080' to the A24 Memory Base register you are selecting a specific V64XSC4 carrier memory address. Also, by enabling memory a read or write to a specific VME address is possible. A read or write to '0x800000' through '0xBFFFFF' will initiate an access to the appropriate memory location of an IP Module on this carrier. In this example, locations '0x800000' through '0x8FFFFF' will be used for IP Module slot 'A,' locations '0x900000' through '0x9FFFFF' will be used for IP Module slot 'B,' for IP Module 'C,' locations '0xA00000' through '0xAFFFFF' will be used, and for IP Module 'D' locations '0xB00000' through '0xBFFFFF' will be used. Access within each one of these 1MB regions will initiate an access to the appropriate memory location of the relevant IP Module.

Keep in mind that the V64XSC4 is byte-addressed while the IP Modules are word-addressed. The memory address used for the IP Module is half of the difference between the address used and the actual address corresponding to the base of the IP Modules memory region. For instance, a read from '0x808210' will result in a read to IP Module A address '0x4108,' as the IP Modules are word addressed. '0x808210' - '0x800000' = '0x8210,' '0x8210' / 2 ='0x4108'.



NOTE: Addresses are A24 VME addresses and not necessarily host addresses. The A24 address space may be mapped into a different location for the host CPU. In addition, your host computer may not support the full range of this address space. See the documentation for your VME Single Board Computer for more details.

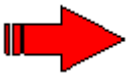
EXAMPLE 2:

In this example, the V64XSC4 is programmed to use VME A32 base address location '0xFE000000' for IP Module memory accesses. Write the appropriate address value to the Memory Base register (table B-6) so the carrier at that address will operate in A32 mode. It is also necessary to write a '3' to the Memory Enable register (Table B-8) for operation in A32.

- Write '0x00FE' to the A32 Memory Base register
- Write '0x0003' to the Memory Enable register

By writing a '0x00FE' to the A32 Memory Base register you are selecting a specific V64XSC4 carrier memory address. Also, by enabling memory and space select a read or write to a specific VME address is possible. A read or write to '0xFE000000' through '0xFFFFFFFF' will initiate an access to the appropriate memory location of an IP Module on this carrier. In this example, locations '0xFE000000' through '0xFE7FFFFF' will be used for IP Module slot 'A', locations '0xFE800000' through '0xFEFFFFFF' will be used for IP Module slot 'B', for IP Module 'C' , locations '0xFF000000' through '0xFF7FFFFF' will be used, and for IP Module 'D' locations '0xFF800000' through '0xFFFFFFFF' will be used. Access within each one of these 8 MB regions will initiate an access to the appropriate memory location of the relevant IP Module.

Keep in mind that the V64XSC4 is byte-addressed while the IP Modules are word-addressed. The memory address used for the IP Module is half of the difference between the address used and the actual address corresponding to the base of the IP Modules memory region. For instance, a read from '0xFE008210' will result in a read to IP Module A address '0x4108', as the IP Modules are word addressed. '0xFE008210' - '0xFE000000' = '0x8210;' '0x8210' / 2 ='0x4108.'



NOTE: Addresses are A32 VME addresses and not necessarily host addresses. The A32 address space may be mapped into a different location for the host CPU. In addition, the full range of this address space may not be supported on your host computer. See the documentation for your VME Single Board Computer for more details.

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APPENDIX C

PERFORMANCE

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C.1 Overview

This section provides logic analyzer snapshots describing typical performance parameters beyond those provided section 2.1.1: “Features.” Remember, these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in chapter 2. Product Overview.

C.2 State Timing Diagrams

The V64XSC4 test configuration consisted of a typical VME card cage with a host MVME-162-23 CPU and four Curtiss-Wright TESTIP modules. State waveforms were generated using the HP 1 GHz Timing Master Module and the Curtiss-Wright IP Module Logic Bus Breakout Board (IPLBB). The IPLBB was attached to a TESTIP in slot ‘A’ (refer to Figure C-1 for the performance test equipment configuration). Figures C-2 through C-12 show these state waveforms. Several of the signals on the logic analyzer’s screen are active low. The active low signals have a ‘/’ as the first character. The signals are defined and summarized on page C-2.

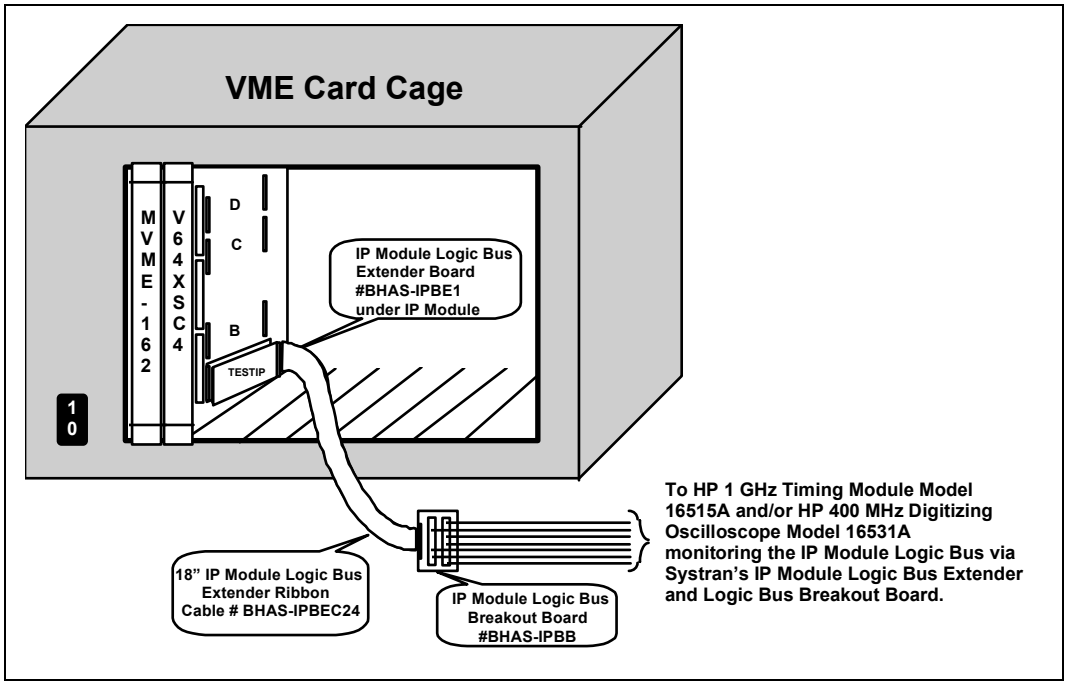


Figure C-1 Performance Test Equipment Configuration

GLOSSARY OF SIGNALS

/ACK ----------IP Module acknowledgment (active low)
/DTACK ----------VME data transfer acknowledge (active low)
/IAKIN ----------VME interrupt acknowledge in (active low)
/IAKOT ----------VME interrupt acknowledge out (active low)
ICLK----------IP Module 8 Mhz clock
/IDSEL ----------IP Module ID select signal (active low)
/INTRQ----------IP Module interrupt request signal 0 (active low)
/INTSL ----------IP Module interrupt select signal (active low)
IPD1 ----------IP Module data bit 1
/IOSEL ----------IP Module I/O select signal (active low)
/MEMSL ----------IP Module Memory select signal (active low)
SYSCLK ----------VME 16 Mhz system clock
VMEA1 ----------VME address bit 1
VMED0 ----------VME data bit 0
VMED1 ----------VME data bit 1
/VMEAS ----------VME address strobe (active low)
/VMEDS ----------VME data strobe 0 (active low)
/VIACK ----------VME interrupt acknowledge (active low)
/VMEIR ----------VME interrupt request 1(active low)
VMER/W ----------VME write signal (low is write, high is read)

C.2.1 ID Read Cycle

Figure C-2 is a complete ID read cycle of the V64XSC4 slot 'A' TESTIP. On the left side of the figure the host CPU initiates a VME read cycle by asserting a valid address (VMEA1). A valid address is followed by the assertion of the VME address and data strobe (/VMEAS and /VMEDS) signals. Within one ICLK period, after the host CPU has begun a valid read to the ID space of IP Module A, the V64XSC4 begins an IP Module read cycle by asserting the /IDSEL signal.

In the very next ICLK period, the TESTIP begins driving the data bus (/IPD1) and asserts the /ACK signal to complete the IP Module read cycle. Toward the right side of the figure, the V64XSC4 latches the data from the TESTIP on the rising edge of ICLK (at the end of the /ACK assertion) and drives the VME data bus. The V64XSC4 asserts the VME data acknowledge (/DTACK) signal about 1 to 4 nanoseconds after the VME data bus is driven. The V64XSC4 then waits for the VME host CPU to terminate the VME read cycle by de-asserting the address and data strobe signals. After the VME host CPU terminates the VME read cycle, the V64XSC4 releases the data bus and de-asserts the /DTACK signal. The entire VME read cycle is complete in four IP Module (8 MHz) clock cycles (which is 500 ns). The V64XSC4's worst- and best-case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the V64XSC4's average 500 ns.



Figure C-2 ID Read (Snapshot taken at 50 ns/Div)

C.2.2 I/O Read Cycle

Figure C-3 is a complete I/O read cycle of the V64XSC4 slot 'A' TESTIP, which is functionally the same as the ID read cycle. On the left side of the figure, the host CPU initiates a VME read cycle by asserting a valid address (VMEA1). The assertion of the VME address and data strobe (/VMEAS and /VMEDS) signals are followed by a valid address. Within one ICLK period after the host CPU has asserted a valid access, the V64XSC4 begins an IP Module read cycle by asserting the /IOSEL signal.

In the very next ICLK period, the TESTIP begins driving the data bus (/IPD1) and asserts the /ACK signal to complete the IP Module read cycle. Toward the right side of the figure, the V64XSC4 latches the data from the TESTIP on the rising edge of ICLK (at the end of the /ACK assertion) and drives the VME data bus. The V64XSC4 asserts the VME data acknowledge (/DTACK) signal about 1 to 4 nanoseconds after the VME data bus is driven. The V64XSC4 then waits for the VME host CPU to terminate the VME read cycle by de-asserting the address and data strobe signals. After the VME host CPU terminates the VME read cycle, the V64XSC4 releases the data bus and de-asserts the /DTACK signal. The entire VME read cycle is complete in four IP Module (8 MHz) clock cycles (which is 500 ns). The V64XSC4 worst- and best-case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the V64XSC4's average 500 ns.

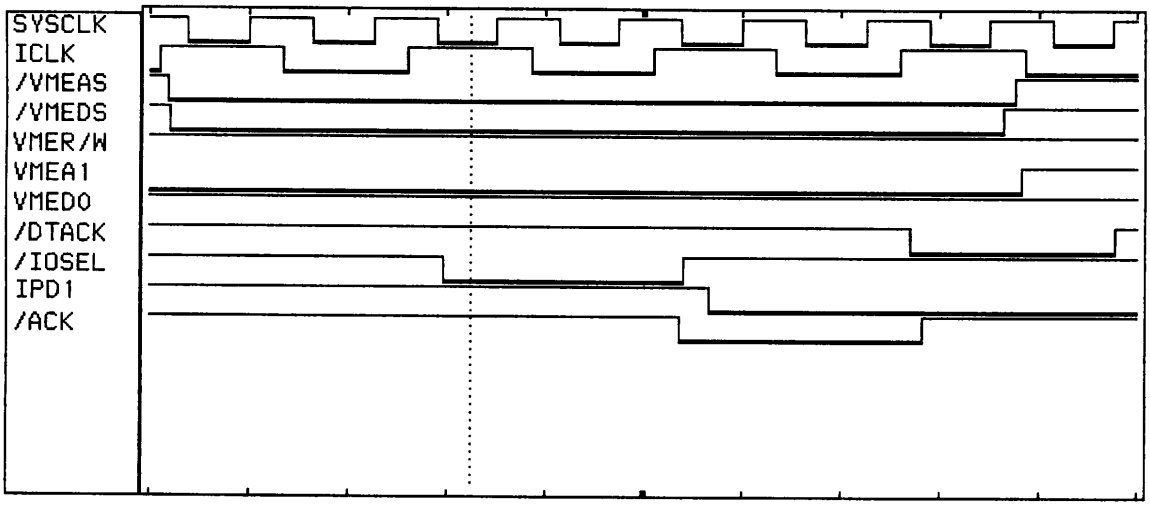


Figure C-3 I/O Read (Snapshot taken at 50 ns/Div)

C.2.3 I/O Write Cycle

Figure C-4 is a complete I/O write cycle of the V64XSC4 slot 'A' TESTIP. On the left side of the figure, the host CPU initiates a VME write cycle by asserting a valid address and drives the VME data bus with valid data. Valid data is present only while the write signal (VMER/W) is low. The assertion of the address and data strobes (/VMEAS and /VMEDS respectively) follows a low VMER/W signal. Within one ICLK period, after the host CPU has asserted a valid access, the V64XSC4 begins an IP Module write cycle by asserting the /IOSEL signal.

In the very next ICLK period, the TESTIP asserts the /ACK signal to complete the IP Module write cycle and latches the data from the VME bus on the rising edge of ICLK (at the end of the /ACK assertion). The TESTIP latches the data 1 to 4 nanoseconds after the V64XSC4 asserts the VME data acknowledge (/DTACK) signal. The V64XSC4 then waits for the VME host CPU to terminate the VME write cycle by de-asserting the address and data strobe signals. After the host CPU terminates the VME write cycle the V64XSC4 de-asserts the /DTACK signal ending the write cycle. In this instance, the entire VME write cycle completes in approximately four IP Module (8 MHz) clock cycles (which is 500 ns). The V64XSC4 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the V64XSC4's average 500 ns. Although not shown, the ID WRITE cycle is functionally the same as the I/O WRITE cycle. The only difference is that the ID_SEL is asserted rather than the IO_SEL line.

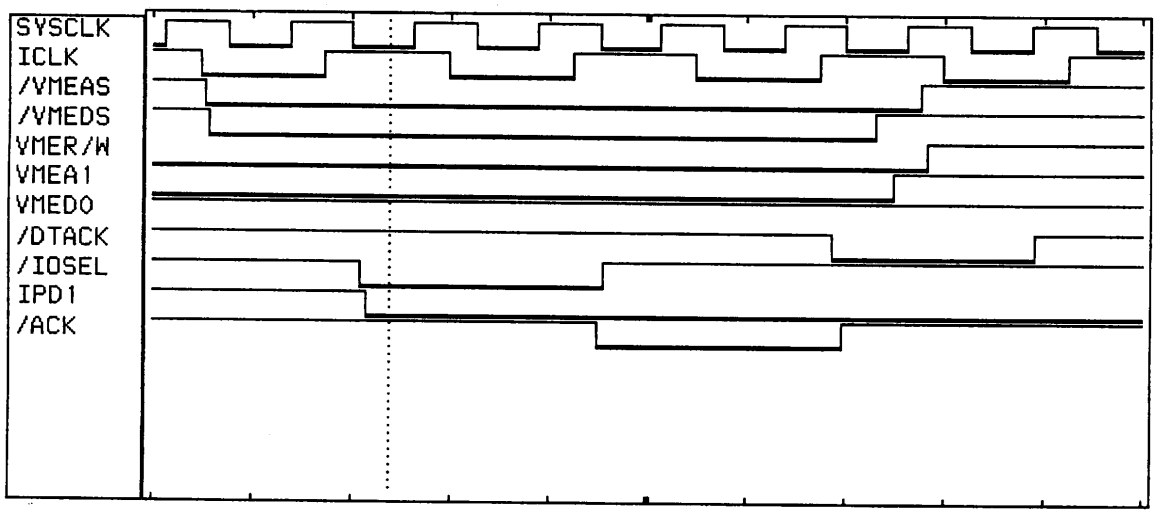


Figure C-4 I/O Write (Snapshot taken at 50 ns/Div)

C.2.4 Memory Read Cycle

Figure C-5 is a complete memory read cycle of the V64XSC4 slot 'A' TESTIP. The host CPU initiates a read cycle by driving the read (VMER/W) signal high while also driving a valid address (VMEA1). The host CPU follows a valid address by asserting its address and data strobes (/VMEAS and /VMEDS). Within one ICLK period, the V64XSC4 begins an IP Module read cycle by asserting the /MEMSL signal.

In a memory read cycle the IP Module data bus is used to drive the upper IP Module address lines (A22:A7). This "extended" address is valid during the select state of the IP Module transfer cycle. In the very next ICLK period, the TESTIP begins driving the data bus (/IPD1) and acknowledges the read and completes the IP Module read cycle by asserting the /ACK signal. On the right side of the figure, the V64XSC4 latches the valid data from the TESTIP on the rising edge of ICLK (toward the end of the /ACK signal's assertion) and begins to drive the VME data bus. About 1 to 4 nanoseconds after the VME data bus is driven the V64XSC4 asserts the VME data acknowledge (/DTACK) signal. The V64XSC4 then waits for the VME host CPU to terminate the VME read cycle by de-asserting the address and data strobe signals. After the VME host CPU terminates the VME read cycle, the V64XSC4 releases the data bus and de-asserts the /DTACK signal. The entire VME read cycle is complete in four IP Module (8 MHz) clock cycles (which is 500 ns). The V64XSC4's worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the V64XSC4's average 500 ns.

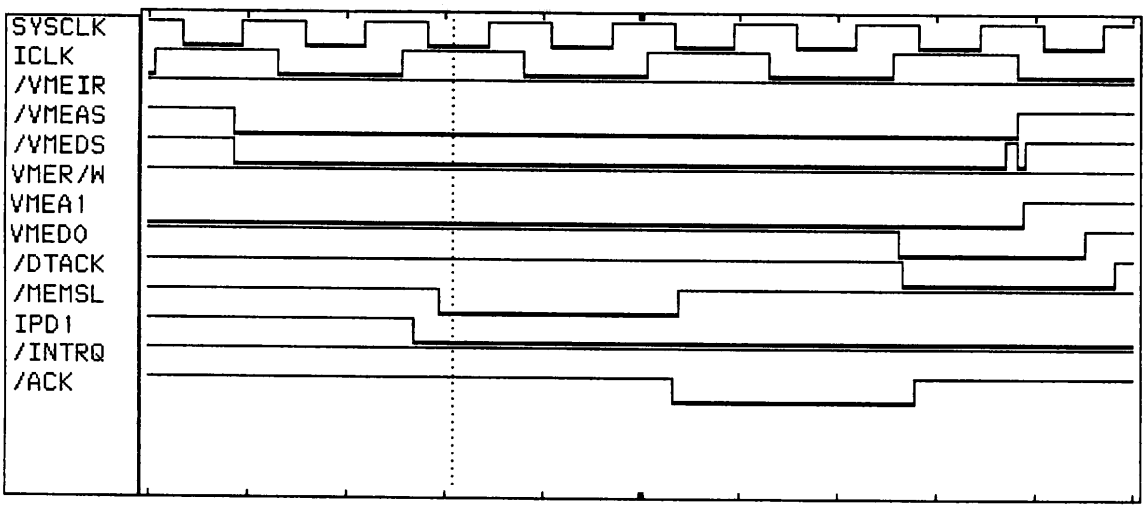


Figure C-5 Memory Read (Snapshot taken at 50 ns/Div)

C.2.5 Memory Write Cycle

Figure C-6 is a complete memory write cycle of the V64XSC4 slot ‘A’ TESTIP . On the left side of the figure, the host CPU initiates a VME write cycle by driving the ‘VMER/W’ signal low, while also asserting a valid address and data. The valid address and data is followed by the active low assertion of the VME address and data strobes (/VMEAS and /VMEDS) signals. Within one ICLK period after the host CPU has begun a valid access, the V64XSC4 begins an IP Module write cycle by asserting the /MEMSL signal.

In the very next ICLK period, the TESTIP asserts the /ACK signal to complete the IP module write cycle and latches the data from the VME bus. The TESTIP latches the data about 1 to 4 nanoseconds after the V64XSC4 asserts the VME data acknowledge (/DTACK) signal. The V64XSC4 then waits for the VME host CPU to terminate the VME write cycle by de-asserting the address and data strobe signals. Finally, upon the de-assertion of the address and data strobe the VME host CPU terminates the VME write cycle and the V64XSC4 de-asserts the /DTACK signal. In this instance the entire VME write cycle finishes in approximately four IP Module (8 MHz) clock cycles (which is 500 ns). The V64XSC4 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the V64XSC4’s average 500 ns.



Figure C-6 Memory Write (Snapshot taken at 70 ns/Div)

C.2.6 I/O Read-Modify-Write Cycle

Figure C-7 is a complete I/O read-modify-write cycle of the V64XSC4 slot ‘A’ TESTIP. On the left side of the figure, the host CPU initiated a VME read cycle by asserting a valid address and then asserting the VME address and data strobe (/VMEAS and /VMEDS) signals. The read cycle completes when the /DTACK is toggled. In the center of the figure, the VME host CPU de-asserts the data strobe signal while keeping the address strobe asserted. A few clock cycles later, the host CPU begins a VME write cycle by asserting a valid address and data line along with the VME write (VMER/W) signal and then re-asserts the VME data strobe (/VMEDS) signal. On the right side of figure, the write cycle terminates normally when the address and data strobes are de-asserted, completing the VME read-modify-write cycle. Notice that the complete read-modify-write cycle was executed by the host CPU in approximately 1.8 µs.

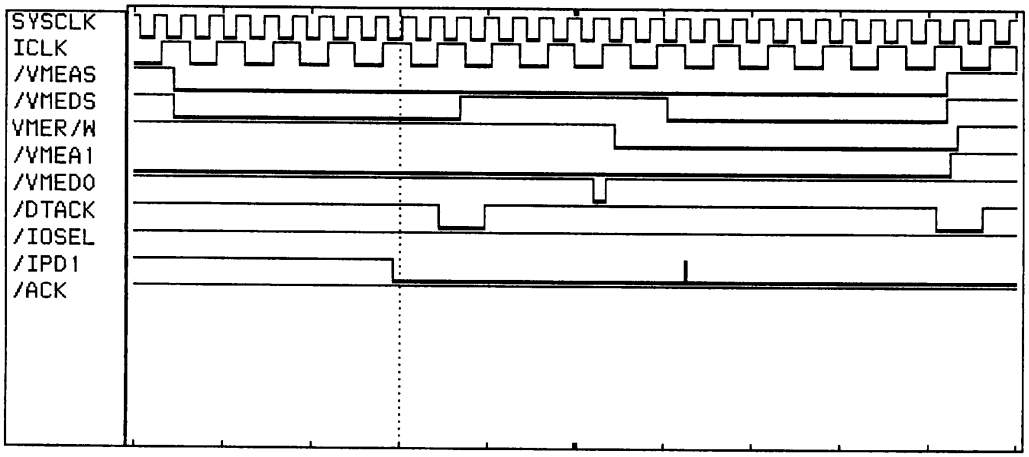


Figure C-7 Read-Modify-Write (Snapshot taken at 200 ns/Div)

C.2.7 I/O Write Cycle With IP Module Wait States

Figure C-8 is a complete I/O write cycle of the V64XSC4 slot ‘A’ TESTIP. This test is similar to Figure 5-4 except that IP Module wait states are inserted. On the left side of the figure, the host CPU initiates a VME write cycle by asserting a valid address and drives the VME data bus with valid data. This occurs only while the address and data strobe (/VMEAS and /VMEDS) and the VMER/W signal are asserted low. Next, the V64XSC4 begins an IP Module write cycle by asserting the /IOSEL signal. In the center of the figure, the TESTIP has inserted five IP Module wait states and then asserts the /ACK signal to complete the IP Module write cycle. Then, on the right side of the figure, the write cycle terminates normally as in Figure C-4 completing the VME write cycle with wait states. Note that the V64XSC4 supports ID, IO, memory, and Interrupt IP module cycles with inserted wait states.

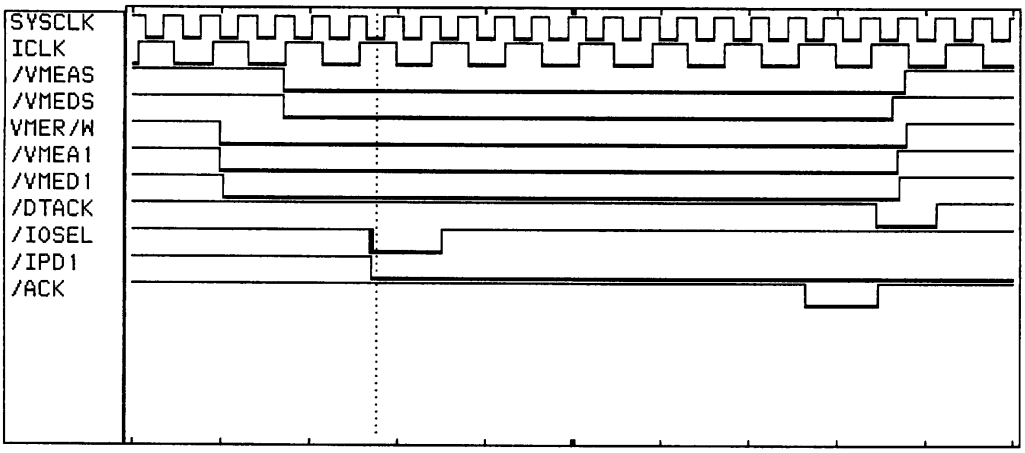


Figure C-8 I/O Write With Wait States (Snapshot taken at 150 ns/Div)

C.2.8 Interrupt Request

Figure C-9 is a waveform view of a complete interrupt request from the TESTIP and the following interrupt service routine (ISR) from the host CPU. The V64XSC4 was configured to drive the VME interrupt level one request (/VMEIR) when the TESTIP asserted the IP Module interrupt request signal zero (/INTRQ). First, the TESTIP asserts an interrupt request and in response to this action, the V64XSC4 asserts the VME interrupt request to the host CPU. Then about 1.5 µs later, the host CPU begins an interrupt acknowledge cycle. This interrupt acknowledge cycle fetches the interrupt vector from the TESTIP and services the interrupt. In the center of the figure, the host CPU is reading a status register on the TESTIP. The host CPU then performs a write to the TESTIP to clear the interrupt request. In response to the de-assertion of the IP Module interrupt request, the V64XSC4 de-asserts the VME interrupt request. Figures C-10 and C-11 show more detail timing data of the V64XSC4 interrupt cycles.

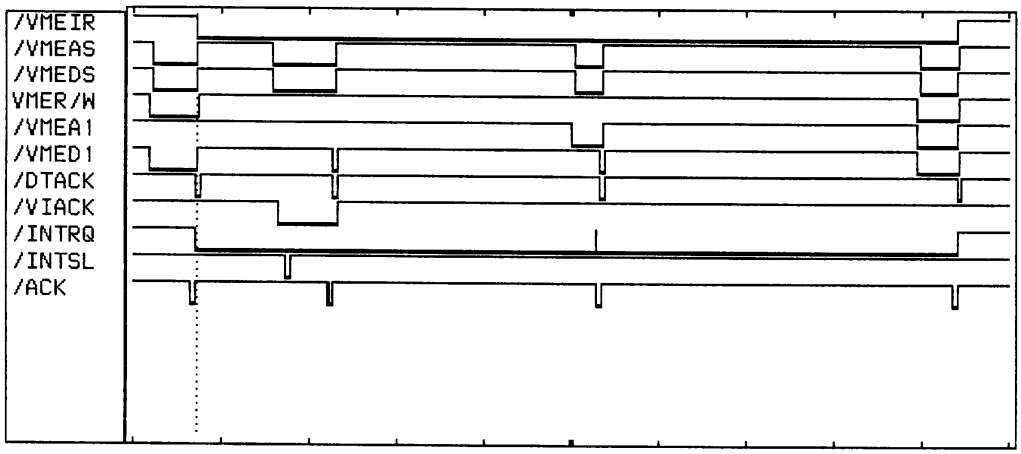


Figure C-9 Complete Interrupt Request and Service Routine (Snapshot taken at 2.00 µs/Div)

Figure C-10 is a zoomed-in view of the TESTIP driving its interrupt request (/INTRQ) signal and in turn the V64XSC4 driving the VME interrupt request signal (/VMEIR) in about 20 ns.

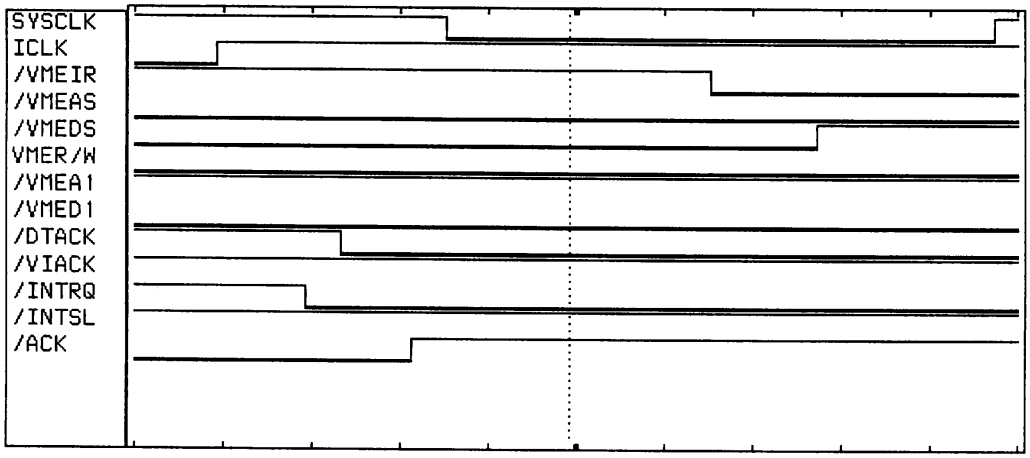


Figure C-10 IP Module INTRQ0 Driving VME IRQ1 (Snapshot taken at 5 ns/Div)

Figure C-11 is a zoomed in view of the TESTIP placing an interrupt vector onto the VME data bus. This interrupt vector cycle functions the same as the ID and IO read cycles. On the left side of the figure, the host CPU initiates an interrupt acknowledge cycle by asserting a valid address. The valid address (presented on VMEA3:1) determines which of the interrupt requests are to be serviced. The VME address strobe, VME data strobe, and interrupt acknowledge input signals (/VMEAS, /VMEDS, and VIACK) are asserted after the address line is valid. Next, in the center of the figure, the interrupt select (/INTSL) signal is asserted. This denotes the beginning of an IP module interrupt cycle. This can only happen after the V64XSC4's interrupt engine determines if the current interrupt acknowledge cycle is for that particular IP.

The V64XSC4 always begins an IP Module select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period, the TESTIP begins driving the data bus and asserts the /ACK signal to complete the IP Module interrupt acknowledge cycle. On the right side of the figure, the V64XSC4 latches the data from the TESTIP on the rising edge of ICLK (at the end of the terminate cycle) and drives the VME data bus. The V64XSC4 asserts the VME data acknowledge (/DTACK) signal 1 to 4 ns after the VME data bus is driven. The V64XSC4 then waits for the VME host CPU to terminate the VME interrupt acknowledge cycle by de-asserting the address strobes, data strobes, and IACKIN signals. After the VME host CPU terminates the VME interrupt acknowledge cycle, the V64XSC4 releases the data bus and de-asserts the /DTACK signal. The entire VME interrupt acknowledge cycle is complete in about four IP Module (8 MHz) clock cycles (which is 500 ns). Again the V64XSC4 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the V64XSC4's average 500 ns.

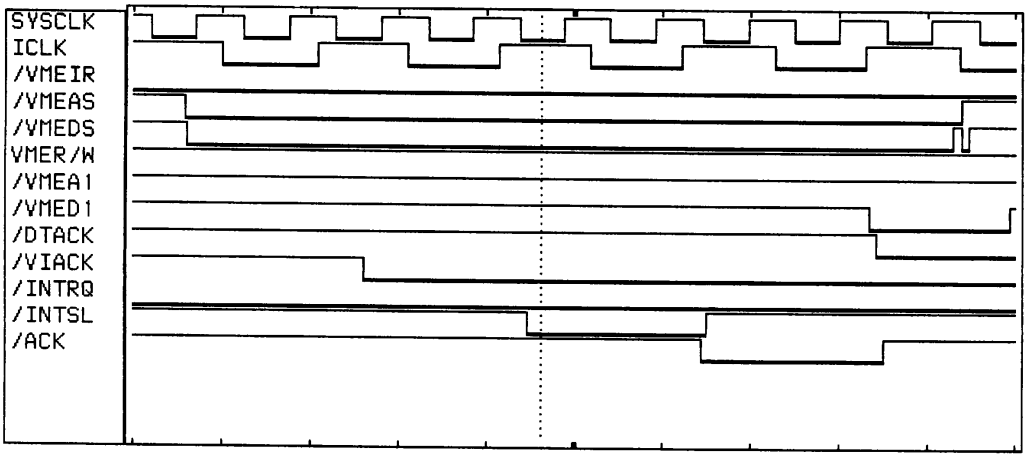


Figure C-11 IP Module Interrupt Vector Cycle (Snapshot taken at 60 ns/Div)

Figure C-12 is a zoomed in view of the V64XSC4 driving the VME IACKOUT (connected to /IAKIN on the next VME board) signal in about 36 ns. In this figure, the V64XSC4 interrupt engine determined that this interrupt acknowledge cycle was not for any of its IP Modules and very quickly passed on the /IAKOT signal in the VME daisy-chain.

NOTE: Figure C-12 is very important information if you are concerned about system response time with the VME IAKOT daisy-chain signal being passed along by the V64XSC4 (about 36 ns). This means that the V64XSC4 will not cause a VME system time-out or bus error by driving the IACKOUT (/IAKOT) signal as fast as possible. If a VME card cage had one host CPU (VME bus master) and twenty V64XSC4 IP Module carriers installed, the V64XSC4 in the slot furthest from the host CPU with an IP Module in slot 'D' will see the IACKIN (/IAKIN) signal in about .72 µs.

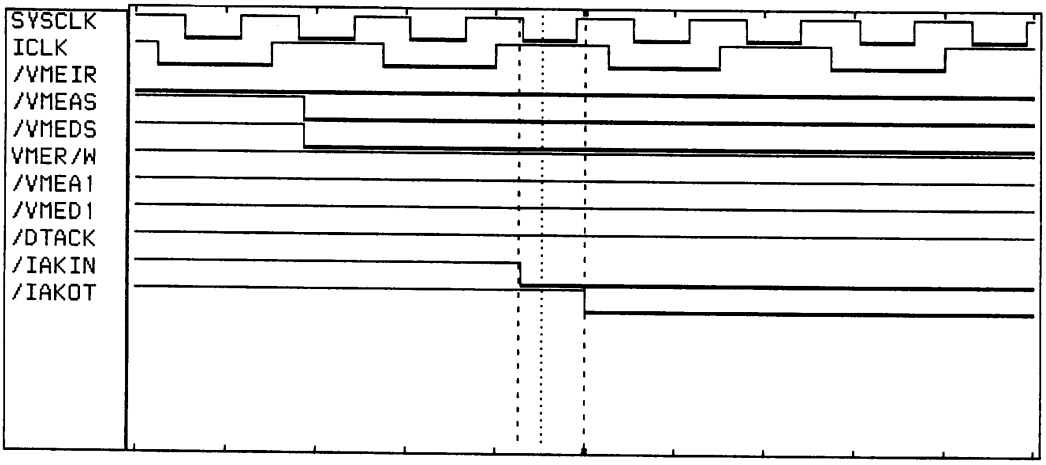


Figure C-12 VME Signals IACKIN to IACKOUT (Snapshot taken at 50 ns/Div)

Time between /IACKIN to /IACKOUT is 36 ns.

APPENDIX D

TYPICAL APPLICATIONS

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FIGURES

Figure D-1 A System With Two VME Masters D-1

D.1 Applications

The Systran division of Curtiss-Wright has an open product application submission policy. You may submit your V64XSC4 Slave Carrier and V64XT4L Transition Module application(s) to us to include in our application library. If we determine the submission will expand the product's functionality we will revise this section to include the application(s).

Submission constitutes permission to publish without additional consent or compensation, and Curtiss-Wright reserves the right to modify submissions to provide for more generic appeal, when necessary.

D.2 Sharing IP Modules Between Multiple VME Masters

It is sometimes desirable for multiple VME bus masters to share IP Module resources. In this case, a semaphore is typically used to lock out access to the resource when it is in use. This example illustrates using the General Purpose registers on the V64XSC4 for this purpose.

Figure D-1 depicts a system comprised of two VME masters, and one or more V64XSC4 carriers populated with I/O modules, in a process monitor and control application. In this hypothetical system, one master performs the process control functions while the second master monitors all of the I/O data values and reports the

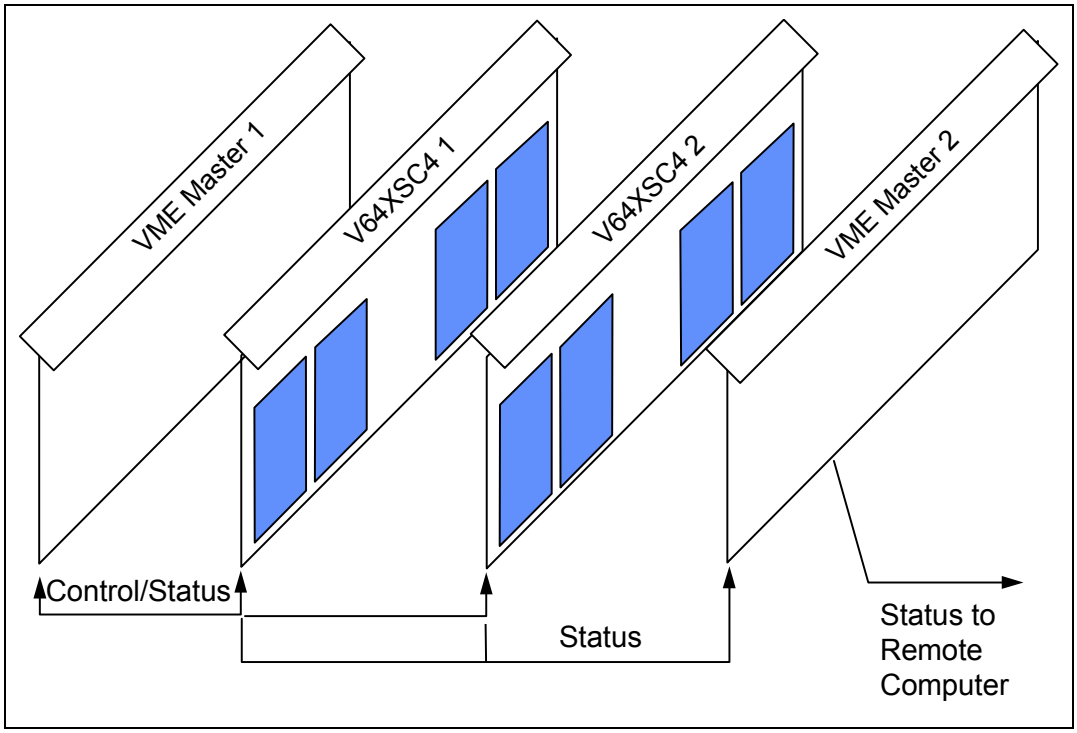


Figure D-1 A System With Two VME Masters

information to a remote computer. The second master is used because one master cannot handle both the process control and communication functions.

The data being reported to the remote computer from any one IP Module must be from the same frame. To insure this requirement is met, a separate semaphore is used for each

IP Module. The exchange of data between the VME masters and the IP Modules would then go something like this, where "x" is the last IP Module on the last carrier:

D.2.1 VME Master 1

- Reserve IP Module A semaphore (in General Purpose register A). If not available then wait until it is available.
- Set the new output values for IP Module A.
- Release IP Module A semaphore.
- •
- •
- •
- Reserve IP Module *x* semaphore (in corresponding General Purpose register). If not available then wait until it is available.
- Set the new output values for IP Module *x*.
- Release IP Module *x* semaphore.

D.2.2 VME Master 2

- Reserve IP Module A semaphore (in General Purpose register A). If not available then wait until it is available.
- Read the data from IP Module A.
- Release IP Module A semaphore.
- Send the IP Module A data to the remote computer.
- •
- •
- •
- Reserve IP Module x semaphore (in corresponding General Purpose register). If not available then wait until it is available.
- Read the data from IP Module x.
- Release IP Module x semaphore.
- Send the IP Module x data to the remote computer.

This is just one example of using the General Purpose registers. They are completely redefinable and you can use them for many purposes.

D.3 Configuring Interrupts for Multiple Priority Schemes

Some systems must run more than one application for a given hardware configuration. The two applications may require two distinct interrupt priority schemes. This example illustrates how to configure the interrupt level registers on the V64XSC4 to achieve two different priority schemes.

The following assumptions are used for this example:

1. The two applications each use four IP Modules, A through D.
2. Each IP Module utilizes interrupts IRQ0 and IRQ1.
3. Application one requires that the interrupts be serviced in the following order:
   C0, C1, B0, B1, A0, A1, D1, D0.
4. Application two requires that the interrupts be serviced in the following order:
   D1, D0, C0, C1, A0, A1, B0, B1.
5. Interrupt level 7 should not be used.

Recall that the IACK daisy chain slot priority is:
A0, A1, B0, B1, C0, C1, D0, D1
which represents the servicing order for equal level interrupt requests. Therefore, the solution is to set interrupt request levels to override the slot priority, where necessary, to achieve the desired servicing order.

To achieve the desired servicing order for application one, the interrupt levels could be set as follows:

- Write ‘0x0033’ to Interrupt Level register A
- Write ‘0x0044’ to Interrupt Level register B
- Write ‘0x0055’ to Interrupt Level register C
- Write ‘0x0022’ to Interrupt Level register D

To achieve the desired servicing order for application two, the interrupt levels could be set as follows:

- Write ‘0x0022’ to Interrupt Level register A
- Write ‘0x0022’ to Interrupt Level register B
- Write ‘0x0033’ to Interrupt Level register C
- Write ‘0x0054’ to Interrupt Level register D

In both cases, there is more than one combination of Interrupt Level register settings to produce the desired results.

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GLOSSARY

[x:y] ----------Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

Carrier ----------A 6U VME board which contains logic for converting the VME Bus to a IP Module Bus and has connectors for mounting IP Modules.

CSR ----------Control and Status Register.

doublewide----------An IP Module that is twice the size of the singlewide board.

DTE ----------Date Transfer Engine.

EPLD ----------Erasable Programmable Logic Device.

hit----------An assertion of an address-detect.

ID PROM ----------The circuitry that presents the proper data patterns to the low 8 bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IP Module ----------Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP Module logic bus ----------A synchronous, 4 MTransfers/sec, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6 bits wide (22 bits wide in memory mode).

IPDbus----------IP Module Data Bus.

ISR ----------Interrupt Service Routine

MTBF----------Mean Time Between Failures.

ns, µs, ms----------Nanoseconds, microseconds, and milliseconds respectively.

one-shot ----------Also mono-stable multi-vibrator. A circuit that generates a pulse for an amount of time determined by the resistor and capacitor in the circuit. For example: For the LEDs, asserts the reset signal for approximately 240 ms.

singlewide----------An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

Transition Module ----------A 6U VME board which has the interconnects for transitioning I/O signals from the Carrier. This Module is used in a VME64 Extensions backplane.

VHDL ----------Very high speed integrated circuit Hardware Description Language.

VME Extensions ----------A VME specification which allows 200 I/O points to be transitioned through the backplane using 160-pin DIN style connectors and a 95-pin 2.0 mm hard-metric connector.

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