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DID48

48-Channel Debounced Discrete Input Board Hardware Reference

Document No. B-T-MR-DID48###-A-0-A7



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CE

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's tristateable, 48-channel debounced discrete input IP Module board, referred to as the DID48 (Debounced, Input, Discrete, 48 channels) part number BHAS-DID48.

1.1.2 Scope

This reference manual covers the physical and operational description of the DID48, both from hardware and software perspectives. This manual also contains detailed technical information about the DID48's performance characteristics, and some typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1          file2             file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- *Systran I/O Products Technical Note #2001 entitled Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)
- *ANSI/VITA 4-1995* published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA. Phone: 480-951-8866, FAX: 480-951-0720, E-mail: info@vita.com, URL: www.vita.com

- Systran Corporation: www.systran.com

1.3 Quality Assurance

Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments (including software), contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **support@systran.com**
- Fax: **(937) 252-1349**
- World Wide Web address: www.systran.com

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- E-mail: **info@systran.com**
- World Wide Web address: www.systran.com

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2. PRODUCT OVERVIEW

2.1 Overview

The Systran 48-Channel Debounced Discrete Input board implements a general-purpose discrete input interface, featuring per-channel overvoltage-protected, bounce/noise elimination circuitry with interrupt-on-change support. The DID48 is a singlewide IP Module designed in accordance with *ANSI/VITA 4-1995 American National Standard for IP Modules*.

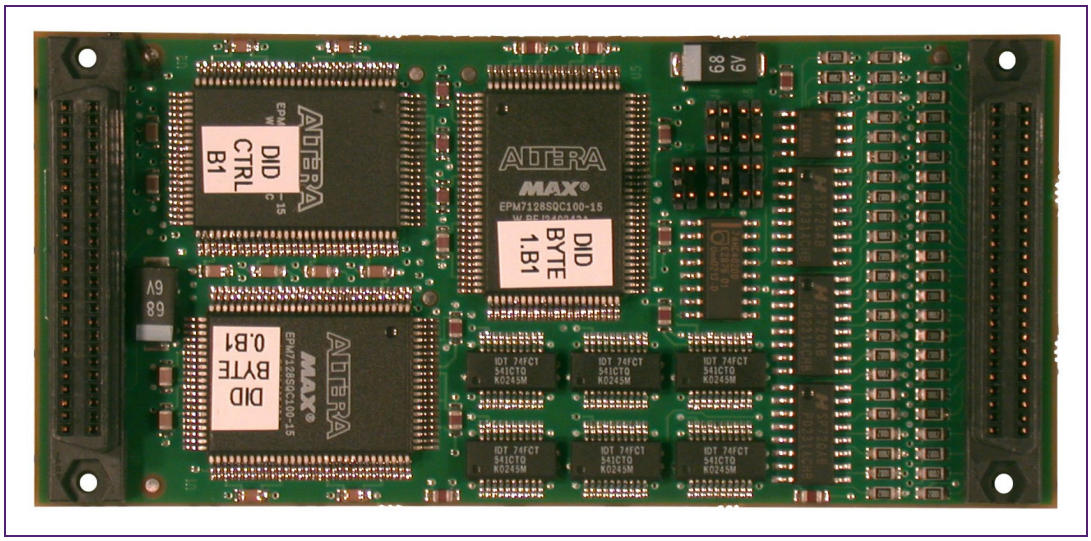


Figure 2-1 DID48 Board

2.2 Features

- 48 channels of hardware debouncing to one of four sampling window time periods: (256 µs, 1.024 ms, 4.096 ms, 16.384 ms).
- Eliminates need for software "debounce" algorithms.
- Software controlled per-byte-lane debounce disabling for direct drive inputs.
- All channels define a logic '1' or 'high' as any input voltage between +2.0 to +32.0 Vdc, and incorporate current-limited high clamps to +5 volts.
- All channels define a logic '0' or 'low' as any input voltage between -32.0 to +0.8 Vdc, and incorporate current-limited low clamps to ground.
- Simple Interrupt engine for signaling special events on any input logic change per-port granularity.
- The DID48's pin-out matches common digital and discrete I/O cards for peripheral compatibility, including screw terminal boards, signal conditioning boards, etc.

2.3 Related Products

- 'C' library and OS-9 device driver routines with documentation
- Windows NT 4.0 library software with documentation

2.4 Block Diagram Description

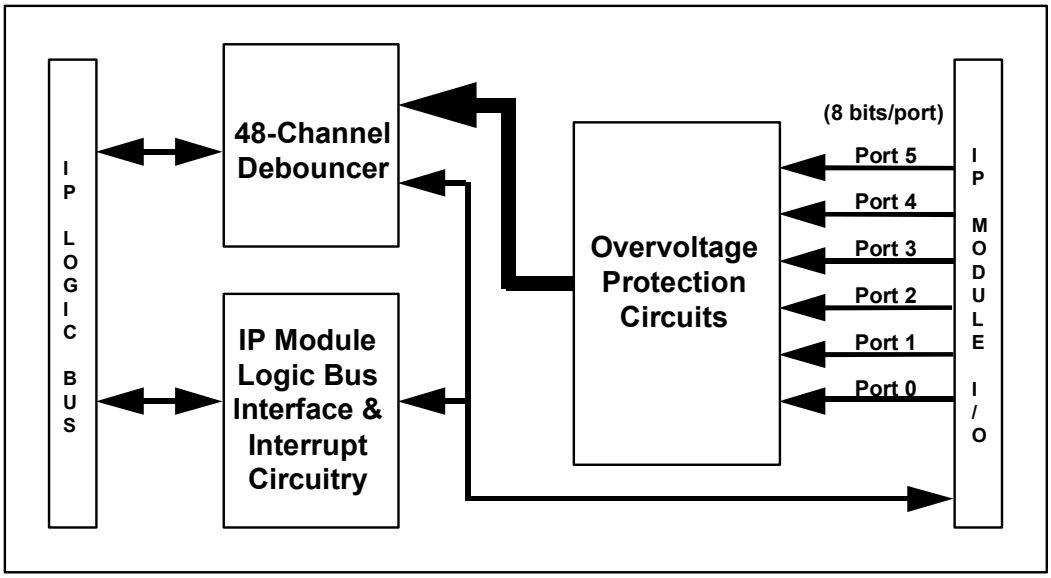


Figure 2-2 DID48 Block Diagram

Figure 2-2 is a simplified block diagram of the DID48 representing the signal flow between the IP Module Logic Bus and I/O connectors. On the left side of the diagram is the IP Module's Logic Bus connector through which all transfers between the IP Module carrier and the DID48's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface and Interrupt Circuitry" contains all of the read data ports, ID "PROM" data, control register, interrupt vector, interrupt control/status registers and interrupt engine, and IP Module sequence/control and data bus interface logic.

The block labeled "48-Channel Debouncer" contains the per-bit debouncing circuitry, implemented by byte-lane with two Altera EPLD devices. The block labeled "Overvoltage Protection Circuits" provides the per-input channel current-limited high and low clamps, implemented with individual SOIC-packaged logic and series current-limiting resistors. On the right side of the block diagram is the DID48's I/O connector where the six 8-bit data ports (48 discrete lines) are brought on-board, and a ground reference. Also, a debouncing sampling signal is provided on the DID48's I/O connector for external synchronization.

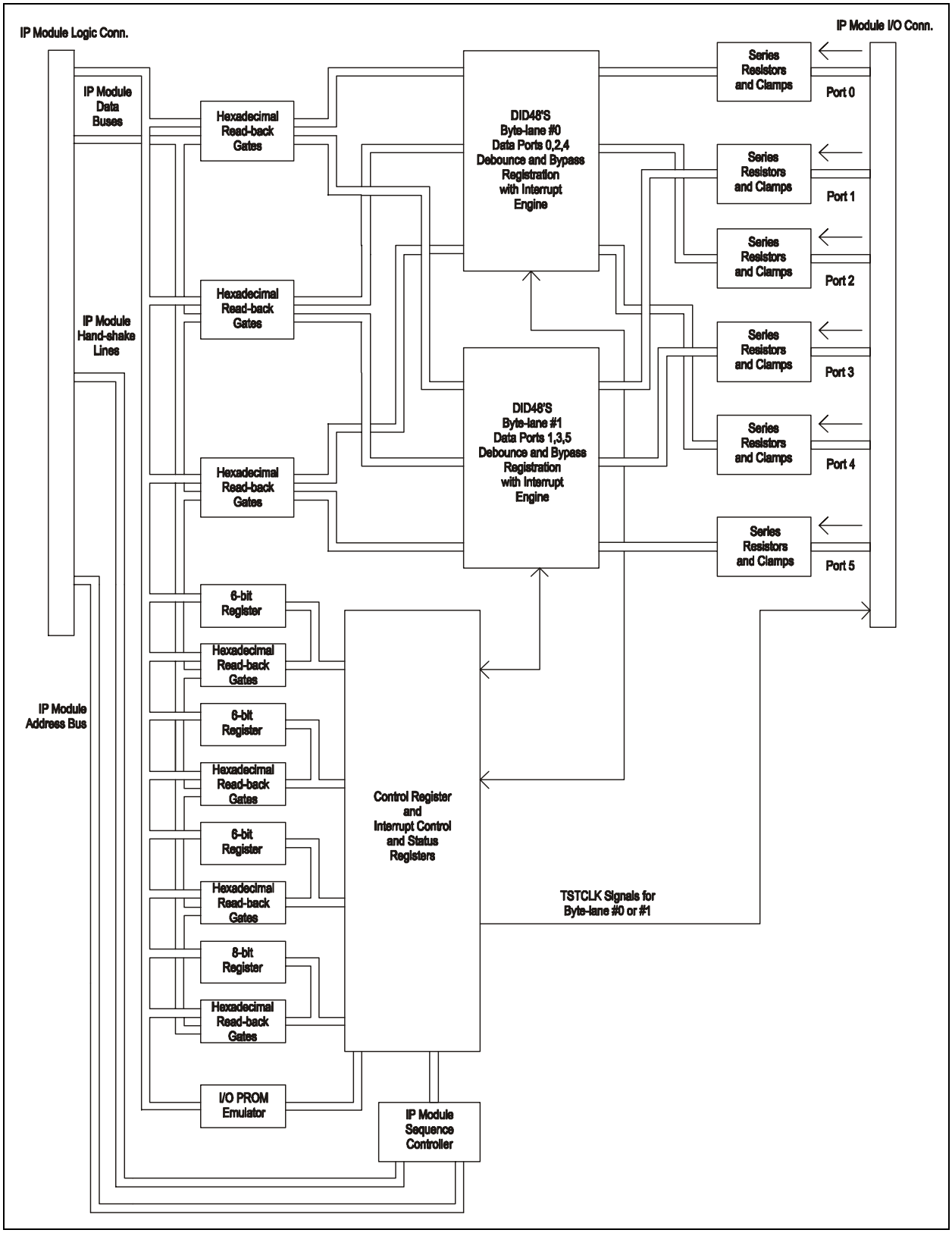


Figure 2-3 DID48 IP Board Detailed Block Diagram

Figure 2-3 presents a detailed block diagram of the DID48. As in the previous figure, on the left side is the IP Module's Logic Bus connector through which all host carrier transfers take place. The six 8-bit input data ports are paired into three 16-bit "words". Each "word" contains a 16-bit tristateable gate for driving the IP Module Data bus (IPDbus) during I/O reads. All I/O data port reads are performed at the "word" width of 16 bits only.

The block labeled "Control Register and Interrupt Control/Status Registers" has a similar IP Module carrier interface. This block's function is maintenance of the debounce enable/disabling for both byte-lanes. The interrupt control/status register's primary functions are maintenance of the interrupt engine.

These registers are for enabling, showing the status of the on-change port data and for registering and driving the interrupt vector.

The ID "PROM" Emulator is the circuitry that presents the proper data patterns to the low 8 bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers. Emulating the (never-changing) ID information in this way reduces parts count and costs, and increases system reliability with its associated Mean Time Between Failures (MTBF) value.

The blocks labeled "IP Module Sequence Controller" contain all of the control logic for performing orderly transfers between the DID48 and its carrier. The power-up default logic for this board is included in this section.

The blocks labeled "DID48's byte-lane 0 and 1 Data Ports 0, 2, 4 and 1, 3, 5 Debounce and Bypass Registration with Interrupt Engine" contain the debounce enabling (resolved independently for 256 µs, 1.024 ms, 4.096 ms, and 16.384 ms input sampling periods) or disabling of each byte-lane (three 8-bit data input port for direct drive inputs). For IP Module interrupts the N_INTREQ0 signal is driven if any (or all) Interrupt Status Register bits is(are) set AND the corresponding bit(s) in the Interrupt Enable Register is(are) also set.

The blocks labeled "Series Resistors and Clamps" contain 10 KΩ series resistors and high/low clamps on each input channel from the IP Module I/O connector.

2.5 Detailed Descriptions

The DID48 was developed using VHDL and Synthesis, targeted to an Altera EPLD, schematic captured and integrated to standard integrated circuits, connectors, and discrete components using VIEWLogic's ViewDraw and associated packages.

2.6 DID48 Components and Functions

Figure 2-4 shows the physical positions of the shunts and jumpers on the DID48 IP Module. Shunt H3 determines the debounce period for byte-lane 0, and if placed on J3 in the position closest to the IP Module Logic connector configures byte-lane 0 for a sampling period of 16.384 ms. H3 placed on J3 in the position closest to the I/O connector configures byte-lane 0 for 4.096 ms sampling period (factory default). Placing H3 on J5 in the position closest to the IP Module Logic connector configures the DID48 for 1.024 ms sampling period, and placing H3 in the position closest to the I/O connector on J5 configures byte-lane 0 for 256 µs sampling period.

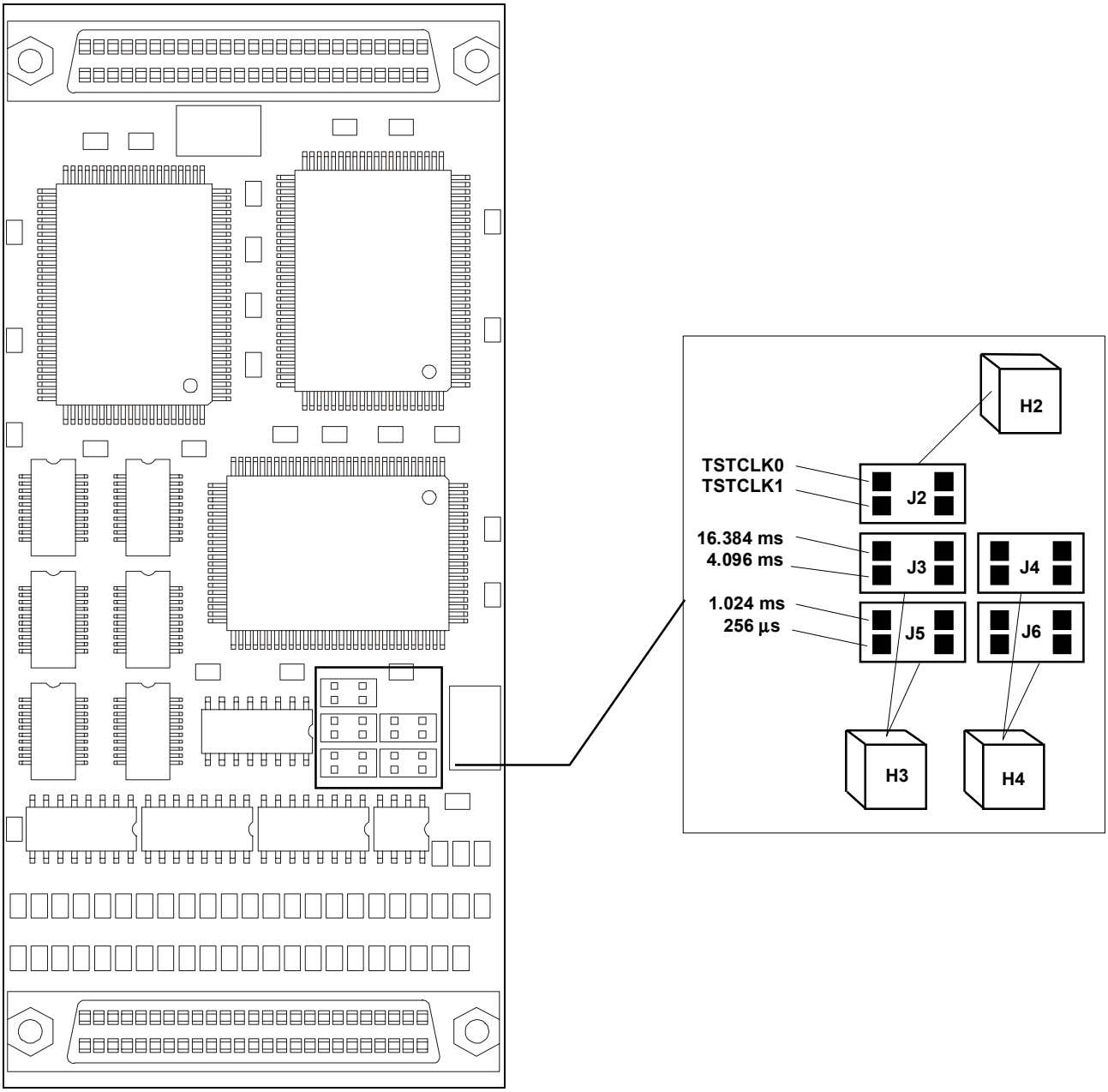


Figure 2-4 DID48 Jumper and Shunt Positions

For byte-lane 1, shunt H4 determines the debounce period, and if placed on J4 in the position closest to the IP Module Logic connector configures byte-lane 1 for a sampling period of 16.384 ms. H4 placed on J4 in the position closest to the I/O connector configures byte-lane 1 for 4.096 ms sampling period (factory default). Placing H4 on

J6 in the position closest to the IP Module Logic connector configures byte-lane 1 for 1.024 ms sampling period, and placing H4 in the position closest to the I/O connector on J6 configures the DID48 for 256 us sampling period.

Shunt H2 on J2 connects the TSTCLK0 (factory default) or TSTCLK1 signal to pin 49 of the I/O connector. If H2 is placed in the position closest to IP Module Logic Connector then the TSTCLK0 signal for port 0 is connected to the I/O connector. Consequently, if H2 is placed in the other position it connects TSTCLK1 to the I/O connector for port1.

The TSTCLK0 and TSTCLK1 signals (one for each byte-lane) pulse to a logic low for 125 ns once every debounce sample period. If debouncing is disabled, then the TSTCLK signals will pulse low once every 500 ns which is a 2 Mhz sampling rate. This signal was provided on the I/O connector for external synchronization.

DID48 CONTROLLER RESPONSIBILITIES

The DID48 Controller's primary responsibilities are registration of the Control register (debounce enable/disable) and Interrupt control/status/vector registers, emulation of the ID PROM data fields, handshake control of the IP Module I/O space driving of the data ports, and generation of the sampling period signal to each byte-lane controller. Figure 2-5 shows the inputs block diagram and debounce model contained in the byte-lane 0 and 1 controllers.

BYTE-LANE 0 RESPONSIBILITIES

The byte-lane 0 controller's primary responsibilities are to provide the IP Module interface operations for the data ports 0, 2, and 4 which are the lower 8 bits ([7:0]) of the 16 IP Module Data Bus bits (IPD[15:0]). The byte-lane 0 controller contains the debouncing logic programmable to one of four sampling periods determined by shunt H3 and jumpers J3 and J5, and contains the on-change logic (per-port granularity) used by the DID48 Controller to generate interrupts.

BYTE-LANE 1 RESPONSIBILITIES

The byte-lane 1 controller's primary responsibilities are exactly the same as byte-lane 0's and include the IP Module interface operations for the data ports 1, 3, and 5 which are the high 8 bits ([15:8]) of the 16 IP Module Data Bus bits (IPD[15:0]). The byte-lane 1's debounce logic is determined by shunt H4 and jumpers J4 and J6, and contains the on-change logic for data ports 1, 3, and 5. Also, the byte-lane 1 drives zeros onto IPD[15:8] bits during ID reads and I/O accesses to the control/interrupt registers.

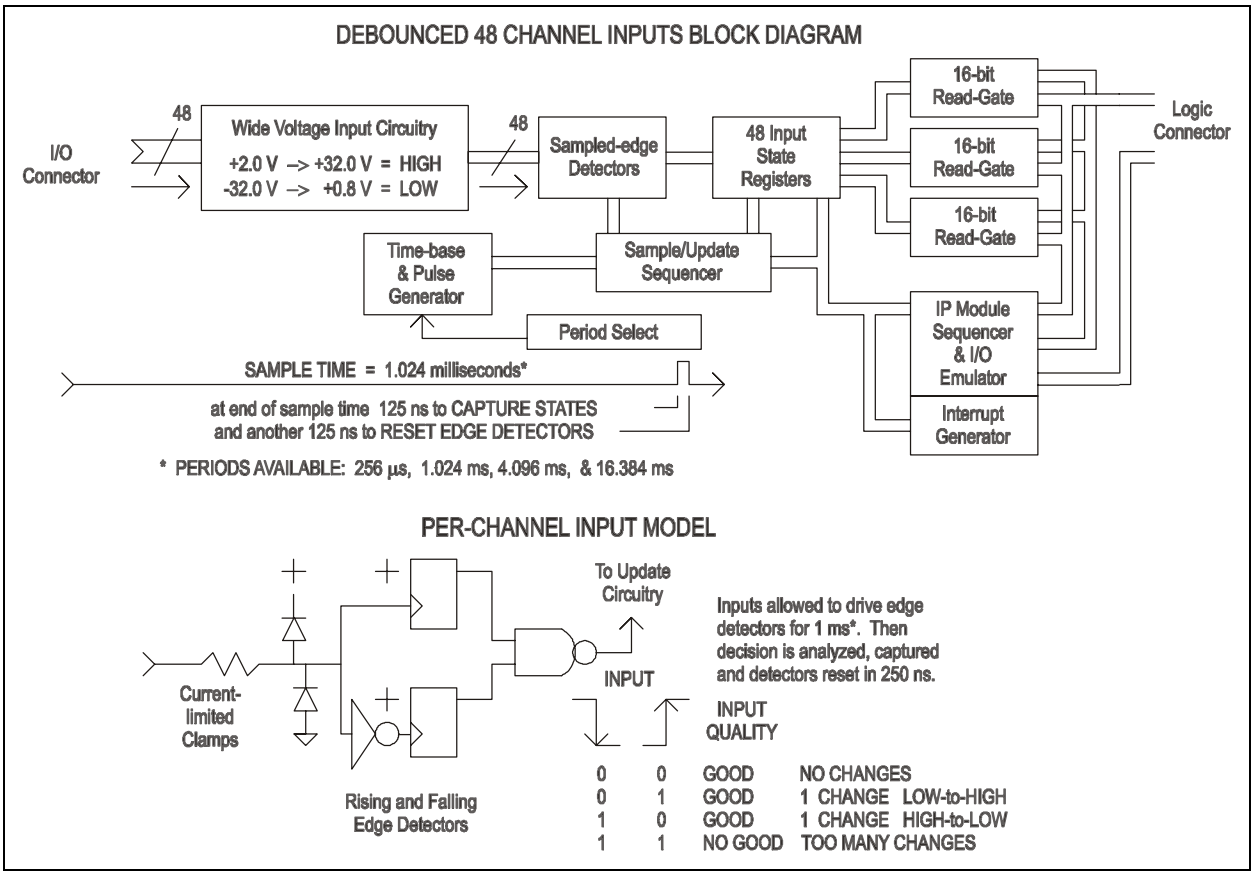


Figure 2-5 Inputs Block Diagram and Debounce Model

CURRENT-LIMITED CLAMPS

The 10 KΩ series resistors (R1-R48) on each input channel provide extra current-limiting protection against electrostatic discharge/overvoltage conditions beyond what is already in the Altera devices' input circuitry. The SP720AB/SP721ABs are arrays of SCR/Diode bipolar structures for the high/low discrete input clamps. They provide a logic '1' or 'high' clamping of any input voltage between +2.0 to +32.0 Vdc to a current-limited +5 Vdc. Correspondingly a logic '0' or 'low' of each input channel voltage between -32.0 to +0.8 Vdc is current-limited clamped to ground.



NOTE: If using interrupts, ground or pull up the unused inputs to prevent spurious interrupts. Also, for any pulse wider than the sampling period, two interrupts will be generated: one for the rising edge and one for the falling edge.

RELIABILITY

All of the components on the DID48 were carefully selected to ensure satisfactory operation and to provide the optimum features necessary to create a highly reliable (high MTBF numbers) and economical general-purpose digital I/O board.

2.7 DID48 Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol.



CAUTION: Do NOT use gasoline or thinner-type solvents on this product.

3. INSTALLATION

3.1 Unpack the DID48

The contents of the DID48 shipping packages are listed in Table 3-1:

Table 3-1 Contents of DID48 Shipping Packages

QTY	DESCRIPTION
1	DID48 Printed Circuit Assembly
1	DID48 Hardware Reference Manual *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped with each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (e.g., BTMR- DID48).

3.2 Inspect the DID48

Examine the DID48 to determine if any damage occurred during shipping.

3.3 Install the DID48



NOTE: The DID48 is an Electrostatic Sensitive Device (ESD). Install the DID48 on an anti-static workbench using good ESD practices to protect the IP Module and its host carrier board.

The DID48 installation requires the tools listed in Table 3-2.

Table 3-2 DID48 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

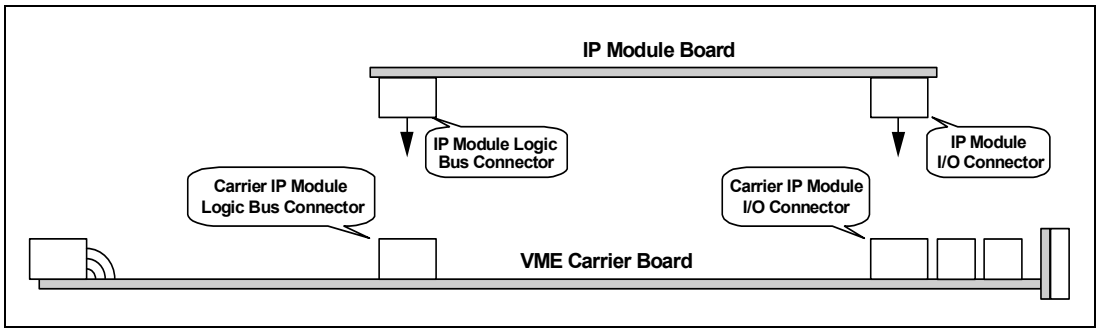


Figure 3-1 DID48 Installed on a VME IP Module Carrier

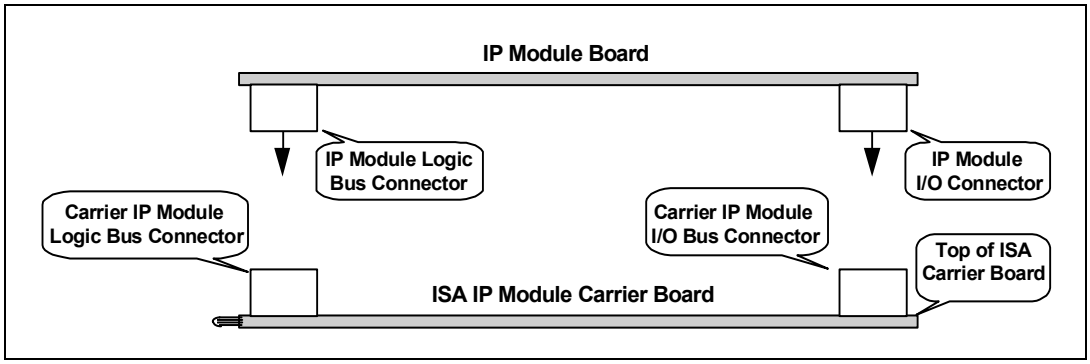


Figure 3-2 DID48 Installed on an ISA IP Module Carrier

Figure 3-1 and Figure 3-2 show how the DID48 is installed on a VME IP Module carrier, and on an ISA carrier, respectively.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals in the left column are of the original IP Module signal nomenclature, and the signals in the right column are those used by Systran Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board user's manual for more information.

Refer to the appropriate figures and table described above, and perform the following steps to install the DID48. The asterisk (∗) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the DID48 can be installed.
3. Remove the DID48 from the shipping package and place it on the ESD bench.
4. Install the DID48 onto the carrier board by applying adequate and equal pressure to the DID48 board at both ends.

* 5. Install four M2x5mm flat head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the DID48 to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Name
50	GND
49	TSTCLK (jumper select)
48	Port 5 Bit 0
47	Port 5 Bit 1
46	Port 5 Bit 2
45	Port 5 Bit 3
44	Port 5 Bit 4
43	Port 5 Bit 5
42	Port 5 Bit 6
41	Port 5 Bit 7
40	Port 4 Bit 0
39	Port 4 Bit 1
38	Port 4 Bit 2
37	Port 4 Bit 3
36	Port 4 Bit 4
35	Port 4 Bit 5
34	Port 4 Bit 6
33	Port 4 Bit 7
32	Port 3 Bit 0
31	Port 3 Bit 1
30	Port 3 Bit 2
29	Port 3 Bit 3
28	Port 3 Bit 4
27	Port 3 Bit 5
26	Port 3 Bit 6
25	Port 3 Bit 7
24	Port 2 Bit 0
23	Port 2 Bit 1
22	Port 2 Bit 2
21	Port 2 Bit 3
20	Port 2 Bit 4
19	Port 2 Bit 5
18	Port 2 Bit 6
17	Port 2 Bit 7
16	Port 1 Bit 0
15	Port 1 Bit 1
14	Port 1 Bit 2
13	Port 1 Bit 3
12	Port 1 Bit 4
11	Port 1 Bit 5
10	Port 1 Bit 6
9	Port 1 Bit 7
8	Port 0 Bit 0
7	Port 0 Bit 1
6	Port 0 Bit 2
5	Port 0 Bit 3
4	Port 0 Bit 4
3	Port 0 Bit 5
2	Port 0 Bit 6
	Port 0 Bit 7

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4. PERFORMANCE

4.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration citied, and do not supplant the maximum and minimum envelopes presented in Appendix A, SPECIFICATIONS.

4.2 State Timing Diagrams

The state waveforms for Figures 4-2 through 4-9 were made using the HP 1 GHz Timing Master Module and the Systran IP Module Logic Bus Extender (IPLBE) with the IP Module Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer‘s screen are active low, and are represented by a ‘/’ as the first character as opposed to the ‘N_’ used elsewhere, due to the limited amount of character spacing.

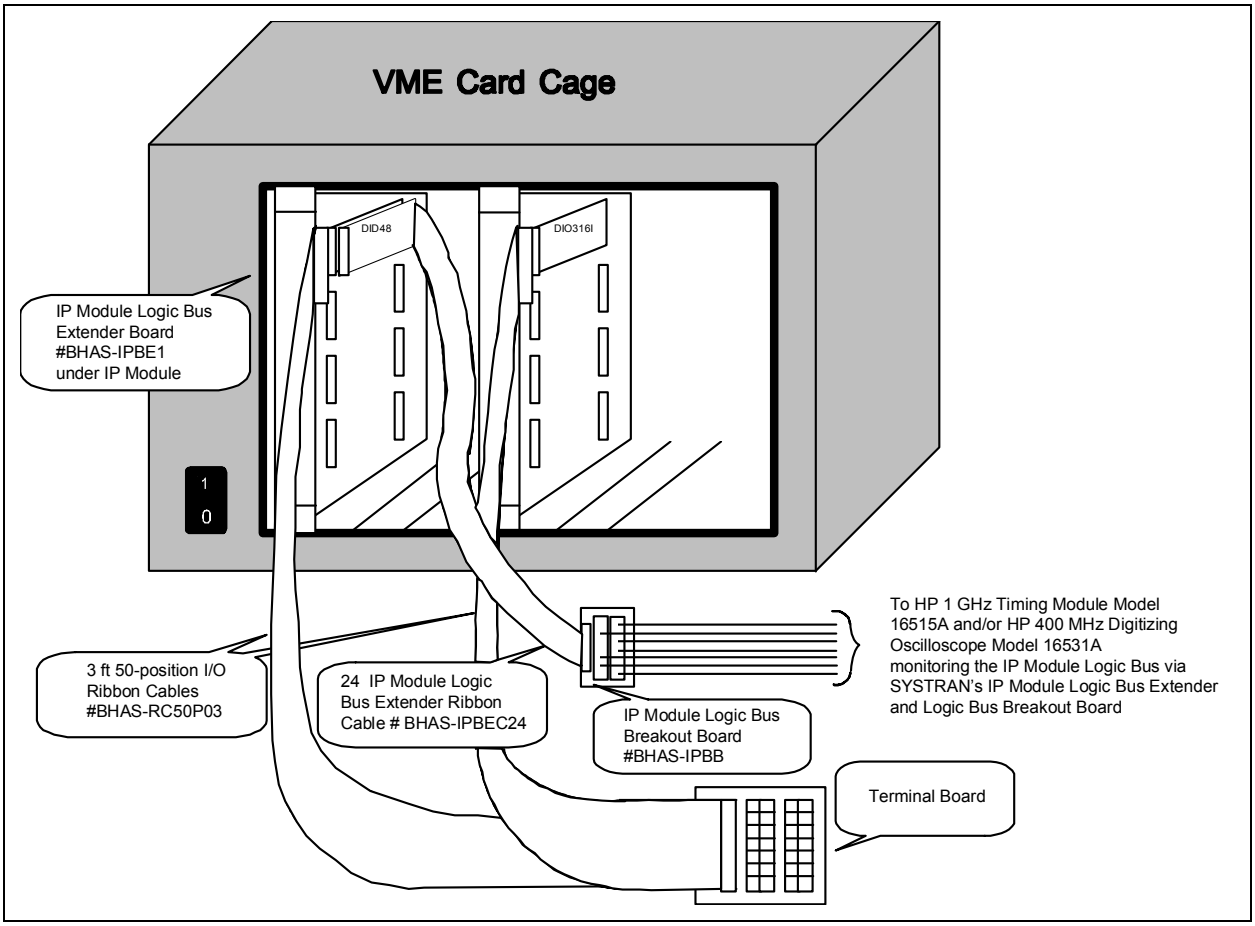


Figure 4-1 IP Module Test Configuration for State Timing Measurements

4.2.1 ID Read Cycle

Figure 4-2 is a complete DID48 ID read cycle. The signals of interest are /IDSEL, N_ACK, and the four IPD0-3 signals.

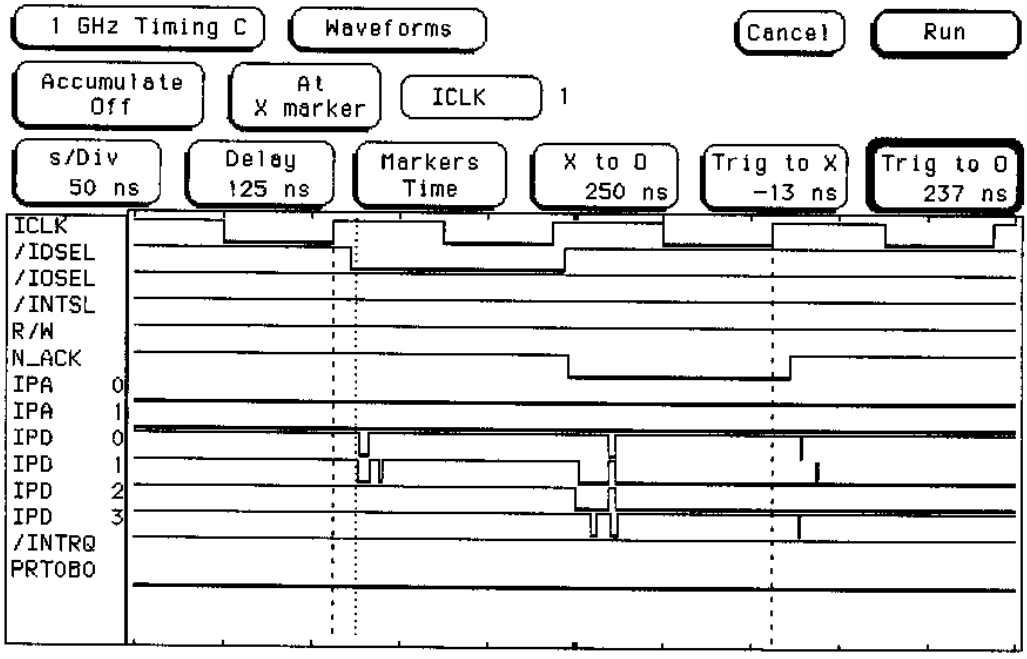


Figure 4-2 Complete DID48 ID Read Cycle

Figure 4-3 is a zoomed-in view of the DID48 ID cycle. It shows the DID48 driving the N_ACK and IPD0-3 signals in response to the rising edge of ICLK while /IDSEL is asserted. The typical response time is about 15 ns. The IP Module Logic I/F Specification (ANSI/VITA 4-1995) requires these signals be driven within 40 ns.

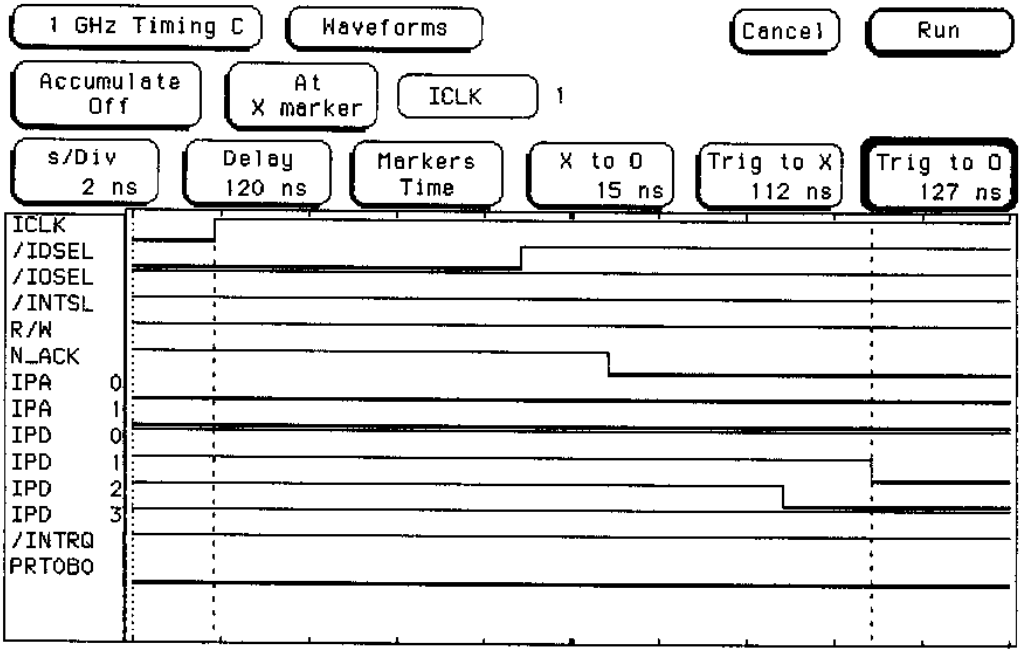


Figure 4-3 Zoomed-in Version of DID48 ID Cycle Driving N_ACK and IPD0-3

4.2.2 I/O Read Cycle

Figure 4-4 is a complete DID48 I/O read cycle. The signals of interest are /IOSEL, N_ACK, and the four IPD0-3 signals.

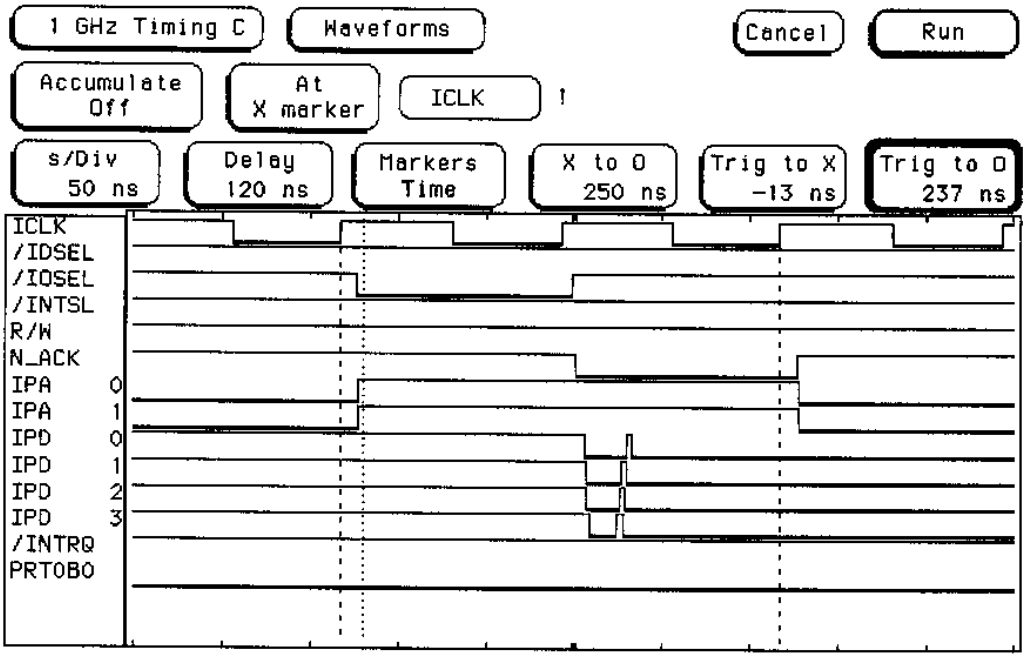


Figure 4-4 Complete DID48 I/O Read Cycle

Figure 4-5 is a zoomed-in view of the DID48 IO read cycle. It shows the DID48 driving the N_ACK and IPD0-3 signals in response to the rising edge of ICLK while /IDSEL is asserted. The typical response time is about 15 ns.

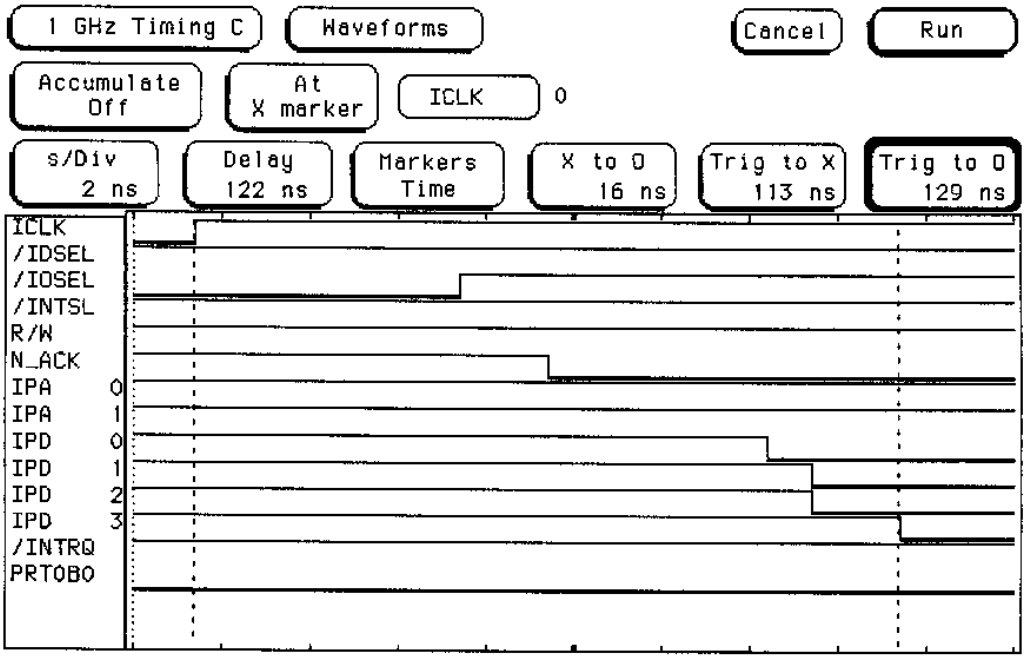


Figure 4-5 Zoomed-in View of DID48 I/O Read Cycle Driving N_ACK and IPD0-3

4.2.3 Interrupt Request With "Debouncing Disabled"

Figure 4-6 shows an Interrupt Request with "Debouncing Disabled" and a few microseconds later an IP Module Interrupt Select Cycle.



NOTE: Figure 4-6 is very important information for users concerned about system response time with debouncing disabled. The Interrupt Request signal is asserted by the DID48 in less than 1 microsecond. This means that the host IP Module carrier board receives the interrupt request signal as fast as possible to begin its interrupt service routine.

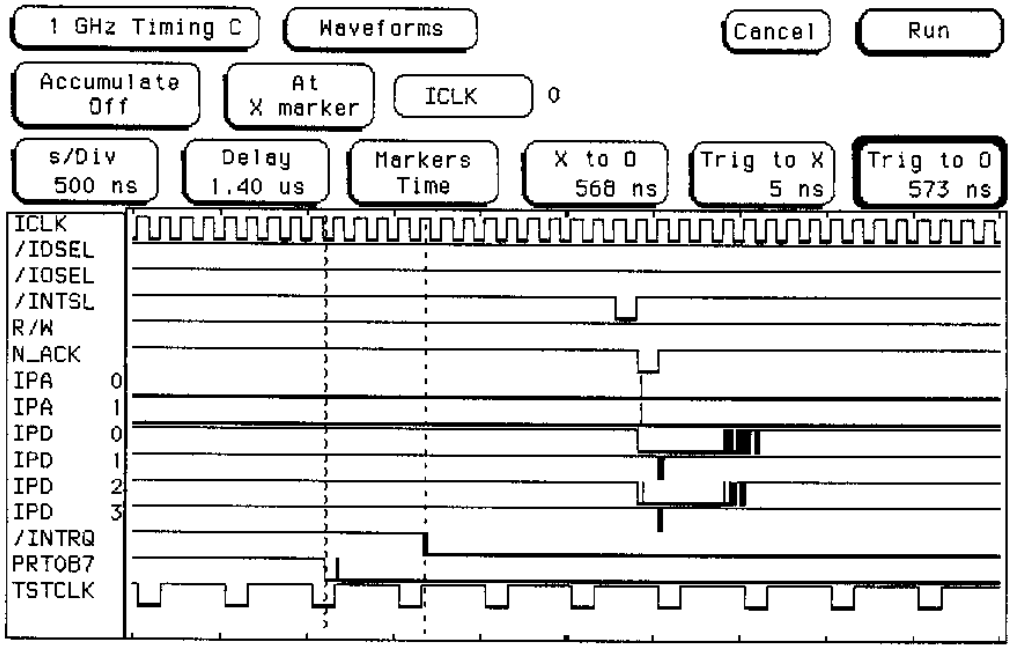


Figure 4-6 DID48 Interrupt Request and Select Cycle (Debounce Disabled)

Figure 4-7 is a view of the DID48's Interrupt Request signal (/INTRQ) being asserted 571 ns after the programmed event "Interrupt on a change of port 0 bit 7 with debouncing disabled", which is the 'PRT0B7' signal label on the waveform diagram.

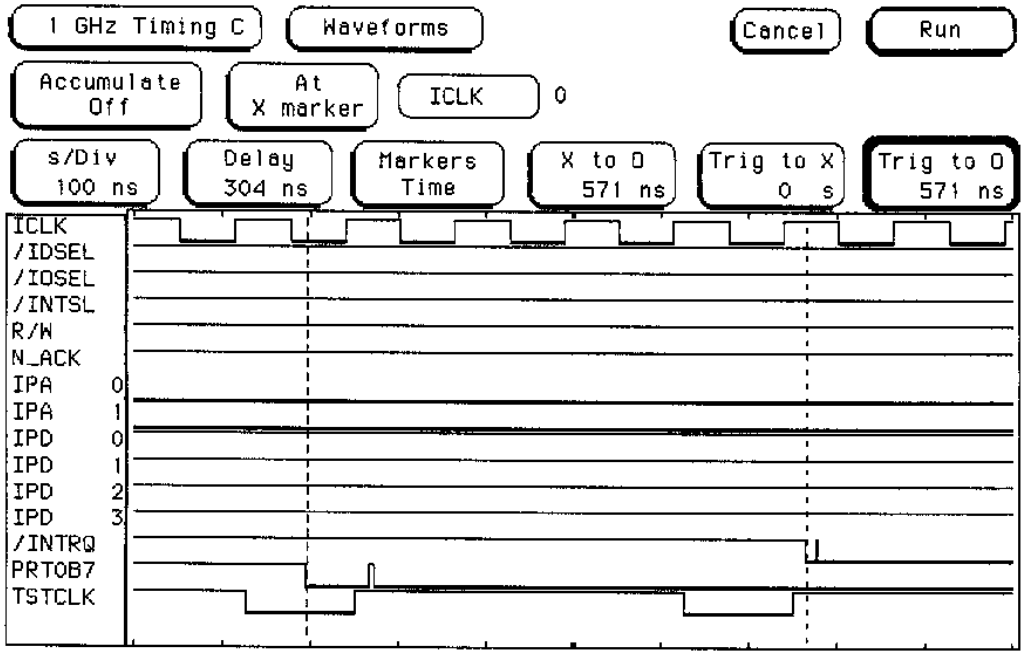


Figure 4-7 DID48 Driving N_INTREQ0 (Debounce Disabled)

4.2.4 Interrupt Request With "Debouncing Enabled"

Figure 4-8 shows an Interrupt Request with "Debouncing Enabled" and a few microseconds later an IP Module Interrupt Select Cycle.

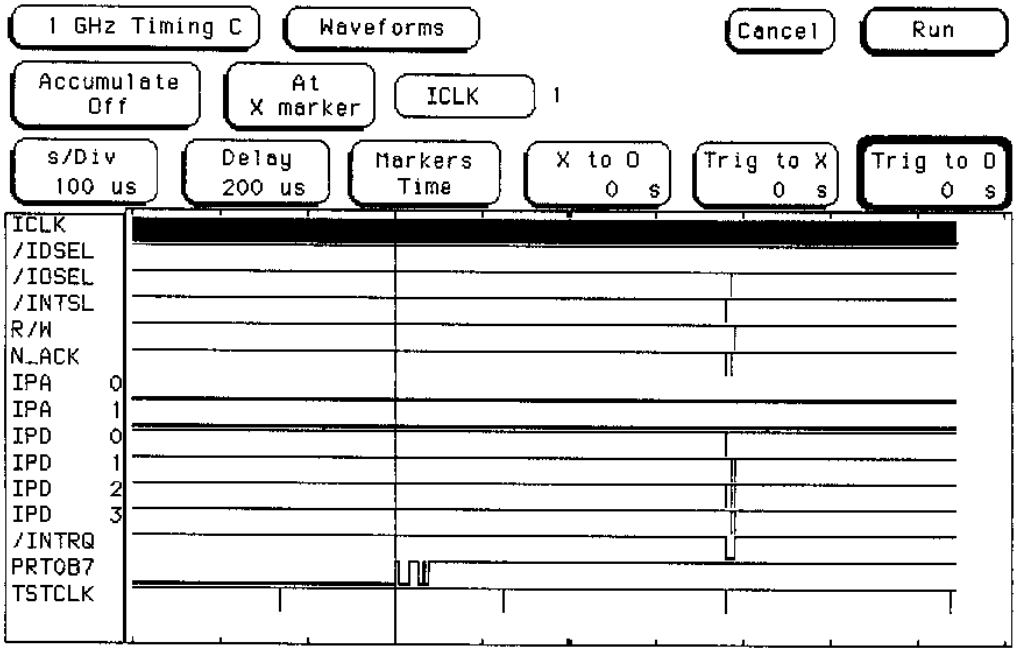


Figure 4-8 DID48 Interrupt Request and Service Routine (Debounce Enabled)

Figure 4-9 is a view of the DID48's Interrupt Request signal (/INTRQ) being asserted a few nanoseconds after the second debounce sample period after the programmed event "Interrupt on a change of port 0 bit 7 with debouncing", which is the 'PRT0B7' signal label on the waveform diagram. This figure also shows N_ACK and IPD0-3.

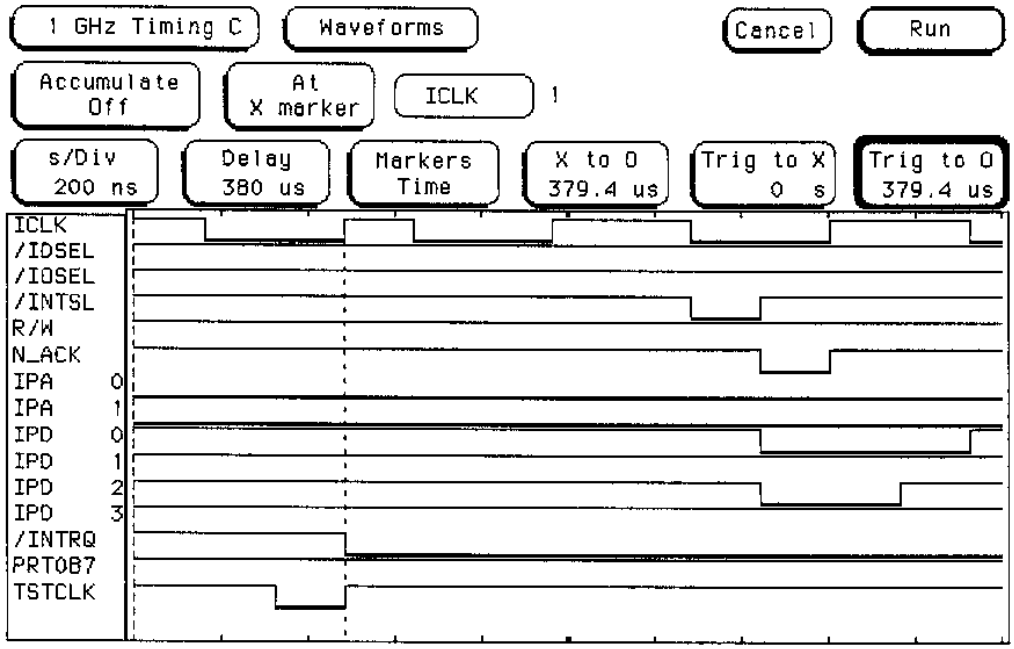


Figure 4-9 DID48 Interrupt Routine and Select Cycle (Debounce Enabled)



NOTE: Figures 5-8 and 5-9 provide very important information concerning system response time with debouncing enabled. With the Interrupt Request signal being asserted by the DID48 a few nanoseconds after the second debounce sample period, the host IP Module carrier board receives the interrupt request signal as fast as possible after the signal is debounced to begin its Interrupt Service Routine. For example, if the debounce sample period is set to 16.384 ms (worst case), it may take as long as just under 32.768 ms to drive the IP Module N_INTREQ0 signal.

APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements	1.800 inches x 3.900 inches x 0.303 inches (above board), 4.572 cm x 9.906 cm x 0.770 cm
Weight	1.076 oz., 30.49 grams
Board thickness	0.062 inches, 0.157 cm, nominally, (4 layers)

PROTOCOL

Clock rate	8 MHz
Wait cycles	None on any transfer types
Hold cycles	Supported on all valid transfer types
Address decoding	Complete (no partial)
I/O transfers	
Writes	8-bit and 16-bit
Reads	16-bit
I/O locations	Seven, 16-bit
Data Ports	3
Control	1
Interrupt control/status	3
Maximum read/write rate	4 MTransfers/second, sustained
ID transfers	8-bit read (only) Zero-fill on upper byte 12 bytes, including CRC
Systran's manufacturer's	ID = 0x45, = E ASCII
DAC128V's model number	0x68, = h ASCII
Cyclic Redundancy Check value	0x89
Maximum read rate	4 MTransfers/second, sustained
Memory transfers	Not supported
Interrupt Vector transfers	8-bit read (only) Zero fill on upper byte
Maximum read rate	4 MTransfers/second, sustained
Interrupt requests	
IP Module signal INTREQ0 is driven on programmed event	
IP Module signal INTREQ1 is not used	
DMA activity	Not supported
Acknowledgment on unsupported transfer attempts	None generated
Memory read and write	
ID write, and addresses beyond those needed for valid transfers	

POWER REQUIREMENTS

Power:	+5 Vdc @ 310 mA (typical no load)

PERFORMANCE CHARACTERISTICS

Electrical Characteristics: Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

Supply voltage with respect to ground:
Minimum.....-0.5 V min. and +7.0 V max.
I/O port signals' voltage .....-32.3 V min. and +32.3 V max. (100% duty cycle)

RECOMMENDED OPERATING CONDITIONS:

Supply voltage .....+4.75 V to +5.25 V
I/O port signals' specifications:
Input voltage range .....-32 V to +32 V
Input rise/fall times .....No limit as long as the input signal is continually rising or falling through the logic transition area (0 – 5 V) with less than 200 mV of hysterisis.
Logic Interface.....ANSI/VITA 4-1995 Specification Compliant Carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): .....0°C to +70°C
Temperature (no bias, storage):.....-40°C to +85°C
Humidity (Non-condensing): .....5% to 95%
Vibration (Operating): .....10 G's RMS, 20 to 2000 Hz, random
Shock (Operating): .....50 G's maximum
Altitude (Operating):.....10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MTBF.....417,982 hours per MIL-HDBK-217F

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

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FIGURES

Figure B-1 Switched Signals Monitor..... B-2
Figure B-2 Relays and Positive Discrete Voltages..... B-3
Figure B-3 Relays and Negative Discrete Voltages..... B-4

B.1 Overview

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the DID48 IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 A Short Glossary of DID48 Applications

The following typical applications were developed using one or more channels on the DID48 IP Module.

- Switched signals monitor
- Relays and positive discrete voltages
- Relays and negative discrete voltages

Most common discrete signal monitoring configuration operations may be performed (within limits) by proper connections and software manipulations.

B.2.1 Switched Signals Monitor

Figure B-1 is an application example that provides the user with one of many possible configurations for using the DID48 as a monitor of common single-pole double-throw switches. The common of up to 48 individual switches may be connected directly to each DID48 input. The switches are debounced and interrupts can be enabled in groups of eight (per 8-bit input port). In this application the discrete signals being monitored are connected to the normally-open contact of the switches. Switches S1 through S4 have the +2.0 to +32.0 voltage range connected to the normally-open contacts, and the -32.0 to GND voltage range connected to the switch common via a resistor. Switches S45 through S48 have the -32.0 to GND voltage range connected to the normally-open contacts, and the +2.0 to +32.0 voltage range connected to the switch common via a resistor.

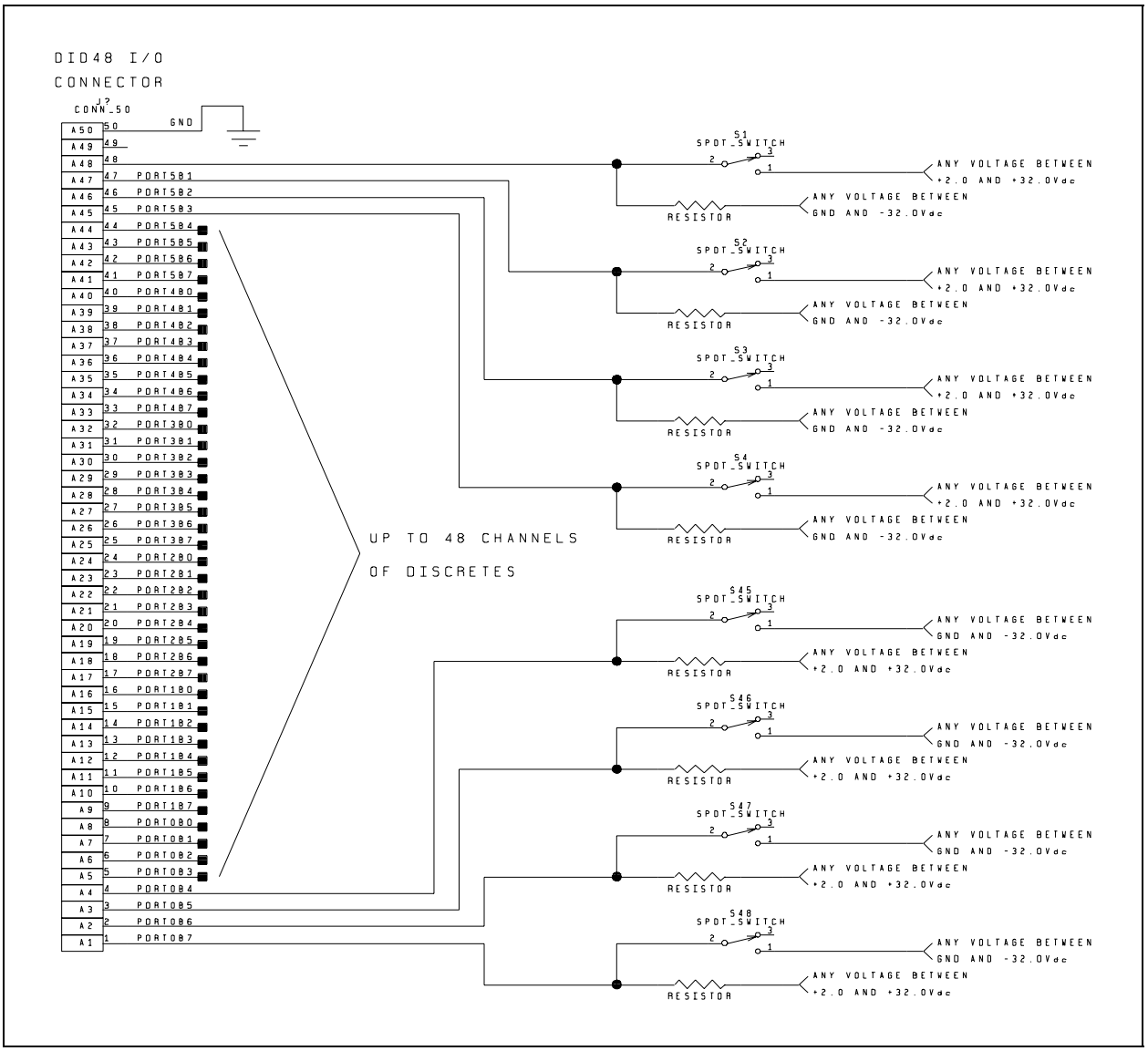


Figure B-1 Switched Signals Monitor

B.2.2 Relays and Positive Discrete Voltages

Figure B-2 is a combination application example of connecting the DID48 to double-pole double-throw relays, and monitoring positive discrete voltages (like +28 Vdc aircraft discretes). The common of up to 48 individual relays can be connected directly to each DID48 input. The relays are debounced and interrupts can be enabled in groups of eight (per 8-bit input port). The discrete signals connected to the normally-open and normally-closed contacts of the relays can be interchanged for make-or-break monitoring.

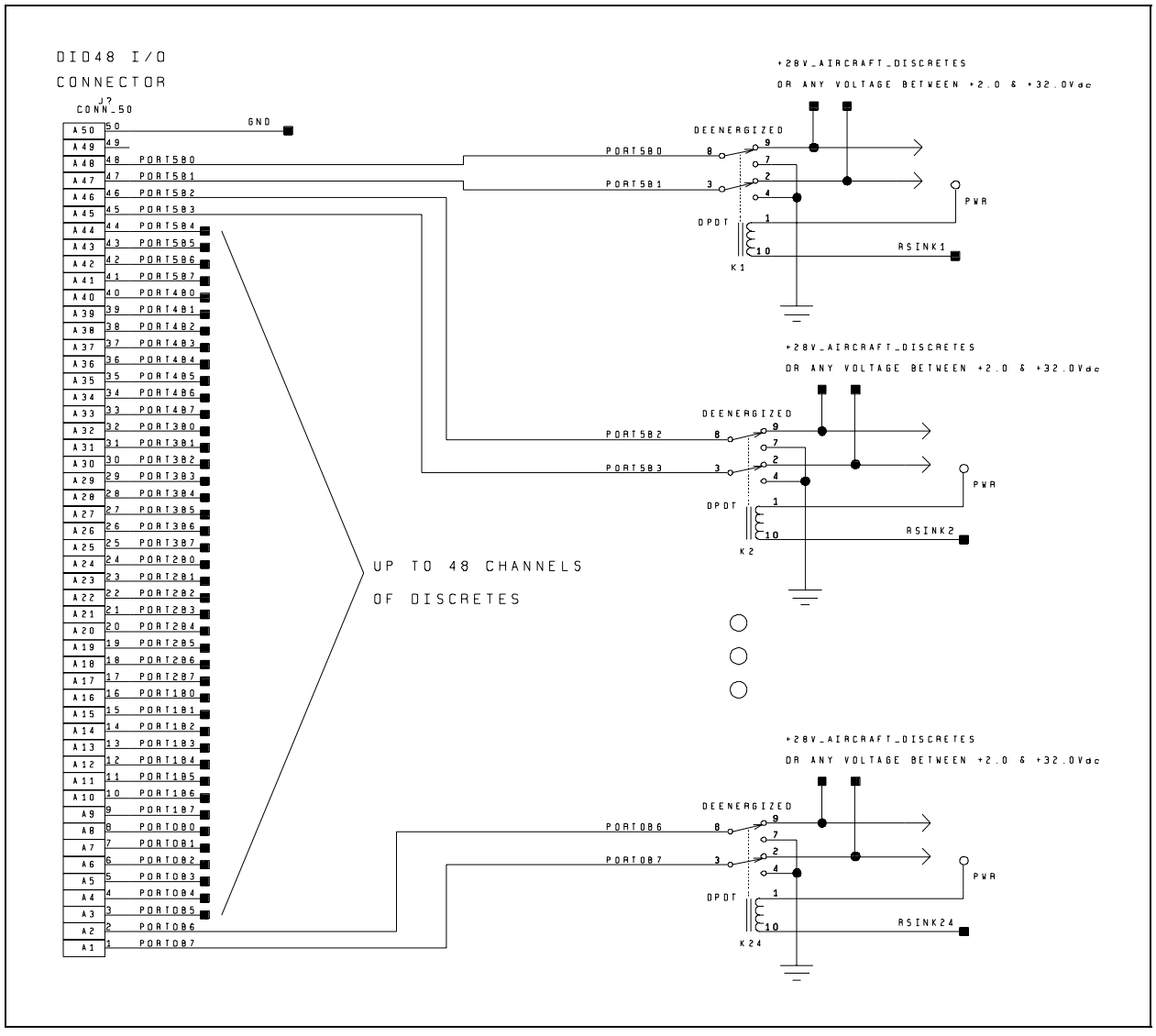


Figure B-2 Relays and Positive Discrete Voltages

B.2.3 Relays and Negative Discrete Voltages

Figure B-3 is a combination application example like Figure B-2 except that the DID48 is connected to double-pole double-throw relays, and uses negative discrete voltages. The common of up to 48 individual relays may be connected directly to each DID48 input. The relays are debounced and interrupts can be enabled in groups of eight (per 8-bit input port). The discrete signals connected to the normally-open and normally-closed contacts of the relays can be interchanged for make-or-break monitoring.

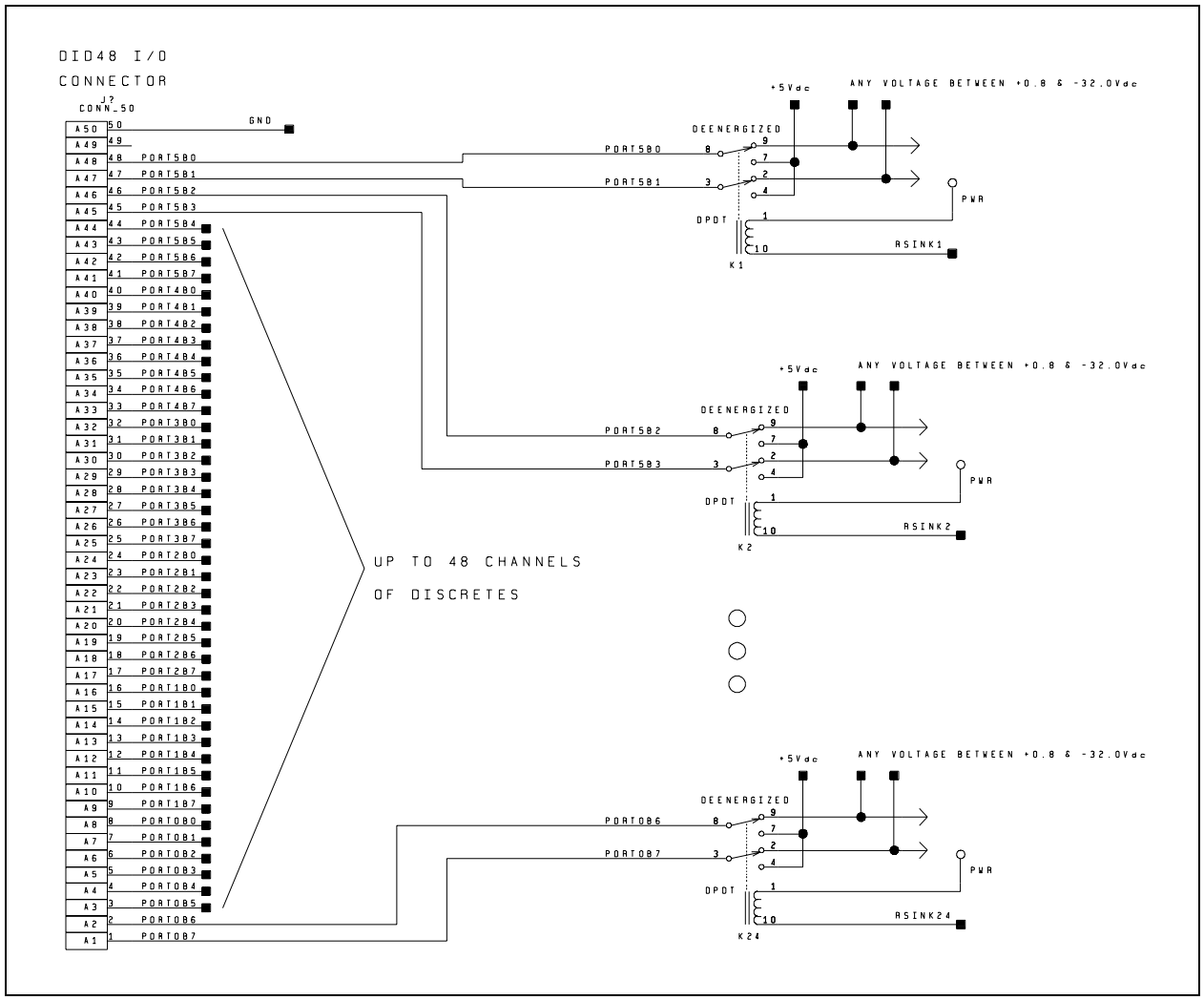


Figure B-3 Relays and Negative Discrete Voltages

APPENDIX C

PROGRAMMING GUIDE

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C.1 Overview

This section of the manual describes the operation of the DID48 from the software perspective, detailing the DID48 registers and providing programming examples. A more detailed description of the hardware can be found in Section 2, PRODUCT OVERVIEW.

C.2 Description

The DID48 has seven 16-bit registers: three data registers, one general control register, and three interrupt-related registers. The data registers may be viewed as either three 16-bit registers or six 8-bit ports. The general control register allows user selection of hardware debounce enable/disable. The interrupt-related registers allow the enabling/disabling of interrupts, provide status of the interrupt-capable ports, and programming of the interrupt vector. Byte writes to any of these registers are not destructive to adjacent bytes.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by the ID PROM feature. This emulation saves space, lowers costs, improves reliability, and enables this IP Module to provide “no-wait” read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

Table C-1 is the DID48 emulated ID Address Space PROM listing:

Table C-1 ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII “I”	0x49
IPA = 0x01	ASCII “P”	0x50
IPA = 0x02	ASCII “A”	0x41
IPA = 0x03	ASCII “C”	0x43
IPA = 0x04	SYSTRAN’s ID	0x45
IPA = 0x05	DID48’s Model Number	0x68
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0x89

C.4 IP Module I/O Address Map

The DID48's I/O Address Map was designed with efficiently located data and control/status registers in the IP Module I/O space (IPA = 0x00 ⇒ 0x06*)*.



NOTE: The address detector circuitry is fully decoded. Therefore, any attempt to access IPA addresses at and above 0x07 will result in no acknowledgment and its subsequent bus time-out error on the IP Module carrier.

The first location (IPA = 0x00) is the read-only Data Register 0 for the input ports 0 and 1. Port 0 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 1 resides on byte-lane 1 such that accesses occur on IPD[15:8]. A valid access from this location is a 16-bit read of both bytes simultaneously.

The second location (IPA = 0x01) is the read-only Data Register 1 for the input ports 2 and 3. Port 2 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 3 resides on byte-lane 1 such that accesses occur on IPD[15:8]. A valid access from this location is a 16-bit read of both bytes simultaneously.

The third location (IPA = 0x02) is the read-only Data Register 2 for the input ports 4 and 5. Port 4 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 5 resides on byte-lane 1 such that accesses occur on IPD[15:8]. A valid access from this location is a 16-bit read of both bytes simultaneously.

The fourth location (IPA = 0x03) is the write and read-back Control Register 0 for the debounce control register bits. There are two bits used in this register to enable/disable the debounce function on a per-byte-lane basis with bit 1 for byte-lane 1 down to bit 0 for byte-lane 0.

The next three addresses (IPA= 0x04⇒0x06) are the interrupt control/status registers and are located in byte-lane 0.

- Interrupt Register 0 (IR0) is the Interrupt Status Register. It uses bits [5:0] to indicate the status of their respective ports, with bit 5 indicating the status of port 5 down to bit 0 indicating the status of port 0.
- Interrupt Register 1 (IR1) is the Interrupt Enable Register. It uses bits [5:0] to control when interrupts are generated by their respective input ports, with bit 5 indicating the status of port 5 down to bit 0 indicating the status of port 0.
- Interrupt Register 2 (IR2) is the Interrupt Vector Register. It uses bits [7:0] and is placed on the IPD[7:0] data lines during an IP Module interrupt cycle.

Table C-2 is the DID48 I/O Address Map and contains the data ports, control registers and interrupt registers:

Table C-2 I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	Data Port 1	Data Port 0	Data Register 0 = Ports 1&0, 8 bits each
IPA = 0x01	Data Port 3	Data Port 2	Data Register 1 = Ports 3&2, 8 bits each
IPA = 0x02	Data Port 5	Data Port 4	Data Register 2 = Ports 5&4, 8 bits each
IPA = 0x03	[XXXX,XXXX]	[XXXX,XX] [1:0]	Control Register 0, Debounce Enable, 2 bits, 0=Debounce, 1=No Debounce
IPA = 0x04	[XXXX,XXXX]	[XX] [5:0]	Interrupt Register 0, Interrupt Status Register, 6 bits, 0=No Interrupt, 1=On Change bit set for that port
IPA = 0x05	[XXXX,XXXX]	[XX] [5:0]	Interrupt Register 1, Interrupt Enable Register, 6 bits, 0=Disabled, 1=Enabled
IPA = 0x06	[XXXX,XXXX]	[7:0]	Interrupt Register 2, Interrupt Vector Register, 8 bits

NOTE: [X] means not used and is read as zero

On power-up, all forty-eight (48) data bits defined above are set to the state of the input pins.

C.5 Word Access Address Translation

Table C-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, the BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VME Bus Address	ISA Bus Address	NuBus Address	IP Module Address
BASE + 0x0	BASE + 0x0	BASE + 0x2	IPA = 0x00
BASE + 0x2	BASE + 0x2	BASE + 0x6	IPA = 0x01
BASE + 0x4	BASE + 0x4	BASE + 0xA	IPA = 0x02
BASE + 0x6	BASE + 0x6	BASE + 0xE	IPA = 0x03
BASE + 0x8	BASE + 0x8	BASE + 0x12	IPA = 0x04
BASE + 0xA	BASE + 0xA	BASE + 0x16	IPA = 0x05
BASE + 0xC	BASE + 0xC	BASE + 0x1A	IPA = 0x06
BASE + 0xE	BASE + 0xE	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B

C.6 Byte Access Address Translation

Table C-4 shows the relationship between VME, ISA, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, the BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VME bus Address	ISA Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 0x1	BASE + 0x0	BASE + 0x3	IPA = 0x00	0
BASE + 0x0	BASE + 0x1	BASE + 0x2	IPA = 0x00	1
BASE + 0x3	BASE + 0x2	BASE + 0x7	IPA = 0x01	0
BASE + 0x2	BASE + 0x3	BASE + 0x6	IPA = 0x01	1
BASE + 0x5	BASE + 0x4	BASE + 0xB	IPA = 0x02	0
BASE + 0x4	BASE + 0x5	BASE + 0xA	IPA = 0x02	1
BASE + 0x7	BASE + 0x6	BASE + 0xF	IPA = 0x03	0
BASE + 0x6	BASE + 0x7	BASE + 0xE	IPA = 0x03	1
BASE + 0x9	BASE + 0x8	BASE + 0x13	IPA = 0x04	0
BASE + 0x8	BASE + 0x9	BASE + 0x12	IPA = 0x04	1
BASE + 0xB	BASE + 0xA	BASE + 0x17	IPA = 0x05	0
BASE + 0xA	BASE + 0xB	BASE + 0x16	IPA = 0x05	1
BASE + 0xD	BASE + 0xC	BASE + 0x1B	IPA = 0x06	0
BASE + 0xC	BASE + 0xD	BASE + 0x1A	IPA = 0x06	1
BASE + 0xF	BASE + 0xE	BASE + 0x1F	IPA = 0x07	0
BASE + 0xE	BASE + 0xF	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

* Byte-lane 1 not applicable for ID Space

C.7 Register Definitions

The DID48 has seven 16-bit registers: three data registers, one control register, and three interrupt registers. The data registers may be viewed as either three 16-bit registers (two data ports each) or six 8-bit ports. Byte writes to any of these registers are nondestructive to adjacent bytes. The registers are described in detail in the following sections.

The values in the Read/Write (R/W) row of the register bit description indicate: Read-Only (R), Write-Only (W), or Read/Write (RW).

C.7.1 Data Register 0 Description (IPA = 0x00)

This 16-bit read-only register is the data register consisting of the 8-bit input ports 0 and 1. These two 8-bit ports can also be viewed as a single 16-bit register. Any write to this register is ignored. When read, it returns the state of the input pins. On power-up, all bits are set to the state of the input pins.

Table C-5 Data Register 0 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	Din1B7	Din1B6	Din1B5	Din1B4	Din1B3	Din1B2	Din1B1	Din1B0	Din0B7	Din0B6	Din0B5	Din0B4	Din0B3	Din0B2	Din0B1	Din0B0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.
Din1B7 - Din1B0 : Bits 7 to 0 of the input data for port 1.
Din0B7 - Din0B0 : Bits 7 to 0 of the input data for port 0.

C.7.2 Data Register 1 Description (IPA = 0x01)

This 16-bit read-only register consists of the 8-bit input ports 2 and 3. These two 8-bit ports can also be viewed as a single 16-bit register. Any write to this register is ignored. When read, it returns the state of the input pins. On power-up all bits are set to the state of the input pins.

Table C-6 Data Register 1 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	Din3B7	Din3B6	Din3B5	Din3B4	Din3B3	Din3B2	Din3B1	Din3B0	Din2B7	Din2B6	Din2B5	Din2B4	Din2B3	Din2B2	Din2B1	Din2B0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.
Din3B7 - Din3B0 : Bits 7 to 0 of the input data for port 3.
Din2B7 - Din2B0 : Bits 7 to 0 of the input data for port 2.

C.7.3 Data Register 2 Description (IPA = 0x02)

This 16-bit read only register consists of the 8-bit input ports 4 and 5. These two 8-bit ports can also be viewed as a single 16-bit register. Any write to this register is ignored. When read, it returns the state of the input pins. On power-up all bits are set to the state of the input pins.

Table C-7 Data Register 2 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power Up State	Din5 B7	Din5 B6	Din5 B5	Din5 B4	Din5 B3	Din5 B2	Din5 B1	Din5 B0	Din4 B7	Din4 B6	Din4 B5	Din4 B4	Din4 B3	Din4 B2	Din4 B1	Din4 B0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.
Din5B7 - Din5B0 : Bits 7 to 0 of the input data for port 5.
Din4B7 - Din4B0 : Bits 7 to 0 of the input data for port 4.

C.7.4 CR0 - Debounce Control Register 0 (IPA = 0x03)

This 16-bit read/write register enables/disables the debounce circuitry for the six input ports on a per-byte-lane basis. Bits[1:0] enable/disable debouncing for byte-lanes 1 and 0, respectively.

Table C-8 Debounce Control Register Bit Descriptions

Bit #	Bits 15 to 2	1	0
Bit Name	Not Used Read as 0's	BL1 DBD	BL0 DBD
R/W	Reads 0s / Writes Disregarded	RW	RW
Power-Up State	N/A	0	0

BL1DBD-BL0DBD: Debounce Disable bits [1:0]

Table C-9 Output Enable Control Bit

DBD Value	OUTPUT ENABLE SELECTION PER PORT
0	Debounce Enabled for byte-lane n
1	Debounce Disabled for byte-lane n

C.7.5 IR0 - Interrupt Status Register (IPA = 0x04)

This 16-bit read/write register provides the status for the input ports. A bit is set in this register if there is a state change in the corresponding input port. If a bit is set in this register, it is cleared by writing a '1' to that bit position. Clearing this bit does not affect any other status bits. The status indication is valid whether the interrupt is enabled or disabled for the bit.

Table C-10 Interrupt Status Register Bit Descriptions

Bit #	Bits 15 to 6	5	4	3	2	1	0
Bit Name	Not Used	P5 IS	P4 IS	P3 IS	P2 IS	P1 IS	P0 IS
R/W	Reads 0s / Writes Disregarded	RW	RW	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0	0	0

Table C-11 Interrupt Status Per Bit

IS Value	Interrupt Enable Selection Per Bit
0	Input condition not detected for bit
1	Input condition detected for bit

C.7.6 Interrupt Enable Control Register (IPA = 0x05)

This 16-bit read/write register enable/disables the interrupt for each port. Interrupts can be enabled/disabled on a per-port basis with bit 5 controlling port 5 down to bit 0 for port 0.

Table C-12 Interrupt Enable Control Register Bit Descriptions

Bit #	Bits 15 to 6	5	4	3	2	1	0
Bit Name	Not Used Read as 0's	P5 IE	P4 IE	P3 IE	P2 IE	P1 IE	P0 IE
R/W	Reads 0s / Writes Disregarded	RW	RW	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0	0	0

C.7.7 IR2 - Interrupt Vector Register (IPA = 0x06)

This 16-bit read/write register contains the interrupt vector. Only the lower 8 bits are used. The upper 8 bits are read as zeros. This vector will be presented on the IP Module data bus during an interrupt-request transfer.

Table C-13 Interrupt Vector Register Bit Descriptions

Bit #	Bits 15 to 8	7	6	5	4	3	2	1	0
Bit Name	Not Used Read as 0's	IV B7	IV B6	IV B5	IV B4	IV B3	IV B2	IV B1	IV B0
R/W	Reads 0s / Writes Disregarded	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0	0	0	0	0

IVB7-IVB0: The 8-bit interrupt vector

C.8 Programming Examples

The following examples show how to control and operate the DID48. The two examples demonstrate how to:

- Enable and disable hardware debouncing.
- How to use the interrupts.

C.8.1 Debounce Enable Example

This example illustrates debounce enable and disable control for the DID48. Only port 0 is used in this example; however, ports 2 and 4 are simultaneously enabled/disabled with port 0 because they are all in byte-lane 0.

- At power-up, the data registers are all cleared (value of '0x0000').
- At power-up, the Debounce Control Register is cleared (value of '0x0000' which equals debounce enabled).
- At this point, the inputs are in the debounce mode, and any change on the input signals will be required to be outside of the jumper-selectable debounce sampling period to see the new input data.
- Read values from data port 0 for debounced input data.
- Write '0x0001' to the CR0 (Debounce Control Register). This disables the debouncing for byte-lane 0.
- Read data value from data port 0 for non-debounced input data.
- Write '0x0000' to the CR0. This enables the debouncing for byte-lane 0 again.

C.8.2 Interrupt Example

This example illustrates how to configure the DID48 for interrupts. Only port 0 is used in this example; however, the programming concept is the same for the other ports.



NOTE: The detection of the selected input condition is independent of whether the interrupt is enabled or disabled. This allows polling of the Interrupt Status Register to determine if the selected input condition was detected. For example, the status register indicates detection of a rising or falling edge within data port 0 regardless of whether the bit 0 interrupt is enabled.



NOTE: This example assumes a suitable ISR (Interrupt Service Routine) exists. An example ISR is shown on page C-12.

- Write a '0x0000' to the Interrupt Enable Register. This disables all interrupts.
- At this point, the input condition required to set the status bit (and generate an interrupt if the interrupt is enabled) is a change (rising or falling edge) on any signal in data port 0.
- Write a '0x0001' to the Interrupt Enable Register. This enables the interrupt for bit 0.
- Applying a rising or falling edge to any bit in data port 0 that will now generate an interrupt.
- Write a '0x0000' to the Interrupt Enable Register. This disables all interrupts.

C.8.3 Interrupt Service Routine Example

If the interrupt capability of the DID48 is used, a suitable ISR must exist. This example describes some steps that the ISR should perform. The host-dependent details are left out since they will vary.

ISR entry point:

- Read the Interrupt Status Register. Test the bits to determine which interrupt(s) has(have) occurred.
- The event (interrupt) usually indicates that some event-driven action is to be taken. If this is the case, take the action associated with the detected interrupt(s). If the action taken must not be interrupted, disable interrupts while taking the action, then re-enable them.
- Remove the condition that caused the interrupt. If this is not practical to do from the ISR, disable the interrupt by clearing the enable bit for the interrupt in the Interrupt Enable Register, and set a flag indicating that some other process should clear the condition. If the condition is cleared outside the ISR, then the clearing process must also re-enable the interrupt.
- Clear the Interrupt Status Register by writing a '1' to the bit(s) that is(are) set in the status register. This can effectively be accomplished by writing back the same value read from the status register.
- Return from exception.

GLOSSARY

[x:y]----------Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit (for example, Data bus [7:0] refers to the least significant eight bits).

byte-lane ----------8 bits of a data bus on octal boundaries.

doublewide ----------An IP Module that is twice the size of the singlewide board.

EPLD----------Erasable Programmable Logic Device.

ID PROM----------The circuitry that presents the proper data patterns to the low 8 bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IP Module----------Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP Module logic bus----------A synchronous, 4 MTransfers/sec, 16-bit bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6 bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

IPDbus ----------IP Module Data Bus.

ISR----------Interrupt Service Routine

MTBF ----------Mean Time Between Failures.

ns, µs, ms ----------Nanoseconds, microseconds, and milliseconds, respectively.

Singlewide----------An IP Module printed circuit board (3.9″ by 1.8″). Each module has two 50-pin connectors.

VHDL ----------Very high-speed integrated circuit Hardware Description Language.

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