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DTI-PC

User Manual

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FOREWORD

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Systran Corporation
4126 Linden Avenue
Dayton, Ohio 45432 USA
(937) 252-5601
Fax: (937) 258-2729

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Chapter 1. Overview

Introduction

The DTI-PC provides a powerful and convenient, interface between a host computer and a MIL-STD-1553 data bus. The DTI-PC enables the host to simultaneously operate in real-time as a MIL-STD-1553 protocol Bus Controller (BC), Multiple Remote Terminal (MRT) and Chronological Monitor (CM). The DTI-PC provides the host with complete access to data received or transmitted on the bus and the ability to detect bus errors.

The DTI-PC utilizes a high-speed controller in conjunction with Dual-Port Random Access Memory (RAM) to provide a complete, intelligent emulation system. Using on-board data structures located in the Dual-Port RAM, the board is capable of sustaining operation on the bus without host intervention. In addition, the CM stores commands, status responses, gap times and time tags within the same buffer.

Single/Dual Channel Configuration

The DTI-PC is offered as a single or dual channel configuration. The dual channel configuration provides all of the functionality of two single DTI-PC boards and twice the amount of onboard dual-port RAM. Each channel contains 64K of dual-port RAM and may be mapped to one area of memory or two different areas of memory.

Modes of Operation

The DTI-PC is capable of operating in BC, MRT and CM modes simultaneously or independently. All MIL-STD-1553 communication between emulated devices occurs over the 1553 bus, rather than through a local bus. The three operating modes provide extensive bus protocol error detection, such as parity error and no response.

Multiple Remote Terminal Mode
Using 32K-words of Dual-Port RAM, the DTI-PC is able to receive, store and count approximately 750 bus messages of 32 data words each. Bus messages are transmitted and received without host intervention. The RT is also capable of generating an interrupt when a message buffer transmits or receives data and enabling specific subaddresses and mode codes.

Bus Controller Mode
The BC provides the capability of defining, storing and executing comprehensive lists of bus instructions. The DTI-PC efficiently addresses up to 32 RTs (31 RTs and one Broadcast RT, RT 31) with a maximum of 32 subaddresses each. The BC can generate and process any valid type of MIL-STD-1553 command:

- BC-to-RT Transfer
- RT-to-BC Transfer
- RT-to-RT Transfer
- Mode Command Without Data Word
- Mode Command With Data Word (Transmit)
- Mode Command With Data Word (Receive)

The BC is also capable of injecting a variety of errors for each transmission on the MIL-STD-1553 bus. These errors are specified as a part of each buslist instruction and may be individually enabled or disabled. You may program an error to be injected once or continuously (each time a message is sent).

Chronological Monitor Mode
The CM captures all or selected traffic while simultaneously acting as one or more RTs. Data transfers may be filtered down to the subaddress level. Mode commands can be selectively monitored down to individual mode codes.

Discrete Output Signal

The DTI-PC is equipped with an RS422 port. This port provides a Discrete Output Signal (DOS) with a resolution of 2 ms, which may be programmed for any buslist instruction. The port also allows for an external elapsed timer (ELT) signal reset.

Memory

Onboard Dual-Port RAM
The DTI-PC Dual-Port Ram allows host access without interfering with operations in progress on the local bus and permits microprocessor access of RAM without imposing overhead on the host bus; thus, the applications program can treat variables and data structures in the Dual-Port RAM the same as variables and data structures residing in the host's main memory. Storing all data in the Dual-Port RAM eliminates continuous data transfers over the host to support MIL-STD-1553 activity.

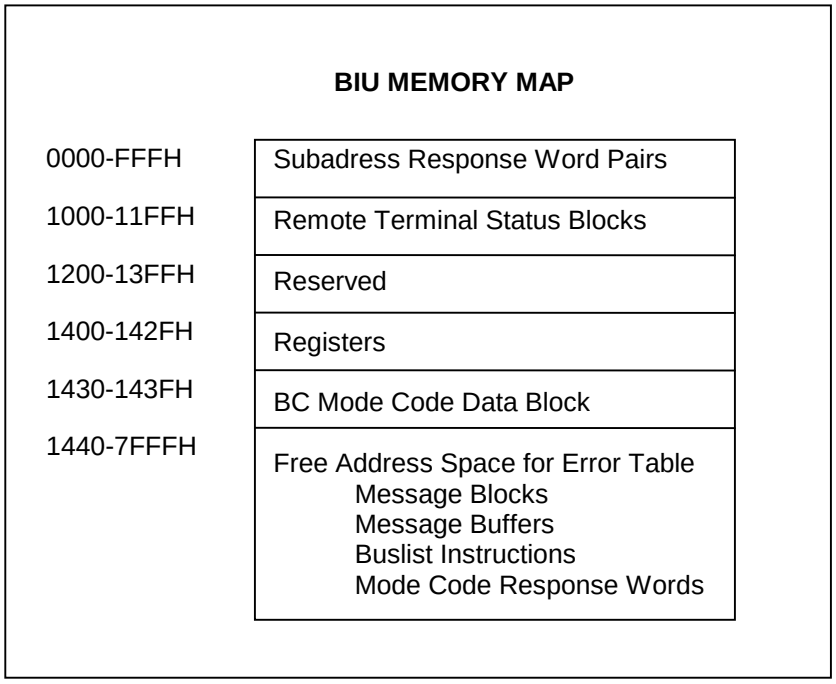


Figure 1-1. DTI-PC Memory Map

Board Configuration
The DTI-PC must be initialized into the MIL-STD-1553 configuration. You may define and load MIL-STD-1553 data for transmission in relation to the 1553 commands and enable RT and subaddress combinations for command responses and/or monitoring. Software executed on the host must set up all the DTI-PC data structures needed to accomplish the desired configuration.

The Dual-Port RAM contains the area required for data structure storage. The RAM is broken down into many different areas, including areas for RT configuration, subaddress configuration, MIL-STD-1553 data transmitting and receiving buffers and CM buffers.

Interrupt Handling

An interrupt notifies the host that a specific condition (such as a Message Transmit interrupt or a BC Halt instruction execution) has occurred. The Interrupt Queue can hold up to 36 interrupt packets.

Because of interrupt latency and host processing speed, multiple interrupts may be generated while the host is processing an interrupt. To preserve the integrity of all enabled events, the DTI-PC continuously buffers interrupt events from within the Interrupt Queue.

Specifications

Table 1-1 provides the specifications for the DTI-PC.

Specifications	
Memory	32K words of Dual-Port RAM
Word Size	16 bits
Communication	MIL-STD-1553 B protocol
Interface to Bus	Transformer or direct coupling
Voltage	+5.0V +5%, +12.0V +5%, -12.0V +5%
Current Drain	3.6 amperes (max.)
Operating Temperature	0 to 55 degrees Celsius
Relative Humidity	10% - 90%, non-condensing
DTI-PC Board Size	332.74 mm x 111.76 mm
Recommended Minimum Specifications	
Host Interface	PC 386
	ESA/ISA Compatibility

Table 1-1. DTI-PC Specifications

Chapter 2. Getting Started

Step 1. Unpacking and Inspecting the Board

Note: The hardware board is shipped in a protective anti-static bag. Do not remove the board from the anti-static package until properly grounded or damage to the board may occur.

Remove the board from the packing box and the protective bag. Place the hardware board on top of the protective bag or on an electrostatically-controlled work surface. If the board appears to be damaged, contact SYSTRAN immediately at (937) 252-5601

Step 2. Setting the Hardware Switches

Two rotary switches, located near the upper middle section of the board, set the I/O Address (Figure 2-1), which defines the Initialization Registers. (See Chapter 7, Registers, for more information.)

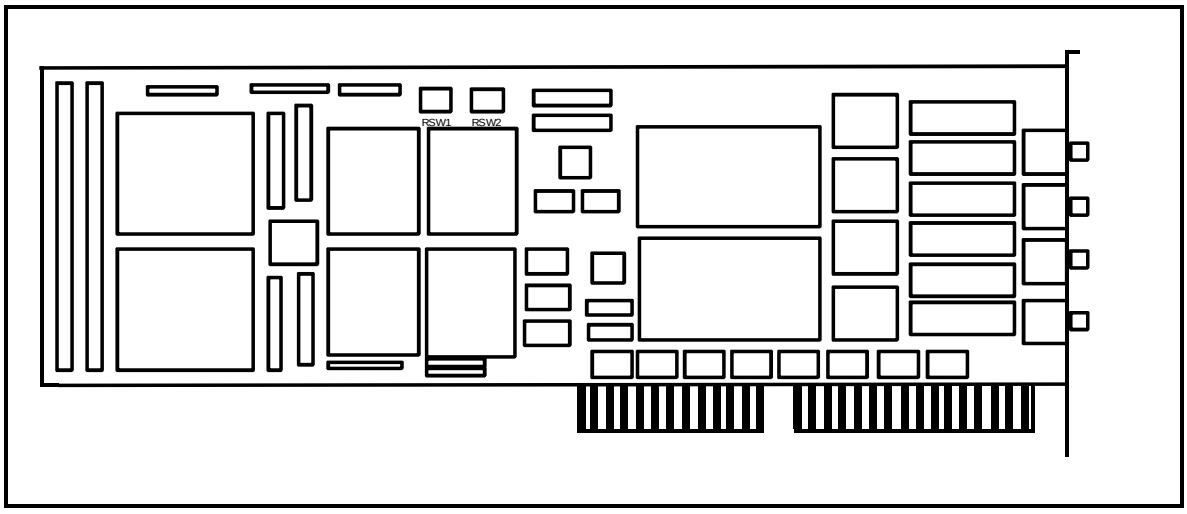


Figure 2-1. DTI-PC Board

Rotary Switches 1 (RSW1) and 2 (RSW2) are factory set at 0100H (Figure 2-2). The DTI-PC I/O Address ranges from 0000H through 07C0H bytes.

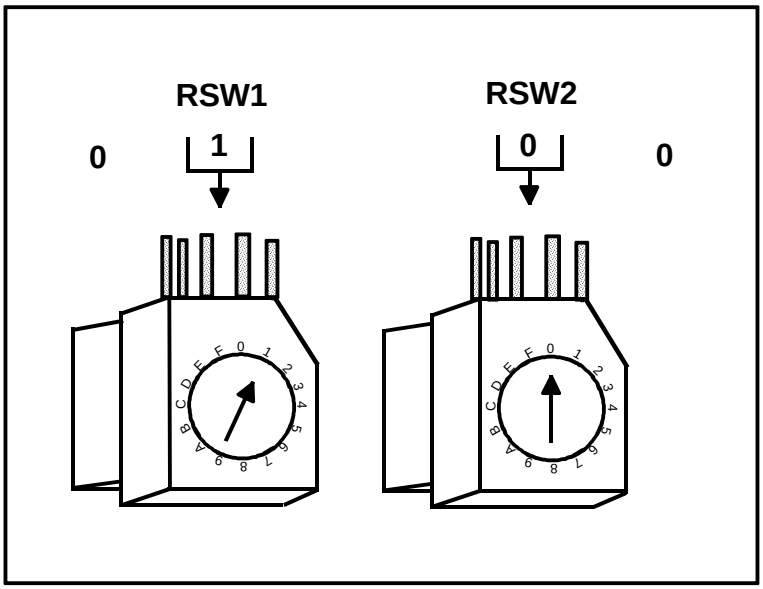


Figure 2-2. I/O Address Rotary Switches 1 and 2

Note: SYSTRAN recommends the user set the Switches 1 and 2 to 300H, 100H or 200H for I/O addressing. The PC-AT has reserved the space 0100-03FF for I/O use.

Step 3. Locating the Fail-safe Timer Jumpers

Leaving Jumpers JP13 and JPB13 open enables the Fail-safe Timer, which allows an interrupt to be generated after 720μs of continuous bus traffic. Installing Jumpers JP13 and JPB13 disables the Fail-safe Timer.

Step 4. Locating the Connectors

The DTI-PC houses four subminiature triax jacks that connect the DTI-PC to the 1553 bus (Figure 2-3). With the board horizontal and the PC connectors facing front, all of the 1553 connectors are located on the right end of the board. Channel 1 is the bottom set of jacks and Channel 2 is the top set. Bus A is the top jack of each set.

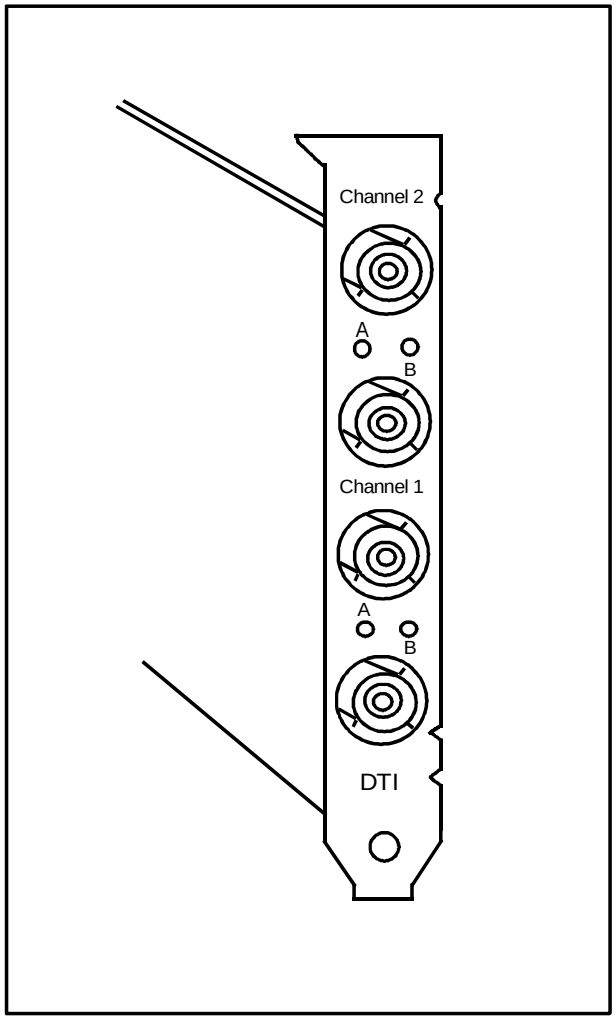


Figure 2-3. Channel 1 and Channel 2 Connector Locations

Step 5. Installing the Board In The Host

Caution: Ensure power is off before installing the DTI-PC.

1. Wear an anti-static wrist strap, position the board over an available slot in the host.
2. Push down firmly on the board until it locks into place.
3. Secure the front panel with a screw.

Step 6. Connecting Direct or Transformer Coupling

The DTI-PC is connected to the MIL-STD-1553 bus via direct or transformer coupling. Use direct coupling if the distance between the DTI-PC and the MIL-STD-1553 bus measures 12 inches or less (Figure 2-4).

Note: The Relay Function Register must be correctly set for direct or transformer coupling and optional internal termination. (See Chapter 7, Registers.)

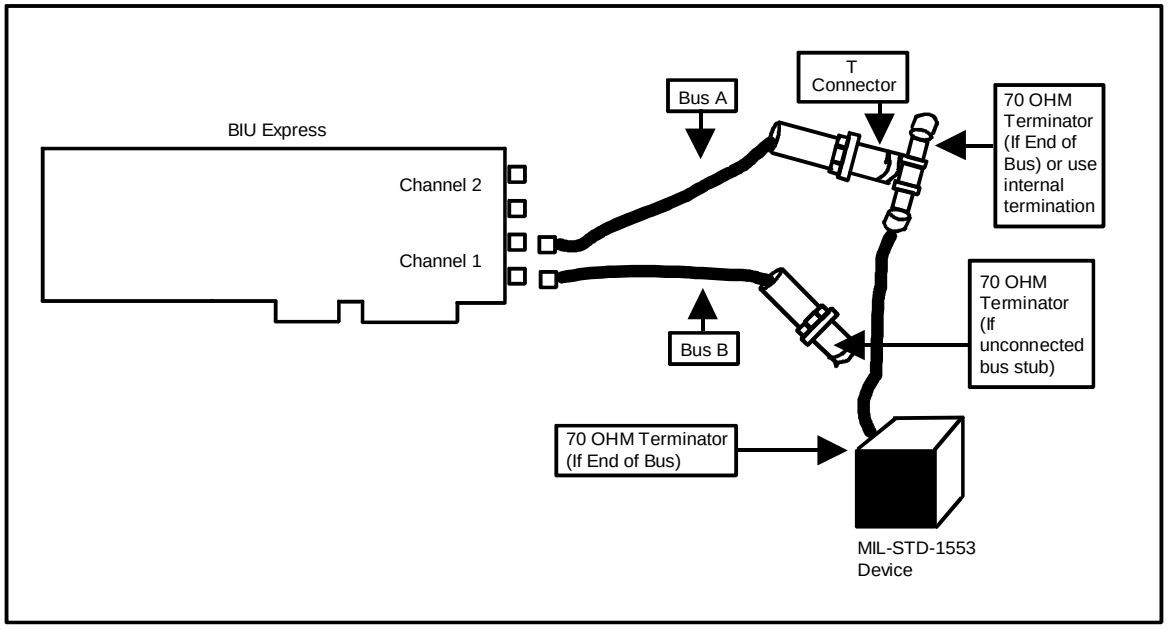


Figure 2-4. Direct Coupled MIL-STD-1553 Bus

Use transformer coupling if the distance between the DTI-PC and the MIL-STD-1553 bus exceeds 12 inches but not 20 feet (Figure 2-5).

Per MIL-STD-1553, if the distance between the board and bus exceeds 20 feet, MIL-STD-1553 cables cannot ensure data integrity. To support greater distance transmission areas, a fiber optic extender may be required. Contact SYSTRAN for more information.

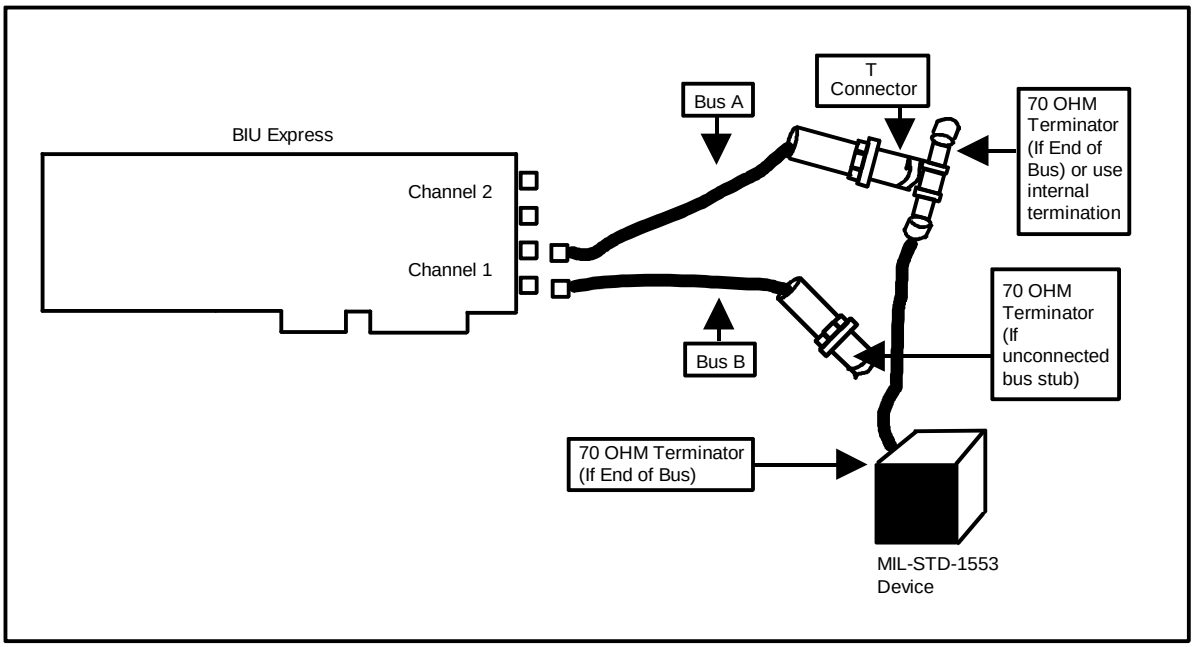


Figure 2-5. Transformer Coupled MIL-STD-1553 Bus

Step 7. Powering On the System

After installing the board and selecting the proper coupling, turn on the system.

For proper board operation you must load a Configuration File into the board using the Upload Utility. Type:

1) dticfg
2) <cfg_file> the name of the data file
3) <io_base> the selected I/O address

For example, if the name of your data file is express.dat and you have selected I/O address 0x100, you would type:

dticfg express.dat 0x100

For a dual channel board, repeat Steps 1-3, adding 10H to the I/O address.

Note: It is recommended that the Configuration File Upload be placed in the AUTOEXEC.BAT file to ensure the board is configured each time the system is powered on.

Uploading the Configuration File run's SYSTRAN's Diagnostics software, which completes the hardware tests.

Step 8. Programming the Board

To program the board, you must first set up the board Configuration Registers. Setting up these registers requires the following steps:

1. Write to the Memory Base Register for the selected channel to select the PC memory page.
2. Write to the Interrupt Level Register for the selected channel to select and enable interrupts.
3. Write to the Control Register for the selected channel to enable memory. (See Chapter 3, Registers, for more information.)

For the DTI-PC to emulate a MIL-STD-1553 device, specific data structures must be created in memory and the BC, MRT and CM modes must be initialized.

To initialize the BC mode, WRITE:

- Buslist instructions
- Message blocks and data buffers for transmitting and receiving MIL-STD-1553 data
- Transmitter data
- BC mode code data
- BC Error Control Register 14H

Start the BC by writing the beginning address of the buslist to the BC Control Register 10H.

To initialize the MRT mode, WRITE:

- Status blocks for each monitored RT
- Subaddress response word pairs for each emulated subaddress
- Data buffers for storing transmitting/receiving MIL-STD-1553 data
- Transmitter data
- Mode code responses

Next, WRITE a start value to the MRT Control Register 11H.

To initialize the CM mode, WRITE:

- Monitor buffers for MIL-STD-1553 message storage
- Subaddress response word pairs for each monitored subaddress
- Data buffers for monitoring MIL-STD-1553 data
- Monitor mode codes

Next, WRITE the address of the first monitor buffer to the Monitor Buffer Pointer Register.

Then, WRITE a start value to the Chronological Monitor Control Register 18.

Bus Controller Data Structures

Bus Controller Instruction
The Bus Controller instructions transmit the MIL-STD-1553 Command Word or control BC execution. You may choose from nine instructions:

- Mode Command
- BC-to-RT Transfer
- RT-to-BC Transfer
- RT-to-RT Transfer
- JUMP
- HALT
- NO-OP
- Reset Stack
- HUE (Halt Until Elapsed Timer expires)

Each BC instruction is made up of four words. Each type of data transfer instruction can inject errors on the command word or one transmitted data word.

Buslist
The Buslist instruction is a sequence of BC instructions that automatically executes after the BC Control Register is written with the address of the first buslist instruction to be executed. Terminate the buslist instruction with a HALT and start the Buslist with a WRITE to the BC Control Register. (See Chapter 7, Registers.)

Bus Controller and Remote Terminal Data Structures

BC Mode Code Data or Data Block Command
This data structure stores single MIL-STD-1553 data words transmitted or received with MIL-STD-1553 mode commands. The address of the words is identified in the mode instruction in the buslist. Sixteen addresses are available for data words transmitted or received during mode commands.

Message Buffer Address Word Pair
This data structure points to the transmit or receive message buffer.

Message Buffer
The Message Buffer data structure stores 1-32 transmitted and received MIL-STD-1553 data words associated with one MIL-STD-1553 message.

Message Block
The Message Block data structure is a list of Message Buffers.

RT Status
The RT Status Block contains 16 words for each RT. This data structure contributes to the creation of the status word by the RT in response to a command word, if the RT is emulated. The RT Status data structure stores single MIL-STD-1553 Data Words for the responses to MIL-STD-1553 mode command words that require the RT to transmit or receive one word.

Remote Terminal and Chronological Monitor Data Structures

SA Response Word Pairs
This data structure identifies the subaddress as a data or mode subaddress. There are two word pairs for each emulated subaddress. If this subaddress is a data subadress, the second word points to a message buffer word pair. One subaddress response word pair each for Receive and Transmit directions. If this subaddress is a data subaddress, the second word points to a message buffer word pair. If the subaddress is a mode subaddress, the second word points to an RT mode code response block.

RT Mode Code Response Word
This data structure specifies the action to take when a mode command is received by the RT. One word exists for each mode code (0-31). This structure also identifies the mode codes to be monitored.

Step 9. Using the RS422 Port Option

The DTI-PC comes equipped with an RS422 port (J4, JB4). The 16-pin port is defined as follows:

Pin	Description
1	ELT RST+ Elapsed Timer Reset
2	ELT RST- Elapsed Timer Reset
3	EXT ELT CLK+ External Elapsed Timer Clock
4	EXT ELT CLK- External Elapsed Timer Clock
5	DOS+ Discrete Output Signal
6	DOS- Discrete Output Signal
7	NC
8	NC
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC

Table 2-1. The RS422 Port Pin Assignments

Note: Do not drive pins designated as having no connection (NC).

Connector J4 is used with Channel 1 and Connector JB4 is used with Channel 2 if the DTI-PC board is equipped with two channels. The orientation of each connector is shown in Figure 2-6.

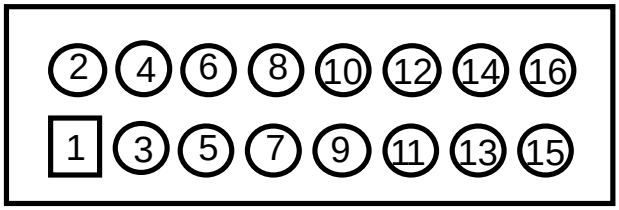


Figure 2-6. Connectors J4 and JB4 Orientation

Chapter 3. Bus Controller Mode of Operation

The DTI-PC can be programmed to operate in the BC mode to emulate all message types defined by MIL-STD-1553. Any series of commands, either valid or invalid, can be sequenced as needed. A sequence of commands that the BC mode executes is called a buslist. Multiple buslists may be constructed and called up by the host in real-time.

The BC mode operates by executing a series of buslist instructions contained in the Dual-Port RAM. The instructions include those allowing generation of all MIL-STD-1553 message types, as well as No-Op, HALT and JUMP instructions for framing of messages.

BC Features

Elapsed Timer Reset
The BC is capable of resetting the on-board elapsed timer, which helps keep track of the time that elapses between messages. The elapsed timer is enabled by setting Bit 14 of the ELT Control Register. The BC resets the timer via Bit 1 of Word Zero of each buslist instruction. If the Discrete Out Signal Bit and the Elapsed Timer Reset Bit are both set for a buslist instruction, the DTI-PC generates a Discrete Out Signal prior to the Elapsed Timer reset.

Interrupts
In BC mode, hardware interrupts may be posted to the host when certain event interrupts occur. (See the Interrupt section for details.) All interrupts may be selectively enabled or disabled under control of the applications software, unless the BC has halted.

- The No-Op instruction can be used to replace an instruction removed from the buslist without restructuring the entire list. The No-Op instruction may also be used to provide space in which to add an instruction to a buslist at a later time. The No-Op instruction also provides an option that posts an interrupt to the host before proceeding to the next instruction. Without an interrupt, the No-Op instruction takes approximately four microseconds to execute.

Error Response
Specific error responses indicate problems in the transmitting or receiving RT. Each BC data transfer command or mode code can be programmed to take a specific action if a protocol error is detected in the response of a transmitting or receiving RT. The available actions include:

- No Retry
- Retry Once on the Same Bus
- Retry Once on the Opposite Bus
- Retry Once on the Same Bus. If unsuccessful, retry once on the opposite bus.

In the action "Retry Once on the Opposite Bus," the instruction may specify that if the retry on the opposite bus is successful, the primary bus should be switched to the opposite bus.

Protocol Errors and Status Exceptions
MIL-STD-1553 Protocol errors are detected when RTs do not respond or respond per MIL-STD-1553. Protocol errors include:

- No Response (the RT does not respond)
- Manchester or parity error occurs in RT transmission
- The RT address field of the RT's status word does not match the RT address field of the command word.

Status exceptions are detected when a bit other than a bit contained in the address field is set in the RTís status word.

Buslist Instructions

Any number of buslists can be defined within the Dual-Port RAM. The DTI-PC executes these lists once the starting address is written to a Control register. In real-time simulation, a buslist is defined for each simulation the BC executes. A Halt instruction terminates the buslist. During simulation, the DTI-PC updates the data in the Dual-Port RAM that the BC transmits or receives, initiates execution of the appropriate buslist and examines data the BC receives during simulation to ensure data conforms to MIL-STD-1553 specifications.

When the emulated BC is commanded to start, it reads instructions from a buslist and executes them sequentially until the BC encounters a Halt or Jump instruction. If the BC is not programmed to continue on errors, it reads and executes instructions until it encounters an error condition.

A buslist instruction block is made up of four 16-bit words. Bits 12-15 of Word Zero of an instruction block identify the instruction type (0-8H).

The Discrete Out Signal (DOS) may be generated by the BC at the beginning of command word transmission. The DOS is enabled or disabled by Bit 0 of Word Zero of each buslist instruction block. The signal is active for two microseconds.

Types of Buslist Instruction Blocks

The following buslist instruction blocks are assigned a hexadecimal number:

0H	No-Op
1H	Jump
2H	Halt
3H	Mode Code
4H	BC-to-RT Transfer
5H	RT-to-BC Transfer
6H	RT-to-RT Transfer
7H	Halt Until ELT
8H	Reset Stack
9-FH	Reserved

Other parameters in a buslist instruction block depend on the block type. Buslist instruction blocks are stored in memory locations from 1440H-7FFFH.

No-Op (Instruction 00H)

The No-Op instruction allows new instructions to be added to a buslist at a later time without altering its length. If the No-Op Interrupt Enable Bit (Bit 11) is ON, the BC posts a No-Op Interrupt before proceeding to the next buslist instruction block. If OFF, the BC proceeds to the next buslist instruction block in approximately four microseconds (Figure 3-1).

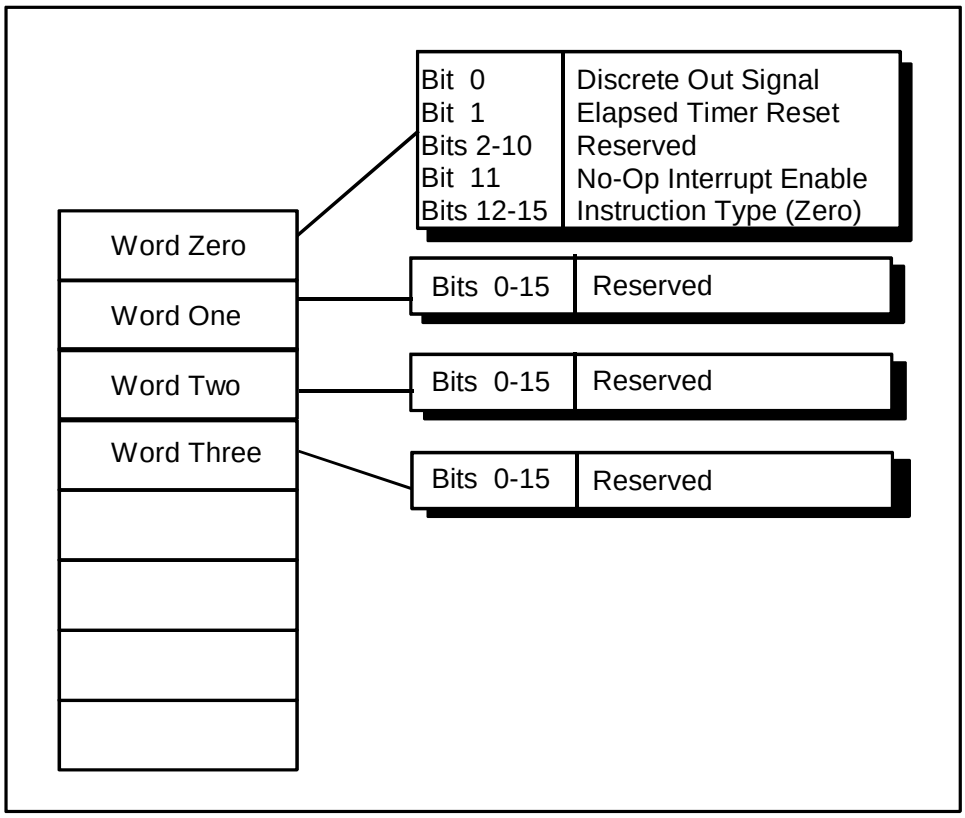


Figure 3-1. No-Op Structure (Instruction 00H)

Word Zero

Bits 15-12	Instruction Type (00H)
Bit 11	No-Op Interrupt Enable
Bits 10-2	Reserved
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Words One, Two and Three

All 16 bits of Words One, Two and Three are reserved.

Jump (Instruction 01H)

The Jump instruction is a branch instruction that can interrupt the sequential execution of buslist instructions (Figure 3-2). Bits 8-11 of Buslist Instruction 01H determine the type of jump instruction (Table 3-1). Three Jump instructions and a Return instruction allow host-independent, RT polling. These Jump instructions include two conditional jump instructions: Status Mask and Protocol Error.

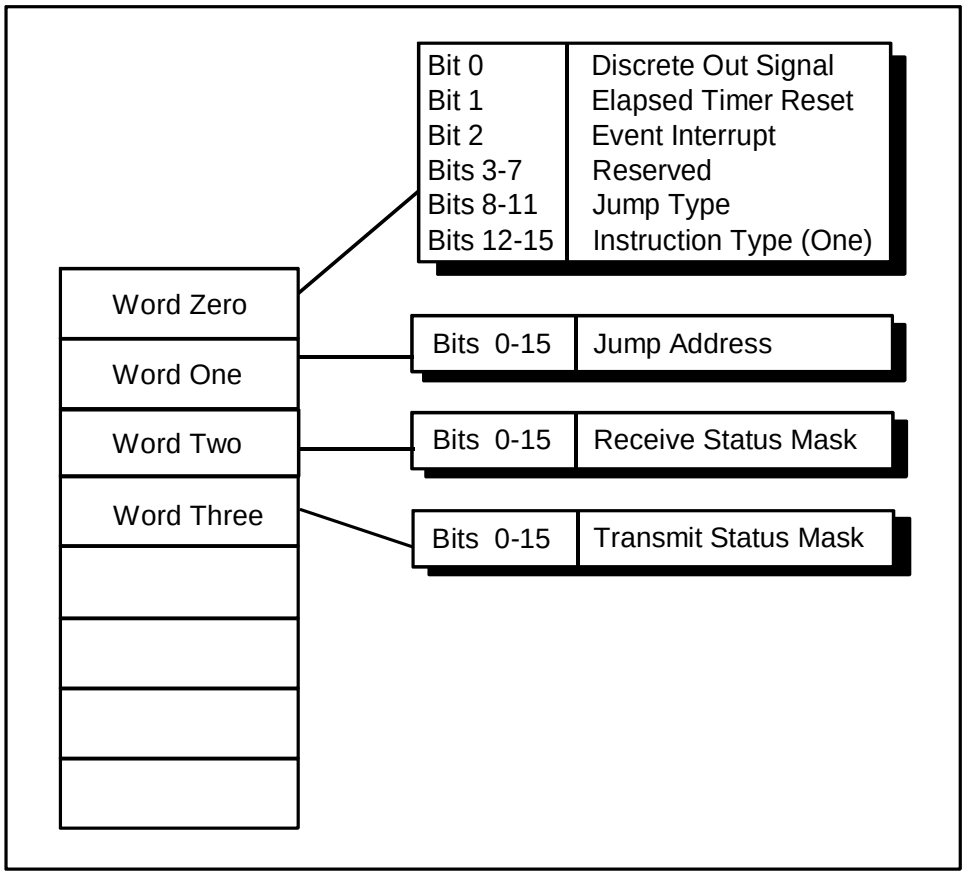


Figure 3-2. Jump (Instruction 01H)

Bits	Jump Types
0000	Jump Always
0001	Conditional Jump to Sublist on Status Mask
0010	Conditional Jump to Sublist on Protocol Error
0011	Return From Sublist
0100	Unconditional Jump Subroutine

Table 3-1. Jump Types (Bits 8-11)

Excluding the Return instruction, the Jump Buslist instruction contains the jump address (Bits 0 through 15 of Word One) that determines the memory address of the next buslist instruction to execute.

The DTI-PC reserved memory contains a stack of four jump addresses. If this jump address stack

overflows, the BC generates a Stack Overflow Interrupt. A software or hardware reset automatically resets the jump address stack pointer. A new address is added to the stack each time a conditional jump is executed.

Jump Always
This branch instruction always causes the buslist instruction block pointer to point to the next desired buslist instruction (as defined in Word One of the buslist instruction block). No entry is added to the jump address stack upon execution of this instruction.

Conditional Jump to Sublist on Status Mask (0001)
This instruction applies when the BC sends a command and the RT returns a status. The user can compare the Transmit or Receive Status Masks (or both in RT-to-RT transfer) to what is received from the buy by setting the bits in the mask that are being compared to the RT status. By ANDing bits in the corresponding Status Mask with bits in the RT Status, the user can determine if a jump occurs. A jump occurs only if a non-zero value is returned after the AND condition. A return to the Buslist after the Jump is completed is achieved by a Return from the Sublist instruction. For Example:

RT Status Response	1400
Status Mask	07FF
Result of AND	0400

Since the result of AND is non-zero, Jump to Sublist occurs.

Conditional Jump to Sublist on Protocol Error
This instruction causes the BC to jump to a sublist of buslist instructions, if a protocol error is detected in the previous MIL-STD-1553 transfer. The following errors result in a conditional jump:

- No Response from an RT. A Broadcast Message is not defined as a No Response.
- Wrong RT Address from Responding RT
- Manchester Error on Status or Data from a Responding RT

A return to the Buslist after the completion of the Jump is achieved by a Return from Sublist instruction.

Return From Sublist
This instruction causes the BC to remove the last address placed on the jump address stack and jump to the buslist instruction that follows the corresponding conditional jump instruction.

Unconditional Jump Subroutine
This instruction places the addresses of the next buslist instruction address (incremented by four) on the internal, four-deep, jump address stack. The instruction then continues executing the buslist at the memory address contained in the current instruction. The Unconditional Jump Subroutine instructions can be nested (Figure 3-3).

Word Zero

Bits 15-12	Instruction Type (01H)
Bits 11-8	Jump Type
	Defines the type of jump that the BC executes.
Bits 7-3	Reserved
Bit 2	Event Interrupt
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Word One
Bits 15-0 Jump Address

The Memory Address of the next buslist instruction to execute.

Word Two
Bits 15-0 Receive Status Mask

The jump to sublist on status mask instruction logically ANDs the Receive status response received from the MIL-STD-1553 bus with the Receive Status Mask. If the result is non-zero the BC executes the next buslist instruction at the location specified by the jump address in Word One. If the result is zero the BC proceeds to the instruction following the Jump.

Word Three
Bits 15-0 Transmit Status Mask

Same as Word Two (except that the status response received from the MIL-STD-1553 bus is a Transmit Status Word).

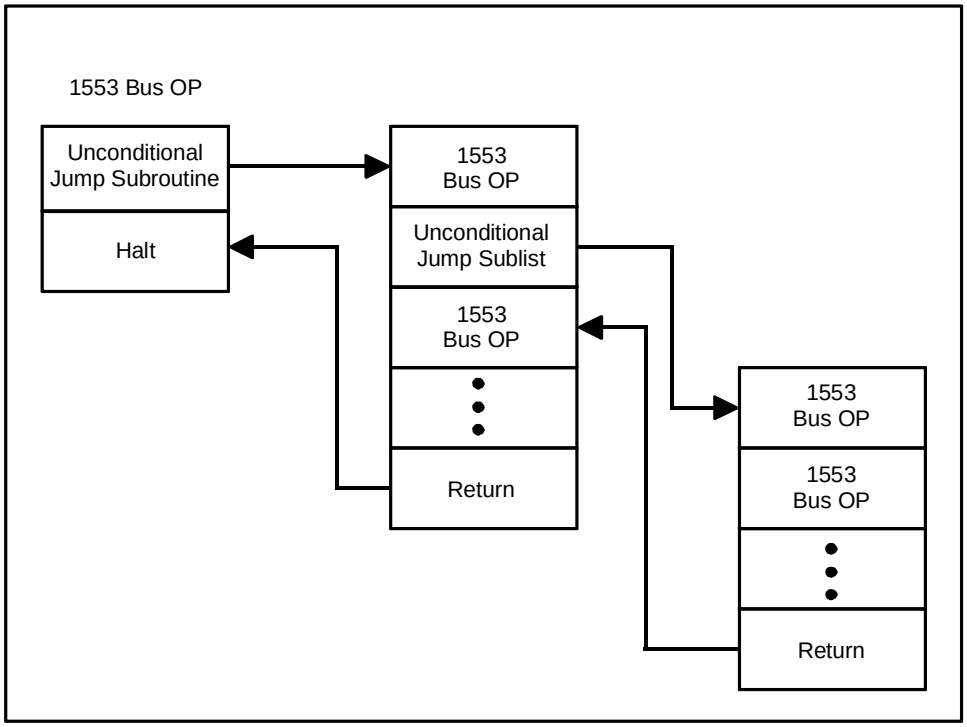


Figure 3-3. Unconditional Jump Subroutine Example

Halt (Instruction 02H)
This instruction terminates a buslist and generates an interrupt.

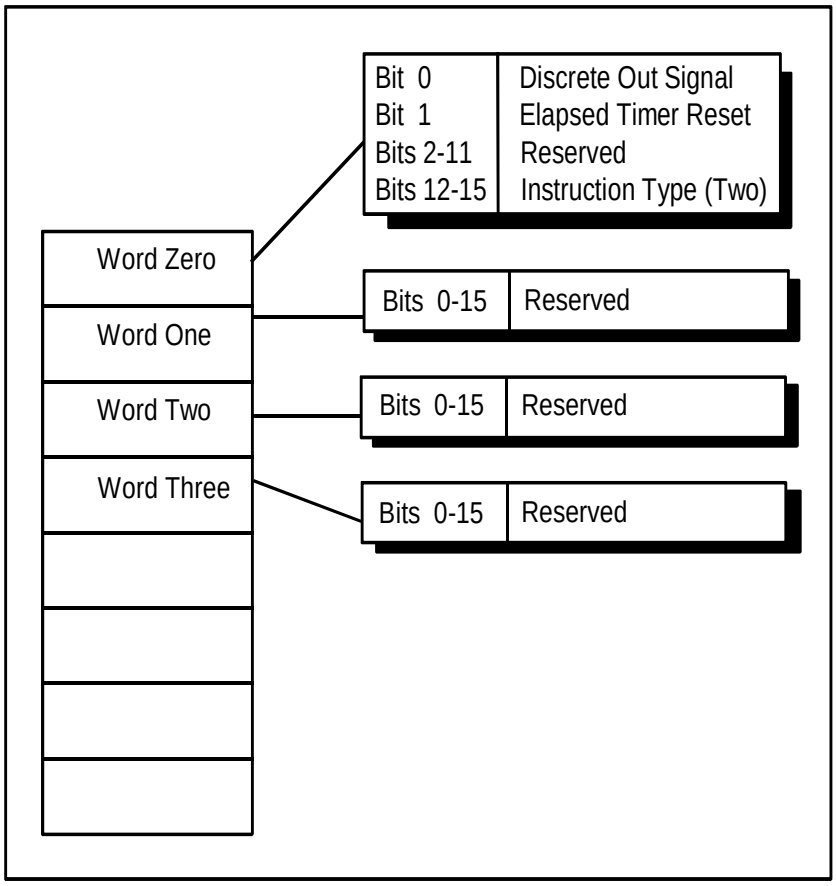


Figure 3-4. Halt (Instruction 02H)

Word Zero

Bits 15-12	Instruction Type (02H)
Bits 11-2	Reserved
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Words One Through Three
All 16 bits on Word One through Three are reserved.

Mode Code (Instruction 03H)
This instruction is composed of the following words (Figure 3-5).

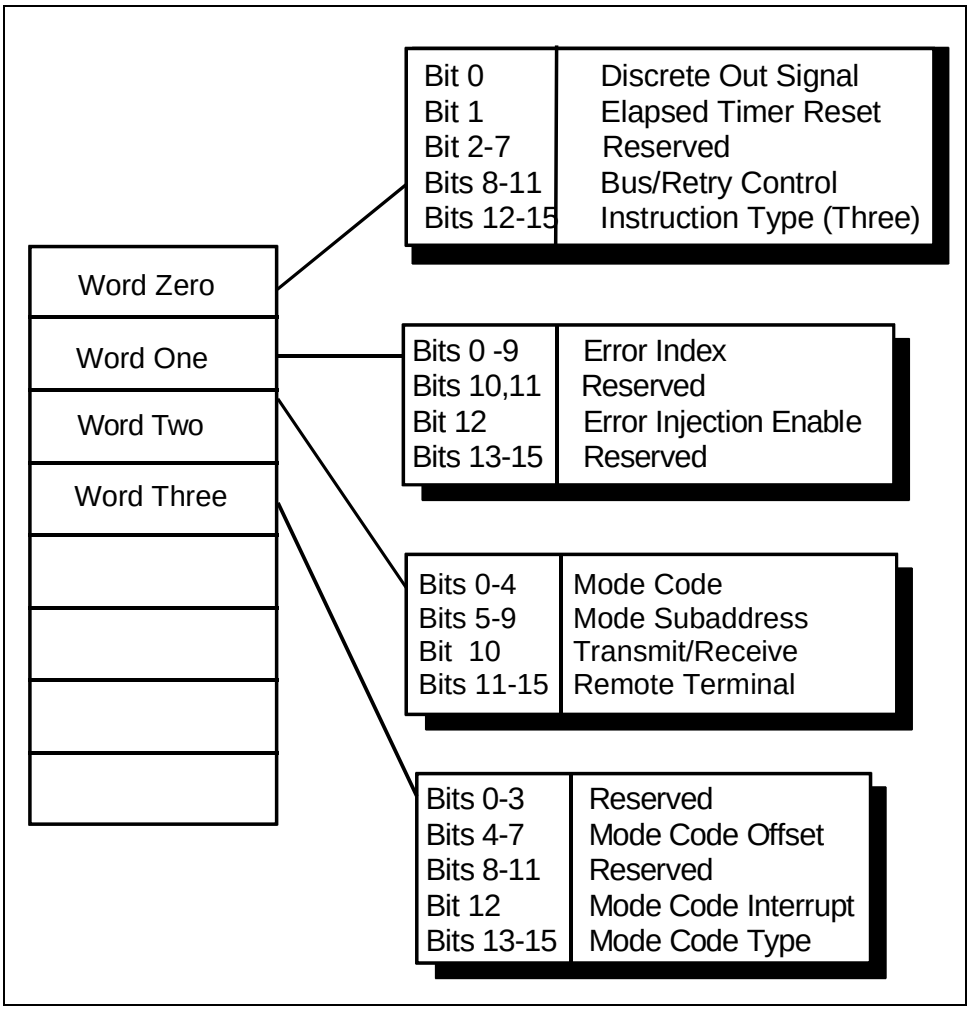


Figure 3-5. Mode Code (Instruction 03H)

Word Zero

Bits 15-12	Instruction Type (03H)
Bits 11	Current Bus
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-2	Reserved
Bit 1	Elapsed Timer Signal
Bit 0	Discrete Out Signal

Note: If Automatic Retry on Opposite Bus (Bit 9) is also set, the DTI-PC retries on the current bus before attempting a retry on the opposite bus.

If your configuration includes error injection, see the BC Error Injection Codes.

Word One

Bits 15-13	Reserved
Bit 12	Error Injection Enabled If set, the DTI-PC injects the error pointed to by the Error Index.
Bits 11 & 10	Reserved
Bits 9-0	Error Index Specifies the error index to be added to the starting address of the Error Table, 1440H.

Word Two

Bits 15-11	Remote Terminal (0-31)
Bit 10	Transmit or Receive
Bits 9-5	Mode Subaddress (0 or 31).
Bits 4-0	Mode Code MIL-STD-1553 Mode Code as hexadecimal value

Word Three

Bits 15-13	Mode Code Type 0=Reserved 1=No Data Word 2=BC Sends Data 3=BC Receives Data 4-7=Reserved
Bit 12	Mode Code Interrupt When set, an interrupt is generated after the buslist instruction is executed.
Bits 11-18	Reserved
Bits 7-4	Offset Into BC Mode Code Data Block. 0-FH Data is transmitted from or received into this location depending on the Mode Code Type. This field is ignored when the mode code Type=1.
Bits 3-0	Reserved

BC-to-RT Transfer (Instruction 04H)
This instruction is composed of the following words (Figure 3-6).

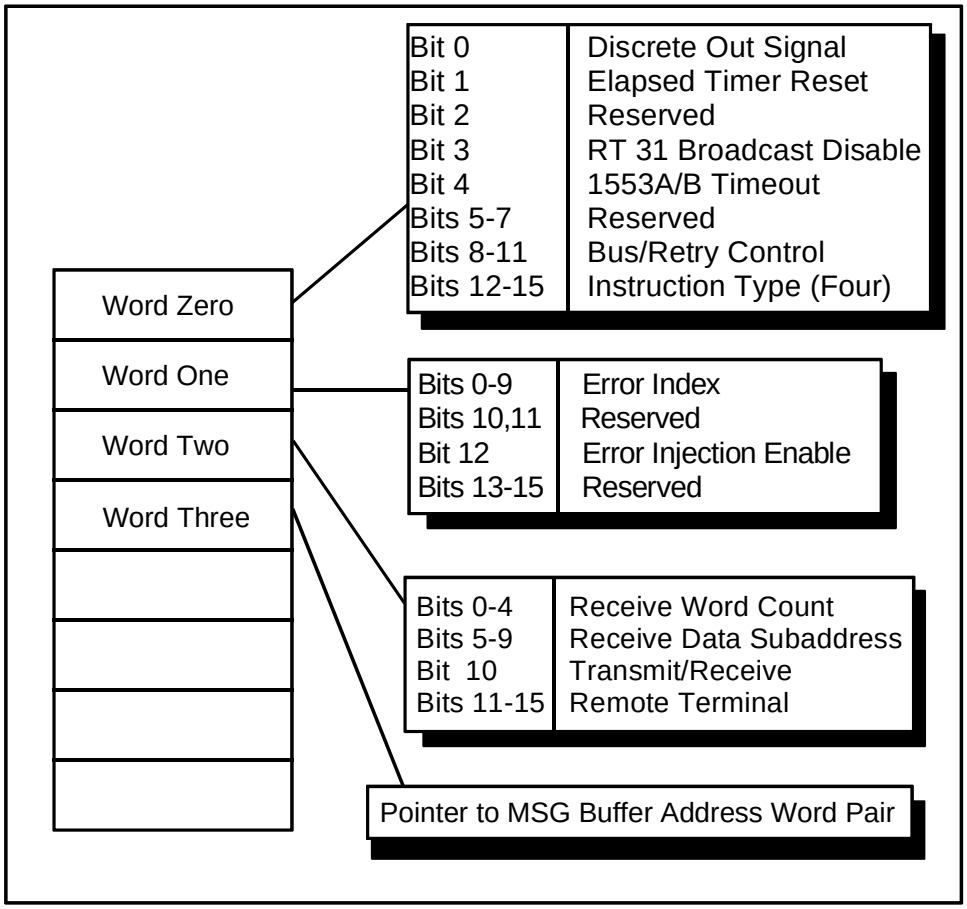


Figure 3-6. BC-to-RT Transfer (Instruction 04H)

Word Zero

Bits 15-12	Instruction Type (04H)
Bit 11	Current Bus
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-3	Reserved
Bit 2	Event Interrupt
	If ON, the DTI-PC posts an interrupt when the command block is executed and processed, before proceeding to the next buslist instruction.
Bit 1	Elapsed Timer Reset
	If ON, the DTI-PC resets the onboard ELT to 0 prior to executing this command block.
Bit 0	Discrete Out Signal
	If ON, the DTI-PC generates a signal to the RS-422 connector prior to executing this command block. The length of this signal is two microseconds.

If your configuration includes error injection, see the Error Codes.

Word One

Bits 15-13	Reserved
Bit 12	Error Injection Enabled
	If set, the DTI-PC injects the error the Error Index points to.
Bits 11 & 10	Reserved
Bits 9-0	Error Index
	Specifies the error index to be added to the starting address of the Error Table, 1440H.

Word Two

Bits 15-11	Receive Remote Terminal
Bit 10	1=Transmit
	0=Receive
Bits 9-5	Receive Data Subaddress
Bits 4-0	Receive Word Count
	The quantity of data words to be received by the RT.
	1H - 1FH = 1 - 31 decimal words
	0H = 32 decimal words

Word Three Pointer to the message Buffer Address Word Pair (Figure 3-6).

Bits 15-0	The message block contains the pointers where the host stores data being transmitted by the BC (Figure 3-7).

Message Block Structure

The DTI-PC allows for one message block, consisting of two words, the address of the last buffer to receive data and the address of the last buffer to transmit data, in free memory, followed by the buffers (Figure 3-7).

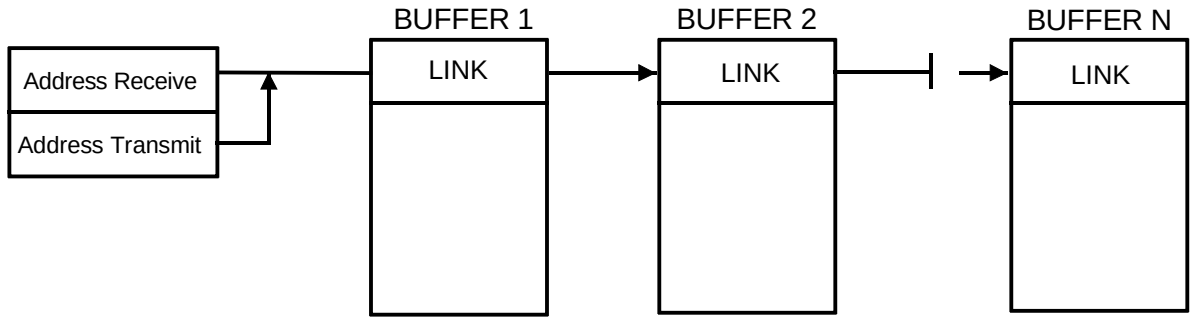


Figure 3-7. DTI-PC SC/DC Message Block

The only words of the 1553 message stored in the buffer are the data words (Figure 3-8). Initially, the software loads both pointers with the address of the last buffer in the message block. The microcode modifies the pointers as the data in the buffers is transmitted and received.

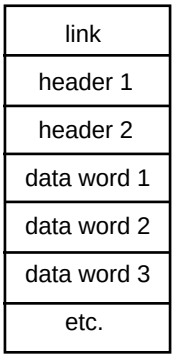


Figure 3-8. Message Buffer

Message Buffer Link Word

The first word of a message buffer is a link word containing the address of the next buffer in the message block. The link word of the last buffer holds the address of the first buffer (Figure 3-9). The software loads the correct value into the link word of each buffer.

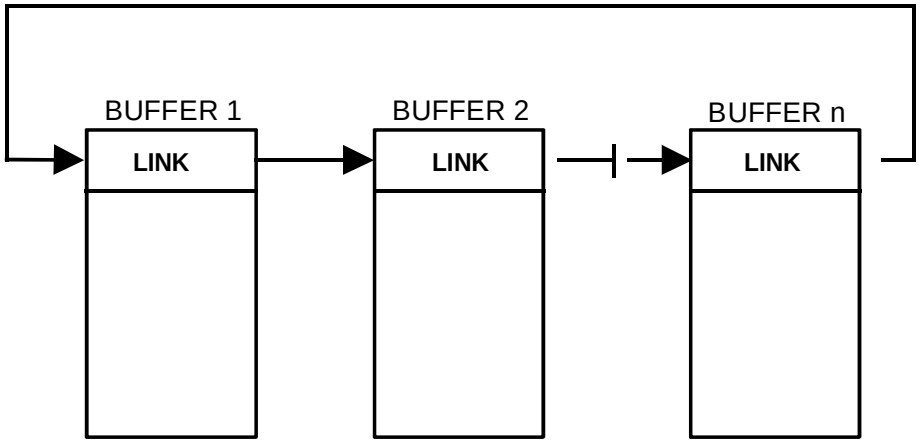


Figure 3-9. Message Buffer Link Words

Header Word 1

The header word contains the buffer word count and the control and status bits. One header word bit indicates if a missed data condition occurs. One header word bit indicates if a missed data condition occurs. The header word also contains a bit that indicates if an overwrite condition occurs. (A message overwrites the previous buffer contents since the new data bit is set in the next buffer and the overwrite current buffer bit is set in this buffer). The software and microcode write to several of the bits (Figure 3-10).

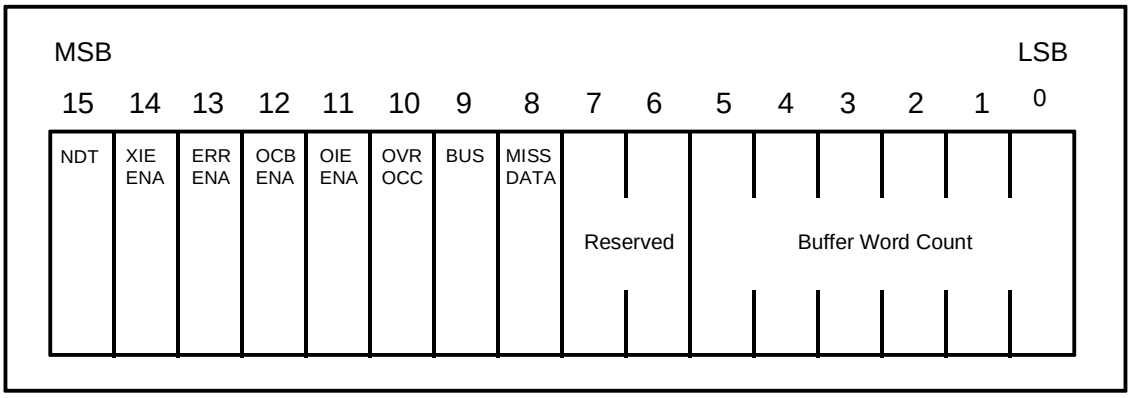


Figure 3-10. Header Word 1

Bit 15 New Data Transmit (NDT)

Set to 1 by software before transmit. Set to 0 by software before receive. Set to 1 by microcode after receive. Set to 0 by microcode after transmit.

Bit 14 Transfer Interrupt Enable (XIE ENA)

Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 13 Error Interrupt Enable (ERR ENA)

Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 12 Overwrite Current Buffer (OCB ENA)

Set to 1 by software to allow overwrite. Set to 0 by software to prevent overwrite. The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. If the new Data Bit is reset in the next buffer, the data words are stored in the next buffer. If the New Data Bit is set in the next buffer and the Overwrite Current Buffer Bit is set in the current buffer, the data is written to the current buffer. Otherwise, the data is not stored in the buffer and the Missed Data Bit is set in the current buffer.

Bit 11 Overwrite Interrupt Enable (OIE ENA)

Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 10 Overwrite Condition Occurred (OVR OCO)

Set to 0 by software initially and set to 1 by microcode when overwrite occurs.

Bit 9 Reserved

Bit 8 Missed Data Condition Occurred (MISS DATA)

Set to 0 by software initially and after it is set by microcode. Set to 1 by microcode when overwrite occurs.

Bits 7-6 Reserved

Bits 5-0 Buffer Word Count (0-3FH)

Header Word 2

The received word count field is stored by the microcode in Header Word 2 and reflects the number of data words stored during a receive message (Figure 3-11). If this same buffer is involved in a transmit message, the received word count field is set to 0 by the microcode. Bits 15-6 are reserved and may be non-zero.

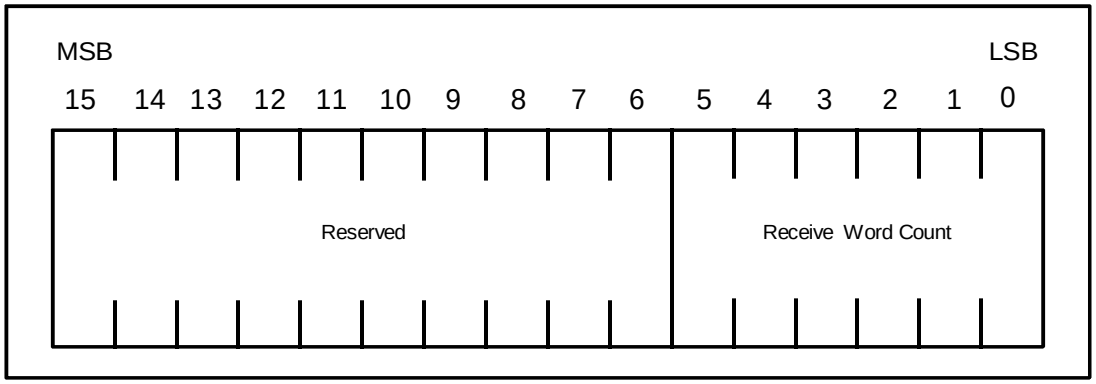


Figure 3-11. Header Word 2

Data Words

The data words transacted in the 1553 message follow Header Word 2.

RT-to-BC Transfer (Instruction 05H)
The structure of this instruction is identical to Instruction Four BC-to-RT Transfer (Figure 3-12).

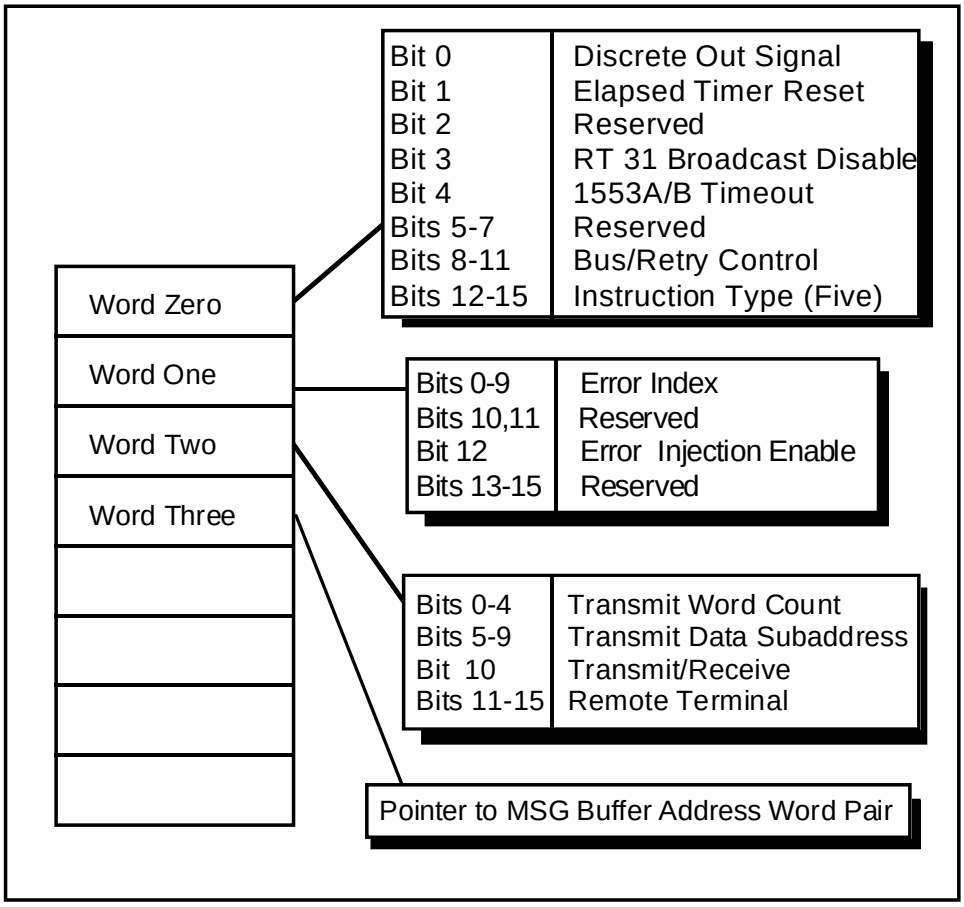


Figure 3-12. RT-To-BC Transfer (Instruction 05H)

Word Zero

Bits 15-12	Instruction Type (05H)
Bit 11	Current Bus
Bits 10	Automatic Retry on Current Bus
Bits 9-0	Automatic Retry on Opposite Bus

If your configuration includes error injection, see the BC Error Injection Codes.

Word Two

Bits 15-11	Transmit Remote Terminal
Bit 10	1 = Transmit 0 = Receive
Bits 9-5	Transmit Data Subaddress
Bits 4-0	Transmit Word Count The quantity of data words to be transmitted by the RT. 1H - 1FH = 1 - 31 decimal words 0H = 32 decimal words

Word Three

Bits 15-0	Pointer to the Message Buffer Address Word Pair

RT-to-RT Transfer (Instruction 06H)
RT-to-RT transfer involves the following words (Figure 3-13).

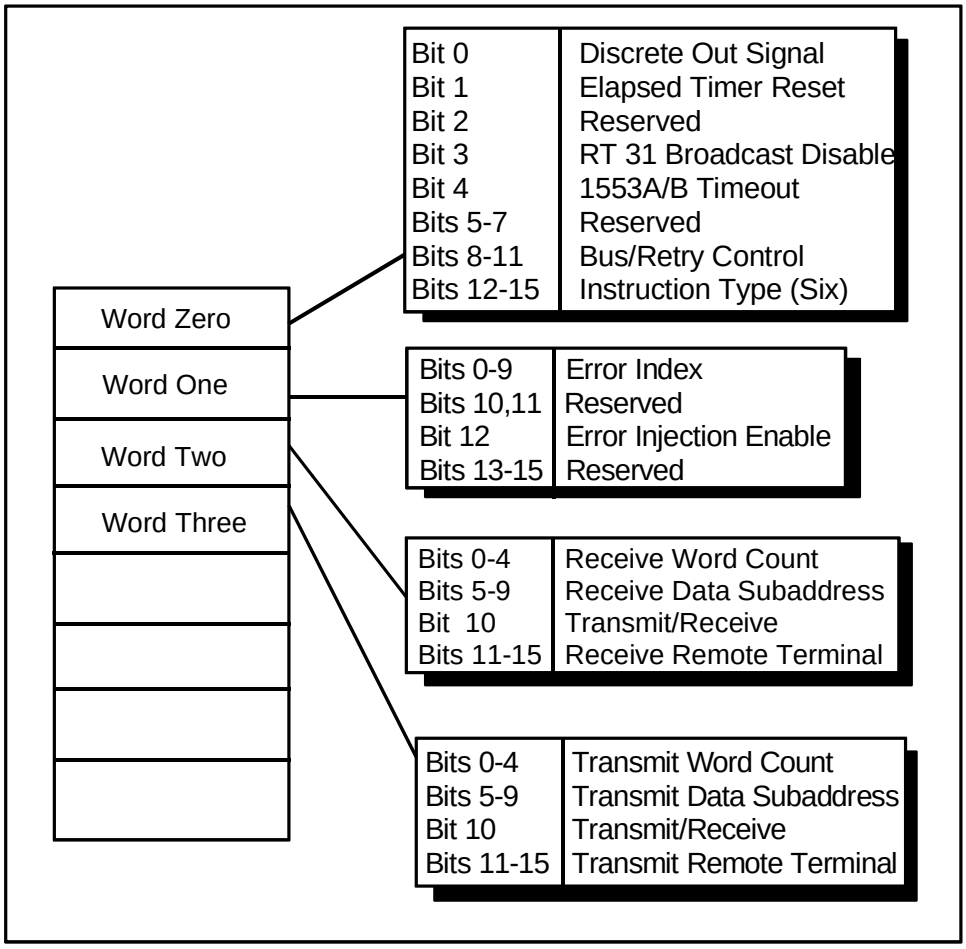


Figure 3-13. RT-to-RT Transfer (Instruction 06H)

Word Zero

Bits 15-12	Instruction Type (06H)
Bit 11	Current Bus
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-3	Reserved
Bit 2	Event Interrupt
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

If your configuration includes error injection, see the Error Codes.

Word One

Bits 15-13	Reserved
Bit 12	Error Injection Enabled If set, the DTI-PC injects the error pointed to by the Error Index.
Bits 11& 10	Reserved
Bits 9-0	Error Index

Specifies the error index to be added to the starting address of the Error Table, 1440H.

Word Two

Bits 15-11	Receive Remote Terminal
Bit 10	1 = Transmit 0 = Receive
Bits 9-5	Receive Data Subaddress
Bits 4-0	Receive Word Count

Word Three

Bits 15-11	Transmit Remote Terminal (0-31)
Bit 10	1 = Transmit 0 = Receive
Bits 9-5	Transmit Data Subaddress
Bits 4-0	Transmit Word Count The quantity of data words to be transmitted by the RT 1H - FH = 1 - 31 decimal words 0H = 32 decimal words

Halt Until ELT (Instruction 07H)
Instruction Seven halts the BC until the ELT equals a value contained within Word Two and Word Three of this instruction (Figure 3-14).

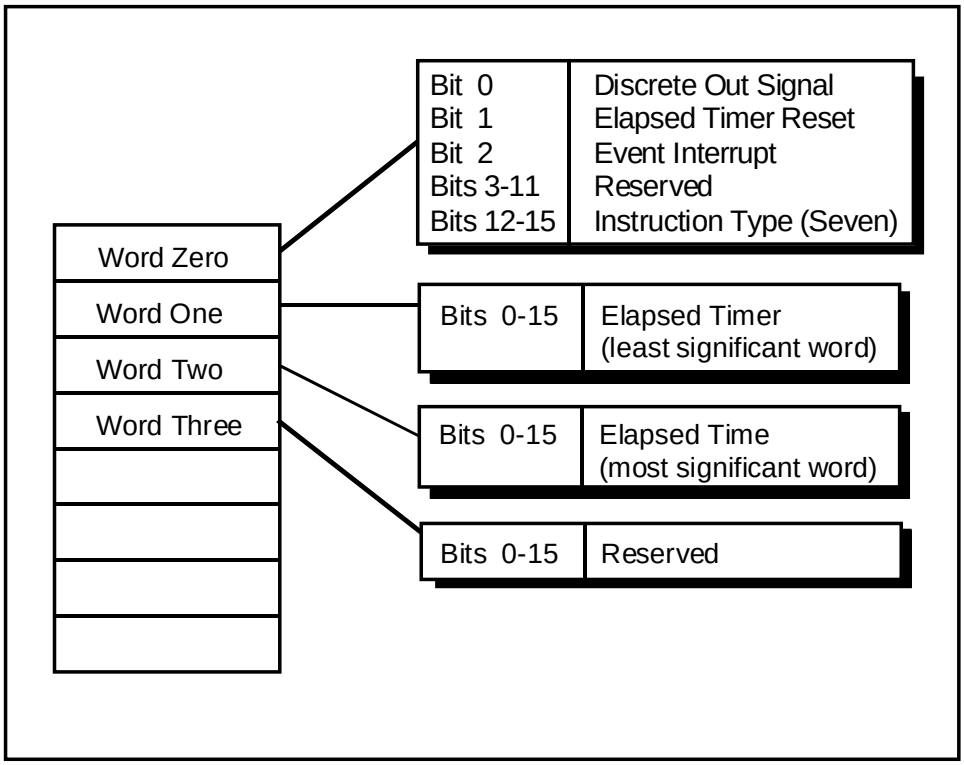


Figure 3-14. Halt Until ELT (Instruction 07H)

Word Zero

Bits 15-12 Instruction Type (07H)

Bits 11-13 Reserved

Bit 2 Event Interrupt
If ON, the DTI-PC posts an interrupt at the completion of executing and processing this command block before proceeding to the next buslist instruction.

Bit 1 Elapsed Timer Reset
If ON, the DTI-PC resets the onboard elapsed timer to zero prior to executing the command block.

Bit 0 Discrete Out Signal
If ON, the DTI-PC generates a signal to the connector prior to executing this command block. The length of this signal is two microseconds.0

Word One

Bits 15-0 Elapsed Timer (least significant word)
One microsecond resolution

Word Two

Bits 15-0 Elapsed Timer (least significant word)
One microsecond resolution

Word Three
Bits 15-0 Reserved

Reset Stack (Instruction 07H)
This instruction resets the internal jump address stack to the top (Figure 3-15).

Word Zero
Bits 15-12 Instruction Type
Bit 11 Event Interrupt Enable
Bits 10-2 Reserved
Bit 1 Elapsed Timer Reset
Bit 0 Discrete Out Signal

Words One through Three
All 16 bits of Words One through Three are reserved.

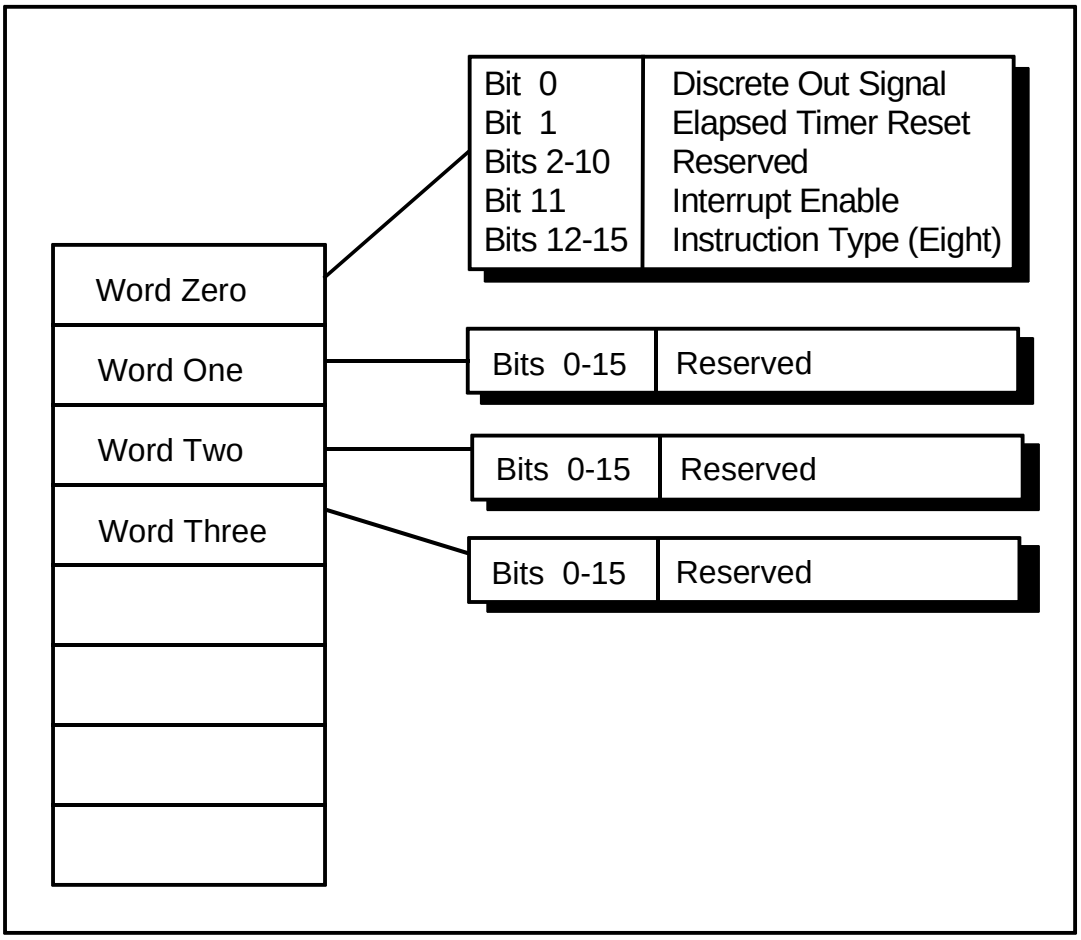


Figure 3-15. Reset Stack (Instruction 08H)

BC Mode Code Data Block

Mode Commands issued by the Bus Controller are stored in the BC Mode Code Data Block. This Block is located at the fixed memory location 1430H - 143FH.

When a Mode Command (with Data Word) is issued by the BC, the Mode Code Instruction in the buslist instruction block contains an offset (0-F) from address 1430H, which is used to transmit a data word or store a received data word (Figure 3-16).

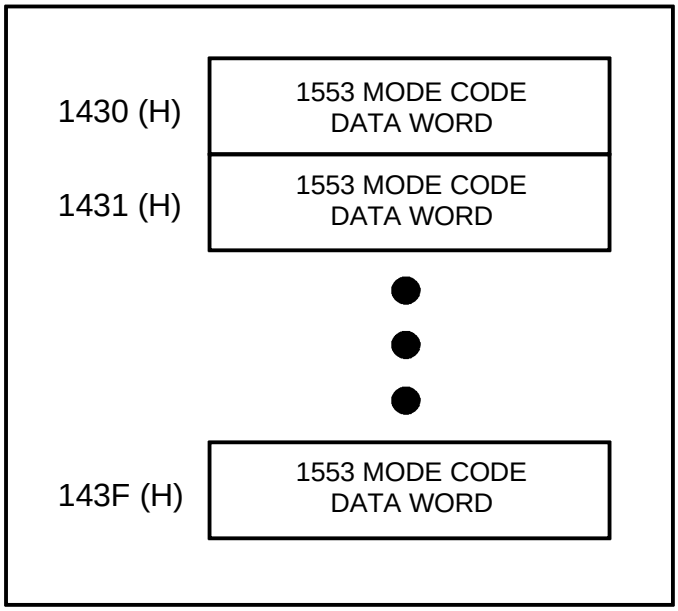


Figure 3-16. BC Mode Code Data Block

Error Injection

The Advanced Error Injection capability is based on an error index field of ten bits that is used as an offset. This offset is added to the starting address of the Error Table 1440H, which points to the user-programmed Error Control Word. This gives the user a high degree of flexibility when programming various errors to be injected.

Note: The area of memory from 1440 through 7FFFH is used for error injection, if error injection is enabled. If "n" unique errors are injected, 1440 through 1440 + (N-1) can be used for error injection and free memory begins at 1440 + n. If no errors are injected, free memory begins at 1440.

The Error Index is specified in the second word of all applicable BC buslist instructions, as well as Word Zero of the Subaddress Response Word Pair and Mode Code Response Word. If Error Injection is enabled, the Error Index field is automatically added to the Error Table and the desired error is injected.

Error Control Word
The 16 bits of the Error Control Word specify the type of error created by the DTI-PC (Figure 3-17).

Bits 0-3	Error Bit/Gap Field
Bits 4-9	Error Word
Bits 10-14	Error Code
Bit 15	Clear Error/Continuous Error

Figure 3-17. Error Control Word

Bit 15 Clear Error/Continuous Error
0 = Error once then clear
1 = Continuous Error

Bits 14-10 Error Code

Bits 9-4 Error Word
The word the error is injected upon, such as command word, second data word, etc.

Bits 0-3 Error Bit/Gap Field

Note: The Error Control Word is used by the DTI-PC only if "BC Error" is enabled in the BC Error Control Register 14 or if the Error Interrupt Enable Bit is set in Word 0 of the Subaddress Response Word Pair or Mode Code Response Word.

Error Codes
The Error Control Word provides 11 types of errors:

- Mid-Sync Zero Crossing
- Mid-Bit Zero Crossing
- Sync Encoding
- Bi-Phase Encoding
- Bit Count Low
- Bit Count High
- Parity
- Gap Injected
- Set Status Bit
- No Response
- Word Count

One error per message can be injected with the error on the command or data word, before the message is transmitted on the multiplex data bus (Table 3-2).

Mid-Sync Zero Crossing
The typical mid-sync zero crossing occurs at 1.5 microseconds from start of sync. When this error is injected, the mid-sync zero crossing is skewed left or right ±150 nanoseconds.

Mid-Bit Zero Crossing
The typical mid-bit zero crossing occurs 500 nanoseconds from the start of the bit time. When this error is

injected, the mid-bit zero crossing is skewed left or right ±150 nanoseconds.

Sync Encoding
Sync encoding injects an encoding error into the sync field.

Bi-Phase Encoding
During a bit time, the bit does not make a zero-crossing transition.

Bit Count Low
Qualified word is transmitted with 18 or 19 bits instead of 20 bits.

Bit Count High
Qualified word is transmitted with 21, 22 or 23 bits instead of 20 bits.

Parity
Qualified MIL-STD-1553 word bits are transmitted with even parity.

Gap Injected
A programmable gap of 2.6 to 8.4 microseconds can be injected between contiguous words within a message stream (Tables 3-2 and 3-3).

Set Status Bits
A qualified bit is set in the 1553 status response word. Only one bit can be set at a time.

No Response
A qualified RT/SA that is addressed and does not respond to the valid command or mode command transmitted on the 1553 bus.

Word Count
A qualified message transmitted with 0-63 data words.

Error Type	Error Code Setting	Error Word	Error Bit/ Gap Count
No Error	0H	N/A	N/A
Mid-Sync Zero Crossing			
<-150 nanoseconds	3H	0-20H	N/A
>+150 nanoseconds	1H	0-20H	N/A
Mid-Bit Zero Crossing			
<-150 nanoseconds	1CH	0-20H	F-0H
>+150 nanoseconds	17H	0-20H	F-0H
Sync Encoding			
111100	2H	0-20H	N/A
111010	4H	0-20H	N/A
110000	5H	0-20H	N/A
011000	6H	0-20H	N/A
000011	7H	0-20H	N/A
000110	AH	0-20H	N/A
001111	CH	0-20H	N/A
100111	DH	0-20H	N/A
000111	EH	0-20H	N/A
111000	FH	0-20H	N/A
Bi-Phase Encoding			
Bits 0-15	1DH	0-20H	F-0H
Parity Bit	1EH	0-20H	N/A
Bit Count Low			
1 Bit	11H	0-20H	N/A
2 Bits	12H	0-20H	N/A
Bit Count High			
1 Bit	13H	0-20H	N/A
2 Bits	14H	0-20H	N/A
3 Bits	19H	0-20H	N/A
Parity	16H	0-20H	N/A
Gap Injected	15H	1-19H	F-0H
Status Bit Injection	8H	N/A	F-0H
No Response Error	9H	N/A	N/A
Word Count Error	BH	0--3F	N/A

Table 3-2. Error Codes

Gap Count	Number of Microseconds
0	2.0
1	2.5
2	3.0
3	3.5
4	4.0
5	4.5
6	5.0
7	5.5
8	6.0
9	6.5
A	7.0
B	7.5
C	8.0
D	8.5
E	9.0
F	9.5

Table 3-3. Gap Count Field in Microseconds

Each value is measured from mid-bit to mid-bit crossing.

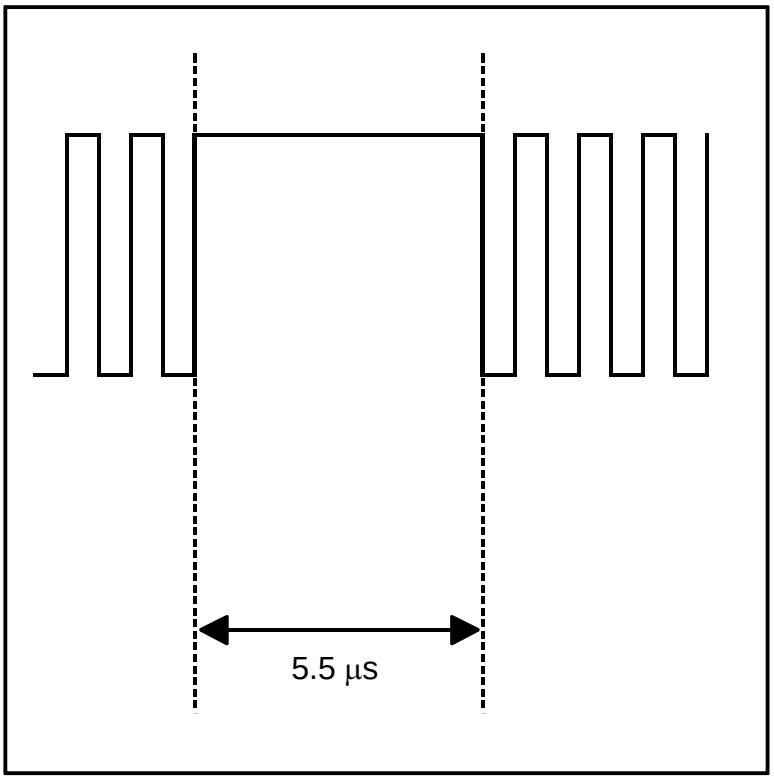


Figure 3-18. Sample Gap Injection of 5.5 Microseconds

Chapter 4. Multiple Remote Terminal Mode of Operation

The MRT mode allows emulation of up to 32 RTs (31 Rts and one Broadcast RT). For each RT, up to 32 subaddresses may be configured. Subaddresses 0 and 31 can only be configured as mode code subaddresses. Subaddresses 1 through 30 can only be configured as data subaddresses.

Status Block

In the MRT mode, each RT address is associated with a Status Block (located in Dual Port RAM) which contains a control word, status word and other data relating to its configuration (Figure 4-1). The RT Status Blocks occupy a space in memory from 1000H- 11FFH.

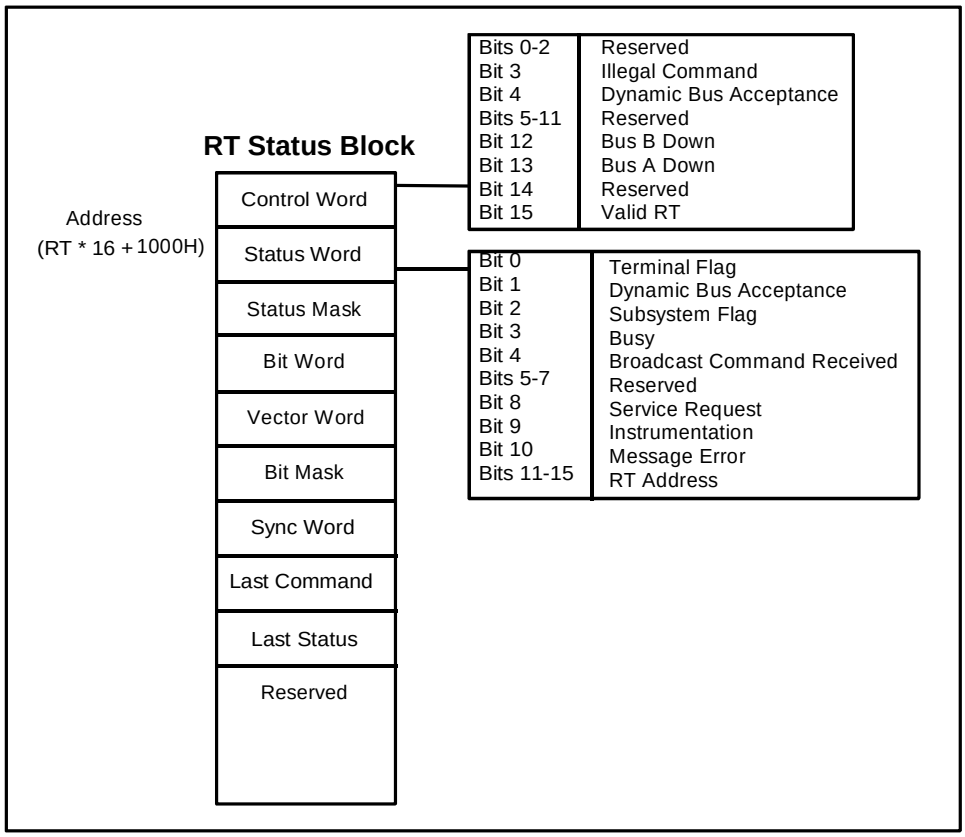


Figure 4-1. RT Status Block

Via the control word, the user can specify a variety of parameters that relate to each individual RT's behavior:

- If the RT is on-line or off-line
- If the RT (when on-line) is enabled only on Bus A, Bus B or Bus A and Bus B.
- If the RT responds to illegal mode commands with no response or with Message Error Bit set.

The status block contains:

- The status response word of the RT
- A mask to be ANDed with the RT's status word before it is sent out
- The RT's BIT word
- The RT's vector word
- A mask that is ANDed with the BIT word if a Reset RT mode code is received
- Sync word
- The last command word to the RT
- The last status response word of the RT

Contents of RT Status Block	Address
Control Word	0000
Status Word	0001
Status Mask	0010
Bit Word	0011
Vector Word	0100
Bit Mask	0101
Sync Word	0110
Last Command	0111
Last Status	1000

During operation, each RT's status word is re-calculated and the last command word and status word are updated as each message is received. Appropriate bits in the status word are set by the microcode. The RT receiving the command is a MIL-STD-1553 compliant RT.

Control Word

Bit 15 Valid RT

Bit 14 Reserved

Bit 13 Bus A Down

Indicates the Primary Bus is shut down. Bit 13 is affected by the Transmitter Shutdown and Override transmitter Shutdown mode commands or may be set by the host software.

Bit 12 Bus B Down

Indicates the Secondary Bus is shut down. Bit 12 is affected by the Transmitter Shutdown and Override Transmitter Shutdown mode commands or may be set by the host software.

Bits 11-5 Reserved

Bit 4 Dynamic Bus Acceptance

Controls the RT's response to an Accept BC mode command. If Bit 4 is ON, the RT sets the BC Acceptance Bit in its status, in response to that mode code.

Bit 3 Illegal Command

If ON, the RT responds to illegal mode commands by returning a status word with the Message Error Bit set, with no data words. If OFF, the RT does not respond to illegal commands.

Bits 2-0 Reserved

Status Word
The Status word is ANDed with the RT Status Mask Word and sent as the RT's status response to all legal commands except a Transmit Last Status or Transmit Last Command mode code.

Bits 15-11 RT Address

Per MIL-STD-1553, Bits 15-11 indicate the RT address (0-31).

Bit 10 Message Error

Bit 10 indicates a sync, length, parity or Manchester error.

Bit 9 Instrumentation

Bit 9 distinguishes a status word from a command word.

Bit 8 Service Request (Optional)

Bit 8 indicates the RT has requested service.

Bits 7-5 Reserved

Bit 4 Broadcast Command Received

Bit 3 Busy

Bit 3 indicates the RT is unable to move data.

Bit 2 Subsystem Flag

Bit 2 indicates a fault in an RT (specifically, invalid data).

Bit 1 Dynamic Bus Acceptance

Controls the RT's response to an Accept BC mode command. If Bit 1 is set to ON, the RT sets the BC Acceptance Bit in its status, in response to that mode code.

Bit 0 Terminal Flag

Bit 0 should be ON when there is a fault in an RT.

Status Mask Word
When the Status Mask Word contains a 1 in any bit position, the corresponding bit in the Status Word is transmitted. A 0 causes the corresponding Status Bit to be transmitted as a zero regardless of the state of the bit in the Status Word. For most conditions, this word should be FFFFH.

Bit Word
The user defines the Bit word to be transmitted in response to a Transmit Bit Word mode command. This word is reset by a Reset RT mode code, depending on the mask value in the RT Bit Mask Word. (ANDed with bit mask on Reset RT mode code).

Vector Word
The user-defined Vector word is transmitted in response to a Transmit Vector Word mode command. The Vector word notifies the BC that the RT requires service over and above the Service Request Bit being set.

Bit Mask Word
When the bit mask word has a 0 in any bit position, the corresponding bit in the Bit Word is reset upon reception of a Reset RT mode command.

Synchronization Word
The received data word with a Synchronize with Data mode command stored by the DTI-PC.

Last Command Word
The last valid command word received by this RT. This word is meaningless, if the Transmit Last Command mode code is the first command to the RT.

Last Status Word
This word is the Status Word associated with the last valid command addressed to the RT. It is loaded during initialization if the Transmit Last Command mode code is the first command to the RT.

Addressing the Status Block

To address the status block, follow this formula:

RT#
0001 000 _ _ _ _ _ 0000

Enter the appropriate RT number (0-31) in the five-bit space reserved for RTs.

Example
To enter RT 2:

0001 0000 0010 0000
RT
1 0 2 0 The address of the status block for RT2 is 1020.

To calculate the origin of RT 2's staus block, enter a "2" in the field (Bits 4-8).

Broadcast Enable Registers

An RT is notified of broadcast commands if it is enabled and the bit corresponding to this RT is set in the appropriate Broadcast Notification Word. Two words of BIU memory, at 140CH (Figure 4-2) and 140FH (Figure 4-3), indicate the RTs to be notified of broadcast messages.

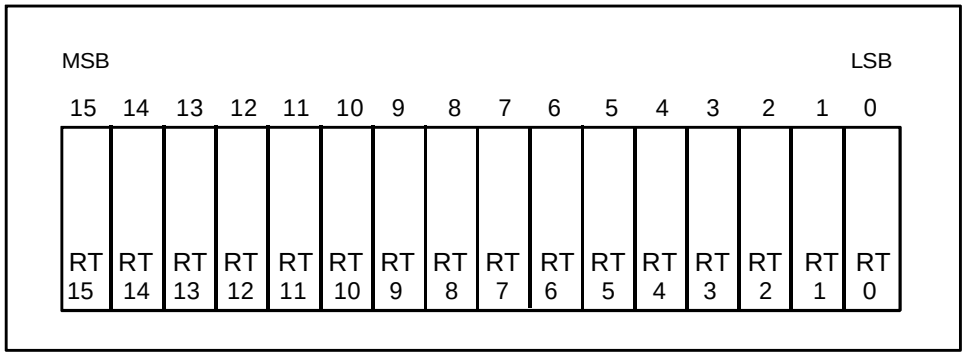


Figure 4-2. RT 0-15 Broadcast Enable Register 140CH

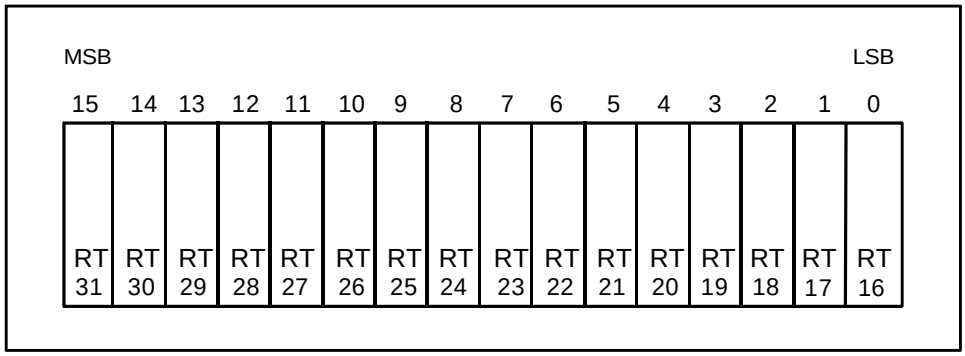


Figure 4-3. RT 16-31 Broadcast Enable Register 140FH

To notify RTs 0, 5, 10, 15, 20, 25 and 30 of broadcast messages, the value of 0x8421 is loaded into BIU address 140CH and 0x4210 is loaded into BIU address 140FH. It is not necessary to set the bit corresponding to RT31.

To see if an enabled RT is participating in the transmitted broadcast message, a Mode Code 2 (Transmit Last Status) or Mode Code 18 (Transmit Last Command) must be transmitted on the 1553 bus. If the RT used in the mode code is enabled for broadcast, the Broadcast Message Received (BRC) bit is set in the 1553 status response.

Extracting Addresses from the Command Word

Each RT's Subaddress Response word pair is located at pre-defined addresses. The DTI-PC computes the address of the RT's Subaddress Response word pair from the command word received by the emulated RT. If the subaddress field of the command word is 1-30, the DTI-PC uses the pointer in the second word to identify the Message Block's address. This message block's data buffer is transferred to or from the MIL-STD-1553 bus. If the command word references subaddress 0 or 31, the DTI-PC uses the pointer in the second word to identify the address of the RT Mode Code Response Block.

Subaddress Response Word Pairs

The subaddress response word pairs are located in memory between addresses 0000H and 0FFFH. There is one pair for the receive direction and one pair for the transmit for each RT SA combination.

To address the subaddress response word pairs, use this formula for RECEIVE:

RT		SA	
0000	0	0	Word One
0000	0	1	Word Two

To address the subaddress response word pairs, use this formula for TRANSMIT:

RT		SA	
0000	1	0	Word One
0000	1	1	Word Two

Note: Transmit is always determined by Bit 6 set to 1 and the second word of a word pair is denoted by Bit 0 set to 1.

Example 1
To address Word One of RT 0, with SA1 to receive:

0000 00000 0 00001 0
RT0 SA

If the second word of the pair is to be written to, enter a 1 in Bit 0 of the address formula to calculate the address.

Enter: 0000 00000 0 00001 1

Example 2
To address Word One of RT5, SA 10 to receive:

0000 00101 0 01010 0
RT5 SA10

If the Monitor Bit (Bit 11) of the first word of the Data Subaddress Response Word Pair for a data subaddress is set, a message directed to this rt/direction/sa combination is captured by the monitor, if it is executing (Figure 4-4). The subaddress does not have to be enabled for the message to be captured (Bit 15 can be zero).

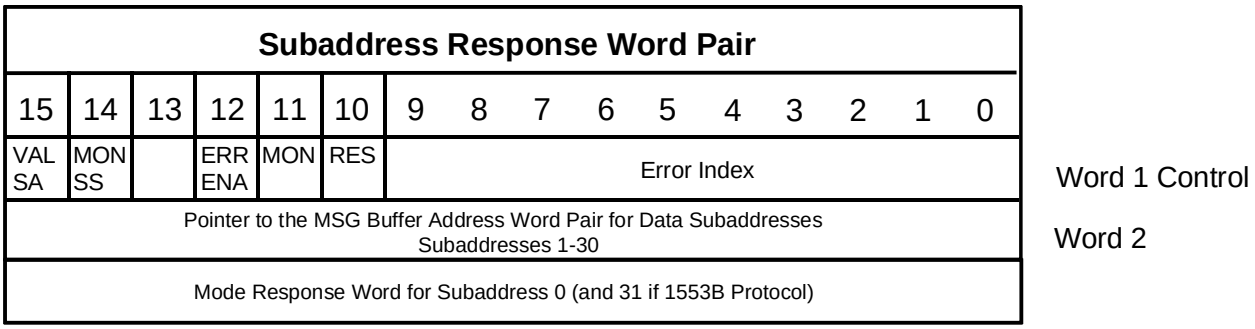


Figure 4-4. Subaddress Response Word Pair

Word One

Bit 15 Valid Subaddress (VAL SA)

Set to 1 by software if this is a valid subaddress. Set to 0 by software if it isn't.

Bit 14 Monitor Snapshot (MON SS)

Set to 1 by software if message to this subaddress should generate a snap shot interrupt. Set to 0 by software if it shouldn't.

Bit 13 Reserved

Bit 12 Enable RT Error Injection (ERR ENA)

Bit 11 Monitor Enable (MON)

Set to 1 by software if subaddress is to be monitored. Set to 0 by software if it isn't.

Bit 10 Reserved

Bits 9-0 Error Index

See the Error Injection section of Chapter 3, Bus Controller, for details.

Word Two (SA1-30)

Word Two points to the Message Buffer Address Word Pair if SA1-30, located in the Message Block (Figure 4-5). This word pair contains the address of the last buffer to receive data and the address of the last buffer to transmit data, in free memory, followed by the buffers.

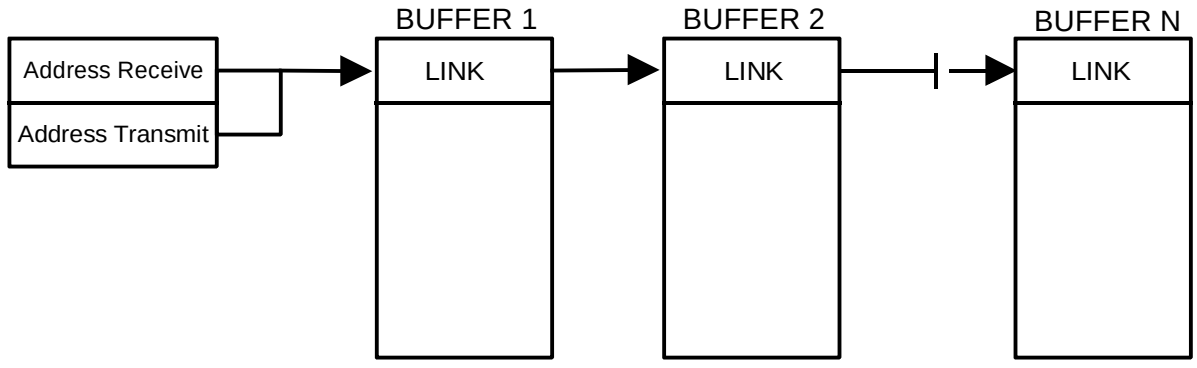


Figure 4-5. DTI-PC Message Block

The only words of the 1553 message stored in the buffer are the data words (Figure 4-6). Initially, the software loads both pointers with the address of the last buffer in the message block. The microcode

modifies the pointers as the data in the buffers is transmitted and received.

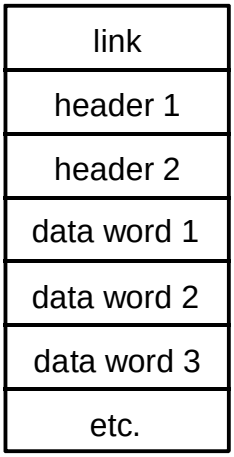


Figure 4-6. Message Buffer

Message Buffers

Message Buffer Link Word

The first word of a message buffer is a link word containing the address of the next buffer in the message block. The link word of the last buffer holds the address of the first buffer (Figure 4-7). The software loads the correct value into the link word of each buffer.

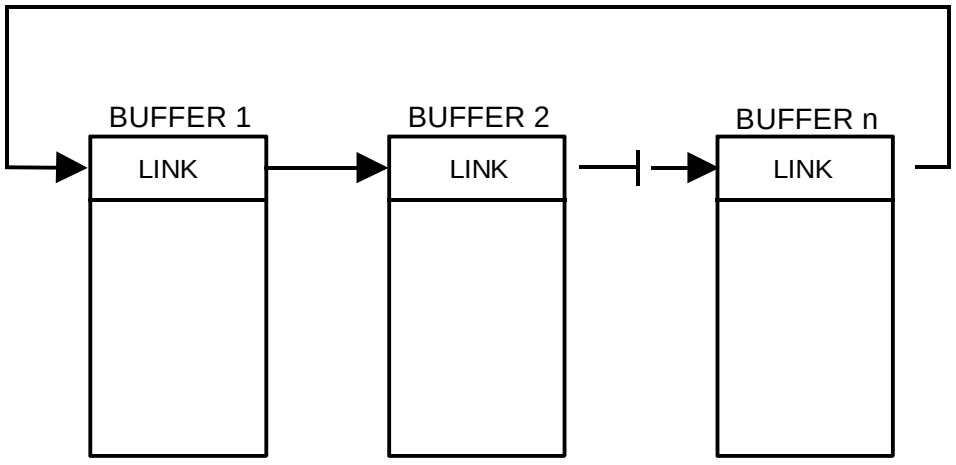


Figure 4-7. Message Buffer Link Words

Header Word 1
The header word contains the buffer word count and the control and status bits. One header word bit indicates if a missed data condition occurs. The header word also contains a bit that indicates if an overwrite condition occurs. (A message overwrites the previous buffer contents since the new data bit is set in the next buffer and the overwrite current buffer bit is set in this buffer). The software and microcode write to several of the bits (Figure 4-8).

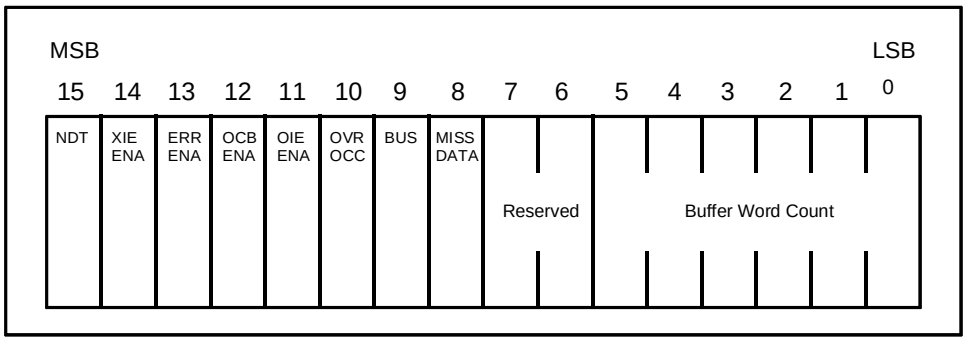


Figure 4-8. Header Word 1

Bit 15 New Data (ND)

Set to 1 by software before transmit. Set to 0 by software before receive. Set to 1 by microcode after receive. Set to 0 by microcode after transmit.

Bit 14 Transfer Interrupt Enable (XIE ENA)

Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 13 Error Interrupt Enable (ERR ENA)

Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 12 Overwrite Current Buffer (OCB ENA)

Set to 1 by software to allow overwrite. Set to 0 by software to prevent overwrite. The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. IF the new Data Bit is reset in the next buffer, the data words are stored in the next buffer. If the New Data Bit is set in the next buffer and the Overwrite Current Buffer Bit is set in the current buffer, the data is written to the current buffer. Otherwise, the data is not stored in the buffer and the Missed Data Bit is set in the current buffer.

Bit 11 Overwrite Interrupt Enable (OIE ENA)

Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 10 Overwrite Condition Occurred (OVR OCO)

Set to 0 by software initially and after it is set by microcode. Set to 1 by microcode when overwrite occurs.

Bit 9 Reserved

Bit 8 Missed Data Condition Occurred (MISS DATA)

Set to 0 by software initially and after it is set by microcode. Set to 1 by microcode when overwrite occurs.

Bits 7-6 Reserved

Bits 5-0 Buffer Word Count (0-63)

Header Word 2
The received word count field is stored by the microcode in Header Word 2 and reflects the number of

data words stored during a receive message (Figure 4-9). If this same buffer is involved in a transmit message, the received word count field is set to 0 by the microcode. Bits 15-6 are reserved and may be non-zero.

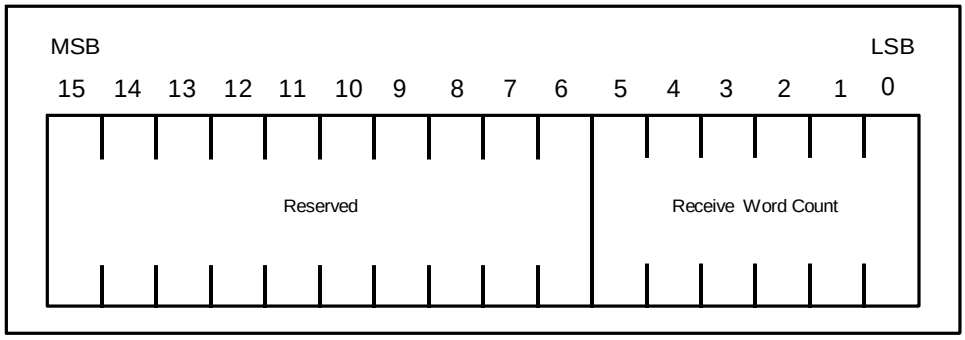


Figure 4-9. Header Word 2

Data Words
All data words transacted in the 1553 message follow Header Word 2.

Word Two (SA0 or 31) Mode Subaddress
If the transmitted or received subaddress is 0 or 31, Word Two of the SA Response Word Pair points to the Mode Code Response Block. The on-board Configuration data adds the Mode Code number to contents of Word Two; thus, pointing to the proper Mode Code Response Word within the Mode Code Response Block.

Mode Code Response Word Subaddress 0 or 31

For mode SA, the message is monitored only if the Monitor Bit (Bit 11) is set in the first word of the corresponding mode code response word (Figure 4-10).

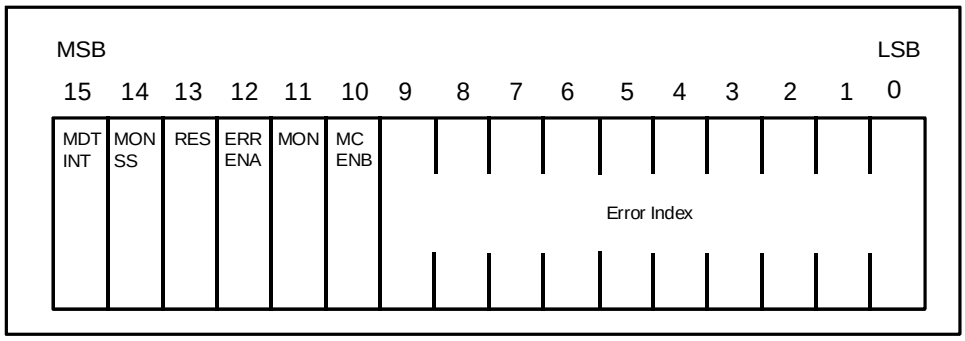


Figure 4-10. Mode Code Response Word

Bit 15 Interrupt Reception of Mode Code (MDT INT)
Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 14 Monitor Snapshot (MON SS)
Set to 1 by software if message to this SA should generate a shap shot interrupt. Set to 0 by software if it shouldn't.

Bit 13 Reserved

Bit 12 Error Enable (ERR ENA)

Bit 11	Monitor Enable (MON) Set to 1 by software, if SA is to be monitored. Set to 0, if not.
Bit 10	Mode Code Enable (MC ENB) Set to 1 by software to endable this mode code.
Bits 0-9	Error Index See the Error Injection section of Chapter 5, Bus Controller, for details.

RT Mode Code Response Word Block

The Mode Code Response Word Block is a group of 32 words, one for each Mode Code, that specify the operation the mode codes perform. The Mode Code Response Block also specifies if the receipt of any particular mode code causes the DTI-PC to interrupt the host. The first word in the block is placed between 1430H- End of Memory. The remaining word is off-set from the initial address by n, where n = mode code.

Associated Mode Code	Function
0	Dynamic Bus Control
1	Synchronize (without data word)
2	Transmit Last Status Word
3	Initiate Self Test
4	Transmitter Shutdown
5	Override Transmitter Shutdown
6	Inhibit Terminal Flag Bit
7	Override Inhibit Terminal Flag Bit
8	Reset Remote Terminal
A-F	Undefined
10	Transmit Vector Word
11	Synchronize (with data word)
12	Transmit Last Command
13	Transmit Bit Word
14-1F	Reserved

Table 4-1. MIL-STD-1553 Mode Codes

RT Mode Code Response Messages
(RT 0-30 Not Broadcast)

Mode Code Number	T/R	Operations Performed By Microcode
0	1	Dynamic Bus Control - Read RT Status Word as Status - If Dynamic Bus Acceptance (DBA) flag set in RT Control Word: Set DBA Bit in Status Word - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
1	1	Synchronize Without Data Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
2	1	Transmit Last Status Word - Read Last Status Word as Status - AND Status with Status Mask - Transmit Status onto Bus - Write Command into Last Command Word
3	1	Initiate Self-Test - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
4	1	Transmitter Shutdown - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Set Bit in RT Control Word to disable opposite bus - Write Status into Last Status Word - Write Command into Last Command Word

RT Mode Code Response Messages - Continued
(RT 0-30 Not Broadcast)

Mode Code Number	T/R	Operations Performed By Microcode
5	1	Override Transmitter Shutdown - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Clear bit in RT Control Word to enable opposite bus - Write Status into Last Status Word
6	1	Inhibit Terminal Flag - Read RT Status Word as Status - Clear Terminal Flag Bit in Status - Mask to inhibit terminal flag - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
7	1	Override Inhibit Terminal Flag - Read RT Status Word as Status - Set Terminal Flag Bit in Status Mask to enable terminal flag - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
8	1	Reset Remote Terminal - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Logically AND the BIT Word with the BIT Mask then place the result back in the BIT Word - Clears bits in Control Word to enable both transmitters - Set the Terminal Flag Bit in the Status Mask to enable the Terminal Flag Bit

RT Mode Code Response Messages - Continued
(RT 0-30 Not Broadcast)

Mode Code Number	T/R	Operations Performed By Microcode
9-15	0 0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing
16	1	Transmit Vector Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit Vector Word onto bus - Write Status into Last Status Word - Write Command into Last Command Word
17	0	Synchronize with Data Word - Read RT Status Word as Status - Write the received data to Sync Word - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
18	1	Transmit Last Command - Read Last Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit Last Command Word onto bus

RT Mode Code Response Messages - Continued
(RT 0-30 Not Broadcast)

Mode Code Number	T/R	Operations Performed By Microcode
19	1	Transmit BIT Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit BIT Word onto bus - Write Status into Last Status Word - Write Command into Last Command Word
20-31	0 0	Illegal

Table 4-2. RT Mode Code Response Messages

RT Mode Code Broadcast Response Messages
(RT=31 Broadcast)

Mode Code Number	T/R	Operations Performed By Microcode
0	0 0	Illegal
1	1	Synchronize - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
2	0 0	Illegal
3	1	Initiate Self Test: - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write Status into Last Status - Write Command into Last Command Word - Link to next broadcast RT

RT Mode Code Broadcast Response Messages - Continued
(RT=31 Broadcast)

Mode Code Number	T/R	Operations Performed By Microcode
4	1	Transmitter Shutdown - Read RT Status Word as Status - Set BRC Bit in Status - Set bit in RT Control Word to disable opposite bus - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
5	1	Override Transmitter Shutdown - Read RT Status Word as Status - Set BRC Bit in Status - Clear bit in RT Control Word to enable opposite bus - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
6	1	Inhibit Terminal Flag: - Read RT Status Word as Status - Set BRC bit in Status - Clear Terminal Flag Bit in status Mask to inhibit Terminal flag - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
7	1	Override Terminal Flag - Read RT Status Word as Status - Set BRC Bit in Status - Set Terminal Flag Bit in Status Mask to enable terminal flag - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT

RT Mode Code Broadcast Response Messages - Continued
(RT=31 Broadcast)

Mode Code Number	T/R	Operations Performed By Microcode
8	1	Reset RT: - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Clear bit in RT Control Word to enable opposite bus - Set Terminal Flag Bit in Status Mask to enable terminal flag - Logically AND the BIT Word with the BIT Mask. Place the result in the BIT Word - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
9-16	0 0	Illegal
17	0	Synchronize with Data: - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write received data to Sync Word - Write Status into Last Status Word - Write Command into Last Command Word - Link to Next Broadcast RT
18-31	0 0	Illegal

Table 4-3. RT Mode Code Broadcast Response Messages

Interrupts

The RT mode may post hardware interrupts to the host including:

- Mode Code Execution
- Message Transmission or Reception to or from a Message Block
- Message Buffer Overflow Condition
- Transfer
- Receiver Error Detected

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Chapter 5. Chronological Monitor Mode of Operation

The Chronological Monitor allows for the capture of all or selected traffic while simultaneously acting as a BC and/or one or more RTs.

Record All/Selected Capture

To capture all traffic, the Monitor bit must be set in all data subaddresses and mode code response words as well as the Monitor Invalid Command Bit in the Control Register.

Monitor Block

The monitor block consists of one or more monitor buffers (Figure 5-1). The monitor block requires that the address of the first monitor buffer be written to reserved memory location 1408H before monitoring begins, by writing a value of 8 to the Monitor Control Register. Writing a value of 18H allows the monitor to record 1553 command words containing protocol errors.

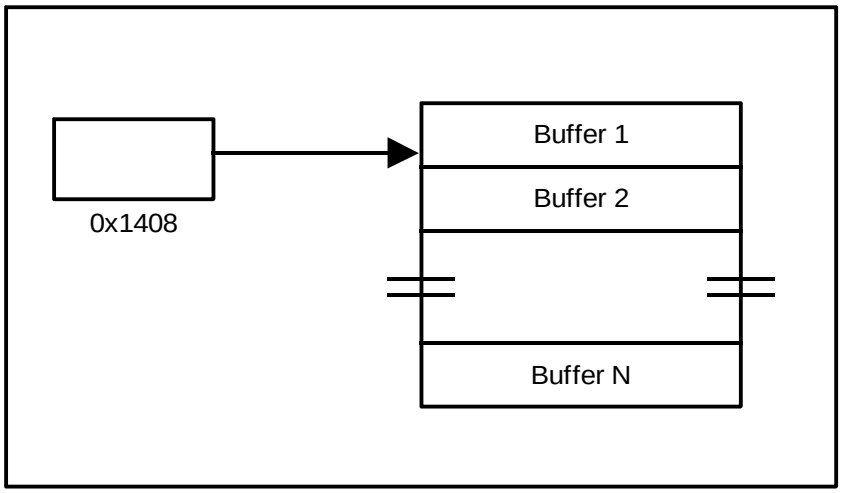


Figure 5-1. Monitor Block

Monitor Buffer

The size of a monitor buffer ranges from 16 to 1008 (63*16) words (Figure 5-2). The buffer begins with a link word and a header word and ends with two reserved words. The remainder of the buffer (Message Records) is used to store 1553 messages and information related to the message, such as tag words and current elapsed timer value.

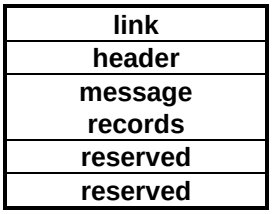


Figure 5-2. Monitor Buffer

Monitor Buffer Link Word

The first word of a monitor buffer, the link word, contains the address of the next monitor buffer. The link word of the last buffer must hold the address of the first buffer (Figure 5-3). The software is responsible for loading the correct value into the link word of each buffer.

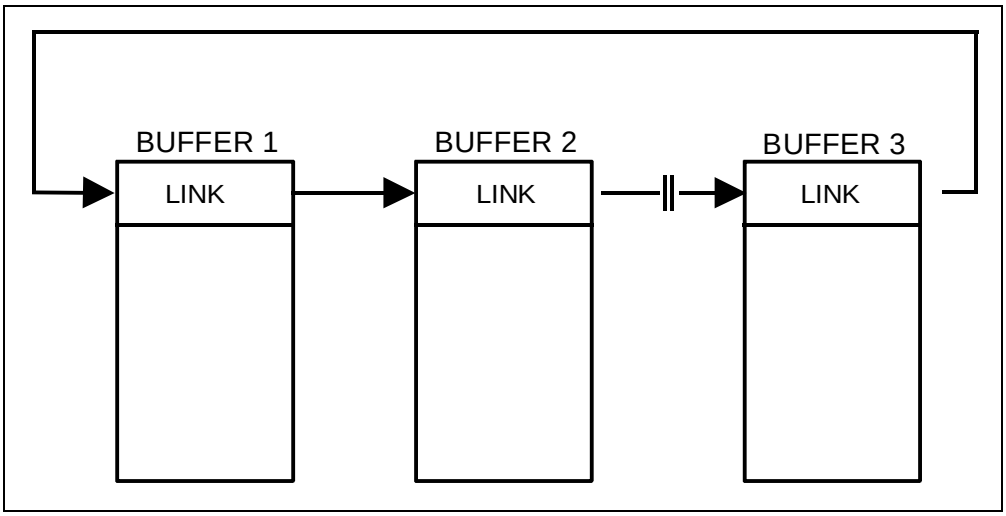


Figure 5-3. Monitor Buffer Link Word

Header Word

The header word contains the buffer block count and the control and status bits. One header word bit indicates if a missed data condition occurs. Another bit indicates if an overwrite condition occurs. (A message overwrites a buffer's previous contents, since the new data bit is set in the next buffer and the overwrite current buffer bit is set in this buffer). The software and microcode write to several of these bits (Figure 5-4).

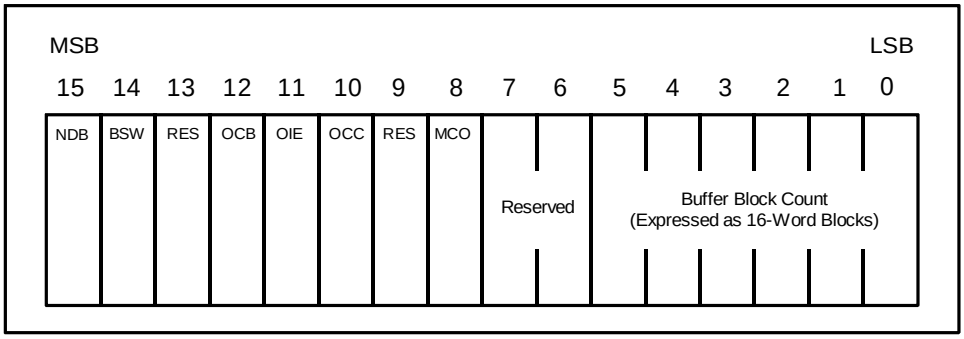


Figure 5-4. Header Word

Bit 15 New Data Bit (NDB)

Set to 1 by software before transmit. Set to 0 by software before receive. Set to 1 by microcode after receive. Set to 0 by microcode after transmit.

Bit 14 Buffer Switch Interrupt Enable (BSW)

If set to 1, the DTI-PC generates an interrupt when switching from current buffer to next buffer.

Bit 13 Reserved

Bit 12 Overwrite Current Buffer (OCB)

Set to 1 by software to allow overwrite. Set to 0 by software to prevent overwrite. The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. If the New Data Bit is reset in the next buffer, the data words are stored in the next buffer. If the New Data Bit is set in the next buffer and the Overwrite Current Buffer Bit is set in the current buffer, the data is written into the current buffer. Otherwise, the data is not stored in the buffer and the Missed Data Bit is set in the current buffer.

Bit 11 Overwrite Interrupt Enable (OIE)

Set to 1 by software to enable interrupt. Set to 0 by software to disable interrupt.

Bit 10 Overwrite Condition Occurred (OCO)

Set to 1 by software initially and after it is set by microcode. Set to 1 by microcode when overwrite occurs.

Bit 9 Reserved

Bit 8 Missed Data Condition Occurred (MCO)

Set to 0 by software initially and after it is set by microcode. Set to 1 by microcode when overwrite occurs.

Bits 7-6 Reserved

Bits 5-0 Buffer Word Count (0-63)

Multiply this number by 16 to get actual buffer size.

Message Record

When a message is monitored, it is stored in a message record (Figure 5-5). (The words in the message record are explained later in this chapter). Part of a message can be stored at the end of one message record buffer and the rest of the message stored at the beginning of the next message record buffer (Figure 5-6).

Reserved
Start of Message
ELT (MSW)
ELT (LSW)
First Word of Message
Tag Word
Second Word of Message
Tag Word
Third Word of message
Tag Word
ETC
Reserved
0000

Figure 5-5. Message Record Format

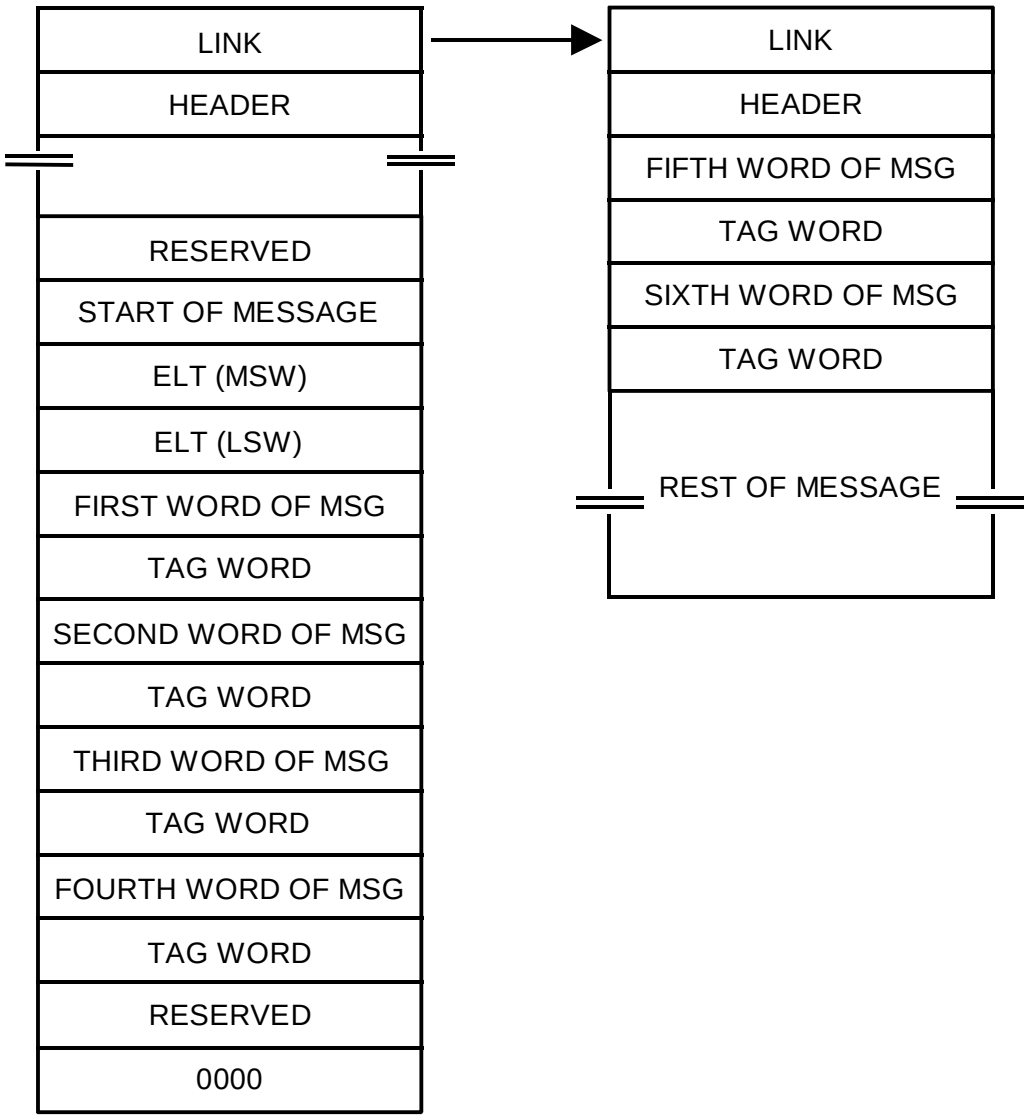


Figure 5-6. Message Record Storage Buffers

Example
If fewer than ten words appear in the message record buffer (eight words for storing 1553 information and two reserved words at the end of the buffer) the next message is stored at the beginning of the next message record buffer, after the last word of the message is stored (Figure 5-7). The message record ends with a reserved word, followed by a word of zeroes. These two words serve as an end-of-message indicator and are overwritten by the first two words of the next message record when the monitored message is received.

If no more messages are captured, the end-of-message indicator signals the end of monitored information in this buffer. As each word of the 1553 message and its tag word are stored in the buffer, the end-of-message indicator is written after the tag word; however, when the next word of the message is stored with its tag word, the end-of-message indicator is overwritten and a new end-of-message indicator is written after the tag.

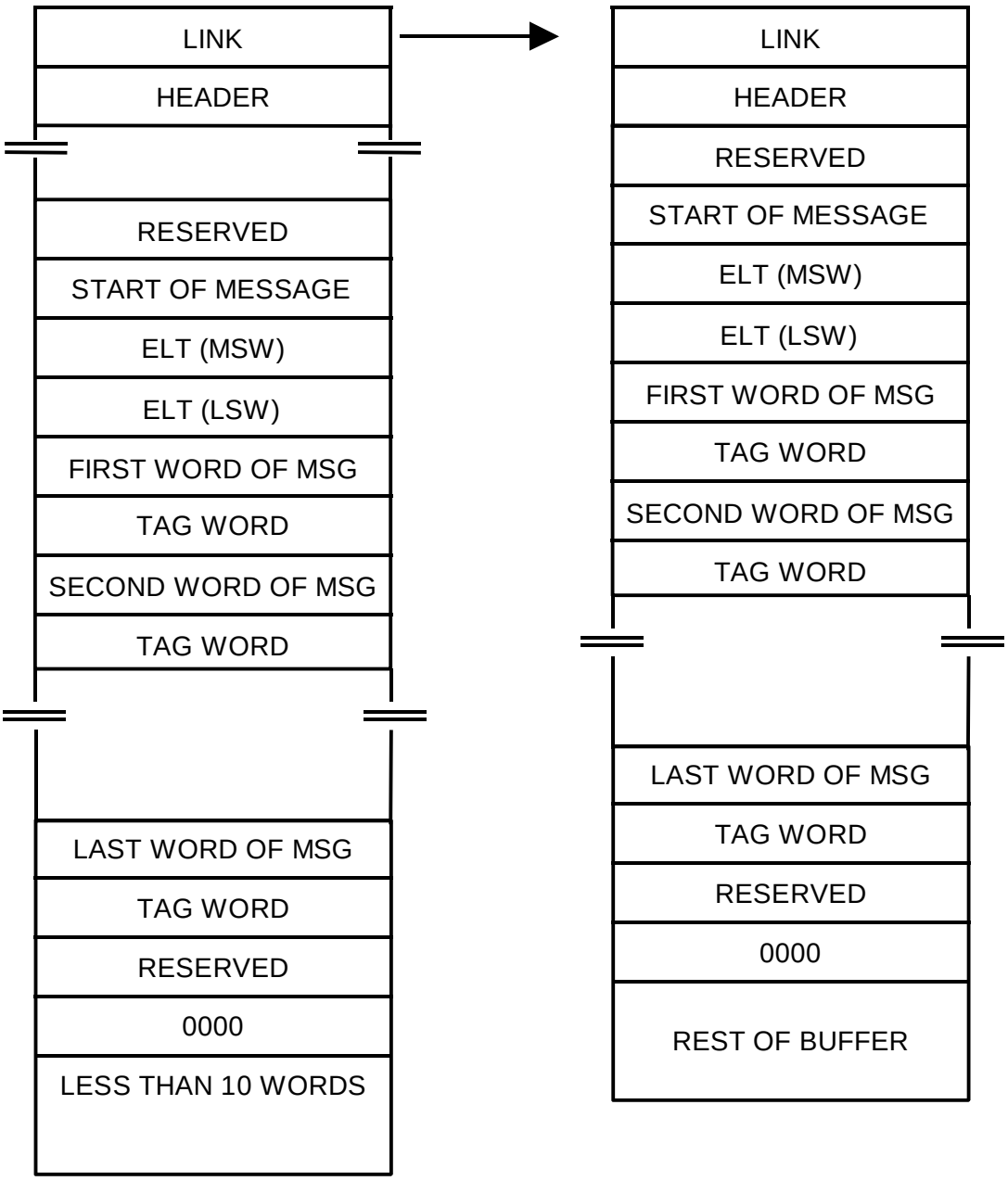


Figure 5-7. Message Record Storage Buffers

First Word
The first word of the message record is reserved.

Start of Message Tag Word
Bits 15 and 14 of this word are set, indicating that this is the start of the message tag word.

Elapsed Timer Word ELT (MSW)
The next word is the most significant 16 bits of the elapsed timer.

Elapsed Timer Word ELT (LSW)
The least significant 16 bits of the elapsed timer are stored next.

1553 Message and Tag Words
A word from the message followed by its tag word alternates until the message is finished.

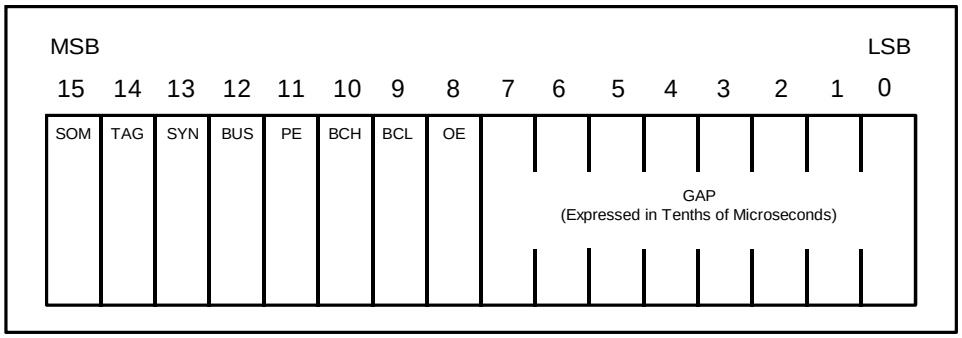


Figure 5-8. Message Record Storage With Split Record

Bit 15	Start of Message (SOM)
	Bit 15 is set if this is the first word of the message.
Bit 14	Tag (TAG)
	Bit 14 is set in every tag word, including start of message tag.
Bit 13	Sync of Word (SYN)
	Bit 13 is set if command or status word and reset if data word.
Bit 12	Bus on Which Word Was Transmitted (BUS)
	Bit 12 is set if word appeared on Bus A and reset if word appeared on Bus B.
Bit 11	Parity Error (PE)
	Bit 11 is set if parity error appeared in this word.
Bit 10	Bit Count High (BCH)
	Bit 10 is set if bit count high error occurred in this word.
Bit 9	Bit Count Low (BCL)
	Bit 9 is set if bit count low error occurred in this word.
Bit 8	Other Error (OE)
	Bit 8 is set if another error (sync, bi-phase, etc.) occurs in this word.
Bits 7-0	Gap Time (+/-200 nanoseconds)
	Expressed as tenths of microseconds (e.g., if value = 34 hex or 52 decimal, gap time = 5.2 microseconds).

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Chapter 6. Interrupts

Table 6-1 lists the DTI-PC interrupt types and identifies the operational modes upon which the interrupts may be enabled.

Event	Mode
Protocol Error	MRT/BC
Buffer Overflow	MRT/BC
Mode Code	MRT/BC
Receive Transfer	MRT/BC
Transmit Transfer	MRT/BC
Monitor Buffer Switch	CM
Snapshot	CM
Asynchronous Halt	BC
Transfer	BC
Instruction Complete	BC
Halt	BC
Status Exception	BC

Table 6-1. DTI-PC Interrupts

When an interrupt occurs, the board generates an interrupt packet and places it at the bottom of the interrupt queue (Figure 6-1). The user must read the Interrupt Queue Control Real-Time Control Register 1409H to determine the beginning of the linked list from which to de-queue interrupts.

When all interrupts are de-queued from the queue, write a 0 to the Interrupt Queue Control Real-Time Control Register 1409H, to instruct the firmware not to add interrupt packets to the linked list being processed by the software. The DTI-PC writes an interrupt packet into the active queue only if one or more of the interrupt bits in the Trailer Word of the interrupt queue is set.

If the interrupt queue is filled, the Queue Full Bit is set in the Trailer Word and no more interrupts are stored in the queue until existing packets are processed by the user's software and a 0 is written to the Valid Interrupt Word in each packet.

Note: A hardware interrupt is only generated when the DTI-PC writes the address of a valid interrupt packet to the Interrupt Queue Control Register 1409H.

The DTI-PC can add packets to the interrupt queue without generating a hardware interrupt, as long as the user's software has not written a 0 to the Interrupt Control Register (indicating the software has begun processing interrupt packets).

Forward Link	
RCV Command	
XMIT Command	
XMIT Data Buffer Address	
XMIT Status or Mode Code Receive Data	
RCV Status	
RCV Error Word or Data Buffer	*
Bus Controller Instruction Address	****
Buffer Switch Monitor Address	**
Command Word Address Pointer	***
Trailer Word	
Valid (FFFF)	
Reserved	
Reserved	

Figure 6-1. Interrupt Packet

* Reserved if monitor (only).
** Reserved if BC/RT modes.
*** Valid if monitor and RT/MON (only).
**** Reserved if not BC mode.

Interrupt Packet

Word 0 Forward Link

This location provides the address of the next interrupt packet. If this is the last packet within the linked list, the value will be 0.

Word 1 1553 Receive Command Word

If the message doesn't contain a Receive Command Word, a value of FFFF is written to this word.

Word 2 1553 Transmit Command Word

If the message doesn't contain a Transmit Command Word, a value of FFFF is written to this word.

Word 3 Transmit Data Buffer Address

Word # contains the address of the first word of the transmit buffer. A value of FFFF indicates that the Transmit Data Interrupt is not enabled.

Word 4 1553 Transmit Status Word or Mode Data

Stores a 1553 status word if one exists. If this message is a Mode Code 17 (Sync with Data), this is the data sent to the RT. If there is no Transmit Status word and this message is not a Mode Code 17, the value FFFF is stored in this word.

Word 5 1553 Receive Status Word

If this message does not contain a receive status, a value of FFFF is written to this word.

Word 6 Receive Error Word or Data Buffer

Address points to Word 1 of Receive Data Buffer or Receive Error Word, if an error was detected. Receive Error Word byte defined below:

MRT Receive Error

Bit 15 No Response

Bit 15 is set if the RT detects an error in data reception and does not respond with its status.

Bit 14 Word Count High

Actual word count exceeds command word count.

Bit 13 Word Count Low

Actual word count is less than command word count.

Bit 12 Wrong Sync

A word was received having data sync rather than command sync or vice versa..

Bit 11 Wrong Bus

A word has been received on the opposite bus.

Bit 10 Manchester Error

A Manchester or parity error has occurred.

Bit 9 Mode of Operation

If Bit 9 is set, it is receiving for BC. If cleared, Bit 9 is receiving for RT or MRT.

Bit 8 Buffer Overflow

Indicates that the New Data Bit has been set in the message buffer into which the received data was to be collected. A Buffer Overflow interrupt is generated if the Interrupt Overflow Error Bit is set in the receiving Message Block Header.

Bit 7-0 Reserved

Bus Controller Receive Error Word

Bit 15 No Response

Bit 14 Word Count High

Bit 13 Word Count Low

Bit 12 WR SYNC

Bit 11 WR Bus

Bit 10 Message Error

Bits 9-0 Reserved

Word 7 Bus Controller Instruction Address

If in BC mode, Word 6 points to Word 1 of the current four-word BC instruction. If not in BC mode, this word is reserved.

Word 8 Buffer Switch Monitor Address

If ten words or less remain in the current monitor buffer and the Buffer Switch Interrupt is enabled, a Buffer Switch Interrupt occurs during the last word to be stored. Word 7 points to the first word of the monitor buffer prior to the switch If no interrupt occurs or the Buffer Switch Interrupt is not enabled, the last message is overwritten.

Word 9 Command Word Address Pointer

If a Snapshot Interrupt is enabled for this command, Word 8 points to the 1553 RCV Command Word or the 1553 XMIT Command Word (if RT-to-BC or RT-to-RT) in the Monitor Buffer per the corresponding 1553 transfer.

Word 10 Trailer Word

As the last word in an interrupt packet (Figure 6-2), the Trailer Word defines valid interrupt types and sources for the corresponding 1553 message.

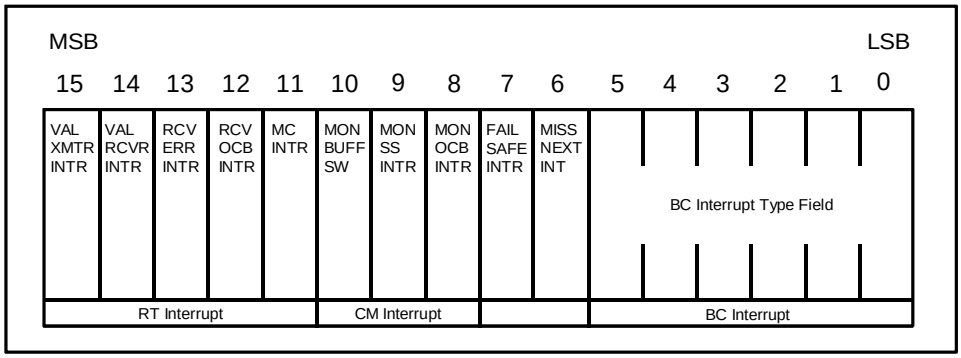


Figure 6-2. Trailer Word

MRT Interrupts (Bits 15-11)

If any of the interrupt bits are enabled in the Message Buffer Header or the Mode Interrupt is enabled in the Mode Code Response Word, the corresponding bit is set in the Trailer Word.

The MRT Interrupts are defined below:

Bit 15 Valid Transmitter Interrupt

Bit 14 Valid Receiver Interrupt

Bit 13 Receiver Error Interrupt

Bit 12 Receiver Overwrite Current Buffer Interrupt

When Bit 12 is set, Bit 14 is never set.

Bit 11 Mode Code Interrupt

Monitor Interrupts (Bits 10-8)

If any of the interrupt bits are enabled in the Monitor Buffer Header Word or any of the monitor interrupt bits are enabled in the Mode Code Response Word, the corresponding bit is set in the Trailer Word.

Bit 10 Monitor Buffer Switch Interrupt

Bit 10 is set if ten words or less remain in the current message buffer.

Bit 9 Monitor Snapshot Interrupt

Posts the address of the Command Word for the corresponding message in the second to last word of the packet. If the transfer was RT-to-RT, the address of the Transmit Command is written.

Bit 8 Monitor Overwrite Current Buffer Interrupt

Bit 7 Failsafe interrupt

Bit 7 is set if a continuous 1553 transmission of greater than 720 microseconds occurs. Jumper FS1 must also be removed.

Miss Next Interrupt (Bit 6)

1 = Interrupt queue overflowed after this block.

0 = No interrupt overflow occurred.

BC Interrupts (Bits 5-0)

Bits 5-0 specify a six-bit field that displays the BC interrupt type in the Hex format (Table 6-2).

Hex Value	Interrupt Type
2	BC Mode Code Instruction Complete
3	BC Transfer Data
4	Instruction Complete (Includes Jump, HUE, etc..)
18h	BC Overrun
6	BC Halt
8	Status Exception
10h	Protocol Error
7	BC Transfer/Instruction Complete
B	BC Transfer/Status Exception
A	BC-MC/Status Exception
F	BC Transfer/Instruction Complete/Status Exception
C	Instruction Complete/Status Exception
14	Instruction Complete/Protocol Error
1F	BC Over/BC Transfer/Instruction Complete
2X	Asynchronous Halt/ etc.

Table 6-2. Bus Controller Interrupts

Word 11 Valid Interrupt (FFFF)

Word 11 is set to a non-zero value when the DTI-PC adds the packet to the interrupt queue. The user's software must write a zero to this word when it has finished processing this packet.

Word 12 Reserved

This location reserved for internal use.

Word 13 Reserved

This location rserved for internal use.

Algorithm for Interrupt Processing

To process interrupts, follow the steps outlined below:

1. Read the value of the Interrupt Control Register to a variable in your program.
2. Write a 0 to the Interrupt Control Register.
3. Process the packet (application dependent).
4. Write a zero to the Valid Interrupt Word in the packet.
5. Read the Link Word in the packet.
6. Repeat Steps 3 through 5 until the Link Word equals 0.
7. Re-enable interrupts.

Chapter 7. Registers

Three types of registers control DTI-PC operation: The I/O-mapped Initialization Registers, the Real-Time Control Registers and the Function Registers.

Initialization Registers

The Initialization Registers should be programmed at initialization. These registers are controlled by user I/O functions and must be mapped into the host I/O space.

Thirty-two registers are defined at the selected host I/O address. This I/O address is selected using Switch Banks 1 and 2 (See Chapter Two, Getting Started for more information on I/O addressing.) The first 16 locations are reserved for Channel 1. These register definitions are duplicated in the next 16 locations for Channel 2. All write registers should be set up for both channels for correct dual channel operation.

Register Offset (HEX)	Register Name	Access Method	Channel
0	ID	Read	1
1	Device Type	Read	1
2	Control	Read/Write	1
3	Memory Base	Read/Write	1
5	Interrupt	Read/Write	1
10	ID	Read	2
11	Device Type	Read	2
12	Control	Read/Write	2
13	Memory Base	Read/Write	2
15	Interrupt	Read/Write	2

Table 7-1. Initialization Registers

ID Register 00H, 10H
This Read-only register provides a Manufacturer ID and can be used to verify that the board is based correctly. A Read from I/O address 00H yields a value of 0FB4H if all settings are correct. For a dual channel board, a read from I/O address 10H also yields a vaule of 0FB4H.

Device Type Register 01H, 11H
This Read-only register provides a Device Type and can be used to verify the board is based correctly along with the present version of the board. A read from I/O address 01H yields a value of 0220CH for a dual channel board and a value of 0210H for a single channel board. For a dual channel board, a read from I/O address 11H also yields a value of 0220CH.

Control Register 02H, 12H
A Control Register at I/O offset 02H must be configured before the board becomes operational.

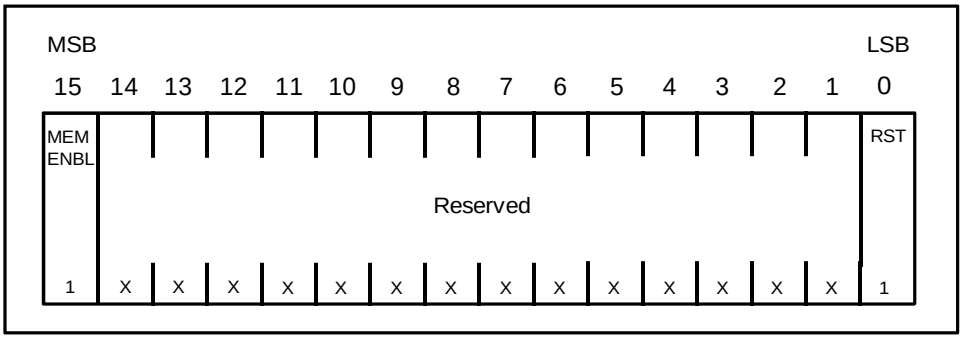


Figure 7-1. Control Register

At powerup, Bit 15 is reset so that the host does not allocate board memory as system memory. This bit must be set to 1 to enable board memory and to allow the board to function properly.

Note: On a dual channel board, each channel contains a bit that controls memory enable. To avoid conflicts with the PC interface, only enable the memory for one channel at any given time, if both channels are set to the same page address.

Writing to the Control Register with a 1 in the least significant position performs a reset of the DTI-PC hardware.

For a dual channel board, the register at offset 12H for the second channel must also be configured.

Memory Base Register 03H, 13H
The Memory Base Register at I/O offset 03H must be set with the address of an available page in memory.

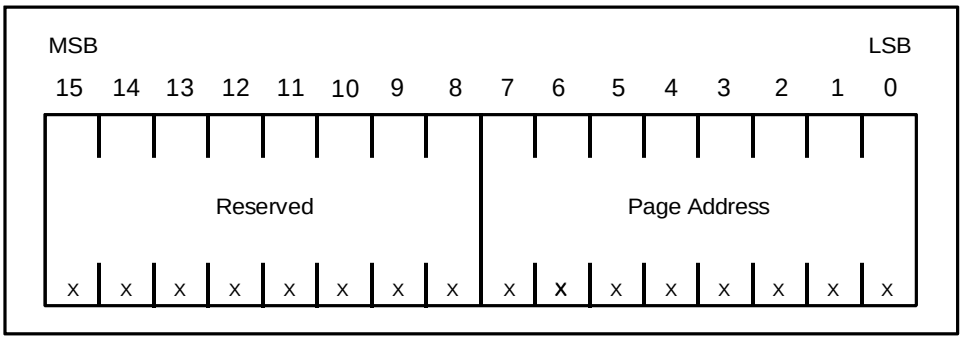


Figure 7-2. Memory Base Register

The Page Address matches the address lines 23-16 on the host bus to identify accesses to the board.

On a dual channel board, the Memory Base Register for each channel must be programmed. To avoid conflict at the PC interface, only one Memory Enable Bit in Registers 02H (Channel 1) and 12H (Channel 2) should be set at any given time, if both channels of a dual channel board are set to the same memory base address.

Interrupt Level Register 05H, 15H
This register sets the interrupt level and also enables interrupts. Use the following formula to set the interrupt level:

Channel 1	Base I/O Address + Register Offset
Channel 2	Base I/O Address + 16D (10H) + Register Offset

Note: Interrupts 3, 5, 10, 11, 12 and 15 are the only valid interrupt levels.

If you select an invalid interrupt level, the next highest interrupt level is automatically selected. For example, if you select Interrupt Level 0110 (Interrupt Level 6), Interrupt Level 10 is automatically selected.

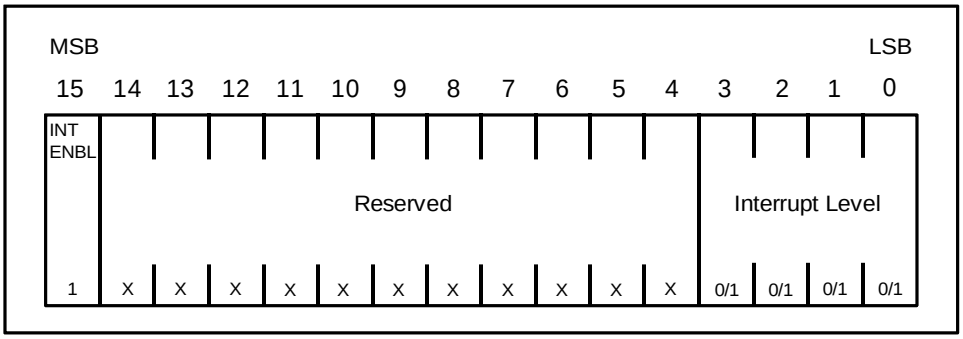


Figure 7-3. Interrupt Level Register

Set Bit 15 to 1 to enable interrupts. Set Bit 15 to 0 to disable interrupts.

The interrupt level is a binary encoded value. For example, set Bits 3-0 to 0101 to select Interrupt Level 5 or to 1100 to select Interrupt Level 12.

For a dual channel board, the register at offset 15H for the second channel must also be configured.

Real-Time Control Registers

The Real-Time Control Registers, located in on-board memory, supply the user with important information, such as operating mode status (Table 7-2). These registers can be accessed at any time (even when traffic exists on the 1553 bus) without degrading the performance of the DTI-PC.

Register Number	Register Name	Access Method
1400H	Alignment	Read
1401H	Board Type	Read
1402H	Firmware Version	Read
1403H	Master Control	Read/Write
1404H	Register Control	Read/Write
1405H	Register Value	Write
1406H	BCMRT Status	Read
1407H	Monitor Status	Read
1408H	Monitor Buffer Control	Read/Write
1409H	Interrupt Queue Control	Read/Write
140AH	ELT HIWD	Read
140BH	ELT LOWD	Read
140CH	RT 0-15 Broadcast Enable	Read/Write
140FH	RT 16-31 Broadcast Enable	Read/Write
1414H	Threshold	Read
1415H	Amplitude State	Read
1416H	Relay State	Read
1417H	ELT State	Read

Table 7-2. Real-Time Control Registers

Alignment Register 1400H
When read, a value of 1553H is returned, indicating that the board has been successfully mapped.

Board Type Register 1401H
When read, a value of 4200H is returned, identifying the board type.

Firmware Version Register 1402H
When read, the current version of the on-board firmware is returned with a value of 0100.

Note: The Master Control, Register Control and the Register Value Registers are used to access the Function Registers. (For more information on how to access the Function Registers, see the Function Registers section of this chapter.)

Master Control Register 1403H
This register acts as a safeguard against any unintentional accesses to the Function Registers. A value of 1553H must be written to this address by the software prior to all register accesses. If the 1553H value has been changed, the user cannot access any of the DTI-PC Function Registers.

Register Control Register 1404H
The Register Control register identifies the Function Register to be accessed and indicates when the access is in progress.

Bit 15 Register Access Pending Bit

Bit 15 indicates if a register access is in progress. The user software loads the register

number into the Register Number Field (Bits 5-0) of this register and writes a 1 to Bit 15. The software polls Bit 15 for a value of 1 or 0. If the value is 1, the DTI-PC examines Bits 5-0 of the Register Control Register and performs the register function loaded by the user. When the register access is completed, the BIU clears the Register Access Pending Bit, allowing another register access to occur.

Bits 14-6 Reserved

Bits 5-0 Register Number Field

Bits 5-0 indicate the function register number to be accessed.

Register Value Register 1405H

This register contains the data value to be written into the register number specified in Bits 5-0 of the Register Control Register 1404H.

BCMRT Status 1406H

A read of this register allows the user to view the DTI-PC operating mode. (Figure 7-4).

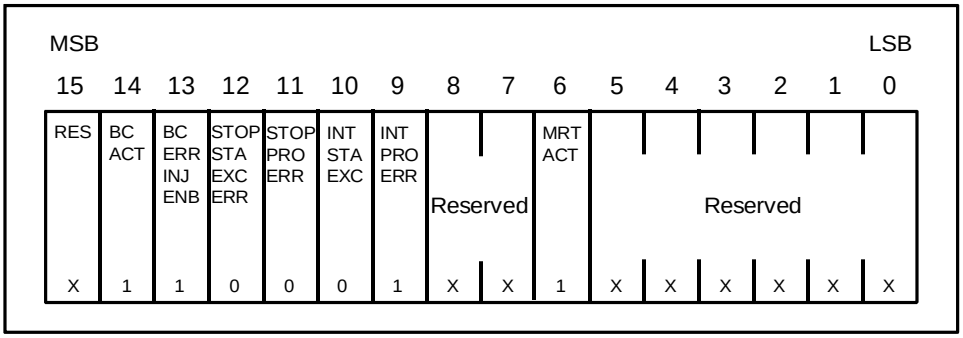


Figure 7-4. BCMRT Status Real-Time Register 1406H

Bit 15 Reserved

Bit 14 BC Active (BC ACT)

If on, the BC is active and executing buslist instructions. Bit 14 is reset by the firmware when the BC executes a Halt instruction or the user WRITEs zeroes to the BC Control Register.

Bit 13 BC Error Injection Enabled (BC ERR INJ ENB)

If on, error injection for the BC is enabled.

Bit 12 Stop On Status Exception Error (STOP STA EXC ERR)

If off, the BC stops if it receives a status response from an RT with any Bits 0-10 set.

Bit 11 Stop On Protocol Error (STOP PRO ERR)

If off, the BC stops if it detects a protocol error.

Bit 10 Interrupt On Status Exception (INT STA EXC)

If on, the BC generates an interrupt when it receives a status response from an RT with any Bits 0-10 set.

Bit 9 Interrupt On Protocol Error (INT PRO ERR)

If 1, the BC generates an interrupt when a protocol error is detected.

Bits 8 & 7 Reserved

Bit 6 MRT Active (MRT ACT)

If set, the MRT mode is activated. Bit 6 reflects accesses to the MRT Control Register and is reset by the firmware when the user WRITEs zeroes to the MRT Control Register.

Bits 5-0 Reserved

Monitor Status Register 1407H
A read of this register returns the Chronological Monitor's operating mode.

Monitor Buffer Control Register 1408H
When read, the starting address of the current monitor buffer is returned.

Interrupt Queue Control Register 1409H
When read, a 0 indicates the interrupt queue is empty. If the microcode writes any other value to the packet, this value represents the address of the first packet to be processed by the software. If a nonzero value is encountered, the software writes a 0 to the register.

ELT HIWD Register 140AH
The ELT HIWD is loaded into this location when a value with Bit 11 set is written to the ELT Control Function Register 17H.

ELT LOWD Register 140BH
The ELT LOWD is loaded into this location when a value with Bit 11 set is written to the ELT Control Function Register 17H.

Broadcast Enable Registers (OCH, OFH)
An RT is notified of broadcast commands if the RT is enabled and the bit corresponding to this RT is set in the appropriate Broadcast Notification Word. Two words of BIU memory, at 140CH (Figure 7-5) and 140FH (Figure 7-6), indicate the RTs to be notified of broadcast messages.

To notify RTs 0, 5, 10, 15, 20, 25 and 30 of broadcast messages, the value of 0x8421 is loaded into BIU address 140CH and 0x4210 is loaded into BIU address 140FH. It is not necessary to set the bit corresponding to RT31.

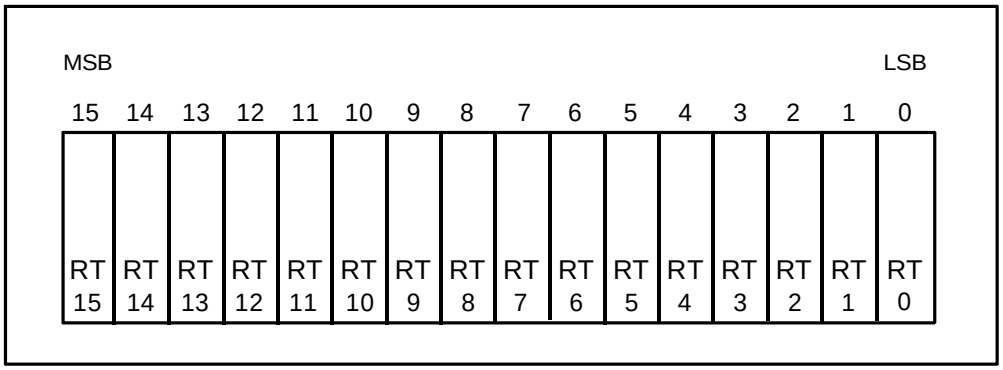


Figure 7-5. RT 0-15 Broadcast Enable Register 0CH

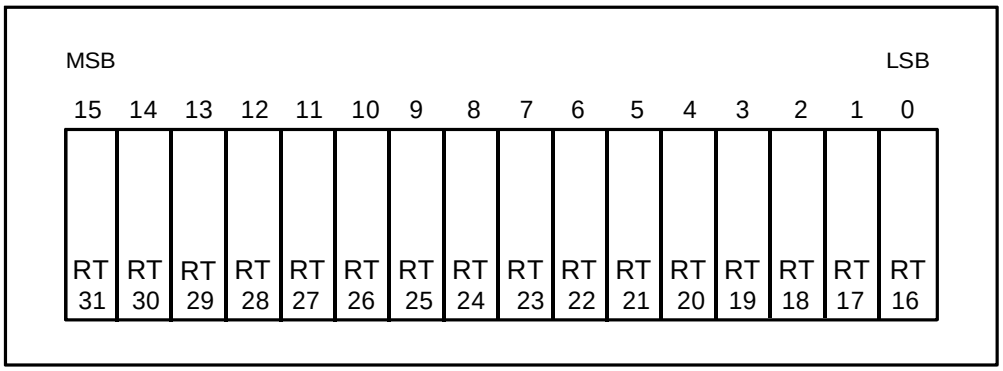


Figure 7-6. RT 16-31 Broadcast Enable Register 0FH

To determine if an enabled RT is participating in the transmitted broadcast message, a Mode Code 2 (Transmit Last Status) or Mode Code 18 (Transmit Last Command) must be transmitted on the 1553 bus. If the specified RT used in the mode code is enabled for broadcast, the Broadcast Message Received (BRC) bit is set in the 1553 status response.

Threshold Register 1414H
Reading this register provides the current variable input threshold setting.

Note: Variable Input Threshold Control is not available on all products.

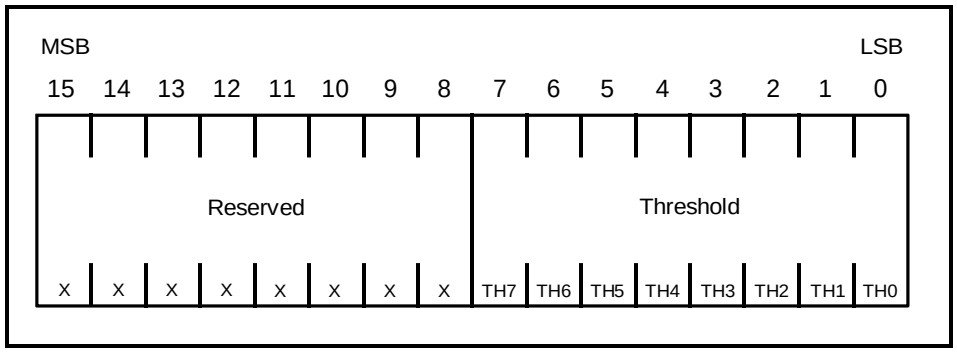


Figure 7-7. Threshold Register

Bits 15-8	Reserved
Bits 7-0	Threshold

Amplitude State Register 1415H
Reading this register provides the current variable amplitude setting.

Note: Variable Input Threshold Control is not available on all products.

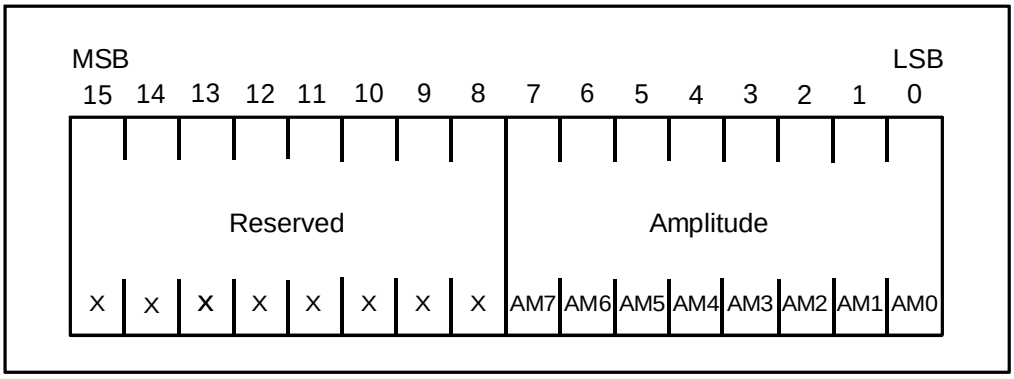


Figure 7-8. Amplitude State Register

Bits 15-8 Reserved

Bits 7-0 Amplitude

Relay State Register 1416H
This register contains the current value written to the Relay Function Register, which determines bus selection, external bus connection and termination options.

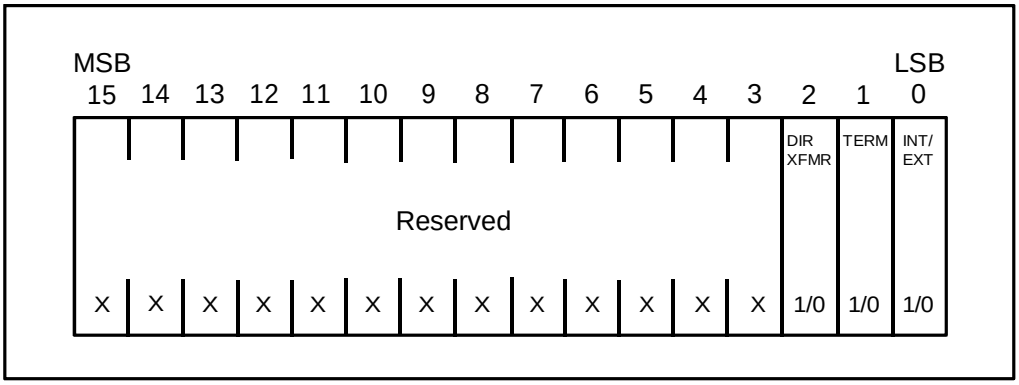


Figure 7-9. Relay State Register

Bits 15-3 Reserved

Bit 2 Direct/Transformer Coupling. Set to 1 for Direct Coupling, 0 for Transformer Coupling.

Bit 1 Termination Option. Set to 1 for Internal Termination, reset to 0 for External Termination.

Bit 0 Internal/External Bus Connection. Set to 1 for Internal Bus Connection, reset to 0 for External Bus Connection.

ELT State Register 1417H

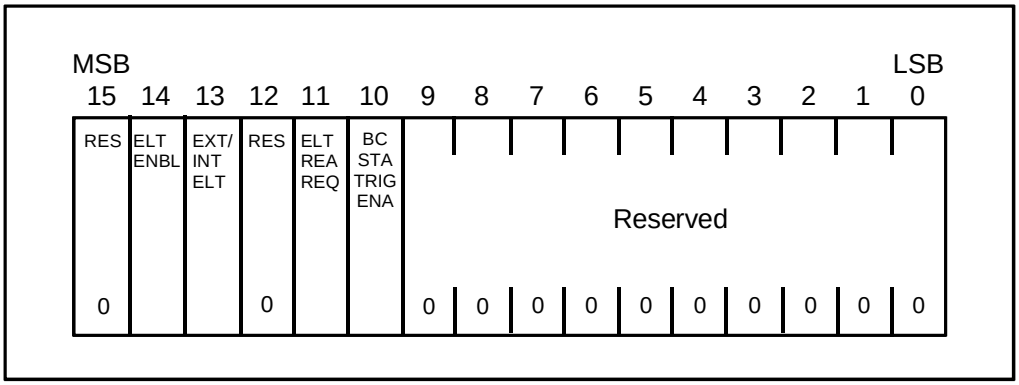


Figure 7-10. ELT State Register

Bit 15 Reserved

Bit 14 If 1, ELT is enabled. If 0, ELT is disabled.

Bit 13 If 1, external ELT is selected. If 0, internal ELT is selected.

Bit 12 If 0, reset the ELT. If 1, do not set the ELT.

Bit 11 If 1, ELT read has been requested. If 0, ELT read has not been requested.

Bits 10-0 Reserved

Function Registers

The Function registers control certain board functions, such as buslist execution. Accessing the Function Registers is controlled via the Real-Time Control Registers 1403H through 1405H. The DTI-PC firmware accesses these registers when no traffic exists on the bus.

Note: None of the Function Registers are readable. All read accesses are performed via the Real-Time Control Registers.

Register Number	Register Name	Access Method
10	BC Control	Write
11	MRT Control	Write
12	Fail-safe Timer	Write
13	Gap Counter Control	Write
14	BC Error Control	
15	AND	Write
16	OR	Write
17	Elapsed Timer Control	Write
18	Chronological Monitor Control	Write
19	Amplitude	Write
1A	Relay	Write
1B	Threshold	Write
1C	Reset	Write
1D	Memory Address	Write

Table 7-3. Function Registers

BC Control Register 10H
The Write-Only BC Control Register controls three functions. This register starts the execution of the buslist and continues the buslist instructions after a halt. Register 10 also halts execution of the buslist after completion of the current instruction.

Start
Load the address of the first buslist instruction to be executed. The offset cannot be less than 1440H, if the RTs are emulated.

Halt
To halt the buslist, WRITE 0. The Halt instruction does not change the BC's instruction pointer. The BC completes the current instruction, halts and generates an asynchronous halt interrupt.

Continue
To continue the buslist, WRITE FFFFH. The BC starts after the last exectued instruction. The Continue Instruction restarts the BC after asynchronous errors, exceptions or a Halt BC. When evident that another buslist instruction will immediately follow the Halt instruction, the Continue instruction restarts the BC.

Follow the steps below to write to the Function Registers:

1. If the Master Control Register 1403H contains the value 1553H and Bit 15 of the Register Control 1404H is set, wait for Bit 15 of the Register Control Register to be reset.
2. Write the value 1553H to the Master Control Register.
3. Write the value to be loaded into the desired Function Register into the Register Value Register

1405H.
4. Write the desired Function Register number into Bits 5-0 and set Bit 15 of the Register Control Register.
5. When Bit 15 of the Register Control Register is reset, the operation is completed.

MRT Control Register 11H

The Write-Only MRT Control Register enables or disables the emulation of RTs for the MRT structures set up in memory.

Note: Initial MRT structures must be in place before the MRT is started.

After the MRT is started, RTs can be enabled or disabled by setting or clearing Bit 15 of the RT Status Block Control Word for the desired RT.

Start MRT
To start the MRT, WRITE a 1.

Halt MRT
To halt the MRT, WRITE a 0.

Fail-safe Timer Register 12H
The Write-Only Failsafe Register resets the Fail-safe Timer and enables both transmitters.

To reset the Fail-safe Timer, WRITE any hexadecimal value (0-FFFF). A hardware or software reset also resets the Fail-safe Timer and enables both transmitters. Reset the Fail-safe Timer for any interruption of the board's transmit capacity.

When a Transmitter Shutdown Interrupt occurs (that is, Bit 5 of the Trailer Word in the Interrupt Packet is set), the Fail-safe Timer Register can be written to re-enable transmitters.

Note: A word count high error greater than 32 words indicates a transmitter hardware failure. Register 12 should not be written to.

Gap Counter Control Register 13H
To use the Gap Counter Control Register:

- Determine the length of time the BC allows for the RT to respond.
- Subtract this value from 256.
- Load the new value into the Gap Counter Control Register.

Example
To set the BC time-out to 18 microseconds, multiply 18 by 10 (to convert 18 to tenths of microseconds) and subtract the result from 256:

256 - 180 = 76

Write this value (76) into the Gap Register.

Note: Since the time-out value is subtracted from 256, the maximum time-out is 25.6 microseconds.

BC Error Control Register 14H
The Write-Only BC Error Control Register modifies BC error control. The BC may be set up to halt or interrupt when a status exception or protocol error occurs. Register 14 also enables/disables all error

control for the BC (Figure 7-10). Set Bit 2 of Register 14 to activate error injection in each buslist instruction.

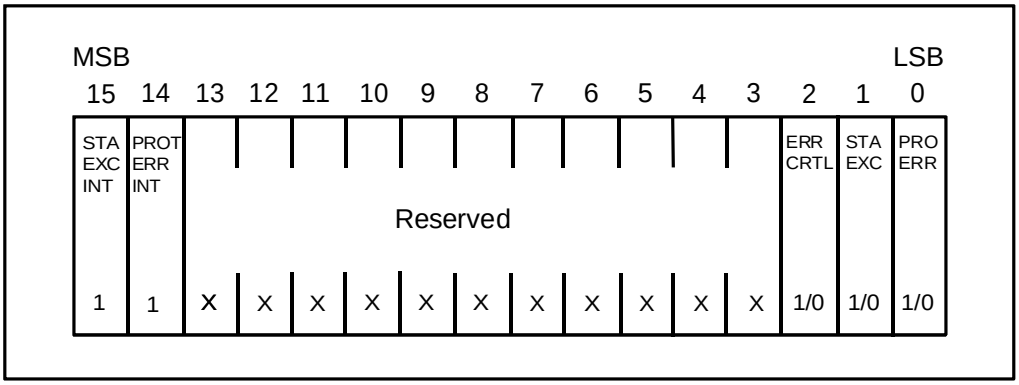


Figure 7-11. BC Error Control Register

Bit 15 Status Exception Interrupt (STA EXC INT)

If Bit 15 is set, an interrupt is posted when the BC encounters a Status Exception.

Bit 14 Protocol Error Interrupt (PRO ERR INT)

If Bit 14 is set, an interrupt is posted when the BC encounters a protocol error.

Bits 13-3 Reserved

Bit 2 Error Control (ERR CRTL)

If Bit 2 is set to 1, the error control information in individual buslist instructions is used on transmission. If Bit 2 is clear, BC error injection capabilities are disabled.

Bit 1 Status Exception (STA EXC)

If Bit 1 is set, the BC continues after a status exception is encountered. If Bit 1 is cleared, the BC halts after a status exception is encountered.

Bit 0 Protocol Error (PRO ERR)

If Bit 0 is set, the BC continues after a protocol error. If Bit 0 is clear, the BC halts after a protocol error occurs.

AND Register 15H
As a WRITE-only register, Register 15H works together with the Memory Address Register 1DH to AND the value in Register 15 with the value pointed to by the memory address contained in Register 1DH. Values are written to the AND register to perform the AND operation. The DTI-PC modifies the Memory content when the AND value is written.

Example
Masking out the upper byte of a value using the AND Register 15H, AAAA ANDed with 00FF results in 00AA.

Address	Data	Operation
Memory 0528H	AAAAH	Load a value of AAAH into address 0528H.
Memory Address Register 1DH	0528H	Load 0528H into Memory Address Register 1DH.
AND Register 15H	00FFH	WRITE 00FFH to the AND register 15H.
Memory 0528H	00AAH	READ back new data value.

Note: The AND/OR Registers provide compatibility with previous BIU products and are not used in most cases, since memory access via these registers takes five to ten times longer than a direct access to memory.

OR Register 16H
The OR Register works together with the Memory Address Register 1DH to OR the value in Register 16H with the value pointed to by the memory address contained in Register 1DH. Memory content is modified after the OR value is written to this register.

Example
To set the upper byte of the value using the Register 16H, 00AAH ORed with 5555 results in 55FFH.

Address	Data	Operation
Memory 1359H	00AAH	Load a value of 00AAH to Memory Location 1359H.
Memory Address Register 1DH	1359H	Load 1359 to Memory Addres Register 1DH.
OR Register 16H	5555H	Write 5555H to OR Register 16H.
Memory 1359H	555FFH	Read back new data value.

Note: The AND/OR Registers provide compatibility with previous BIU products and are not used

in most cases, since memory access via these registers takes five to ten times longer than a direct access to memory.

Elapsed Timer (ELT) Control Register 17H

The WRITE-only ELT Control Register controls the 32-bit Elapsed Timer (Figure 7-11, Table 7-4). The ELT Control Register selects the source for the Elapsed Timer clock, internal 1 Mhz or external RS-422 signal. A WRITE to Register 17 enables/disables the ELT, selects the external signal or internal clock source, resets the ELT and reads the ELT. (See the Real-Time Control Registers 140AH and 140BH). The ELT contains a resolution of 1 microsecond. The ELTCLK is user-defined.

WRITE Value	Action
0H	Halt and Reset the ELT
1000H	Halt the ELT
1800H	Read the ELT
4000H	Enable and Reset the ELT
5000H	Enable the ELT

Table 7-4. Register 17 Values and Actions

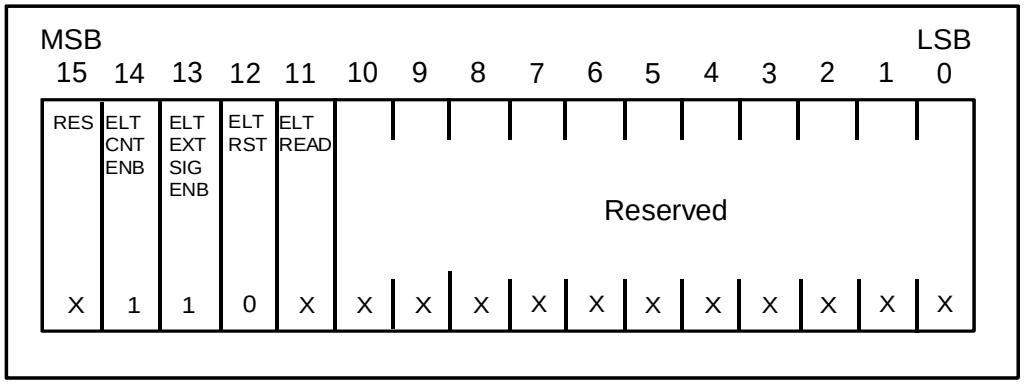


Figure 7-12. Elapsed Timer (ELT) Control Register

Bit 15 Reserved

Bit 14 Elapsed Timer Count Enable (ELT CNT ENB)

When cleared, Bit 14 stops the Elapsed Timer. Clearing Bit 14 resumes ELT operation, using the current ELT value as the starting value.

Bit 13 ELT External Signal Enable (ELT EXT SIG ENB)

Setting Bit 13 enables the external signal for the Elapsed Timer Clock. Clearing Bit 13 selects the internal 1 MHz clock.

Bit 12 Reset Elapsed Timer (RST ELT)

When reset to 0, Bit 12 resets the Elapsed Timer. Bit 12 must be set if the user is writing to this register and doesn't wish to reset the ELT.

Bit 11 ELT Write Control (ELT READ)

When set to 1, the ELT LOWD and ELT HIWD Real-Time Control Registers are loaded with

the current ELT value.

Bits 10-0 Reserved

Chronological Monitor Control Register 18H

The Chronological Monitor Control Register starts and stops the monitor. The monitor is started by writing a value of 8 to this register.

Note: Before the monitor can be started, the address of the first monitor buffer must be loaded into the Real-Time Register at 1408H.

The monitor is stopped by writing a value of 0 to this register. Writing a value of 18H allows the monitor to record 1553 command words that may contain protocol errors and permits the capture of all bus traffic. If Bit 4 is not set, only messages with valid commands can be monitored.

Amplitude Register 19H

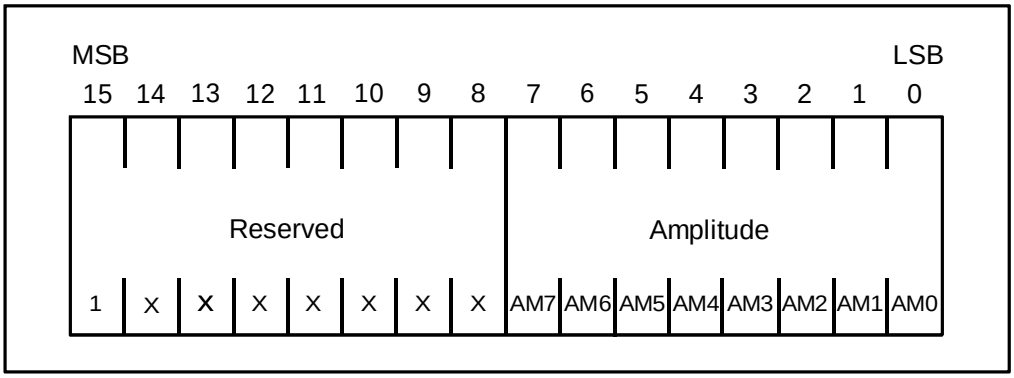


Figure 7-13. Amplitude Register

Bits 15-8 Reserved

Bits 7-0 Amplitude

Vary the waveform amplitude by writing an eight-bit hexadecimal value (0-FF) to Register 19. Set to FFH by configuration data at powerup.

Note: Accessing this register affects only those boards supporting this feature.

Relay Register 1AH

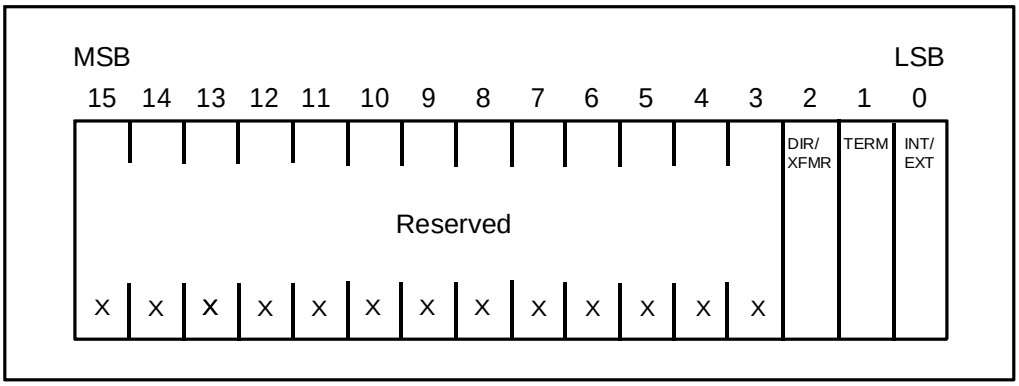


Figure 7-14. Relay Register

Bits 15-3 Reserved

Bit 2 Direct/Transformer Coupling. Set bit to 0 for transformer coupling. Set to Bit 1 for direct coupling. Set Bit 1 according to the coupling requirement.

Bit 1 Termination Option. Set bit to 0 for external termination. Set bit to 1 for internal termination.

Bit 0 Internal/External Bus Connection

Set bit to 0 for external bus connection. Set bit to 1 for internal bus connection.

Note: SYSTRAN recommends that the Bit 2= 0, Bit 0 = 0 options be avoided. If an internal bus connection is selected, it should be internally terminated (Bit 2 = 1, Bit 0 = 0).

Threshold Register 1BH

Bits 15-8 Reserved

Bits 7-0 Threshold

Vary the input threshold voltage by writing an eight-bit hexadecimal value (0-FF) to Register 1B. Set to FFH by configuration data at powerup. A value of 0 sets the threshold at 0 volts; value of FFH sets the threshold at approximately 3 volts.

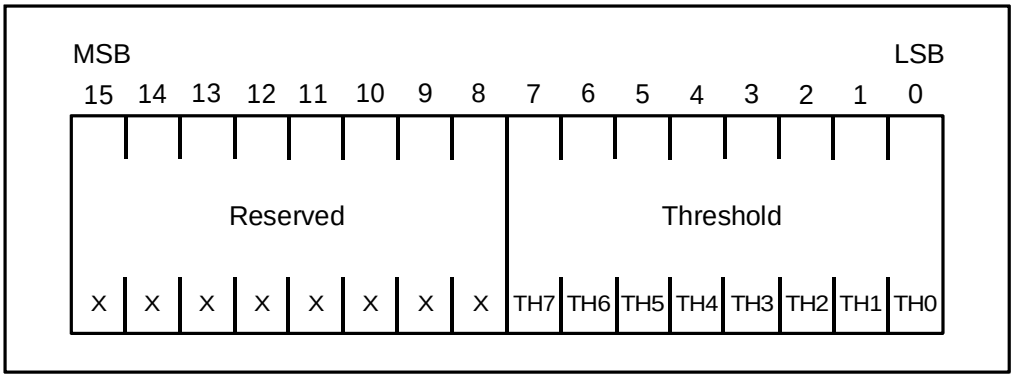


Figure 7-15. Threshold Register

Note: Accessing this register affects only those boards supporting this feature.

Reset Register 1CH
The Reset Register resets the DTI-PC, affecting any data structures set up in memory.

Resetting the DTI-PC:

- Halts BC, RT and CM operations
- Resets BC Error Control Register bits to their default values:
  - Stop on Protocol Error
  - Stop on Status Exception
  - Do not interrupt on Protocol Error
  - Do not interrupt on Status Exception
  - Disable BC error injection
- Resets the Terminal Fail-safe Timer
- Ignores the remainder of a message in progress on the 1553 data bus
- Turns off any pending interrupts
- Resets the interrupt queue to 1200H

To perform a RESET, WRITE any hexadecimal value (0-FFFF).

Memory Address Register 1DH
Use Register 1DH to address memory and, in conjunction with the AND or the OR Register, to set or reset bits. The Memory Address Register contains the value of the address to be modified. Perform a WRITE to Register 1DH first. Then perform the appropriate "AND" or "OR" function.

AND

Example
Masking out the upper byte of a value using the AND Register 15H, AAAA ANDed with 00FF results in 00AA.

Address	Data	Operation
Memory 0528H	AAAAH	Load a value of AAAH into address 0528H.
Memory Address Register 1DH	0528H	Load 0528H into Memory Address Register 1DH.
AND Register 15H	00FFH	WRITE 00FFH to the AND register 15H.
Memory 0528H	00AAH	READ back new data value.

OR
To operate the OR Register:

- Enter the address of the memory location being modified to the Memory Address Register (identical with Step 1 of AND).
- Load the OR Register 16H with the value to be OR'd.

Example
To set the upper byte of the value using the OR Register 16H, 00AAH OR'd with 5555 results in 55FFH.

Address	Data	Operation
Memory 1359H	00AAH	Load a value of 00AAH into address 1359H.
Memory Address Register 1DH	1359H	Load 1359 into Memory Address Register 1DH.
OR Register 16H	5555H	WRITE 5555 to the OR register 16H.
Memory 1359H	55FFH	READ back new data value.

Note: The AND/OR Registers provide compatibility with the BIU Express and are not used in most cases because memory access via this register takes five to ten times as long as a direct access to memory.

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