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DTI-PC/S

User Manual

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FOREWORD

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Systran Corporation
4126 Linden Avenue
Dayton, Ohio 45432 USA
(800) 252-5601 (U.S. only)
(937) 252-5601
Fax: (937) 258-2729

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CE

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Overview

The DTI-PC/S is an intelligent interface between a PC ISA bus host and a MIL-STD 1553B data bus. Designed for high performance environments with multiple host applications, the DTI-PC/S enables the PC host to operate in real time as a MIL-STD 1553B Bus Controller (BC), Remote Terminal (RT) or Bus Monitor (BM).

The PC host processor and DTI-PC/S communicate via a flexible, programmable interrupt structure, internal registers, and a definable dual-port RAM. A wide range of software programmable registers deliver the features and capabilities that provide flexibility and ease of use for complete MIL-STD 1553B system control, emulation, analysis and data reporting.

The DTI-PC/S is available in both single and dual channel configurations. The dual channel option allows a second independent MIL-STD 1553B channel interface on one board.

Enhanced Intelligence

The high performance architecture of the DTI-PC/S allows distributed processing solutions: BC-to-RT, RT-to-BC and RT-to-RT instructions, mode code, broadcast mode and broadcast. For applications requiring a high degree of host processing, the following functions may be incorporated without host intervention:

- Interrupt Lists
- Multiple Message Processing
- Automatic Polling
- Variable Memory Space Allocation
- Selectable Data Storage
- Indexing

This architecture is also effective when more than one DTI-PC/S is controlled by the same PC host. Environments requiring multiple boards under single-host control include:

- Interfaces to multiple MIL-STD 1553B data buses.

- Emulation of multiple data buses.

Highly Flexible Configuration

To meet a wide range of systems requirements, the DTI-PC/S allows the user to define the size of the dual-port RAM (16K or 32K words) and the starting address of the memory block.

The unique interface features provide the flexibility for changing system load requirements and also provide the options for effective deployment of more than one DTI-PC/S within the same PC host.

Enhanced Bus Connection Capability

Internal and external termination, transformer or direct coupling, and connected or isolated buses are supported by the DTI-PC/S. Bus connection is enabled via a software-accessible control register (Bus Connection Relay Control Register).

DTI-PC/S Onboard Dual-Port RAM

The DTI-PC/S provides up to 32K words of dual-port RAM for maximum processing throughput. The highly flexible RAM area allows you to alter the size of the RAM to enhance data handling, alter the configuration to meet specific requirements and change the starting location of the dual-port RAM to provide more effective application compatibility. These options are enabled via Configuration Registers 26 and 27 (See Getting Started for details).

The dual-port RAM is accessible directly from the PC ISA bus or from the DTI-PC/S. All accesses to the dual-port RAM must be in 16-bit word transfers.

Remote Terminal Mode

The RT mode provides the capability of emulating an RT, with up to 31 data subaddresses and one or two mode subaddresses. (Subaddress 31 is selectable.) The DTI-PC/S responds to bus instructions in real-time, easily handling the traffic of a 100 percent loaded bus.

Using the onboard dual-port RAM, the DTI-PC/S receives, stores, time tags and counts up to 1,000 32-data word transfers. Bus messages are transmitted and received without host intervention. As each valid bus message is received, an RT index counts the number of storage buffers. If the buffers for a particular subaddress are full, only the last message buffer is overwritten.

Other RT features include:

- Generating an interrupt when addressed
- Providing a 64 microsecond resolution time tag for each stored message
- Detecting message errors
- Enabling specific subaddress/mode codes

Bus Controller Mode

The BC mode provides the capability of defining, storing and implementing multiple lists of bus instructions. Controlled by the application, DTI's inter-message timing allows the BC to emulate the instruction set and bus command timing without host intervention. The instructions allow the specification of an inter-message timer to delay the implementation of the subsequent instructions.

The DTI-PC/S addresses up to 32 RTs, with up to 32 subaddresses each. Each Command Block instruction, size of the instruction and method of implementation is definable.

The DTI-PC/S BC is also capable of:

- Monitoring data during RT-to-RT transfers.
- Controlling the bus retry option;, which allows the BC to re-send bus instructions on the same or opposite bus up to four times.
- Polling RT status.
- Setting the inter-message timer.
- Initiating mode broadcast or broadcast mode commands.
- Detecting protocol and bus errors;
- Implementing RT 31 as a broadcast RT or a normal RT.

Bus Monitor Mode

The BM mode monitors one, any combination or up to 32 RTs. Software programmable registers determine the number and address of the RT to monitor. (See the Registers section of this manual.) Using the registers and command structures, the DTI-PC/S processes a series of monitored messages without host intervention. The BM also detects response time out, long and short word count, bit count, Manchester II and parity errors.

Interrupt Handling

The DTI-PC/S defines MIL-STD 1553B events as a high priority interrupt, standard priority interrupt or no interrupt. High priority interrupts are recorded in registers and are typically handled upon occurrence. (See the Registers section of this manual.)

Standard priority interrupts are queued and handled via application requirements. The host can periodically or continuously monitor the number of standard priority interrupts queued.

The standard priority interrupt queue is initialized by the host and consists of a first-in/first-out queue of enabled interrupt events. The standard priority interrupt queue holds up to 255 packets (or entries) in contiguous or non-contiguous memory. (See the Interrupts section of this manual.)

Theory of Operation

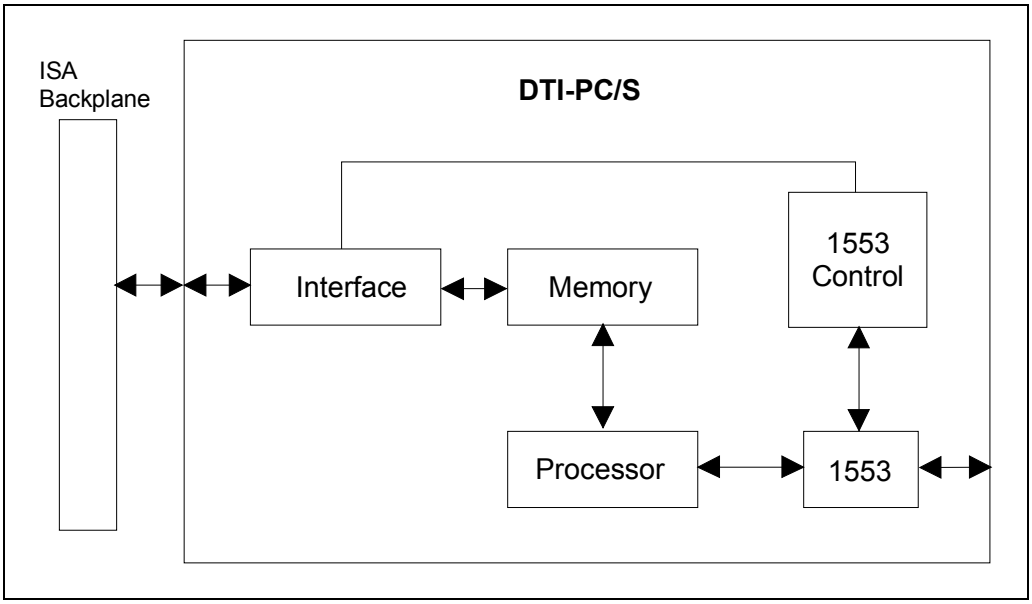


Figure 1-1. DTI-PC/S Theory of Operation

The DTI-PC/S interface mechanism is responsible for two key functions of DTI-PC/S board operation. The interface orders the access to the onboard dual-port RAM by implementing the PC ISA interface logic and is responsible for arbitration of memory between the onboard processor and the PC host. The interface also allows the PC host to program the Operational Registers on the processor and also contains the Configuration Registers.

The onboard processor provides the interface to the MIL-STD-1553 bus by emulating a BC, RT or BM. This processor also contains the Operational Registers.

The 1553 logic contains the transceiver, transformers and relays. The relays isolate or connect the 1553 bus, select transformer or direct coupled connection to the bus or terminates the bus.

Specifications

Table 1-1 provides a list of specifications for the DTI-PC/S.

Specifications	
Memory:	32K words of dual-port RAM
Word size:	16 bits
Communication:	MIL-STD-1553B protocol dual redundant bus
Interface to bus:	Transformer or direct coupling
Voltage:	+ 5.0V +/- 5%, +12.0V + 5%, -12.0V + 5%
Current Drain:	2.3 amperes (maximum - single channel) 3.3 amperes (maximum - dual channel)
Temperature range: Operating: Storage:	 0 to 70 degrees Celsius -55 to 125 degrees Celsius
Relative humidity:	10% to 90%, non-condensing
Processor clock speed:	12 megahertz (MHz)
DTI-PC/S board size:	13.1 in. x 4.2 in. 332.7 mm by 106.68 mm

Table 1-1. DTI-PC/S Specifications

Quality Assurance

Each DTI-PC/S is designed, developed, and manufactured by Systran. to military standards as well as Systran's high standards of quality. Sophisticated manufacturing processes ensure that each DTI-PC/S is comprehensively tested before shipment. Systran manages a fully-staffed customer service department available to answer your questions and training requirements.

For **Customer Service**, call Systran at:

(800) 252-5601 (U.S. only)
or (937) 252-5601
8:00 a.m. to 5:00 p.m. ES/DT

or fax :
(937) 258-1349

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Getting Started

Step 1. Unpacking and Examining The Board

Remove the hardware board from the packing box (Figure 2-1).

Note: The board is shipped in a protective anti-static bag. Do not remove the board from the protective bag until grounded.

Once grounded, remove the board from the protective bag and place the board on the bag or any electrostatically-controlled surface.

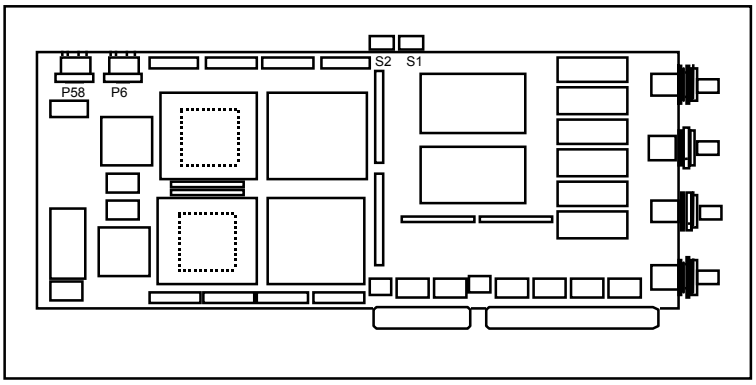


Figure 2-1. DTI-PC/S Board

If the board appears to be damaged, contact Systran immediately.

Step 2. Selecting The I/O Base Address

Use Switches S1 and S2, located on the top of the board, to select the I/O base address. S1 represents the most significant digit. For example, if S1 = 1, S2 = 0, the I/O base address is 100H (Figure 2-2).

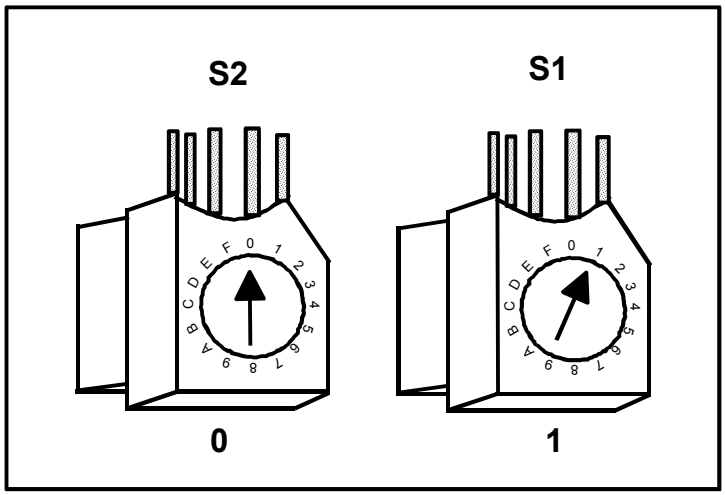


Figure 2-2. Example I/O Address Switch Settings

Step 3. Installing The Board

Caution: Install the DTI-PC/S with power off.

1. Locate an available slot in the host computer.
2. Seat the DTI-PC/S in the selected slot and push down firmly on the board.
3. Secure the front panel plate with a screw.

Step 4. Interconnection to DTI-PC/S Boards or RTs

External ports, located on the top of the DTI-PC/S board, each contain a four-pin, male-type MTA miniature connector P6, P5B (Figure 2-1). This connector provides the options of:

- Connecting multiple DTI-PC/Ss within one PC host.
- Connecting the DTI-PC/S to an RT (for interaction between an RT and the DTI-PC/S).

Viewing the component side of the board with the connector down, Pin One is the left most pin.

The TTL level signals for the external port follow:

Pin 1 Command Strobe (Output)

The DTI-PC/S activates Pin 1 after receiving a valid 1553B command and deactivates the pin after servicing the command.

Pin 2 Subsystem Fail (Input)

When Pin 2 is set, it causes the Subsystem Fail Bit in Register 01 to be set. An interrupt can then be enabled, notifying the host. Pin 2 detects a test hardware failure, such as a failure of the 1553B test equipment.

Pin 3 External Override (Input)

Pin 3 is used for Input from the RT command strobe. Pin 3 can also be used for multi-redundant applications. Upon receiving the Pin 3 signal, all current activity is aborted. The pin may be connected to the RT command strobe Output of an adjacent DTI-PC/S when used.

Pin 4 Ground

Pin 4 can be used for grounding connections.

Step 5. Setting The Configuration Registers

The operational programmable registers replace hardware programmable switches and jumpers. The I/O base address is the only hardware-programmable option the user must select. (See Step 3.)

The bits in the programmable registers are set to their default values when the system is powered up or a system hardware reset is performed. The software reset performed by reading Register 18 does not affect the register settings. Existing configurations are maintained when a software reset is performed.

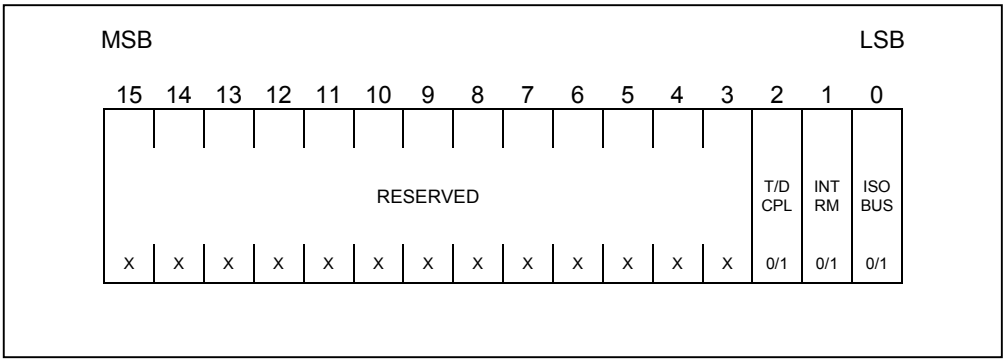
The configuration registers must be programmed to meet the user system requirements before the DTI-PC/S is operational. The operation of these registers is described in the following sections. This information, combined with the definitions in the Registers section, provide the information required to write low-level software drivers for a PC host computer.

The register numbers are decimal and are relative to the base register address of the board. For the optional dual channel board, the register set of the second channel is offset by 64 (40H) from the base register address of the first channel. The base register address of the first channel is selected by setting switches S1 and S2. (See Step 3.)

Note: For a dual channel board, the configuration registers for both channels must be programmed to operate correctly. Programming only the configuration registers of one channel on a dual channel board may cause unpredictable results.

Register 25: Bus Connection Relay Control

Three bits in this register control relays that isolate the DTI-PC/S from the 1553 bus for self-test, connect an internal termination resistor to the DTI-PC/S and select a direct or transformer coupled connection to the bus. These selections are typically configured once for a particular test setup. An additional bit in this register allows the machine controlling the bit test pattern to output data continuously for diagnostic purposes.



Bits 15-3 Reserved.

Bit 2 T/D CPL - Transformer/Direct Coupling.
This relay can connect the DTI-PC/S to the 1553 bus in a direct or transformer coupled configuration. Use direct coupling if the distance between the DTI-PC/S and the 1553 bus measures 12 inches or less. Use transformer coupling if the distance between the DTI-PC/S and the 1553 bus exceeds 12 inches, but not 20 feet. Direct coupling is applied during the isolated internal self-test at powerup. After the self-test concludes, the bit is set according to UUT connection requirements. The selected connection applies to Buses A and B.

0 = Transformer coupling selected.
1 = Direct coupling selected.
Default = 1.

Bit 1 INTRM - Internal Termination.
This relay connects a termination resistor, required when using the direct coupling. The resistor is applied during the isolated internal self-test at powerup to provide a test load. After the self-test concludes, the bit is set per UUT connection requirements. The selected connection applies to Buses A and B.

0 = No termination connected.
1 = Internal termination connected.
Default = 1.

Bit 0 **ISOBUS - Isolate Bus.**
This relay can isolate the DTI-PC/S from the 1553 bus. To isolate the DTI-PC/S from the 1553 bus, set the bit to 1 (the default value). When the bit is set to 0, the DTI-PC/S is connected to the 1553 bus. This relay is typically used only for powerup self-test of the DTI-PC/S board and doesn't require disconnecting the board from any UUT. After a successful powerup self-test, the bit is usually set to 0. The selected connection applies to both Buses A and B.

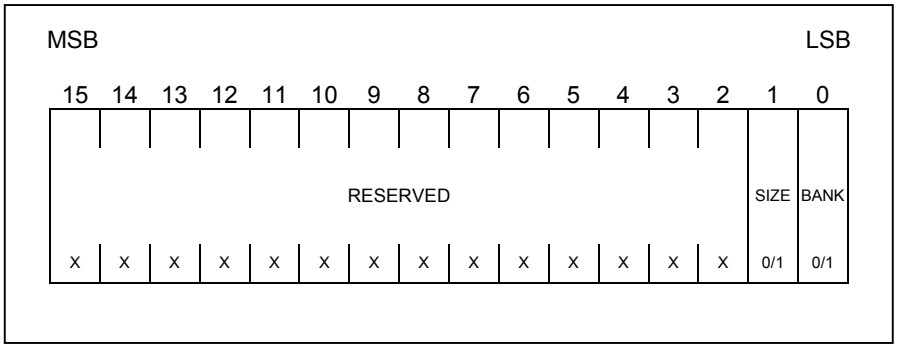
0 = Connected to 1553 bus.
1 = Isolated from 1553 bus.
1 = Default.

Note: For the DTI-PC/S to operate on a 1553 bus, this value must be changed to 0.

Register 26: Memory Size/Bank Select

The least significant two bits of this register are used to select the dual-port RAM size, and select the bank of onboard RAM to be used for dual-port operation. The DTI-PC/S can address 32K words of memory; therefore, this is the maximum size of space that can be allotted in the PC memory address space. However, the user has the option of selecting smaller dual-port memory sizes. By selecting a 16K word size and different banks, you can configure two channels to share one memory page.

Note: All accesses to the operational registers, the configuration registers or the dual-port RAM from the PC host must be word transfers. Byte transfers cause unpredictable results.



Register 27 is used to select the base memory address on 64 KB module boundaries. The dual-port RAM size and Bank Select Bits of Register 26 are used to select decoding locations for smaller increments of memory within the 64 KB space. Selecting other address locations for smaller increments of memory is useful when several boards are mapped into a limited address space. The default selection is 64 KB (32K words) of RAM starting at the base address.

Bits 15-2 Reserved.

Bit 1 RAM Size Select.
This bit selects the amount of RAM appearing in the PC address space. The amount of RAM selected is shared in dual-ported fashion with the DTI-PC/S.

0 = 16 K words; 32 KB
1 = 32 K words; 64 KB
Default = 1.

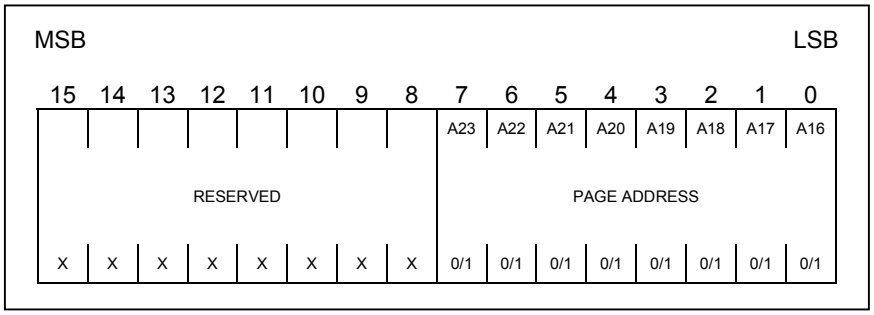
Bit 0 Bank Select.
This bit selects the upper or lower half of the selected page via Register 27. To enable, set Bit 1 to 0, which selects 32 KB of dual-port RAM.

0 = Lower half of page (0-7FFF)
1 = Upper half of page (8000-FFFF)
Default = 0

Note: This bit is meaningless if a 64KB RAM size is selected.

Register 27: Base Memory Address Select

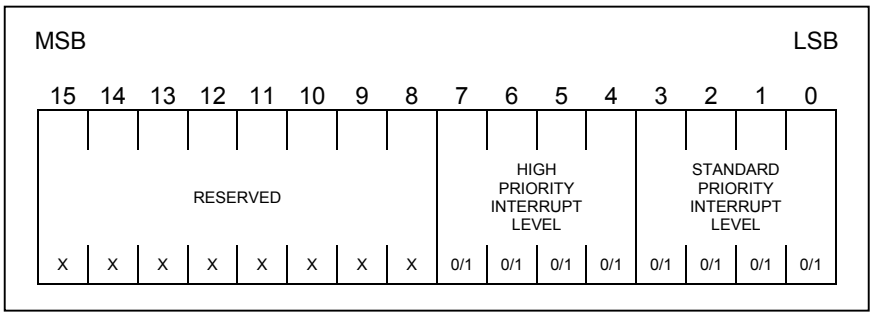
This register sets the base starting address for the amount of dual-ported RAM selected in Register 26. The bits of Register 26 can be used to offset the RAM address within the 64 KB space selected by this register.



The page address matches the address line A23-A16 on the host bus to identify accesses to the board. On systems with multiple channels, the memory space for each channel must not overlap.

Register 29: Interrupt Level and Vector Width Selection

Eight bits in this register are used to select the standard priority interrupt level and the high priority interrupt level.



Bits 15-8 Reserved.

Bits 7-4 High Priority Interrupt Level.
These three bits are used to select the high priority interrupt level. Valid levels are 3, 5, 10, 11, 12 and 15. Programming an invalid level results in selecting the next highest level. For example, selecting Interrupt Level 7 (0111) allows the high priority interrupts to occur on Level 10 (1010).

Bits 3-0 Standard Priority Interrupt Level.
These three bits are used to select the standard priority interrupt level. Valid levels are 3, 5, 10, 11 12 and 15. Programming an invalid level results in selecting the next highest level. For example, selecting Interrupt Level 13 (1101) allows standard priority interrupts to occur on Level 15 (1111).

Step 6. Basic Commands For The BC, RT and BM

BC Operational Sequence with Interrupts

1. Set up the first Command Block instruction block for a four-word RT-to-BC transfer (Control Word, Command Word 1) and initialize Register 2 with the onboard RAM address of the beginning of the block.

2. Enable the auto-retry on the opposite bus using only one retry attempt, if the incoming message is received with a message error. (Control Register 00 = 0C90H; Bus A enabled).

3. Set the End Of List Bit in the control word (2C00H), Interrupt And Continue Bit, and the Auto Retry Enable Bit.

4. Set up the data list pointer to store all data words in the preferred area of memory.

5. Configure the standard interrupt queue in the preferred area of memory and initialize Register 5 with the onboard RAM address of the beginning of the queue.

6. Enable the Standard Interrupt Bit and the End Of List Bit in the High Priority Interrupt Enable Register. Enable the Command Block Interrupt Bit in the Standard Interrupt Enable Register.

7. Set the Start Enable Bit in the Control Register (Register 00).

8. Message implementation now begins by transmitting the transmit command stored in the Command Block. The DTI-PC/S waits to receive the status word book from the transmitting RT.

9. The status word is received and stored in Command Block 1. The incoming data words from the transmitting RT follow and the DTI-PC/S stores them in memory as pointed to by the data list pointer.

10. The DTI-PC/S, having encountered the End Of List Bit being set, halts message transactions and waits for another start signal.

11. The DTI-PC/S asserts a high priority interrupt indicating the end of the Command Block Buslist. The DTI-PC/S also asserts a standard interrupt due to the command block bit being enabled in the Standard Interrupt Enable Register and logs the event in the interrupt queue.

RT Operational Sequence with Interrupts

The DTI-PC/S receives a command to receive 32 data words to Subaddress 2 (BC-to-RT).

1. The RT response block for Subaddress 2 is set up with an index of 1 in the preferred area of memory. The onboard RAM address of the RT response block for the receive subaddress is stored in Register 02.

2. The data list pointer of the RT response block is set up to store all data words in memory beginning at the indicated address. It is updated at the end of each successful message with the starting address of the next message when the index field ≠ 0.

3. The message status pointer is set up to store all message status list information in memory. It is incremented by 1 with each successful message transfer except when the index field equals 0.

4. Configure the standard interrupt queue in the preferred area of memory and initialize Register 06 with the onboard RAM address of the beginning of the queue.

5. Select the desired RT in Register 10.

6. Enable the Standard Interrupt Bit in the high priority interrupt enable register and the interrupt when index = 0 bit in the control word.

7. Enable the desired bus and set the Start Enable Bit in Register 00.

8. The DTI-PC/S receives the incoming data words and stores them in memory as pointed to by the data list pointer. All incoming data is checked for validity.

9. The DTI-PC/S checks the status of the input bits from the RT Address Register (Register 10) and inputs them into the 1553 status word. The DTI-PC/S then transmits the status word.

10. A message status word is then written to memory as pointed to by the message status pointer and the pointer is incremented by 1 (since the index ≠ 0).

11. The data list pointer is incremented by 32 and the index field of the control word is decremented to 0.

12. The DTI-PC/S asserts a standard interrupt because the index equals 0. The interrupt queue entry indicates a subaddress event interrupt occurred and the interrupt queue pointer contains the address of the corresponding Subaddress 2 RT response block.

BM Operational Sequence with Interrupts

1. Configure the monitor control blocks in the preferred area of memory and initialize Register 02 with the onboard RAM address of the beginning of the Block 5.

2. Set up the data list pointers of the monitor control blocks to store all data words in the preferred area of memory.

3. Verify the BC/RT Bit in Register 00 is 0. The RTs to be monitored can be enabled via Registers 16 and 17. Enable desired bus in Register 00.

4. Ensure the RT address parity bit in Register 10 is set to 0.

5. Enable the Standard Interrupt Bit in the High Priority Interrupt Enable Register (Register 07). Also, enable the command block bit in Register 09 and the Command Block Access Bit in the control/status word of the monitor control block.

6. Select the enable bit in the Bus Monitor Control Register (Register 14). Select the RTs to monitor via Registers 14, 16, and 17.

7. Configure the standard interrupt queue in the preferred area of memory and initialize Register 06 with the onboard RAM address of the beginning of the queue.

8. Set Bit 0 in Register 00.

9. Message monitoring begins. The command, status and data words are written into memory.

10. If an RT-to-BC message is being monitored, the command word is stored at Command Word 1 of the monitor control block, the status is stored at Status Word 2 of the monitor control block, and the incoming data words are stored in memory as pointed to by the data list pointer.

11. The DTI-PC/S, having encountered the Command Block Access Bit, asserts a standard interrupt and logs the event in the interrupt queue.

Registers

The DTI-PC/S contains 26 16-bit registers. Seven of these registers control interrupt handling. The following six interrupt registers, described in the Interrupts section, control operation:

- Interrupt Queue Pointer Register (06)
- High Priority Interrupt Enable Register (07)
- High Priority Interrupt Status/Reset Register (08)
- Standard Priority Interrupt Enable Register (09)
- Interrupt Counter Read/Clear Register (19)
- Autodecrement Interrupt Counter Register (20)

Four Configuration Registers control bus connection, memory size, memory banking, base memory address, and standard and high priority interrupt level. These registers are:

- Bus Connection Relay Control Register (25)
- Memory Size/Bank Select Register (26)
- Base Address Select Register (27)
- Interrupt Level Selection Register (29)

(See Getting Started for more information on the Configuration Registers.)

The following two registers, described in the Remote Terminal section, control the RT:

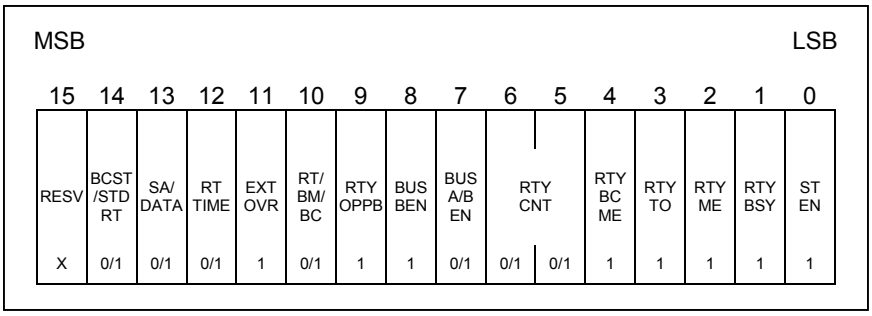
- Control Register (00)
- RT Address Register (10)

Ten registers control the Bus Monitor and are described in the Bus Monitor section:

- Control Register (00)
- Start of Message Record Block Register (02)
- Interrupt Queue Pointer Register (06)
- High Priority Interrupt Enable Register (07)
- Standard Priority Interrupt Enable Register (09)
- RT Address Register (10)
- Reset Timer Register (13)
- Bus Monitor Control Register (14)
- Bus Monitor Terminal Address Select Register (16)
- Bus Monitor Terminal Address Select Register (17)

Note: 1 = Set (Enable). 0 = Clear (Disable).

Control Register 00



Bit 15 **Reserved**

Bit 14 **BC ST/STD RT - Broadcast/Standard RT Select.**
1 = RT 31 is standard RT. 0 = RT 31 is enabled for broadcast.

Bit 13 **SA/DATA - SAs/Data Select.**
0 = SA0 and SA31= mode SAs. 1 = SA0 = Mode. SA31 = data.

Bit 12 **RT TIME - RT Timeout.**
BC Mode - RT Response Timeout. The time the BC waits for the RT to respond. RT Response Timeout 16 µs = 0. RT Response Timeout 32 µs = 1.

Bit 11 **EXT OVR - External Override Enable .**
Set this bit to enable external override; used in a multi-redundant system. You need to ground the External Port Pin 3.

Bit 10 **RT/BM/BC - RT, BM or BC Select.**
Select operating mode of DTI-PC/S. BC = 1; RT/BM = 0.

Bit 9 **RTY OPPB - Retry on Opposite Bus.**
BC Mode - enables Retry on alternate bus. If you have enabled Bus A for multiple retries via Bits 5 and 6, these retries take place on Bus B.

Bit 8 **BUS BEN - Enable Bus B.**
RT/BM Mode - 1 enables Bus B for communication.

Bit 7 **BUS A/B EN - Enable Bus A/B.**
BC Mode - selects the communication bus. Bus A = 1. Bus B = 0. RT/BM Mode - 1 enables Bus A for communication.

Bits 6 & 5 **RTY CNT - Retry Count.**
BC Mode - defines the number of transmission retries (1 to 4):

Bit Value of Registers 5 and 6	Number of Retries
00	1
01	2
10	3
11	4

Bit 4 **RTY BC ME - Retry On Message Error.**
BC Mode - enables an automatic RETRY on any Message Error detected by the BC.

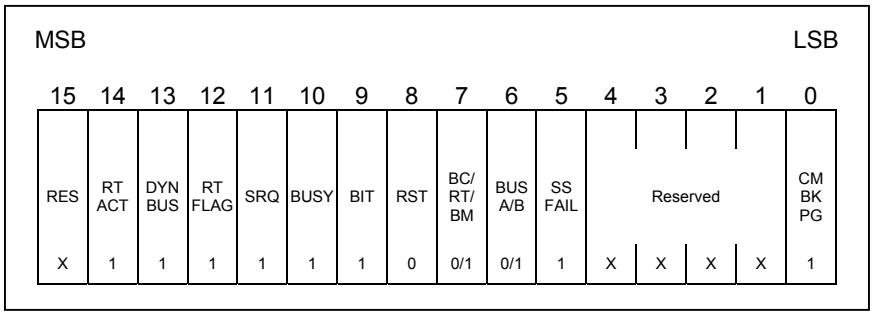
Bit 3 **RTY TO - Retry On Timeout.**
BC Mode - enables an automatic RETRY on a Response Time Out condition.

Bit 2 **RTY ME - Retry On Message Error.**
BC Mode - enables automatic RETRY when message error bit is set in the 1553 RT status message.

Bit 1 **RTY BSY - Retry on Busy Bit.**
BC Mode - enables automatic RETRY on a received busy bit in the 1553 RT status response.

Bit 0 **ST EN - Start Enable.**
Start Enable (not READable) for RT/BM modes. BC Mode - starts/restarts a buslist execution. After any RESET, the RT, BM or buslist execution must be restarted via this bit.

Status Register 01 (Read Only)



Bit 15 **Reserved**

Bit 14 **RT ACT - RT Active.**
Indicates the RT is active (servicing a command).

Bit 13 **DYN BUS - Dynamic Bus Control Acceptance.**
Indicates the state of the Dynamic Bus Control Acceptance Bit in the RT Status Word.

Bit 12 **RT FLAG - Terminal Flag.**
Terminal Flag Bit is set in the RT Status Word.

Bit 11 **SRQ - Service Request.**
Service Request Bit is set in the RT Status Word.

Bit 10 **BUSY - Busy Bit.**
Busy Bit is set in the RT Status Word.

Bit 9 **BIT - Built-In Test.**
Built-in Test in progress.

Bit 8 **RST - RESET.**
RESET in progress.

Bit 7 **BC/RT/BM - Bus Controller, Remote Terminal or Bus Monitor Mode.**
Indicates the current mode of operation. 1 = BC. 0 = RT/BM.

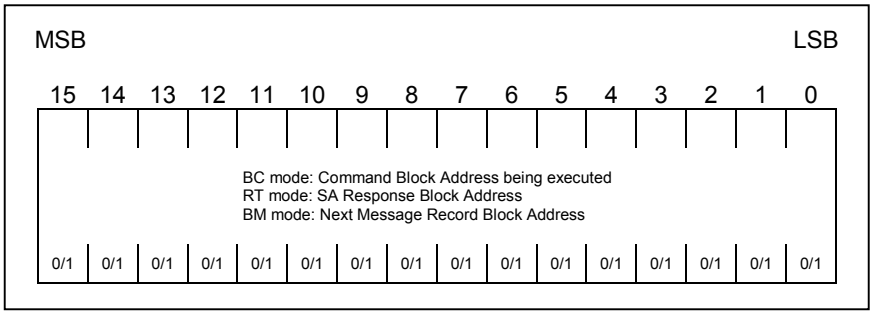
Bit 6 **BUS A/B.**
Indicates the Bus in use or last used. 1 = Bus A. 0 = Bus B.

Bit 5 **SSFAIL - Subsystem Fail Indicator.**
Indicates receiving a subsystem fail signal from the host subsystem on the SSYSF input (External Port).

Bits 4-1 **Reserved**

Bit 0 **CM BK PG - (BC) Command Block/RT, BM.**
BC - Command Block execution in progress. RT/BM - in Operation.

Current Command Block Instruction Address (BC), Subaddress Response Block Address (RT) and Next Message Record Block Register (BM) 02

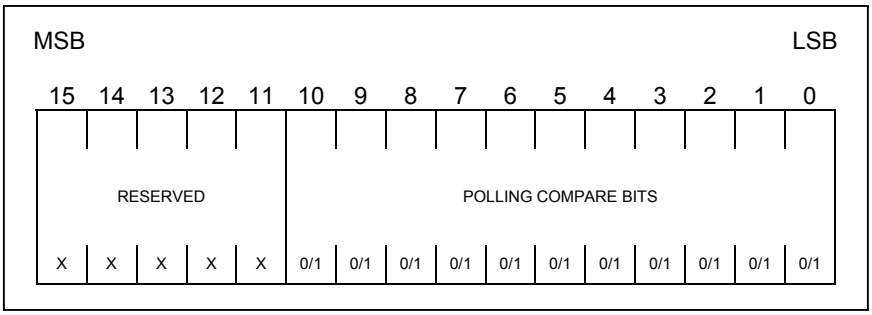


In BC mode, this register contains the onboard RAM address of the Command Block instruction being executed. Accessing a new Command Block instruction updates the register.

In RT mode, the PC host CPU initializes this register to the onboard RAM starting location of the SA Response Block. The host must allocate 320 sequential locations following this starting address. For proper operation, this location must start in a *i* x 512 decimal address boundary, where *i* is an integer.

In BM mode, this register contains the onboard RAM address for the next Message Record Block to be recorded.

Polling Compare Register 03

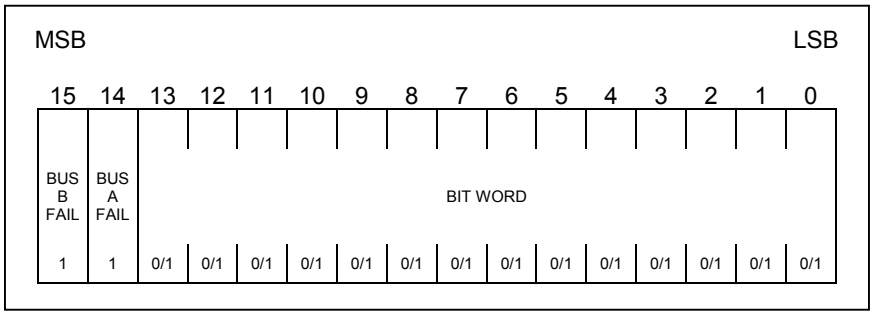


In the Polling Mode, the RT Response is compared to the Polling Compare Register. If any bits of the Polling Register match the Status Word, a Polling Compare Interrupt is generated. The eleven bits of this register (Bits 0 through 10) correspond to Bits 9 through 19 of the RT's MIL-STD-553B Status Word. For example, Bit 0 of Register 03 corresponds to Bit 19 of the Status Word. The RT's sync, RT Address and Parity Bits are not included.

Bits 15-11 Reserved

Bits 10-0 Polling Compare Bits.
The bits to be compared with the Status Word.

Bit Word Register 04



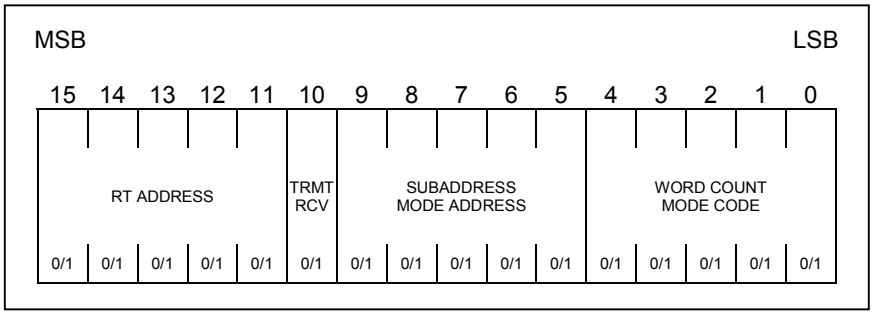
Bit 15 **BUS B FAIL - Bus B Failure.**
Updated during BIT-MC3.

Bit 14 **BUS A FAIL - Bus A Failure.**
Updated during BIT-MC3.

Bits 13-0 **BIT Word.**
Contains the BIT word returned by the RT in response to Mode Code 19. The DTI-PC/S writes values to this register in response to either an Initiate Self-Test Mode Code (RT Mode) or a WRITE to Register 11. If the Bit Word needs to be modified, it can be read out, modified and re-written to this register. The contents of this register are transmitted onto the 1553 bus in response to a Mode Code 19 command (Transmit BIT word).

Current Command Register 05 (Read Only)

In RT mode, this register contains the command currently being processed. When not processing a command, the DTI-PC/S stores the last command or status transmitted on the 1553 bus. This register is updated only when Bit 0 of Register 00 is set. In BC mode, this register contains the most current command sent out on the 1553 bus.



Bits 15-11 RT Address.

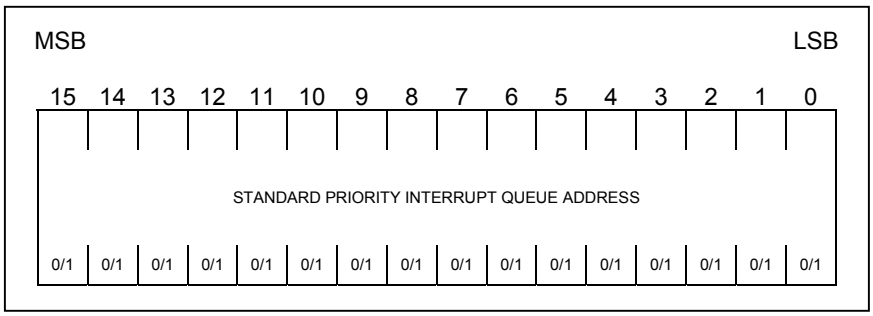
Bit 10 TRMT/RCV. Transmit/Receive.

Bits 9-5 Subaddress/Mode.

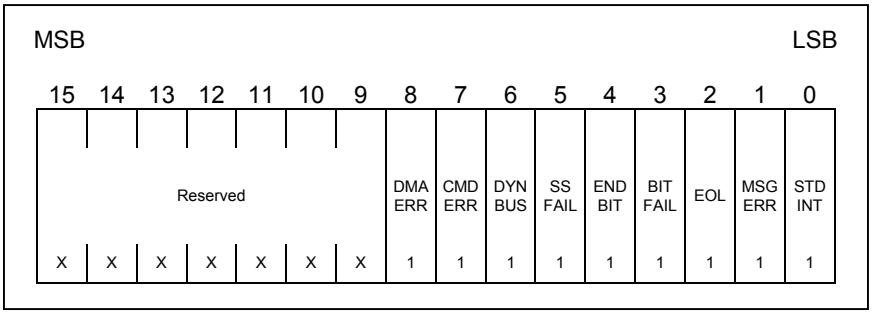
Bits 4-0 Word Count/Mode Code.

Interrupt Queue Pointer Register 06

Contains the onboard RAM starting location of the Standard Priority Interrupt Queue (initialized by host). This register is updated by the DTI-PC/S with the address of the next entry in the queue when an interrupt block is written to the queue.



High Priority Interrupt Enable Register 07



Bits 15-9 Reserved

Bit 8 DMA ERR - Data Overrun Enable.
Data Overrun indicates that an internal DMA grant for access to the onboard RAM was not received by the DTI-PC/S within the allocated time required for a successful data transfer to memory.

Bits 7 CMD ERR - Illogical Command Error Enable (BC).
This bit enables a high priority interrupt to be asserted upon the occurrence of an Illogical Command. Illogical commands include incorrectly formatted RT-to-RT Command Blocks.

Bit 6 DYN BUS - Dynamic Bus Control Mode Code Interrupt Enable.
Used in conjunction with the Dynamic Bus Control Bit in the RT Address Register to generate a high priority interrupt.

Bit 5 SS FAIL - Subsystem Fail Enable.
Enables the high priority interrupt when receiving a SSYSF input.

Bit 4 END BIT - End of BIT Enable.
Indicates the end of the internal BIT routine.

Bit 3 BIT FAIL - BIT Word Fail Enable.
Enables the high priority interrupt upon the detection of a BIT failure.

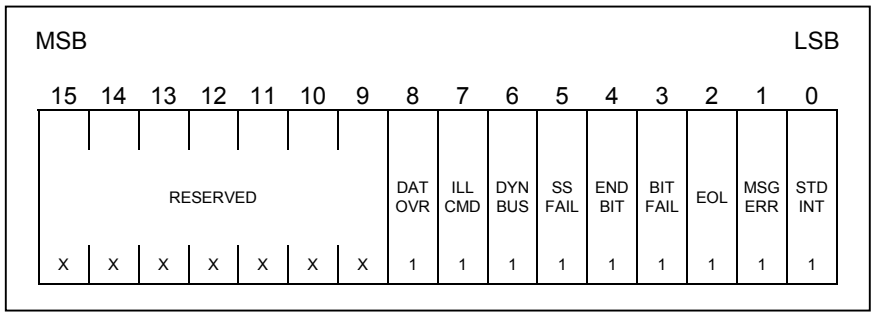
Bit 2 EOL - End of Buslist (BC).
Enables the high priority interrupt when the end of the buslist is reached. This interrupt can be superseded by other high priority interrupts.

Bit 1 MSG ERR - Message Error Enable.
Enables interrupts on bus message errors in the BC, RT or BM mode.

Bit 0 STD INT - Standard Interrupt Enable.
Enables all standard interrupts to notify the host.

High Priority Interrupt Status/Reset Register 08

When a high priority interrupt is asserted, this register indicates the event that caused the interrupt. To clear the interrupt signal and reset the bit, write a 1 to the appropriate bit.



Bits 15-9 Reserved.

Bit 8 DAT OVR - Data Overrun.
Data Overrun indicates that an internal DMA grant for access to the onboard RAM was not received by the DTI-PC/S within the allocated time required for a successful data transfer to memory.

Bit 7 ILL CMD - Illogical Broadcast Command.
Asserted upon the occurrence of an Illogical Command. Illogical commands include incorrectly formatted RT-to-RT Command Blocks.

Bit 6 DYN BUS - Dynamic Bus Control Acceptance.
Indicates that a Dynamic Bus Control command was received.

Bit 5 SS FAIL - Subsystem Fail.
Indicates that a SSYSF input was received.

Bit 4 END BIT - End of BIT.
Indicates the end of the internal BIT routine.

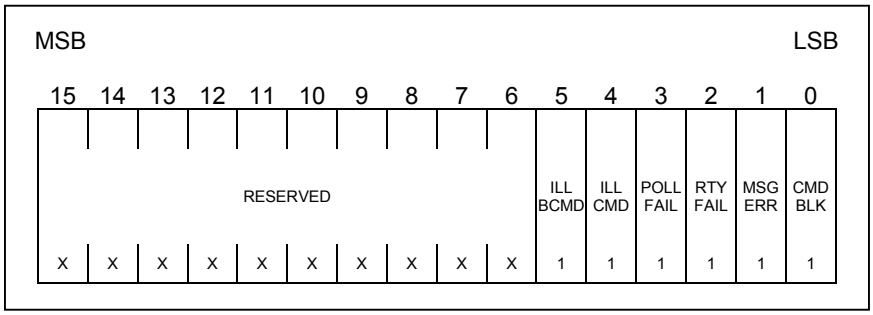
Bit 3 BIT FAIL - BIT Word Fail.
Indicates the detection of a BIT failure.

Bit 2 EOL - End of Buslist.
Indicates that the end of the buslist was reached. This interrupt can be superseded by other high priority interrupts.

Bit 1 MSG ERR - Message Error (BC, RT or BM) .
Enables interrupts on bus message errors in the BC, RT or BM mode.

Bit 0 STD INT - Standard Interrupt.
Set when any standard interrupt occurs if standard interrupts are enabled (Register 7, Bit 6).

Standard Priority Interrupt Enable Register 09



Bits 15-6 Reserved.

Bit 5 ILL BC MD - Illegal Broadcast Command (RT).
When set, this bit enables an interrupt indicating that an illegal Broadcast Command has been received.

Bit 4 ILL CMD - Illegal Command (RT).
When set, this bit enables an interrupt indicating that an illegal command has been received.

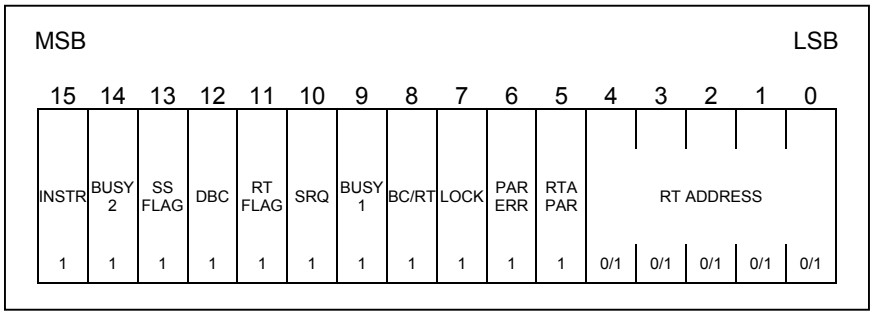
Bit 3 POLL FAIL - Polling Comparison Match (BC).
This enables an interrupt indicating that a polling event has occurred.

Bit 2 RTY FAIL - Retry Fail (BC).
This bit enables an interrupt indicating that all the programmed number of retries have failed.

Bit 1 MSG ERR - Message Error Event (BC, RT, BM).
This bit enables a standard interrupt for message errors.

Bit 0 CMD BLK - Command/Monitor Block Interrupt and Continue (BC/BM).
This bit enables an interrupt indicating that a Command Block Instruction or a Monitor Message block, with the Interrupt and Continue function enabled, has been executed.

Remote Terminal Address Register 10



Bit 15 **INSTR - Instrumentation (RT).**
This function enables the Instrumentation Bit in the RT Status Word.

Bit 14 **BUSY2 - Busy.**
This bit sets the Busy Bit in the RT Status Word. It does not inhibit data transfers.

Bit 13 **SS FLAG - Subsystem Fail.**
This bit sets the Subsystem Flag bit in the MIL-STD 1553B Status Word. In the RT Mode, the Subsystem Fail is also logged into the Message Status Word.

Bit 12 **DBC - Dynamic Bus Control Acceptance (RT).**
Enabling this bit allows the DTI-PC/S to accept Dynamic Bus Control and to set the appropriate bit in the MIL-STD-1553B Status Word and the DTI-PC/S Status Register. Host intervention is required for the DTI-PC/S to take over as BC.

Bit 11 **RT FLAG - Terminal Flag (RT).**
This bit sets the MIL-STD 1553B Status Word Terminal Flag bit. The bit in the MIL-STD 1553B Status Word is also internally set if the BIT fails

Bit 10 **SRQ - Service Request (RT).**
This bit sets the Status Word Service Request bit.

Bit 9 **BUSY1 - Busy Mode Enable (RT).**
This bit sets the Status Word Busy Bit and inhibits all data transfers to the subsystem. The only possible DMA transfers are for the enabled events logged in the Interrupt Log List.

Bit 8 **BC/RT - BC/RT Mode Select.**
This bit indicates the internal BCRTSEL signal is set. This is not a useful bit as it does not reflect the state of the BC/RT Mode Select Bit (Register 00, Bit 10).

Bit 7 **LOCK - Change Lock-Out.**
Change Lock-Out Enable. When set, this bit prohibits changes to the RT Address or the BC/RT mode select, using internal registers.

Bit 6 **PAR ERR - RT Address Parity Error.**
This bit indicates an RT Address Parity Error. It appears after the RT Address is latched, if a parity error exists.

Bit 5 **RTA PAR - RT Address Parity.**
This is an odd parity used with the RT Address. It ensures accurate recognition of the RT.

Bits 4-0 **RT Address**
Modify the RT Address by writing to these bits. Must be written after Reset.

BIT Start Register 11 (Write Only)

Any write to this register's address initiates the internal BIT routine. This test only checks internal encoders/decoders and protocol logic.

Reset Command Register 12 (Write Only)

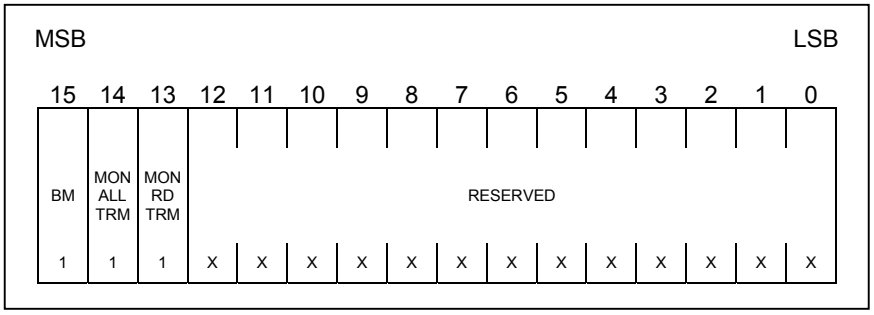
Any write to this register's address location initiates an immediate reset sequence of the encoder/decoder and protocol sections of the DTI-PC/S, lasting one microsecond. This reset is identical to the one used for the RT mode code.

Note: Bit 15 (Bus Monitor Mode Select) of Register 14 is set to OFF after a write to this register.

Reset Timer Register 13 (Write Only)

Any WRITE to this register resets the RT or BM timer to 0.

Bus Monitor Control Register 14



Bit 15 **BM - Bus Monitor Select.**
Cleared by a write to Reset Register 12. This bit should be cleared for RT operations.

Note: Bit 10 of Register 00 must be set to 0 to enable BM mode.

Bit 14 **MON ALL TRM - Monitor All Terminals.**
If set, all RT activity is monitored. If not set, Bit 13 must be set.

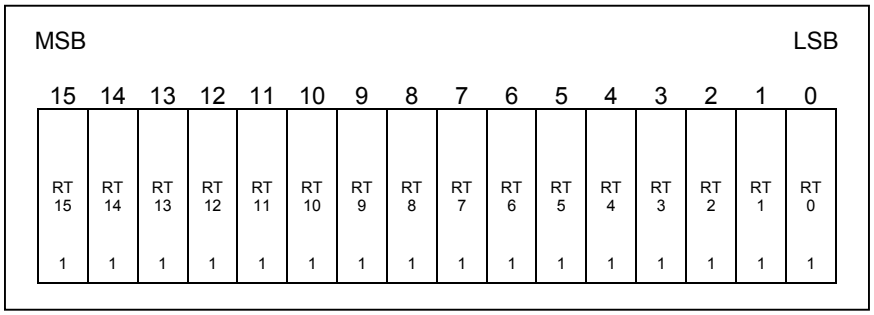
Bit 13 **MON RD TRM - Monitor Register Declared Terminals.**
If set, RTs selected in Registers 16 ad 17 are monitored. If not set, Bit 14 must be set.

Bits 12-0 **Reserved**

Register 15 Reserved

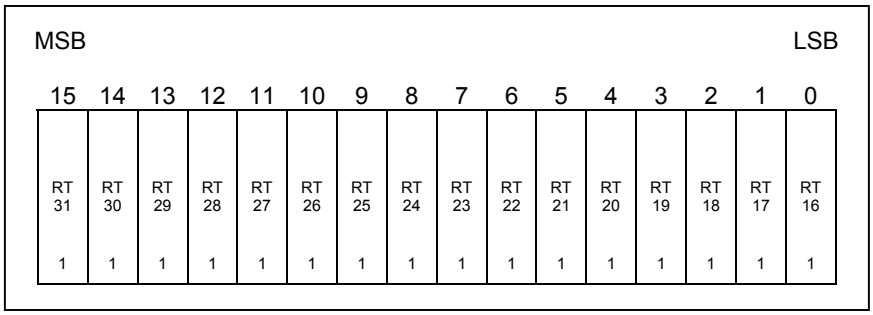
Bus Monitor Terminal Address Select (RT 0 - 15) 16

If Bit 13 of Register 14 is set, setting the appropriate bit in this register enables monitoring of the selected RT.



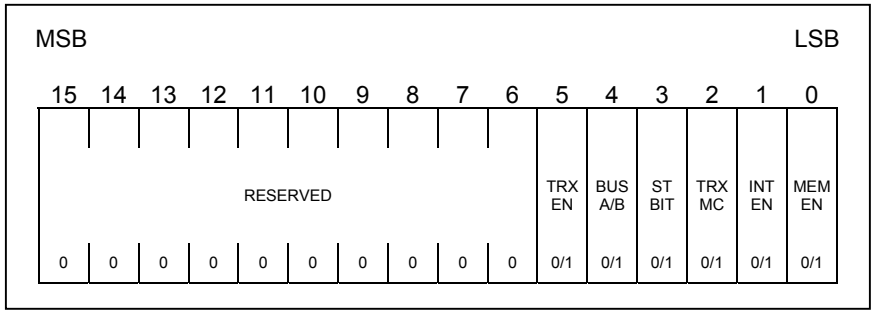
Bus Monitor Terminal Address Select (RT 16 - 31) 17

If Bit 13 of Register 14 is set, setting the appropriate bit in this register enables monitoring of the selected RT.



Master Reset Register 18

A READ of Register 18, initializes a Master Reset on the DTI-PC/S, clearing all sequencers and internal registers. Memory is not cleared. The READ data is not meaningful. The definitions below are valid for writes.



Bits 15-6 Reserved (Must be 0).

Bit 5 TRX EN - Transceiver Enabled.
Write : 0 = Enable Transceiver. 1 = Disable Transceiver. Default = 1.

Bit 4 BUS A/B - Bus A/B Enable.
Write: 0 = Bus B. 1 = Bus A. Default = 0.

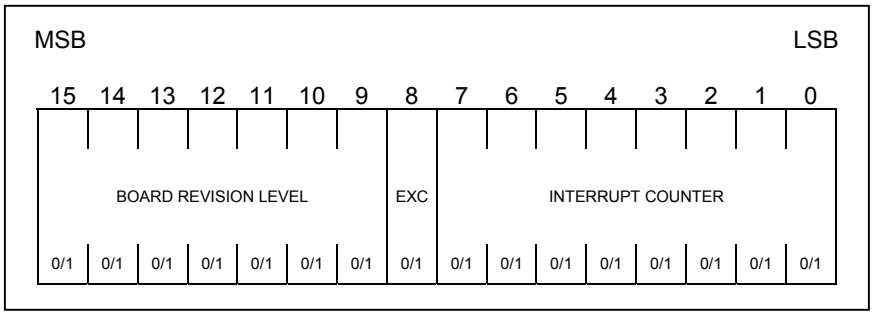
Bit 3 ST BIT - Start BIT Test.
To start the BIT Test, WRITE a 0 and then a 1. Default = 0.

Bit 2 TRX MC - Transmit Mode Code.
Write: 0 = Transmit Mode Code 3 to RT 30 (Word = F403). 1 = Transmit Mode Code 19 (Word = F413) to RT 30 on self-test. Default = 0.

Bit 1 INTEN - Interrupt Enable (High/Standard Priority Interrupts)
Write: 0 = Enable Interrupts. 1 = Disable Interrupts. Default = 1.

Bit 0 MEMEN - Memory Enable
Write: 0 = Dual-Port Memory Disable. 1= Dual-Port Memory Enable. Default = 0.

Interrupt Counter Read/Clear Register 19

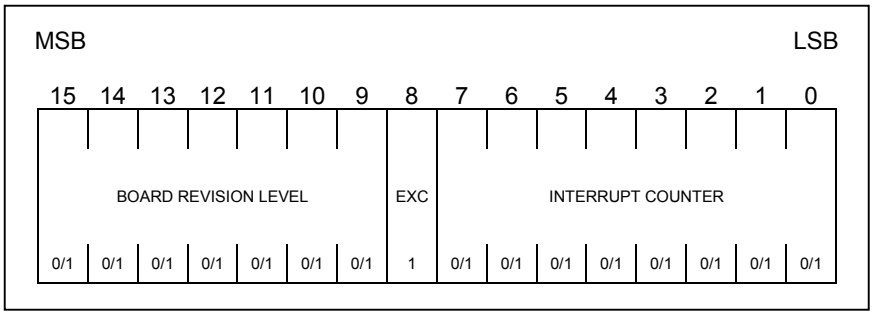


Bits 15-9 Board Revision Level.
These seven bits reflect the revision level of the DTI-PC/S.

Bit 8 EXC - Exceed Bit.
This bit is set when 255 standard interrupts have been generated, but not processed, and another interrupt occurs (256th). This bit is cleared via a WRITE to Register 19, a master reset or a host system reset.

Bits 7-0 Interrupt Counter
These bits store the number of interrupts held within the Standard Interrupt Queue. A READ from this register returns the contents. A WRITE clears the Exceed Bit and the Interrupt Counter Bits.

Autodecrement Interrupt Counter Register 20



Bits 15-9 Board Revision Level.
These seven bits reflect the revision level of the DTI-PC/S.

Bit 8 EXC. Exceed Bit.
When the 256th interrupt has been stored, but not processed, the Exceed Bit is set. This bit can be cleared via a WRITE to Register 19, a master reset or host system reset. It is not cleared by decrementing the counter.

Bits 7-0 Interrupt Counter.
These bits store the number of interrupts held within the Standard Interrupt Queue. A READ from this register decrements the count field by 1, then returns the contents. A WRITE decrements the count field by 1.

Registers 21 Through 22 Reserved

Device Type Register 23 (Read-Only)

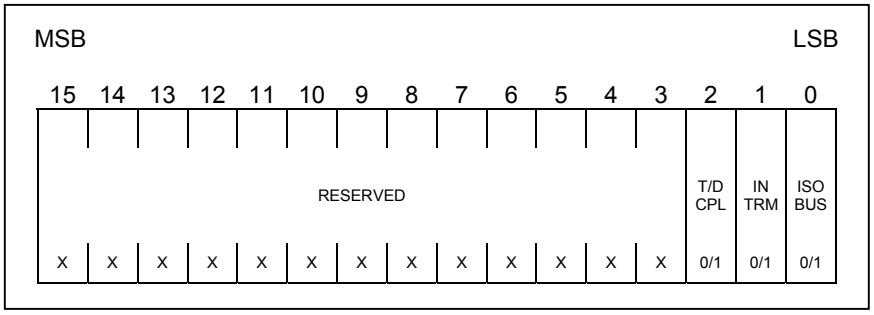
This register identifies the DTI board and can be used to verify the I/O address alignment. Values are 218H for a single channel board and 228H for a dual channel board.

Manufacturer ID Register 24 (Read-Only)

This register identifies the DTI board and can be used to verify I/O Address alignment. A value of FB4H is always read from this register.

Bus Connection Relay Control 25

Three bits in this register control relays that isolate the DTI-PC/S from the 1553 bus for self-test, connect an internal termination resistor to the DTI-PC/S and select a direct or transformer coupled connection to the bus. These selections are typically configured once for a particular test setup. An additional bit in this register allows the machine controlling the bit test pattern to output data continuously for diagnostic purposes.



Bits 15-3 Reserved.

Bit 2 T/D CPL - Transformer/Direct Coupling.
This relay can connect the DTI-PC/S to the 1553 bus in a direct or transformer coupled configuration. Use direct coupling if the distance between the DTI-PC/S and the 1553 bus measures 12 inches or less. Use transformer coupling if the distance between the DTI-PC/S and the 1553 bus exceeds 12 inches, but not 20 feet. Direct coupling is applied during the isolated internal self-test at powerup. After the self-test concludes, the bit is set according to UUT connection requirements. The selected connection applies to Buses A and B.

0 = Transformer coupling selected.
1 = Direct coupling selected.
Default = 1.

Bit 1 INTRM - Internal Termination.
This relay connects a termination resistor, required when using the direct coupling. The resistor is applied during the isolated internal self-test at powerup to provide a test load. After the self-test concludes, the bit is set per UUT connection requirements. The selected connection applies to Buses A and B.

0 = No termination connected.
1 = Internal termination connected.
Default = 1.

Bit 0 **ISOBUS - Isolate Bus.**
This relay can isolate the DTI-PC/S from the 1553 bus. To isolate the DTI-PC/S from the 1553 bus, set the bit to 1 (the default value). When the bit is set to 0, the DTI-PC/S is connected to the 1553 bus. This relay is typically used only for powerup self-test of the DTI-PC/S board and doesn't require disconnecting the board from any UUT. After a successful powerup self-test, the bit is usually set to 0. The selected connection applies to both Buses A and B.

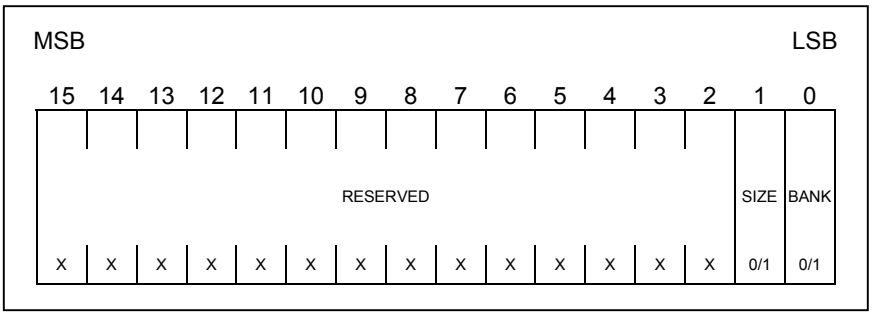
0 = connected to 1553 bus.
1 = isolated from 1553 bus.
1 = Default.

Note: For the DTI-PC/S to operate on a 1553 bus, this value must be changed to 0.

Memory Size/Start Address/Bank Select 26

The least significant six two of this register are used to select the dual-port RAM size, and select the bank of onboard RAM to be used for dual-port operation. The DTI-PC/S can address 32K words of memory; therefore, this is the maximum size of space that can be allotted in the PC memory address space. However, the user has the option of selecting smaller dual-port memory sizes. By selecting a 16K word size and different banks, you can configure two channels to share one memory page.

Note: All accesses to the operational registers, the configuration registers or the dual-port RAM from the PC host must be word transfers. Byte transfers do cause unpredictable results.



Register 27 is used to select the base memory address on 64 KB module boundaries. The dual-port RAM size and Bank Select Bits of Register 26 are used to select decoding locations for smaller increments of memory within the 64 KB space. Selecting other address locations for smaller increments of memory is useful when several boards are mapped into a limited address space. The default selection is 64 KB (32K words) of RAM starting at the base address.

Bits 15-2 Reserved.

Bit 1 RAM Size Select.
This bit selects the amount of RAM appearing in the PC address space. The amount of RAM selected is shared in dual-ported fashion with the DTI-PC/S.

0 = 16 K words; 32 KB
1 = 32 K words; 64 KB
Default = 64 KB.

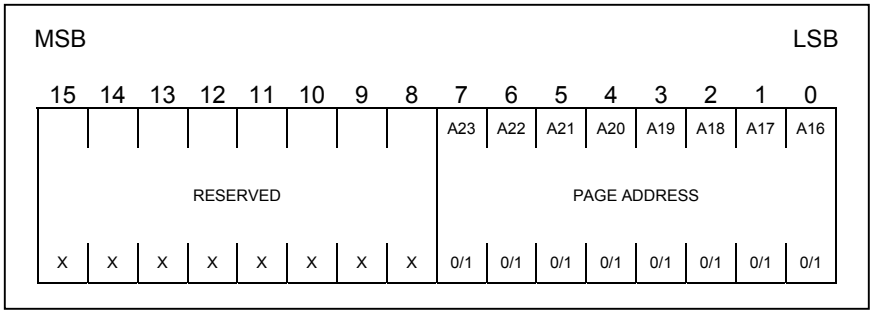
Bit 0 Bank Select.
This bit selects the upper or lower half of the selected page via Register 27. To enable, set Bit 1 to 0, which selects 32KB of dual-port RAM.

0 = Lower half of page (0-7FFF)
1 = Upper half of page (8000-FFFF)
Default = 0

Note: This bit is meaningless if a 64KB RAM size is selected.

Standard Address Select 27

This register sets the base starting address for the amount of dual-ported RAM selected in Register 26. The bits of Register 26 can be used to offset the RAM address within the 64 KB space selected by this register.

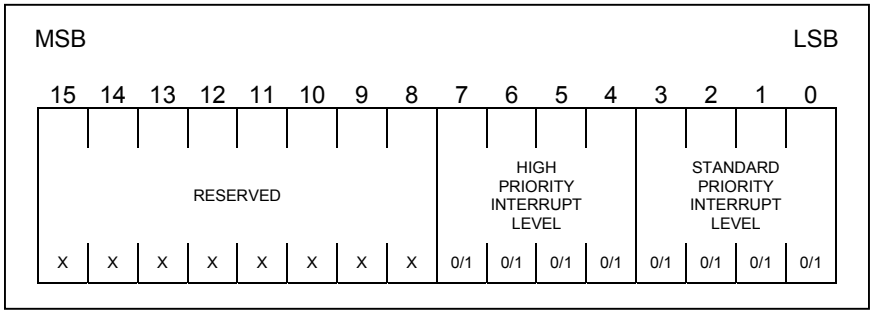


The page address matches the address line A23-A16 on the host bus to identify accesses to the board. On systems with multiple channels, the memory space for each channel must not overlap.

Register 28 - Reserved

Interrupt Level And Vector Width Selection 29

Eight bits in this register are used to select the standard priority interrupt level and the high priority interrupt level.



Bits 15-8 Reserved.

Bits 7-4 High Priority Interrupt Level.
These three bits are used to select the high priority interrupt level. Valid levels are 3,5, 10, 11, 12 and 15. Programming an invalid level results in selecting the next highest level. For example, selecting Interrupt Level 7 (0111) allows the high priority interrupts to occur on Level 10 (1010).

Bits 3-0 Standard Priority Interrupt Level.
These three bits are used to select the standard priority interrupt level. Valid levels are 3, 5, 10, 11 12 and 15. Programming an invalid level results in selecting the next highest level. For example, selecting Interrupt Level 13 (1101) allows standard priority interrupts to occur on Level 15 (1111).

Registers 30 and 31 - Reserved

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Interrupts

Standard and High Priority Interrupts

The DTI-PC/S allows MIL-STD-1553B events to be defined as high priority interrupt, standard priority interrupt or no interrupt. The main difference between standard interrupts and high priority interrupts is the method by which they are serviced. High priority interrupts are recorded in the registers and generally handled upon occurrence. Standard priority interrupts are queued to a log (Figure 4-1).

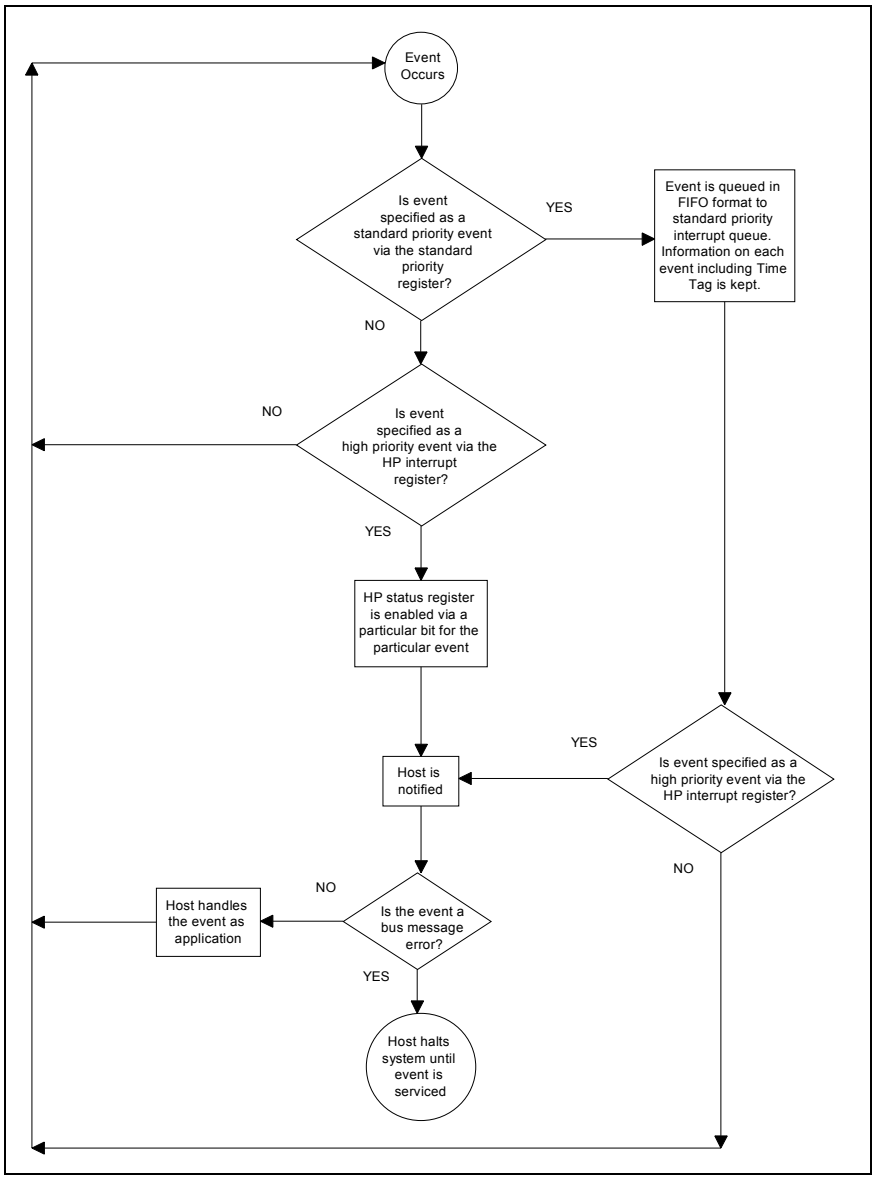


Figure 4-1. The Interrupt Process

Once interrupted, you have the option of reading the interrupt from a queue. By setting Bit 0 of the High Priority Interrupt Register (Register 07), the host is notified each time a standard priority interrupt occurs. If Bit 0 is not set, the events are queued to the log but the host is not notified.

The standard priority interrupt queue can store up to 255 entries (or messages). The number of standard priority interrupts queued is continuously counted and reflected in the Interrupt Counter (Register 19). This register allows applications to quickly assess the level of standard priority interrupts queued.

Interrupt messages include:

- MIL-STD 1553B status information that defines the event causing the interrupt (message retry, polling comparison failure, illegal command, illegal broadcast command, specific mode code interrupt, subaddress interrupt, message error, no response time out, interrupt and continue)
- Location of corresponding Command Block instruction, subaddress response block or bus monitor message record block
- Address of the next standard priority interrupt entry in the queue

Interrupt Level

Standard Priority Interrupt Level
Bits 3-0 of Register 29 set the standard priority interrupt level. To set the standard priority interrupt to Level 5, Bits 0 and 2 must each be set to 1 and Bits 1 and 3 must be set to 0. The standard priority interrupt default is Level 3.

High Priority Interrupt Level
Bits 7-4 of Register 29 set the high priority interrupt level. To set the high priority interrupt to Level 10, Bits 7 and 5 must each be set to 1 and Bits 6 and 4 must be set to 0. The high priority interrupt default is Level 3.

Interrupt Queue

You can define the interrupt queue as circular or standard. In a circular queue, the last entry points to the first entry in the queue. The Interrupt Count Registers accept a maximum of 255 entries before the queue overflows. If the queue fills up, the most recent entries remain in the queue.

When the queue fills up in a standard interrupt queue, the last entry is overwritten, if the interrupts are not serviced. The standard interrupt queue is initialized by the host and consists of a first-in/first-out (FIFO) queue of enabled interrupt events (Figure 4-2).

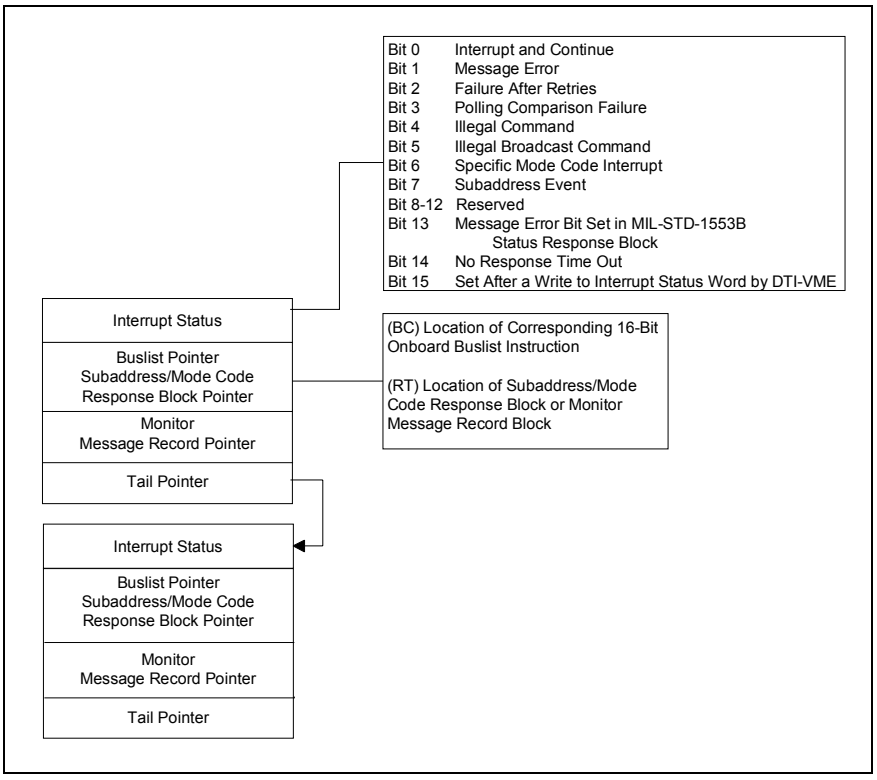


Figure 4-2. The Interrupt Queue

Each entry in the standard priority interrupt queue consists of the following three 16-bit words:

Interrupt Status Word

The 16 bits of status information define the type of interrupt. The Message Error Event Bit must be set in Register 09 for error details to be stored.

Pointer

BC Mode - The pointer indicates the location of the corresponding Command Block instruction.

RT Mode - The pointer indicates the location of the corresponding subaddress/mode code response block.

BM Mode - The pointer indicates the location of the corresponding Bus Monitor record.

Tail Pointer

The Tail Pointer contains the address of the next standard priority interrupt entry in the queue. That address does not have to be the next contiguous address.

Operational Interrupt Registers

Six Operational Interrupt Registers control interrupt processing and are discussed on the following pages. (See the Registers section of this manual for more information.)

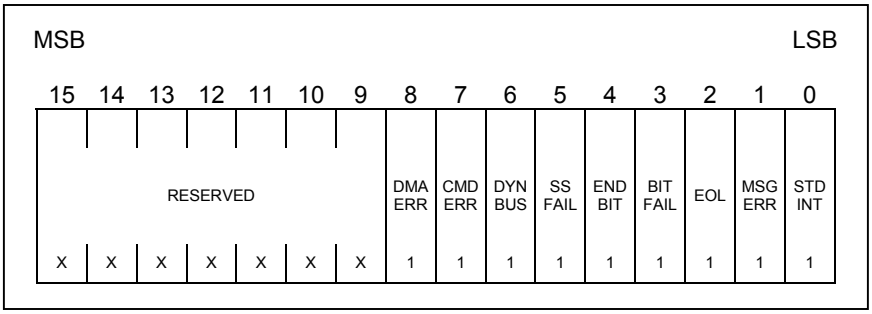
Interrupt Queue Pointer Register 06

The onboard RAM starting address of the standard priority interrupt queue is specified in the Interrupt Queue Pointer. As interrupt entries are added to the queue, the contents of this register are updated with the address of the next entry in the queue.

High Priority Interrupt Enable Register 07

The High Priority Interrupt Enable Register allows you to select up to nine events to be enabled for high priority system handling. When you enable an event as high priority, the host is notified each time the event occurs .

To enable a particular event for high priority interrupt handling, set the corresponding bit to 1. Setting Bit 0 to 1 enables all standard interrupts to notify the host.

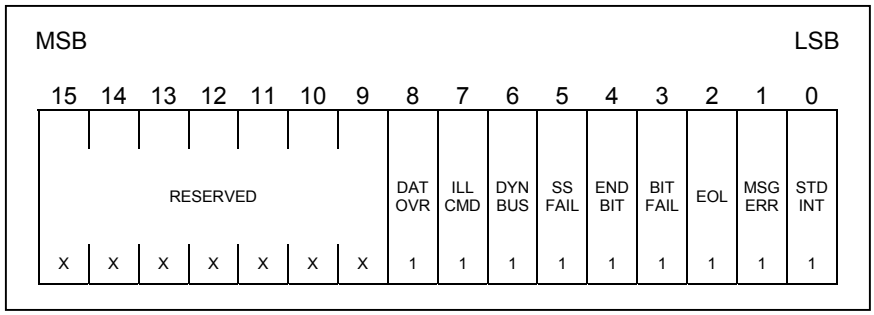


High Priority Interrupt Status/Reset Register 08

The High Priority Interrupt Status/Reset Register reflects the enabled events that have occurred. As each high priority interrupt is serviced, the corresponding bit is reset to 0 by writing a value of 1 to the bit.

If an event enabled for high priority occurs, the corresponding bit of this register reflects a value of 1. If more than one enabled event occurs before being serviced, all corresponding bits of this register reflect a value of 1. To clear an event, a value of 1 is written to the corresponding bit.

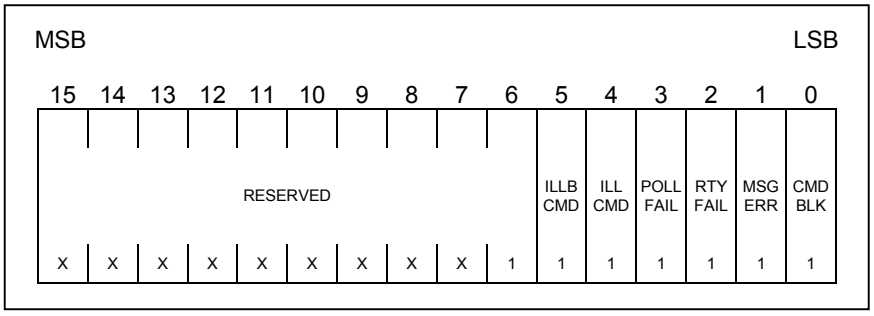
DTI-PC/S operation is suspended while generating a high priority interrupt until the corresponding status bit is reset by writing a 1 to that bit.



Standard Priority Interrupt Enable Register 09

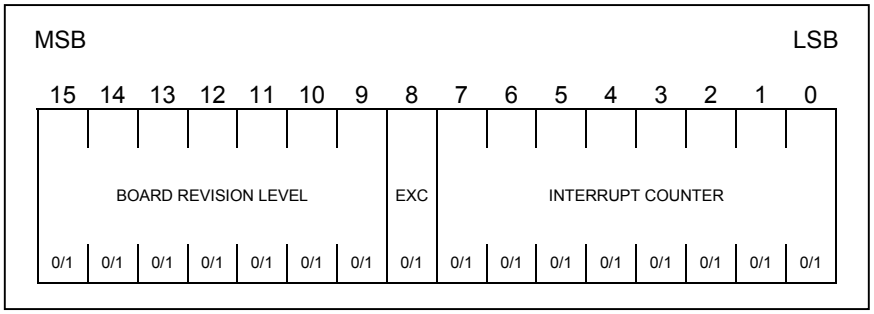
The Standard Priority Interrupt Enable Register allows you to select up to six events to be enabled for standard priority system handling.

Note: Set Bit 0 of Register 07 to allow standard priority interrupts to notify the host.



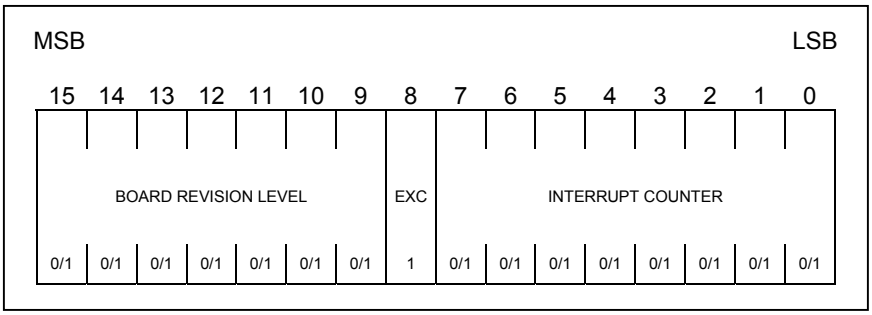
Interrupt Counter Read/Clear Register 19

The DTI-PC/S has a circular or standard interrupt queue that provides the ability to store up to 255 standard interrupt packets before writing over any packets. The number of standard interrupts in the interrupt queue at any time is recorded by Bits 0-7 of the interrupt counter. A READ of this register returns the contents. A WRITE clears the Exceed Bit and the Interrupt Counter Bits.



Autodecrement Interrupt Counter Register 20

Each time a queued standard interrupt is serviced, the interrupt queue counter must be reduced, or decremented. The Autodecrement Interrupt Counter Register provides the capability of reducing the queue counter. By issuing a command (READ or WRITE) to the Autodecrement Interrupt Counter Register, the count of standard priority interrupts is reduced by one.



Bits 15-9 Board Revision Level.
Reflect the revision level of the DTI-PC/S.

Bit 8 EXC - Exceed Bit.
When the 256th interrupt has been stored, but not processed, the Exceed Bit is set. This bit can be cleared via a WRITE to Register 19, a master reset or host system reset. It is not cleared by decrementing the counter.

Bits 7-0 Interrupt Counter.
Store the number of interrupts held within the Standard Interrupt Queue. A READ from this register decrements the count field by 1, then returns the contents. A WRITE decrements the count field by 1.

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Bus Controller Mode Of Operation

In the BC mode, the DTI-PC/S Command Block structure and internal registers provide the capability of defining, storing and executing comprehensive lists of Command Block (or bus) instructions, which allow specification of subsequent instructions.

Other BC features include:

- Reading instructions from a Command Block and sequentially retrieving the Command Block.
- Implementing programmable inter-message timing, which executes the next bus instruction up to a maximum of 64 microseconds (programmable at 16 usec resolution) after the beginning of the current message.
- Detecting protocol and bus errors, including command and associated status word address comparisons, response time out, long and short word count, bit count, parity and Manchester II errors.
- Initiating any broadcast or broadcast mode commands using RT Address 31.
- Polling RTs for information.
- Generating software selectable standard and high priority interrupts.
- Providing programmable bus retry capability (up to four retries on selected bus with retry on same bus or retry on opposite bus).
- Addressing up to 32 RTs.

Bus Controller Structure

For each message issued on the 1553 bus, an associated Command Block is set up. This eight-word Command Block contains all relevant message and RT status information (Figure 5-1). Bits within the header words allow you to enable certain functions and interrupts.

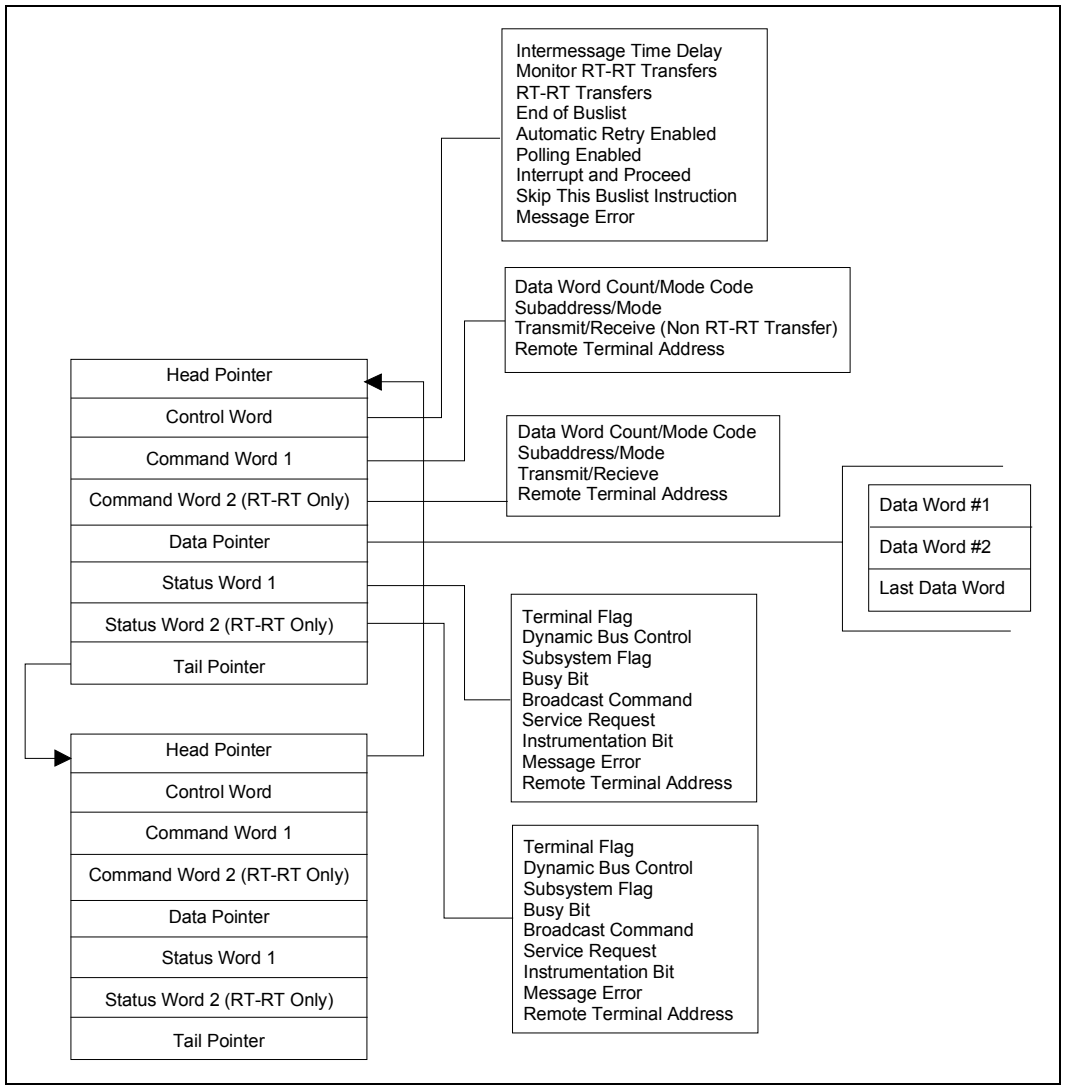


Figure 5-1. BC Command Block Structure

Head Pointer

The head pointer's 16 bits contain the onboard RAM address of the previous host-written bus instruction. This linkage allows you to loop through a list of bus instructions.

Control Word

The 16 control word bits control the several features:

Bit 15 **Bus Message Error.**
If a message error is detected during the execution of this bus instruction, this bit is set by the DTI-PC/S. Bus message errors can be enabled as high priority interrupts, standard priority interrupts or no interrupt. If a bus message error is enabled as a high priority interrupt and a bus message occurs, the DTI-PC/S halts operation until the interrupt is serviced. If a bus message error is enabled as standard priority, the data is queued and operation does not halt.

Bit 14 **Skip.**
If this bit is enabled with a value of 1, the bus instruction associated with the bus message is skipped. If the inter-message timer is enabled, the timer value expires before proceeding to the next bus message.

Example
If the timer is set for 64 microseconds, the next command block is executed 64 microseconds later.

Bit 13 **Interrupt and Continue.**
If this bit set, a standard interrupt is asserted when this instruction is transacted.

Bit 12 **Polling.**
Enables polling. The contents of the least significant 11 bits of the RTs status word are added with the value of the Polling Compare Register. You may then generate an interrupt.

Bit 11 **Automatic Retry Enable.**
Enables retries and operates with the Control Register to specify how retries are handled: On the same or opposite bus, Busy Bit set in RT status response, message error set in RT status response, response time out, message error detected by the BC and retry count (1 - 4).

Bit 10 **End of Buslist.**
If set, indicates this instruction is the last Command Block instruction in the buslist.

Bit 9 **Message Type is RT-to-RT Transfer.**
Identifies the bus instruction as an RT-to-RT transfer.

Bit 8 **Monitor RT-to-RT Transfer.**
Specifies RT-to-RT monitoring for the message enabled. Because the data is stored in the BC's data buffer, you can read data received/transmitted between the two RTs.

Bits 7-0 **Inter-message Timing.**
These bits define the period of time from the start of the currently executing Command Block instruction to the start of the next sequential Command Block buslist. They are enabled by a value greater than the time needed to complete the current message or a non-zero value used in conjunction with the Skip Bit in the control word.

The inter-message timer operates on a 16-microsecond resolution (Figure 5-2). If you require between 4,080 and 4,095 microseconds delay between the start of the current bus instruction and the start of the next sequential Command Block instruction, use a value of 1111 1111.

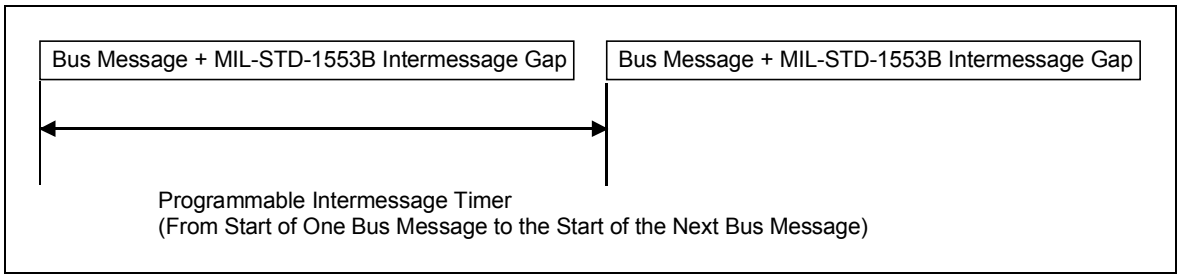


Figure 5-2. Inter-Message Timer

Note: If the inter-message timer is enabled and the Skip Bit is set, the timer provides the programmed delay before proceeding. If the current bus instruction exceeds the inter-message timer delay, the next message begins as if the timer was not enabled.

Command Word One

Used for all MIL-STD 1553B transfers, Command Word One is initialized by the VME host and contains the RT address, subaddress and the word count or mode code. The first command of an RT-to-RT message type is a receive command.

Command Word Two

Used in RT-to-RT transfers, Command Word Two is initialized by the host and contains the second command for RT-to-RT transfers. This command contains the transmitting RT address, subaddress and the word count. (Command Word Two is not used in single RT transfers).

Data Pointer

Initialized by the host, the 16 bits of this word point to the onboard memory storage location (buffer). The number of data words per bus instruction is 32 or less.

Status Word One

Status Word One is loaded when one of the following situations occurs:

- RT Response Status for a BC-to-RT transfer or an RT-to-BC transfer.
- Status Word of MIL-STD 1553B mode code transfer.
- RT Transmit Status for RT-to-RT transfer.

Status Word Two

The 16 bits of this word contain the Receiving Status in RT-to-RT transfers. If RT-to-RT transfers do not occur, the word is not used.

Tail Pointer

The 16 bits of this word contain the onboard RAM location of the next Command Block.

A buslist consists of one or several Command Blocks. Each Command Block is doubly-linked, either top-to-bottom or bottom-to-top (Figure 5-3). With top-to-bottom linkage, the tail pointer points to the next sequential Command Block's head pointer. With bottom-to-top linkage the head pointer points to the previous sequential Command Block's head pointer.

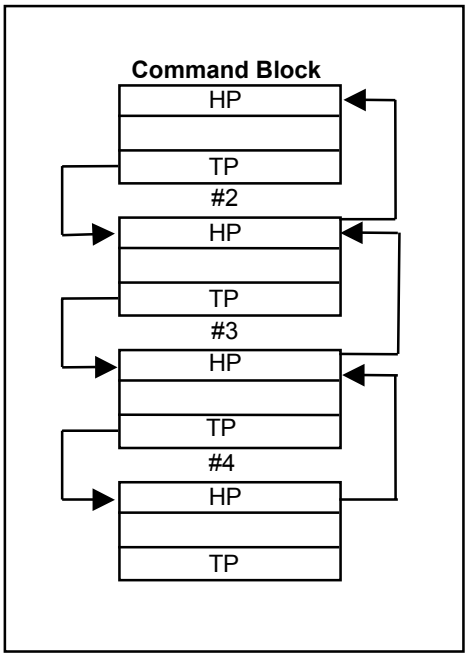


Figure 5-3. Command Block Linked Buslist

Mode Code/Broadcast Commands

This section describes the series of event that occur during Mode Code, Broadcast and Mode Code/Broadcast transfers.

Mode Command With Data Word (Transmit)

Functioning as a BC, the DTI-PC/S issues a transmit command to the RT using a mode code specified in MIL-STD 1553B. After command word validation, the RT transmits a status word, followed by one data word. The status word and data word transmit in one continuous fashion.

Mode Command Without Data Word (Transmit)

The DTI-PC/S issues a transmit command to the RT using a mode code specified in MIL-STD 1553B. After command word validation, the RT transmits a status word.

Mode Command With Data Word (Receive)

The DTI-PC/S issues a receive command to the RT using a mode code specified in MIL-STD 1553B, followed by one data word. The command word and data word transmit in a contiguous fashion with no gap. After command and data word validation, the RT transmits a status word back to the BC.

Mode Command With Data Word (Broadcast)

The DTI-PC/S issues a receive command word with 11111 in the RT address field and a mode code, followed by one data word. The command word and data word transmit in a contiguous fashion with no gap. After message validation, the RTs with the broadcast option set the Broadcast Received Bit in the status word and do not transmit the status word.

Mode Command Without Data Word (Broadcast)

The DTI-PC/S issues a transmit command word with 11111 in the RT address field and a mode code. After command word validation, the RTs with the broadcast option set the Broadcast Received Bit in the status word and do not transmit the status word.

BC-to-RT Transfer (Broadcast)

The DTI-PC/S issues a receive Command Word One with RT 31 (11111) in the RT address field, followed by the specified number of data words. The command word and data words transmit in a continuous fashion with no gap. After message validation, RTs with the broadcast option set the Broadcast Received Bit in the status word and do not transmit the status word.

RT-to-RT Transfer (Broadcast)

The DTI-PC/S issue a receive Command Word One with RT 31 (11111) in the RT address field, followed by a transmit command to another RT (RT "X") using the selected broadcast of RT X. After command word validation, RT X transmits a status word, followed by the specified number of data words. The status and data words transmit in a contiguous fashion. After message validation, the RTs with the broadcast option (excluding RT X) set the Broadcast Received Bit in the status word and do not transmit the status word (Table 5-1).

Associated Mode Code	Function	Data Word	Broadcast
0	Dynamic Bus Control	No	No
1	Synchronize	No	Yes
2	Transmit Status	No	No
3	Initiate Self Test	No	Yes
4	Transmitter Shutdowns	No	Yes
5	Override Transmitter Shutdown	No	Yes
6	Inhibit Terminal Flag Bit	No	Yes
7	Override Inhibit Terminal Flag	No	Yes
8	Reset Remote Terminal	No	Yes
16	Transmit Vector Word	Yes	No
17	Synchronize With Data Word	Yes	Yes
18	Transmit Last Command	Yes	No
19	Transmit BIT Word	Yes	No
20	Selected Transmitter Shutdown	Yes	Yes

Table 5-1. Mode Codes

Remote Terminal Mode Of Operation

In the RT mode, the DTI-PC/S emulates a MIL-STD 1553B RT with up to 30 data subaddresses and two mode code subaddresses or 31 data subaddresses and one mode code subaddress. Changing RT emulation from one RT number to another RT number is software selectable. Additional DTI-PC/S boards may be installed in a PC host for multiple RT emulations.

Other RT features include:

- Buffering up to 128 receive and 128 transmit messages to the same subaddress. Over 2,000 messages can be stored when the board is set up for 64K words of RAM.

- Asserting an interrupt when a user-defined number of messages are reached or a specific subaddress is addressed.

- Storing data per subaddress in a first-in/first-out (FIFO) methodology with time tag.

RT Subaddress Response Block Structure

The RT data structure includes a subaddress response block that is linked to any associated data words (Figure 6-1). Each RT subaddress block includes the following four header words:

- Control Word
- Message Status Pointer
- Data List Pointer
- Reserved Word

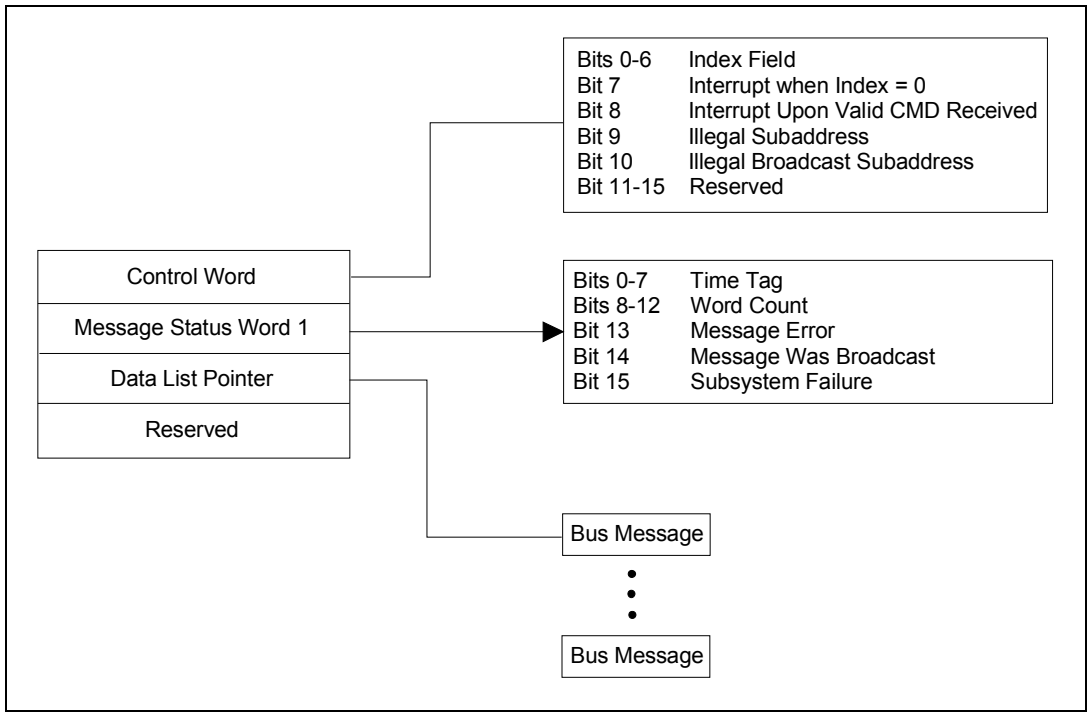


Figure 6-1. RT Subaddress Response Block

Control Word

The Control Word consists of 16 bits of information that select or disable message transfers as well as an index of the number of messages queued to each subaddress.

Bits 15-11 Reserved

Bit 10 Illegalize Broadcast Subaddress
If this bit is enabled, this subaddress is disabled for broadcast. If via the Standard Interrupt Enable Register (09), Illegal Broadcast Command Received events are enabled and a broadcast message references this subaddress, an Illegal Broadcast Command Received interrupt occurs. This interrupt sets the Message Error and Broadcast Command Received Bits in the status word, but does not transmit the status response onto the 1553 bus. The Broadcast Message and Message Error Bits in the message status word are set. Bit 10 identifies the RT subaddresses issued a broadcast, but disabled to receive broadcasts.

Bit 9 **Illegal Subaddress**
If this bit is enabled, the subaddress responds with the Message Error Bit set in the status. If via the Standard Interrupt Enable Register (09), Illegal Command Received events are enabled, this bit is set and a message involving this subaddress is transacted, an Illegal Command Received standard priority interrupt occurs. This interrupt sets the Message Error Bit in the message status word. No data is stored or transferred. Via this bit, you can determine if the bus message was sent to the correct RT subaddress or if the RT subaddress is "supposed" to be valid (indicating that the RT configuration may be incorrect).

Bit 8 **Interrupt Upon Valid Command Received**
If this bit is enabled, a Subaddress Event Interrupt standard priority interrupt occurs when this subaddress is addressed. Enabling this bit allows you to monitor activity to and from a specific subaddress.4.

Bit 7 **Interrupt When Index is Equal to Zero**
Used in conjunction with Bits 0 through 6 to define a subaddress event. If the index field changes from 1 to 0 and Bit 7 equals 1, a Subaddress Event Interrupt standard priority interrupt occurs. The host is notified when a particular RT subaddress is full, maximizing the integrity of stored data.

Bits 6-0 **Index**
These bits keep a running count of the number of messages stored per subaddress. When a message is stored to a subaddress, the particular subaddress index is decremented by 1. (This index is not decremented if an invalid command word is received or if the index field equals 0). Up to 128 messages can be stored for both RT transmits and receives per subaddress before overwriting occurs; however, total RT storage area for 64K words of RAM before service is required is over 2,000 32 data word messages. Upon the completion of each valid message, the Index Field (Bits 6 through 0) is decremented by 1 unless the index equals 0.

Message Status Pointer

The 16-bit Message Status Pointer specifies the location of the RT subaddress message status information.

Bit 15 **Subsystem Failure**
Indicates that the SSYSF signal was asserted just before the status word transferred to memory. This signal corresponds to Pin 2 of the external port.

Bit 14 **Broadcast Message**
Indicates that the broadcast message was received at this subaddress.

Bit 13 **Message Error**
This bit is set when any of the following errors occur: Word Count, Bit Count, Manchester II (including zero crossing deviation and rise and fall times), parity, data contiguity, illegal subaddress or illegal broadcast subaddress.

Bits 12-8 **Word Count**
Indicates the number of words stored from the transacted message.

Bits 7-0 **Time Tag**
Indicates when the message was recorded (in 64 microsecond increments). For example, if Bits 0 through 7 read 0000 0010 (binary), the message was completed 128 to 191 microseconds after the timer started. The timer is reset via Register 13.

Data List Pointer

Each time a bus message is sent to an RT, the data words are placed in the message queue for that particular subaddress (Figure 6-2). The data list pointer contains a 16-bit address of the next available location for storing incoming data. If the index field of the subaddress response block control word equals 0, the data list pointer is not incremented. The data last stored in the data buffer is overwritten.

If the index field of the subaddress block control word does not equal 0, the data list pointer moves to the next available data location when the message ends. If the data is erroneous, the pointer is not incremented past the position of the last valid data word stored.

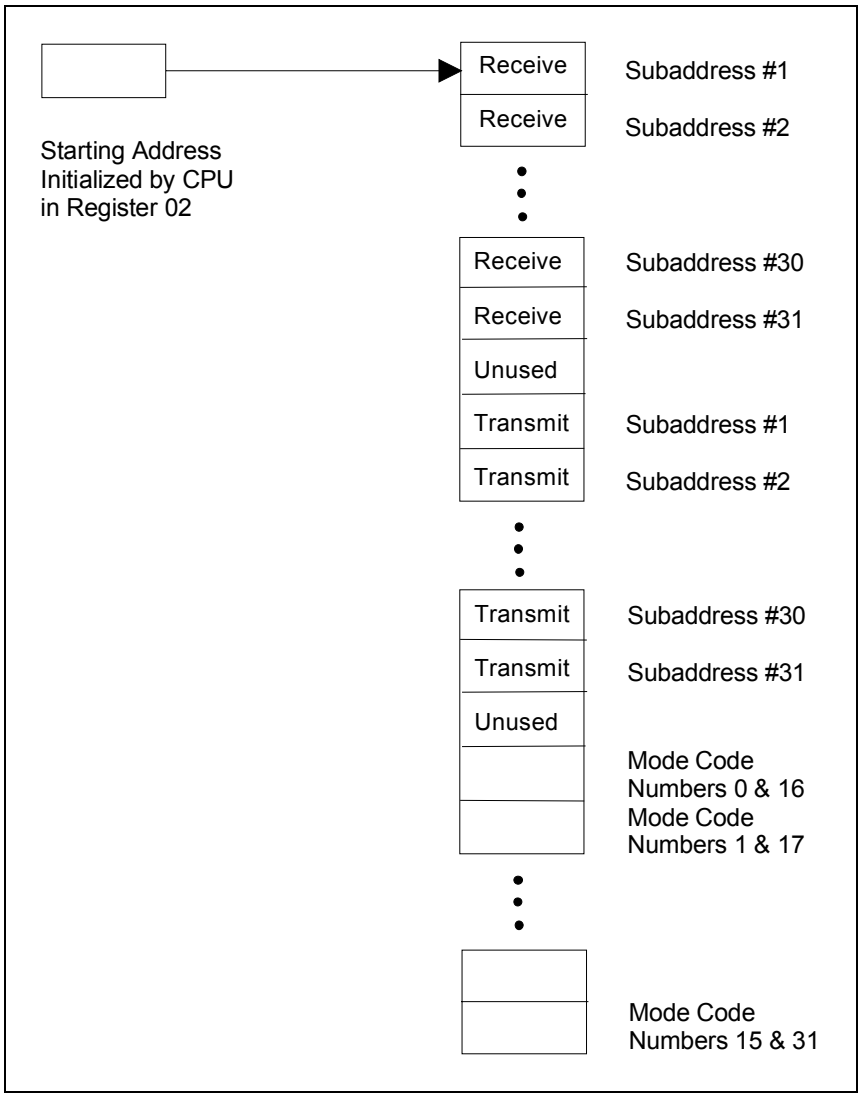


Figure 6-2. RT Subaddress and Mode Code Response Blocks

RT Subaddress Response Block Operation

When the BC requests a transmit, the RT's subaddress response block is read from the onboard RAM. The subaddress response block Data List Pointer points to the data buffer that contains the requested data words. The RT retrieves the requested data words from the specified data buffer and transmits the data words to the BC.

If the BC sends a receive command, the RT buffers data into a first-in/first-out indexed queue that stores up to 128 buffers per subaddress. Each buffer can store up to 32 data words. When a message is placed in the RT's queue, the message is automatically time-tagged.

You may count messages by noting the original value of the message status pointer. The message status pointer is incremented each time a message is received. Subtracting the previous message status pointer value from the current message status pointer's value gives you the number of messages received. (Example: Number of messages received = current pointer - previous pointer).

Note: Only data buffers with valid status conditions are queued; however, a valid command word (including words containing invalid data) generates a message status word, decrements the index and increments the message status pointer (providing index ≠ 0).

The number of messages stored in each queue may be monitored. To maximize data integrity, only the last message of the queue is overwritten when the buffer fills up. Interrupts may be generated when the buffer fills up.

RT Mode Code Response Block

Frequently, the instruction sent to an RT takes the form of a mode code. Table 6-1 displays the MIL-STD 1553B mode codes supported by the DTI-PC/S.

Associated Mode Code	Function	Data Word	Broadcast
0	Dynamic Bus Control	No	No
1	Synchronize	No	Yes
2	Transmit Status	No	No
3	Initiate Self Test	No	Yes
4	Transmitter Shutdowns	No	Yes
5	Override Transmitter Shutdown	No	Yes
6	Inhibit Terminal Flag Bit	No	Yes
7	Override Inhibit Terminal Flag	No	Yes
8	Reset Remote Terminal	No	Yes
16	Transmit Vector Word	Yes	No
17	Synchronize With Data Word	Yes	Yes
18	Transmit Last Command	Yes	No
19	Transmit BIT Word	Yes	No
20	Selected Transmitter Shutdown	Yes	Yes

Table 6-1. Mode Codes

Two mode codes share one block (Figure 6-3). For example, Codes 0 and 16 and 1 and 17 share one block. Each mode code block includes the following four header words:

- Control Word
- Message status pointer
- Data list pointer
- Reserved

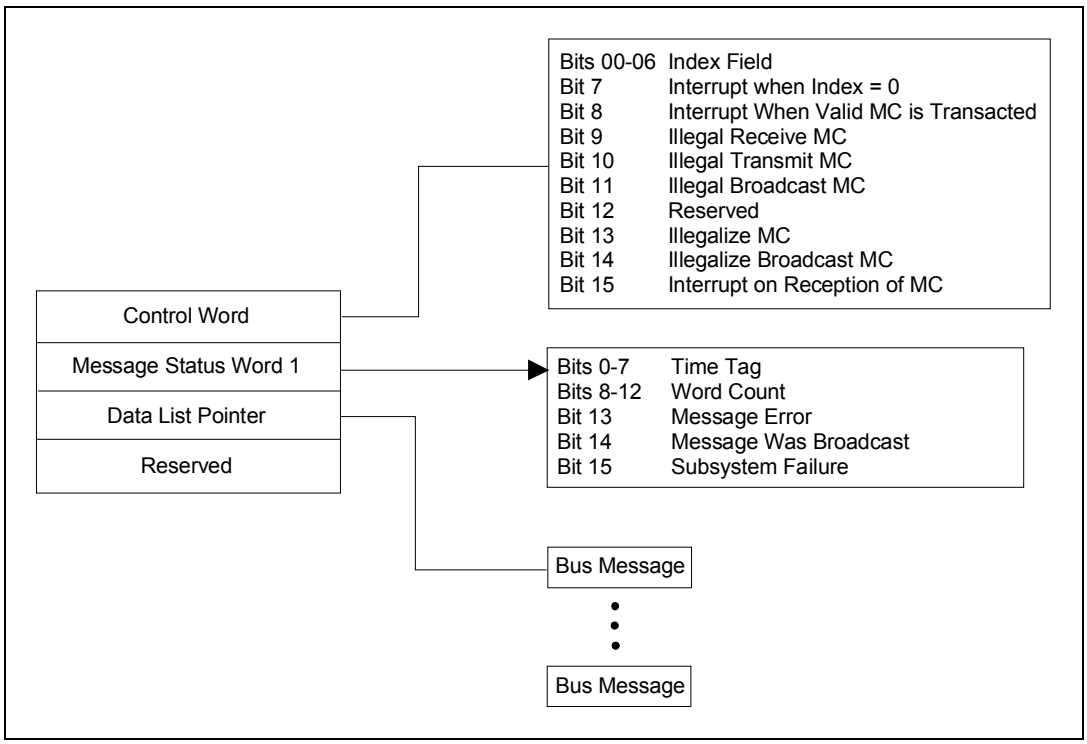


Figure 6-3. RT Mode Code Subaddress Response Block

Control Word

The mode code subaddress response block control word consists of 16 bits of response information that select or disable message transfers as well as select an index of the number of messages queued to each mode code with data. These 16 bits are divided into two parts:

- 0 - 15 refer to mode codes without data
- 16 - 31 refer to mode codes with data

Bit 15 **Interrupt on Reception of Mode Code (without Data Word)**
If this bit is enabled, the RT interrupts when this mode code is transacted. If this bit is set and the RT transacts this mode code without data, a Specific Mode Code Interrupt occurs.

Bit 14 **Illegalize Broadcast Mode Code (without Data Word)**
If this bit is enabled, the RT does not accept this Broadcast Mode Code. If via the Standard Interrupt Enable Register (09) Illegal Broadcast Command Received

events are enabled, this bit is set and the RT transacts this mode code, an Illegal Broadcast Command Received standard priority interrupt occurs. (This interrupt sets the Broadcast Command Received Bit and Message Error Bit in the message status word and status but does not send them onto the 1553 bus).

Bit 13 **Illegalize Mode Code (without Data Word)**
If this bit is enabled, the RT responds when a mode code without data is sent to the RT with the Message Error Bit set in the status. If via the Standard Interrupt Enable Register (09) Illegal Command events are enabled, Bit 13 is set and the RT transacts with mode code without data, a subaddress standard priority interrupt occurs. (This interrupt sets the Message Error Bit in the message status word).

Bit 12 **Reserved**

Bit 11 **Illegalize Broadcast Mode Code (with Data Word)**
If this bit is enabled, the RT does not accept a Broadcast Mode Code with Data Word sent to the RT. If via the Standard Interrupt Enable Register (09), Illegal Broadcast Command Received events are enabled, this bit is set, the RT transacts this mode code with data and this bit equals 1, an Illegal Broadcast Command Received standard priority interrupt occurs. (This interrupt sets the Broadcast Command Bit and Message Error Bit in the message status word and the status word, but does not send them onto the 1553 bus.)

Bit 10 **Illegalize Transmit Mode Code (with Data Word)**
If this bit is enabled, the RT responds to a Transmit Mode Code with Data Word sent to its mode subaddress with the Message Error Bit set in the status and no data word. If via the Standard Interrupt Enable Register (09), Illegal Command events are enabled, this bit is set and the RT transacts this mode code, an Illegal Command standard priority interrupt occurs. (This interrupt also sets the Message Error Bit in the message status word.) This bit notifies you of attempts to transact the broadcast mode code.

Bit 9 **Illegalize Receive Mode Code (with Data Word)**
If this bit is enabled, the RT responds to a Receive Mode Code with Data Word sent to its mode subaddress with the Message Error Bit set in the status. When this bit is enabled, a bus message has been sent to an illegal mode code with data in the receive direction. If, via the Standard Interrupt Enable Register (09), Illegal Command events are enabled, this bit is set, an Illegal Command standard priority interrupt occurs when the RT transacts this mode code with data (and also sets the Message Error Bit in the message status word). Mode codes may also be validated using this bit.

Bit 8 **Interrupt When Mode Code (with Data Word) is Transacted**
This bit allows an interrupt to be generated when this mode code with data is transacted. When the RT transacts this mode code with data a Subaddress Event Interrupt occurs. Enabling this bit, makes monitoring activity to/from a specific subaddress easy.

Bit 7 **Interrupt When Index is Equal to Zero**
Used in conjunction with Bits 6 through 0 to define a Subaddress Event Interrupt event. When Bits 6 through 0 change from 1 to 0 and Bit 7 equals 1, a

Subaddress Event Interrupt occurs. The host is notified when all message buffers of a particular mode code with data block fill up, maximizing the integrity of stored data.

Bits 6-0 Index
The maximum number of messages stored per mode code with data before overwriting occurs is 128. The initial value per mode code with data is user-definable up to 128. When a message is stored to a mode code with data block, the particular index is decremented by 1. This index is not decremented if an invalid command is received or if the index field equals 0.

Message Status Pointer

The Message Status Pointer links RT status information to each mode code with data word message. This 16-bit onboard RAM pointer specifies the location of the RT status information.

Bit 15 Subsystem Failure
This bit indicates that the SSYSF (subsystem failure) signal was asserted just before the status word transferred to memory. This signal corresponds to Pin 2 of the external port.

Bit 14 Broadcast Message
This bit indicates that the broadcast message was received at this subaddress.

Bit 13 Message Error
This bit is set when any of the following errors occur: Word Count, Bit Count, Sync, Manchester II (including zero crossing deviation, rise, and fall times), parity, data contiguity, illegal subaddress or illegal broadcast subaddress.

Bits 12-8 Word Count
These bits indicate the number of data words stored from the MIL-STD 1553B data bus transfer.

Bits 7-0 Time Tag
These bits indicate the time (in 64 microsecond increments) the message was recorded. For example, if Bits 7 through 0 read 0000 0010 (binary), the message was completed 128 to 191 microseconds after the timer started. The timer is reset via Register 13.

Data List Pointer

Each time a bus message is sent to an RT, it is placed in the message queue for that particular mode code with data. Any associated data words are linked via the data list pointer to the corresponding bus message.

The data list pointer contains a 16-bit address of the next available location for storing incoming data. If the index field (Bits 6 through 0) of the mode code block control word equals 0, the data list pointer is not incremented. The last stored data is overwritten.

If the index field of the RT response messages control word does not equal 0, the data list pointer is updated with the next available data location at the end of the message. If the data is erroneous, the pointer is not changed.

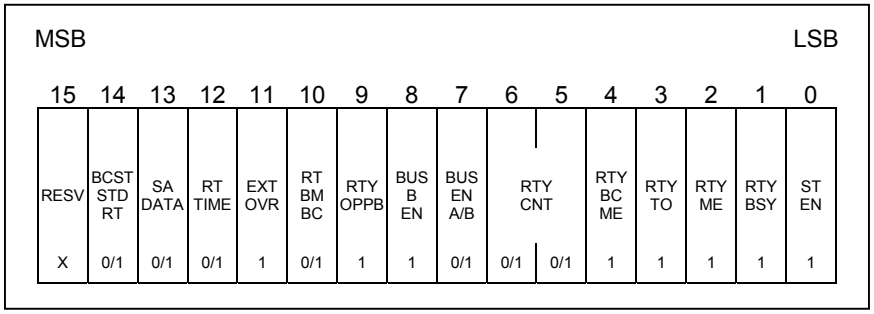
RT Registers

Two registers affect RT operations, the Control Register (00) and the RT Address Register (10).

Control Register (00)

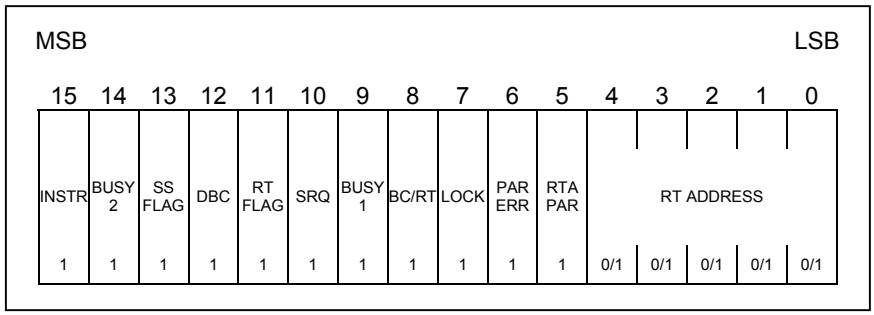
To start RT operations, set Bit 0 of the Control Register (00). To enable the 1553 buses in RT mode, set the following bits in Register 00:

- Set Bit 7 for Bus A.
- Set Bit 8 for Bus B.
- Clear Bit 10 for RT mode.



RT Address Register (10)

The Remote Terminal Register (10) sets the RT via software. The change lock-out enable feature, when set, prevents the RT address from changing.



Bit 15 **INSTR - Instrumentation (RT).**
Enables the Instrumentation Bit in the RT Status Word.

Bit 14 **BUSY2 - Busy.**
Sets the Busy Bit in the RT Status Word without inhibiting data transfers.

Bit 13 **SS FLAG - Subsystem Fail.**
Sets the Subsystem Flag Bit in the 1553B Status Word. In RT Mode, the Subsystem Fail is logged into the Message Status Word.

Bit 12 **DBC - Dynamic Bus Control Acceptance (RT).**
Allows the DTI-PC/S to accept Dynamic Bus Control and set the appropriate bit in the 1553B Status Word and the Status Register. Host intervention is required for the DTI-PC/S to take over as BC.

Bit 11 **RT FLAG - Terminal Flag (RT).**
Sets the 1553B Status Word Terminal Flag Bit. The bit in the 1553B Status Word is also internally set if the BIT fails

Bit 10 **SRQ - Service Request (RT).**
Sets the Status Word Service Request Bit.

Bit 9 **BUSY1 - Busy Mode Enable (RT).**
This bit sets the Status Word Busy Bit and inhibits all data transfers to the subsystem. The only possible DMA transfers are for the enabled events logged in the Interrupt Log List.

Bit 8 **BC/RT - BC/RT Mode Select.**
This bit indicates the internal BCRTSEL signal is set. This is not a useful bit, as it does not reflect the state of the BC/RT Mode Select Bit (Bit 10 of Register 00).

Bit 7 **LOCK - Change Lock-Out.**
Change Lock-Out Enable. When set, this bit prohibits changes to the RT Address or the BC/RT mode select, using internal registers.

Bit 6 **PAR ERR - RT Address Parity Error.**
This bit indicates an RT Address Parity Error. It appears after the RT Address is latched, if a parity error exists.

Bit 5 **RTA PAR - RT Address Parity.**
This is an odd parity used with the RT Address. It ensures accurate recognition of the RT.

Bits 4-0 **RT Address**
Modify the RT Address by writing to these bits. Must be written after reset.

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Bus Monitor Mode Of Operation

As a bus monitor, the DTI-PC/S monitors all RTs or a select number of RTs and their subaddresses. Changing RT monitoring from one RT number to another is software-selectable.

Using dual-port RAM, the DTI-PC/S monitors, time tags and stores over 1,000 messages of 32 data words each without host intervention.

The BM also detects the following errors:

- Response Time Out
- Long and Short Word Count
- Bit count
- Manchester II
- Parity

Bus Monitor Message Blocks

The BM Message Record Blocks, which resemble the BC Command Blocks described in the BC section of this manual, contain the data recorded for the RTs and subaddresses. Each Message Record Block consists of seven 16-bit words (Figure 7-1).

The Message Record Blocks are linked through the tail pointer so that either the entire list or a portion of the list of Message Record Blocks can be rewritten.

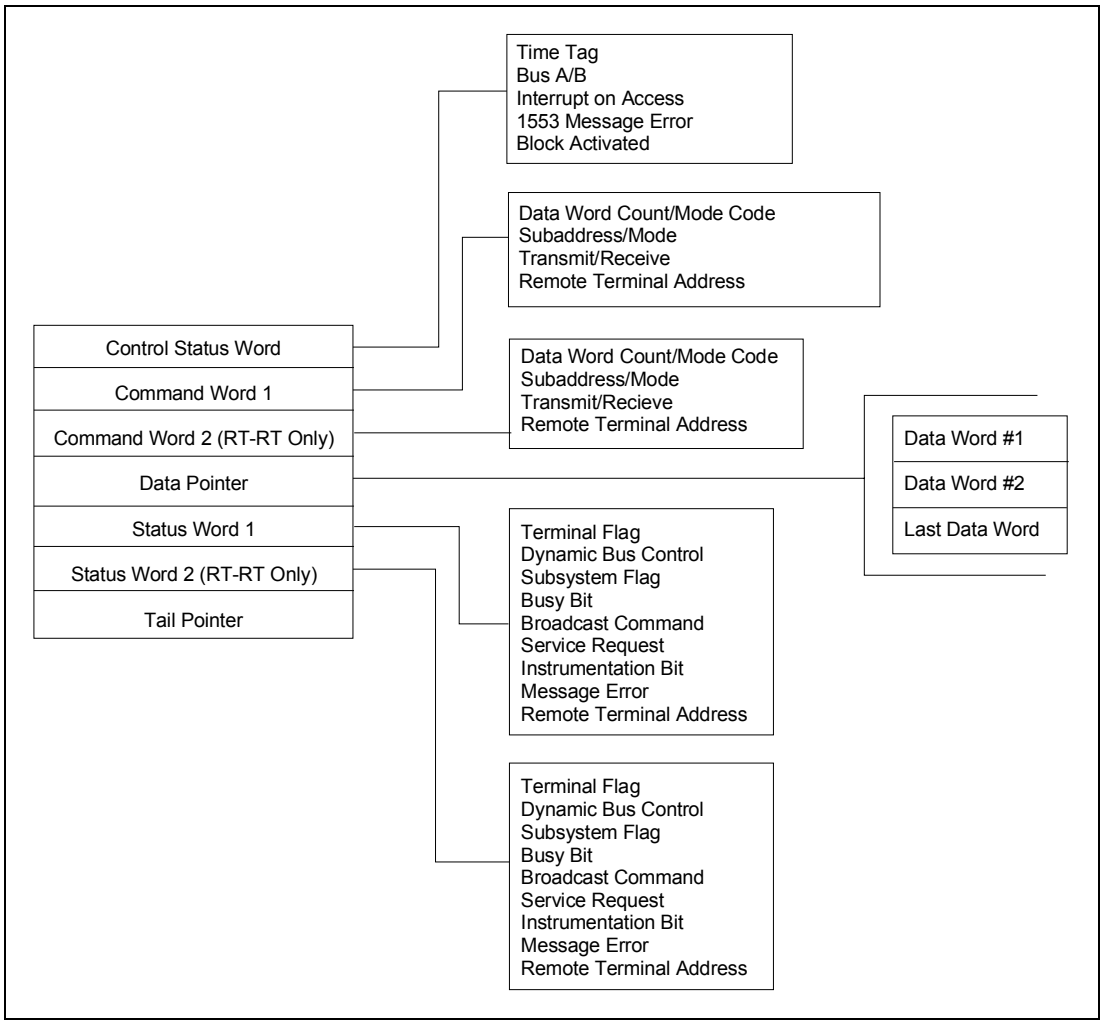


Figure 7-1. BM Message Record Block

Control/Status Word

The 16 bits of the Control Word perform the following functions:

- Time Tagging
- Bus Indicator
- Interrupt Upon Access
- Message Error
- Message Record Activated

Bit 15 **Message Indicator**

If this bit is set, the block contains a 1553B message. This bit indicates if data has been written to the message record block. Each message record block has one data buffer. Reserve space in memory, before monitoring begins, for the maximum number of data words to appear in any message. If sufficient memory is not allocated for the data buffers, some data words may be overwritten by sequential messages.

Bit 14 **Message Error**
If the 1553B message contains an error, this bit is set.

Bit 13 **Interrupt On Access**
If set, this bit enables an Interrupt On Access to the particular message record block. This bit can be used to generate an interrupt when the first message is received or generate an interrupt every n messages (n is a multiple of the total number of message record blocks). If you set an interrupt after five messages, you receive an interrupt at the end of the 10th, 15th, 20th interrupt .

Bit 12 **Bus Indicator**
This bit specifies on which bus the message was received. 1 = Bus A. 0 = Bus B.

Bits 11-8 **Reserved**

Bits 7-0 **Time Tag**
These bits indicate the time (in 64 microsecond increments) the message was recorded. For example, if Bits 7-0 read 0000 0010 (binary), the message was completed 128 to 191 microseconds after the timer was reset. The timer is reset via Register 13.

Command Word One

Used for all 1553B transfers, Command Word One contains the RT address, T/R Bit, subaddress and the word count or mode code. The first command of an RT-to-RT message type is a receive command.

Command Word Two

Command word Two, used during RT-to-RT transfers, contains the second command for RT-to-RT transfers. This word contains the transmitting RT address, subaddress and the word count. Command Word Two is not used in single RT transfers.

Data Pointer

The Data Pointer is a 16-bit word that points to the onboard RAM starting location of the DTI-PC/S dual-port RAM, where the data buffer of the current message record block resides. The number of data words per message record block instruction is 32 or less. You must initialize the pointer each time you want to use it.

Status Word One

Status Word One contains either an RT Status Response for a BC-to-RT transfer or an RT-to-BC transfer, a status word of MIL-STD-1553B Mode Code transfer or and RT Transmit Status for an RT-to-RT transfer.

Status Word Two

The 16 bits of this word contain the receiving status in RT-to-RT transfers. If RT-to-RT transfers do not occur, the word is not used.

Tail Pointer

The 16 bits of the tail pointer contain the onboard RAM starting address of the next sequential message record block.

Initializing Data Buffers

If memory is cleared, all data buffers contain 0s.

Loading Bus Monitor Registers

The Bus Monitor Control Register (14) and the Bus Monitor Terminal Address Select Registers (16 and 17) control the bus monitor. The loading of these and other registers that affect the BM is described in the following sections.

Bus Monitor Control Register (14)

Bit 15 of this register enables the BM . Bits 13 and 14 determine if selected RTs or all RTs respectively are to be monitors. (Bit 15 is used in conjunction with Bit 10 of Register 00 being cleared in RT mode). Bit 15 of Register 14 is cleared by a WRITE to Register 12 (Reset Command Register).

Note: If Bit 10 is set (BC mode) and Bit 15 is set, unpredictable results may occur.

Bus Monitor Terminal Address Select Registers (16 and 17)

These registers determine the RTs to be monitored. Bits 0 - 15 of Register 16 select RT addresses 0 through 15. Bits 0 - 15 of Register 17 select RT addresses 16 through 31. (These registers are unused when Bit 14 of Register 14 is set to monitor all RTs).

Interrupt Queue Pointer Register (06)

If interrupt blocks are to be generated, the onboard RAM location of the top of the interrupt queue is written to this register.

Next Message Record Block Register (02)

The onboard RAM address of the start of the message record block is written to this register. As messages are captured, the contents of this register are automatically updated to point to the next message record block to be used.

Control Register (00)

The Start Bit of this register is set to begin execution of the message record blocks. Either or both buses (Bit 7, Bus A = 1. Bit 8, Bus B = 1) can be enabled for monitoring.

High Priority Interrupt Enable Register (07) and Standard Interrupt Enable Register (09)

Interrupts are enabled/disabled by writing to these registers.

Reset Timer Register (13)

This register resets the bus monitor time tag counter to 0.

Remote Terminal Address Register (10)

Bit 6 must be cleared to 0 prior to starting the bus monitor.

Collecting Data

To ensure data stored in memory is not overwritten, write data to disk and generate interrupts during message intervals. For example, you have 2,000 Message Record Blocks with an interrupt generated every 500 blocks. (The Interrupt Bit for Blocks 500, 1,000, 1,500 and 2,000 is set. If, upon interrupt, a message is stored in any of the blocks, the present block and the previous 499 blocks are written to disk.

The Message Record Blocks and data buffers maintain a one-to-one relationship. The order of your memory might be:

Message Record Block 1	or	Message Record Block 1
Message Record Block 2		Data Buffer 1
Data Buffer 1		Message Record Block 2
Data Buffer 2		Data Buffer 2

Post-Run Processing

Interrupts are generated so that the user can examine each message. The nature of each interrupt should also be examined to determine if an interrupt was expected and if not, why did an interrupt occur?

Look for the following important information in the Message Record Block:

- Bit 15 of the control word is set and the block contains a message.
- Bit 14 of the control word is set and a message error has occurred.
- Bit 12 of the control word is set and the message has been transmitted on Bus A.

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