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GLD-PC

Hardware Reference Manual

Document No. T-T-MR-GLXXA###-A-0-A4

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1. INTRODUCTION

1.1 How To Use This Manual

1.1.1 Purpose

This manual describes the GLD-PC (multi-function) hardware product; its configuration, modes of operation, output signals, timers, memory, interrupts and registers. It describes how to unpack, set up, and install the hardware.

1.1.2 Scope

This information is intended for systems designers, engineers and MIL-STD-1553 network installation personnel. You need an understanding of MIL-STD-1553 networking, hardware installation and operation to effectively use this manual.

1.1.3 Style Conventions

- Hexadecimal values are written with "0x" preceding the value; for example, 0x03FF.
- Switch, signal and jumper abbreviations are in capital letters; for example, RSW1, JP5, etc.
- Buslist instruction names are in capital letters; for example, NO-OP, JUMP, etc.
- Bit values are shown in single-quotes; for example, Set bit 15 to '1'.

1.2 Related Information

- *GLD-PC Interface Library for DOS*
  (Document No. T-T-ML-GLDXA)
- *GLD-PC Interface Library for Windows 3.1*
  (Document No. T-T-ML-GLWNA)

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- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

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2. PRODUCT OVERVIEW

2.1 Overview

The GLD-PC multi-function board provides a powerful and convenient interface between a host computer and a MIL-STD-1553 data bus. The GLD-PC enables the host to simultaneously operate in real-time as a MIL-STD-1553A or B protocol Bus Controller (BC), Multiple Remote Terminal (MRT) and Chronological Monitor (CM). The GLD-PC provides the host with complete access to data received or transmitted on the bus and the ability to detect bus errors.

The GLD-PC uses a high-speed controller in conjunction with Dual-Port Random Access Memory (RAM) to provide a complete, intelligent emulation system. Using on-board data structures located in the Dual-Port RAM, the board can sustain operation on the bus without host intervention. In addition, the CM stores commands, status responses, gap times and time tags within the same buffer.

2.2 Single/Dual Channel Configuration

The GLD-PC is offered as a single (1A and 1B bus) or dual (2A and 2B buses) channel configuration. The dual-channel configuration provides all of the functionality of two single GLD-PC boards and twice the amount of on-board dual-port RAM. Each channel contains 32 K of dual-port RAM and may be mapped to one area of memory or two different areas of memory.

2.3 Modes of Operation

The GLD-PC can operate in BC, MRT and CM modes simultaneously or independently. All MIL-STD-1553A or B protocol communication between emulated devices occurs over the 1553 bus, rather than through a local bus. The three operating modes provide extensive bus protocol error detection, such as parity error and no response.

2.3.1 Multiple Remote Terminal Mode

Using 32 K words of Dual-Port RAM, the GLD-PC can receive, store and count approximately 750 bus messages of 32 data words each. Bus messages are transmitted and received without host intervention. The RT can generate an interrupt when a message buffer transmits or receives data and enabling specific subaddresses and mode codes. RT's can be programmed individually for 1553A or B protocol.

The MRT mode can inject the same errors as the BC mode. These errors are programmed at the subaddress level. An error can be injected once or continuously.

2.3.2 Bus Controller Mode

The BC mode defines, stores and executes comprehensive lists of bus instructions. The GLD-PC efficiently addresses up to 32 RTs (31 RTs and one Broadcast RT, RT 31 in 1553B mode). The BC can generate and process any valid type of MIL-STD-1553A or B protocol message:

- BC-to-RT Transfer
- RT-to-BC Transfer
- RT-to-RT Transfer
- Mode Command Without Data Word
- Mode Command With Data Word (Transmit, 1553B mode only)
- Mode Command With Data Word (Receive, 1553B mode only)
- Broadcast commands (1553B mode only)

The BC can inject a variety of errors for each transmission on the MIL-STD-1553 bus. These errors are specified as a part of each buslist instruction and may be individually enabled or disabled. An error can be programmed to be injected once or continuously (each time a message is sent).

2.3.3 Chronological Monitor Mode

The CM mode captures all or selected traffic. The GLD-PC can monitor traffic while simultaneously acting as a BC and/or one or more RTs. Data transfers may be filtered down to the subaddress level. Mode commands can be selectively monitored down to individual mode codes.

2.3.4 Error Detection

The GLD-PC can detect a variety of protocol and electrical errors. Errors detected in the BC mode fall into one of three categories:

- Protocol violation
- Status exception
- No response.

Subsection 4.2.4, Error Response, explains in more detail how the Bus Controller mode handles errors. In the MRT mode, protocol errors are noted in any interrupt packet, and the RT will take appropriate response, according to MIL-STD-1553A or 1553B protocol definition. In the Chronological Monitor mode, errors detected include parity and high and low bit count. All other errors are grouped together and indicated in the Tag Word. See Chapter 6, CM MODE OPERATION, for details.

2.4 Discrete RS-422 Signals

The GLD-PC is equipped with an RS-422 port. This port provides a Discrete Output Signal (DOS) with two-microsecond duration, which may be programmed to signal the start of any buslist instruction. The port also allows for input of an external elapsed timer (ELT) clock and reset signal, as well as a start trigger for the BC mode.

Table 2-1 summarizes the discrete available signals. See Section 3.8, RS-422 Port Option, for details on accessing these signals.

Table 2-1 Discrete Signals

Signal Name	Direction	Mode Affected
BC Start Trigger	Input	BC
Discrete Output Signal	Output	BC
Ext. Elapsed Timer Reset	Input	CM
Ext. Elapsed Timer Clock	Input	CM

2.5 Separate Elapsed Timers

The GLD-PC has two on-board 32-bit elapsed timers. One timer is used for bus controller intermessage timing while the other tracks absolute simulation time for the chronological monitor and RT time stamping. Each timer has a one-microsecond resolution.

2.5.1 On-board Dual-Port RAM

The GLD-PC Dual-Port RAM allows host access to share data and structures without 1553 process interference. Application programs can use the Dual-Port RAM for variables and data structures residing in the host's main memory. Storing all data in the Dual-Port RAM eliminates the need for continuous host bus support of MIL-STD-1553 activity.

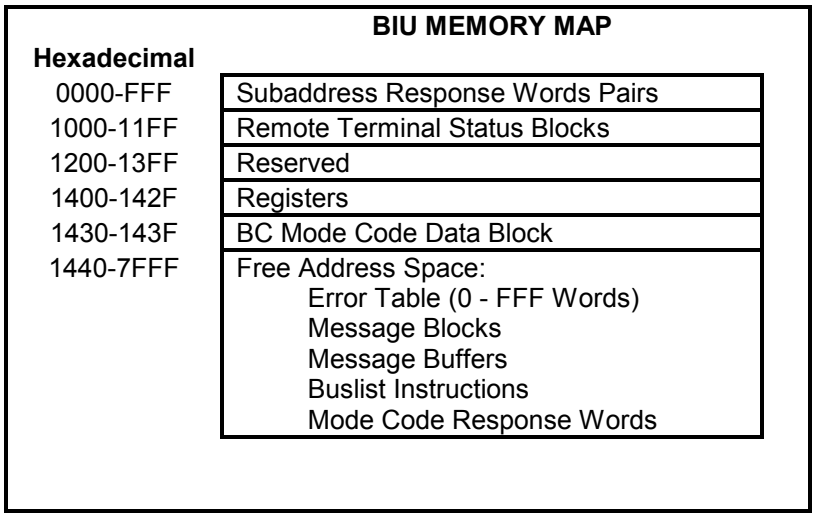


Figure 2-1 GLD-PC Memory Map

2.5.2 Board Configuration

Microcode must be loaded to each channel before the board can be used. A microcode-load application shipped with the board loads the microcode for the on-board processor. After this has been successfully accomplished the 1553 data structures must be defined. These structures configure the 1553 modes for simulation and/or monitor of the 1553 bus. Once the microcode is loaded, it sets a default condition of MIL-STD-1553B timing and protocol.

The Dual-Port RAM contains the area required for data structure storage. The RAM is broken down into many different areas, including areas for RT configuration, subaddress configuration, MIL-STD-1553A or B protocol data buffers and CM buffers. With a dual-channel model each channel must be treated as if there were two cards in the system. Each channel is fully independent, sharing only the host bus buffering chips.

2.6 Interrupt Handling

An interrupt notifies the host that a specific condition (such as a message buffer access, a BC instruction execution, or a 1553 error) has occurred.

Because of interrupt latency and host processing speed, multiple interrupts may be generated while the host is processing an interrupt. To preserve the integrity of all enabled events, the GLD-PC continuously buffers interrupt events from within the Interrupt Queue. The interrupt queue can hold up to 36 14-word interrupt packets and resides at memory addresses 1200 to 13FF.

2.7 Registers

Each channel of the GLD-PC has three register spaces:

- I/O space. The Configuration Registers are for user I/O functions and must be mapped into the host I/O space.
- Memory space. The Real-Time Control Registers provide important information, such as operating mode status and control.
- Function Registers. A subset of the Real-Time Control Registers that controls certain board functions. For example, buslist execution.

For details, see Appendix C, REGISTERS.

3. INSTALLATION

3.1 Overview

This chapter provides step-by-step instructions on the unpacking, setup, and connection of the board; software installation, board initialization, and 1553 function programming.

3.2 Unpack and Inspect the Board



NOTE: The hardware board is shipped in a protective anti-static bag. Do not remove the board from the anti-static package until properly grounded or damage to the board may occur.

Remove the board from the packing box and the protective bag. Place the hardware board on top of the protective bag or on an electrostatically controlled work surface. If the board appears to be damaged, contact Systran immediately at: **(800) 252-5601** or send an e-mail message to **support@systran.com** for additional assistance.

Save the packing materials for possible use in the future.

3.3 Set the Hardware Switches

The channel I/O Address rotary switches are located near the upper middle section of the board Figure 3-1). These rotary switches define the Initialization Registers for each channel on the card. (See Appendix C: REGISTERS, for more information.)

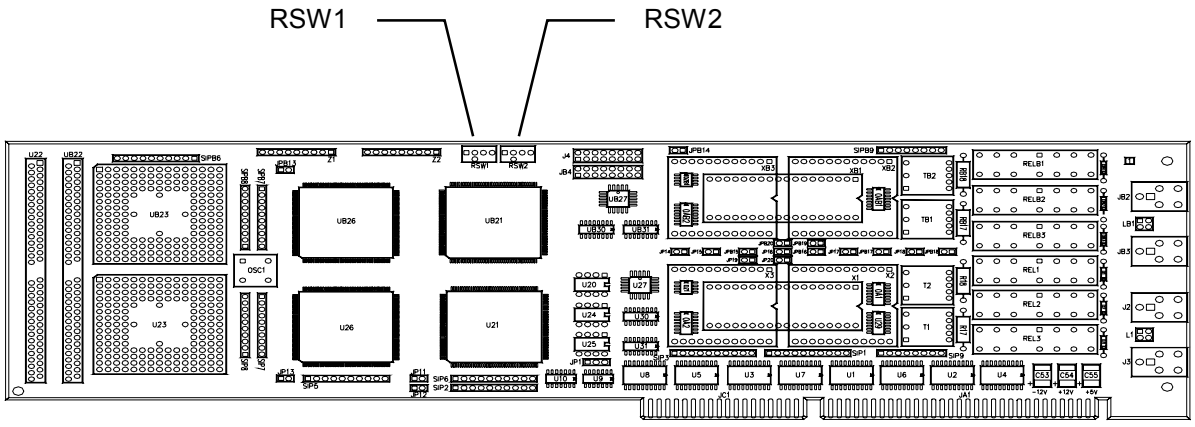


Figure 3-1 GLD-PC Board

Rotary Switches 1 (RSW1) and 2 (RSW2) are factory set at 0x0100 (Figure 3-2). The GLD-PC I/O Address ranges from 0x0000 through 0x07C0 bytes although the ISA specification only allows valid addressing between 0x0100 to 0x03FF.

NOTE: Systran recommends switches 1 and 2 be set to 0x300, 0x100 or 0x200 for I/O addressing. Consult your system configuration documentation to select a free 32-word (64-byte) address space before setting these switches. For dual-channel boards, both channels will be addressed in this 32-word block. The first channel initialization registers will always start from the switch setting base and extend to 0x0F offset from this. If a second channel is present, it will exist at an offset of 0x10 up to 0x1F.

Using a blade screwdriver, turn the arrow clockwise until it points to the desired hexadecimal character.

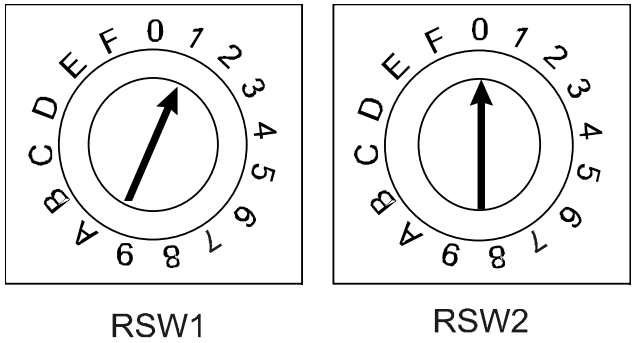


Figure 3-2 I/O Address Rotary Switches 1 and 2

0	1	0	0

3.4 Locate Fail-Safe Timer Jumpers

Jumpers JP13 and JPB13 control the transmit Fail-Safe Timer. This timer allows an interrupt to be generated after 720 µs of continuous bus transmission. This interrupt also disables the transmitter from further use. The factory setting enables the timer. Installing jumpers JP13 and JPB13 disables the Fail-Safe Timer. Use Figure 3-3 to locate the jumpers.

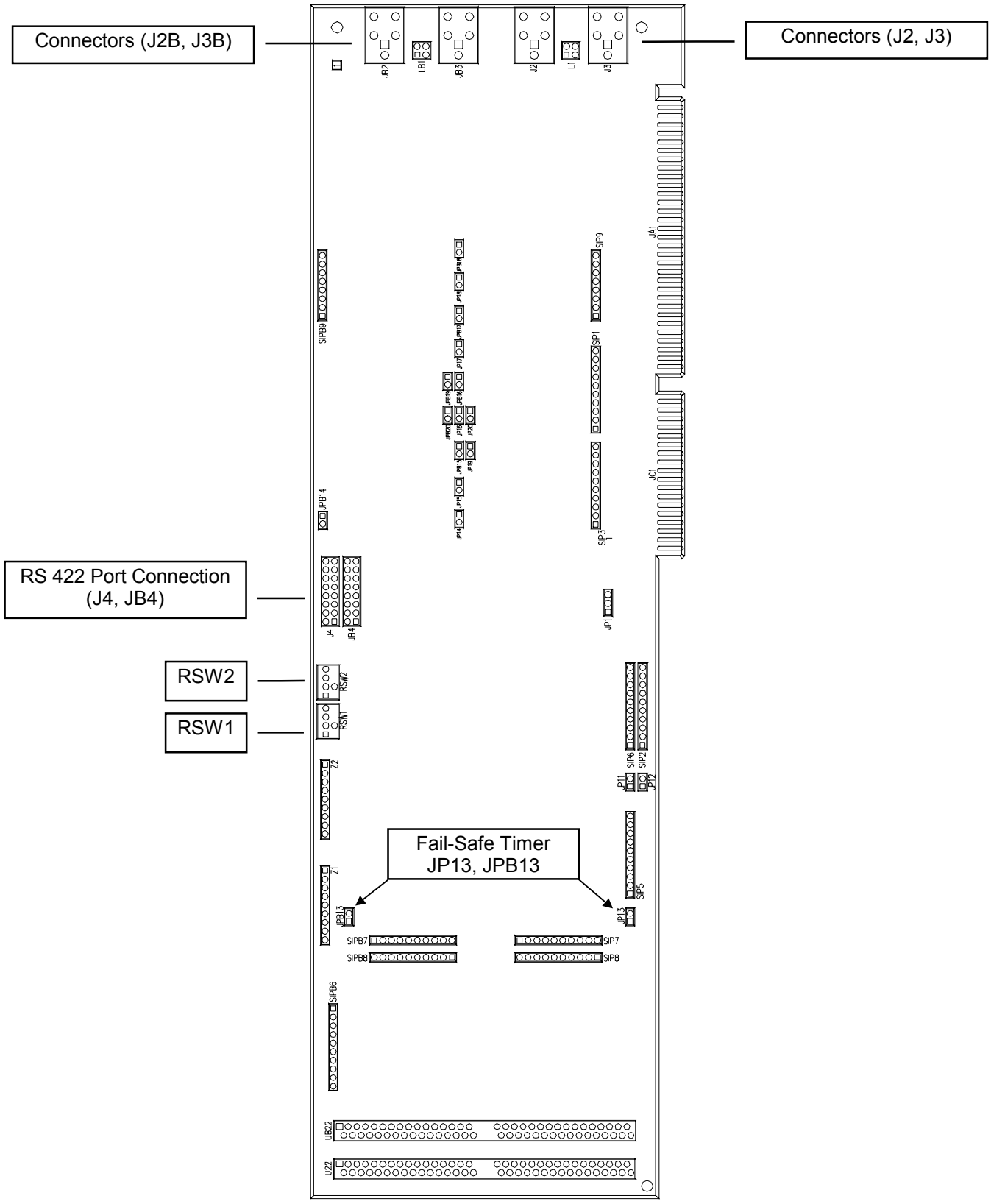


Figure 3-3 GLD-PC Board

3.5 Locate the Connectors

The GLD-PC uses subminiature triax jacks, to connect the GLD-PC to the 1553 bus (Figure 2-3). With the board oriented as in Figure 3-4, these connectors can be found at the right side of the board. Channel 1 is the bottom set of jacks (J2, J3) and if a second channel is present, Channel 2 is the top set (JB2, JB3). Bus A is the top jack of each set.

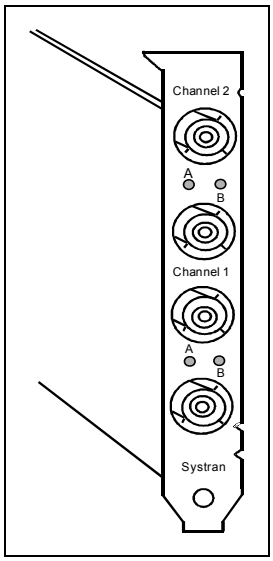


Figure 3-4 Channel 1 and Channel 2 (Dual-channel Board Only) Connector Locations

3.6 Install Board In The Host



CAUTION: Ensure power is off before installing the board.

1. Identify the location of the 16-bit slot in the PC-AT where the board will be installed. Remove the cover and open the back of the system.
2. Wearing an anti-static wrist strap, position the board over an available slot in the host.
3. Push down firmly on the board until it locks into place.
4. Secure the front panel with a single screw.
5. Apply power to the board by turning on the system.

3.7 Select Direct or Transformer Coupling

The GLD-PC can be connected to the MIL-STD-1553 bus via a Direct or Transformer connection.

- Direct Coupling can be used if the distance between the GLD-PC and the MIL-STD-1553 bus is 12 inches or less.
- Transformer Coupling can be used between the GLD-PC and the MIL-STD-1553 bus for any distance up to 20 feet.

An external Coupling Box is required if Transformer coupling is selected. In any case, it is important that the bus be a valid, properly terminated configuration.

To change the type of coupling, change the coupling relay configuration (Relay Register 0x1A).

CAUTION: Regardless if the board is Direct or Transformer coupled, both 1553 buses (BUSA and BUSB) must always be terminated properly! System errors may occur on the various devices if the board is not properly terminated.

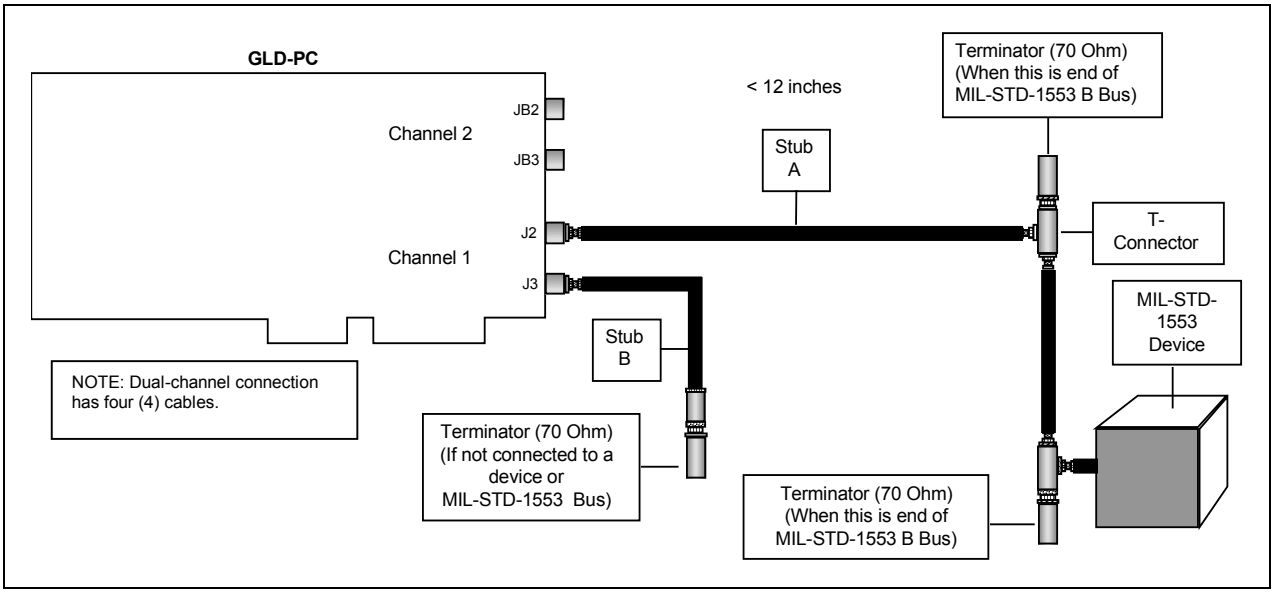


Figure 3-5 Direct Coupled MIL-STD-1553A or B Protocol Bus

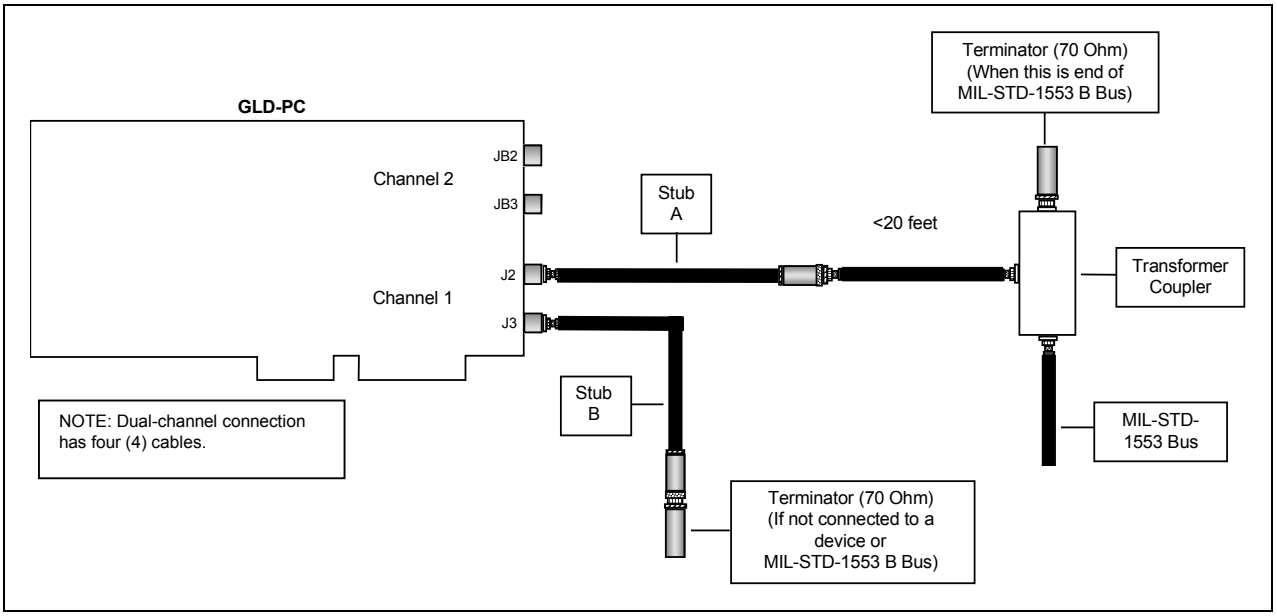


Figure 3-6 Transformer Coupled MIL-STD-1553A or B Protocol Bus

3.8 RS-422 Port Option

The GLD-PC comes equipped with an RS-422 port (J4, JB4). The 16-pin port is defined as follows:

Table 3-1 The RS-422 Port Pin Assignments

Pin	Description
1	ELT RST +
2	ELT RST -
3	ELT CLK +
4	ELT CLK -
5	DOS +
6	DOS -
7	NC
8	NC
9	START BC +
10	START BC -
11	NC
12	NC
13	NC
14	NC
15	NC
16	NC



NOTES:

1. Do not drive pins designated as having no connection (NC).
2. Setting Bit 0 in Word 0 of any BC buslist instruction enables the Discrete Output Signal. See Chapter 4, BC MODE OPERATION for details.
3. The BC Start Trigger Input (START BC+, START BC-) is used in conjunction with the BC Pause instruction. This signal allows you to control the execution of the buslist externally. See Chapter 4, BC MODE OPERATION for details.
4. The ELT CLK signal must not be faster than 1 µs per cycle (1 MHz)

Connector J4 is used with Channel 1, and Connector JB4 is used with Channel 2 if the GLD-PC board is equipped with two channels. The orientation of each connector is shown in Figure 3-7.

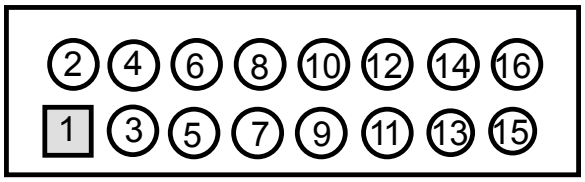


Figure 3-7 Connectors J4 and JB4 Orientation

3.9 Power On The System

After the board and the MIL-STD-1553 connection are properly installed, switch on the system. Use the diagnostics software to complete the hardware tests. See the *GLD-PC Hardware Confidence Test Manual* for more information.

3.10 Load Microcode

The microcode must be loaded to each channel before the board can be used. See subsection 2.5.2 Board Configuration.

3.11 Software Installation, Configuration and Operation

Refer to the *GLD-PC Interface Library* and the *GLD-PC Hardware Confidence Test (HCT) Manual* to perform the following procedures:

- Install software.
- Load the microcode.
- Initialize the channel.
- Program 1553 functions.
- Run the channel.

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4. BC MODE OPERATION

4.1 Overview

The GLD-PC can be programmed to operate in the BC mode to emulate all message types defined by MIL-STD-1553A or B. Any series of commands, either valid or invalid, can be sequenced as needed. A sequence of commands that the BC mode executes is called a buslist. Multiple buslists may be constructed and called up by the host in real-time.

The BC mode operates by executing a series of buslist instructions contained in the Dual-Port RAM. The instructions include those allowing generation of all MIL-STD-1553 message types, as well as NO-OP, HALT and JUMP instructions for framing of messages. The BC mode can operate simultaneously with the MRT and CM modes.

4.2 BC Features

4.2.1 Timers

The GLD-PC has two timers - The BC Delay Timer and the Chronological Monitor's Elapsed Timer (ELT). See Chapter 6, CM MODE OPERATION, for a description of the Elapsed Timer.

BC-DELAY TIMER

This timer is used to control the major and minor frame timing of buslists. It is a 32-bit timer with one-microsecond resolution. It starts upon execution of the first bus instruction in the buslist.



Frame Timing – The BC mode is started by writing to the BC Control Register. The time between starting the BC mode and the actual execution of the first instruction varies, depending on the instruction. For best frame-timing accuracy when introducing a delay in the buslist, reset the BC Delay Timer (by setting the appropriate bit in the last bus instruction) and then delay *n* microseconds using the Delay BC instruction in the Interface Library. The BC minimum inter-message gap time is approximately 20 microseconds.

4.2.2 Discrete Output Signals

The BC mode allows interaction with two discrete RS-422 signals:

- The Discrete Output Signal: This signal can be enabled on any bus instruction by setting bit 0 of the bus instruction to '1'. This signal is active for 2 ms and occurs before the command is placed out on the 1553 bus.
- BC Start Trigger: The board allows an external RS-422 pulse to trigger the execution of the buslist. This signal can work in conjunction with the PAUSE instruction.

If the Discrete Out Signal Bit and the Delay Timer Reset Bit are both set for a buslist instruction, the GLD-PC generates the Discrete Out Signal prior to the Delay-Timer Reset.

4.2.3 Interrupts

In BC mode, hardware interrupts may be posted to the host when certain event interrupts occur. (See Appendix B, INTERRUPTS, for details.) All interrupts may be selectively enabled or disabled under control of the applications software, except for a BC HALT. HALT interrupts are always enabled whether it is a buslist instruction or an asynchronous halt (BC Control Register write of 0x0000).

4.2.4 Error Response

In actual 1553 applications, specific transmitting or receiving errors indicate problems. As in the case of the BC, each data-transfer command or mode code can be programmed to take a specific action if a protocol error is detected on the 1553 bus. The available actions include:

- No Retry
- Retry Once on the Same Bus
- Retry Once on the Opposite Bus
- Retry Once on the Same Bus (If unsuccessful, retry once on the opposite bus.)

In the action "Retry Once on the Opposite Bus," the instruction may specify that if the retry on the opposite bus is successful, the primary bus should be switched to the opposite bus.

4.2.5 Protocol Errors and Status Exceptions

MIL-STD-1553A or B Protocol errors are detected when RTs do not respond or respond with a message error bit set in the status word. Protocol errors include:

- No Response (the RT does not respond).
- Manchester or parity error occurs in RT transmission.
- The RT address field of the RT's status word does not match the RT address field of the command word.

Status exceptions are detected when a bit other than the address field is set in the RT's status word.



NOTE: The GLD-PC cannot simulate or handle the superseding valid command function in BC mode.

4.3 Buslist Instructions

Any number of buslists can be defined within the Dual-Port RAM. The GLD-PC executes these lists once the starting address is written to the BC Control Register. A buslist can be defined for each simulation allowing minimal host intervention during real-time simulation. A HALT instruction terminates the buslist. During simulation, the GLD-PC updates BC data in the Dual-Port RAM, continues execution of the appropriate buslist instructions, and ensures 1553 bus traffic conforms to MIL-STD-1553A or B specifications.

When the emulated BC is commanded to start, it reads instructions from a buslist and executes them sequentially until the BC encounters a HALT or JUMP instruction. If the BC is programmed to stop on errors, it will halt when it encounters an error condition.

A buslist instruction block is made up of four 16-bit words. Bits 12-15 of Word Zero of an instruction block identify the instruction type (0-0xA).

The Discrete Out Signal (DOS) may be generated by the BC to signal the start of the desired command. This signal is enabled or disabled by Bit 0 of Word Zero of each buslist instruction block. The signal is active for 2 μs and occurs before the command is placed out on the 1553 bus.

4.3.1 Types of Buslist Instruction Blocks

The following buslist instruction blocks are assigned a *hex*adecimal number:

#	Buslist Instruction Block
0x0	NO-OP
0x1	JUMP
0x2	HALT
0x3	MODE CODE
0x4	BC-TO-RT TRANSFER
0x5	RT-TO-BC TRANSFER
0x6	RT-TO-RT TRANSFER
0x7	HALT UNTIL DELAY
0x8	RESET STACK
0x9	INTERMESSAGE DELAY
0xA	PAUSE
B-0xF	Reserved

Other parameters in a buslist instruction block depend on the block type. Buslist instruction blocks are stored in memory locations from 0x1440 - 0xFFF.

4.3.2 Bit Ordering

Bit 15 is the most significant bit and bit 0 is the least significant bit.

4.3.3 NO-OP (Instruction 0x00)

The NO-OP instruction can be used as a placeholder instruction. It can be inserted or removed to change the buslist without re-structuring the entire sequence. The BC proceeds to the next buslist instruction block in approximately four microseconds. Adding interrupt, Delay Timer reset and Discrete Out signaling will increase this time. If the NO-OP Interrupt Enable Bit (Bit 11) is set to 1, the BC posts a NO-OP Interrupt before proceeding to the next buslist instruction block. (Figure 4-1).

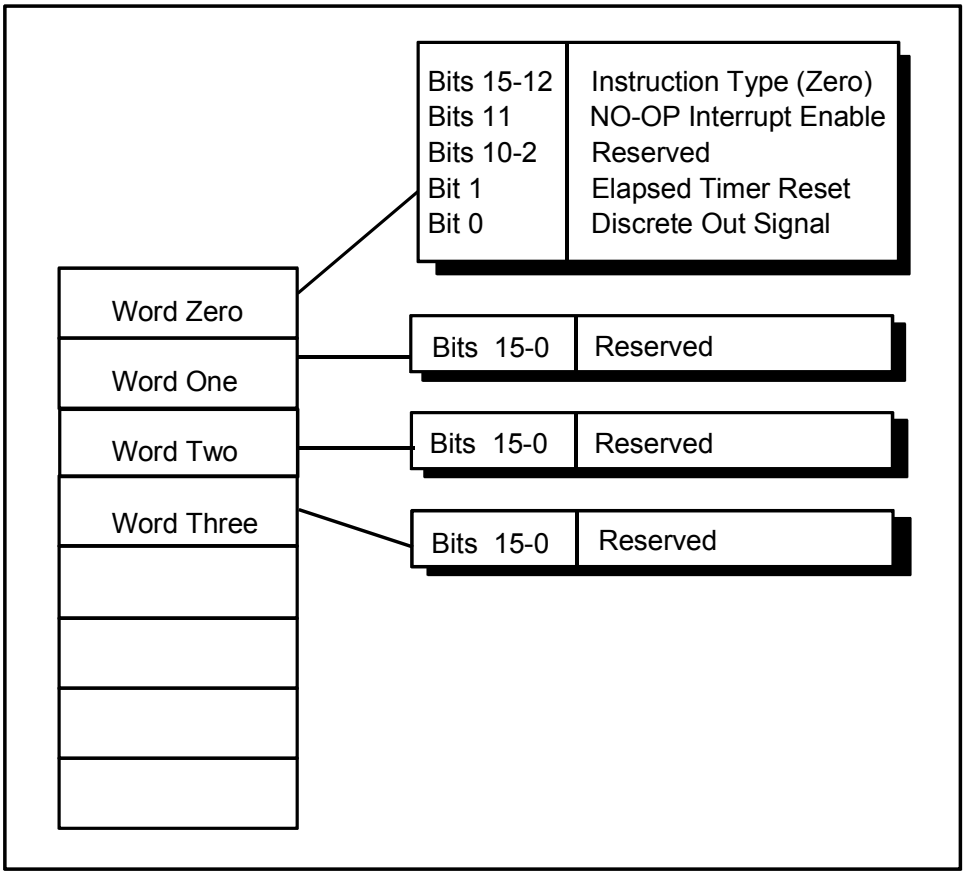


Figure 4-1 NO-OP Structure (Instruction 0x00)

Word Zero

Bits 15-12	Instruction Type (0x00)
Bit 11	NO-OP Interrupt Enable
Bits 10-2	Reserved
Bit 1	Delay Timer Reset
Bit 0	Discrete Out Signal

Words One, Two and Three

All 16 bits of Words One, Two and Three are reserved.

4.3.4 JUMP (Instruction 0x01)

The JUMP instruction is a branch instruction that can interrupt the sequential execution of buslist instructions (Figure 4-2). Bits 11-8 of buslist Instruction 0x01 determine the type of JUMP instruction (Table 4-1). Three types of JUMP instructions and a RETURN instruction allow host-independent real-time RT polling.

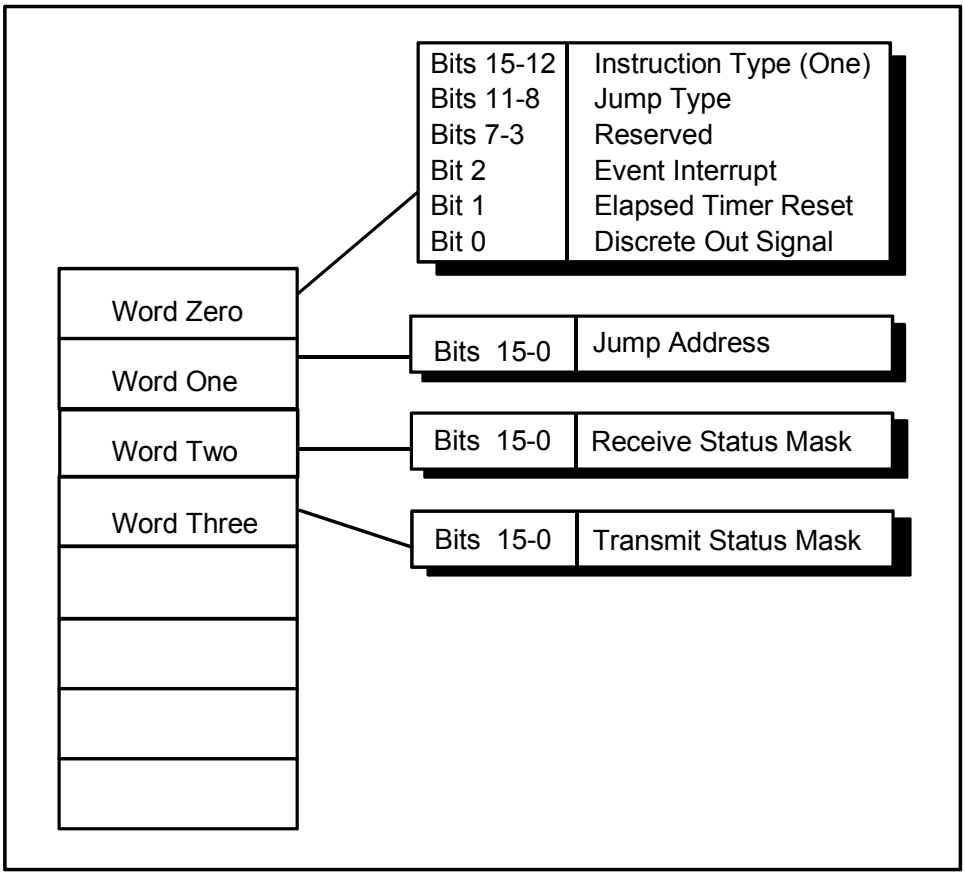


Figure 4-2 JUMP (Instruction 0x01)

Table 4-1 JUMP Types (Bits 8-11)

Bits	JUMP Types
0000	Jump Always
0001	Conditional Jump to Sublist on Status Mask
0010	Conditional Jump to Sublist on Protocol Error
0011	Return From Sublist
0100	Unconditional Jump Sublist

JUMP instructions contain the jump address (Bits 15 through 0 of Word One) that locates the memory address of the next buslist instruction to execute.

When a JUMP sublist is executed, the address of the instruction is stored in a stack of up to four JUMP addresses. If this JUMP address stack overflows, the BC generates a Stack Overflow Interrupt. A software or hardware reset automatically resets the jump address

stack pointer. The return from sublist instruction will pop the address from the top of the stack.

Word Zero

Bits 15-12	Instruction Type (0x01)
Bits 11-8	JUMP Type Defines the type of jump that the BC executes.
Bits 7-3	Reserved
Bit 2	Event Interrupt
Bit 1	Delay Timer Reset
Bit 0	Discrete Out Signal

Word One

Bits 15-0	JUMP Address The Memory Address of the next buslist instruction to execute.

Word Two

Bits 15-0	Receive Status Mask The JUMP to sublist on status mask instruction logically ANDs the Receive status response received from the MIL-STD-1553A or B bus with this word. If the result is non-zero the BC pushes the next instruction address on the stack then jumps to the buslist instruction at the location specified in Word One. If the result is zero the BC proceeds to the instruction following the JUMP.

Word Three

Bits 15-0	Transmit Status Mask Same as Word Two (except that the status response received from the MIL-STD-1553A or B bus is a Transmit Status Word).

JUMP ALWAYS (0000)

This branch instruction always causes the buslist instruction block pointer to point to the next desired buslist instruction (as defined in Word One of the buslist instruction block). No entry is added to the jump address stack upon execution of this instruction.

CONDITIONAL JUMP TO SUBLIST ON STATUS MASK (0001)

The user can have the BC compare a mask to the Transmit or Receive Status (or both in RT-to-RT transfer). By ANDing bits in the corresponding Status Mask with the RT Status, the BC can determine if a jump will occur. A jump occurs only if a non-zero value is returned after the AND condition.

EXAMPLE

RT Status Response	1400
Status Mask	07FF
Result of AND	0400

Since the result of AND is non-zero, JUMP to Sublist occurs.

CONDITIONAL JUMP TO SUBLIST ON PROTOCOL ERROR (0010)

This instruction causes the BC to jump to a sublist of buslist instructions, if a protocol error is detected in the previous MIL-STD-1553A or B transfer. The following errors result in a conditional jump:

- No Response from an RT. A Broadcast Message is excluded since no response is correct.
- Wrong RT Address from Responding RT
- Manchester Error on Status or Data from a Responding RT

RETURN FROM SUBLIST (0011)

This instruction causes the BC to remove the last address placed on the JUMP address stack and jump to the buslist instruction at that address.



NOTE: A return execution from an empty jump stack will result in unpredictable buslist sequence.

UNCONDITIONAL JUMP SUBLIST (0100)

This instruction is similar to a jump-always but places a return address on the stack before executing the jump. The instruction then continues executing the buslist at the memory address contained in the instruction (Figure 4-3).

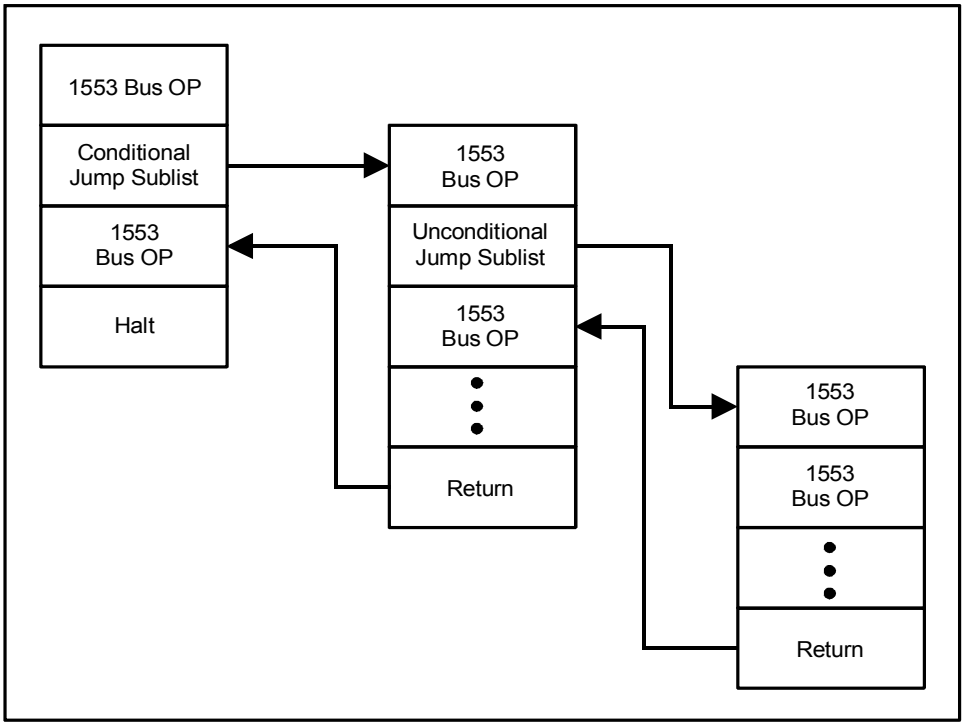


Figure 4-3 JUMP Sublist Example

4.3.5 HALT (Instruction 0x02)

This instruction terminates a buslist and generates an interrupt. The interrupt cannot be disabled and will always serve as confirmation of the buslist completion.

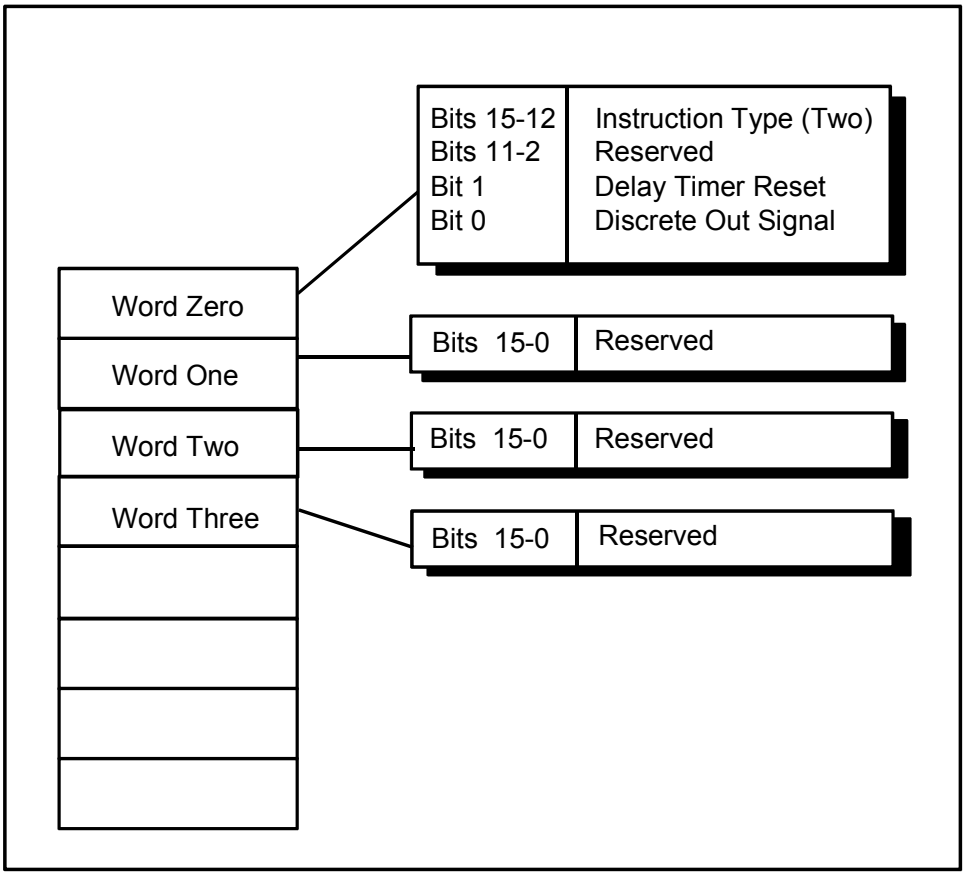


Figure 4-4 HALT (Instruction 0x02)

Word Zero

Bits 15-12	Instruction Type (0x02)
Bits 11-2	Reserved
Bit 1	Delay Timer Reset
Bit 0	Discrete Out Signal

Words One through Three

All 16 bits on Words One through Three are reserved.

4.3.6 MODE CODE (Instruction 0x03)

This instruction causes the BC to generate a MODE CODE Command on the 1553 bus and is composed of the following words (Figure 4-5).

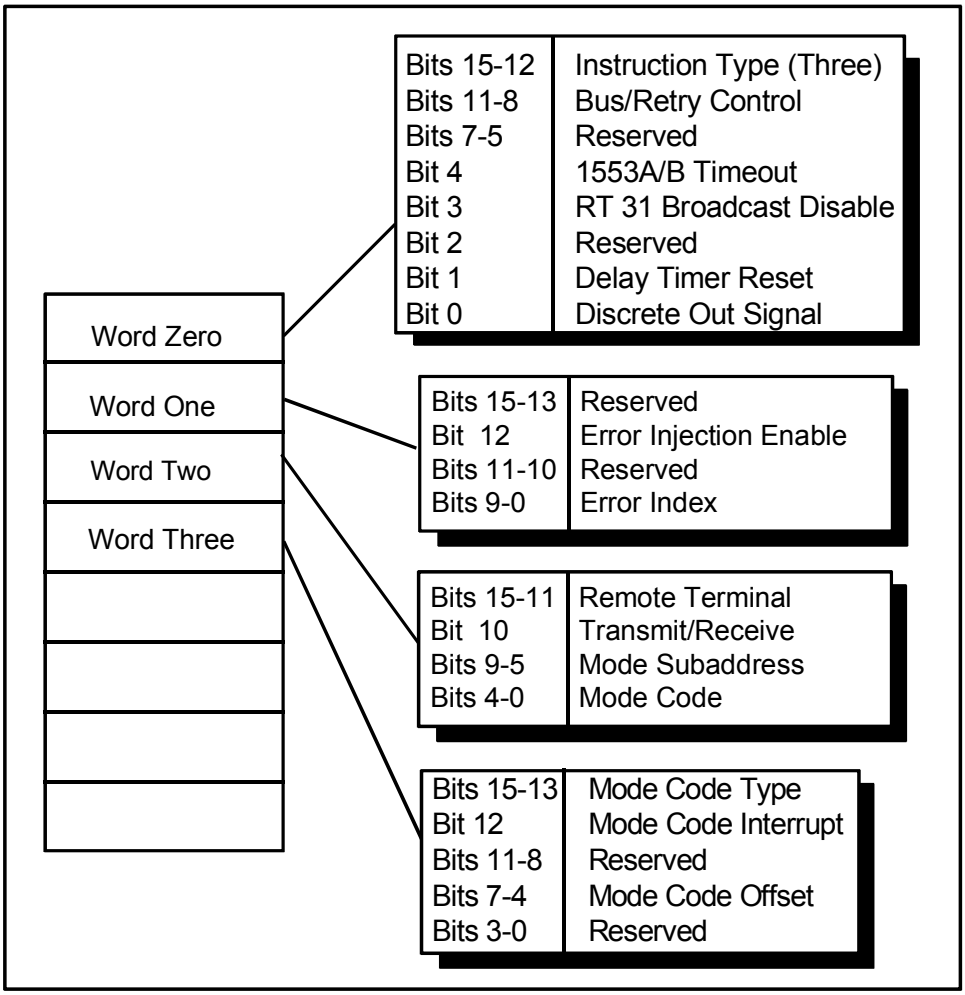


Figure 4-5 MODE CODE (Instruction 0x03)

Word Zero - Control Word

Bits 15-12	Instruction Type (0x03)
Bit 11	Current Bus
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 µs) 1 = 1553A (9 µs)
Bit 3	RT31 Broadcast Disable - must be set for 1553A instructions
Bit 2	Reserved. This bit must be set to '0' or an interrupt-on-instruction will occur.

Bit 1 — Delay Timer Reset
Set to '1' to reset the on-board Delay Timer to '0' prior to executing this command block.

Bit 0 — Discrete Out Signal
Set to '1' to generate a signal to the RS-422 connector prior to executing this command block. The duration of this signal is two microseconds.



NOTE: If Automatic Retry on current bus (Bit 10) and Opposite Bus (Bit 9) are both set, the GLD-PC retry on the current bus before attempting a retry on the opposite bus.



NOTE: If using error injection, see the Error Injection Codes (Table 4-2).

Word One - Error Control Pointer

Bits 15-13 — Reserved

Bit 12 — Error Injection Enabled
If set to '1', the GLD-PC injects the error pointed to by the Error Index.

Bits 11 & 10 — Reserved

Bits 9-0 — Error Index
Specifies the error index to be added to the starting address of the Error Table, 0x144.

Word Two - 1553 Command Word

Bits 15-11 — Remote Terminal (0-31)

Bit 10 — Transmit or Receive
1 = Transmit 0 = Receive

Bits 9-5 — Mode Subaddress (0 or 31)

Bits 4-0 — MODE CODE
MIL-STD-1553A or B Mode Code as *hex*adecimal value

Word Three - Interpretation Word

Bits 15-13 — MODE CODE Type
0 = Reserved
1 = No Data Word
2 = BC Sends Data
3 = BC Receives Data
4-7 = Reserved

Bit 12 — MODE CODE Interrupt
When set to '1' an interrupt is generated after the buslist instruction is executed.

Bits 11-8 — Reserved

Bits 7-4 — Offset Into BC Mode Code Data Block (0 - 0xF)
Data is transmitted from or received into this location (0x1430+ offset) depending on the Mode Code Type. This field is ignored when the Mode Code Type =1.

Bits 3-0 — Reserved

4.3.7 BC-to-RT Transfer(Instruction 0x04)

This instruction generates a master to remote terminal command on the 1553 bus. This instruction is composed of the following words (Figure 4-6).

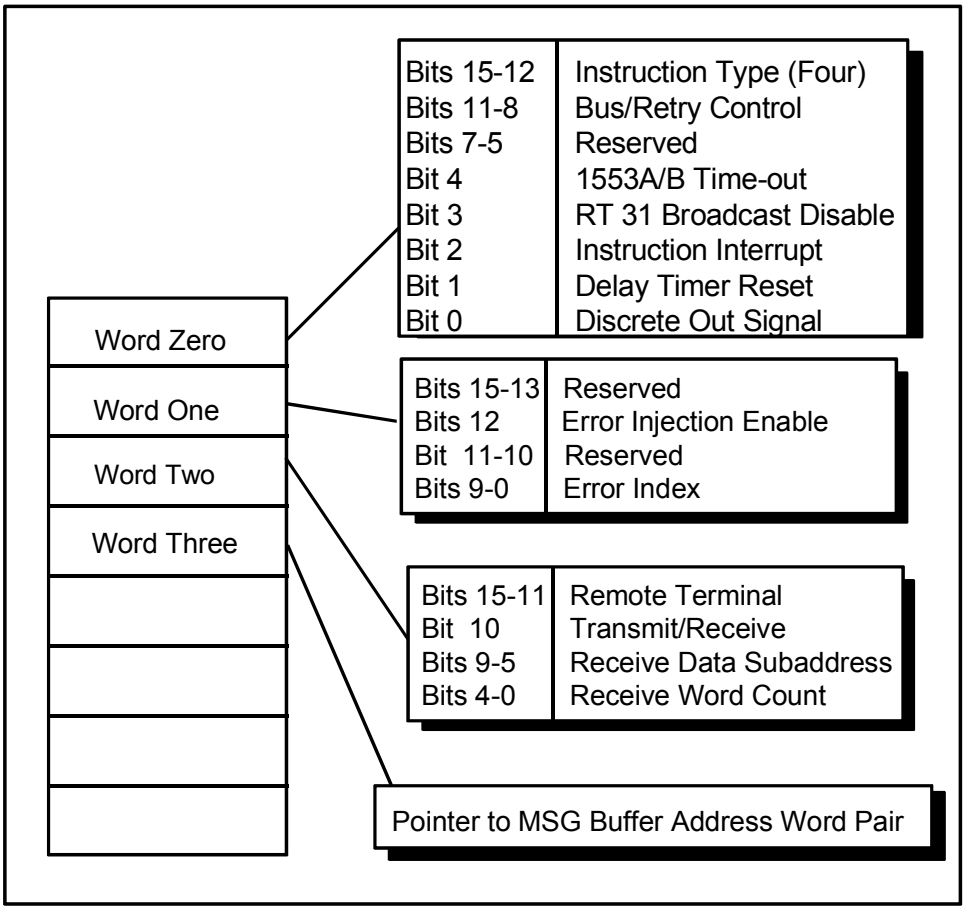


Figure 4-6 BC-TO-RT TRANSFER (Instruction 0x04)

Word Zero - Control Word

Bits 15-12	Instruction Type (0x04)
Bit 11	Current Bus - Set to '0' for bus A Set to '1' for bus B
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 μs) 1 = 1553A (9 μs)
Bit 3	RT 31 Broadcast Disable - must be set to '1' for 1553A instructions.
Bit 2	Instruction Interrupt If set to '1', the GLD-PC posts an interrupt when the command block is

executed and processed, before proceeding to the next buslist instruction.

Bit 1 — Delay Timer Reset
Set to '1' to reset the on-board Delay Timer to '0' prior to executing this command block.

Bit 0 — Discrete Out Signal
Set to '1' to generate a signal to the RS-422 connector prior to executing this command block. The duration of this signal is two microseconds.



NOTE: If using error injection, see the Error Injection Codes (Table 4-2).

Word One - Error Control Pointer

Bits 15-13 — Reserved

Bit 12 — Error Injection Enabled
If set to '1', the GLD-PC injects the error pointed to by the Error Index.

Bits 11 & 10 — Reserved

Bits 9-0 — Error Index
Specifies the error index to be added to the starting address of the Error Table, 0x1440.

Word Two - 1553 Command Word

Bits 15-11 — Receive Remote Terminal

Bit 10 — 0 = Receive - since this is a BC to RT

Bits 9-5 — Receive Data Subaddress

Bits 4-0 — Receive Word Count
The quantity of data words to be received by the RT.
0x1 - 0x1F = 1 - 31 decimal words
0x0 = 32 decimal words

Word Three - Message Buffer Address Word Pair

Bits 15-0 — The message block contains the pointers where the host stores data being transmitted by the BC (Figure 3-7).

4.3.8 RT-to-BC Transfer (Instruction 0x05)

This instruction generates a Remote Terminal to Master Command on the 1553 bus. The structure of this instruction is identical to Instruction Four BC-to-RT Transfer (Figure 4-7).

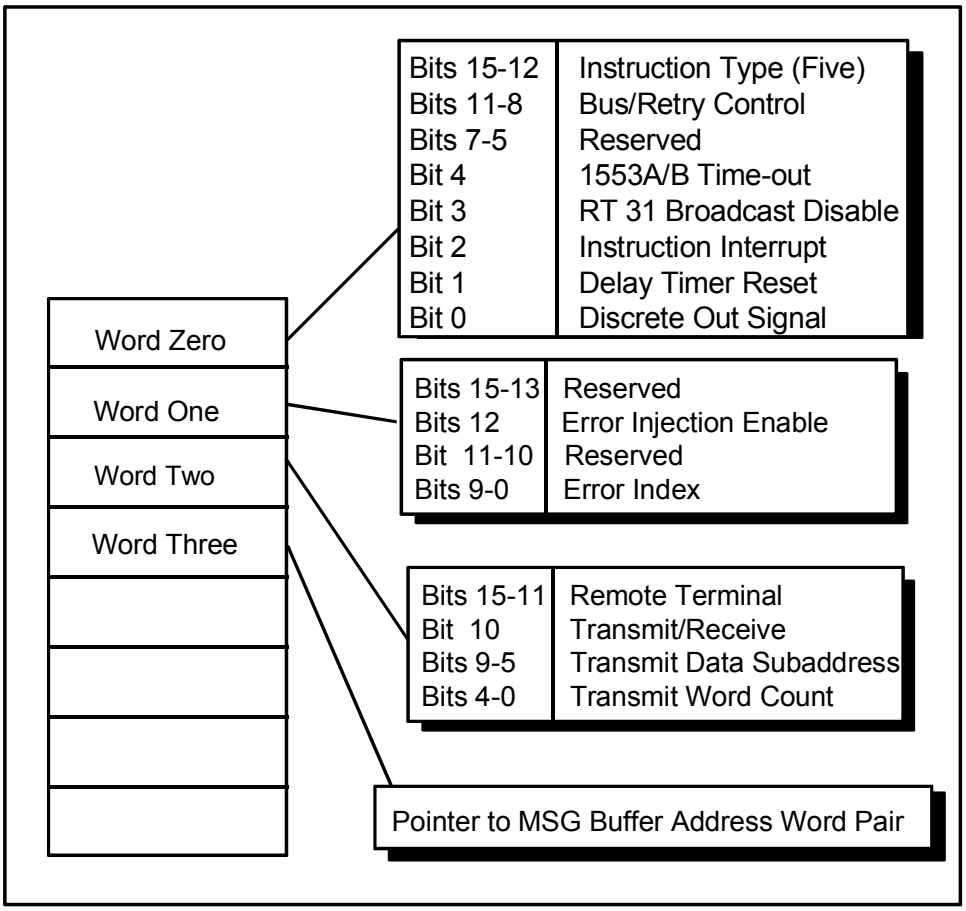


Figure 4-7 RT-TO-BC TRANSFER (Instruction 0x05)

Word Zero - Control Word

Bits 15-12	Instruction Type (0x05)
Bit 11	Current Bus - Set to '0' for bus A Set to '1' for bus B
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 μs) 1 = 1553A (9 μs)
Bit 3	RT31 Broadcast Disable - must be set for 1553A instructions
Bit 2	Instruction Interrupt

Set to '1' to post an interrupt when the command block is executed and processed, before proceeding to the next buslist instruction.

Bit 1 Delay Timer Reset

Set to '1' to reset the on-board Delay Timer to 0 prior to executing this command block.

Bit 0 Discrete Out Signal

Set to '1' to generate a signal to the RS-422 connector prior to executing this command block. The duration of this signal is two microseconds.



NOTE: If using error injection, see the Error Injection Codes (Table 4-2).

Word One - Error Control Pointer

Bits 15-13 Reserved

Bit 12 Error Injection Enabled
Set to '1' to inject the error pointed to by the Error Index.

Bits 11 & 10 Reserved

Bits 9-0 Error Index
Specifies the error index to be added to the starting address of the Error Table, 0x1440.

Word Two - 1553 Command Word

Bits 15-11 Transmit Remote Terminal

Bit 10 1 = Transmit - since this is a RT to BC transfer

Bits 9-5 Transmit Data Subaddress

Bits 4-0 Transmit Word Count

The quantity of data words to be transmitted by the RT.
0x1 - 0x1F = 1 - 31 decimal words
0x0 = 32 decimal words

Word Three - Message Buffer Address Word Pair

Bits 15-0 Pointer to the Message Buffer Address Word Pair for BC data storage.

4.3.9 RT-to-RT Transfer (Instruction 0x06)

This instruction generates the two commands for a 1553 Remote Terminal to Remote Terminal transfer. RT-to-RT transfer involves the following words (Figure 4-8).

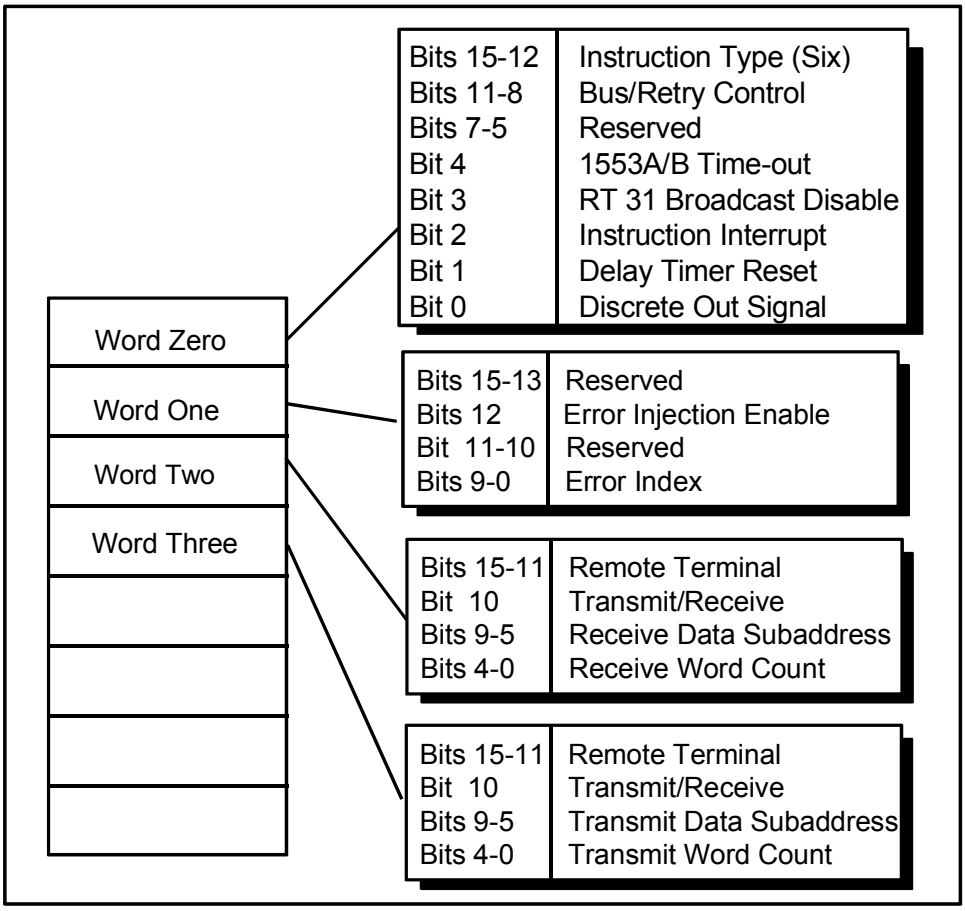


Figure 4-8 RT-TO-RT TRANSFER (Instruction 0x06)

Word Zero - Control Word

Bits 15-12	Instruction Type (0x06)
Bit 11	Current Bus - Set to '0' for bus A Set to '1' for bus B
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 μs) 1 = 1553A (9 μs)
Bit 3	RT 31 Broadcast Disable - must be set for 1553A instructions.

Bit 2	Instruction Interrupt Set to '1' to post an interrupt when the command block is executed and processed, before proceeding to the next buslist instruction.
Bit 1	Delay Timer Reset Set to '1' to reset the on-board Delay Timer to 0 prior to executing this command block.
Bit 0	Discrete Out Signal Set to '1' to generate a signal to the RS-422 connector prior to executing this command block. The duration of this signal is two microseconds.



NOTE: If using error injection, see the Error Injection Codes (Table 4-2).

Word One - Error Control Pointer

Bits 15-13	Reserved
Bit 12	Error Injection Enabled Set to '1' to inject the error pointed to by the Error Index.
Bits 11 & 10	Reserved
Bits 9-0	Error Index Specifies the error index to be added to the starting address of the Error Table, 0x1440.

Word Two - 1553 Receive Command

Bits 15-11	Receive Remote Terminal
Bit 10	0 = Receive
Bits 9-5	Receive Data Subaddress
Bits 4-0	Receive Word Count The quantity of data words to be received by the RT 0x1 - 0x1F = 1 - 31 decimal words 0x0 = 32 decimal words

Word Three - 1553 Transmit Command

Bits 15-11	Transmit Remote Terminal (0-31)
Bit 10	1 = Transmit
Bits 9-5	Transmit Data Subaddress
Bits 4-0	Transmit Word Count The quantity of data words to be transmitted by the RT 0x1 - 0x1F = 1 - 31 decimal words 0x0 = 32 decimal words

4.3.10 HALT UNTIL DELAY (Instruction 0x07)

This instruction is used for controlling the timing of commands to the 1553 bus. Instruction Seven halts the BC until the Bus Controller Delay Timer equals a value contained within Word One and Word Two of this instruction (Figure 4-9).



NOTE: This instruction uses the BC Delay Timer. This timer is free running and begins when power is supplied to the GLD-PC board. When using this instruction, reset the Delay Timer at the start of the buslist.

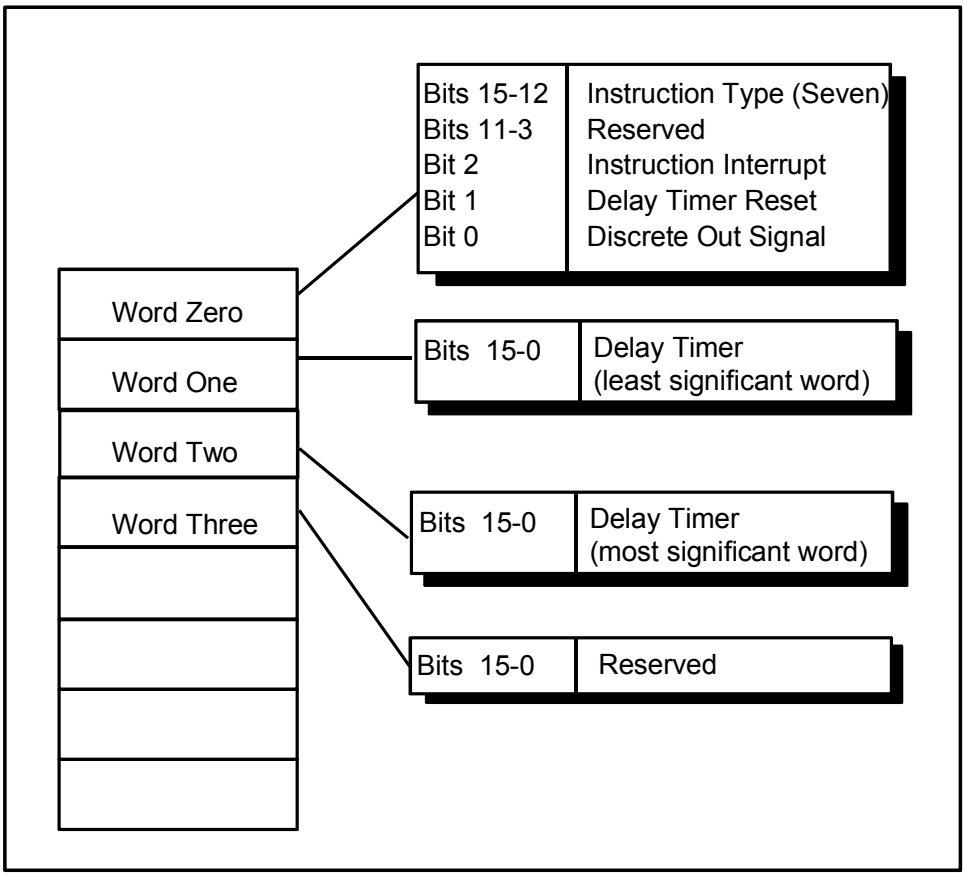


Figure 4-9 HALT UNTIL DELAY (Instruction 0x07)

Word Zero

Bits 15-12	Instruction Type (0x07)
Bits 11-3	Reserved
Bit 2	Event Interrupt Set to '1' to post an interrupt at the completion of executing and processing this command block before proceeding to the next buslist instruction.
Bit 1	Delay Timer Reset Set to '1' to reset the on-board Delay timer to zero prior to executing this command block.

Bit 0	Discrete Out Signal Set to '1' to generate a signal to the connector prior to executing this command block. The duration of this signal is two microseconds.

Word One

Bits 15-0	Delay Timer (least significant word) One microsecond resolution

Word Two

Bits 15-0	Delay Timer (most significant word) One microsecond resolution

Word Three

Bits 15-0	Reserved

4.3.11 RESET STACK (Instruction 0x08)

This instruction resets the internal jump address stack pointer to the top. Addresses are not cleared; therefore any return instruction after a reset-stack will yield unpredictable buslist sequencing (Figure 4-10).

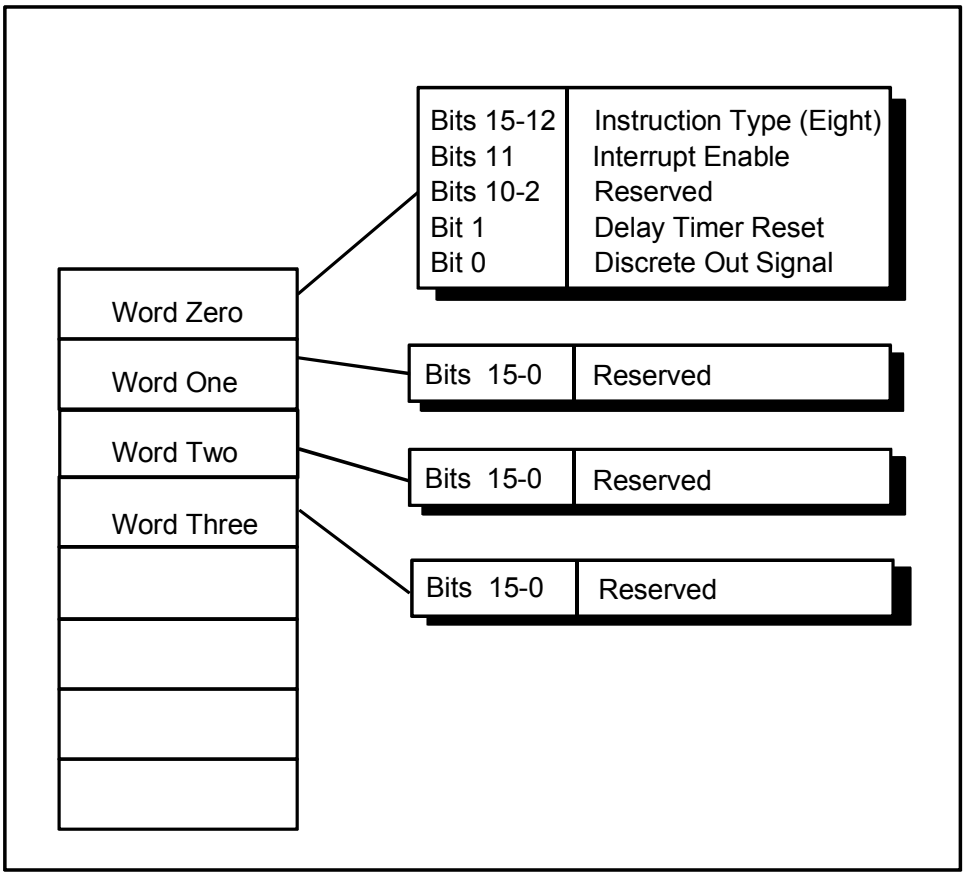


Figure 4-10 RESET STACK (Instruction 0x08)

Word Zero

Bits 15-12	Instruction Type (0x08)
Bit 11	Event Interrupt Enable
Bits 10-2	Reserved
Bit 1	Delay Timer Reset
Bit 0	Discrete Out Signal

Words One through Three

All 16 bits of Words One through Three are reserved.

4.3.12 INTERMESSAGE DELAY (Instruction 0x09)

This instruction allows the GLD-PC to wait a predetermined time before sending out the next instruction. This is used to insure a minimum gap between the end of one 1553 message and the beginning of the next command (Figure 4-11).

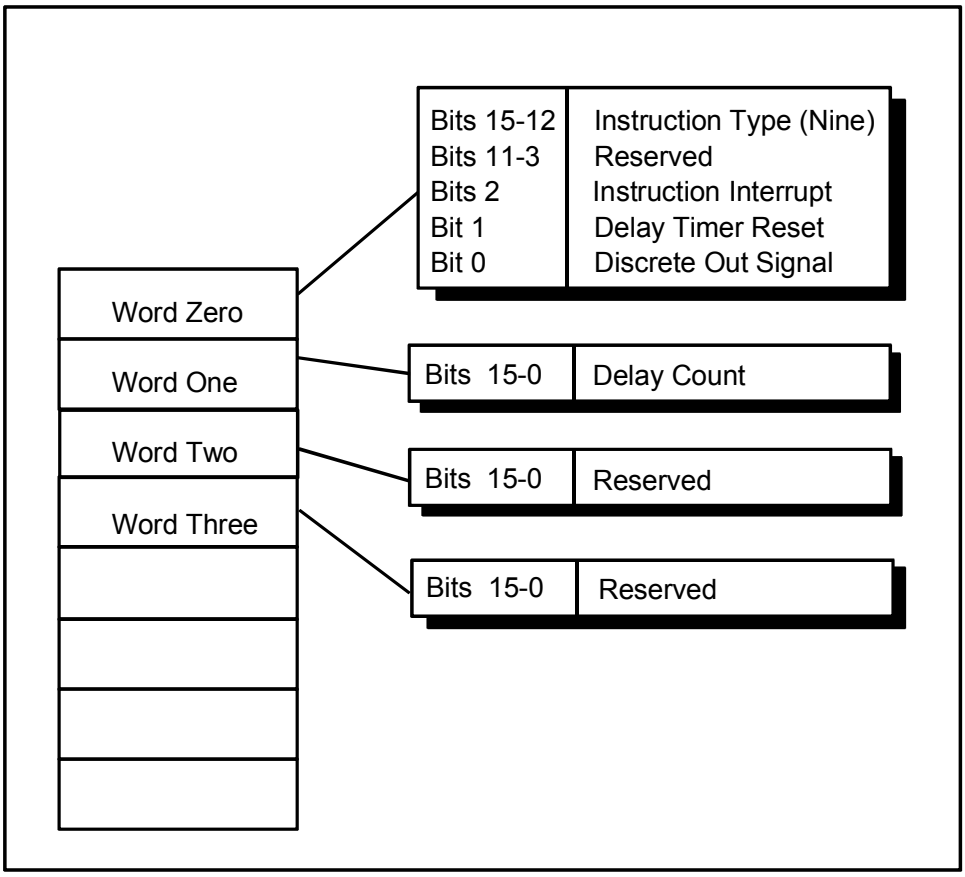


Figure 4-11 INTERMESSAGE DELAY (Instruction 0x09)

Word Zero

Bits 15-12	Instruction Type (0x09)
Bits 11-3	Reserved
Bit 2	Event Interrupt
Bit 1	Delay Timer Reset
Bit 0	Discrete Out Signal

Word One - Delay Count (in *Hex*adecimal)

Delay count (1 µs resolution)
If the event interrupt is not enabled, subtract 4 µs for overhead time.
If interrupt is enabled, subtract 8.5 µs.

4.3.13 PAUSE (Instruction 0x0A)

This instruction allows the GLD-PC to pause until a BC Start Trigger (RS 422 input) is received. This allows the user to synchronize buslist execution with external events (Figure 4-12).

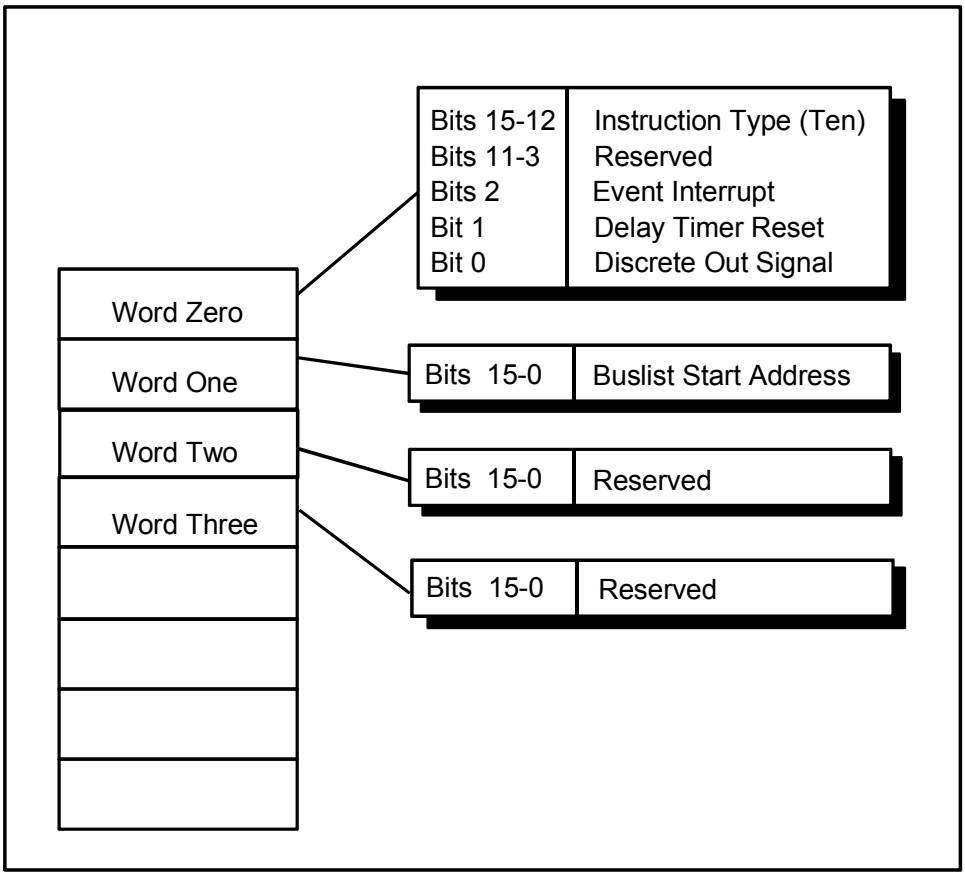


Figure 4-12 PAUSE Instruction (Instruction 0x0A)

Word Zero

Bits 15-12	Instruction Type (0x0A)
Bits 11-3	Reserved
Bit 2	Event Interrupt
Bit 1	Delay Timer Reset
Bit 0	Discrete Out Signal

Word One

Starting address of the bus controller's buslist is to be executed upon receiving a BC Start Trigger.

4.4 Message Block Structure

The GLD-PC records the message blocks to indicate the addresses of the last buffer to receive data and the last buffer to transmit data. (Figure 4-13).

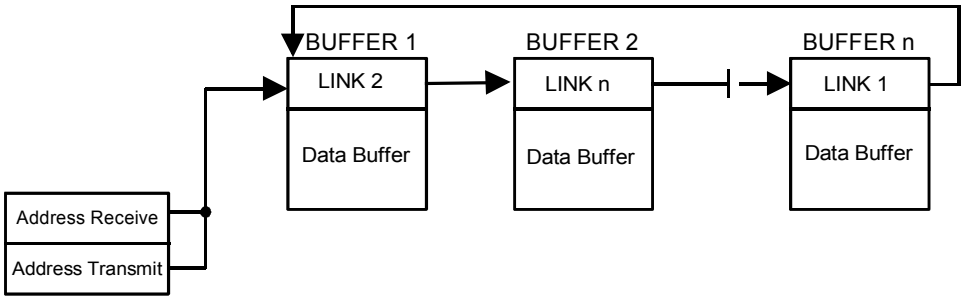


Figure 4-13 Message Block

The only words of the 1553 message stored in the buffer are the data words (Figure 4-14). Initially, the software loads both pointers with the address of the last buffer in the message block. The microcode modifies the pointers as the data in the buffers is transmitted and received.

link
header 1
header 2
data word 1
data word 2
data word 3
etc.

Figure 4-14 Message Buffer

4.4.1 Message Buffer Link Word

The first word of a message buffer is a link word containing the address of the next buffer in the message block. The link word of the last buffer holds the address of the first buffer (Figure 4-15). The software loads the correct value into the link word of each buffer.

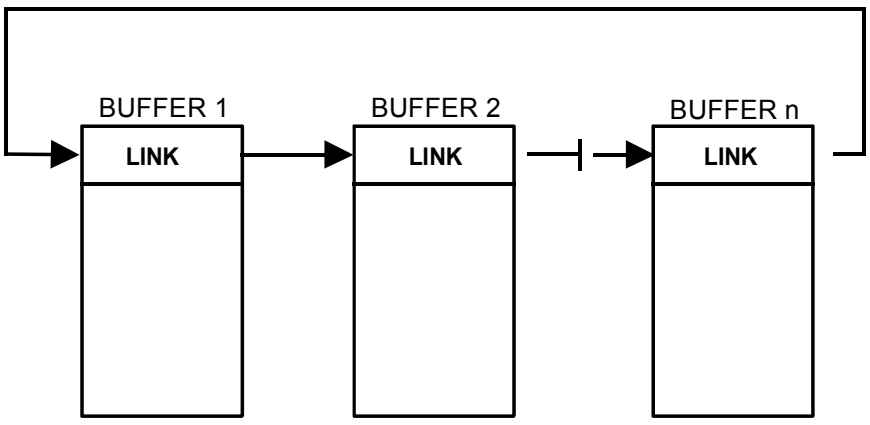


Figure 4-15 Message Buffer Link Words

Header Word 1

The header word contains the buffer word count and the control and status bits. One header word bit indicates if a missed data condition occurs. The header word also contains a bit that indicates if a message has overwritten the buffer contents (new data bit was set in the next buffer and the overwrite current buffer bit is set in this buffer). The software and microcode write to several of the bits (Figure 4-16).

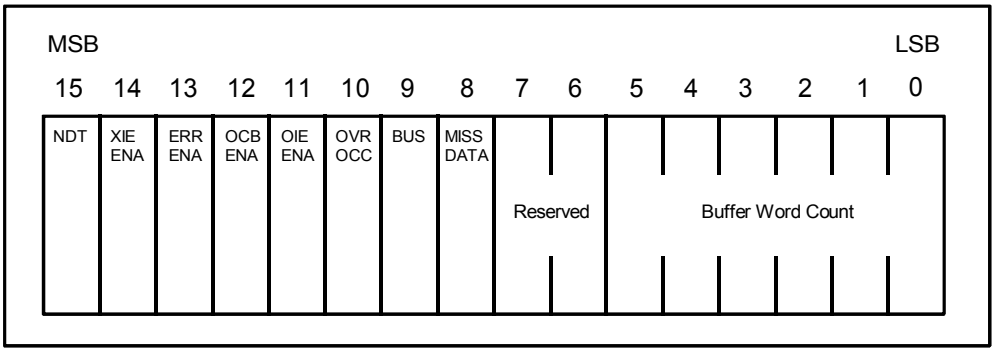


Figure 4-16 Header Word 1

Bit 15 New Data (NDT)
Set to '1' by software before transmit.
Set to '0' by software before receive.
Set to '1' by microcode after receive.
Set to '0' by microcode after transmit.

This bit indicates when data is placed in the buffer or removed from the buffer. It is the handshake between software and microcode for real time processing. For a receive buffer, the microcode **writes** into the buffer and software **reads** data out of the buffer. Therefore, the microcode will set this bit when storing data and software will clear this bit when the buffer has been read by the host.

Conversely, for transmit buffers, the software **writes** into the buffer and microcode **reads** out of the buffer. Therefore, the software sets this bit when writing 'newdata' to transmit and the microcode clears this bit after it reads the data for transmit to the 1553 bus.

Bit 14 Transfer Interrupt Enable (XIE ENA)
Set to '1' by software to enable interrupt.
Set to '0' by software to disable interrupt.

Bit 13 Error Interrupt Enable (ERR ENA)
Set to '1' by software to enable interrupt.
Set to '0' by software to disable interrupt.

Bit 12 Overwrite Current Buffer (OCB ENA)
Set to '1' by software to allow overwrite.
Set to '0' by software to prevent overwrite.
The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. If the new Data Bit is reset in the next buffer, the data words are stored in the next buffer. If the New Data Bit is set in the next buffer and the Overwrite Current Buffer Bit is set in the current buffer, the data is written to the current buffer. Otherwise, the data is not stored in the buffer and the Missed Data Bit is set in the current buffer.

Bit 11	Overwrite Interrupt Enable (OIE ENA) Set to '1' by software to enable interrupt, when an overwrite has occurred. Set to '0' by software to disable interrupt.
Bit 10	Overwrite Condition Occurred (OVR OCC) Set to '0' by software initially and after it is set by microcode. Set to '1' by microcode when overwrite occurs.
Bit 9	Bus Used Set to '0' initially. During simulation it is set or cleared by microcode. Set to '1' for Bus A Set to '0' for Bus B.
Bit 8	Missed Data Condition Occurred (MISS DATA) Set to '0' by software initially and after it is set by microcode. Set to '1' by microcode when missed data occurs. If the new data bit is set in the next buffer and the Overwrite Current buffer is cleared in this buffer, then the Missed Data bit will be set and the data will not be stored.
Bits 7-6	Reserved
Bits 5-0	Buffer Word Count (0-63)

Header Word 2

The received word count field is stored by the microcode in Header Word 2 and reflects the number of data words stored during a receive message (Figure 4-17). If this same buffer is involved in a transmit message, the received word count field is set to '0' by the microcode. Bits 15-6 are reserved and may be non-zero.

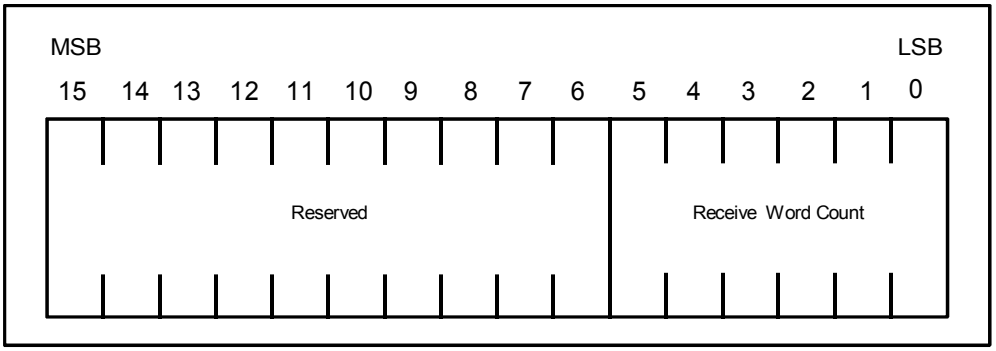


Figure 4-17 Header Word 2

Data Words

The data words transacted in the 1553 message follow Header Word 2.

4.5 BC Mode Code Data Block

Mode Commands with data are stored in the BC Mode Code Data Block. This Block is located at the fixed memory location 0x1430 - 0x143F.

When a Mode Command (with Data Word) is issued by the BC, the Mode Code Instruction in the buslist instruction block contains an offset (0-F) from address 0x1430, which is used to transmit a data word or store a received data word (Figure 3-18).

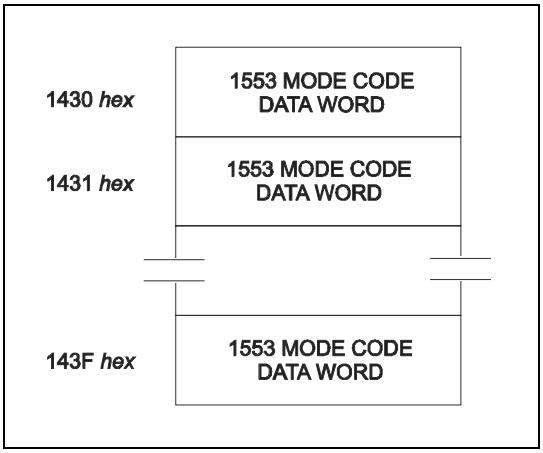


Figure 4-18 BC Mode Code Data Block

4.6 Error Injection

Error Injection capability is based on an error index field in the error control pointer. This index is an offset from the starting address of the Error Table (0x1440), and points to the user-programmed Error Control Word. This gives the user a high degree of flexibility when programming various errors to be injected.



NOTE: The area of memory from 1440 through 0xFFFF is free memory. If error injection is enabled, "n" unique errors can be configured between addresses 1440 through 1440 + (N-1). Free memory then begins at 1440 + n. If no errors are injected, free memory begins at 1440.

The Error Index is specified in the second word of all applicable BC buslist instructions, as well as Word Zero of the Subaddress Response Word Pair and Mode Code Response Word. If Error Injection is enabled, the Error Index field is automatically added to the Error Table and the desired error is injected.

4.6.1 Error Control Word

The 16 bits of the Error Control Word specify the type of error created by the GLD-PC (Figure 3-19).

Bits 0-3	Error Bit Gap Field
Bits 4-9	Error Word
Bits 10-14	Error Code
Bit 15	Clear Error/Continuous Error

Figure 4-19 Error Control Word

Bit 15 Clear Error/Continuous Error
0 = Error once then clear
1 = Continuous Error

Bits 14-10 Error Code

Bits 9-4 Error Word
The word the error is injected upon, such as command word, second data word, etc. With the command always word 0 and all others incremented after.

Bits 3-0 Error Bit/Gap Field



NOTE: The GLD-PC uses the Error Control Word only if "BC Error" is enabled in the BC error Control Register 14, or if the Error Interrupt Enable Bit is set in Word 0 of the Subaddress Response Word Pair or Mode Code Response Word.

4.6.2 Error Codes

The Error Control Word provides 11 types of errors:

- Mid-Sync Zero Crossing
- Mid-Bit Zero Crossing
- Sync Encoding
- Bi-Phase Encoding
- Bit Count Low
- Bit Count High
- Parity
- Gap Injected
- Set Status Bit
- No Response
- Word Count

One error per message can be injected with the error on the command or data word, before the message is transmitted on the multiplex data bus (Table 3-2).

MID-SYNC ZERO CROSSING

The typical mid-sync zero crossing occurs at 1.5 microseconds from start of sync. When this error is injected, the mid-sync zero crossing is skewed left or right ±150 nanoseconds.

MID-BIT ZERO CROSSING

The typical mid-bit zero crossing occurs 500 nanoseconds from the start of the bit time. When this error is injected, the mid-bit zero crossing is skewed left or right ±150 nanoseconds.

SYNC ENCODING

Sync encoding injects an encoding error into the sync field.

BI-PHASE ENCODING

During a bit time, the bit does not make a zero-crossing transition.

BIT COUNT LOW

Qualified word is transmitted with 18 or 19 bits instead of 20 bits.

BIT COUNT HIGH

Qualified word is transmitted with 21, 22 or 23 bits instead of 20 bits.

PARITY

Qualified MIL-STD-1553A or B word bits are transmitted with even parity.

GAP INJECTED

A programmable gap of 2.0 to 9.5 microseconds can be injected between contiguous words within a message stream (Table 4-2 and Table 4-3).

SET STATUS BITS

A qualified bit is set in the 1553 status response word. Only one bit can be set at a time.

NO RESPONSE

A qualified RT/SA that is addressed and does not respond to the valid command or mode command transmitted on the 1553 bus.

WORD COUNT

A qualified message transmitted with 0-63 data words.

Table 4-2 Error Injection Codes

Error Type	Err Code Setting	Err Word	Err Bit/Gap Count
No Error	0x0	N/A	N/A
Mid-Sync Zero Crossing			
<-150 ns	0x3	0-0x20	N/A
>+150 ns	0x1	0-0x20	N/A
Mid-Bit Zero Crossing			
<-150 ns	1C*hex*	0-0x20	F-0x0
>+150 ns	17*hex*	0-0x20	F-0x0
Sync Encoding			
111100	0x2	0-0x20	N/A
111010	0x4	0-0x20	N/A
110000	0x5	0-0x20	N/A
011000	0x6	0-0x20	N/A
000011	0x7	0-0x20	N/A
000110	0xA	0-0x20	N/A
001111	0xC	0-0x20	N/A
100111	0xD	0-0x20	N/A
000111	0xE	0-0x20	N/A
111000	0xF	0-0x20	N/A
Bi-Phase Encoding			
Bits 0-15	0x1D	0-0x20	F-0x0
Parity Bit	0x1E	0-0x20	N/A
Bit Count Low			
1 Bit	0x11	0-0x20	N/A
2 Bits	0x12	0-0x20	N/A
Bit Count High			
1 Bit	0x13	0-0x20	N/A
2 Bits	0x14	0-0x20	N/A
3 Bits	0x19	0-0x20	N/A
Parity	0x16	0-0x20	N/A
Gap Injected	0x15	1-0x1F	F-0x0
Status Bit Injection (RT Mode only)	0x8	N/A	F-0x0
No Response Error (RT Mode only)	0x9	N/A	N/A
Word Count Error	0xB	0-0x3F	N/A

Table 4-3 Gap Count Field in Microseconds

Gap Count	Number of Microseconds
0	2.0
1	2.5
2	3.0
3	3.5
4	4.0
5	4.5
6	5.0
7	5.5
8	6.0
9	6.5
A	7.0
B	7.5
C	8.0
D	8.5
E	9.0
F	9.5

Each value is measured from mid-bit to mid-bit crossing.

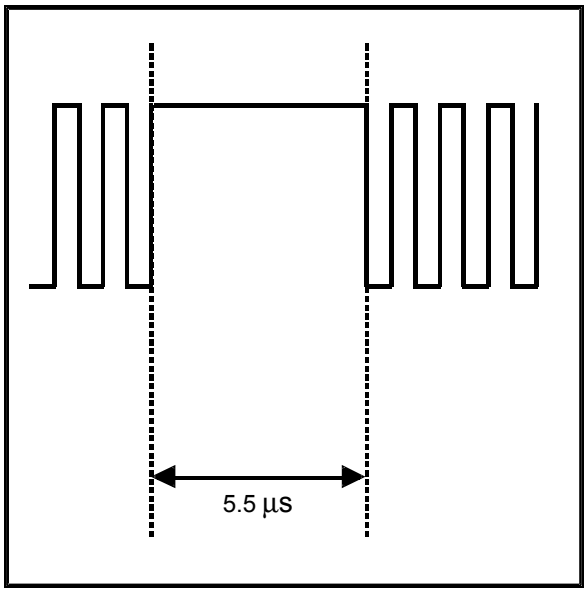


Figure 4-20 Sample Gap Injection of 5.5 µs

4.7 BC Start Trigger

This feature allows the Bus Controller to be automatically started when an external RS-422 pulse is received on pins 9 and 10 of the 16-pin connector J4 (or JB4 for the second channel.) The board must also be configured properly as a Bus Controller, and bit 15 (BC STA TRG ENA) of the BC Start Trigger Control Register must be set to a '1'.

Write the Bus Controller's buslist start address to the BC Start Trigger Address Register (0x141A) as opposed to writing the BC Control Function Register (0x10) with the starting address of the buslist.

5. MRT MODE OPERATION

5.1 Overview

The MRT mode allows emulation of up to 32 RTs in 1553A mode and 31 RTs and one Broadcast RT in 1553B mode. For each RT, up to 32 subaddresses may be configured. Subaddresses 0 (for both 1553A and B protocol) and 31 (for 1553B mode only) are allowed as **mode code subaddresses**. Subaddresses 1 through 30 (and 31 for 1553A mode only) can only be configured as **data subaddresses**. This mode can operate simultaneously with the BC and CM modes on the GLD-PC multi-function board.



NOTE: The GLD-PC does not handle the superseding valid commands in the MRT mode.

5.2 Status Block

In the MRT mode, each RT address is associated with a Status Block (located in Dual-Port RAM), which contains a control word, status word and other data relating to its configuration (Figure 5-1). The RT Status Blocks occupy a space in memory from 0x1000 - 0x11FF.

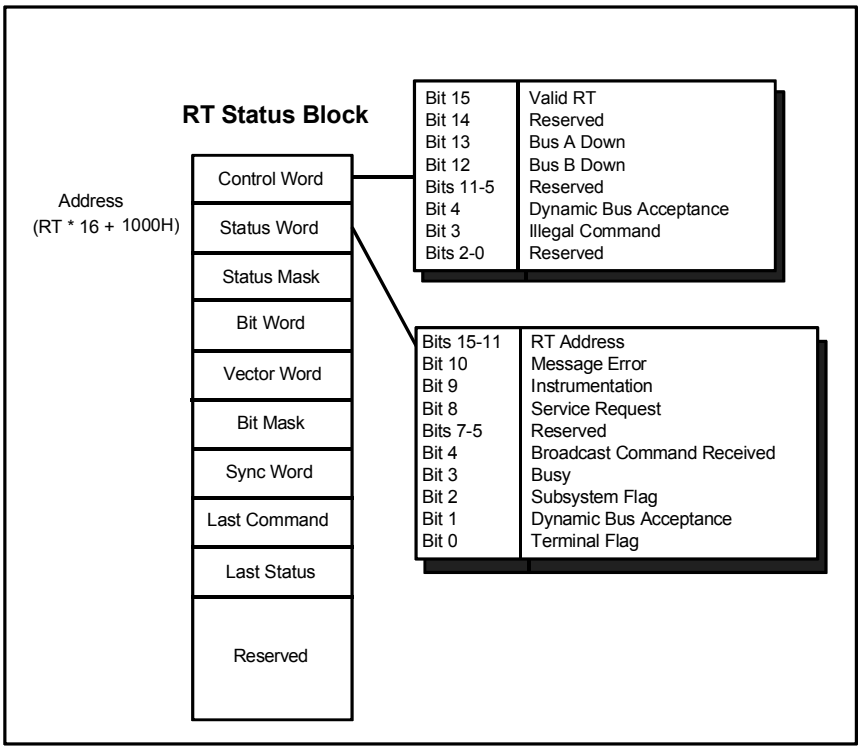


Figure 5-1 RT Status Block

The status block contains:

- A control word for enabling and configuring RT characteristics.
- The status response word of the RT
- A mask to be ANDed with the RT's status word before it is sent out
- The RT's BIT word
- The RT's vector word
- A mask that is ANDed with the BIT word if a Reset RT mode code is received
- Sync word
- The last command word to the RT
- The last status response word of the RT

Table 5-1 RT Status Block Words

Words	Block Offset
Control Word	0000
Status Word	0001
Status Mask	0010
Bit Word	0011
Vector Word	0100
Bit Mask	0101
Sync Word	0110
Last Command	0111
Last Status	1000

During operation, each RT's status word is recalculated and the last command word and status word are updated as each message is received. Appropriate bits in the status word are set by the microcode. The RT receiving the command is a MIL-STD-1553A or B compliant RT.

Control Word

Bit 15 Valid RT

Bit 14 Reserved

Bit 13 Bus A Down
Indicates the Primary Bus is shut down. Bit 13 is affected by the Transmitter Shutdown and Override transmitter Shutdown mode commands. To have the host activate this function you must also select the corresponding RT bit in the RT Shutdown Enable Register (0x140D and 0x1410).

Bit 12 Bus B Down
Indicates the Secondary Bus is shut down. Bit 12 is affected by the Transmitter Shutdown and Override Transmitter Shutdown mode commands. To have the host activate this function you must also select the corresponding RT bit in the RT Shutdown Enable Register (0x140D and 0x1410).

Bits 11-5 Reserved

Bit 4 Dynamic Bus Acceptance
Controls the RT's response to an Accept BC mode command.

	Set to ‘1’, the RT sets the BC Acceptance Bit in its status, in response to that mode code.
Bit 3	Illegal Command Set to ‘1’, the RT responds to illegal mode commands by returning a status word with the Message Error Bit set, with no data words. Set to ‘0’, the RT does not respond to illegal commands.
Bits 2-0	Reserved

Status Word

The Status word is ANDed with the RT Status Mask Word and sent as the RT's status response to all legal commands except a Transmit Last Status or Transmit Last Command mode code.

Bits 15-11	RT Address Per MIL-STD-1553A or B, Bits 15-11 indicate the RT address (0-31).
Bit 10	Message Error Bit 10 indicates a sync, length, parity or Manchester error. In 1553A mode, in the event of a Manchester error on the received data, the RT will properly respond with this bit set to ‘1’.
Bit 9	Instrumentation Bit 9 distinguishes a status word from a command word.
Bit 8	Service Request (Optional) Bit 8 indicates the RT has requested service.
Bits 7-5	Reserved
Bit 4	Broadcast Command Received
Bit 3	Busy Bit 3 indicates the RT is unable to move data.
Bit 2	Subsystem Flag Bit 2 indicates a fault in an RT (specifically, invalid data).
Bit 1	Dynamic Bus Acceptance Controls the RT’s response to an Accept BC mode command. Set to ‘1’, the RT sets the BC Acceptance Bit in its status, in response to that mode code.
Bit 0	Terminal Flag Set to ‘1’ when there is a fault in an RT.

Status Mask Word

When the Status Mask Word contains a ‘1’ in any bit position, the corresponding bit in the Status Word is transmitted. A ‘0’ causes the corresponding Status Bit to be transmitted as a zero regardless of the state of the bit in the Status Word. For most conditions, this word should be 0xFFFF.

Bit Word

The user-defined Bit word is transmitted in response to a Transmit Bit Word mode command. This word is reset by a Reset RT mode code, depending on the mask value in the RT Bit Mask Word (ANDed with bit mask on Reset RT mode code).

Vector Word

The user-defined Vector word is transmitted in response to a Transmit Vector Word mode command. The Vector word notifies the BC that the RT requires service over and above the Service Request Bit being set.

Bit Mask Word

When the bit mask word has a '0' in any bit position, the corresponding bit in the Bit Word is reset upon reception of a Reset RT mode command. For most conditions this word should be 0xFFFF .

Synchronization Word

The received data word with a Synchronize-with-Data mode command stored by the RT.

Last Command Word

The last valid command word received by this RT. This word is meaningless if the Transmit Last Command mode code is the first command to the RT.

Last Status Word

This word is the Status Word associated with the last valid command addressed to the RT.

5.2.1 Addressing the Status Block

To address the status block, follow this formula:

RT#
0001 000 _ _ _ _ _ 0000 *bin*

Enter the appropriate binary RT number (0-31) in the five-bit space reserved for RTs.

EXAMPLE

To enter RT 2:

To calculate the origin of RT 2's status block, enter a binary '2' in the RT field (Bits 4-8).

RT#
0001 000 0 0 0 1 0 0000 *bin*

1	0	2	0x0	Convert to hexadecimal to arrive at the address of the status block.

5.3 Subaddress Response Word Pairs

Each RT's Subaddress Response word pair is located at pre-defined addresses. The GLD-PC computes the address of the RT's Subaddress Response word pair from the command word received by the emulated RT. If the subaddress field of the command word is 1-30 (and subaddress 31 for MIL-STD-1553A protocol), the GLD-PC uses the pointer in the second word to identify the message block's address. This message block's data buffer is used for the transfer on the MIL-STD-1553A or B bus. If the command word references subaddress 0 or 31 (MIL-STD-1553B protocol only), the GLD-PC uses the pointer in the second word to identify the address of the RT Mode Code Response Block.

5.4 Error Injection

Protocol and electrical errors can be injected at the subaddress level. This is done in the subaddress-response word pairs. The types and method of error injection are identical to the Bus Controller mode. Refer to Table 4-2, page 4-28 for Error Injection Codes.

5.5 Extracting Address from the Command Word

The subaddress response word pairs are located in memory between addresses 0x0000 and 0x0FFF . There is one pair for the receive direction and one pair for the transmit direction for each RTSA combination.

To address the RECEIVE subaddress response word pairs:

RT		SA		
0000	0		0	Word One - Control Word
0000	0		1	Word Two - Pointer

To address the TRANSMIT subaddress response word pairs:

RT		SA		
0000	1		0	Word One - Control Word
0000	1		1	Word Two - Pointer

EXAMPLES

Example 1
To address Word One of RT 3, with SA1 to receive:

0000 00011 0 00001 0
RT3 SA 1

To access the second word, enter a '1' in Bit 0 of the address formula to calculate the address.

0000 00011 0 00001 1

Example 2
To address Word One of RT5, SA 10 to transmit:

0000 00101 1 01010 0
RT5 SA10

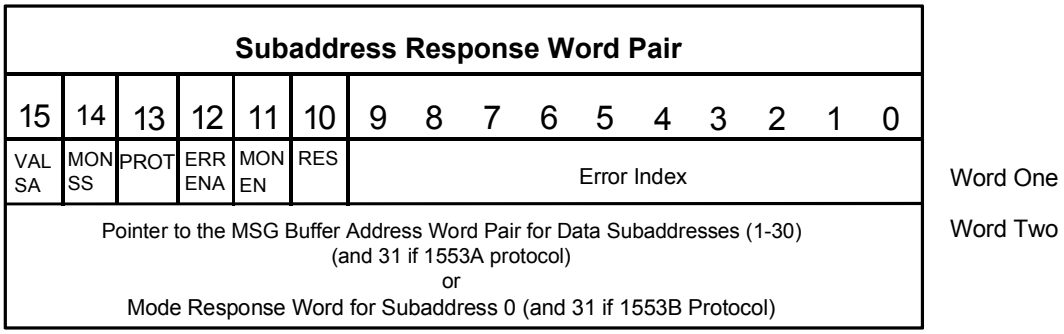


Figure 5-2 Subaddress Response Word Pair

Word One - Control Word

Bit 15 Valid Subaddress (VAL SA)
Set to '1' by software if this is a valid subaddress.
Set to 0 by software if it isn't.

Bit 14 Monitor Snapshot (MON SS)
Set to '1' by software if message to this subaddress should generate a snap shot interrupt.
Set to '0' by software if snap shot interrupt is not used.

Bit 13 1553 Protocol (PROT)
Set to '0' will declare subaddress a 1553B type.
Set to '1' will declare subaddress to be a 1553A protocol device.

Bit 12 Enable RT Error Injection (ERR ENA)
Set to '1' to enable error injection capability and signal microcode to use the error index.

Bit 11 Monitor Enable (MON EN)
Set to '1' by software if subaddress is to be monitored.
Set to '0' by software if this subaddress is not monitored.

Bit 10 Reserved

Bits 9-0 Error Index
See Table 4-2, page 4-28 for error-injection codes.

If the Monitor Bit (Bit 11) of the first word of Data Subaddress Response Word Pair is set to '1', a message directed to this RT/direction/SA combination is captured by the monitor. (Figure 5-2). The subaddress does not have to be enabled for the message to be captured (Bit 15 can be zero).

Word Two - Data Subaddress Pointer

Word Two points to the Message Buffer Address Word Pair located in the Message Block (Figure 5-3). This word pair contains the address in free memory of the last buffer used (one for receive and one for transmit).

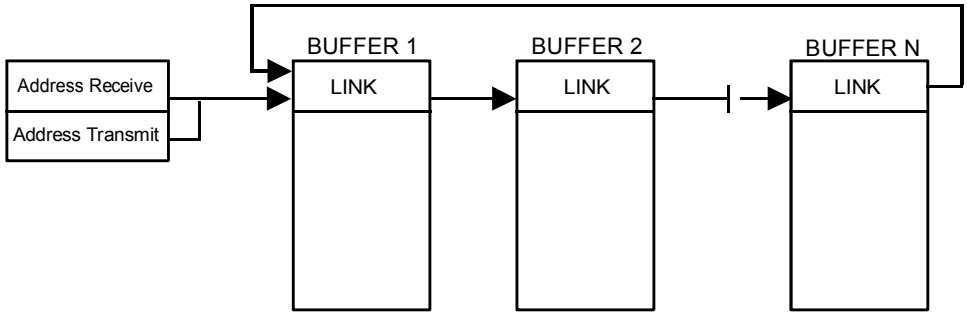


Figure 5-3 Message Block

When setting up a message block (using the *DefineBlockMBGld()* routine in the Interface Library), the routine loads both the receive and transmit address pointers with the same address, that of the last buffer in the message block. These pointers are automatically updated by the microcode to the next buffer in the linked list as data is received or transmitted into or out of a buffer. The only words of the 1553 message stored in the buffer are the data words (Figure 5-4).

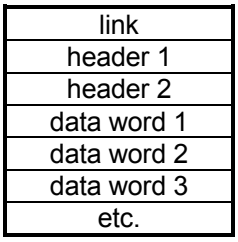


Figure 5-4 Message Buffer

Word Two - Mode Response Pointer

If the transmitted or received subaddress is ‘0’ (or ‘31’ for 1553B protocol), Word Two of the SA Response Word Pair points to the Mode Code Response Block. The on-board Configuration data adds the Mode Code number to contents of Word Two; thus, pointing to the proper Mode Code Response Word within the Mode Code Response Block.

5.6 Message Buffers

5.6.1 Message Buffer Link Word

The first word of a message buffer is a link word containing the address of the next buffer in the message block. The link word of the end buffer must contain the address of the first buffer (Figure 5-5). The software loads the correct value into the link word of each buffer.

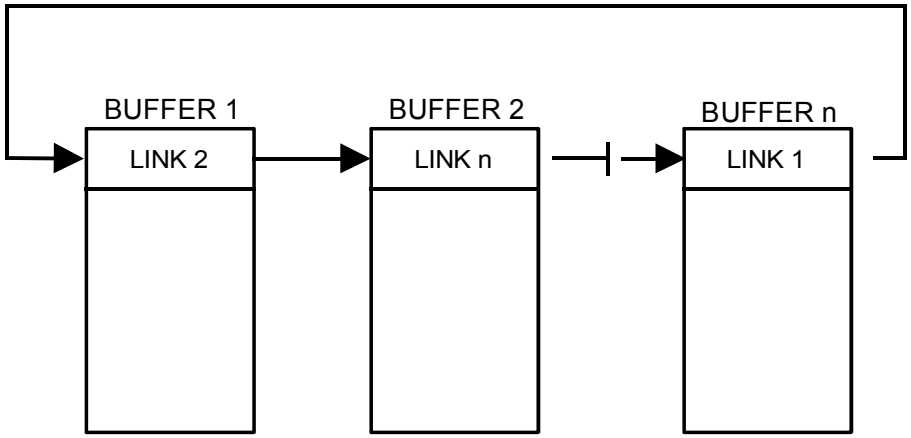


Figure 5-5 Message Buffer Link Words

5.6.2 Header Words

Header Word 1

The header word contains control bits and the word count for the message in the buffer. An overwrite control scheme is contained within the control bits. A message can overwrite the current buffer contents when the new data bit is set in the next buffer. Overwrite Current Buffer bit, Missed Data and New Data bits are set to '1' in this buffer to indicate the overwrite occurred (Figure 5-6). The software also writes to several of the bits to control interrupts and error handling.

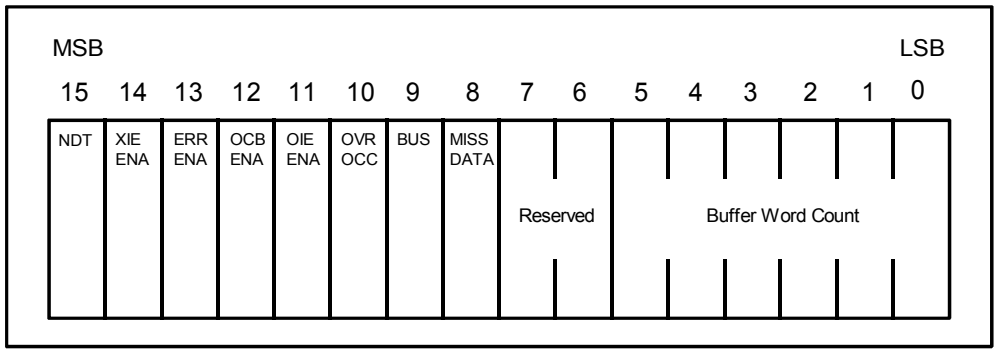


Figure 5-6 Header Word 1

Bit 15	New Data (NDT) Set to '1' by software before transmit. Set to '0' by software before receive. Set to '1' by microcode after receive. Set to '0' by microcode after transmit. This bit indicates when data is placed in the buffer or removed from the buffer. It is the handshake between software and microcode for real time processing. For a receive buffer, the microcode **writes** into the buffer and software **reads** data out of the buffer. Therefore, the microcode sets this bit when storing data, and software clears this bit when the buffer has been read by the host. Conversely, for transmit buffers, the software **writes** into the buffer and microcode **reads** out of the buffer. Therefore, the software sets this bit when writing 'newdata' to transmit and the microcode clears this bit after it reads the data for transmit to the 1553 bus.
Bit 14	Transfer Interrupt Enable (XIE ENA) Set to '1' by software to enable interrupt. Set to '0' by software to disable interrupt.
Bit 13	Error Interrupt Enable (ERR ENA) Set to '1' by software to enable interrupt. Set to '0' by software to disable interrupt.
Bit 12	Overwrite Current Buffer (OCB ENA) Set to '1' by software to allow overwrite. Set to '0' by software to prevent overwrite. The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. If the new Data Bit is reset in the next buffer, the data words are stored in the next buffer. If the New Data Bit is set in the next buffer and the Overwrite Current Buffer Bit is set in the current buffer, the data is written to the current buffer. Otherwise, the data is not stored in the buffer and the Missed Data Bit is set in the current buffer.
Bit 11	Overwrite Interrupt Enable (OIE ENA) Set to '1' by software to enable interrupt, when overwrite has occurred. Set to '0' by software to disable interrupt.
Bit 10	Overwrite Condition Occurred (OVR OCC) Set to '0' by software initially, and after it is set by microcode. Set to '1' by microcode when overwrite occurs.
Bit 9	Bus Used Set to '0' initially. During simulation it is set or cleared by microcode. Set to '1' for Bus A. Set to '0' for Bus B.
Bit 8	Missed Data Condition Occurred (MISS DATA) Set to '0' by software initially and after it is set by microcode. Set to '1' by microcode when overwrite occurs. If the New Data bit is set in the next buffer and the Overwrite Current Buffer bit is cleared in this buffer, then the Missed Data bit is set and the data is not stored.
Bits 7-6	Reserved
Bits 5-0	Buffer Word Count (0-63)

Header Word 2

The received word count field is stored by the microcode in Header Word 2 and reflects the number of 1553 data words received from the bus and stored in the buffer. If this same buffer is involved in a transmit message, the received word count field is set to '0' by the microcode (Figure 5-7). Bits 15-6 are reserved and may be non-zero.

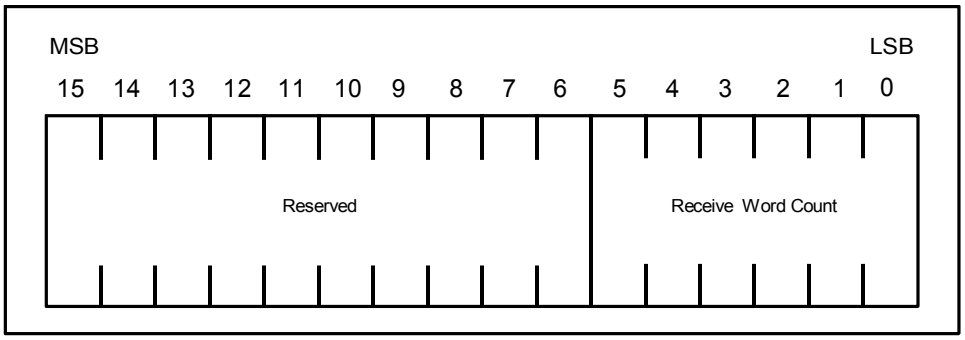


Figure 5-7 Header Word 2

5.6.3 Data Words

All data words transmitted in the 1553 message follow Header Word 2.

5.7 RT Mode Code Response Word Block

The Mode Code Response Word Block (Figure 5-8) is group of 32 words, one for each Mode Code, that specify the operation the mode codes perform. The Mode Code Response Block also specifies if the receipt of any particular mode code causes the GLD-PC to interrupt the host. The first word in the block is placed in free memory between 0x1440 - End of Memory. The remaining words are offset from the initial address by *n*, where *n* = mode code.

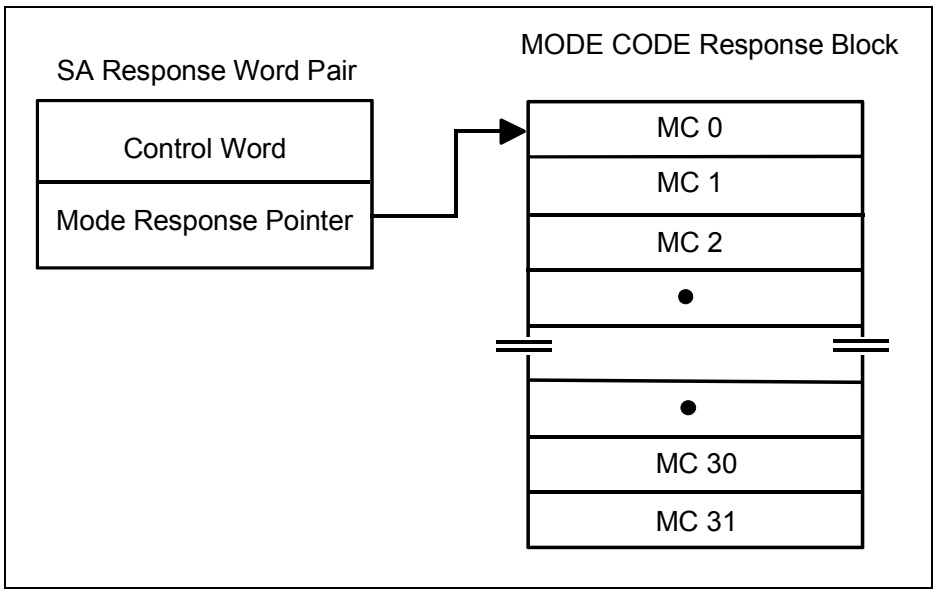


Figure 5-8 Mode Code Response Block

5.8 MODE CODE Response Word

For a mode SA, the message is monitored only if the Monitor Bit (Bit 11) is set in the corresponding MODE CODE response word (Figure 5-9).

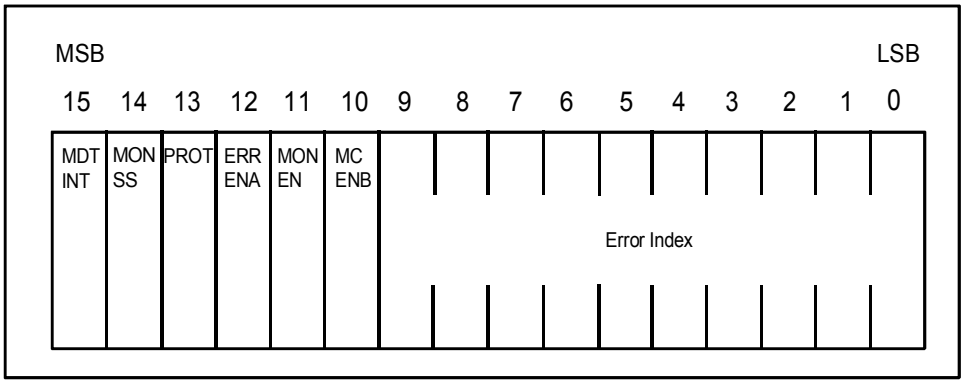


Figure 5-9 Mode Code Response Word

Bit 15 Interrupt on Reception of MODE CODE (MDT INT)
Set to '1' by software to enable interrupt.
Set to '0' by software to disable interrupt.

Bit 14 Monitor Snapshot (MON SS)
Set to '1' by software if message to this subaddress should generate a snap shot interrupt.
Set to '0' by software if snap shot interrupt is not used.

Bit 13 1553 Protocol (PROT)
Set to '0' will declare mode a 1553B type.
Set to a '1' will declare mode to be a 1553A protocol device.

Bit 12 Enable RT Error Injection (ERR ENA)
Set to '1' to enable error injection capability and signal microcode to use the error index.

Bit 11 Monitor Enable (MON EN)
Set to '1' by software if subaddress is to be monitored.
Set to '0' by software if this subaddress is not monitored.

Bit 10 Mode Code Enable (MC ENB)
Set to '1' by software to enable this mode code.

Bits 9-0 Error Index
See Table 4-2, page 4-28 for error-injection codes.

5.9 Description of Mode Code Microcode Operations

The only valid Mode Code for 1553A operation is zero. Table 5-2 describes the Mode Code operations for 1553B.

Table 5-2 MIL-STD-1553B Non-Broadcast Mode Code Microcode Operations (RT 0-30)

MC Number	T/R	Operations Performed By Microcode
0	1	Dynamic Bus Control - Read RT Status Word as Status - If Dynamic Bus Acceptance (DBA) flag set in RT Control Word: Set DBA Bit in Status Word - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
1	1	Synchronize Without Data Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
2	1	Transmit Last Status Word - Read Last Status Word as Status - AND Status with Status Mask - Transmit Status onto Bus - Write Command into Last Command Word
3	1	Initiate Self-Test - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
4	1	Transmitter Shutdown - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Set Bit in RT Control Word to disable opposite bus - Write Status into Last Status Word - Write Command into Last Command Word

MC Number	T/R	Operations Performed By Microcode
5	1	Override Transmitter Shutdown - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Clear bit in RT Control Word to enable opposite bus - Write Status into Last Status Word
6	1	Inhibit Terminal Flag - Read RT Status Word as Status - Clear Terminal Flag Bit in Status - Mask to inhibit terminal flag - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
7	1	Override Inhibit Terminal Flag - Read RT Status Word as Status - Set Terminal Flag Bit in Status Mask to enable terminal flag - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
8	1	Reset Remote Terminal - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Logically AND the BIT Word with the BIT Mask then place the result back in the BIT Word - Clears bits in Control Word to enable both transmitters - Set the Terminal Flag Bit in the Status Mask to enable the Terminal Flag Bit
9-15	0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing

MC Number	T/R	Operations Performed By Microcode
16	1	Transmit Vector Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit Vector Word onto bus - Write Status into Last Status Word - Write Command into Last Command Word
17	0	Synchronize with Data Word - Read RT Status Word as Status - Write the received data to Sync Word - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
18	1	Transmit Last Command - Read Last Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit Last Command Word onto bus
19	1	Transmit BIT Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit BIT Word onto bus - Write Status into Last Status Word - Write Command into Last Command Word
20-31	0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing

Table 5-3 MIL-STD-1553B Broadcast Mode Code Microcode Operations (RT=31)

MC Number	T/R	Operations Performed By Microcode
0	0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing
1	1	Synchronize - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
2	0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing
3	1	Initiate Self Test - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write Status into Last Status - Write Command into Last Command Word - Link to next broadcast RT

MC Number	T/R	Operations Performed By Microcode
4	1	Transmitter Shutdown - Read RT Status Word as Status - Set BRC Bit in Status - Set bit in Master Shutdown Control Register to disable opposite bus - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
5	1	Override Transmitter Shutdown - Read RT Status Word as Status - Set BRC Bit in Status - Clear bit in Master Shutdown Control Register to enable opposite bus - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
6	1	Inhibit Terminal Flag - Read RT Status Word as Status - Set BRC bit in Status - Clear Terminal Flag Bit in status Mask to inhibit Terminal flag - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
7	1	Override Terminal Flag - Read RT Status Word as Status - Set BRC Bit in Status - Set Terminal Flag Bit in Status Mask to enable terminal flag - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT

MC Number	T/R	Operations Performed By Microcode
8	1	Reset RT - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Clear bit in RT Control Word to enable opposite bus - Set Terminal Flag Bit in Status Mask to enable terminal flag - Logically AND the BIT Word with the BIT Mask. Place the result in the BIT Word - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
9-16	0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing
17	0	Synchronize with Data - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write received data to Sync Word - Write Status into Last Status Word - Write Command into Last Command Word - Link to Next Broadcast RT
18-31	0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing

5.10 Interrupts

The RT mode may post hardware interrupts to the host including:

- Mode Code Execution
- Message Transmission or Reception to or from a Message Block
- Message Buffer Overflow Condition
- Valid Transfer
- Receiver Error Detected

6. CM MODE OPERATION

6.1 Overview

The Chronological Monitor (CM) Mode allows the capture of all or selected 1553 bus traffic regardless of other modes enabled at the same time. The GLD-PC board is able to monitor 1553A, 1553B and mixed-bus-traffic systems.

6.2 Data Capturing Methods

The CM mode operates in one of two methods:

- Record all (with and without snapshot)
- Filtered.

Both methods involve setting bits in the Data Subaddress Word Pairs and Mode Code Response Words. These are described in detail in Chapter 5 MRT MODE OPERATION.

6.2.1 Record All

To record all bus traffic, set Bit 11 (Monitor Enable) in every Transmit and Receive Data Subaddress Word Pair for each RT, and also set Bit 11 in each Mode Code Response Word. During active-chronological monitoring a Snapshot Interrupt may be generated for a particular message based on the RT number, subaddress and direction of transmission.

The Snapshot Interrupt causes an interrupt packet to be put into the interrupt queue. This packet contains the memory address within the Monitor Buffer of the first command word in the message. To generate a Snapshot Interrupt, set Bit 14 (Monitor Snapshot) in the appropriate Receive or Transmit Data Subaddress Word Pair. Snapshot interrupts can also be generated for any particular mode code. See Appendix B: INTERRUPTS for details.

6.2.2 Filter

To filter bus traffic and record only specific messages, set only Bit 11 as described above for the particular messages of interest.

6.2.3 Monitoring 1553A Devices

The default setting for all Subaddress Response Word Pairs is for 1553B devices. To monitor any 1553A devices, bit 13 must be set in the Subaddress Response Word Pair for each 1553A subaddress to be monitored.

6.3 Chronological-Monitor Elapsed Timer (ELT)

This timer is used to time-tag messages in the monitor mode. It is a 32-bit value with one-microsecond resolution when using the internal 1 MHz pulse as input. The ELT can be triggered and reset by internal and external clocks or signals. The Elapsed Timer Control Register (Function register 0x17) controls the 32-bit timer for the CM mode.

Writing to this register will do any of the following:

- Enable/disable the ELT
- Read the ELT
- Enable the internal/external clock input
- Reset the ELT

The current status of the ELT can be determined by reading the ELT state (0x1417), ELT HIWD (0x140A), and ELT LOWD (0x140B) registers. The ELT HIWD and LOWD registers are only updated when the "Read" bit is set in the value written to the Elapsed Timer Control Register.

The external elapsed-timer-reset signal is an RS-422 input which resets the ELT to zero upon receipt. The external elapsed-timer-clock input is also an RS-422 signal. This signal allows the user to supply an external clock source for the ELT.

See Appendix C: REGISTERS for details.

6.4 Monitor Block

The monitor block consists of one or more monitor buffers (Figure 6-1). The monitor block requires that the address of the first monitor buffer be written to reserved memory location 0x1408 before monitoring begins. To start monitoring, write a value of 0x0008 to the Chronological Monitor Control Register. This captures all messages selected for monitoring with valid command words. Write a value of 0x18 to have the monitor record 1553 command words containing protocol errors.

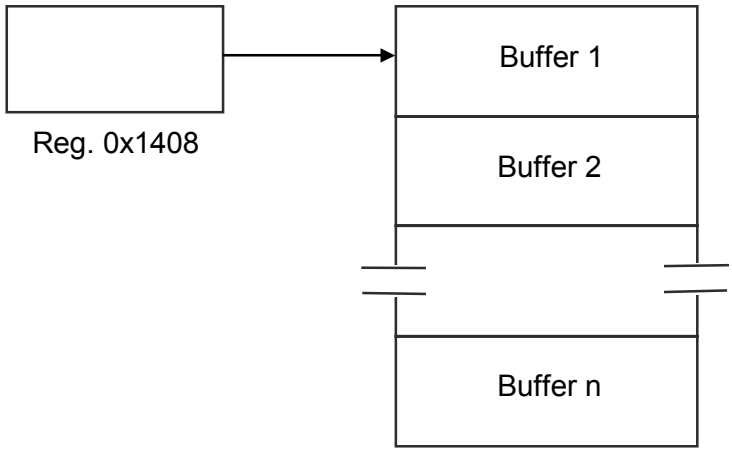


Figure 6-1 Monitor Block

To control the monitor mode:

1. Capture all bus traffic: write a value of 0x0018 to Chronological Monitor Control Register.
2. Capture only bus traffic with valid commands: write a value of 0x0008 to Chronological Monitor Control Register.
3. Stop operation of the chronological monitor mode at any time: write 0x0000 to the Register. This will not affect operation of the BC or MRT modes.

6.5 Monitor Buffer

The size of a monitor buffer ranges from 16 to 1008 (63*16) words for boards running microcode revision D or later. Revision E microcode requires a minimum Monitor Buffer length of 80 words (Figure 6-2). The buffer begins with a link word and a header word and ends with two reserved words. The remainder of the buffer (Message Records) is used to store 1553 messages and information related to the message, regarding error and time tagging (see subsection 6.8.1).

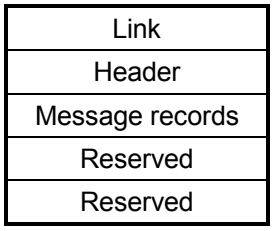


Figure 6-2 Monitor Buffer

6.5.1 Monitor Buffer Link Word

The first word of a monitor buffer, the link word, contains the address of the next monitor buffer. The link word of the last buffer must hold the address of the first buffer (Figure 6-3) to ensure a circular queue. User software is responsible for loading the correct value into the link word of each buffer.

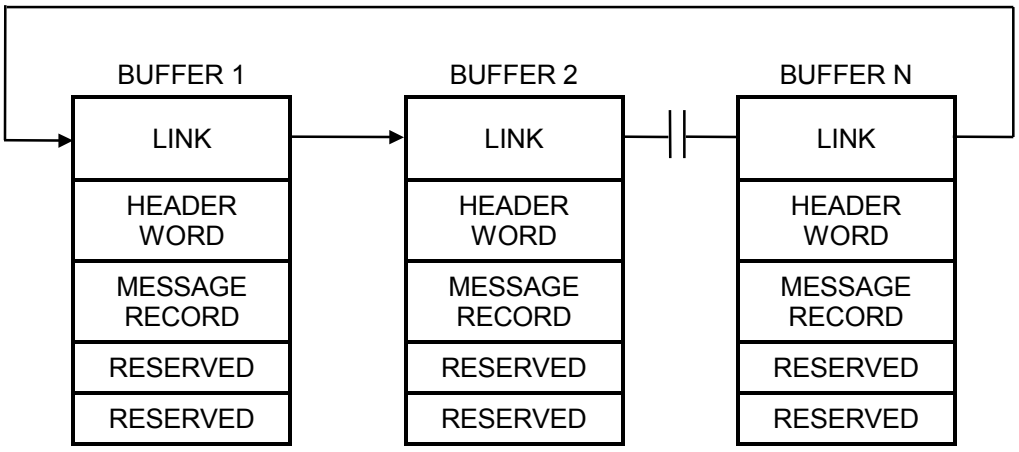


Figure 6-3 Monitor Buffer Link Word

6.5.2 Header Word

The header word (Figure 5-4) contains the control and status bits and buffer block count.

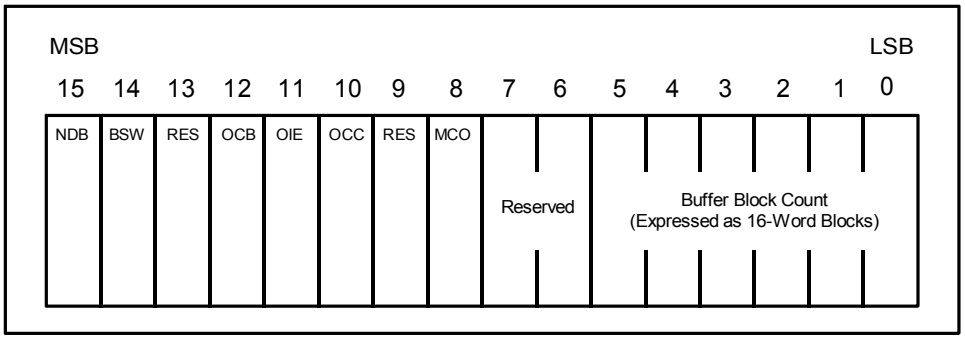


Figure 6-4 Header Word

Bit 15 — New Data Bit (NDB)
Set to '1' by microcode to indicate new data recorded.
Set to '0' by software after data is read to indicate buffer is available for message receipt.

Bit 14 — Buffer Switch Interrupt Enable (BSW)
Set to '1' by software to generate an interrupt when switching from current buffer to next buffer.
Set to '0' by software to disable interrupt.

Bit 13 — Reserved

Bit 12 — Overwrite Current Buffer (OCB)
Set to '1' by software to allow overwrite.
Reset to '0' by software to prevent overwrite.
The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. If the New Data Bit is set in the next buffer and the Overwrite Current Buffer Bit is set in this buffer, the data is written into this buffer.

Bit 11 — Overwrite Interrupt Enable (OIE)
Set to '1' by software to enable interrupt.
Set to '0' by software to disable interrupt.

Bit 10 — Overwrite Condition Occurred (OCC)
Reset to '0' by software initially.
Set to '1' by microcode when an overwrite condition occurs.

Bit 9 — Reserved

Bit 8 — Missed Data Condition Occurred (MCO)
Set to '0' by software initially.
Set to '1' by microcode when missed data occurs.
If the overwrite Current Buffer is not set and the new data bit in the next buffer is set, then data is not stored and this bit is set in this buffer.

Bits 7-6 — Reserved

Bits 5-0 — Buffer Word Count (0-63) (see subsection 6.8.1).
Multiply this number by 16 to get actual buffer size.

6.6 Message Record

When a message is monitored, it is stored in a message record (Figure 6-5). Each message will be stored in its own message record. There can be many message records in one message buffer, depending on the length of the buffer. A word of the message followed by its tag word alternates until the message is finished.

Reserved
Start of Message
ELT (MSW)
ELT (LSW)
First Word Of Message
Tag Word
Second Word of Message
Tag Word
Third Word of Message
Tag Word
• • •
Last Word Of Message
Tag Word

Figure 6-5 Message Record Format

The words of a message will vary, depending on the message types. For example:

Message Type	First Word of Message	Second Word of Message	Third Word. Of Message	Fourth Word of Message
BC - RT	Receive Cmd.	Data Word 1	Data Word 2	- - -
RT - BC	Transmit Cmd.	Status Word	Data Word 1	- - -
RT - RT	Receive Cmd.	Transmit Cmd.	Transmit Status Word	Data Word 1
Mode (no data)	Mode Cmd.	Status Word	0x0000	
Transmit Mode (data)	Mode Cmd.	Status Word	Data Word	
Receive Mode (data)	Mode Cmd.	Data Word	Status Word	

START OF MESSAGE WORD

Microcode stores the hexadecimal word CODE, indicating this is the start of the message.

ELAPSED TIMER WORD ELT (MSW)

The most-significant 16 bits of the elapsed timer.

ELAPSED TIMER WORD ELT (LSW)

The least-significant 16 bits of the elapsed timer are stored next.

TAG WORD

Figure 6-6 shows the format of the tag word.

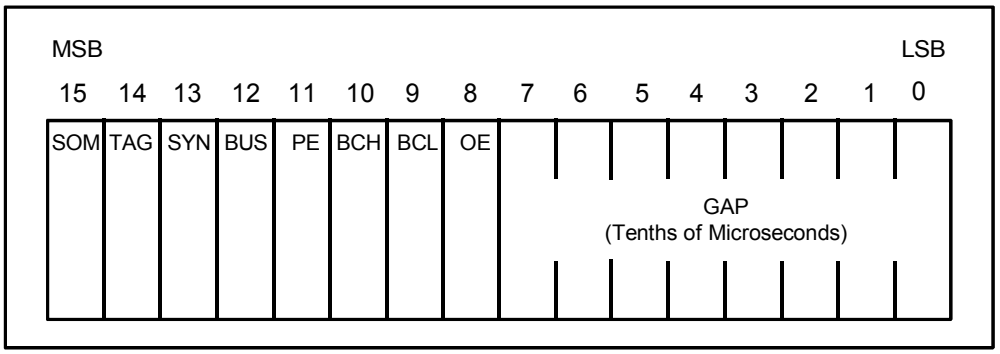


Figure 6-6 Tag Word

Bit 15 — Start of Message (SOM)
Bit 15 is set if this is the first word of the message.

Bit 14 — Tag (TAG)
Bit 14 is set in every tag word, including start of message tag.

Bit 13 — Sync of Word (SYN)
Bit 13 is set if command or status word and reset if data word.

Bit 12 — Data Received From Bus (BUS)
Bit 12 is set if tag word appeared on Bus A and reset if tag word appeared on Bus B.

Bit 11 — Parity Error (PE)
Bit 11 is set if parity error appeared in this word.

Bit 10 — Bit Count High (BCH)
Bit 10 is set if bit count high error occurred in this word.

Bit 9 — Bit Count Low (BCL)
Bit 9 is set if bit count low error occurred in this word.

Bit 8 — Other Error (OE)
Bit 8 is set if another error (sync, bi-phase, etc.) occurs in this word.

Bits 7-0 — Gap Time (+/-200 nanoseconds)
Expressed as tenths of microseconds (For example, if value = 0x34 or 52 decimal, gap time = 5.2 microseconds).

6.6.1 Split Message Records (Rev. D Microcode or Earlier)

When a complete message record cannot be stored in a single message buffer, it will be split between the current message buffer and the next one in the linked list. Figure 6-7 shows an example of how this is done.

Link2
Header
Reserved
Start of Message
ELT (MSW)
ELT (LSW)
First Word Of Message
Tag Word
Second Word of Message
Tag Word
Third Word of Message
Tag Word
Last Word Of Message 1
Reserved (0000)
0000

→→→

Link N
Header
Fourth Word of Message
Tag Word
Fifth Word of Message
Tag Word
•
•
•
Rest of Messages

Figure 6-7 Split Message Record

6.7 Buffer Switching (Rev. D Microcode or Earlier)

Link2	→→→	Link N
Header		Header
•		Reserved
•		Start of Message)
•		Start of Message (0xC0DE)
Reserved		ELT (MSW)
Start of Message		ELT (LSW)
ELT (MSW)		First Word Of Message
ELT (LSW)		Tag Word
First Word Of Message		Second Word of Message
Tag Word		Tag Word
Second Word of Message		•
Tag Word		•
•		•
•		Last Word Of Message
•		Tag Word
Last Word Of Message		Reserved (0000)
Tag Word		0000
Reserved (0000)		•
0000		•
•		•
•		Rest of Buffer
•		
Less than 10 Words		

Figure 6-8 Message Record Storage With Buffer Switch Alignment

If fewer than ten words appear in the message record buffer (eight words for storing 1553 information and two reserved words at the end of the buffer), the microcode will switch buffers and store the complete message in the next message buffer. (Figure 6-8).

The message record ends with a reserved word, followed by a word of zeroes. These two words serve as an end-of-buffer indicator. If there are more than ten words left in the buffer, these words are overwritten by the next message record. If no more messages are captured, the end-of-buffer indicator signals the end of monitored information in this buffer.

As each word of the 1553 message and its tag word are stored in the buffer, the end-of-buffer indicator is written after the tag word; however, when the next word of the message is stored with its tag word, the end-of-buffer indicator is overwritten and a new end-of-buffer indicator is written after the tag.

If during receipt of a message the end of a buffer is reached, then the microcode automatically switches buffers and continues the message storage after the buffer header word. (Figure 6-8).



NOTE: In Chronological Monitor mode the start of a command signals the microcode to begin storage of a record. This involves writing the first four words of a record (reserved, start of message, ELT MSW ELT LSW) in preparation for the 1553 command word. If the monitor is not to store the message (SA is disabled for monitoring), then the end of buffer words will have been overwritten.

To avoid confusion, enable all RT Subaddresses when using monitor mode. This will also give a more accurate record of the 1553 bus activity for off-line data analysis.

6.8 Buffer Switching (Revision E Microcode or Greater)

A feature has been added to the microcode for the GLD– series 1553 products. This feature aids in processing values from the chronological-monitor buffer.

When the microcode has finished writing a complete 1553 command sequence to the monitor, it stores the address of the last tag word. This value is written into the very last word of the chronological-monitor buffer. This allows easy determination as to where the last complete message ends.

This microcode has also been modified so it does not split messages between buffers. The microcode changes to another buffer if there is not room left for a 78-word message. A 78-word buffer is the maximum size of a 1553 RT-RT message including tag words (76 words) and two words reserved to keep track of the last message's tag word. See Figure 6-9 for details.

6.8.1 Monitor Buffer Size (Revision E.5 or Later)

Additional buffer sizes of 4 K and 2 K have been added to the Chronological Monitor for users who require larger buffer sizes beyond 1 K. This feature is only supported in microcode revision E.5 or later. Bits 6 and 7 of the Monitor Header Word (see subsection 6.5.2) are now used to expand the buffer size from 16 to 4000.

Link1	→→→	Link N
Header 1		Header N
Reserved (0x0000)		Reserved (0x0000)
Start of Message (0xC0DE)		Start of Message (0xC0DE)
ELT (MSW)		ELT (MSW)
ELT (LSW)		ELT (LSW)
First Word Of Message 1		First Word Of Message 1
Tag Word		Tag Word
Second Word of Message 1		Second Word of Message 1
•		•
•		•
Last Word Of Message 1		Last Word Of Message 1
Tag Word		Tag Word
Reserved (0x0000)		Reserved (0x0000)
Start of Message (0xC0DE)		Start of Message (0xC0DE)
ELT (MSW)		ELT (MSW)
ELT (LSW)		ELT (LSW)
First Word Of Message n		First Word Of Message n
Tag Word		Tag Word
Second Word of Message n		Second Word of Message n
•		•
•		•
Last Word Of Message n		Last Word Of Message n
Last Tag Word		Last Tag Word
Reserved (0x000)		Reserved (0x000)
0x0000		0x0000
• 78 Words or less •		• 78 Words or less •
Address of Last Tag Word		Address of Last Tag Word

Figure 6-9 Rev.E Microcode Buffer-Switch Mechanism



NOTE: These changes require that chronological-monitor buffers must be at least 80 words long. Versions of the microcode prior to Revision E do not include the described enhancements.

APPENDIX A

SPECIFICATIONS

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A.1 Hardware Specifications A-1
A.2 Board Dimensions A-2

A.1 Hardware Specifications

Hardware Compatibility:	MIL-STD-1553
System Minimum Recommended	PC-386, EISA/ISA (1EEE 996)
Physical Dimensions:	332.74 mm x 111.76 mm (full slot)
Weight:	
Dual Channel	13 oz.
Single Channel	10 oz
Electrical Requirements:	
Single Channel Max Power	5 V @ 2.4 Amps +12 V @ .19 Amps -12 V @ .0125 Amps
Dual Channel Max Power	5 V @ 4.2 Amps +12 V @ .38 Amps -12 V @ .05 Amps
Temperature Range:	
Storage	-20° to 85° Celsius
Operation	0° to 55° Celsius
Humidity Range:	
Storage	0% to 95% (noncondensing)
Operation	10% to 90% (noncondensing)
Communication:	MIL-STD-1553A or B protocol
Data Size Supported:	Memory: D16 Registers: D16
Interface to Bus:	Transformer or direct coupling
Memory:	32 K words of Dual-Port RAM per channel

A.2 Board Dimensions

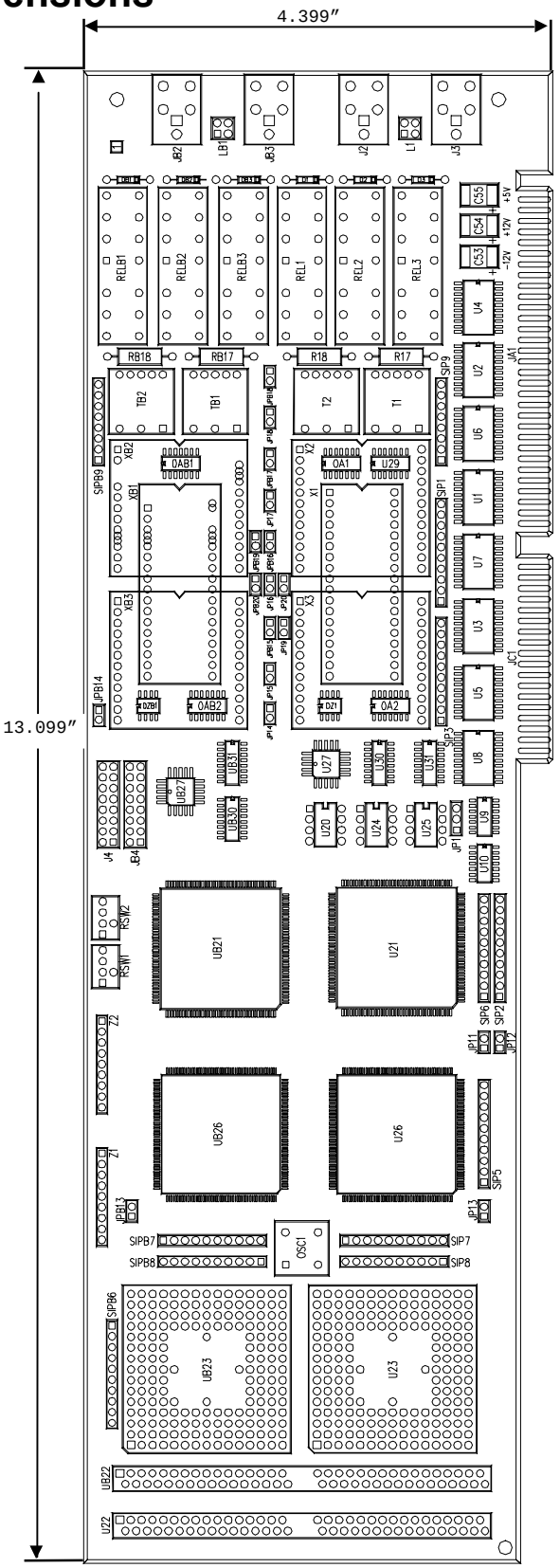


Figure A-1 GLD-PC Dimensions

APPENDIX B

INTERRUPTS

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B.3 Algorithm for Interrupt Processing B-6

B.1 Overview

Table B-1 lists the GLD-PC interrupt types and identifies the operational modes upon which the interrupts may be enabled.

Table B-1 GLD-PC Interrupts

Event	Mode
Protocol Error	MRT/BC
Buffer Overflow	MRT/BC
Mode Code	MRT/BC
Receive Transfer	MRT/BC
Transmit Transfer	MRT/BC
Monitor Buffer Switch	CM
Snapshot	CM
Asynchronous Halt	BC
Instruction Complete	BC
Halt	BC
Status Exception	BC

When an interrupt occurs, the board generates an interrupt packet and places it at the bottom of the interrupt queue (Table B-2). Read the Interrupt Queue Control Real-Time Control Register 0x1409 to determine the beginning of the linked list from which to de-queue interrupts. Once the application software reads this pointer it must write a '0' to the Interrupt Queue Control Real-Time Control Register 0x1409. This instructs the microcode not to add interrupt packets to the linked list under process and to start a new list.

The trailer word is used to determine the modes and events that generated the packet. If the interrupt queue is filled, the Queue Full Bit is set in the Trailer Word and no more interrupts are stored in the queue. When the application software processes existing packets, a '0' must be written to the Valid Interrupt Word in each packet to return the packet to the queue.



NOTE: A hardware interrupt is only generated when the microcode writes the address of a valid interrupt packet to the Interrupt Queue Control Register 0x1409.

B.2 Interrupt Packet

The GLD-PC adds packets to the interrupt queue without generating a hardware interrupt, as long as the Interrupt Queue Control Register has a non-zero value (indicating the software has not begun processing interrupt packets).

Table B-2 Interrupt Packet

Word	Definition	Notes
0	Forward Link Word	
1	Receive Command	
2	Transmit Command	
3	Transmit Data Buffer Address	
4	Transmit Status or Mode Code Receive Data Word	
5	Receive Status or Mode Code Transmit Data Word	
6	Receive Error Word or Receive Data Buffer Address	→ Reserved for transmit mode codes and if monitoring only
7	Bus Controller Instruction Address	→ BC mode only; all others reserved
8	Buffer Switch Monitor Address	→ Monitor mode only; all others reserved
9	Command Word Address Pointer	→ Monitor mode snapshot pointer; all others reserved
10	Trailer Word	
11	Valid (FFFF)	
12	Reserved	
13	Reserved	

Word 0 **Forward Link Word**

This word stores the address of the next interrupt contained in the linked list of interrupts. A ‘0’ indicates this is the last interrupt in the linked list.

Word 1 **1553 Receive Command Word**

If the message doesn't contain a Receive Command Word, a value of ‘FFFF’ is written to this word.

Word 2 **1553 Transmit Command Word**

If the message doesn't contain a Transmit Command Word, a value of ‘FFFF’ is written to this word.

Word 3 **Transmit Data Buffer Address**

Contains the address of the first word of the transmit buffer. A value of ‘FFFF’ indicates that this word is unused.

Word 4 **1553 Transmit Status or Mode Code Receive Data Word**

Stores a 1553 status word if one exists. If this message is a Mode Code 17 (Sync with Data), this is the data sent to the RT. If there is no Transmit Status word and this message is not a MODE CODE 17, the value ‘FFFF’ is stored in this word.

Word 5 **1553 Receive Status or Mode Code Transmit Data Word**

Stores a 1553 receive status word or the data word received from a Mode Code transfer. If there is no receive status or transmitted mode data word a value of 'FFFF' is written.

Word 6 **Receive Error Word or Data Buffer**

Address points to Word 1 of Receive Data Buffer or Receive Error Word, if an error was detected. A value of 'FFFF' indicates this word is unused. The value is reserved for all transmit Mode Codes.

MRT Receive Error Word

Bit 15 No Response
Bit 15 is set if the RT detects an error in data reception and does not respond with its status.

Bit 14 Word Count High
Actual word count exceeds command word count.

Bit 13 Word Count Low
Actual word count is less than command word count.

Bit 12 Wrong Sync
The 1553 receive logic expected a sync other than what was received.

Bit 11 Wrong Bus
A word has been received on the opposite bus from the command.

Bit 10 Manchester Error
A Manchester or parity error has occurred on the message received.

Bit 9 Mode of Operation
If set to '1', the receiver is the BC.
If set to '0', the receiver is an emulated RT.

Bit 8 Buffer Overflow
Indicates that a buffer overflow condition occurred and the Interrupt Overflow Error Bit was set in the receiving Message Block header. See description of overwrite current buffer bit (header Bit 12) in message block header. For details, refer to Chapter 4, BC MODE OPERATION, Section 4.4.1, Header Word 1 definition.

Bit 7-0 Reserved

BC Receive Error Word

Bit 15 No Response
Bit 15 is set if the RT detects an error in data reception and does not respond with its status.

Bit 14 Word Count High
Actual word count exceeds command word count.

Bit 13 Word Count Low
Actual word count is less than command word count.

Bit 12 Wrong Sync
The 1553 receive logic expected a sync other than what was received.

Bit 11 Wrong Bus
A word has been received on the opposite bus from the command.

Bit 10 Manchester Error
A Manchester or parity error has occurred on the message received.

Bits 9-0 Reserved

Word 7 **Bus Controller Instruction Address**

If in BC mode, Word 7 points to Word 1 of the current four-word BC instruction. If not in BC mode, this word is reserved.

Word 8 **Buffer Switch Monitor Address**

If ten words* or less remain in the current monitor buffer and the Buffer Switch Interrupt is enabled, a Buffer Switch Interrupt occurs during the last word to be stored. Word 8 points to the first word of the monitor buffer just filled.

Word 9 **Command Word Address Pointer**

If a Snapshot Interrupt is enabled for this command, Word 9 contains the address for the first Command Word of the transfer within the Monitor Buffer per the corresponding 1553 transfer.

Word 10 **Trailer Word**

As the last word in an interrupt packet (Figure B-1), the Trailer Word defines valid interrupt types and sources for the corresponding 1553 message.

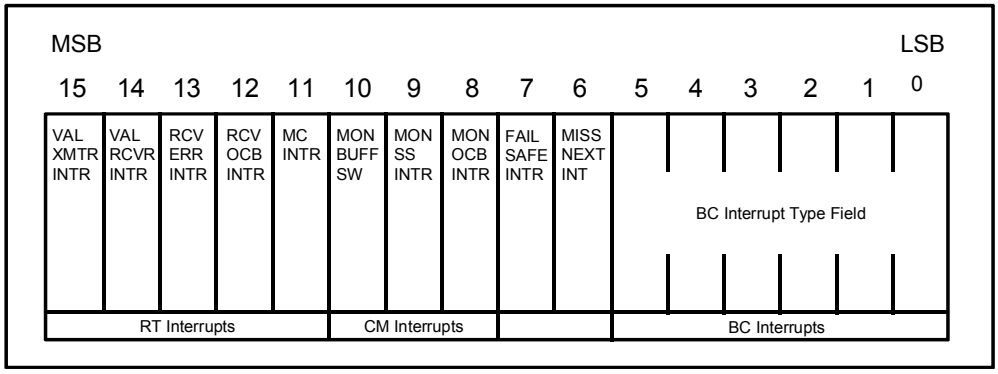


Figure B-1 Trailer Word

* See Section 6.8 if revision E microcode or greater.

MRT Interrupts (Bits 15-11)

If any of the interrupt bits are enabled in the Message Buffer Header or the Mode Interrupt is enabled in the Mode Code Response Word, the corresponding bit is set in the Trailer Word. The MRT Interrupts are defined below:

Bit 15 Valid Transmitter Interrupt
The transmit RT and SA were emulated for the transfer.

Bit 14 Valid Receiver Interrupt
The Receive RT and SA were emulated for the transfer.

Bit 13 Receiver Error Interrupt
The RT Mode detected an error on the received data.

Bit 12 Receiver Overwrite Current Buffer Interrupt
When Bit 12 is set, Bit 14 is never set. The emulated RT buffer had the Overwrite bit set and the New data bit was set in the buffer data was to be stored.

Bit 11 Mode Code Interrupt
The RT emulated the Mode Code transfer.

Bits 10-8 Monitor Interrupts

If any of the interrupt bits are enabled in the Monitor Buffer Header Word or any of the monitor interrupt bits are enabled in the Mode Code Response Word, the corresponding bit is set in the Trailer Word.

Bit 10 Monitor Buffer Switch Interrupt
A buffer switch occurred during this message.

Bit 9 Monitor Snapshot Interrupt
Posts the address of the Command Word for the corresponding message in the second to the last word of the packet. If the transfer was RT-to-RT, the address of the Transmit Command is written.

Bit 8 Monitor Overwrite Current Buffer Interrupt

Bits 7-0 Other Interrupts

Bit 7 Fail-safe Interrupt
If set to '1': a continuous 1553 transmission of greater than 720 microseconds has occurred causing a transmitter shutdown. Jumper header JP13 and/or JPB13 must also be removed.

Bit 6 Miss Next Interrupt
1 = Interrupt queue overflowed after this block.
0 = No interrupt overflow occurred.

Bits 5-0 BC Interrupts
Bits 5-0 specify a six-bit field that displays the BC interrupt type in the Hexadecimal format (Table B-3).

Table B-3 Bus Controller Interrupts

Hex Value	Interrupt Type
2	BC Mode Code Instruction Complete
3	BC Transfer Data
4	Instruction Complete (Includes Jump, HUE, etc.)
18	BC Overrun
6	BC Halt
8	Status Exception
10	Protocol Error
7	BC Transfer/Instruction Complete
B	BC Transfer/Status Exception
A	BC-MC/Status Exception
F	BC Transfer/Instruction Complete/Status Exception
C	Instruction Complete/Status Exception
14	Instruction Complete/Protocol Error
1F	BC Over/BC Transfer/Instruction Complete
2X	Asynchronous Halt/ etc.

Word 11 **Valid Interrupt (FFFF)**

Word 11 is set to a non-zero value when the GLD-PC adds the packet to the interrupt queue. The user's software must write a zero to this word when it has finished processing this packet.

Word 12 **Forward Link**

Reserved for microcode use.

Word 13 **Reverse Link**

Reserved for microcode use.

B.3 Algorithm for Interrupt Processing

To process interrupts, follow the steps outlined below:

1. Read the value of the Interrupt Control Register to a variable in your program.
2. Write a '0' to the Interrupt Control Register.
3. Process the packet (application dependent).
4. Read the Link Word in the packet.
5. Write a '0' to the Valid Interrupt Word to return the packet.
6. Repeat Steps 3 through 5 until the Link Word equals zero.
7. Re-enable system interrupts.

APPENDIX C

REGISTERS

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C.1 Overview

Three types of registers control GLD-PC operation:

- The I/O-mapped Configuration Registers
- Real-Time Control Registers
- Function Registers.

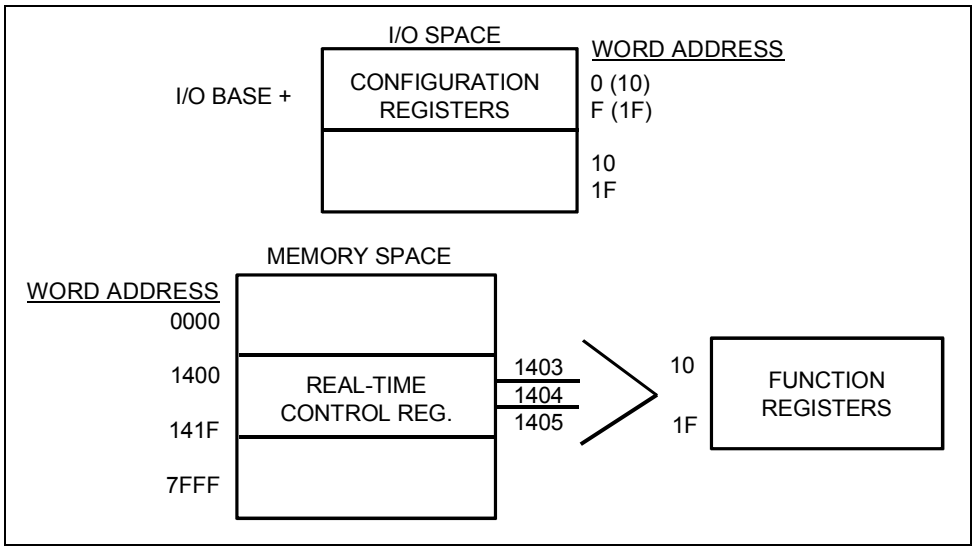


Figure C-1 Types of Register Controls

C.2 Configuration Registers

Initialize the Configuration registers when the board is powered on. These registers are controlled by user I/O functions and must be mapped into the host I/O space.

Thirty-two registers are defined at the selected host I/O address. This I/O address is selected using Switch Banks 1 and 2 (See Chapter 3, INSTALLATION, for more information on I/O addressing.) The first 16 locations are reserved for Channel 1. These register definitions are duplicated in the next 16 locations for Channel 2 (the second channel is an option and might not be installed in your board). Set up all write registers for both channels to provide correct dual-channel operation.

Table C-1 Initialization Registers

Register Number	Register Name	Access Method	Channel
0	ID	READ	1
1	Device Type	READ	1
2	Control	READ/WRITE	1
3	Memory Base	READ/WRITE	1
5	Interrupt Level	READ/WRITE	1
10	ID	READ	2
11	Device Type	READ	2
12	Status/Control	READ/WRITE	2
13	Memory Base	READ/WRITE	2
15	Interrupt Level	READ/WRITE	2

C.2.1 ID Register 0x00, 0x10

This read–only register provides a Manufacturer ID and can be used to verify that the board is based correctly. A read from I/O offset 0x00 yields a value of 0x0FB4 if all settings are correct. For a dual–channel board, a read from I/O offset 0x10 also yields a value of 0x0FB4.

C.2.2 Device Type Register 0x01, 0x11

This read–only register provides a Device Type and can be used to verify the board is based correctly along with the present version of the board. A read from I/O offset 0x01 yields a value of 0x0220 for a dual–channel board and a value of 0x0210 for a single channel board. For a dual–channel board, a read from I/O offset 0x11 also yields a value of 0x0220.

C.2.3 Control Register 0x02, 0x12

A Control register at I/O offset 0x02 must be configured before the board becomes operational.

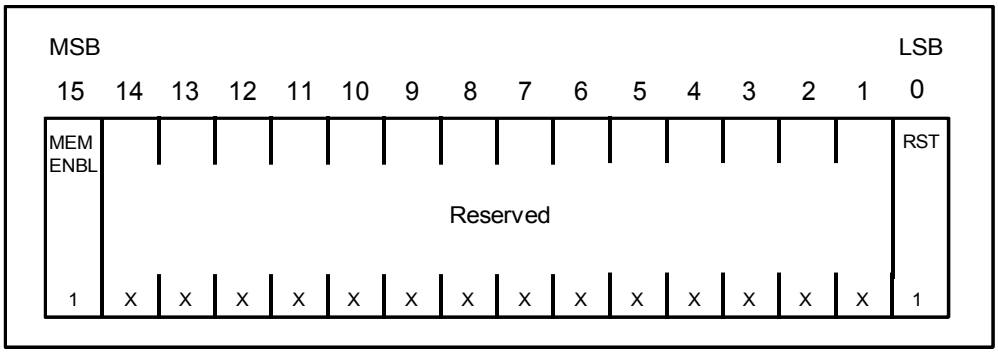


Figure C-2 Control Register 0x02, 0x12

At power-up, Bit 15 is reset so that the host does not allocate board memory as system memory. This bit must be set to '1' to enable board memory and to allow the board to function properly.



NOTE: On a dual–channel board, each channel contains a bit that controls memory enable. If both channels are set to the same page address, only enable the memory for one channel at any given time to avoid conflict with the PC interface.

Writing to the Control register with a '1' in the least significant position performs a reset of the GLD-PC hardware.

For a dual–channel board, the register at offset 0x12 for the second channel must also be configured.

C.2.4 Memory Base Register 0x03, 0x13

The Memory Base register at I/O offset 0x03 must be set with the address of an available page in memory.

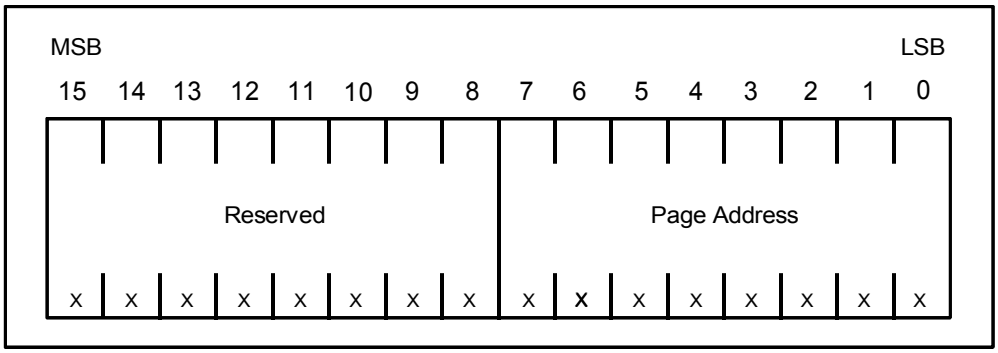


Figure C-3 Memory Base Register 0x03, 0x13

The Page Address matches the address lines 23-16 on the host bus to identify accesses to the board.

On a dual–channel board, the Memory Base register for each channel must be programmed. Both channels of a dual–channel board can be set to the same memory base address, but the software must only enable one channel at a time.

C.2.5 Interrupt Level Register 0x05, 0x15

This register sets the interrupt level and also enables interrupts.



NOTE: Interrupts 3, 5, 10, 11, 12 and 15 are the only valid interrupt levels.

If an invalid interrupt level is selected, the next highest interrupt level is automatically selected. For example, if Interrupt Level 0110 (Interrupt Level 6) is selected, Interrupt Level 10 is automatically selected.

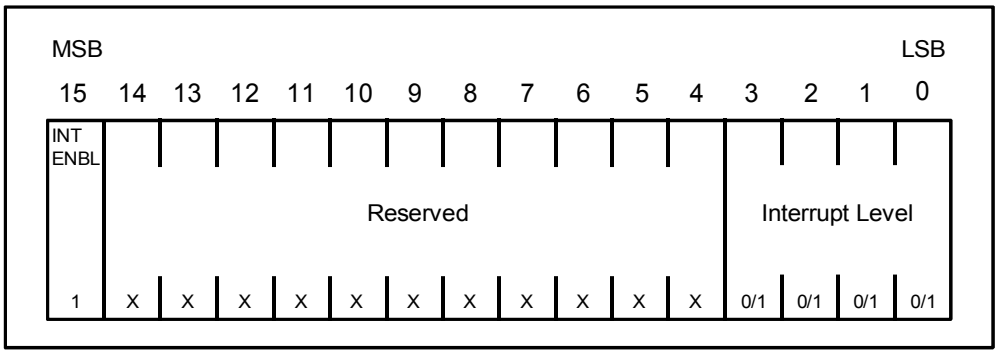


Figure C-4 Interrupt Level Register 0x05, 0x15

Bits 15 Set to '1' to enable interrupts.
Set to '0' to disable interrupts.

Bits 3-0 The interrupt level is a binary encoded value. For example:
Set to '0101' to select Interrupt Level 5.
Set to '1100' to select Interrupt Level 12.

For a dual-channel board, the register at offset 0x15 for the second channel must also be configured.

C.3 Real-Time Control Registers

The Real-Time Control registers, located in on-board memory, supply important information such as operating mode status (Table C-2). These registers can be accessed at any time (even when traffic exists on the 1553 bus) without degrading the performance of the GLD-PC. The memory base address for these registers is at offset 0x1400.

To calculate the register address:

Channel Base Memory Address + 0x1400 + Register Number

Table C-2 Real-Time Control Registers

Memory Address	Register Name	Access Method
0x1400	Alignment	Read *
0x1401	Board Type	Read *
0x1402	Firmware Version	Read *
0x1403	Master Control	Read/Write
0x1404	Register Control	Read/Write
0x1405	Register Value	Write
0x1406	BCMRT Status	Read
0x1407	Monitor Status	Read
0x1408	Monitor Buffer Control	Read/Write
0x1409	Interrupt Queue	Read/Write
0x140A	ELT HIWD	Read
0x140B	ELT LOWD	Read
0x140C	RT 0-15 Broadcast Enable	Read/Write
0x140D	RT 0-15 Shutdown Enable	Read/Write
0x140F	RT 16-31 Broadcast Enable	Read
0x1410	RT 16-31 Shutdown Enable	Read/Write
0x1413	BC Trigger Status	READ
0x1414	Threshold	Read
0x1415	Amplitude State	Read
0x1416	Relay State	Read
0x1417	ELT State	Read
0x1418	Current Buslist Inst. Address	Read
0x141A	BC Start Trigger Address	Read/Write

* These registers are only updated after a microcode load. Any accidental write to these memory locations will result in incorrect read values.

C.3.1 Alignment Register 0x1400

When read, a value of 0x1553 is returned, indicating that the board has been successfully mapped.

C.3.2 Board Type Register 0x1401

When read, a value of 0x4200 is returned, identifying the board as a GLD-PC.

C.3.3 Firmware Version Register 0x1402

When read, the current version of the on-board firmware is returned.



NOTE: The Master Control, Register Control and the Register Value registers are used to access the Function registers. (For more information on how to access the Function registers, see page C-16.)

C.3.4 Master Control Register 0x1403

This register acts as a safeguard against any unintentional accesses to the Function Registers. A value of 0x1553 must be written to this address by the software prior to all register accesses. If the 0x1553 value has been changed, access to any of the GLD-PC Function registers is denied.

C.3.5 Register Control Register 0x1404

The Register Control register identifies the Function Register to be accessed and indicates when the access is in progress. The user software loads the function register offset into the Register Number Field (Bits 5-0) of this register and writes a '1' to Bit 15.

Bit 15	Register Access Pending Bit Bit 15 indicates if a register access is in progress. The software polls Bit 15 for a value of '1' or '0'. If the value is '1', the microcode examines Bits 5-0 of the Register Control Register and performs the register function loaded by the user. When the register access is completed, the microcode clears this bit to allow another register access to occur.
Bits 14-6	Reserved
Bits 5-0	Register Number Field Bits 5-0 indicate the function register number to be accessed.

C.3.6 Register Value Register 0x1405

This register contains the data value to be written into the register number specified in Bits 5-0 of the Register Control Register 0x04.

C.3.7 BCMRT Status 0x1406

A read of this register allows the user to view the current operating modes and status of execution.

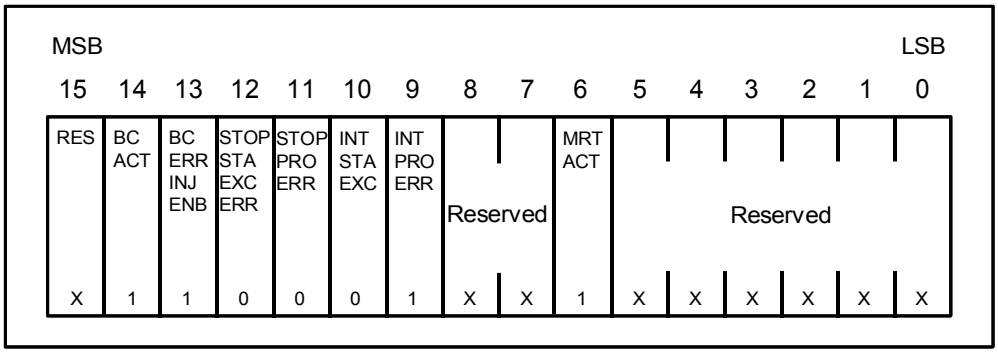


Figure C-5 BCMRT Status Real-Time Register 0x1406

Bit 15 Reserved

Bit 14 BC Active (BC ACT)
If set to '1', the BC is active and executing buslist instructions. Bit 14 is reset by the firmware when the BC executes a Halt instruction or the user writes zeroes to the BC Control Register.

Bit 13 BC Error Injection Enabled (BC ERR INJ ENB)
If set to '1', error injection for the BC is enabled.

Bit 12 Stop On Status Exception Error (STOP STA EXC ERR)
If set to '0', the BC stops if it receives a status response from an RT with any Bits 10-0 set.

Bit 11 Stop On Protocol Error (STOP PRO ERR)
If set to '0', the BC stops if it detects a protocol error.

Bit 10 Interrupt On Status Exception (INT STA EXC)
If set to '1', the BC generates an interrupt when it receives a status response from an RT with any Bits 10-0 set.

Bit 9 Interrupt On Protocol Error (INT PRO ERR)
If set to '1', the BC generates an interrupt when a protocol error is detected.

Bits 8 and 7 Reserved

Bit 6 MRT Active (MRT ACT)
If set to '1', the MRT mode is activated. Bit 6 reflects accesses to the MRT Control Register and is reset by the firmware when zeroes are written to the MRT Control Register.

Bits 5-0 Reserved

C.3.8 Monitor Status Register 0x1407

A read of this register returns the operational status of the Chronological Monitor. The possible values, set in the Chronological Monitor Control Register, are:

0x0008	-	Monitor is active, will only capture all messages with valid commands.
0x0018	-	Monitor is active, will capture all bus traffic.
0x0000	-	Monitor is not active.

C.3.9 Monitor Buffer Control Register 0x1408

When read, the starting memory address of the current monitor buffer is returned.

C.3.10 Interrupt Queue Control Register 0x1409

When read, a '0' indicates the interrupt queue is empty. If the microcode writes any other value to this register, this value represents the address of the first packet to be processed by the software. Software writes a '0' to this register to notify microcode that processing of the queue has started.

C.3.11 ELT HIWD Register 0x140A

The ELT HIWD is loaded into this location after a value is written to the ELT Control Function Register 0x17 with bit 11 set to '1'.

C.3.12 ELT LOWD Register 0x140B

The ELT LOWD is loaded into this location after a value is written to the ELT Control Function Register 0x17, with bit 11 set to '1'.

C.3.13 Broadcast Enable Registers (0x140C, 0x140F)

An RT is notified of broadcast commands if the RT is enabled and the bit corresponding to this RT is set in the appropriate Broadcast Notification Word. Two words of BIU memory, at memory addresses 0x140C (Figure C-6) and 0x140F (Figure C-7), indicate the RTs to be notified of broadcast messages.

To notify RTs 0, 5, 10, 15, 20, 25 and 30 of broadcast messages, the value of 0x8421 is loaded into BIU address 0x140C and 0x4210 is loaded into BIU address 0x140F. It is not necessary to set the bit corresponding to RT31.

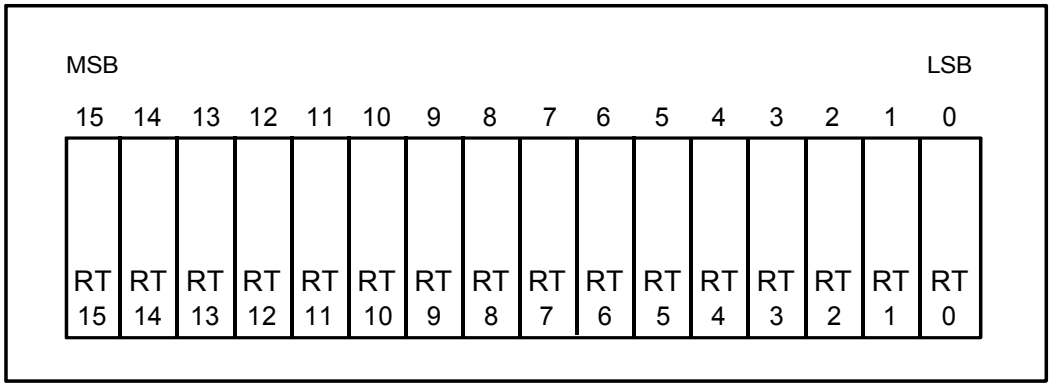


Figure C-6 RT 0-15 Broadcast Enable Register 0x140C

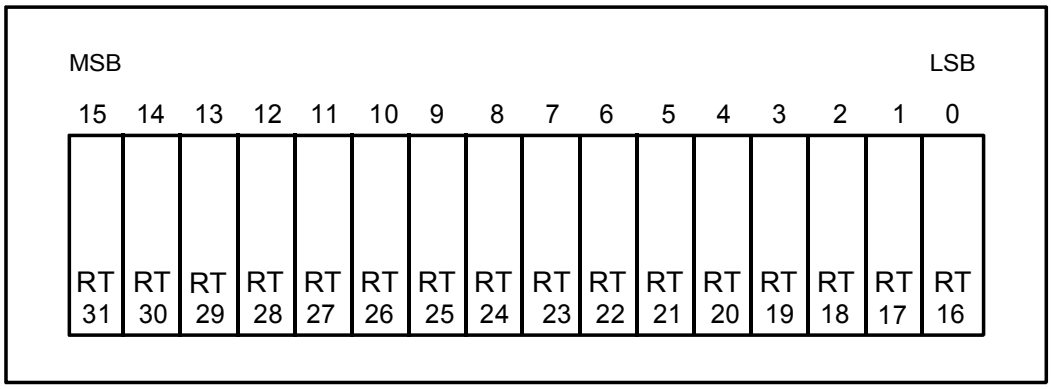


Figure C-7 RT 16-31 Broadcast Enable Register 0x140F

To determine if an enabled RT is participating in the transmitted broadcast message, a MODE CODE 2 (Transmit Last Status) or MODE CODE 18 (Transmit Last Command) must be transmitted on the 1553 bus. If the specified RT used in the MODE CODE is enabled for broadcast, the Broadcast Message Received (BRC) bit is set in the 1553 status response.

C.3.14 Shutdown Enable Registers (0x140D, 0x1410)

An RT bus shutdown will occur if the RT is enabled and the bit corresponding to this RT is set in the appropriate shutdown Enable register. These two words of BIU memory, at 0x140D (Figure 7-8) and 0x1410 (Figure 7-9), indicate the RTs to be shutdown on a specific bus.

To notify RTs 0, 5, 10, 15, 20, 25 and 30 to be shutdown on Bus B, the value of 0x8421 is loaded into BIU memory address 0x140D and 0x4210 is loaded into BIU memory address 0x1410. It is also necessary to set the corresponding Bus B down bit in each of the RT Control Words.

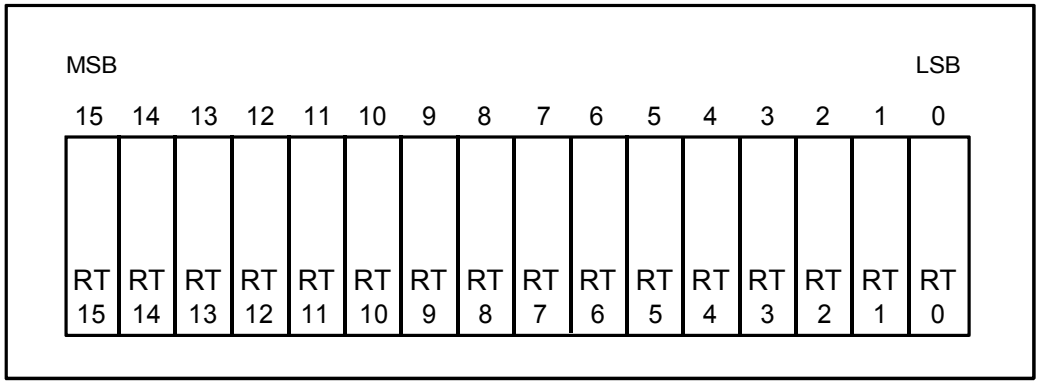


Figure C-8 RT 0-15 Shutdown Enable Register 0x140D

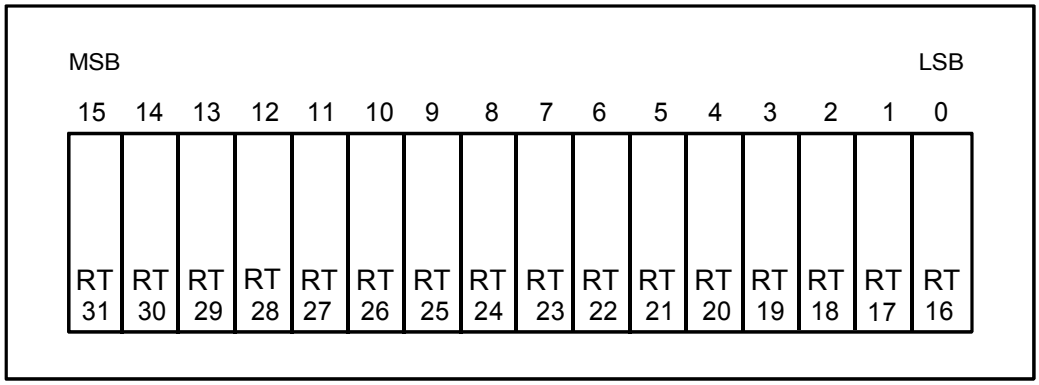


Figure C-9 RT 16-31 Shutdown Enable Register 0x1410

C.3.15 BC Trigger Status Register 0x1413

This register indicates if the BC Trigger is enabled.

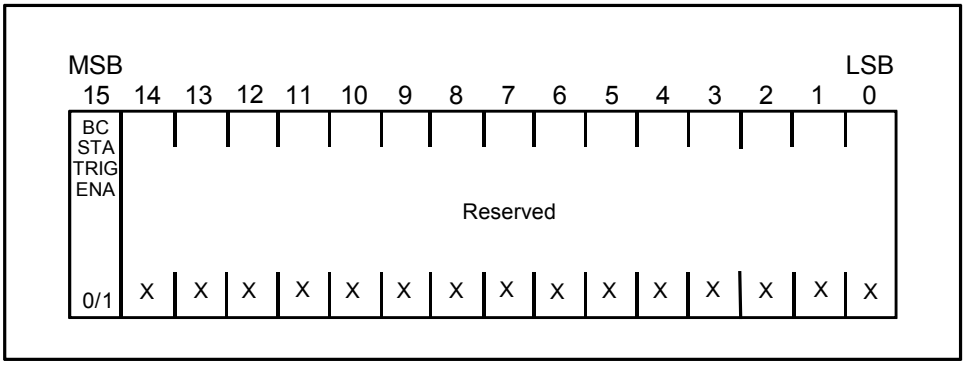


Figure C-10 BC Trigger Status Register 0x1413

Bits 15 Set to '1' if BC Trigger was enabled by writing to the BC Start Trigger Control Function Register (0x1F).
Set to '0' if BC Trigger is disabled.

Bits 14-0 Reserved

C.3.16 Threshold Register 0x1414

Reading this register provides the current variable input threshold setting. The default setting is the maximum value (0x00FF).



NOTE: The standard GLD-PC product does not support this feature. This feature requires different transceivers and must be ordered as an option.

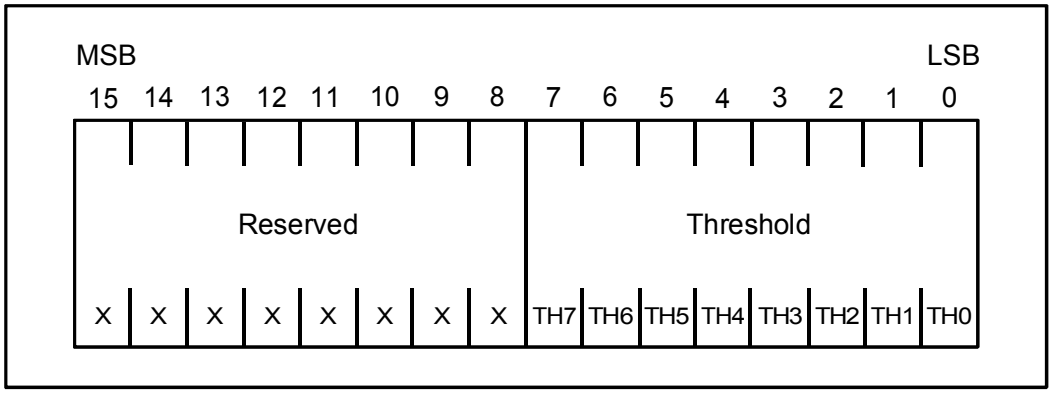


Figure C-11 Threshold Register 0x1414

Bits 15-8 Reserved

Bits 7-0 Threshold in hexadecimal

C.3.17 Amplitude State Register 0x1415

Reading this register provides the current variable amplitude setting. The default setting is the maximum value (0x00FF). This value is set when the microcode is uploaded.



NOTE: The standard GLD-PC product does not support this feature. This feature requires different transceivers and must be ordered as an option.

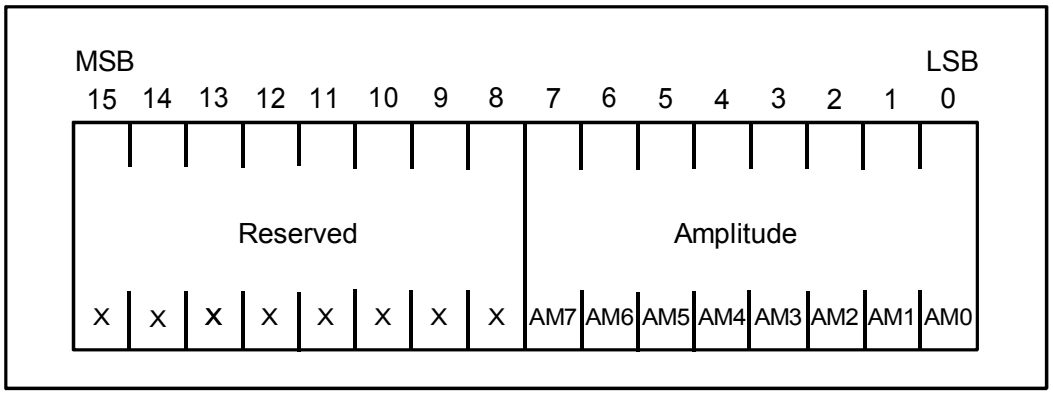


Figure C-12 Amplitude State Register 0x1415

Bits 15-8 Reserved

Bits 7-0 Amplitude in hexadecimal

C.3.18 Relay State Register 0x1416

This register contains the current value written to the Relay Function Register, which determines bus selection, external bus connection and termination options. The default setting is direct coupled and internal termination and connection (0x0007*)*.

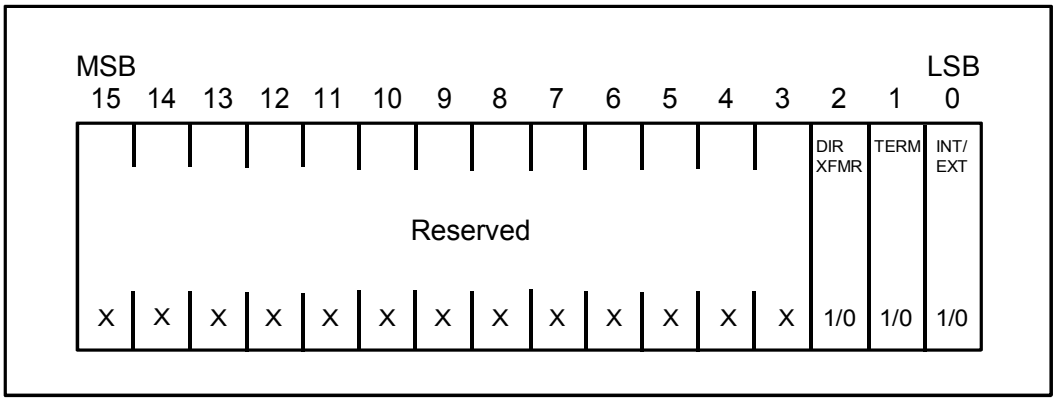


Figure C-13 Relay State Register 0x1416

Bits 15-3	Reserved
Bit 2	Direct/Transformer Coupling. Set to '1' for Direct Coupling Set to '0' for Transformer Coupling.
Bit 1	Termination Option. Set to '1' for Internal Termination Reset to '0' for External Termination.
Bit 0	Internal/External Bus Connection. Set to '1' for Internal Bus Connection Reset to '0' for External Bus Connection.



NOTE: Transformer coupling (Bit 2=0) and internal termination (Bit 1=1) is **not** recommended, since transformer coupling requires an external bus coupler box.

C.3.19 ELT State Register 0x1417

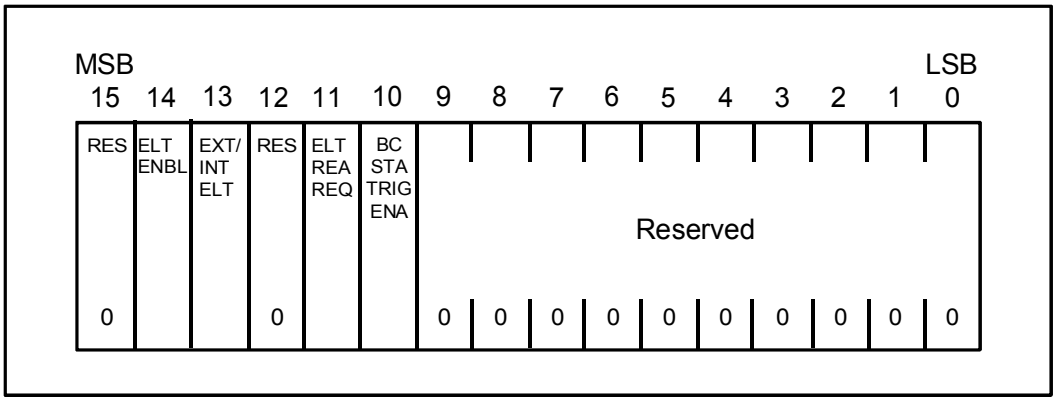


Figure C-14 ELT State Register 0x1417

Bit 15	Reserved
Bit 14	If '1', ELT is enabled. If '0', ELT is disabled.
Bit 13	If '1', external ELT is selected. If '0', internal ELT is selected.
Bit 12	If '0', reset the ELT. If '1', do not set the ELT.
Bit 11	If '1', ELT read has been requested. If '0', ELT read has not been requested.
Bit 10	BC Start Trigger Enable. If '1', BC Start Trigger input is enabled. If '0', option is disabled.
Bits 9-0	Reserved

C.3.20 Current Buslist Instruction Address Register 0x1418

A read of this register displays the current location of the Buslist instruction under execution.

C.3.21 BC Start Trigger Address Register 0x141A

This register holds the pointer for the first instruction when the BC Start Trigger is enabled. This value is written by software and read by microcode.



NOTE: This register should be written before enabling the BC Start Trigger option to avoid accidental starts.

C.4 Function Registers

The Function registers control certain board functions, such as buslist execution. Access to the Function Registers is controlled by Real-Time Control Registers 0x1403 through 0x1405. The GLD-PC firmware accesses these registers when no traffic exists on the bus.



NOTE: The Function Registers are not readable. All read accesses are performed via the Real-Time Control Registers located in memory starting at address 0x1400.

Table C-3 Function Registers

Register Number	Register Name	Access Method
10	BC Control	Write
11	MRT Control	Write
12	Fail-Safe Timer	Write
13	Gap Counter Control	Write
14	BC Error Control	Write
15	AND	Write
16	OR	Write
17	Elapsed Timer Control	Write
18	Chronological Monitor Control	Write
19	Amplitude	Write
1A	Relay	Write
1B	Threshold	Write
1C	Reset	Write
1D	Memory Address	Write
1E	Buslist Instruction Address	Write
1F	BC Start Trigger Control	Write

Follow the steps below to write to the Function Registers:

1. If the Master Control Register memory address 0x1403 contains the value 0x1553 and Bit 15 of the Register Control 0x1404 is set, wait for Bit 15 of the Register Control Register to be reset.
2. Write the value 0x1553 to the Master Control Register.
3. Write the value to be loaded into the desired Function Register into the Register Value Register 5 at memory address 0x1405.
4. Write the desired Function Register number into Bits 5-0 and set Bit 15 of the Register Control Register 4 at memory address 0x1404.
5. When Bit 15 of the Register Control Register 4 is reset by the onboard microcode, the operation has completed.

C.4.1 BC Control Register 0x10

The write–only BC Control Register controls three functions. These are:

START

Load the address of the first buslist instruction to be executed. The offset cannot be less than 0x1440*,* if the RTs are emulated.

HALT

To halt the buslist, write ‘0’. The BC completes the current instruction, halts and generates an asynchronous halt interrupt, and does not update the instruction counter.

CONTINUE

To continue the buslist, write 0xFFFF. The BC increments the instruction counter then starts the BC. The CONTINUE instruction can be used to restart the BC after asynchronous errors, exceptions or a HALT BC instruction. When it is evident that another buslist instruction will immediately follow the HALT instruction, the CONTINUE instruction restarts the BC.



NOTE: Writing to this register automatically resets and enables the BC elapsed timer. If using the external BC trigger, the timer is held reset until a trigger is received.

C.4.2 MRT Control Register 0x11

The write–only MRT Control Register enables or disables the emulation of RTs for the MRT structures set up in memory.



NOTE: Initial MRT structures must be in place before the MRT is started.

After the MRT is started, RTs can be enabled or disabled by setting or clearing Bit 15 of the RT Status Block Control Word for the desired RT.

START MRT

To start the MRT, write a non-zero value.

HALT MRT

To halt the MRT, write a ‘0’.

C.4.3 Fail-Safe Timer Register 0x12

In the event of a runaway transmitter (continuously transmitting greater than 720 µs) the GLD-PC will activate a fail-safe timer to disable the transmit circuitry and queue an interrupt to indicate the event. This write–only Fail-Safe Timer register resets the Fail-Safe Timer and enables both transmitters.

During simulation any write to the Fail-Safe Timer register will reset the timer and re-enable both transmitters. Also, a hardware or software reset to the card will have the same effect.

When a Transmitter Shutdown Interrupt occurs (that is, Bit 5 of the Trailer Word in the Interrupt Packet is set), the Fail-Safe Timer register can be written to re-enable transmitters.



NOTE: A word count high error greater than 32 words indicates a transmitter hardware failure. If the transmitter is not emulated on this channel, then register 12 should not be written for resetting. Register 12 should not be written to.

C.4.4 Gap Counter Control Register 0x13

This register enables the BC to accept different response times other than the 1553 spec allows.

To use the Gap Counter Control register:

- Determine the length of time the BC allows for the RT to respond. Calculated as tenths of microseconds. (14 µs = 140 tenths µs)
- Subtract this value from 256.
- Convert to hexadecimal.
- Load the new value into the Gap Counter Control Register.

EXAMPLE

To set the BC time-out to 18 microseconds, multiply 18 by 10 (to convert 18 to tenths of microseconds) and subtract the result from 256:

256 - 180 = 76 *Decimal*

Convert to Hexadecimal:

76 *Decimal* = 0x4C

Write this value (0x4C) into the Gap Counter Control register.



NOTE: Since the time-out value is subtracted from 256, the maximum time-out is 25.6 microseconds.

C.4.5 BC Error Control Register 0x14

The write–only BC Error Control Register modifies BC reaction to 1553 errors. The BC may be set up to halt or interrupt for both status exception and protocol error events. (Figure C-15). Bit 2 is used to activate error injection for the BC mode. The defined error word (word 2 of instruction) in any buslist instruction is used on transmission.

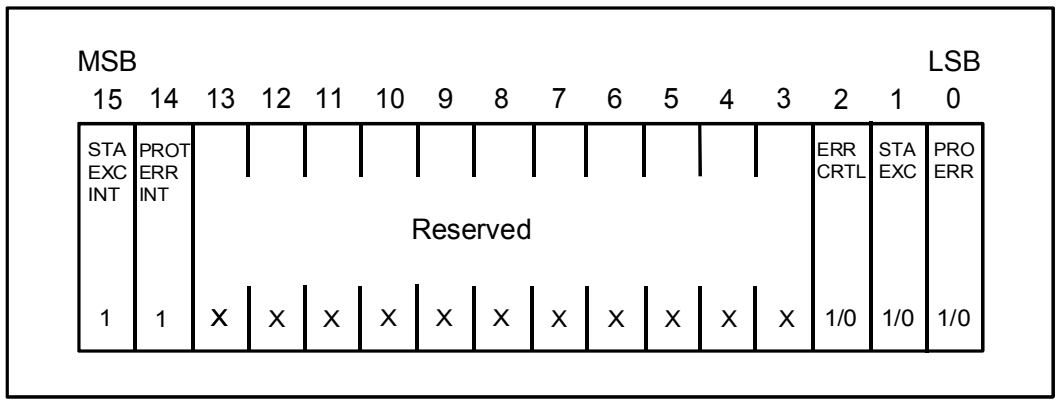


Figure C-15 BC Error Control Register 0x14

Bit 15 Status Exception Interrupt (STA EXC INT)

Set to ‘1’ to post an interrupt when the BC encounters a Status Exception.

Bit 14 Protocol Error Interrupt (PRO ERR INT)

Set to ‘1’ to post an interrupt when the BC encounters a protocol error.

Bits 13-3 Reserved

Bit 2 Error Control (ERR CRTL)

Set to ‘1’ to use the error-injection information in each individual buslist instructions on transmission.
Set to ‘0’ to disable all BC error-injection capabilities.

Bit 1 Status Exception (STA EXC)

Set to ‘1’ to continue the BC after a status exception is encountered.
Reset to ‘0’ to halt the BC after a status exception is encountered.

Bit 0 Protocol Error (PRO ERR)

Set to ‘1’ to continue the BC after a protocol error.
Reset to ‘0’ to halt the BC after a protocol error occurs.

C.4.6 AND Register 0x15

The write–only register 0x15 works together with the Memory Address register 0x1D to AND the value in register 0x15 with the value pointed to by the memory address contained in Register 0x1D . The GLD-PC modifies the Memory content after the AND value is written to this register.

EXAMPLE

Masking out the upper byte of a value using the AND register 0x15, AAAA ANDed with 00FF results in 00AA.

Operation	Address	Data
Write a value of 0xAAAA into address 0x0528.	Memory 0x0528	0xAAAA
Write 0x0528 into Memory Address Register 0x1D.	Memory Address Register 0x1D	0x0528
Write 0x00FF to the AND Register 0x15.	AND Register 0x15	0x00FF
Read back new data value.	Memory 0x0528	0x00AA



NOTE: The AND/OR registers provide compatibility with previous BIU products and are not used in most cases, since memory access via these registers takes five to ten times longer than a direct access to memory.

C.4.7 OR Register 0x16

The OR register works together with the Memory Address register 0x1D to OR the value in register 0x16 with the value pointed to by the memory address contained in Register 0x1D . Memory content is modified after the OR value is written to this register.

EXAMPLE

To set the upper byte of the value using the register 0x16, 0x00AA OR'ed with 5555 results in 0x55FF.

Operation	Address	Data
Write a value of 0x00AA to Memory Location 0x1359.	Memory 0x1359	0x00AA
Write 1359 to Memory Address Register 0x1D.	Memory Address Register 0x1D	0x1359
Write 5555 to OR Register 0x16.	OR Register 0x1	0x5555
Read back new data value.	Memory 0x135	0x55FF



NOTE: The AND/OR Registers provide compatibility with previous BIU products and are not used in most cases, since memory access via these registers takes five to ten times longer than a direct access to memory.

C.4.8 Elapsed Timer (ELT) Control Register 0x17

The write–only ELT Control register controls the 32-bit Elapsed Timer for MRT and CM modes (Figure C-16, Table C-4). A write to register 0x17 enables/disables the ELT, selects the external signal or internal clock source, resets the ELT and reads the ELT. (See the Real-Time Control registers 0x140A and 0x140B.) The ELT contains a resolution of one microsecond. The ELTCLK resolution is user-defined.



NOTE: Be sure to read the Real time control ELT STATE register to verify configuration before changing.

Table C-4 Register 0x17 Values and Actions

WRITE Value	Action
0x0	HALT and reset the ELT
0x1000	HALT the ELT
0x1800	HALT and read the ELT
0x2000	Enable the external clock input and reset the ELT
0x4000	Enable and reset the ELT
0x5000	Enable the ELT
0x5800	Read the ELT without HALT.

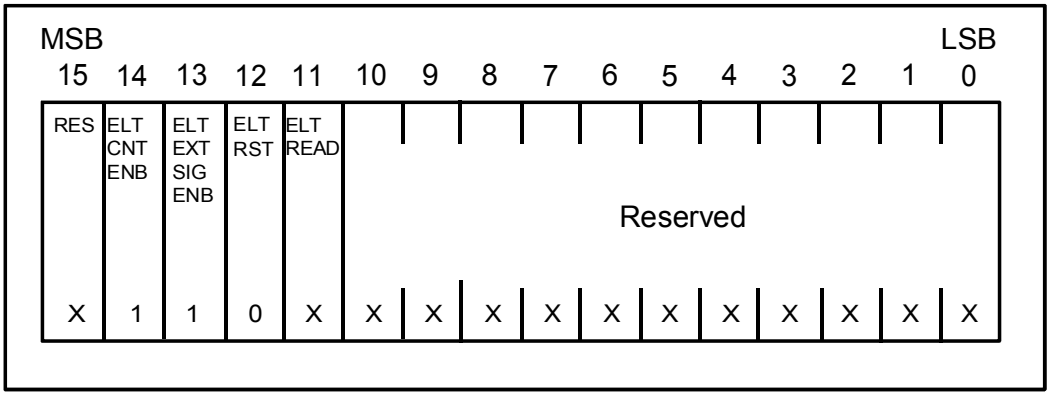


Figure C-16 Elapsed Timer (ELT) Control Register 0x17

Bit 15 Reserved

Bit 14 Elapsed Timer Count Enable (ELT CNT ENB)

Set to '1' to resume count of Elapsed timer from the current value. Reset to '0' to halt the Elapsed timer.

Bit 13 ELT External Signal Enable (ELT EXT SIG ENB)

Setting Bit 13 enables the external signal for the Elapsed Timer Clock. Clearing Bit 13 selects the internal 1 MHz clock.



NOTE: The external clock may not exceed 1 MHz, as unpredictable timing will occur.

Bit 12 Reset Elapsed Timer (RST ELT)

Set to '0' to clear the Elapsed Timer.
Set to '1' if writing to this register and no reset of the ELT is desired.

Bit 11 ELT Write Control (ELT READ)

Set to '1' to load the ELT LOWD and ELT HIWD Real-Time Control Registers with the current ELT value.

Bits 10-0 Reserved

C.4.9 Chronological Monitor Control Register 0x18

The Chronological Monitor Control Register starts and stops the monitor. Writing a value of '8' to this register starts the monitor.



NOTE: Before the monitor can be started, the address of the first monitor buffer must be loaded into the Real-Time Register at 0x1408.

Writing a value of '0' to this register stops the monitor. Writing a value of '0x18' allows the monitor to record 1553 command words that may contain protocol errors and permits the capture of all bus traffic. If Bit 4 is not set, only messages with valid commands can be monitored.

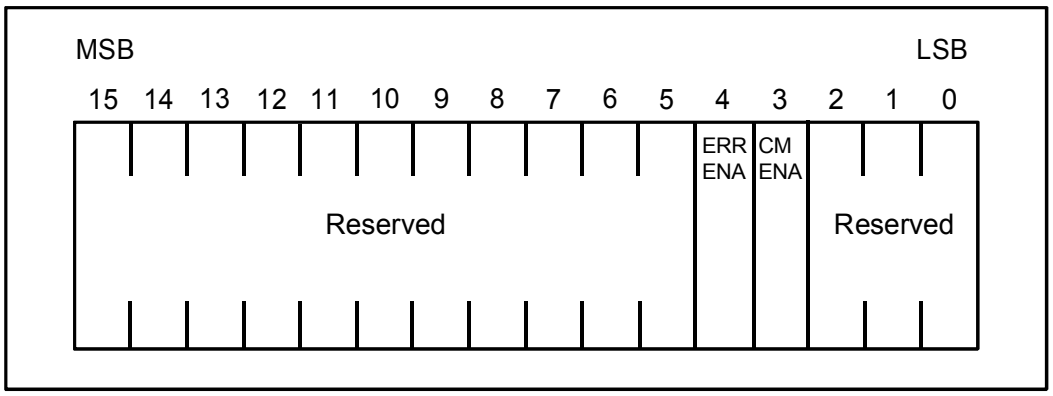


Figure C-17 Chronological Monitor Control Register 0x18

Bits 15-6 Reserved

Bit 5 External Chronological Monitor Start Trigger Enable
This bit is used to enable and disable the external RS-422 CM Start Trigger option. All other CM mode data structures must be set up properly before using this feature.

Bit 4 Error Enable.

Set to '1' to monitor all traffic.
Reset to '0' to monitor only messages with valid command words.

Bit 3 CM Start.

When set to '1' the CM will start recording data in the buffer pointed to by the Real-Time Control Register 0-0x8.

Bits 2-0 Reserved

C.4.10 Amplitude Register 0x19

NOTE: The standard GLD-PC product does not support this feature.

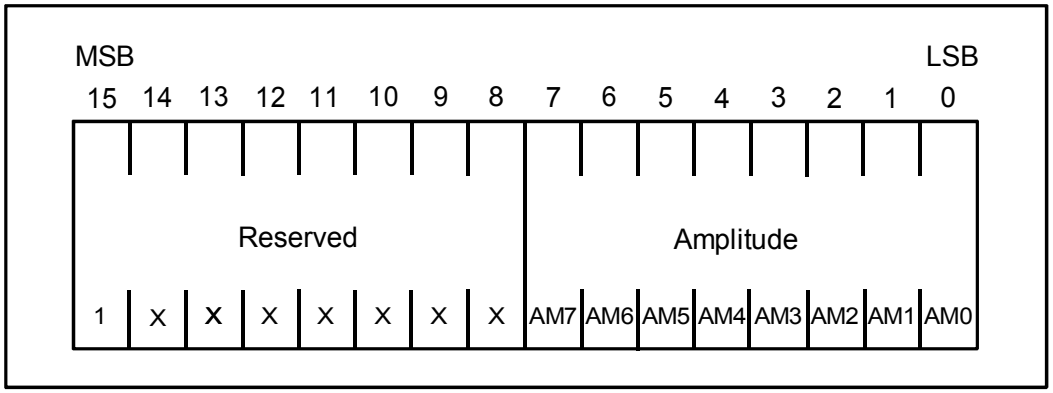


Figure C-18 Amplitude Register 0x19

Bits 15-8 Reserved

Bits 7-0 Output Amplitude
Vary the waveform amplitude by writing an eight-bit hexadecimal value (0-FF) to Register 0x19. Set to 0xFF by configuration data at power-up.

NOTE: Bus voltage has two possible setting ranges, depending upon the type of bus coupling chosen. Uploading the microcode to the board during the Getting Started procedure sets the defaults to direct coupled and maximum voltage, which is 10 V. The range for direct coupling is 0-10 V peak-to-peak. The range for transformer coupling is 0-30 V peak-to-peak. The value in the Amplitude Register is a percentage of maximum output level. To get a voltage correlation, measurements must be made at the 1553 stub connection with external instrumentation. Actual bus voltages will vary depending on such factors as bus loading, cable lengths, etc.

C.4.11 Relay Register 0x1A

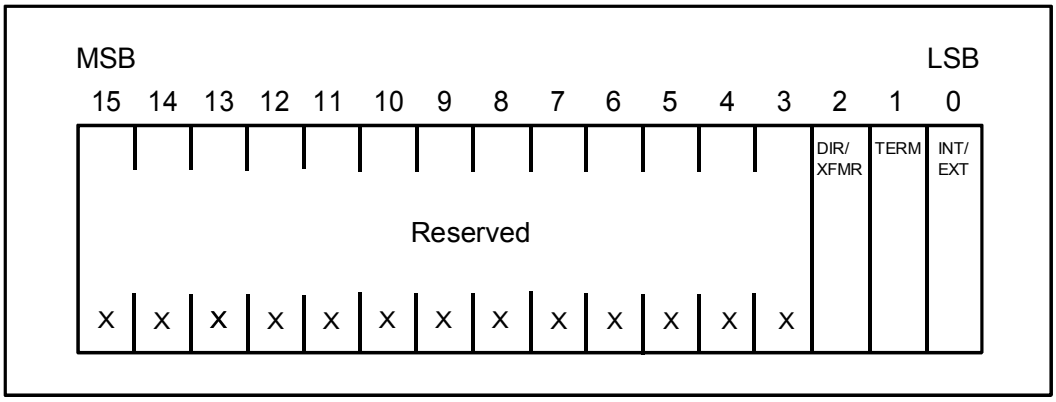


Figure C-19 Relay Register 0x1A

Bits 15-3 Reserved

Bit 2 Direct/Transformer Coupling.
Set to '0' for transformer coupling.

Bit 1 Termination Option.
Set to '0' for external termination.
Set to '1' for internal termination.

Bit 0 External Bus Connection
Set to '0' for external 1553 bus connection.
Set to '1' for internal 1553 bus connection.

The internal connection is used during self-test and by software while configuring the channel to avoid unwanted 1553 effects during setup.

To connect to the 1553 bus, select a value from the following table:

Table C-5 Relay Settings

Coupling	Termination	1553 Bus	Value
Direct	Internal	Connected	0x0006
Direct	Internal	Disconnected	0x0007 (default, set when microcode is uploaded to the channel)
Direct	External	Connected	0x0004
Direct	External	Disconnected	0x0005
Transformer	Internal	Connected	Do not use, need an external transformer bus coupler.
Transformer	Internal	Disconnected	Do not use
Transformer	External	Connected	0x0000
Transformer	External	Disconnected	0x0001

The default value is 0x0007, which means the board is not connected to the 1553 bus.

C.4.12 Threshold Register 0x1B

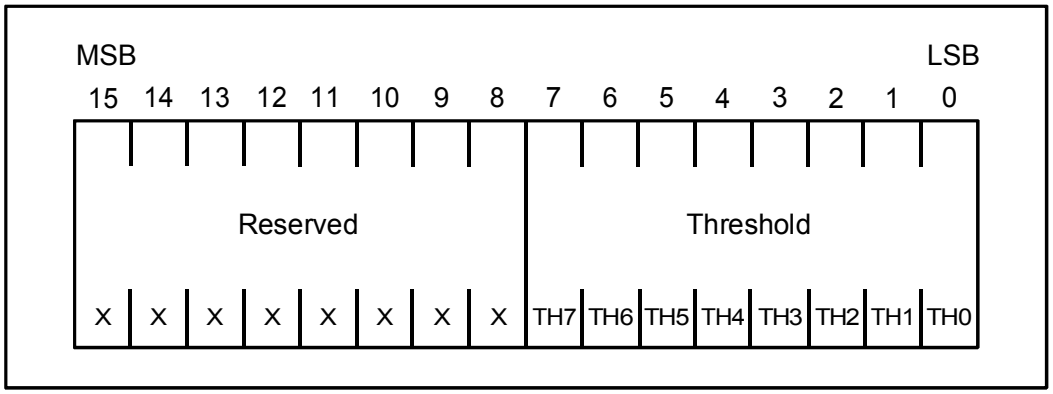


Figure C-20 Threshold Register 0x1B

Bits 15-8 Reserved

Bits 7-0 Threshold
Vary the input threshold voltage by writing an eight-bit hexadecimal value (0-FF) to register 1B. Set to 0xFF by configuration data at power-up. A value of '0' sets the threshold at 0 volts; a value of 0xFF sets the threshold at approximately 3 volts.



NOTE: Accessing this register affects only those boards supporting this feature. The value is only a percentage of the 3-volt maximum threshold. Testing for voltage correlation depends on traffic, loading of 1553 bus and location of connection to traffic sources. Therefore, absolute values must be measured at the 1553 stub with external instrumentation.

C.4.13 Reset Register 0x1C

The Reset Register resets the GLD-PC, affecting only register data structures set up in the processor. All memory structures are left alone.

Resetting the GLD-PC:

- Halts BC, RT and CM operations
- Resets BC Error Control Register bits to their default values:
  - Stop on Protocol Error
  - Stop on Status Exception
  - Do not interrupt on Protocol Error
  - Do not interrupt on Status Exception
  - Disable BC error injection
- Resets the Terminal Fail-Safe Timer
- Ignores the remainder of a message in progress on the 1553 data bus
- Turns off any pending interrupts
- Resets the interrupt queue to 0x120

To perform a RESET, write any hexadecimal value (0-FFFF).

C.4.14 Memory Address Register 0x1D

Use register 0x1D to address memory and, in conjunction with the AND or the OR register, to set or reset bits. The Memory Address register contains the value of the address to be modified. Perform a write to register 0x1D before performing the appropriate "AND" or "OR" function. For examples of usage, see the definitions for Function registers 0x15 (AND) and 0x16 (OR).

C.4.15 Buslist Instruction Address Register 0x1E

Any write to this register will cause the currently executing buslist instruction pointer to be written to the Real-Time Control Buslist Instruction register (at memory location 0x1418*)*.

C.4.16 External BC Start Trigger Control Register 0x1F

This register enables and disables the BC Start Trigger option. The bus controller's buslist start address must also be written to the BC Start Trigger Address Register (0x141A*)*.

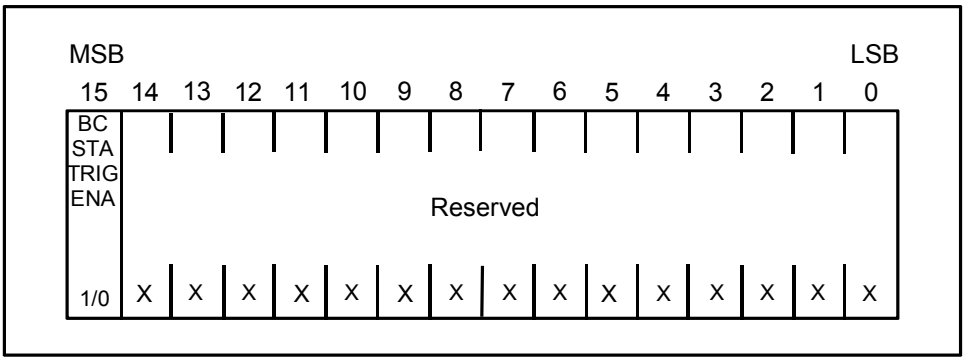


Figure C-21 External BC Start Trigger Control Register

Bit 15 BC Start Trigger Enable (BC STA TRIG ENA)
If set to '1', the start trigger option is enabled
If set to '0', the start trigger option is disabled

Bits 14-0 Reserved

GLOSSARY

BC	Bus Controller; provides the capability of defining, storing, and executing comprehensive lists of bus instructions.
BC Start Trigger	An external RS-422 pulse used to control the execution of the buslist.
BC-delay timer	Used to control timing of buslist major and minor frames.
BIU	Bus Interface Unit (see channel).
buslist	A sequence of commands to be executed by the BC mode. Multiple buslists may be constructed and called up by the host in real-time.
channel	A single 1553 data-bus interface board; contains 64 K of dual-port RAM and may be mapped to one area of memory or two different areas of memory.
CM	Chronological Monitor; captures all or selected bus traffic.
direct coupling	A 1553 bus connection using a T-connector when the distance between the board and the 1553 bus measures 12 inches or less.
DOS	Discrete Output Signal; a signal transmitted out the RS-422 port, which may be used to signal the start of a buslist instruction. The signal is active for two microseconds before the command is placed on the bus.
dual channel	Dual-channel configuration provides all of the functionality of two single 1553 data-bus interface boards and twice the amount of on-board dual-port RAM. Each channel is fully independent sharing only the host-bus-buffering chips.
EC	European Community.
elapsed timer	An on-board, 32-bit timer with one-microsecond resolution.
ELT	Chronological-Monitor Elapsed Timer
fail-safe timer	A timer that allows an interrupt to be generated after 720 μs of continuous bus transmission.
FCC	Federal Communication Commission.
header word	A section of the monitor buffer containing the control and status bits and buffer-block count.
MRT	Multiple Remote Terminal; able to receive, store and count bus messages.
RAM	Random Access Memory.
snapshot interrupt	An interrupt packet placed on the interrupt queue containing the memory address within the monitor buffer of the first command word in the message. Snapshot interrupts can also be generated for any particular mode code.
sublist	A set of buslist instructions subordinate to the primary buslist.
transformer coupling	A 1553 bus connection using a transformer coupler when the distance between the board and the 1553 bus measures exceeds 12 inches but not 20 feet.
variable amplitude	Permits varying the amplitude of the 1553 waveform to test RT and BC error detection capabilities.

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