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GLD-PC/S

User Manual

Document No. T-T-MU-GLXXAS##-A-0-A2

FOREWORD

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Systran Corporation
4126 Linden Avenue
Dayton, OH 45432-3068 USA
(937) 252-5601
Fax: (937) 258-2729

FCC

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CE

Please note: As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

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1. 0 INTRODUCTION

1.1 Overview

The GLD-PC/S provides a powerful and convenient, interface between a host computer and a MIL-STD-1553 data bus. The GLD-PC/S enables the host to operate in real-time as a single mode, MIL-STD-1553A or B protocol Bus Controller (BC), Multiple Remote Terminal (MRT) or Chronological Monitor (CM). The GLD-PC/S provides the host with complete access to data received or transmitted on the bus and the ability to detect bus errors.

The GLD-PC/S utilize a high-speed controller in conjunction with Dual-Port Random Access Memory (RAM) to provide a complete, intelligent 1553 emulation system. Using on-board data structures located in the Dual-Port RAM, the board is capable of sustaining operation on the bus without host intervention. In addition, the CM stores commands, status responses, gap times and time tags within the same buffer.



NOTE: The single-function GLD-PC/S does not support error injection and cannot operate simultaneously as a bus controller, multiple remote terminal, and/or monitor.

1.2 Modes of Operation

The GLD-PC/S is capable of operating in BC or MRT or CM modes. All MIL-STD-1553A or B protocol communication between emulated devices occurs over the 1553 bus, rather than through a local bus. The three operating modes provide extensive bus protocol error detection, such as parity error and no response.

1.2.1 Multiple Remote Terminal Mode

Using 32K-words of Dual-Port RAM, the GLD-PC/S is able to receive, store and count approximately 750 bus messages of 32 data words each. Bus messages are transmitted and received without host intervention. The RT is also capable of generating an interrupt when a message buffer transmits or receives data and enabling specific subaddresses and mode codes. RT's can be programmed individually for 1553A or B protocol.

1.2.2 Bus Controller Mode

The BC provides the capability of defining, storing and executing comprehensive lists of bus instructions. The GLD-PC/S efficiently addresses up to 32 RTs (31 RTs and one Broadcast RT, RT 31 in 1553B mode). The BC can generate and process any valid type of MIL-STD-1553A or B protocol message:

- BC-to-RT Transfer
- RT-to-BC Transfer
- RT-to-RT Transfer
- Mode Command Without Data Word
- Mode Command With Data Word (Transmit)

- Mode Command With Data Word (Receive)
- Broadcast commands (1553B mode only)

1.2.3 Chronological Monitor Mode

The CM captures all or selected 1553A or B bus traffic. Data transfers may be filtered down to the subaddress level. Mode commands can be selectively monitored down to individual mode codes.

1.3 Discrete Output Signal

The GLD-PC/S is equipped with an RS422 port. This port provides a Discrete Output Signal (DOS) with a duration of two microseconds, which may be programmed for any buslist instruction. The Discrete Output Signal is sent out as the buslist instruction is fetched and decoded. The port also allows for an external elapsed timer (ELT) signal reset.

1.4 Memory

1.4.1 Onboard Dual-Port RAM

The GLD-PC/S Dual-Port RAM allows host access to share data and structures without 1553 process interference. Application programs can use the Dual-Port RAM for variables and data structures residing in the host's main memory. Storing all data in the Dual-Port RAM eliminates the need for continuous host bus support of MIL-STD-1553 activity.

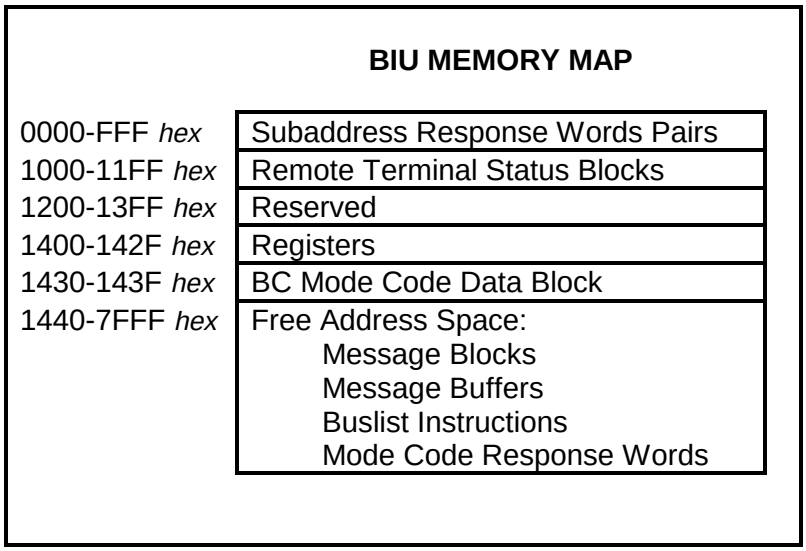


Figure 1-2 GLD-PC/S Memory Map

The Dual-Port RAM contains the area required for data structure storage. The RAM is broken down into many different areas, including areas for RT configuration, subaddress configuration, MIL-STD-1553A or B protocol data transmitting and receiving buffers and CM buffers.

1.5 Interrupt Handling

An interrupt notifies the host that a specific condition (such as a Message buffer access, a BC instruction execution, or a 1553 error) has occurred.

Because of interrupt latency and host processing speed, multiple interrupts may be generated while the host is processing an interrupt. To preserve the integrity of all enabled events, the GLD-PC/S continuously buffers interrupt events from within the Interrupt Queue. The interrupt queue can hold up to 36 interrupt packets.

1.6 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct questions not satisfactorily answered by this document, or concerns about the functional-fit of this product for your particular application, or programming questions, to the factory at **(937) 252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance. Our goal is to help solve your problem.

1.7 Ordering Process

To learn more about SYSTRAN products or to place an order, the following contacts are available:

- Phone: **(937) 252-5601**
- E-mail address: **info@systran.com**
- World Wide Web address: **http://www.systran.com**

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2. 0 GETTING STARTED

2.1 Unpack and Inspect the Board



NOTE: The hardware board is shipped in a protective anti-static bag. Do not remove the board from the anti-static package until properly grounded or damage to the board may occur.

Remove the board from the packing box and the protective bag. Place the hardware board on top of the protective bag or on an electrostatically-controlled work surface. If the board appears to be damaged, contact SYSTRAN immediately at: **(937) 252-5601** or send an e-mail message to **support@systran.com** for additional assistance.

It is suggested the packing materials be retained for future.

2.2 Set the Hardware Switches

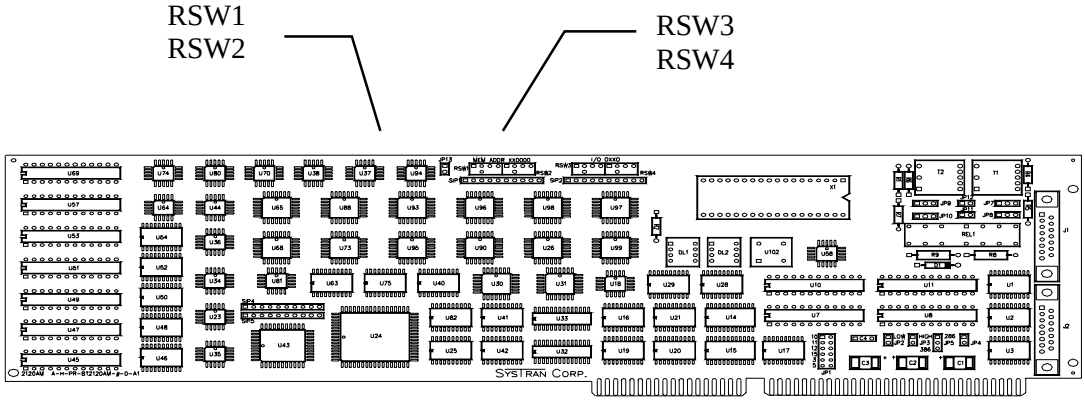


Figure 2-1 GLD-PC/S Board



NOTE: The hardware switches must be set before placing the GLD-PC/S in the host.

Four switch banks, located near the upper middle of the GLD-PC/S, set the memory and I/O addresses. Rotary Switch Banks 1 (RSW1) and 2 (RSW2) set the memory address space, while Rotary Switch Banks 3 (RSW3) and 4 (RSW4) set the I/O address space.



NOTE: Throughout this manual, figures and registers are labeled with MSB and LSB, denoting most significant and least significant bits.

2.2.1 Input/Output Addressing

The I/O address switch banks are factory set at 0100 *hex*. (See Figure 2-2.) The first and last bytes are fixed at '0'. The I/O address ranges from 0000 *hex* through 07C0 *hex* bytes.

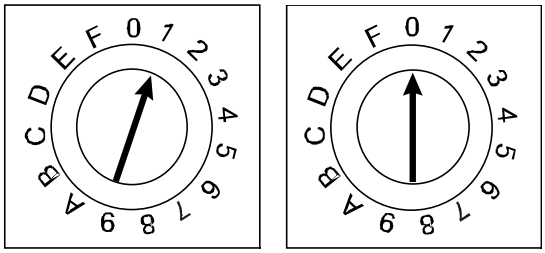


Figure 2-2 I/O Address Rotary Switches 3 and 4 (Factory Set)

0	1	0	0



NOTE: SYSTRAN recommends that the rotary switches be set to 0100 *hex*, 0200 *hex*, or 0300 *hex* for I/O host-to-GLD-PC/S addressing. Space 0100-03FF has been reserved by the PC-AT for add-on card I/O addressing.

2.2.2 Memory Address

The memory address switch banks are factory set at 0D *hex*. (See Figure 2-3.)

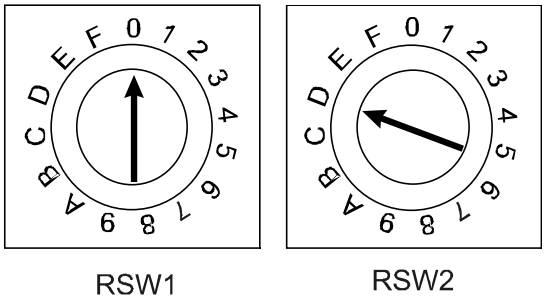


Figure 2-3 Memory Address Rotary Switches 1 and 2

0	D

2.2.3 Interrupt Level

There are six jumper positions (IRQ3, IRQ5, I4Q10, IRQ11, IRQ12, IRQ15) used to select the preferred interrupt level. (Figure 2-4.)

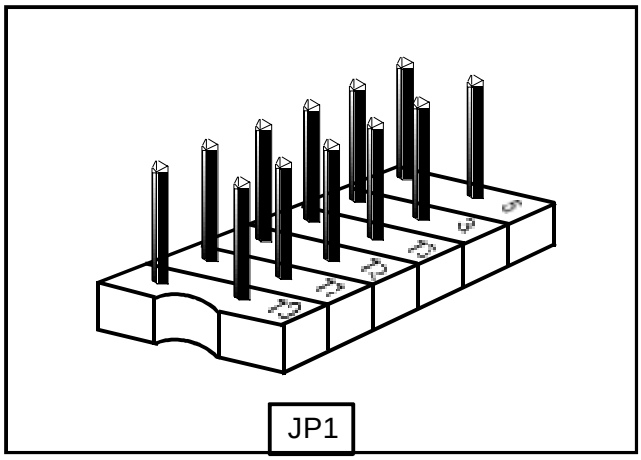


Figure 2-4 Interrupt Level Settings

EXAMPLE

To operate at IRQ3 (interrupt Level 3), install the jumper cap on the prongs next to IRQ3.(See Figure 2-5.)

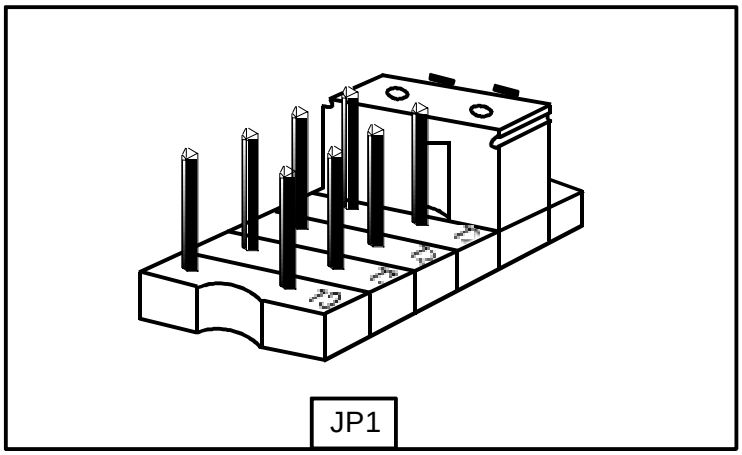


Figure 2-5 Interrupt Level 3

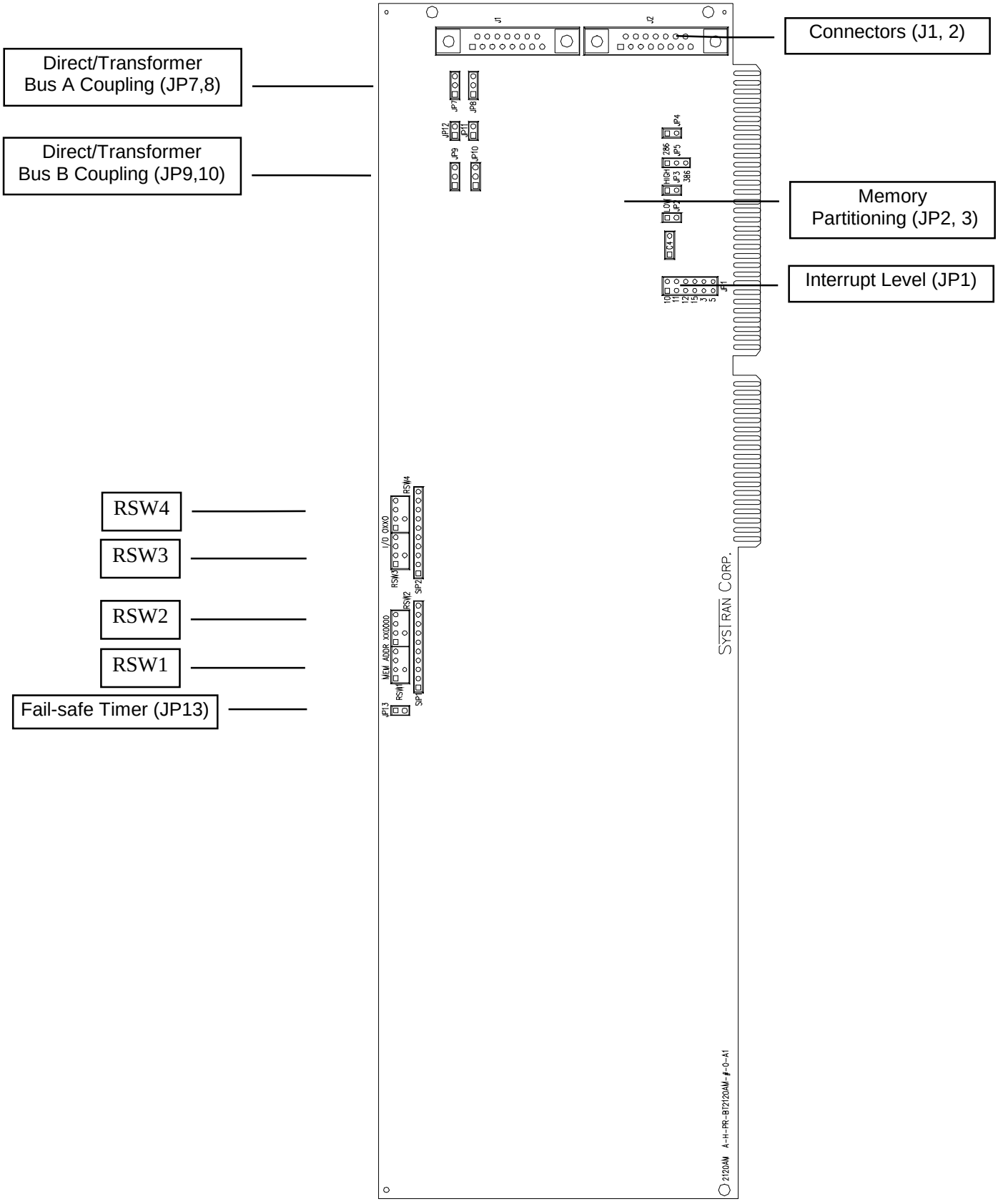


Figure 2-6 GLD-PC/S Board

2.3 Locate Connectors

The GLD-PC/S has two fifteen-pin connectors (J1 and J2). With the board placed horizontally, with the PC Connectors facing toward you, all 1553 connectors are located on the right end of the board. The pins are in numerical order, from left to right, and contain the following functions. (See Table 2-1.)

Table 2-1 The J1 and J2 Connectors

J1 Signal	Pin Number	J2 Signal
Bus A	1	Discrete Output +
Bus A*	2	Discrete Output -
Reserved	3	Reserved
Reserved	4	Reserved
Reserved	5	Reserved
Bus B	6	Reserved
Bus B*	7	Reserved
Chassis Ground	8	Chassis Ground
Reserved	9	External Clock +
Reserved	10	External Clock -
Reserved	11	Reserved
Reserved	12	Reserved
Reserved	13	Reserved
Reserved	14	External Reset +
Reserved	15	External Reset -

2.4 Locate The Jumpers

There are twelve jumpers located on the bus interface board. These jumpers functions are described in Table 2-2.

Table 2-2 Jumper Functions

Jumper	Function
JP1	Interrupt Level
JP2, JP3	Memory Partitioning
JP4	Reserved
JP5	Reserved
JP7, JP8	Direct/Transformer Bus A Coupling
JP9, JP10	Direct/Transformer Bus B Coupling
JP11,JP12	Waveform Jumpers (Always installed)
JP13	Fail-safe Timer

2.4.1 Partition The Memory

The memory on the GLD-PC/S is divided into two 16 K-word partitions which can be individually enabled or dissolved. Two jumpers (JP2 and JP3), located at the lower right corner of the board, control the memory partition. If the jumper is ON, the partition is enabled. To indicated which half of the memory address is controlled, each partition is labeled with HIGH or LOW (See Figure 2-7.) Enable both partitions to select the full 32 K words of memory.

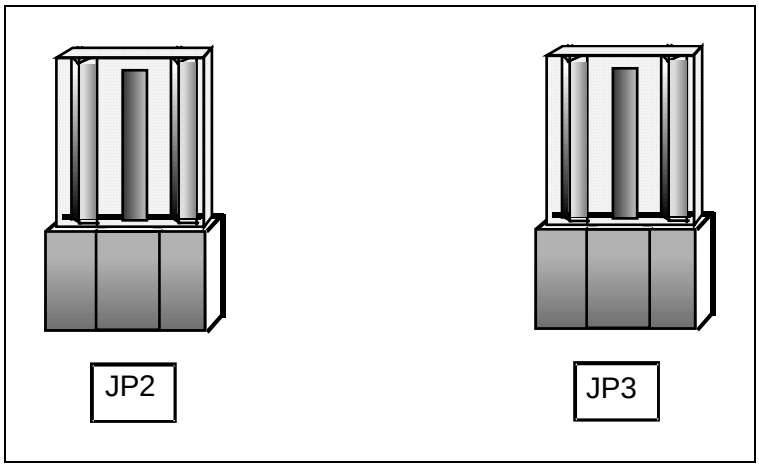


Figure 2-7 Memory Partition with Memory Address on 32 K Words (Default)

2.4.2 Direct or Transformer Coupling

The JP7-JP10 Jumpers, located on the upper right corner of the controller board, determine direct or transformer coupling. (See Table 2-2.)

Table 2-3 Direct/Transformer Jumpers

Jumpers	Jumper Position	Pins	Type of Coupling
JP7, JP8	ON	Pins 1,2	Direct (Bus A)
JP7,JP8	ON	Pins 2,3	Transformer (Bus A)
JP9, JP10	ON	Pins 1,2	Direct (Bus B)
JP9, JP10	ON	Pins 2,3	Transformer (Bus B)

2.4.3 Waveform Jumpers

Jumpers JP11 and JP12 are located above Jumpers JP7-JP10, on the upper right corner of the GLD-PC/S. They select transformer center tap grounding and should always be installed.

2.4.4 Fail-safe Timer

The JP13 jumper, located in the upper left corner of the board, controls the fail-safe timer. If the jumper for JP13 is ON, the timer is disabled.

2.5 Install Board In The Host



CAUTION: Ensure power is off before installing the board.

1. Identify the location of the 16-bit slot in the PC-AT where the board will be installed. Remove the cover and open the back of the system.
2. Wearing an anti-static wrist strap, position the board over an available slot in the host.
3. Push down firmly on the board until it locks into place.
4. Secure the front panel with a single screw.

Apply power to the board by turning on the system.

2.6 Select Direct or Transformer Coupling

The GLD-PC/S can be connected to the MIL-STD-1553 bus via a Direct or Transformer connection.

- Direct Coupling can be used if the distance between the GLD-PC/S and the MIL-STD-1553 bus is 12 inches or less.
- Transformer Coupling can be used between the GLD-PC/S and the MIL-STD-1553 bus for any distance up to 20 feet.

An external Coupling Box is required if Transformer coupling is selected. In any case, it is important that the bus be a valid, properly terminated configuration.

To change the type of coupling, change the coupling jumper configuration.

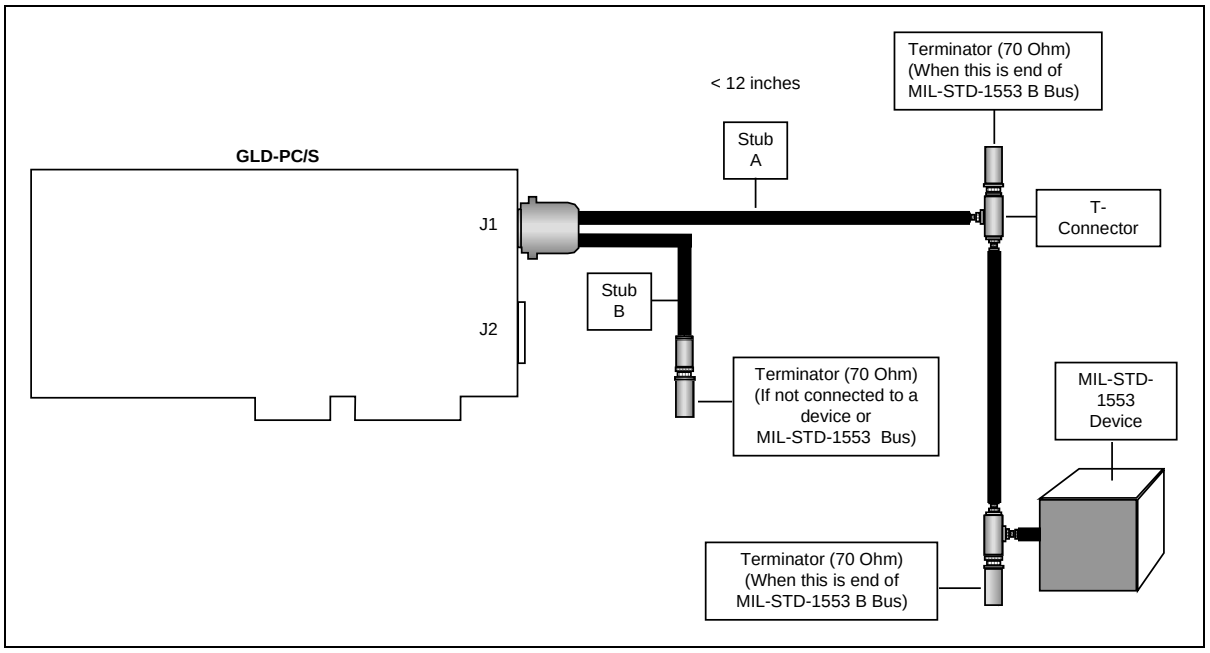


Figure 2-8 Direct Coupled MIL-STD-1553A or B Protocol Bus

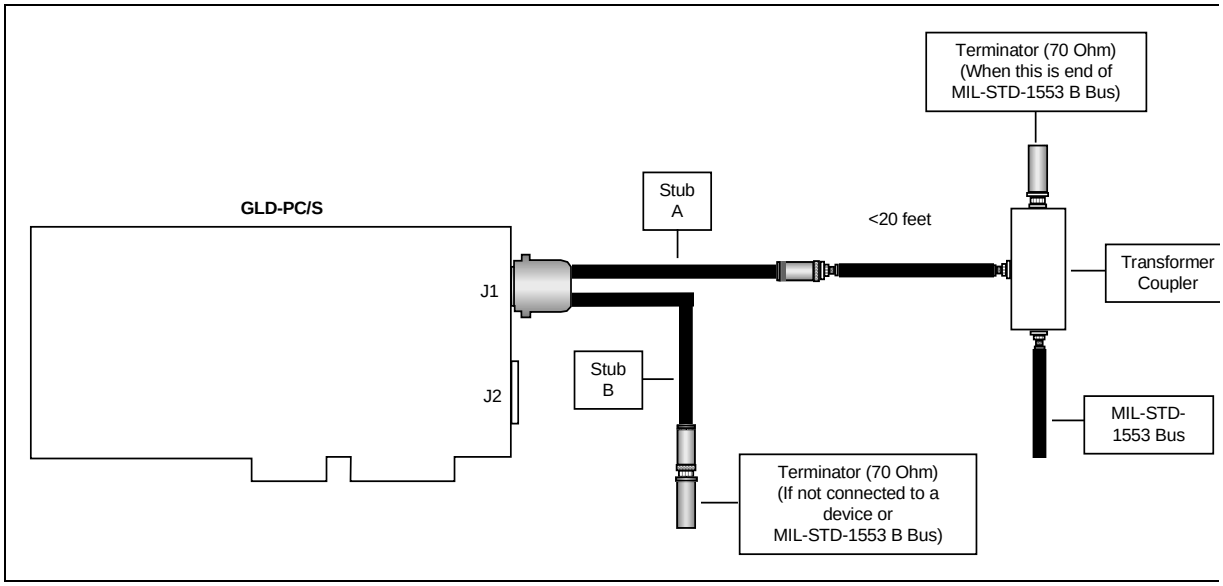


Figure 2-9 Transformer Coupled MIL-STD-1553A or B Protocol Bus

2.7 Powering On The System

After the board and the MIL-STD-1553 connection are properly installed, switch on the system. Use the diagnostics software to complete the hardware tests. See the GLD-PC/S Hardware Confidence Test manual for more information.

2.8 Software Installation, Configuration and Operation

Refer to the *GLD-PC/S Interface Library* and the *GLD-PC/S Hardware Confidence Test (HCT)* manual to perform the following procedures:

- Install software
- Upload the microcode
- Initialize the channel
- Program 1553 functions
- Run the channel

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3. 0 BUS CONTROLLER MODE

3.1 Overview

The GLD-PC/S can be programmed to operate in the BC mode to emulate all message types defined by MIL-STD-1553A or B. Any series of commands, either valid or invalid, can be sequenced as needed. A sequence of commands that the BC mode executes is called a buslist. Multiple buslists may be constructed and called up by the host in real-time.

The BC mode operates by executing a series of buslist instructions contained in the Dual-Port RAM. The instructions include those allowing generation of all MIL-STD-1553 message types, as well as NO-OP, HALT and JUMP instructions for framing of messages. The BC mode cannot operate simultaneously with the MRT or CM modes.

3.2 BC Features

3.2.1 Timers

The GLD-PC/S has an Elapsed Timer (ELT) that is used to schedule buslist instructions and control frame timing.

If the Discrete Out Signal Bit and the ELT Reset Bit are both set for a buslist instruction, the GLD-PC/S generates the Discrete Out Signal prior to the ELT Reset.

3.2.2 Interrupts

In BC mode, hardware interrupts may be posted to the host when certain event interrupts occur. (See the Interrupt section for details.) All interrupts may be selectively enabled or disabled under control of the applications software, except for a BC HALT. HALT interrupts are always enabled whether it is a buslist instruction or an asynchronous halt (BC Control Register write of 0000 *hex*).

The NO-OP instruction can be used as a place holder instruction. It can be inserted or removed to change the buslist without re-structuring the entire sequence. The NO-OP instruction also provides an option that posts an interrupt to the host before proceeding to the next instruction. The NO-OP instruction takes approximately four microseconds to execute. Adding interrupt, ELT reset and Discrete Out signaling will increase this time.

3.2.3 Error Response

In actual 1553 applications specific transmitting or receiving errors indicate problems. As the BC, each data transfer command or mode code can be programmed to take a specific action if a protocol error is detected on the 1553 bus. The available actions include:

No Retry
Retry Once on the Same Bus
Retry Once on the Opposite Bus
Retry Once on the Same Bus. If unsuccessful, retry once on the opposite bus.

In the action "Retry Once on the Opposite Bus," the instruction may specify that if the retry on the opposite bus is successful, the primary bus should be switched to the opposite bus.

3.2.4 Protocol Errors and Status Exceptions

MIL-STD-1553A or B Protocol errors are detected when RTs do not respond or respond with a message error bit set in the status word. Protocol errors include:

No Response (the RT does not respond)
Manchester or parity error occurs in RT transmission
The RT address field of the RT's status word does not match the RT address field of the command word

Status exceptions are detected when a bit other than the address field is set in the RT's status word.



NOTE: The GLD-PC/S cannot simulate or handle the superseding valid command function in BC mode.

3.3 Buslist Instructions

Any number of buslists can be defined within the Dual-Port RAM. The GLD-PC/S execute these lists once the starting address is written to the BC Control Register. A buslist can be defined for each simulation allowing minimal host intervention during real-time simulation. A HALT instruction terminates the buslist. During simulation, the GLD-PC/S updates BC data in the Dual-Port RAM, continue execution of the appropriate buslist instructions, and ensure 1553 bus traffic conforms to MIL-STD-1553A or B specifications.

When the emulated BC is commanded to start, it reads instructions from a buslist and executes them sequentially until the BC encounters a HALT or JUMP instruction. If the BC is programmed to stop on errors, it will halt when it encounters an error condition.

A buslist instruction block is made up of four 16-bit words. Bits 12-15 of Word Zero of an instruction block identify the instruction type (0-9 *hex*).

The Discrete Out Signal (DOS) may be generated by the BC to signal the start of the desired command. This signal is enabled or disabled by Bit 0 of Word Zero of each buslist instruction block. The signal is active for two microseconds and occurs before the command is placed out on the 1553 bus.

3.3.1 Types of Buslist Instruction Blocks

The following buslist instruction blocks are assigned a hexadecimal number:

0 *hex*	NO-OP
1 *hex*	JUMP
2 *hex*	HALT
3 *hex*	MODE CODE
4 *hex*	BC-TO-RT TRANSFER
5 *hex*	RT-TO-BC TRANSFER
6 *hex*	RT-TO-RT TRANSFER
7 *hex*	HALT UNTIL DELAY
8 *hex*	RESET STACK
9 *hex*	INTERMESSAGE DELAY
A-F *hex*	Reserved

Other parameters in a buslist instruction block depend on the block type. Buslist instruction blocks are stored in memory locations from 1440 *hex* - 7FFF *hex*.

3.3.2 Bit Ordering

Bit 15 is the most significant bit and bit 0 is the least significant bit.

3.3.3 NO-OP (Instruction 00 *hex*)

The NO-OP instruction can be used as a place-holder instruction. It can be inserted or removed to change the buslist without re-structuring the entire sequence. The BC proceeds to the next buslist instruction block in approximately four microseconds. Adding interrupt, Elapsed Timer reset and Discrete Out signaling will increase this time. If the NO-OP Interrupt Enable Bit (Bit 11) is set to 1, the BC posts a NO-OP Interrupt before proceeding to the next buslist instruction block. (Figure 3-1).

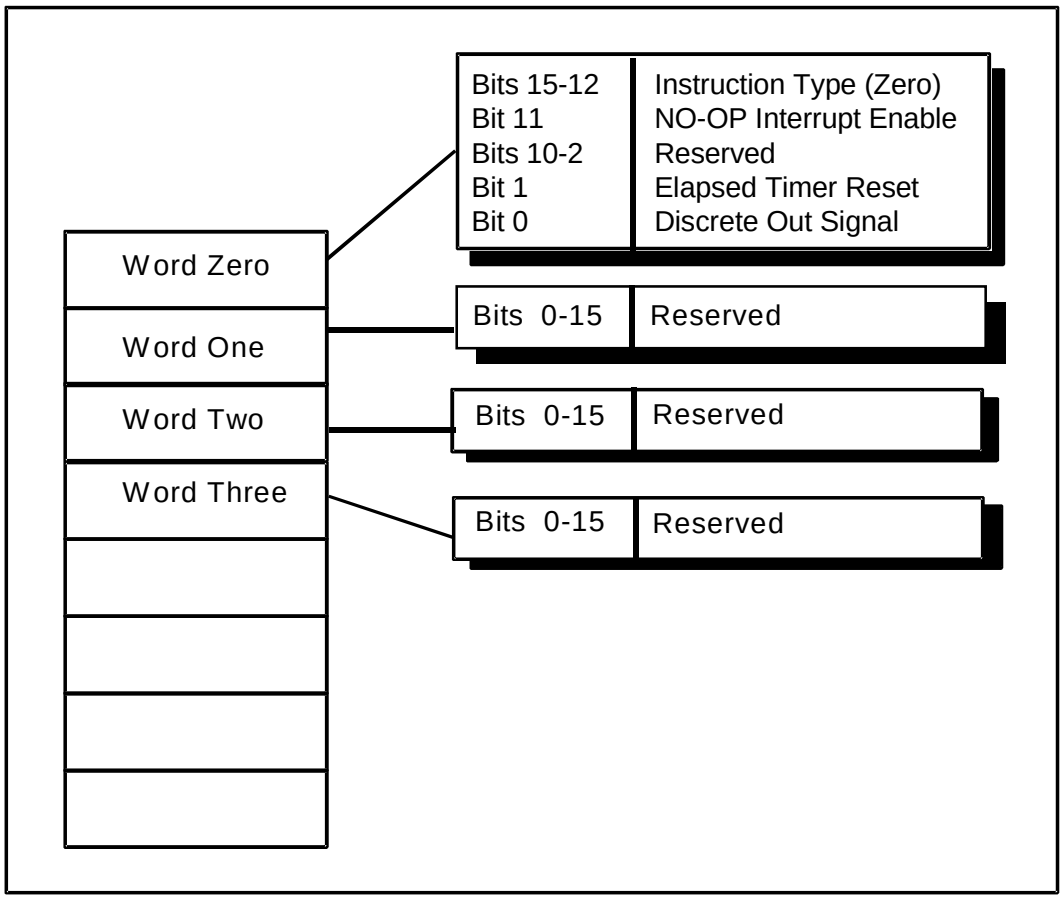


Figure 3-1 NO-OP Structure (Instruction 00 hex)

Word Zero

Bits 15-12	Instruction Type (00 *hex*)
Bit 11	NO-OP Interrupt Enable
Bits 10-2	Reserved
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Words One, Two and Three

All 16 bits of Words One, Two and Three are reserved.

3.3.4 JUMP (Instruction 01 hex)

The JUMP instruction is a branch instruction that can interrupt the sequential execution of buslist instructions (Figure 3-2). Bits 11-8 of buslist Instruction 01 *hex* determine the type of JUMP instruction (Table 3-1). Three types of JUMP instructions and a RETURN instruction allow host-independent real-time RT polling.

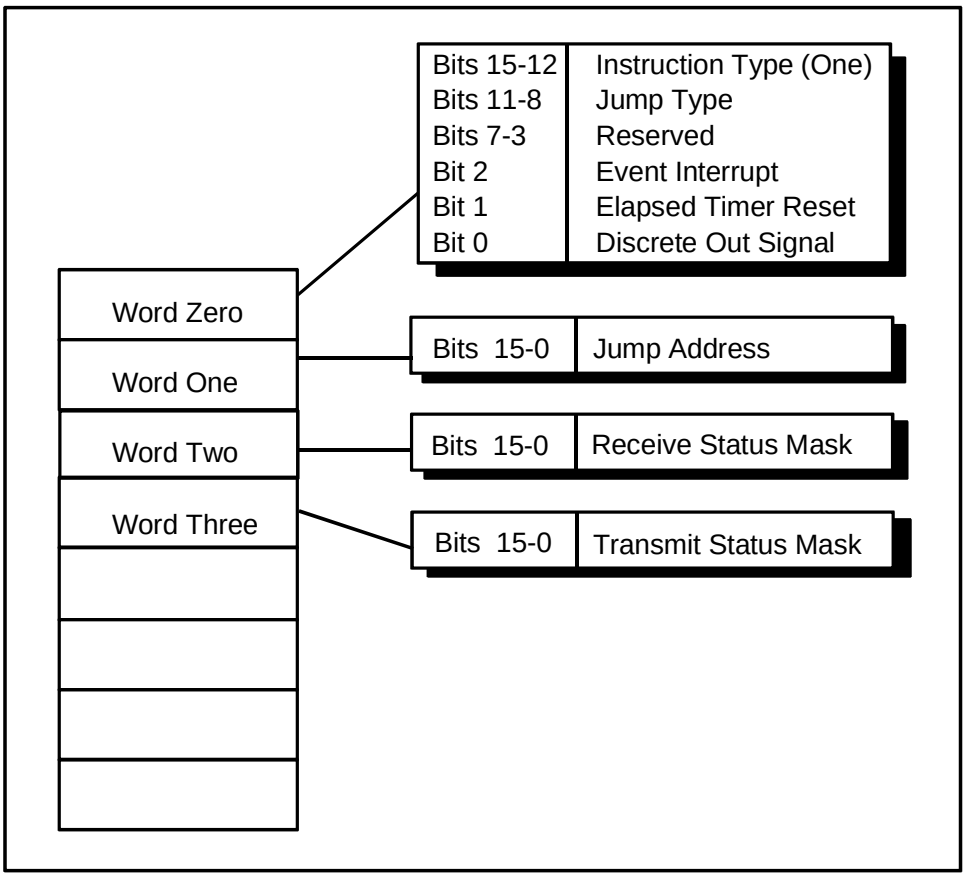


Figure 3-2 JUMP (Instruction 01 hex)

Table 3-1 JUMP Types (Bits 8-11)

Bits	JUMP Types
0000	Jump Always
0001	Conditional Jump to Sublist on Status Mask
0010	Conditional Jump to Sublist on Protocol Error
0011	Return From Sublist
0100	Unconditional Jump Sublist

JUMP instructions contain the jump address (Bits 15 through 0 of Word One) that locates the memory address of the next buslist instruction to execute.

When a JUMP sublist is executed, the address of the instruction is stored in a stack of up to four JUMP addresses. If this JUMP address stack overflows, the BC generates a Stack

Overflow Interrupt. A software or hardware reset automatically resets the JUMP address stack pointer. The return from sublist instruction will pop the address from the top of the stack.

Word Zero

Bits 15-12	Instruction Type (01 *hex*)
Bits 11-8	JUMP Type Defines the type of jump that the BC executes.
Bits 7-3	Reserved
Bit 2	Event Interrupt
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Word One

Bits 15-0	JUMP Address The Memory Address of the next buslist instruction to execute.

Word Two

Bits 15-0	Receive Status Mask The JUMP to sublist on status mask instruction logically ANDs the Receive status response received from the MIL-STD-1553A or B bus with this word. If the result is non-zero the BC pushes the next instruction address on the stack then jumps to the buslist instruction at the location specified in Word One. If the result is zero the BC proceeds to the instruction following the JUMP.

Word Three

Bits 15-0	Transmit Status Mask Same as Word Two (except that the status response received from the MIL-STD-1553A or B bus is a Transmit Status Word).

JUMP ALWAYS (0000)

This branch instruction always causes the buslist instruction block pointer to point to the next desired buslist instruction (as defined in Word One of the buslist instruction block). No entry is added to the JUMP-address stack upon execution of this instruction.

CONDITIONAL JUMP TO SUBLIST ON STATUS MASK (0001)

The BC can be made to compare a mask to the Transmit or Receive Status (or both in RT-to-RT transfer). By ANDing bits in the corresponding Status Mask with the RT Status, the BC can determine if a jump will occur. A jump occurs only if a non-zero value is returned after the AND condition.

EXAMPLE

RT Status Response	1400
Status Mask	07FF
Result of AND	0400

Since the result of AND is non-zero, JUMP to Sublist occurs.

CONDITIONAL JUMP TO SUBLIST ON PROTOCOL ERROR (0010)

This instruction causes the BC to jump to a sublist of buslist instructions, if a protocol error is detected in the previous MIL-STD-1553A or B transfer. The following errors result in a conditional jump:

No Response from an RT. A Broadcast Message is excluded since no response is correct.
Wrong RT Address from Responding RT
Manchester Error on Status or Data from a Responding RT

RETURN FROM SUBLIST (0011)

This instruction causes the BC to remove the last address placed on the JUMP address stack and jump to the buslist instruction at that address.



NOTE: A return execution from an empty JUMP stack will result in unpredictable buslist sequence.

UNCONDITIONAL JUMP SUBLIST (0100)

This instruction is similar to a JUMP-ALWAYS but places a return address on the stack before executing the jump. The instruction then continues executing the buslist at the memory address contained in the instruction. (Figure 3-3).

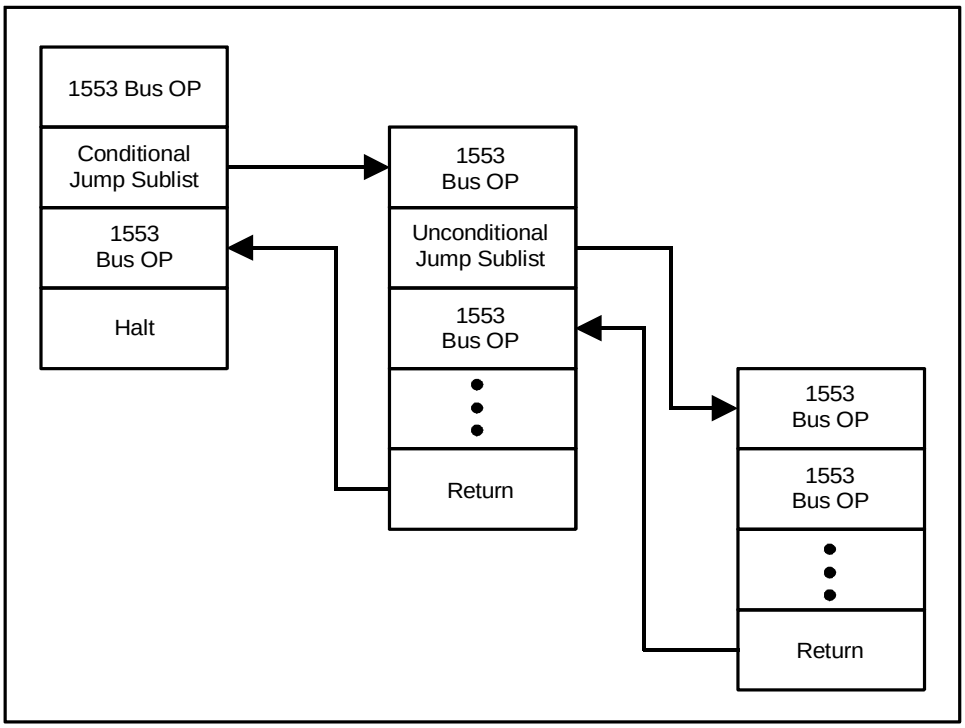


Figure 3-3 JUMP Sublist Example

3.3.5 HALT (Instruction 02 *hex*)

This instruction terminates a buslist and generates an interrupt. The interrupt cannot be disabled and will always serve as confirmation of the buslist completion.

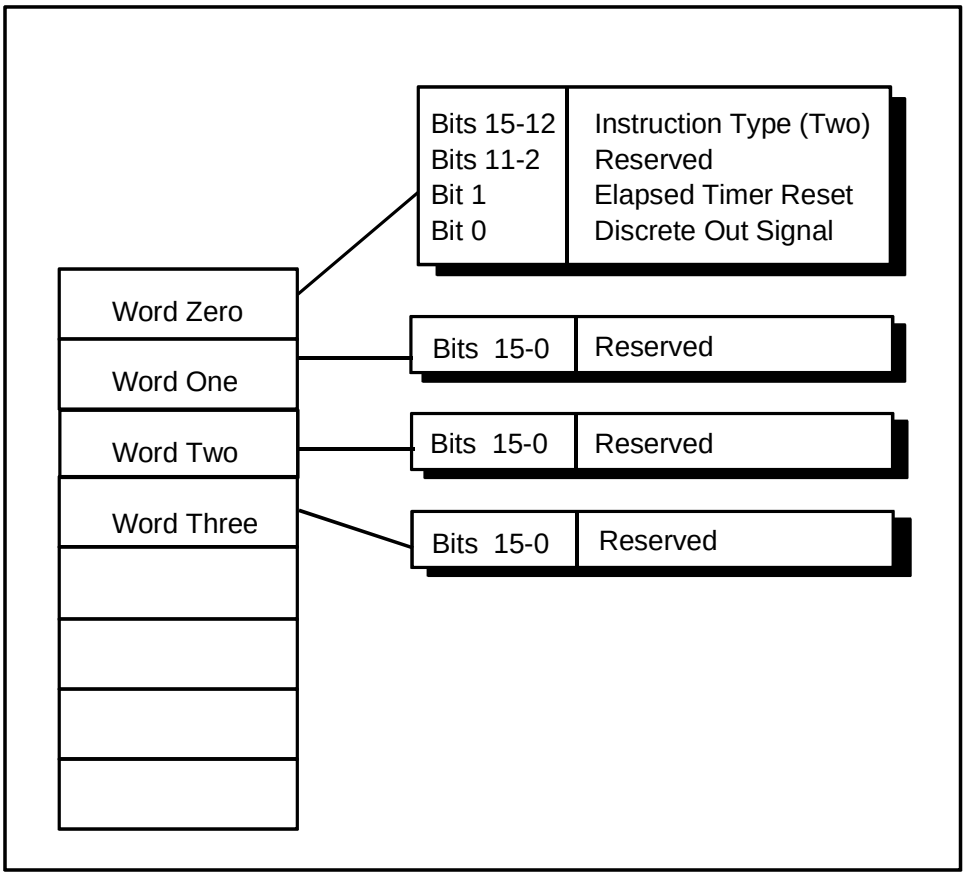


Figure 3-4 HALT (Instruction 02 *hex*)

Word Zero

Bits 15-12	Instruction Type (02 *hex*)
Bits 11-2	Reserved
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Words One through Three

All 16 bits on Words One through Three are reserved.

3.3.6 MODE CODE (Instruction 03 *hex*)

This instruction causes the BC to generate a MODE CODE Command on the 1553 bus and is composed of the following words (Figure 3-5).

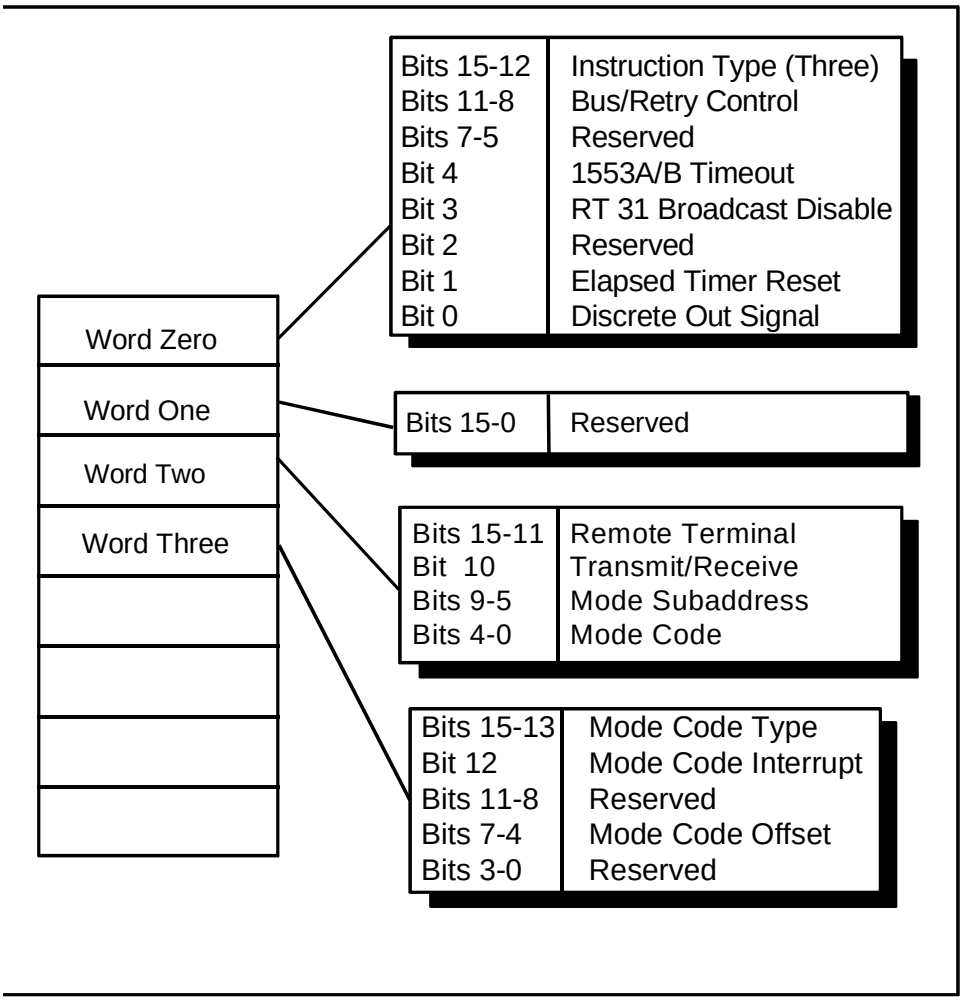


Figure 3-5 MODE CODE (Instruction 03 hex)

Word Zero - Control Word

Bits 15-12	Instruction Type (03 *hex*)
Bit 11	Current Bus
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 µsec) 1 = 1553A (9 µsec)
Bit 3	RT31 Broadcast Disable - must be set for 1553A instructions
Bit 2	Reserved. This bit must be set to ‘0’ or an interrupt-on-instruction will occur.

Bit 1 Elapsed Timer Reset
If set to '1', the GLD-PC/S resets the onboard Elapsed Timer to '0' prior to executing this command block.

Bit 0 Discrete Out Signal
If set to '1', the GLD-PC/S generates a signal to the RS-422 connector prior to executing this command block. The length of this signal is two microseconds.



NOTE: If Automatic Retry on current bus (Bit 10) and Opposite Bus (Bit 9) are both set, the GLD-PC/S retries on the current bus before attempting a retry on the opposite bus.

Word One - Reserved

Bits 15-0 Reserved

Word Two - 1553 Command Word

Bits 15-11 Remote Terminal (0-31)

Bit 10 Transmit or Receive
1=Transmit 0=Receive

Bits 9-5 Mode Subaddress (0 or 31)

Bits 4-0 MODE CODE
MIL-STD-1553A or B Mode Code as *hex*adecimal value

Word Three - Interpretation Word

Bits 15-13 MODE CODE Type
0=Reserved
1=No Data Word
2=BC Sends Data
3=BC Receives Data
4-7=Reserved

Bit 12 MODE CODE Interrupt
When set, an interrupt is generated after the buslist instruction is executed.

Bits 11-8 Reserved

Bits 7-4 Offset Into BC Mode Code Data Block (0-F *hex*)
Data is transmitted from or received into this location (1430 *hex* + offset) depending on the Mode Code Type. This field is ignored when the Mode Code Type =1.

Bits 3-0 Reserved

3.3.7 BC-to-RT TRANSFER (Instruction 04 *hex*)

This instruction generates a master to remote terminal command on the 1553 bus. This instruction is composed of the following words (Figure 3-6).

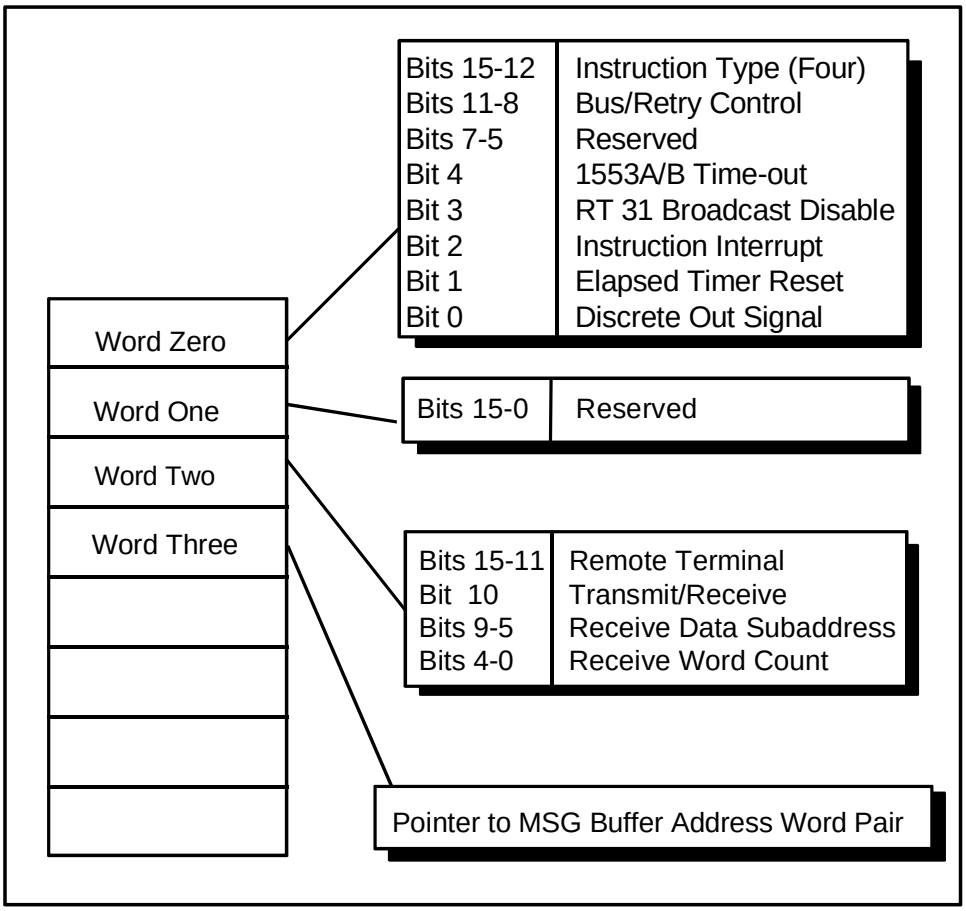


Figure 3-6 BC-TO-RT TRANSFER (Instruction 04 hex)

Word Zero - Control Word

Bits 15-12	Instruction Type (04 *hex*)
Bit 11	Current Bus - Set to '0' for bus A Set to '1' for bus B
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 μsec) 1 = 1553A (9 μsec)
Bit 3	RT 31 Broadcast Disable - must be set to '1' for 1553A instructions.
Bit 2	Instruction Interrupt If set to '1', the GLD-PC/S posts an interrupt when the command block

is executed and processed, before proceeding to the next buslist instruction.

Bit 1 — Elapsed Timer Reset
If set to '1', the GLD-PC/S resets the onboard Elapsed Timer to '0' prior to executing this command block.

Bit 0 — Discrete Out Signal
If set to '1', the GLD-PC/S generates a signal to the RS-422 connector prior to executing this command block. The length of this signal is two microseconds.

Word One - Reserved

Bits 15-0 — Reserved

Word Two - 1553 Command Word

Bits 15-11 — Receive Remote Terminal

Bit 10 — 0 = Receive - since this is a BC to RT

Bits 9-5 — Receive Data Subaddress

Bits 4-0 — Receive Word Count

The quantity of data words to be received by the RT.

1 *hex* - 1F *hex* = 1 - 31 decimal words

0 *hex* = 32 decimal words

Word Three - Message Buffer Address Word Pair

Bits 15-0 — The message block contains the pointers where the host stores data being transmitted by the BC (Figure 3-12).

3.3.8 RT-to-BC TRANSFER (Instruction 05 *hex*)

This instruction generates a Remote Terminal to Master Command on the 1553 bus. The structure of this instruction is identical to Instruction Four BC-to-RT Transfer (Figure 3-7).

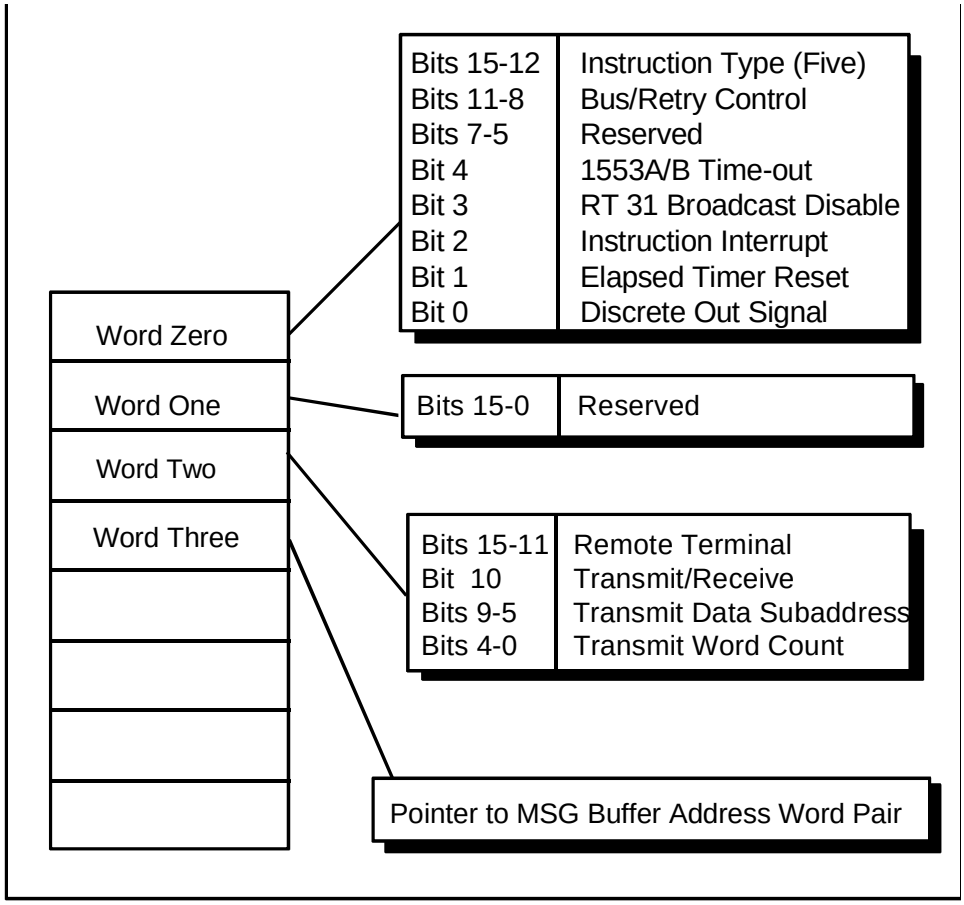


Figure 3-7 RT-TO-BC TRANSFER (Instruction 05 *hex*)

Word Zero - Control Word

Bits 15-12	Instruction Type (05 *hex*)
Bit 11	Current Bus - Set to '0' for bus A Set to '1' for bus B
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 μsec) 1 = 1553A (9 μsec)
Bit 3	RT31 Broadcast Disable - must be set for 1553A instructions
Bit 2	Instruction Interrupt

If set to '1', the GLD-PC/S posts an interrupt when the command block is executed and processed, before proceeding to the next buslist instruction.

Bit 1 Elapsed Timer Reset

If set to '1', the GLD-PC/S resets the onboard Elapsed Timer to 0 prior to executing this command block.

Bit 0 Discrete Out Signal

If set to '1', the GLD-PC/S generates a signal to the RS-422 connector prior to executing this command block. The length of this signal is two microseconds.

Word One - Reserved

Bits 15-0 Reserved

Word Two - 1553 Command Word

Bits 15-11 Transmit Remote Terminal

Bit 10 1 = Transmit - since this is a RT to BC transfer

Bits 9-5 Transmit Data Subaddress

Bits 4-0 Transmit Word Count

The quantity of data words to be transmitted by the RT.

1 *hex* - 1F *hex* = 1 - 31 decimal words

0 *hex* = 32 decimal words

Word Three - Message Buffer Address Word Pair

Bits 15-0 Pointer to the Message Buffer Address Word Pair for BC data storage.

3.3.9 RT-to-RT TRANSFER (Instruction 06 *hex*)

This instruction generates the two commands for a 1553 Remote Terminal to Remote Terminal transfer. RT-to-RT transfer involves the following words (Figure 3-8).

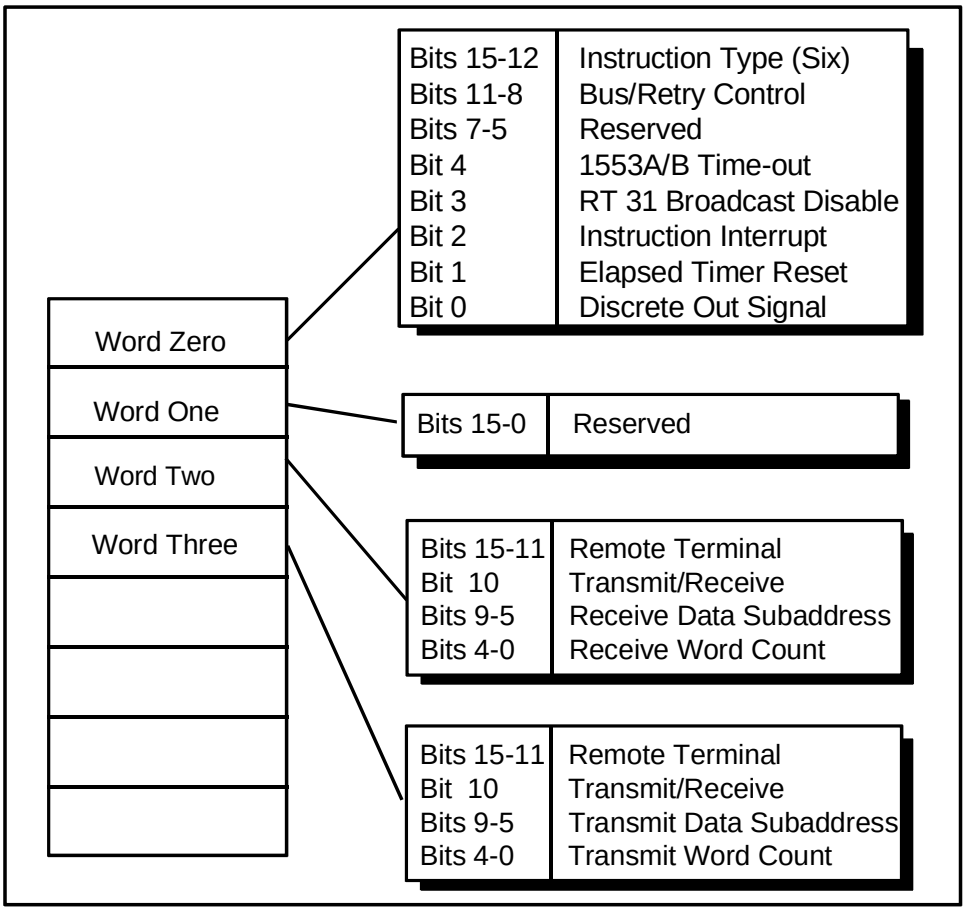


Figure 3-8 RT-TO-RT TRANSFER (Instruction 06 hex)

Word Zero - Control Word

Bits 15-12	Instruction Type (06 *hex*)
Bit 11	Current Bus - Set to '0' for bus A Set to '1' for bus B
Bit 10	Automatic Retry on Current Bus
Bit 9	Automatic Retry on Opposite Bus
Bit 8	Modify Current Bus
Bits 7-5	Reserved
Bit 4	1553A/B Response Time-out - 0 = 1553B (14 μsec) 1 = 1553A (9 μsec)
Bit 3	RT 31 Broadcast Disable - must be set for 1553A instructions.

Bit 2	Instruction Interrupt If set to '1', the GLD-PC/S posts an interrupt when the command block is executed and processed, before proceeding to the next buslist instruction.
Bit 1	Elapsed Timer Reset If set to '1', the GLD-PC/S resets the ELT to '0' prior to executing this command block.
Bit 0	Discrete Out Signal If set to '1', the GLD-PC/S generates a signal to the RS-422 connector prior to executing this command block. The length of this signal is two microseconds.

Word One - Reserved

Bits 15-0	Reserved

Word Two - 1553 Receive Command

Bits 15-11	Receive Remote Terminal
Bit 10	0 = Receive
Bits 9-5	Receive Data Subaddress
Bits 4-0	Receive Word Count The quantity of data words to be received by the RT 1 *hex* - 1F *hex* = 1 - 31 decimal words 0 *hex* = 32 decimal words

Word Three - 1553 Transmit Command

Bits 15-11	Transmit Remote Terminal (0-31)
Bit 10	1 = Transmit
Bits 9-5	Transmit Data Subaddress
Bits 4-0	Transmit Word Count The quantity of data words to be transmitted by the RT 1 *hex* - 1F *hex* = 1 - 31 decimal words 0 *hex* = 32 decimal words

3.3.10 HALT UNTIL ELT (Instruction 07 *hex*)

This instruction is used for controlling the timing of commands to the 1553 bus. Instruction Seven halts the BC until the ELT equals a value contained within Word One and Word Two of this instruction (Figure 3-9).

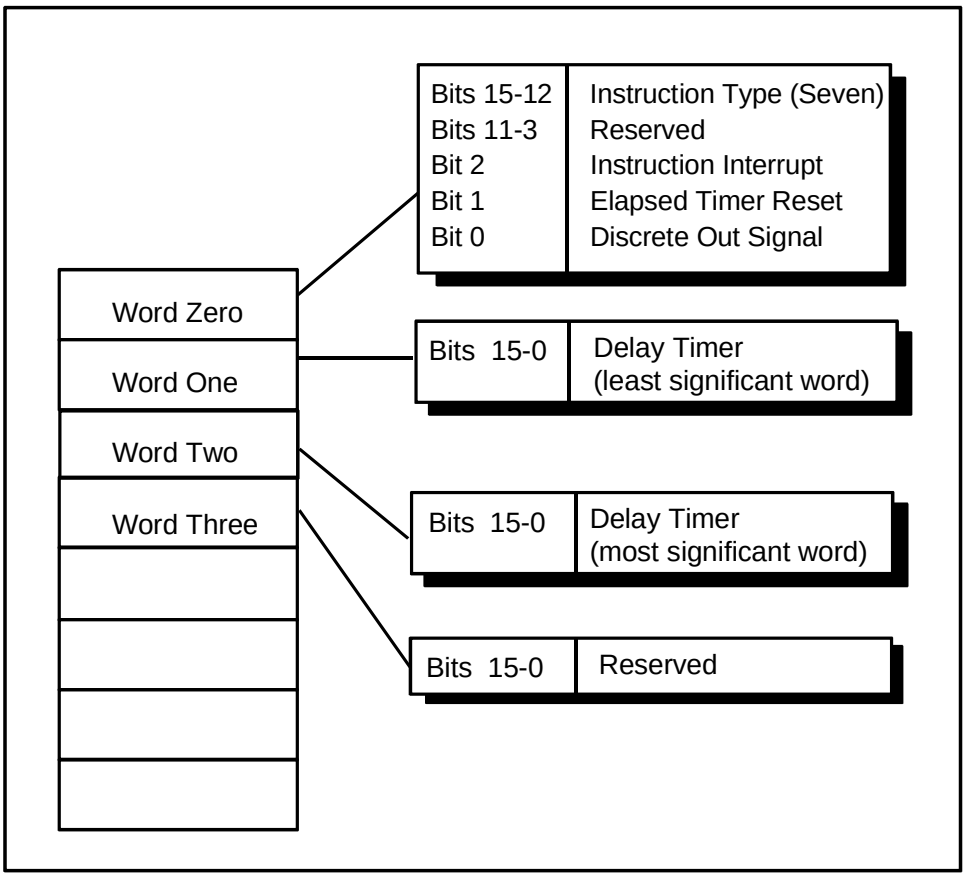


Figure 3-9 HALT UNTIL ELT (Instruction 07 hex)

Word Zero

Bits 15-12	Instruction Type (07 *hex*)
Bits 11-3	Reserved
Bit 2	Event Interrupt If set to '1', the GLD-PC/S posts an interrupt at the completion of executing and processing this command block before proceeding to the next buslist instruction.
Bit 1	Elapsed Timer Reset If set to '1', the GLD-PC/S resets the onboard Elapsed Timer to zero prior to executing this command block.
Bit 0	Discrete Out Signal If set to '1', the GLD-PC/S generates a signal to the connector prior to executing this command block. The length of this signal is two microseconds.

Word One

Bits 15-0	Elapsed Timer (least significant word) One microsecond resolution

Word Two

Bits 15-0	Elapsed Timer (most significant word) One microsecond resolution

Word Three

Bits 15-0	Reserved

3.3.11 RESET STACK (Instruction 08 *hex*)

This instruction resets the internal jump address stack pointer to the top. Addresses are not cleared, therefore any return instruction after a reset-stack will yield unpredictable buslist sequencing. (Figure 3-10).

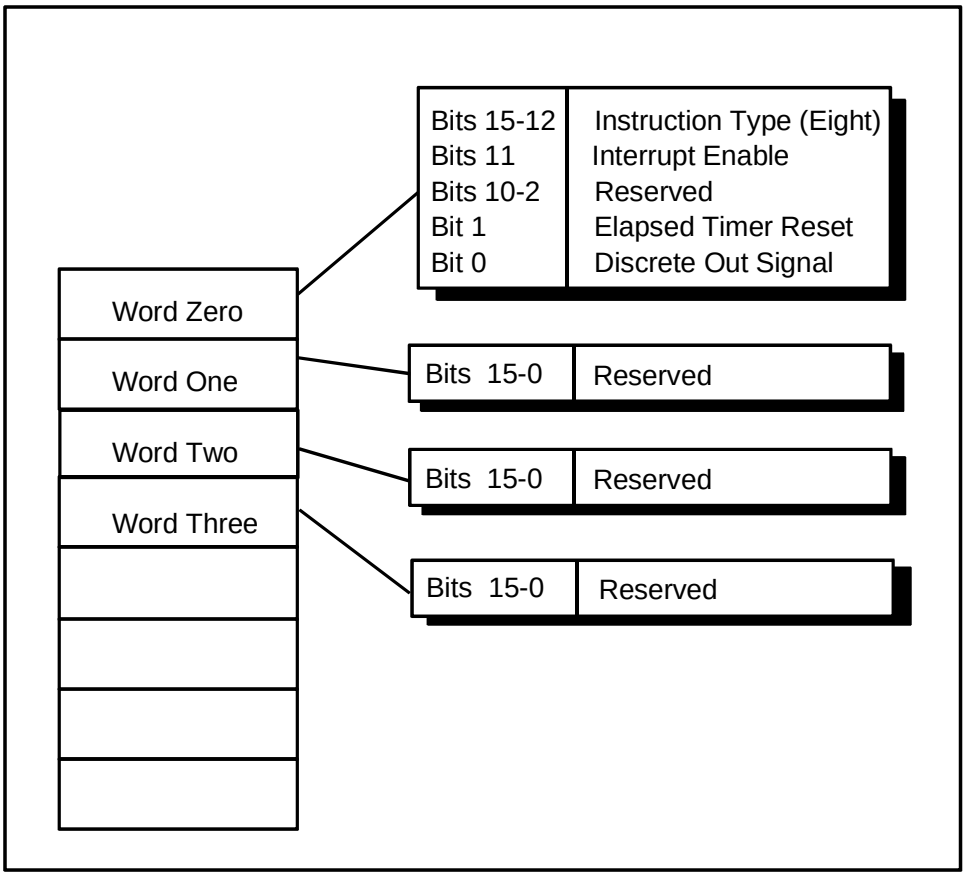


Figure 3-10 RESET STACK (Instruction 08 *hex*)

Word Zero

Bits 15-12	Instruction Type (08 *hex*)
Bit 11	Event Interrupt Enable
Bits 10-2	Reserved
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Words One through Three

All 16 bits of Words One through Three are reserved.

3.3.12 INTERMESSAGE DELAY (Instruction 09 *hex*)

This instruction allows the GLD-PC/S to wait a predetermined time before sending out the next instruction. This is used to insure a minimum gap between the end of one 1553 message and the beginning of the next command (Figure 3-11)

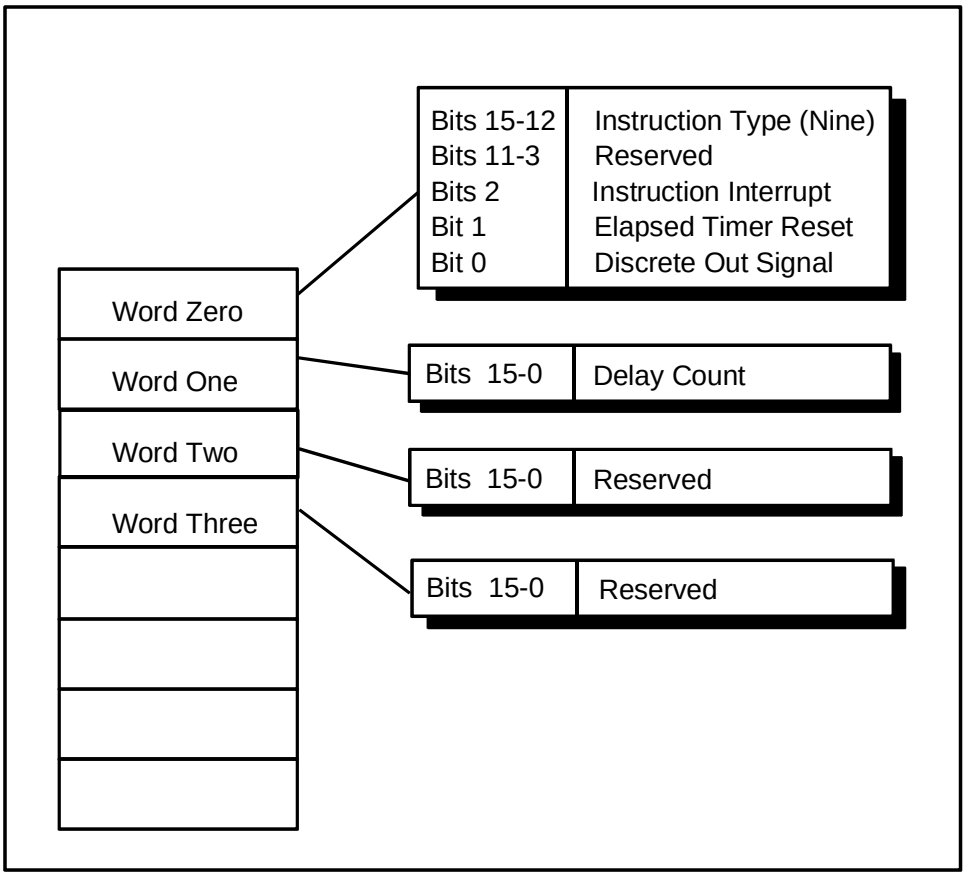


Figure 3-11 INTERMESSAGE DELAY (Instruction 09 *hex*)

Word Zero

Bits 15-12	Instruction Type (09 *hex*)
Bits 11-3	Reserved
Bit 2	Event Interrupt
Bit 1	Elapsed Timer Reset
Bit 0	Discrete Out Signal

Word One - Delay Count (in Hexadecimal)

Delay count (1 microsecond resolution)
If the event interrupt is not enabled, subtract 4 microseconds for overhead time.
If interrupt is enabled, subtract 8.5 microseconds.

3.4 Message Block Structure

The GLD-PC/S records the message blocks to indicate the addresses of the last buffer to receive data and the last buffer to transmit data. (Figure 3-12).

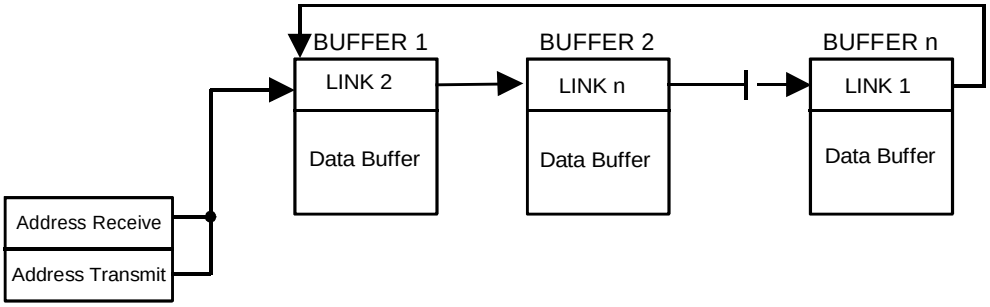


Figure 3-12 Message Block

The only words of the 1553 message stored in the buffer are the data words (Figure 3-13). Initially, the software loads both pointers with the address of the last buffer in the message block. The microcode modifies the pointers as the data in the buffers is transmitted and received.

link
header 1
header 2
data word 1
data word 2
data word 3
etc.

Figure 3-13 Message Buffer

3.4.1 Message Buffer Link Word

The first word of a message buffer is a link word containing the address of the next buffer in the message block. The link word of the last buffer holds the address of the first buffer (Figure 3-14). The software loads the correct value into the link word of each buffer.

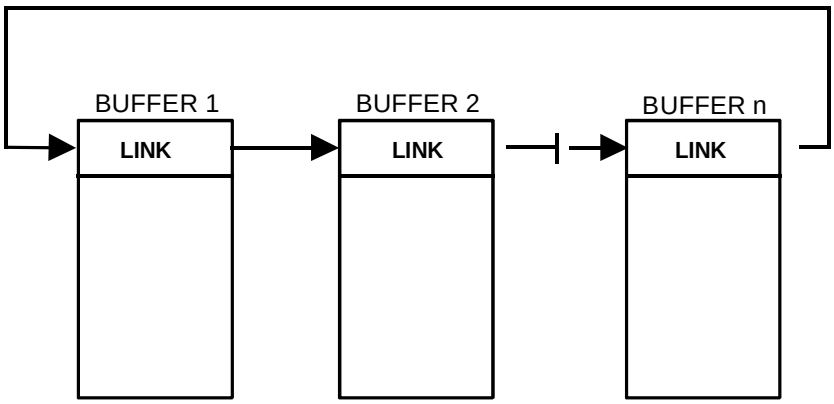


Figure 3-14 Message Buffer Link Words

HEADER WORD 1

The header word contains the buffer word count and the control and status bits. One header word bit indicates if a missed data condition occurs. The header word also contains a bit that indicates if a message has overwritten the buffer contents (new data bit was set in the next buffer and the overwrite current buffer bit is set in this buffer). The software and microcode write to several of the bits (Figure 3-15).

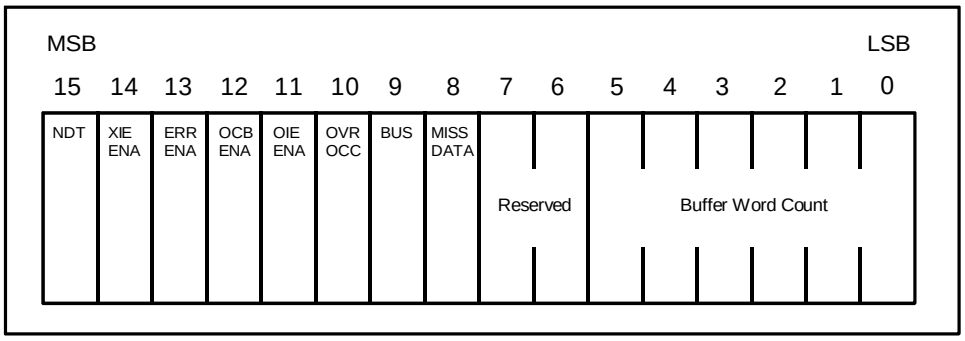


Figure 3-15 Header Word 1

Bit 15 New Data (NDT)

Set to ‘1’ by software before transmit. Set to ‘0’ by software before receive. Set to ‘1’ by microcode after receive. Set to ‘0’ by microcode after transmit.

This bit indicates when data is placed in the buffer or removed from the buffer. It is the handshake between software and microcode for real time processing. For a receive buffer, the microcode **writes** into the buffer and software **reads** data out of the buffer. Therefore, the microcode will set this bit when storing data and software will clear this bit when the buffer has been read by the host.

Conversely, for transmit buffers, the software **writes** into the buffer and microcode **reads** out of the buffer. Therefore, the software sets this bit when writing ‘newdata’ to transmit and the microcode clears this bit after it reads the data for transmit to the 1553 bus.

Bit 14 Transfer Interrupt Enable (XIE ENA)

Set to ‘1’ by software to enable interrupt. Set to ‘0’ by software to disable interrupt.

Bit 13 Error Interrupt Enable (ERR ENA)

Set to ‘1’ by software to enable interrupt. Set to ‘0’ by software to disable interrupt.

Bit 12 Overwrite Current Buffer (OCB ENA)

Set to ‘1’ by software to allow overwrite. Set to ‘0’ by software to prevent overwrite. The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. The data is stored in the current buffer if the New Data bit is clear or if the Overwrite Current Buffer bit is set and the new data bit in the next buffer is set.

Bit 11 Overwrite Interrupt Enable (OIE ENA)

Set to ‘1’ by software to enable interrupt, when an overwrite has occurred. Set to ‘0’ by software to disable interrupt.

Bit 10 Overwrite Condition Occurred (OVR OCC)

	Set to ‘0’ by software initially and after it is set by microcode. Set to ‘1’ by microcode when overwrite occurs.
Bit 9	Bus Used
	Set to ‘0’ initially and during simulation it is set or cleared by microcode. A ‘1’ indicates Bus A and a ‘0’ indicates Bus B.
Bit 8	Missed Data Condition Occurred (MISS DATA)
	Set to ‘0’ by software initially and after it is set by microcode. Set to ‘1’ by microcode when overwrite occurs. If the new data bit is set in the next buffer and the Overwrite Current buffer is cleared in this buffer, then the Missed Data bit will be set and the data will not be stored.
Bits 7-6	Reserved
Bits 5-0	Buffer Word Count (0-63)

HEADER WORD 2

The received word count field is stored by the microcode in Header Word 2 and reflects the number of data words stored during a receive message (Figure 3-16). If this same buffer is involved in a transmit message, the received word count field is set to 0 by the microcode. Bits 15-6 are reserved and may be non-zero.

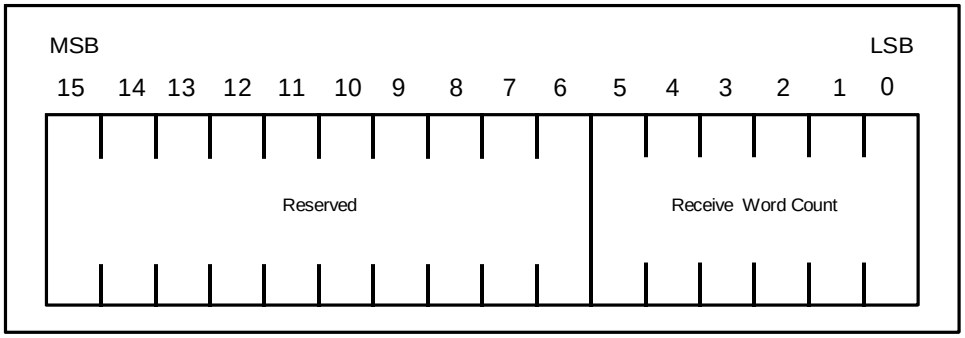


Figure 3-16 Header Word 2

DATA WORDS

The data words transacted in the 1553 message follow Header Word 2.

3.5 BC MODE CODE Data Block

MODE Commands with data are stored in the BC MODE CODE Data Block. This Block is located at the fixed memory location 1430 *hex* - 143F *hex*.

When a MODE Command (with Data Word) is issued by the BC, the MODE CODE Instruction in the buslist instruction block contains an offset (0-F) from address 1430 *hex*, which is used to transmit a data word or store a received data word (Figure 3-17).

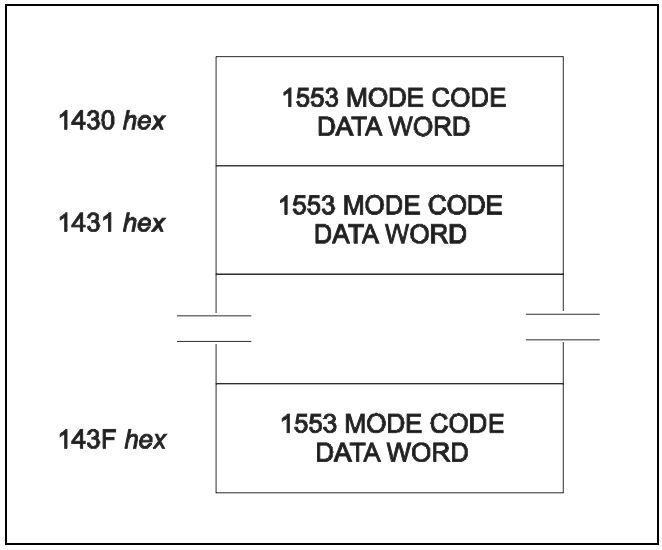


Figure 3-17 BC MODE CODE Data Block

4. 0 MULTIPLE REMOTE TERMINAL MODE

4.1 Overview

The MRT mode allows emulation of up to 32 RTs in 1553A mode and 31 RTs and one Broadcast RT in 1553B mode. For each RT, up to 32 subaddresses may be configured. Subaddresses 0 (for both 1553A and B protocol) and 31 (for 1553B mode only) are allowed as **mode code subaddresses**. Subaddresses 1 through 30 (and 31 for 1553A mode only) can only be configured as **data subaddresses**. This mode cannot operate simultaneously with the BC or CM modes.



NOTE: The GLD-PC/S does not handle the superseding valid commands in the MRT mode.

4.2 Status Block

In the MRT mode, each RT address is associated with a Status Block (located in Dual-Port RAM) which contains a control word, status word and other data relating to its configuration (Figure 4-1). The RT Status Blocks occupy a space in memory from 1000 *hex* - 11FF *hex*.

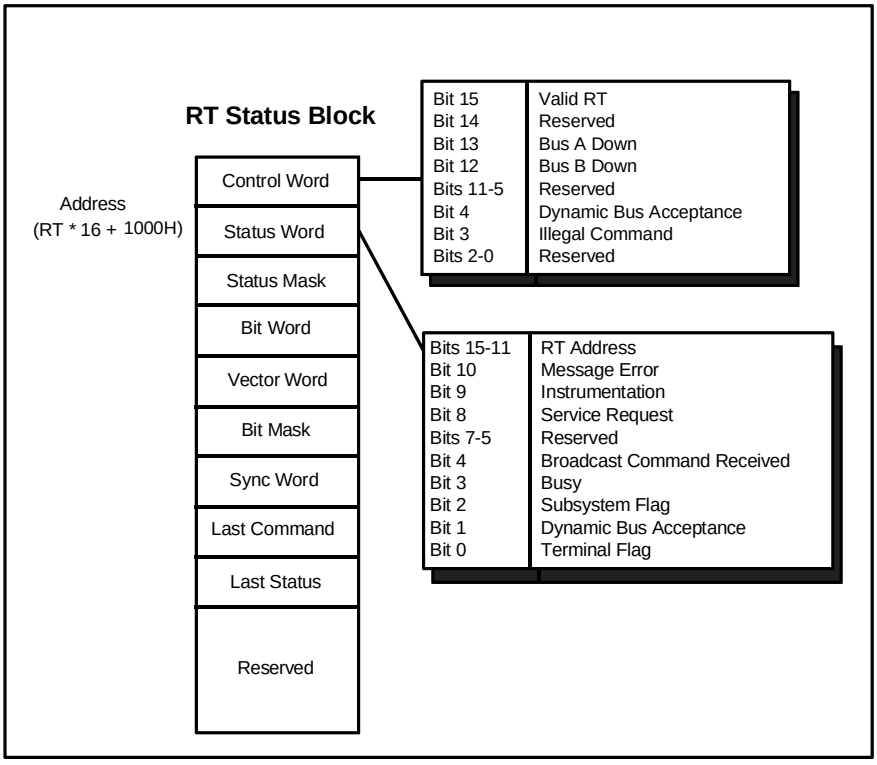


Figure 4-1 RT Status Block

The status block contains:

A control word for enabling and configuring RT characteristics.
The status response word of the RT
A mask to be ANDed with the RT's status word before it is sent out
The RT's BIT word
The RT's vector word
A mask that is ANDed with the BIT word if a Reset RT mode code is received
Sync word
The last command word to the RT
The last status response word of the RT

Table 4-1 RT Status Block Words

Words	Block Offset
Control Word	0000
Status Word	0001
Status Mask	0010
Bit Word	0011
Vector Word	0100
Bit Mask	0101
Sync Word	0110
Last Command	0111
Last Status	1000

During operation, each RT's status word is recalculated and the last command word and status word are updated as each message is received. Appropriate bits in the status word are set by the microcode. The RT receiving the command is a MIL-STD-1553A or B compliant RT.

Control Word

Bit 15 Valid RT

Bit 14 Reserved

Bit 13 Bus A Down
Indicates the Primary Bus is shut down. Bit 13 is affected by the Transmitter Shutdown and Override transmitter Shutdown mode commands. To have the host activate this function you must also select the corresponding RT bit in the RT Shutdown Enable Register (140D *hex* and 1410 *hex*).

Bit 12 Bus B Down
Indicates the Secondary Bus is shut down. Bit 12 is affected by the Transmitter Shutdown and Override Transmitter Shutdown mode commands. To have the host activate this function you must also select the corresponding RT bit in the RT Shutdown Enable Register (140D *hex* and 1410 *hex*).

Bits 11-5 Reserved

Bit 4 Dynamic Bus Acceptance
Controls the RT's response to an Accept BC mode command. If Bit 4 is

set to ‘1’, the RT sets the BC Acceptance Bit in its status, in response to that mode code.

Bit 3 — Illegal Command
If set to ‘1’, the RT responds to illegal mode commands by returning a status word with the Message Error Bit set, with no data words. If set to ‘0’, the RT does not respond to illegal commands.

Bits 2-0 — Reserved

Status Word

The Status word is ANDed with the RT Status Mask Word and sent as the RT's status response to all legal commands except a Transmit Last Status or Transmit Last Command mode code.

Bits 15-11 — RT Address
Per MIL-STD-1553A or B, Bits 15-11 indicate the RT address (0-31).

Bit 10 — Message Error
Bit 10 indicates a sync, length, parity or Manchester error. In 1553A mode, in the event of a Manchester error on the received data, the RT will properly respond with this bit set to ‘1’.

Bit 9 — Instrumentation
Bit 9 distinguishes a status word from a command word.

Bit 8 — Service Request (Optional)
Bit 8 indicates the RT has requested service.

Bits 7-5 — Reserved

Bit 4 — Broadcast Command Received

Bit 3 — Busy
Bit 3 indicates the RT is unable to move data.

Bit 2 — Subsystem Flag
Bit 2 indicates a fault in an RT (specifically, invalid data).

Bit 1 — Dynamic Bus Acceptance
Controls the RT’s response to an Accept BC mode command. If Bit 1 is set to ‘1’, the RT sets the BC Acceptance Bit in its status, in response to that mode code.

Bit 0 — Terminal Flag
Bit 0 should be set to ‘1’ when there is a fault in an RT.

Status Mask Word

When the Status Mask Word contains a ‘1’ in any bit position, the corresponding bit in the Status Word is transmitted. A ‘0’ causes the corresponding Status Bit to be transmitted as a zero regardless of the state of the bit in the Status Word. For most conditions, this word should be FFFF *hex*.

Bit Word

The user defines the Bit word to be transmitted in response to a Transmit Bit Word mode command. This word is reset by a Reset RT mode code, depending on the mask value in the RT Bit Mask Word. (ANDed with bit mask on Reset RT mode code).

Vector Word

The user-defined Vector word is transmitted in response to a Transmit Vector Word mode command. The Vector word notifies the BC that the RT requires service over and above the Service Request Bit being set.

Bit Mask Word

When the bit mask word has a '0' in any bit position, the corresponding bit in the Bit Word is reset upon reception of a Reset RT mode command. For most conditions this word should be FFFF *hex*.

Synchronization Word

The received data word with a Synchronize with Data mode command stored by the RT.

Last Command Word

The last valid command word received by this RT. This word is meaningless, if the Transmit Last Command mode code is the first command to the RT.

Last Status Word

This word is the Status Word associated with the last valid command addressed to the RT.

4.2.1 Addressing the Status Block

To address the status block, follow this formula:

RT#
0001 000 _ _ _ _ _ 0000 *bin*

Enter the appropriate binary RT number (0-31) in the five-bit space reserved for RTs.

EXAMPLE

To enter RT 2:

To calculate the origin of RT 2's status block, enter a binary '2' in the RT field (Bits 4-8).

RT#
0001 000 0 0 0 1 0 0000 *bin*

1 0 2 0 *hex* Convert to hexadecimal to arrive at the address of the status block .

4.3 Subaddress Response Word Pairs

Each RT's Subaddress Response word pair is located at pre-defined addresses. The GLD-PC/S computes the address of the RT's Subaddress Response word pair from the command word received by the emulated RT. If the subaddress field of the command word is 1 - 30 (and subaddress 31 for MIL-STD-1553A protocol), the GLD-PC/S uses the pointer in the second word to identify the message block's address. This message block's data buffer is used for the transfer on the MIL-STD-1553A or B bus. If the command word references subaddress 0 or 31 (MIL-STD-1553B protocol only), the GLD-PC/S uses the pointer in the second word to identify the address of the RT Mode Code Response Block.



NOTE: Subaddress 31 will respond as a data subaddress if 1553A protocol is selected, and as a mode subaddress if 1553B protocol is selected.

4.4 Extracting Address from the Command Word

The subaddress response word pairs are located in memory between addresses 0000 *hex* and 0FFF *hex*. There is one pair for the receive direction and one pair for the transmit direction for each RTSA combination.

To address the RECEIVE subaddress response word pairs:

	RT		SA	
0000	_____	0	_____	0 Word One - Control Word
0000	_____	0	_____	1 Word Two - Pointer

To address the TRANSMIT subaddress response word pairs:

	RT		SA	
0000	_____	1	_____	0 Word One - Control Word
0000	_____	1	_____	1 Word Two - Pointer

EXAMPLES

Example 1
To address Word One of RT 3, with SA1 to receive:

0000 00011 0 00001 0
RT3 SA 1

To access the second word, enter a '1' in Bit 0 of the address formula to calculate the address.

0000 00011 0 00001 1

Example 2
To address Word One of RT5, SA 10 to transmit:

0000 00101 1 01010 0
RT5 SA10

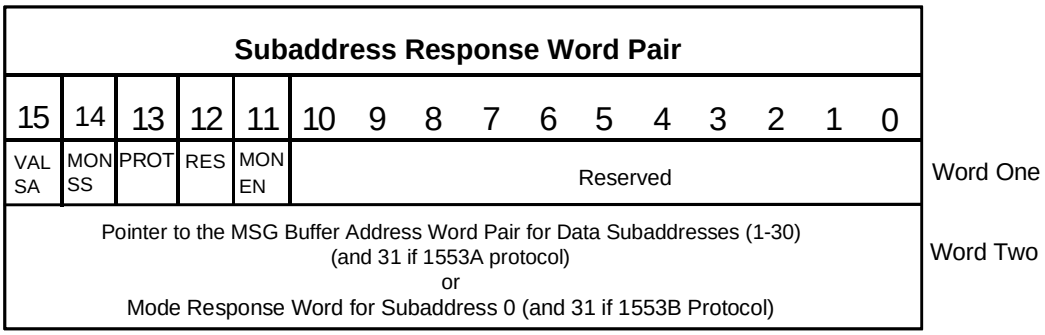


Figure 4-2 Subaddress Response Word Pair

Word One - Control Word

Bit 15 Valid Subaddress (VAL SA)

Set to '1' by software if this is a valid subaddress. Set to 0 by software if it isn't.

Bit 14 Monitor Snapshot (MON SS)

Set to '1' by software if message to this subaddress should generate a snap shot interrupt. Set to '0' by software if snap shot interrupt is not used.

Bit 13 1553 Protocol (PROT)

Set to '0' will declare subaddress a 1553B type. Set to a '1' will declare subaddress to be a 1553A protocol device.

Bit 12 Reserved

Bit 11 Monitor Enable (MON EN)

Set to '1' by software if subaddress is to be monitored. Set to '0' by software if this subaddress is not monitored.

Bit 10-0 Reserved

If the Monitor Bit (Bit 11) of the first word of Data Subaddress Response Word Pair is set to '1', a message directed to this RT/direction/SA combination is captured by the monitor. (Figure 4-2). The subaddress does not have to be enabled for the message to be captured (Bit 15 can be zero).

Word Two - Data Subaddress Pointer

Word Two points to the Message Buffer Address Word Pair located in the Message Block (Figure 4-3). This word pair contains the address in free memory of the last buffer used (one for receive and one for transmit).

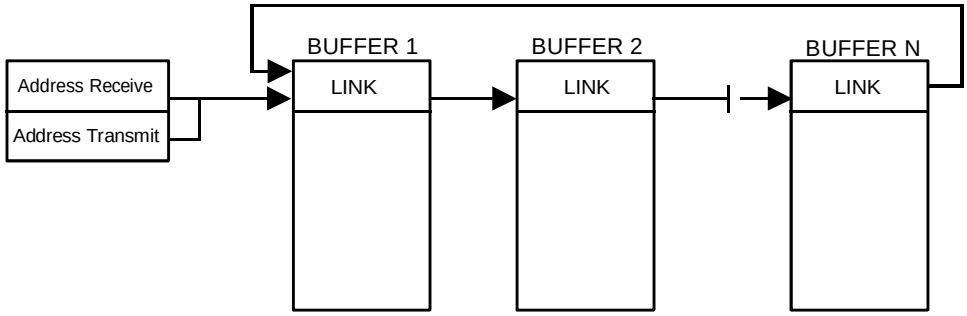


Figure 4-3 Message Block

When setting up a message block (using the *DefineBlockMBGld()* routine in the Interface Library), the routine loads both the receive and transmit address pointers with the same address, that of the last buffer in the message block. These pointers are automatically updated by the microcode to the next buffer in the linked list as data is received or transmitted into or out of a buffer. The only words of the 1553 message stored in the buffer are the data words (Figure 4-4).

link
header 1
header 2
data word 1
data word 2
data word 3
etc.

Figure 4-4 Message Buffer

Word Two - Mode Response Pointer

If the transmitted or received subaddress is ‘0’ (or ‘31’ for 1553B protocol), Word Two of the SA Response Word Pair points to the Mode Code Response Block. The on-board Configuration data adds the Mode Code number to contents of Word Two; thus, pointing to the proper Mode Code Response Word within the Mode Code Response Block.

4.5 Message Buffers

4.5.1 Message Buffer Link Word

The first word of a message buffer is a link word containing the address of the next buffer in the message block. The link word of the end buffer must contain the address of the first buffer (Figure 4-5). The software loads the correct value into the link word of each buffer.

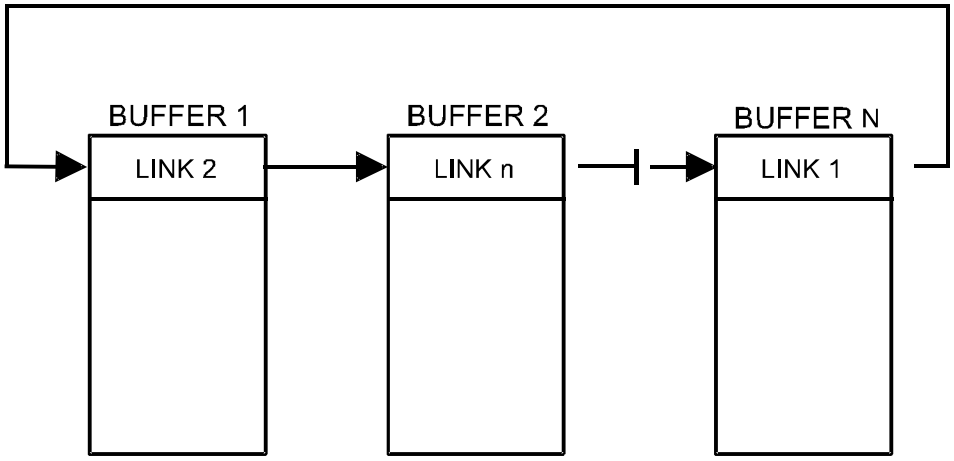


Figure 4-5 Message Buffer Link Words

4.5.2 Header Words

Header Word 1

The header word contains control bits and the word count for the message in the buffer. An overwrite control scheme is contained within the control bits. A message can overwrite the current buffer contents when the new data bit is set in the next buffer. Overwrite Current Buffer bit, Missed Data and New Data bits are set to '1' in this buffer to indicate the overwrite occurred. (Figure 4-6). The software also writes to several of the bits to control interrupts and error handling.

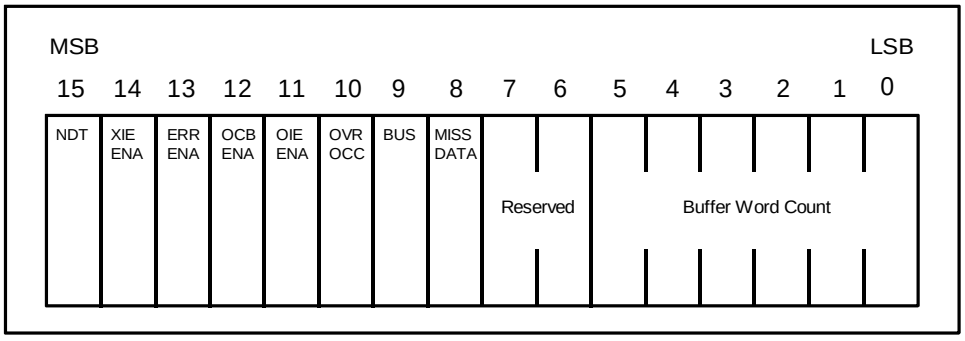


Figure 4-6 Header Word 1

Bit 15	New Data (NDT) Set to ‘1’ by software before transmit. Set to ‘0’ by software before receive. Set to ‘1’ by microcode after receive. Set to ‘0’ by microcode after transmit. This bit indicates when data is placed in the buffer or removed from the buffer. It is the handshake between software and microcode for real time processing. For a receive buffer, the microcode **writes** into the buffer and software **reads** data out of the buffer. Therefore, the microcode will set this bit when storing data and software will clear this bit when the buffer has been read by the host. Conversely, for transmit buffers, the software **writes** into the buffer and microcode **reads** out of the buffer. Therefore, the software sets this bit when writing ‘newdata’ to transmit and the microcode clears this bit after it reads the data for transmit to the 1553 bus.
Bit 14	Transfer Interrupt Enable (XIE ENA) Set to ‘1’ by software to enable interrupt. Set to ‘0’ by software to disable interrupt.
Bit 13	Error Interrupt Enable (ERR ENA) Set to ‘1’ by software to enable interrupt. Set to ‘0’ by software to disable interrupt.
Bit 12	Overwrite Current Buffer (OCB ENA) Set to ‘1’ by software to allow overwrite. Set to ‘0’ by software to prevent overwrite. The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. The data is stored in the current buffer if the New Data bit is clear or if the Overwrite Current Buffer bit is set and the new data bit in the next buffer is set.
Bit 11	Overwrite Interrupt Enable (OIE ENA) Set to ‘1’ by software to enable interrupt, when an overwrite has occurred. Set to ‘0’ by software to disable interrupt.
Bit 10	Overwrite Condition Occurred (OVR OCC) Set to ‘0’ by software initially and after it is set by microcode. Set to ‘1’ by microcode when overwrite occurs.
Bit 9	Bus Used Set to ‘0’ initially and during simulation it is set or cleared by microcode. A ‘1’ indicates Bus A and a ‘0’ indicates Bus B.
Bit 8	Missed Data Condition Occurred (MISS DATA) Set to ‘0’ by software initially and after it is set by microcode. Set to ‘1’ by microcode when overwrite occurs. If the new data bit is set in the next buffer and the Overwrite Current buffer is cleared in this buffer, then the Missed Data bit will be set and the data will not be stored.
Bits 7-6	Reserved
Bits 5-0	Buffer Word Count (0-63)

Header Word 2

The received word count field is stored by the microcode in Header Word 2 and reflects the number of 1553 data words received from the bus and stored in the buffer. If this same buffer is involved in a transmit message, the received word count field is set to ‘0’ by the microcode (Figure 4-7). Bits 15-6 are reserved and may be non-zero.

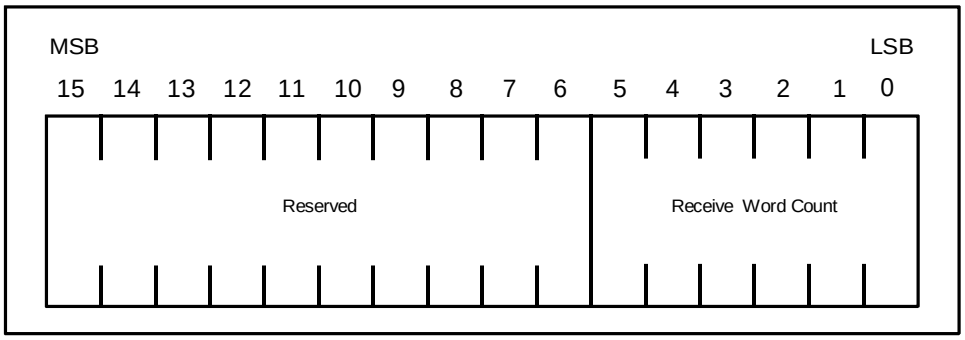


Figure 4-7 Header Word 2

4.5.3 Data Words

All data words transmitted in the 1553 message follow Header Word 2.

4.6 RT MODE CODE Response Word Block

The MODE CODE Response Word Block (Figure 4-8) is group a of 32 words, one for each MODE CODE, that specify the operation the MODE CODEs perform. The MODE CODE Response Block also specifies if the receipt of any particular MODE CODE causes the GLD-PC/S to interrupt the host. The first word in the block is placed in free memory between 1440 *hex*- End of Memory. The remaining words are offset from the initial address by n, where n = MODE CODE.

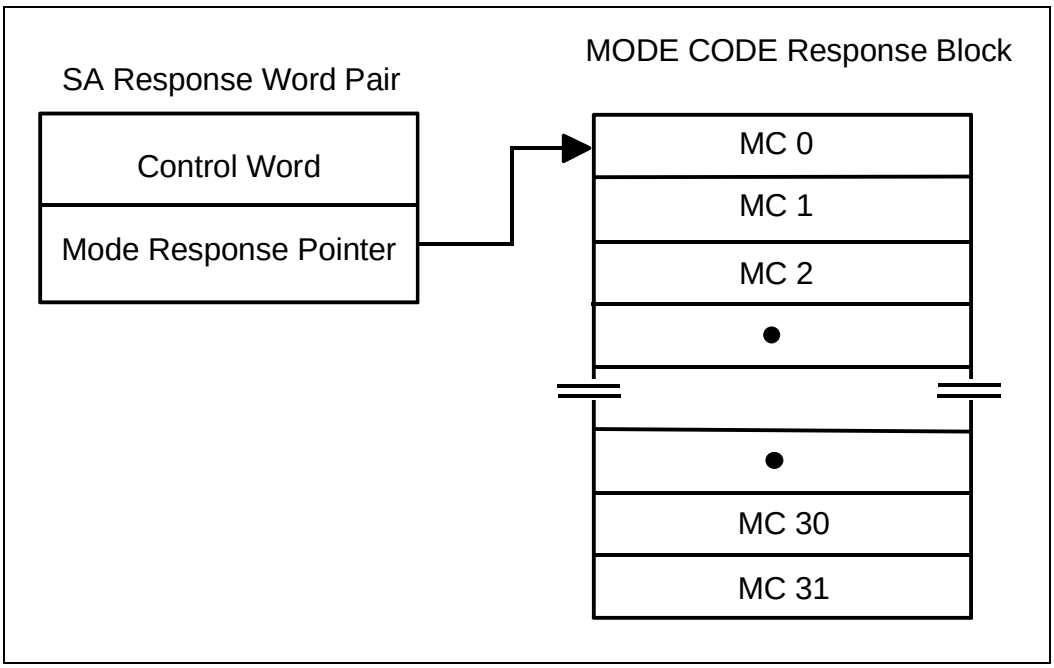


Figure 4-8 MODE CODE Response Block

4.7 MODE CODE Response Word

For a mode SA, the message is monitored only if the Monitor Bit (Bit 11) is set in the corresponding MODE CODE response word (Figure 4-9).

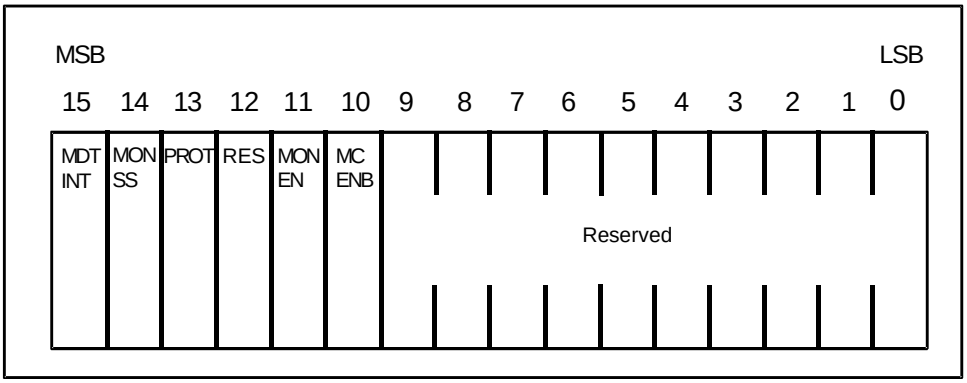


Figure 4-9 MODE CODE Response Word

Bit 15	Interrupt on Reception of MODE CODE (MDT INT) Set to '1' by software to enable interrupt. Set to '0' by software to disable interrupt.
Bit 14	Monitor Snapshot (MON SS) Set to '1' by software if message to this subaddress should generate a snap shot interrupt. Set to '0' by software if snap shot interrupt is not used.
Bit 13	1553 Protocol (PROT) Set to '0' will declare mode a 1553B type. Set to a '1' will declare mode to be a 1553A protocol device.
Bit 12	Reserved
Bit 11	Monitor Enable (MON EN) Set to '1' by software if subaddress is to be monitored. Set to '0' by software if this subaddress is not monitored.
Bit 10	MODE CODE Enable (MC ENB) Set to '1' by software to enable this mode code.
Bits 9-0	Reserved

4.8 Description of MODE CODE Microcode Operations

The only valid MODE CODE for 1553A operation is zero. Table 4-2 describes the MODE CODE operations for 1553B.

Table 4-2 MIL-STD-1553B Non-Broadcast MODE CODE Microcode Operations (RT 0-30)

MC Number	T/R	Operations Performed By Microcode
0	1	Dynamic Bus Control - Read RT Status Word as Status - If Dynamic Bus Acceptance (DBA) flag set in RT Control Word: Set DBA Bit in Status Word - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
1	1	Synchronize Without Data Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
2	1	Transmit Last Status Word - Read Last Status Word as Status - AND Status with Status Mask - Transmit Status onto Bus - Write Command into Last Command Word
3	1	Initiate Self-Test - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
4	1	Transmitter Shutdown - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Set Bit in RT Control Word to disable opposite bus - Write Status into Last Status Word - Write Command into Last Command Word

MC Number	T/R	Operations Performed By Microcode
5	1	Override Transmitter Shutdown - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Clear bit in RT Control Word to enable opposite bus - Write Status into Last Status Word
6	1	Inhibit Terminal Flag - Read RT Status Word as Status - Clear Terminal Flag Bit in Status - Mask to inhibit terminal flag - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
7	1	Override Inhibit Terminal Flag - Read RT Status Word as Status - Set Terminal Flag Bit in Status Mask to enable terminal flag - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
8	1	Reset Remote Terminal - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Logically AND the BIT Word with the BIT Mask then place the result back in the BIT Word - Clears bits in Control Word to enable both transmitters - Set the Terminal Flag Bit in the Status Mask to enable the Terminal Flag Bit
9-15	0 0	Illegal Mode Command - Read RT Status Word as Status If illegal flag set in RT control word, set Message Error Bit in Status. - AND Status with Status Mask - Transmit Status on bus - Write status in last status word - Write Command into Last Command Word - If flag clear in RT control word, do nothing

MC Number	T/R	Operations Performed By Microcode
16	1	Transmit Vector Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit Vector Word onto bus - Write Status into Last Status Word - Write Command into Last Command Word
17	0	Synchronize with Data Word - Read RT Status Word as Status - Write the received data to Sync Word - AND Status with Status Mask - Transmit Status onto bus - Write Status into Last Status Word - Write Command into Last Command Word
18	1	Transmit Last Command - Read Last Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit Last Command Word onto bus
19	1	Transmit BIT Word - Read RT Status Word as Status - AND Status with Status Mask - Transmit Status onto bus - Transmit BIT Word onto bus - Write Status into Last Status Word - Write Command into Last Command Word
20-31	0 0	Illegal

Table 4-3 MIL-STD-1553B Broadcast Mode Code Microcode Operations (RT=31)

MC Number	T/R	Operations Performed By Microcode
0	0 0	Illegal
1	1	Synchronize - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
2	0 0	Illegal
3	1	Initiate Self Test - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write Status into Last Status - Write Command into Last Command Word - Link to next broadcast RT
4	1	Transmitter Shutdown - Read RT Status Word as Status - Set BRC Bit in Status - Set bit in Master Shutdown Control Register to disable opposite bus - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
5	1	Override Transmitter Shutdown - Read RT Status Word as Status - Set BRC Bit in Status - Clear bit in Master Shutdown Control Register to enable opposite bus - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT

MC Number	T/R	Operations Performed By Microcode
6	1	Inhibit Terminal Flag - Read RT Status Word as Status - Set BRC bit in Status - Clear Terminal Flag Bit in status Mask to inhibit Terminal flag - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
7	1	Override Terminal Flag - Read RT Status Word as Status - Set BRC Bit in Status - Set Terminal Flag Bit in Status Mask to enable terminal flag - AND Status with Status Mask - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
8	1	Reset RT - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Clear bit in RT Control Word to enable opposite bus - Set Terminal Flag Bit in Status Mask to enable terminal flag - Logically AND the BIT Word with the BIT Mask. Place the result in the BIT Word - Write Status into Last Status Word - Write Command into Last Command Word - Link to next broadcast RT
9-16	0 0	Illegal
17	0	Synchronize with Data - Read RT Status Word as Status - Set BRC Bit in Status - AND Status with Status Mask - Write received data to Sync Word - Write Status into Last Status Word - Write Command into Last Command Word - Link to Next Broadcast RT
18-31	0 0	Illegal

4.9 Interrupts

The RT mode may post hardware interrupts to the host including:

Mode Code Execution
Message Transmission or Reception to or from a Message Block
Message Buffer Overflow Condition
Valid Transfer
Receiver Error Detected

5. 0 CHRONOLOGICAL MONITOR MODE

5.1 Overview

The Chronological Monitor (CM) Mode allows the capture of all or selected 1553 bus traffic This mode cannot run at the same time as either the BC or MRT modes. The GLD-PC/S board is able to monitor 1553A, 1553B and mixed-bus-traffic systems.

5.2 Data Capturing Methods

The CM mode operates in one of two methods:

record all (with and without snapshot)
filtered.

Both methods involve setting bits in the Data Subaddress Word Pairs and Mode Code Response Words. These are described in detail in Section 4.0 MULTIPLE REMOTE TERMINAL MODE.

5.2.1 Record All

To record all bus traffic, set Bit 11 (Monitor Enable) in every Transmit and Receive Data Subaddress Word Pair for each RT, and also set Bit 11 in each Mode Code Response Word. During active-bus monitoring a snapshot interrupt may be generated for a particular message based on the RT number, subaddress and direction of transmission.

The snapshot interrupt causes an interrupt packet to be put into the interrupt queue. This packet contains the memory address within the Monitor Buffer of the first command word in the message. The snapshot interrupt is generated by setting Bit 14 (Monitor Snapshot) in the appropriate Receive or Transmit Data Subaddress Word Pair. Snapshot interrupts can also be generated for any particular mode code. See Section 6.0 INTERRUPTS for details.

5.2.2 Filter

To filter bus traffic and record only specific messages, set only Bit 11 as described above for the particular messages of interest.

5.3 Monitoring 1553A Devices

The default setting for all Subaddress Response Word Pairs is for 1553B devices. To monitor any 1553A devices, Bit 13 must be set in the Subaddress Response Word Pair for each 1553A subaddress to be monitored.

5.4 Monitor Block

The monitor block consists of one or more monitor buffers (Figure 5-1). The monitor block requires that the address of the first monitor buffer be written to reserved-memory location 1408 *hex* before monitoring begins. To start monitoring, write a value of 0008 *hex* to the Chronological Monitor Control Register. This will capture all messages selected for monitoring with valid command words. Writing a value of 18 *hex* allows the monitor to record 1553 command words containing protocol errors.

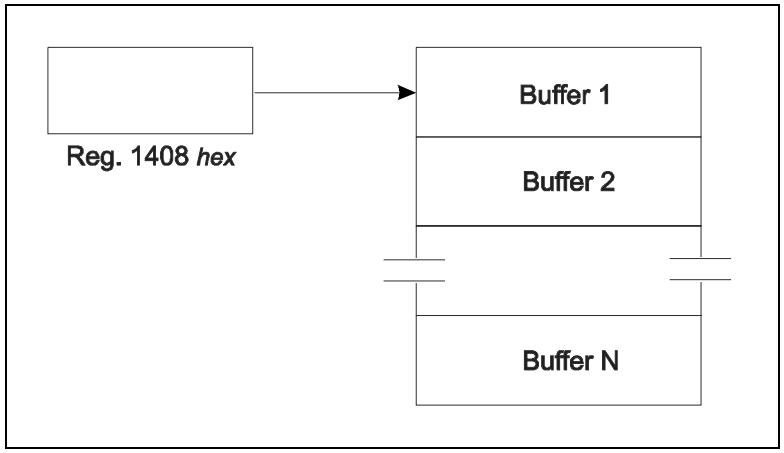


Figure 5-1 Monitor Block

Controling the monitor mode:

1. To capture all bus traffic, write a value of 0018 *hex* to Chronological Monitor Control Register.
2. To capture only bus traffic with valid commands, write a value of 0008 *hex* to Chronological Monitor Control Register.
3. To stop operation of the bus monitor mode at any time, write 0000 *hex* to the Register. This will not affect operation of the BC or MRT modes.

5.5 Monitor Buffer

The size of a monitor buffer ranges from 16 to 1008 (63*16) words (Figure 5-2). The buffer begins with a link word and a header word and ends with two reserved words. The remainder of the buffer (Message Records) is used to store 1553 messages and information related to the message, regarding error and time tagging.

link
header
message records
reserved
reserved

Figure 5-2 Monitor Buffer

5.5.1 Monitor Buffer Link Word

The first word of a monitor buffer, the link word, contains the address of the next monitor buffer. The link word of the last buffer must hold the address of the first buffer (Figure 5-3) to ensure a circular queue. User software is responsible for loading the correct value into the link word of each buffer.

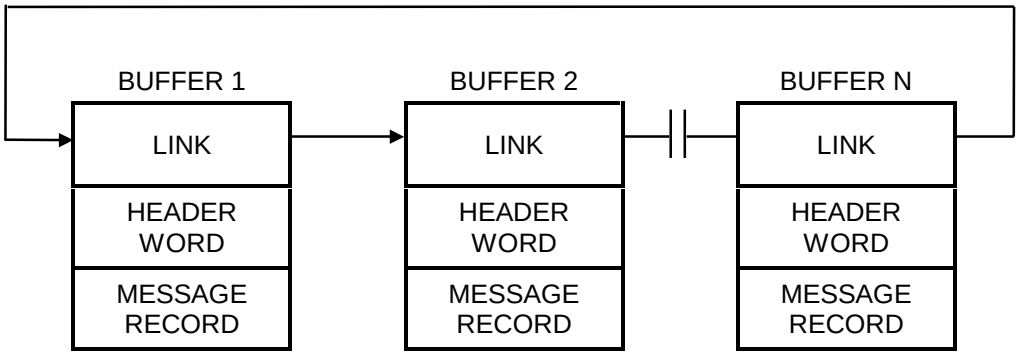


Figure 5-3 Monitor Buffer Link Word

Header Word

The header word (Figure 5-4) contains the control and status bits and buffer block count.

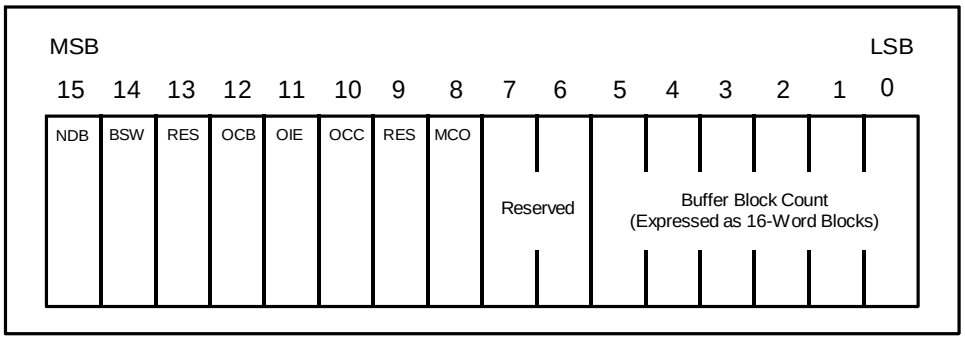


Figure 5-4 Header Word

Bit 15 New Data Bit (NDB)

Set to '1' by microcode to indicate new data recorded. Set to '0' by software after data is read to indicate buffer is available for message receipt.

Bit 14 Buffer Switch Interrupt Enable (BSW)

Set to '1' by software to generate an interrupt when switching from current buffer to next buffer.
Set to '0' by software to disable interrupt.

Bit 13 Reserved

Bit 12 Overwrite Current Buffer (OCB)

Set to '1' by software to allow overwrite. Reset to '0' by software to prevent overwrite. The Overwrite Buffer Bit is not restricted to use with single buffer message blocks. If the New Data Bit is set in the next buffer and the Overwrite Current Buffer Bit is set in this buffer, the data is written into this buffer.

Bit 11	Overwrite Interrupt Enable (OIE) Set to ‘1’ by software to enable interrupt. Set to ‘0’ by software to disable interrupt.
Bit 10	Overwrite Condition Occurred (OCC) Reset to ‘0’ by software initially and set to ‘1’ by microcode when an overwrite condition occurs.
Bit 9	Reserved
Bit 8	Missed Data Condition Occurred (MCO) Set to ‘0’ by software initially and set to ‘1’ by microcode when missed data occurs. If the overwrite Current Buffer is not set and the new data bit in the next buffer is set, then data is not stored and this bit is set in this buffer.
Bits 7-6	Reserved
Bits 5-0	Buffer Word Count (0-63) Multiply this number by 16 to get actual buffer size.

5.6 Message Record

When a message is monitored, it is stored in a message record (Figure 5-5). Each message will be stored in its own message record. There can be many message records in one message buffer, depending on the length of the buffer. A word of the message followed by its tag word alternates until the message is finished.

Reserved
Start of Message
ELT (MSW)
ELT (LSW)
First Word Of Message
Tag Word
Second Word of Message
Tag Word
Third Word of Message
Tag Word
• • •
Last Word Of Message
Tag Word

Figure 5-5 Message Record Format

The words of a message will vary depending on the message types. For example:

Message Type	First Word of Message	Second Word of Message	Third Word. Of Message	Fourth Word of Message
BC - RT	Receive Cmd.	Data Word 1	Data Word 2	- - -
RT - BC	Transmit Cmd.	Status Word	Data Word 1	- - -
RT - RT	Receive Cmd.	Transmit Cmd.	Transmit Status Word	Data Word 1
Mode (no data)	Mode Cmd.	Status Word	0000 *hex*	
Transmit Mode (data)	Mode Cmd.	Status Word	Data Word	

START OF MESSAGE WORD

Microcode stores the hex word CODE, indicating this is the start of the message.

ELAPSED TIMER WORD ELT (MSW)

The most-significant 16 bits of the elapsed timer.

ELAPSED TIMER WORD ELT (LSW)

The least-significant 16 bits of the elapsed timer are stored next.

TAG WORD

Figure 5-6 shows the format of the tag word.

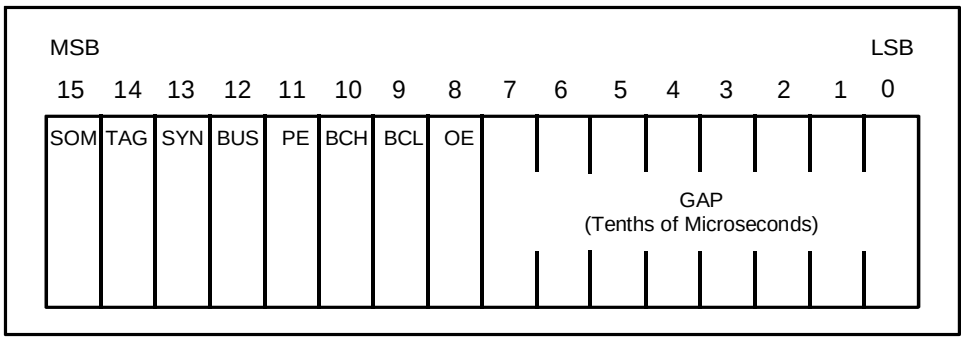


Figure 5-6 Tag Word

Bit 15 Start of Message (SOM)
Bit 15 is set if this is the first word of the message.

Bit 14 Tag (TAG)
Bit 14 is set in every tag word, including start of message tag.

Bit 13 Sync of Word (SYN)
Bit 13 is set if command or status word and reset if data word.

Bit 12 Data Received From Bus (BUS)
Bit 12 is set if tag word appeared on Bus A and reset if tag word appeared on Bus B.

Bit 11 Parity Error (PE)
Bit 11 is set if parity error appeared in this word.

Bit 10 Bit Count High(BCH)
Bit 10 is set if bit count high error occurred in this word.

Bit 9	Bit Count Low (BCL) Bit 9 is set if bit count low error occurred in this word.
Bit 8	Other Error (OE) Bit 8 is set if another error (sync, bi-phase, etc.) occurs in this word.
Bits 7-0	Gap Time (±200 nanoseconds) Expressed as tenths of microseconds (e.g., if value = 34 *hex* or 52 decimal, gap time = 5.2 microseconds).

5.6.1 Split Message Records

When a complete message record cannot be stored in a single message buffer, it will be split between the current message buffer and the next one in the linked list. Figure 5-7 shows an example of how this is done.

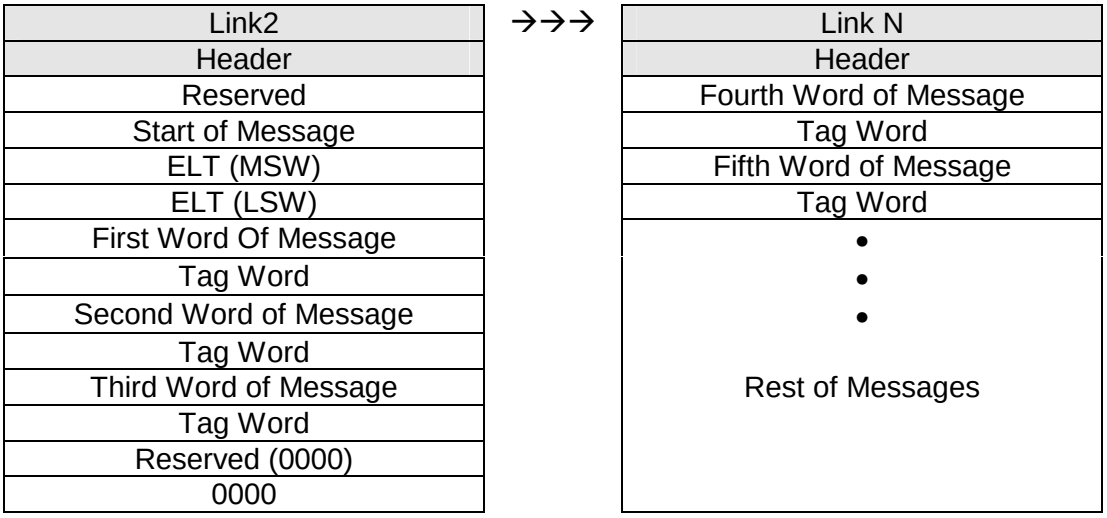


Figure 5-7 Split Message Record

5.7 Buffer Switching

Link2
Header
•
•
•
Reserved
Start of Message
ELT (MSW)
ELT (LSW)
First Word Of Message
Tag Word
Second Word of Message
Tag Word
•
•
•
Last Word Of Message
Tag Word
Reserved (0000)
0000
•
•
•
Less than 10 Words

→→→

Link N
Header
Reserved
Start of Message)
Start of Message (0xC0DE)
ELT (MSW)
ELT (LSW)
First Word Of Message
Tag Word
Second Word of Message
Tag Word
•
•
•
Last Word Of Message
Tag Word
Reserved (0000)
0000
•
•
•
Rest of Buffer

Figure 5-8 Message Record Storage With Buffer Switch Alignment

If fewer than ten words appear in the message record buffer (eight words for storing 1553 information and two reserved words at the end of the buffer), the microcode will switch buffers and store the complete message in the next message buffer. (Figure 5-8).

The message record ends with a reserved word, followed by a word of zeroes. These two words serve as an end-of-buffer indicator. If there are more than ten words left in the buffer, these words are overwritten by the next message record. If no more messages are captured, the end-of-buffer indicator signals the end of monitored information in this buffer.

As each word of the 1553 message and its tag word are stored in the buffer, the end-of-buffer indicator is written after the tag word; however, when the next word of the message is stored with its tag word, the end-of-buffer indicator is overwritten and a new end-of-buffer indicator is written after the tag.

If during receipt of a message the end of a buffer is reached, then the microcode automatically switches buffers and continues the message storage after the buffer-header word. (Figure 5-8).



NOTE: In Chronological Monitor mode the start of a command signals the microcode to begin storage of a record. This involves writing the first four words of a record (reserved, start of message, ELT MSW, ELT LSW) in preparation for the 1553 command word. If the monitor is not to store the message (SA is disabled for monitoring), then the end of buffer words will have been overwritten.

To avoid confusion, enable all RT Subaddresses when using monitor mode. This will also give a more accurate record of the 1553 bus activity for off-line data analysis.

6. 0 INTERRUPTS

6.1 Overview

Table 6-1 lists the GLD-PC/S interrupt types and identifies the operational modes upon which the interrupts may be enabled.

Table 6-1 GLD-PC/S Interrupts

Event	Mode
Protocol Error	MRT/BC
Buffer Overflow	MRT/BC
Mode Code	MRT/BC
Receive Transfer	MRT/BC
Transmit Transfer	MRT/BC
Monitor Buffer Switch	CM
Snapshot	CM
Asynchronous Halt	BC
Instruction Complete	BC
Halt	BC
Status Exception	BC

When an interrupt occurs, the board generates an interrupt packet and places it at the bottom of the interrupt queue (Table 6-2). Read the Interrupt Queue Control Real-Time Control Register 1409 *hex* to determine the beginning of the linked list from which to de-queue interrupts. Once the application software reads this pointer it must write a '0' to the Interrupt Queue Control Real-Time Control Register 1409 *hex*. This instructs the microcode not to add interrupt packets to the linked list under process and to start a new list.

The trailer word is used to determine the modes and events that generated the packet. If the interrupt queue is filled, the Queue Full Bit is set in the Trailer Word and no more interrupts are stored in the queue. When existing packets are processed by the application software a '0' must be written to the Valid Interrupt Word in each packet to return the packet to the queue.



NOTE: A hardware interrupt is only generated when the Microcode writes the address of a valid interrupt packet to the Interrupt Queue Control Register 1409 *hex*.

6.2 Interrupt Packet

The GLD-PC/S will add packets to the interrupt queue without generating a hardware interrupt, as long as the Interrupt Queue Control Register has a non-zero value (indicating the software has not begun processing interrupt packets).

Table 6-2 Interrupt Packet

Word	Definition	Notes
0	Reserved Link or '0'	
1	Receive Command	
2	Transmit Command	
3	Transmit Data Buffer Address	
4	Transmit Status or Mode Code Receive Data Word	
5	Receive Status or mode Code Transmit Data Word	
6	Receive Error Word or Receive Data Buffer Address	→ Reserved for transmit mode codes and if monitoring only
7	Bus Controller Instruction Address	→ BC mode only; all others reserved
8	Buffer Switch Monitor Address	→ Monitor mode only; all others reserved
9	Command Word Address Pointer	→ Monitor mode snapshot pointer; all others reserved
10	Trailer Word	
11	Valid (FFFF)	
12	Reserved	
13	Reserved	

Word 0 **Reserved**

Word 1 **1553 Receive Command Word**

If the message doesn't contain a Receive Command Word, a value of FFFF is written to this word.

Word 2 **1553 Transmit Command Word**

If the message doesn't contain a Transmit Command Word, a value of FFFF is written to this word.

Word 3 **Transmit Data Buffer Address**

Contains the address of the first word of the transmit buffer. A value of FFFF indicates that this word is unused.

Word 4 **1553 Transmit Status or Mode Code Receive Data Word**

Stores a 1553 status word if one exists. If this message is a Mode Code 17 (Sync with Data), this is the data sent to the RT. If there is no Transmit Status word and this message is not a Mode Code 17, the value FFFF is stored in this word.

Word 5 **1553 Receive Status or Mode Code Transmit Data Word**

Stores a 1553 receive status word or the data word received from a Mode Code transfer.

Word 6 **Receive Error Word or Data Buffer**

Address points to Word 1 of Receive Data Buffer or Receive Error Word, if an error was detected. A value of FFFF indicates this word is unused. The value is reserved for all transmit Mode Codes.

MRT Receive Error Word

Bit 15 No Response

Bit 15 is set if the RT detects an error in data reception and does not respond with its status.

Bit 14 Word Count High

Actual word count exceeds command word count.

Bit 13 Word Count Low

Actual word count is less than command word count.

Bit 12 Wrong Sync

The 1553 receive logic expected a sync other than what was received.

Bit 11 Wrong Bus

A word has been received on the opposite bus from the command.

Bit 10 Manchester Error

A Manchester or parity error has occurred on the message received.

Bit 9 Mode of Operation

If Bit 9 is set, the receiver is the BC. If clear the receiver is an emulated RT.

Bit 8 Buffer Overflow

Indicates that a buffer-overflow condition occurred and the Interrupt Overflow Error Bit was set in the receiving Message Block header. See description of overwrite current buffer bit (header Bit 12) in message block header. For details, refer to Section 3, Bus Controller Mode, Message Block Structure section, Header Word 1 definition.

Bit 7-0 Reserved

BC Receive Error Word

Bit 15 No Response

Bit 15 is set if the RT detects an error in data reception and does not respond with its status.

Bit 14 Word Count High

Actual word count exceeds command word count.

Bit 13 Word Count Low

Actual word count is less than command word count.

Bit 12 Wrong Sync

The 1553 receive logic expected a sync other than what was received.

Bit 11 Wrong Bus

A word has been received on the opposite bus from the command.

Bit 10 Manchester Error

A Manchester or parity error has occurred on the message received.

Bits 9-0 Reserved

Word 7 Bus Controller Instruction Address

If in BC mode, Word 7 points to Word 1 of the current four-word BC instruction. If not in BC mode, this word is reserved.

Word 8 Buffer Switch Monitor Address

If ten words or less remain in the current monitor buffer and the Buffer Switch Interrupt is enabled, a Buffer Switch Interrupt occurs during the last word to be stored. Word 8 points to the first word of the monitor buffer just filled.

Word 9 Command Word Address Pointer

If a Snapshot Interrupt is enabled for this command, Word 9 contains the address for the first Command Word of the transfer within the Monitor Buffer per the corresponding 1553 transfer.

Word 10 Trailer Word

As the last word in an interrupt packet (Figure 6-1), the Trailer Word defines valid interrupt types and sources for the corresponding 1553 message.

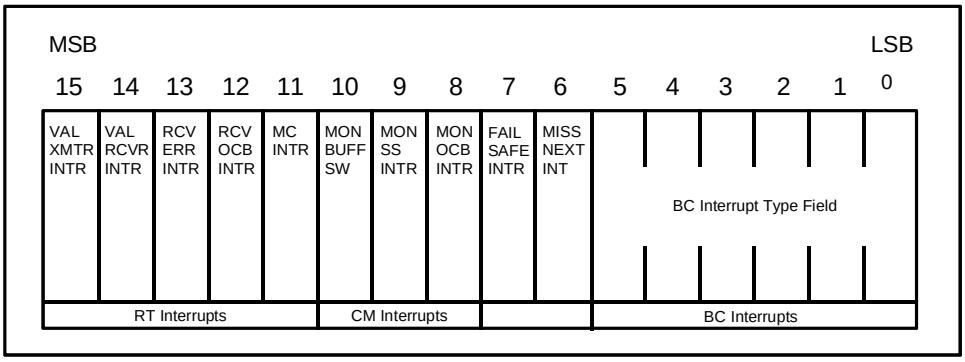


Figure 6-1 Trailer Word

MRT Interrupts (Bits 15-11)

If any of the interrupt bits are enabled in the Message Buffer Header or the Mode Interrupt is enabled in the Mode Code Response Word, the corresponding bit is set in the Trailer Word. The MRT Interrupts are defined below:

Bit 15 Valid Transmitter Interrupt

The transmit RT and SA were emulated for the transfer.

Bit 14 Valid Receiver Interrupt

The Receive RT and SA were emulated for the transfer.

Bit 13 Receiver Error Interrupt

The RT Mode detected an error on the received data.

Bit 12 Receiver Overwrite Current Buffer Interrupt

When Bit 12 is set, Bit 14 is never set. The emulated RT buffer had the Overwrite bit set and the New data bit was set in the buffer data was to be stored.

Bit 11 Mode Code Interrupt

The RT emulated the Mode Code transfer.

Bits 10-8 Monitor Interrupts

If any of the interrupt bits are enabled in the Monitor Buffer Header Word or any of the monitor interrupt bits are enabled in the Mode Code Response Word, the corresponding bit is set in the Trailer Word.

Bit 10 Monitor Buffer Switch Interrupt

A buffer switch occurred during this message.

Bit 9 Monitor Snapshot Interrupt

Posts the address of the Command Word for the corresponding message in the second to the last word of the packet. If the transfer was RT-to-RT, the address of the Transmit Command is written.

Bit 8 Monitor Overwrite Current Buffer Interrupt

Bits 7-0

Bit 7 Fail-safe Interrupt

Bit 7 is set if a continuous 1553 transmission of greater than 720 microseconds occurs causing a transmitter shutdown. Jumper JP13 must also be removed.

Bit 6 Miss Next Interrupt

1 = Interrupt queue overflowed after this block.
0 = No interrupt overflow occurred.

Bits 5-0 BC Interrupts

Bits 5-0 specify a six-bit field that displays the BC interrupt type in the *hex*adecimal format (Table 6-3).

Table 6-3 Bus Controller Interrupts

Hex Value	Interrupt Type
2	BC Mode Code Instruction Complete
3	BC Transfer Data
4	Instruction Complete (Includes Jump, HUE, etc.)
18	BC Overrun
6	BC Halt
8	Status Exception
10	Protocol Error
7	BC Transfer/Instruction Complete
B	BC Transfer/Status Exception
A	BC-MC/Status Exception
F	BC Transfer/Instruction Complete/Status Exception
C	Instruction Complete/Status Exception
14	Instruction Complete/Protocol Error
1F	BC Over/BC Transfer/Instruction Complete
2X	Asynchronous Halt/ etc.

Word 11 **Valid Interrupt (FFFF)**

Word 11 is set to a non-zero value when the GLD-PC/S adds the packet to the interrupt queue. The user's software must write a zero to this word when it has finished processing this packet.

Word 12 **Forward Link**

Reserved for microcode use.

Word 13 **Reverse Link**

Reserved for microcode use.

6.3 Algorithm for Interrupt Processing

To process interrupts, follow the steps outlined below:

1. Read the value of the Interrupt Control Register to a variable in your program.
2. Write a '0' to the Interrupt Control Register.
3. Process the packet (application dependent).
4. Read the Link Word in the packet.
5. Write a '0' to the Valid Interrupt Word to return the packet.
6. Repeat Steps 3 through 5 until the Link Word equals zero.
7. Re-enable system interrupts.

7. 0 REGISTERS

7.1 Overview

Three types of registers control GLD-PC/S operation: The I/O-mapped Initialization Registers, the Function Registers and the Real-Time Control Registers.

7.2 Initialization Registers

The Initialization Registers should be programmed at initialization. These registers are controlled by user I/O functions and must be mapped into the host I/O space.

Table 7-1 Initialization Registers

Register Number	Register Name	Access Method
19	Board Status/Amplitude	Read/Write
1A	Bit Test	Read/Write
1B	Memory Enable	Write
1F	Firmware Reset/Board Base	Read/Write

7.3 Board Status/Amplitude Register 19 *hex*

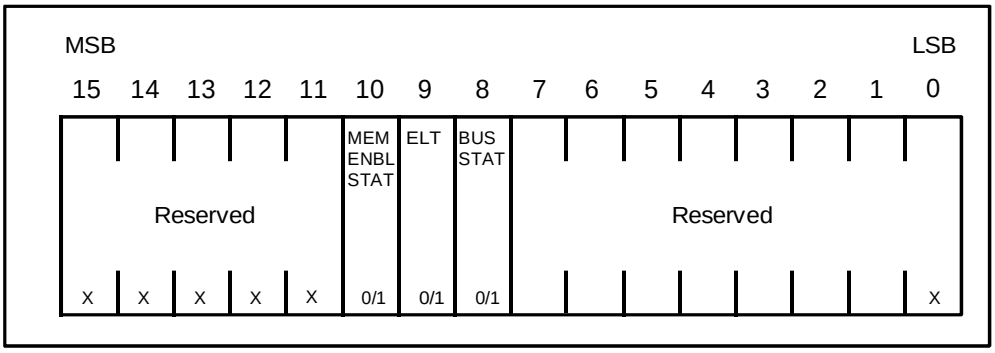


Figure 7-1 Board Status/Amplitude Register 19 *hex*

Bits 15-11 Reserved

Bit 10 Memory Enable Status Bit (MEM ENBL STAT) (Read-Only).
A value of 1 indicates memory is enabled.
A value of 0 indicates memory is disabled.

Bit 9 Elapsed Timer Enable (ELT ENBL) (Read Only).
A value of 0 indicates the ELT is enabled.
A value of 1 indicates the ELT is disabled.

Bit 8 Bus Status (BUS STAT) (Read Only).
A value of 0 indicates the 1553 bus is externally disconnected.
A value of 1 indicates the bus is externally connected.

Bits 7-0 Reserved

7.3.1 BIT Test Register 1A *hex*

A write to Register 1A *hex* disconnects the bus from the Bus A/Bus B connectors and selects the internal termination network. The internal termination network, built directly into the board, is used specifically to run this test program. A read to Register 1A *hex* connects the bus to the Bus A/Bus B connectors and disables the internal termination network. The status of Register 1A *hex* is displayed in Bit 8 of the Board Status/Amplitude Register 19 *hex*.

7.3.2 Memory Enable Register 1B *hex*

The write–only Memory Enable Register enables GLD-PC/S memory by setting Bit 0 of the register with a value of '1'. To disable memory access to the GLD-PC/S, reset Bit 0 by writing a '0'. At powerup, Bit 0 is reset so that the host does not allocate the board memory as system memory. The status of Register 1B *hex* is displayed in Bit 10 of the Board Status/Amplitude Register 19 *hex*.



NOTE: If the GLD-PC/S address is above the first megabyte of memory (extended memory), Bit 0 is automatically set and cannot be reset.

7.3.3 Firmware Reset/Board Base Register 1F *hex*

A write to Register 1F *hex* resets the on-board firmware. The reset must be performed initially after powerup. A read of Register 1F *hex* will return a value of CAFE *hex* signifying that the board has been based.

7.4 Real-Time Control Registers

The Real-Time Control registers, located in on-board memory, supply important information, such as operating mode status (Table 7-2). These registers can be accessed at any time (even when traffic exists on the 1553 bus) without degrading the performance of the GLD-PC/S boards. The memory base address for these registers is at offset 1400 *hex*.

To calculate the register address:

Channel Base Memory Address + (1400 *hex* + Register Number)

Table 7-2 Real-Time Control Registers

Memory Address	Register Name	Access Method
1400 *hex*	Alignment	READ
1401 *hex*	Board Type	READ
1402 *hex*	Firmware Version	READ
1403 *hex*	Master Control	READ/WRITE
1404 *hex*	Register Control	READ/WRITE
1405 *hex*	Register Value	WRITE
1406 *hex*	BCMRT Status	READ
1407 *hex*	Monitor Status	READ
1408 *hex*	Monitor Buffer Control	READ/WRITE
1409 *hex*	Interrupt Queue	READ/WRITE
140A *hex*	ELT HIWD	READ
140B *hex*	ELT LOWD	READ
140C *hex*	RT 0-15 Broadcast Enable	READ/WRITE
140F *hex*	RT 16-31 Broadcast Enable	READ

7.4.1 Alignment Register 1400 *hex*

When read, a value of 1553 *hex* is returned, indicating that the board has been successfully mapped.

7.4.2 Board Type Register 1401 *hex*

When read, a value of 4200 *hex* is returned which identifies the board type:

7.4.3 Firmware Version Register 1402 *hex*

When read, the current version of the on-board firmware is returned.
For example: 0A01 *hex* is version A1.



NOTE: The Master Control, Register Control and the Register Value registers are used to access the Function registers. (For more information on how to access the Function registers, see page 7-8.)

7.4.4 Master Control Register 1403 *hex*

This register acts as a safeguard against any unintentional accesses to the Function registers. A value of 1553 *hex* must be written to this address by the software prior to all

register accesses. If the 1553 *hex* value has been changed, access to any of the GLD-PC/S Function Registers is denied.

7.4.5 Register Control Register 1404 *hex*

The Register Control register identifies the Function register to be accessed and indicates when the access is in progress. The user software loads the function register offset into the Register Number Field (Bits 5-0) of this register and writes a '1' to Bit 15.

Bit 15	Register Access Pending Bit If the value is '1', a register access has been requested by the software or is in progress. The microcode examines Bits 5-0 of the Register Control register and performs the register function loaded by the user. When the register access is completed, the microcode clears this bit to allow another register access to occur.
Bits 14-6	Reserved
Bits 5-0	Register Number Field Bits 5-0 indicate the function register number to be accessed.

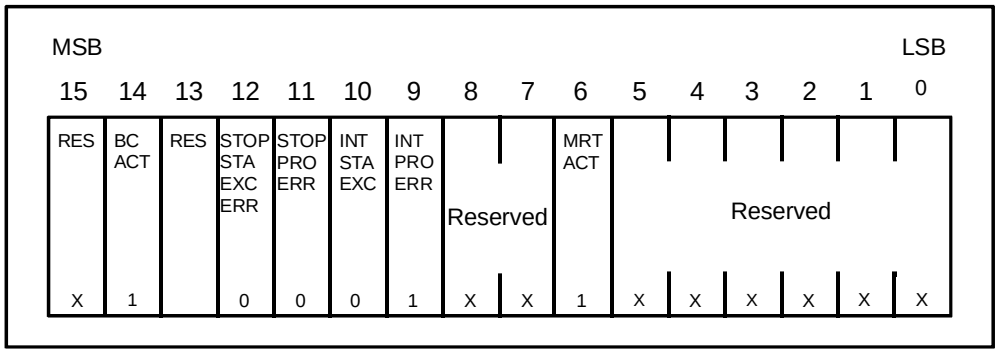
7.4.6 Register Value Register 1405 *hex*

This register contains the data value to be written into the register number specified in Bits 5-0 of the Register Control register 1404 *hex*.

7.4.7 BCMRT Status 1406 *hex*

Reading this register provides a view of the current operating modes and status of execution.

Table 7-3 BCMRT Status Real-Time Register



Bit 15 Reserved

Bit 14 BC Active (BC ACT)
If '1', the BC is active and executing buslist instructions. Bit 14 is reset by the firmware when the BC executes a HALT instruction or the user writes zeroes to the BC Control Register.

Bit 13 Reserved

Bit 12 Stop On Status Exception Error (STOP STA EXC ERR)
If '0', the BC stops if it receives a status response from an RT with any Bits 0-10 set.

Bit 11 Stop On Protocol Error (STOP PRO ERR)
If '0', the BC stops if it detects a protocol error.

Bit 10 Interrupt On Status Exception (INT STA EXC)
If '1', the BC generates an interrupt when it receives a status response from an RT with any Bits 0-10 set.

Bit 9 Interrupt On Protocol Error (INT PRO ERR)
If '1', the BC generates an interrupt when a protocol error is detected.

Bits 8, 7 Reserved

Bit 6 MRT Active (MRT ACT)
If '1', the MRT mode is activated. Bit 6 reflects accesses to the MRT Control Register and is reset by the firmware when the user writes zeroes to the MRT Control Register.

Bits 5-0 Reserved

7.4.8 Monitor Status Register 1407 *hex*

A read of this register returns the operational status of the Chronological Monitor. The possible values, set in the Chronological Monitor Control Register, are:

0008 *hex* - Monitor is active, will only capture all messages with valid commands.
0018 *hex* - Monitor is active, will capture all bus traffic.
0000 *hex* - Monitor is not active.

7.4.9 Monitor Buffer Control Register 1408 *hex*

When read, the starting memory address of the current monitor buffer is returned.

7.4.10 Interrupt Queue Control Register 1409 *hex*

When read, a '0' indicates the interrupt queue is empty. If the microcode writes any other value to this register, this value represents the address of the first packet to be processed by the software. Software writes a '0' to this register to notify microcode that processing of the queue has started.

7.4.11 ELT HIWD Register 140A *hex*

The ELT HIWD is loaded into this location after a value is written to the ELT Control Function Register 17 *hex* with bit 11 set to '1'.

7.4.12 ELT LOWD Register 140B *hex*

The ELT LOWD is loaded into this location after a value is written to the ELT Control Function Register 17 *hex*, with bit 11 set to '1'.

7.4.13 Broadcast Enable Registers (140C *hex*, 140F *hex*)

An RT is notified of broadcast commands if the RT is enabled and the bit corresponding to this RT is set in the appropriate Broadcast Notification Word. Two words of BIU memory, at memory addresses 140C *hex* (Figure 7-2) and 140F *hex* (Figure 7-3), indicate the RTs to be notified of broadcast messages.

To notify RTs 0, 5, 10, 15, 20, 25 and 30 of broadcast messages, the value of 8421 *hex* is loaded into BIU address 140C *hex* and 4210 *hex* is loaded into BIU address 140F *hex*. It is not necessary to set the bit corresponding to RT31.

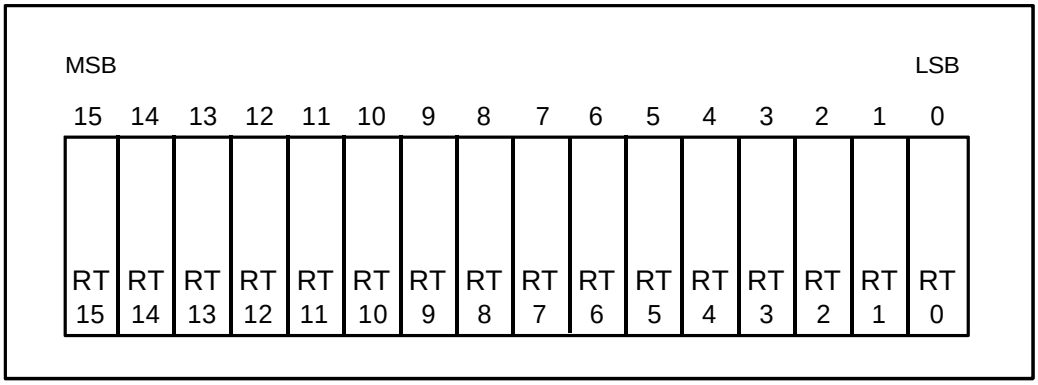


Figure 7-2 RT 0-15 Broadcast Enable Register 140C hex

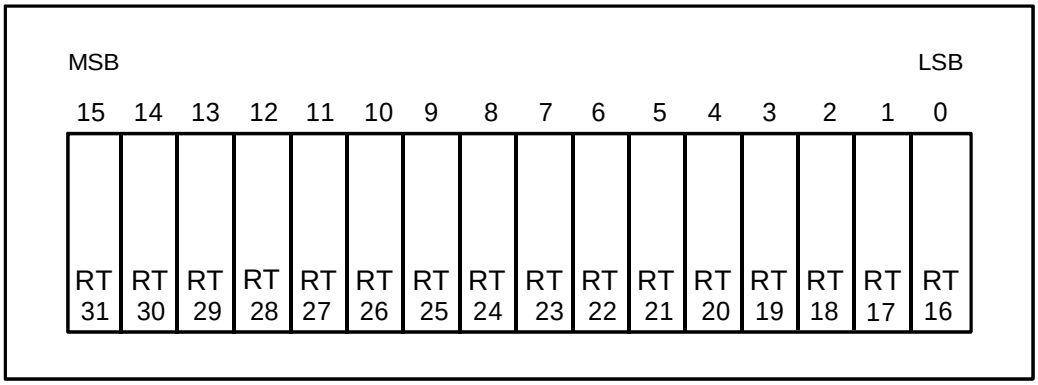


Figure 7-3 RT 16-31 Broadcast Enable Register 140F *hex*

To determine if an enabled RT is participating in the transmitted broadcast message, a Mode Code 2 (Transmit Last Status) or Mode Code 18 (Transmit Last Command) must be transmitted on the 1553 bus. If the specified RT used in the mode code is enabled for broadcast, the Broadcast Message Received (BRC) bit is set in the 1553 status response.

7.5 Function Registers

The Function registers control certain board functions, such as buslist execution. Accessing the Function Registers is controlled via the Real-Time Control registers 1403 *hex* through 1405 *hex*. The GLD-PC/S firmware accesses these registers when no traffic exists on the bus.



NOTE: None of the Function registers are readable. All read accesses are performed via the Real-Time Control registers located in memory starting at address 1400 *hex*.

Table 7-4 Function Registers

Register Number	Register Name	ACCESS METHOD
10	BC Control	WRITE
11	MRT Control	WRITE
12	Fail-safe Timer	WRITE
13	Gap Counter Control	WRITE
14	BC Error Control	WRITE
15	AND	WRITE
16	OR	WRITE
17	Elapsed Timer Control	WRITE
18	Chronological Monitor Control	WRITE
1C	Reset	WRITE
1D	Memory Address	WRITE

7.5.1 Writing to the Function Registers

To write to the Function registers:

If the Master Control register memory address 1403 *hex* contains the value 1553 *hex* and Bit 15 of the Register Control 1404 *hex* is set, wait for Bit 15 of the Register Control Register to be reset.

1. Write the value 1553 *hex* to the Master Control Register.
2. Write the value to be loaded into the desired Function Register into the Register Value Register 5 at memory address 1405 *hex*.
3. Write the desired Function Register number into Bits 5-0 and set Bit 15 of the Register Control Register 4 at memory address 1404 *hex*.
4. When Bit 15 of the Register Control Register 4 is reset by the onboard microcode, the operation has completed.

7.5.2 BC Control Register 10 *hex*

The write–only BC Control Register controls three functions. These are:

START

Load the address of the first buslist instruction to be executed. The offset cannot be less than 1440 *hex*, if the RTs are emulated.

HALT

To halt the buslist, write 0. The BC completes the current instruction, halts and generates an asynchronous halt interrupt, and does not update the instruction counter.

CONTINUE

To continue the buslist, write FFFF *hex*. The BC increments the instruction counter then starts the BC. The CONTINUE instruction can be used to restart the BC after asynchronous errors, exceptions or a HALT BC instruction. When evident that another buslist instruction will immediately follow the HALT instruction, the CONTINUE instruction restarts the BC.



NOTE: Writing to this register automatically resets and enables the BC elapsed timer. If using the external BC trigger, the timer is held reset until a trigger is received.

7.5.3 MRT Control Register 11 *hex*

The write–only MRT Control Register enables or disables the emulation of RTs for the MRT structures set up in memory.



NOTE: Initial MRT structures must be in place before the MRT is started.

After the MRT is started, RTs can be enabled or disabled by setting or clearing Bit 15 of the RT Status Block Control Word for the desired RT.

START MRT

To start the MRT, write a non-zero value.

HALT MRT

To halt the MRT, write a ‘0’.

7.5.4 Fail-safe Timer Register 12 *hex*

In the event of a runaway transmitter (continuously transmitting greater than 720 µsec) the GLD-PC/S activates a Fail-safe timer to disable the transmit circuitry and queue an interrupt to indicate the event. This write–only, Fail-safe Timer Register resets the Fail-safe Timer and enables both transmitters.

During simulation any write to the Fail-safe Timer Register resets the timer and re-enables both transmitters. Also, a hardware or software reset to the card has the same effect.

When a Transmitter Shutdown Interrupt occurs (that is, Bit 5 of the Trailer Word in the Interrupt Packet is set), a write to the Fail-safe Timer Register re-enables the transmitters.



NOTE: A word count high error greater than 32 words indicates a transmitter hardware failure. If the transmitter is not emulated on this channel, then register 12 should not be written for resetting. Register 12 should not be written to.

7.5.5 Gap Counter Control Register 13 *hex*

This register enables the BC to accept different response times other than the 1553 spec allows.

To use the Gap Counter Control Register:

- Determine the length of time the BC allows for the RT to respond. Calculated as tenths of microseconds. (14 µs = 140 ⅒ µs)
- Subtract this value from 256.
- Convert to hexadecimal.
- Load the new value into the Gap Counter Control Register.

EXAMPLE

To set the BC time-out to 18 microseconds, multiply 18 by 10 (to convert 18 to tenths of microseconds) and subtract the result from 256:

256 - 180 = 76 *Decimal*

Convert to hexadecimal:

76 *Decimal* = 4C *hex*

Write this value (4C *hex*) into the Gap Register.



NOTE: Since the time-out value is subtracted from 256, the maximum time-out is 25.6 ms.

7.5.6 BC Error Control Register 14 *hex*

The write–only BC Error Control Register (Figure 7-4) modifies BC reaction to 1553 errors. The BC may be set up to halt or interrupt for both status exception and protocol error events.

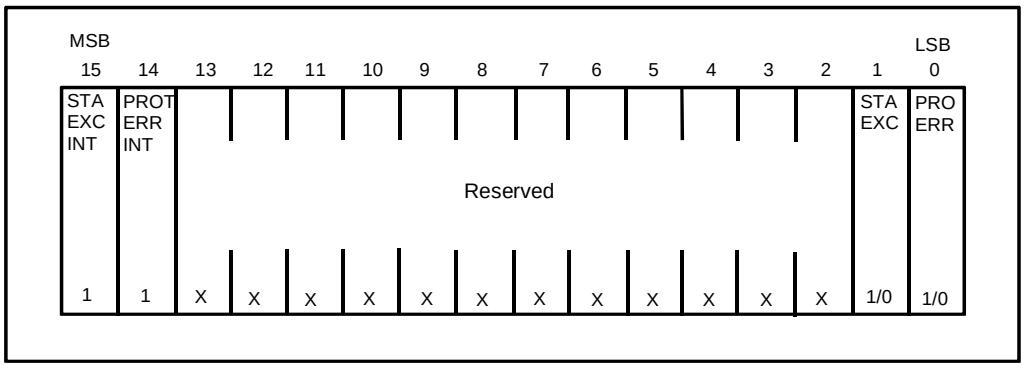


Figure 7-4 BC Error Control Register 14 *hex*

Bit 15 — Status Exception Interrupt (STA EXC INT)
If Bit 15 is set to ‘1’, an interrupt is posted when the BC encounters a Status Exception.

Bit 14 — Protocol Error Interrupt (PRO ERR INT)
If Bit 14 is set to ‘1’, an interrupt is posted when the BC encounters a protocol error.

Bits 13-2 — Reserved

Bit 1 — Status Exception (STA EXC)
If Bit 1 is set to ‘1’, the BC continues after a status exception is encountered. If Bit 1 is reset to ‘0’, the BC halts after a status exception is encountered.

Bit 0 — Protocol Error (PRO ERR)
If Bit 0 is set to ‘1’, the BC continues after a protocol error. If Bit 0 is reset to ‘0’, the BC halts after a protocol error occurs.

7.5.7 AND Register 15 *hex*

As a write-only register, Register 15 *hex* works together with the Memory Address register 1D *hex* to AND the value in register 15 *hex* with the value pointed to by the memory address contained in Register 1D *hex*. The GLD-PC/S modifies the Memory content after the AND value is written to this register.

EXAMPLE

Masking out the upper byte of a value using the AND Register 15 *hex*, AAAA ANDed with 00FF results in 00AA.

Operation	Address	Data
Write a value of AAAA *hex* into address 0528 *hex*.	Memory 0528 *hex*	AAAA *hex*
Write 0528 *hex* into Memory Address Register 1D *hex*.	Memory Address Register 1D *hex*	0528 *hex*
Write 00FF *hex* to the AND Register 15 *hex*.	AND Register 15 *hex*	00FF *hex*
Read back new data value.	Memory 0528 *hex*	00AA *hex*



NOTE: The AND/OR Registers provide compatibility with previous BIU products and are not used in most cases, since memory access via these registers takes five to ten times longer than a direct access to memory.

7.5.8 OR Register 16 *hex*

The OR Register works together with the Memory Address Register 1D *hex* to OR the value in Register 16 *hex* with the value pointed to by the memory address contained in Register 1D *hex*. Memory content is modified after the OR value is written to this register.

EXAMPLE

To set the upper byte of the value using the Register 16 *hex*, 00AA *hex* ORed with 5555 results in 55FF *hex*.

Operation	Address	Data
Write a value of 00AA *hex* to Memory Location 1359 *hex*.	Memory 1359 *hex*	00AA *hex*
Write 1359 to Memory Address Register 1D *hex*.	Memory Address Register 1D *hex*	1359 *hex*
Write 5555 to OR Register 16 *hex*.	OR Register 16 *hex*	5555 *hex*
Read back new data value.	Memory 1359 *hex*	55FF *hex*



NOTE: The AND/OR registers provide compatibility with previous BIU products and are not used in most cases, since memory access via these registers takes five to ten times longer than a direct access to memory

7.5.9 Elapsed Timer (ELT) Control Register 17 *hex*

The write-only ELT Control Register controls the 32-bit Elapsed Timer for BC and CM modes (Figure 7-5, Table 7-5). A write to Register 17 enables/disables the ELT, selects the external signal or internal clock source, resets the ELT and reads the ELT. (See the Real-Time Control Registers 140A *hex* and 140B *hex*.) The ELT contains a resolution of 1 microsecond. The ELTCLK (external clock) resolution is user-defined.

NOTE: Read the Real time control ELT STATE register to verify configuration before changing.

Table 7-5 Register 17 Values and Actions

Write Value	Action
0 *hex*	HALT and Reset the ELT
1000 *hex*	HALT the ELT
1800 *hex*	Read the ELT
2000 *hex*	Enable the external clock input
4000 *hex*	Enable and Reset the ELT
5000 *hex*	Enable the ELT

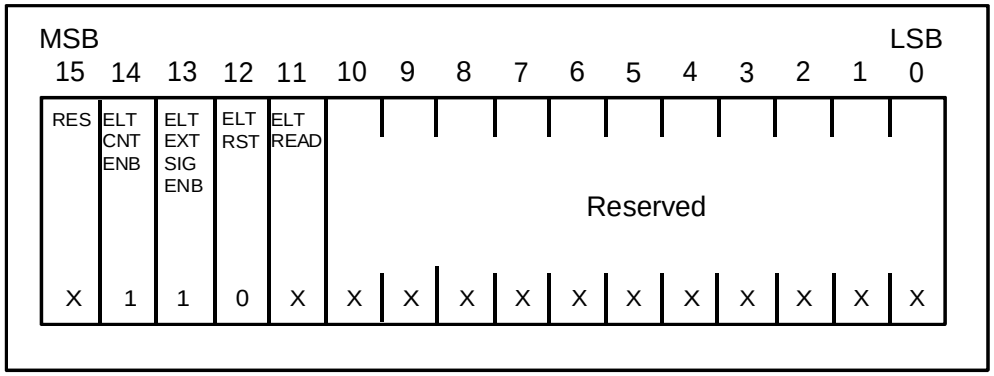


Figure 7-5 Elapsed Timer (ELT) Control Register 17 *hex*

Bit 15 Reserved

Bit 14 Elapsed Timer Count Enable (ELT CNT ENB)
When reset to '0' the Elapsed timer is halted.
Setting to '1' resumes count of Elapsed timer from the current value.

Bit 13 ELT External Signal Enable (ELT EXT SIG ENB)
Setting Bit 13 enables the external signal for the Elapsed Timer Clock.
Clearing Bit 13 selects the internal 1 MHz clock.

NOTE: The external clock may not exceed 1 MHz as unpredictable timing will occur.

Bit 12	Reset Elapsed Timer (RST ELT) When reset to ‘0’ clears the Elapsed Timer. Bit 12 must be set if writing to this register and no reset of the ELT is desired.
Bit 11	ELT Write Control (ELT read) When set to ‘1’, the ELT LOWD and ELT HIWD Real-Time Control Registers are loaded with the current ELT value.
Bits 10-0	Reserved

7.5.10 Chronological Monitor Control Register 18 *hex*

The Chronological Monitor Control Register starts and stops the monitor. The monitor is started by writing a value of '8' to this register.



NOTE: Before the monitor can be started, the address of the first monitor buffer must be loaded into the Real-Time Register at 1408 *hex*.

The monitor is stopped by writing a value of '0' to this register. Writing a value of 18 *hex* allows the monitor to record 1553 command words that may contain protocol errors and permits the capture of all bus traffic. If Bit 4 is not set, only messages with valid commands can be monitored.

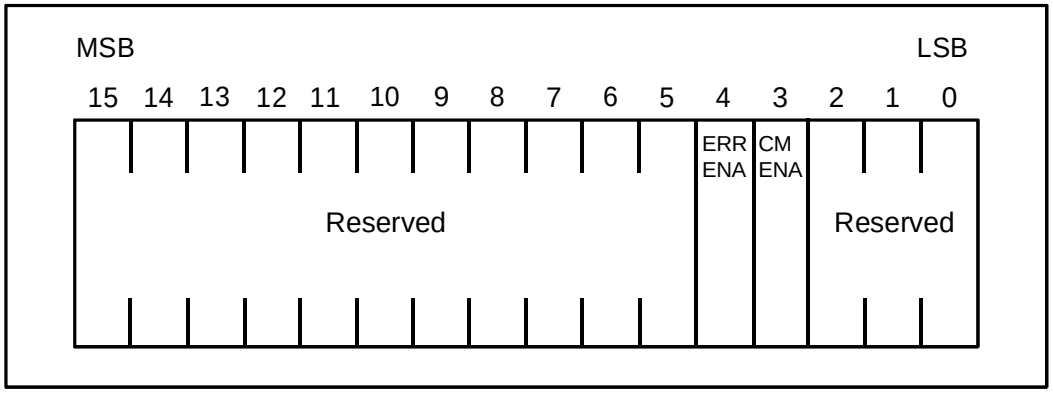


Figure 7-6 Chronological Monitor Control Register 18 *hex*

Bits 15-5	Reserved
Bit 4	Error Enable When set to '1' the CM will monitor all traffic. When reset to '0' the CM will only monitor messages with valid command words.
Bit 3	CM Start. When set to '1' the CM will start recording data in the buffer pointed to by the Real-Time Control Register 0-8 *hex*.
Bits 2-0	Reserved

7.5.11 Reset Register 1C *hex*

The Reset Register resets the GLD-PC/S, affecting only register data structures set up in the processor. All memory structures are left alone.

Resetting the GLD-PC/S:

- Halts BC, RT and CM operations
- Resets BC Error Control Register bits to their default values:
  - Stop on Protocol Error
  - Stop on Status Exception
  - Do not interrupt on Protocol Error
  - Do not interrupt on Status Exception
- Resets the Terminal Fail-safe Timer
- Ignores the remainder of a message in progress on the 1553 data bus
- Turns off any pending interrupts
- Resets the interrupt queue to 1200 *hex*

To perform a RESET, write any hexadecimal value (0 - FFFF).

7.5.12 Memory Address Register 1D *hex*

Use Register 1D *hex* to address memory and, in conjunction with the AND or the OR Register, to set or reset bits. The Memory Address Register contains the value of the address to be modified. Perform a write to Register 1D *hex* before performing the appropriate “AND” or “OR” function. For example usage, see the definitions for Function registers 15 *hex* (AND) and 16 *hex* (OR).

APPENDIX A
SPECIFICATIONS

A.1 Hardware Specifications

Hardware Compatibility:	MIL-STD-1553
System Minimum Recommended	PC-386, EISA/ISA (1EEE 996)
Physical Dimensions:	332.74 mm x 111.76 mm (full slot)
Electrical Requirements:	
Voltage	5 V + 5% @ 2.4 Amps
	+12 V + 5% @ .19 Amps
	-12 V + 5% @ .0125 Amps
Current Drain	3.6 amps (max.)
Temperature Range:	
Storage	-20° to 85° Celsius
Operation	0° to 55° Celsius
Humidity Range:	
Storage	0% to 95% (noncondensing)
Operation	10% to 90% (noncondensing)
Communication:	MIL-STD-1553A or B protocol
Data Size Supported:	Memory: D16 Registers: D16
Interface to Bus:	Transformer or direct coupling
Memory:	32 K words of Dual-Port RAM



NOTE: The GLD-PC/S board is designed to be memory-mapped in the first 1 MB of PC address space.

A.2 Board Dimensions

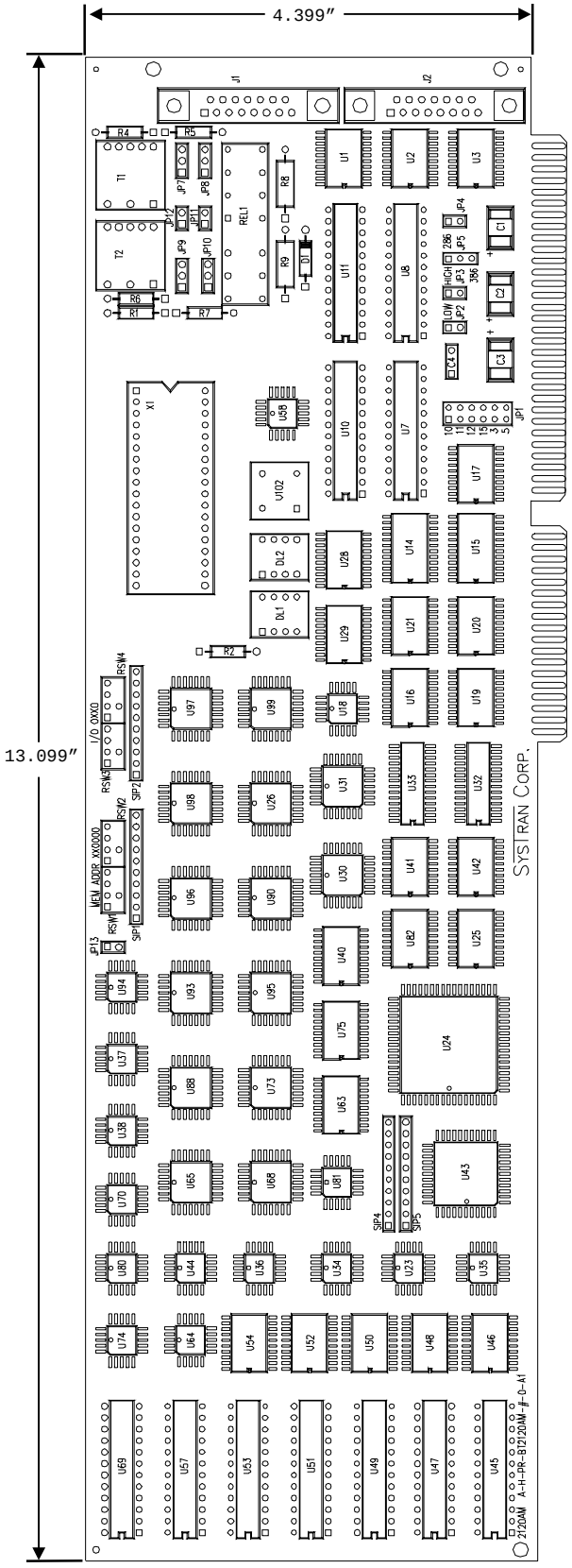


Figure A-1 GLD-PC/S Dimensions

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