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GLD-VME/R

User Manual Addendum

Document No. T-T-MU-GLXXVR##-A-0-A2

FOREWORD

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FCC

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CE

Please note: As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

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1.0 INTRODUCTION

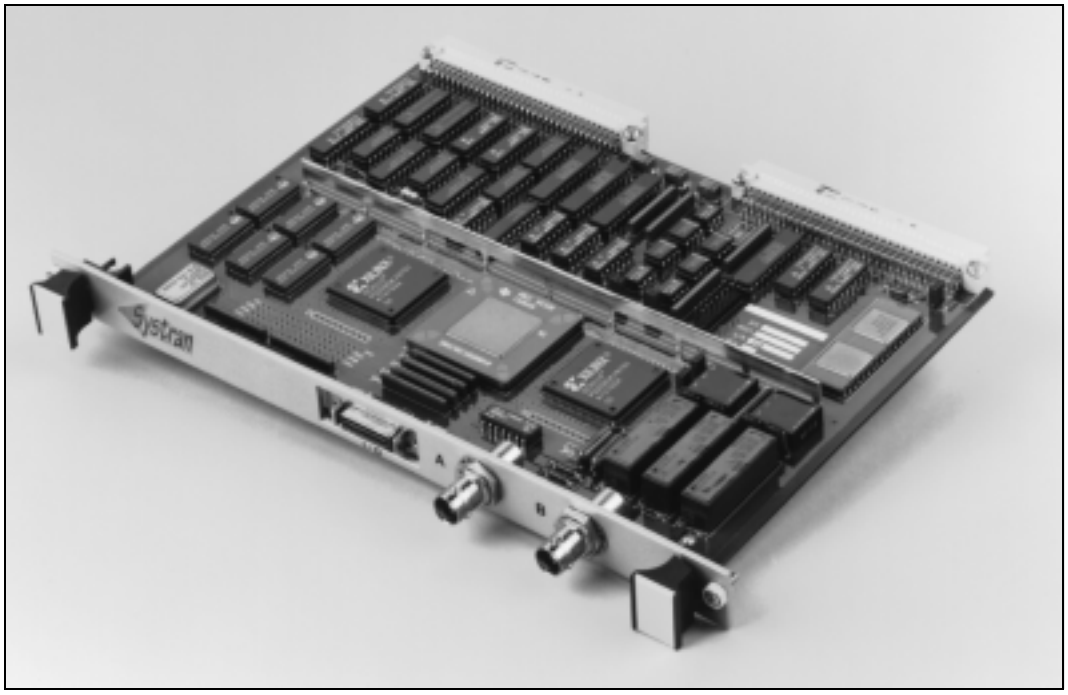


Figure 1-1 GLD-VME/R Board

The GLD-VME/R is fundamentally identical to a single-channel GLD-VME. It provides the same functionality and uses the same downloaded microcode. The ruggedization provides extended temperature operation to -40° to 80° C, moisture resistance, and extended shock and vibration handling characteristics.

The GLD-VME/R is physically different from the GLD-VME due in large part to the different selection of components. Extended temperature components were required, resulting in the use of many DIP components instead of the commercial grade SOIC packages used on the GLD-VME. Population of components allows the GLD-VME/R to act as a slave board in a VME system in a manner identical to the GLD-VME.

There are three fundamental differences between the GLD-VME and the GLD-VME/R:

- The rotary switches used to set the base I/O address are replaced with I/O jumpers that may be wire-wrapped, solder-jumpered, or shunted by the end user to set the base I/O address. This is required because the rotary switches are operational only over a commercial temperature range.
- The RS-422 discrete signal interface has been brought out to the front panel for easier access by users that incorporate this feature in designs.
- The P2 connector pins used for back-panel 1553 connections have been modified.

Any reference in the GLD-VME user manual to the second channel of a dual-channel board may be ignored.



NOTE: The GLD-VME/R is shipped from the factory using jumper shunts to select the base I/O address, fail-safe timer enable, and 1553 front-panel or back-panel connection. This permits the easiest modification of these selections according to the requirements of the end user. Jumper shunts, as shipped, will not necessarily perform up to the rated shock and vibration characteristics of the board. It is suggested that the end user use wire-wrap wire or a hard-soldered connection to specify the I/O address, fail-safe timer selection, and 1553 front or back panel connection

The documentation on the following pages replaces the corresponding sections of the GLD-VME user manual.

2.0 GETTING STARTED

2.1 Overview

Replace the corresponding paragraphs in the GLD-VME User manual with the following:

2.2 Set the Hardware Switches

There are three sets of four jumper blocks near the front panel labeled RSW1, RSW2, and RSW3. Each group of bits represents a hexadecimal digit in the base I/O address of the board in a A16 address space, with RSW1 being the most significant part.

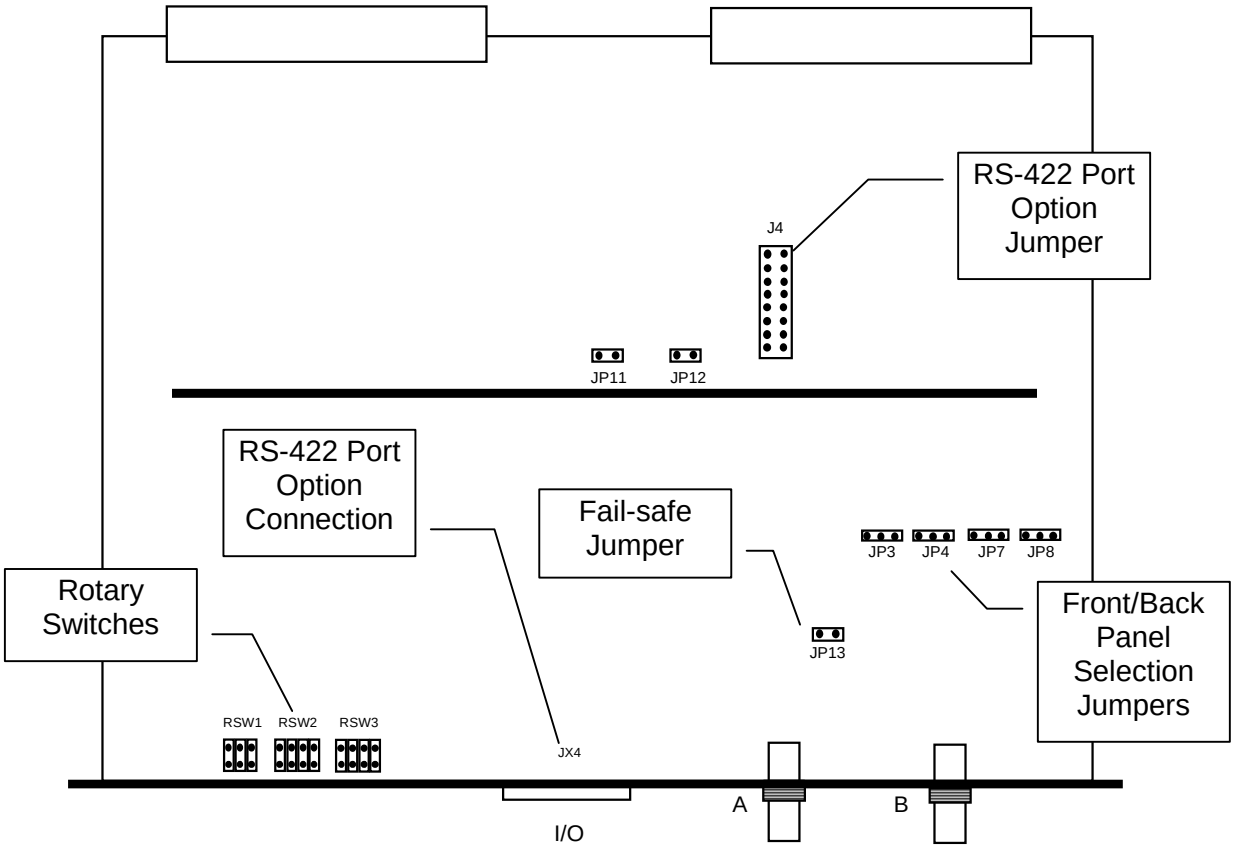


Figure 2-1 GLD-VME/R Connector and Jumper Locations

With the board in the orientation shown above, the most significant bit of each digit is on the left. The left-most bit of RSW1 represents the most significant bit of the A16 address space for register I/O access. When jumpered, a bit represents a logic zero; when left open, a bit represents a logic one.

EXAMPLE

To set the I/O address to 1580 *hex*, the following jumpers must be installed:

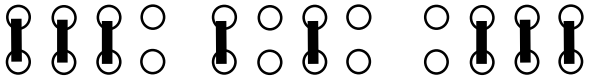


Figure 2-2 I/O Address 1580 *hex* Example

NOTE: The I/O address must be on an even 40-byte boundary.

NOTE: The GLD-VME/R is shipped with a factory-set I/O base address of 1000 *hex*. The end user may modify the jumper shunts, wire wrap, or solder across the RSW jumpers to set a required I/O address.

2.3 Locate the Fail-safe Timer Jumpers

Leaving jumper JP13 open enables the fail-safe timer which allows an interrupt to be generated after 720 µs of continuous bus operation. Installing jumper JP13 disables the fail-safe timer.

NOTE: The GLD-VME/R is shipped from the factory with the fail-safe timer enabled. The end user may modify the jumper shunt, wire wrap, or solder across the jumper to disable the fail-safe timer.

2.4 Locate the Connectors

FRONT PANEL CONNECTORS

The GLD-VME/R contains two standard triax jacks that connect the board to the 1553 data bus. With the board horizontal and the front panel facing the front, the Bus A connection is to the left and the Bus B connection is to the right.

BACK PANEL CONNECTORS

The GLD-VME/R is available with optional P2 1553 connections. Table 2-1 provides P2 connection information.

Table 2-1 P2 1553 Connector

Connector	Output	Routing Jumper
Bus A+	P2 Pin A8	JP3
Bus A-	P2 Pin C8	JP4
Bus B+	P2 Pin A13	JP7
Bus B-	P2 Pin C13	JP8

FRONT OR BACK PANEL 1553 SELECTION

The routing of the 1553 bus signals is selected via jumpers as indicated in column three of Table 2-1 and as shown in Figure 2-1. For all jumpers, connecting pins 1 and 2 select front-panel connection. Connecting pins 2 and 3 selects back-panel connection. Pin 1 is indicated by the square solder pad.



NOTE: The GLD-VME/R is shipped from the factory with front-panel connection selected. The end user may modify the jumper shunts, wire wrap, or solder across the 1553 selection jumpers as required.

2.11 Using the RS422 Port Option

The GLD-VME/R comes equipped with an RS422 port (J4, JX4). Jumper J4 is a 16-pin jumper block on the board. JX4 is a 26-pin D-style sub-miniature connector accessible from the front panel. Table 2-2 indicates pin assignments.

Table 2-2 RS422 Port Pin Assignments

Description	J4 Pin	JX4 Pin
ELT RST + Elapsed Timer Reset	1	10
ELT RST - Elapsed Timer Reset	2	11
EXT ELT CLK + External Elapsed Timer Clock	3	7
EXT ELT CLK - External Elapsed Timer Clock	4	8
DOS + Discrete Output Signal	5	24
DOS - Discrete Output Signal	6	3
NC No Connection	7 - 16	1, 2, 4 - 6, 9, 12 - 23, 25, 26



NOTE: Do not drive a pin designated as having no connection (NC.)

The orientation of connector J4 is shown in Figure 2-3. The layout is from the component side of the board.

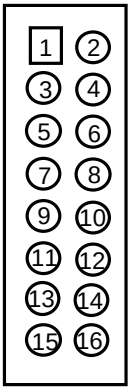


Figure 2-3 J4 Connector Pin Description

The pin description for connector JX4 is shown in Figure 2-4.

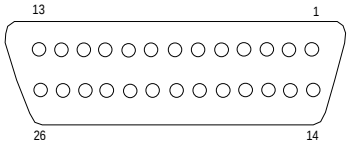


Figure 2-4 JX4 Connector Pin Description

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