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DIO316I

Tristateable 48-Channel
Digital I/O Board Hardware Reference

Document No. B-T-MR-DIO316I#-A-0-A5

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's tristateable, 48-channel Digital I/O board, referred to in this document as DIO316I (part number BHAS-DIO316I).

1.1.2 Scope

This reference manual covers the physical and operational description of the DIO316I, both from hardware and software perspectives. This manual also contains detailed technical information about the DIO316I's performance characteristics, and some typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2              file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)
- ANSI/VITA 4-1995 published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA. Phone: 480-951-8866, FAX: 480-951-0720, E-mail: info@vita.com, URL: www.vita.com
- Systran Corporation: www.systran.com

1.3 Quality Assurance

Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments (including software), contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

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- Fax: **(937) 252-1349**
- World Wide Web address: www.systran.com

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2. PRODUCT OVERVIEW

2.1 Overview

The DIO316I is a singlewide IP Module board, implementing a general-purpose digital I/O interface conforming both mechanically and electrically to ANSI/VITA 4-1995 specification.

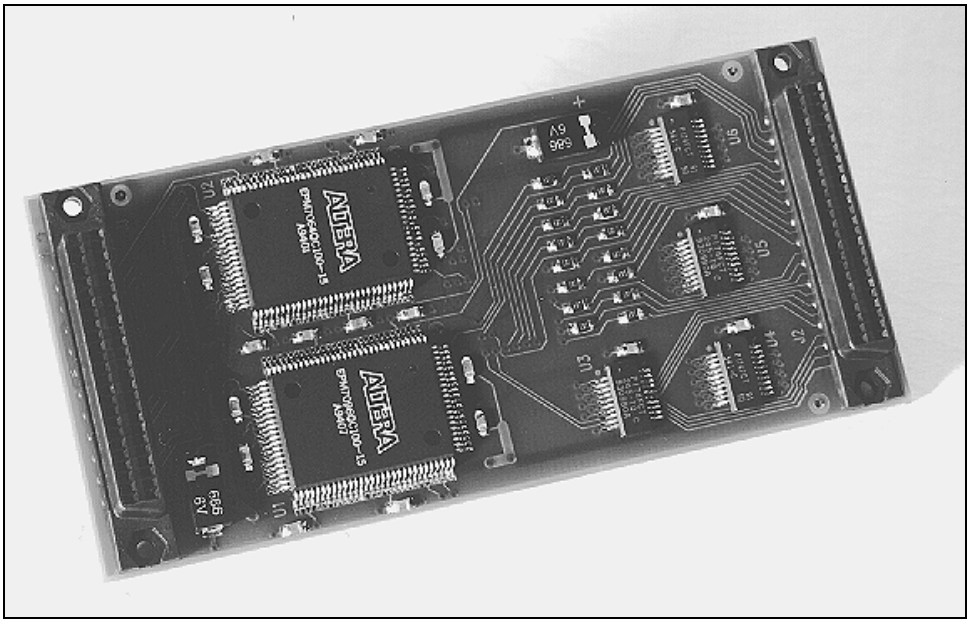


Figure 2-1 DIO316I, Version A1

2.2 Features

- Two bi-directional octal ports, two octal output ports, and two octal input ports.
- Software controllable low/high impedance states for the bi-directional and output ports.
- Configurable basic functionality for 32 outputs/16 inputs, 16 outputs/32 inputs, or 24 outputs/24 inputs; definable to Rising or Falling Edges, High or Low Levels, or On-change, for digital logic I/O applications.
- TTL-compatible port drivers, with source and sink ratings per channel at -5 mA and 64 mA, respectively.

2.3 Related Product

- Software: 'C' library and OS-9 device-driver routines and documentation.
- Windows NT 4.0 library software with documentation.

2.4 Block Diagram Description

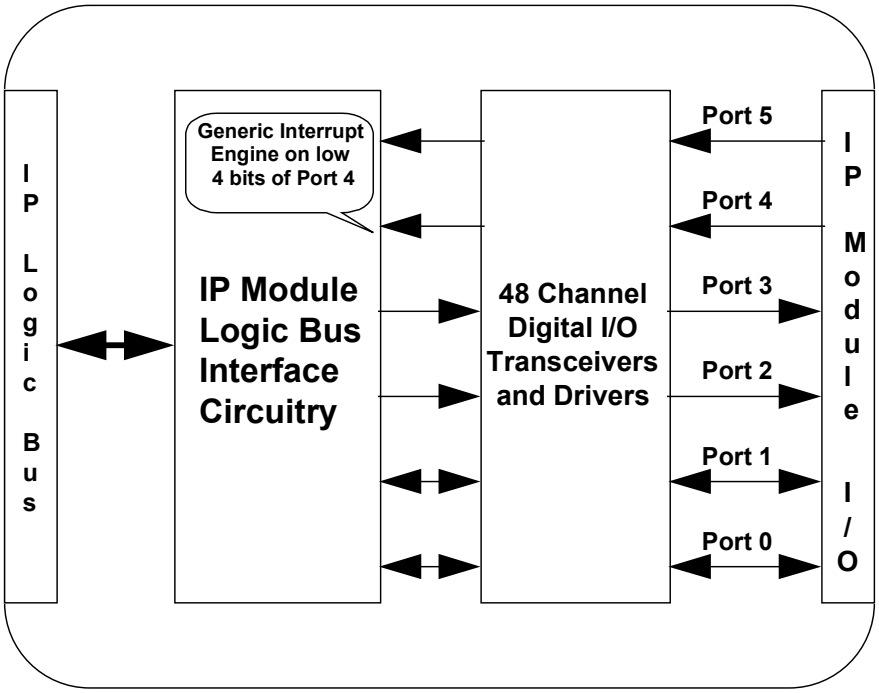


Figure 2-1 DIO316I Block Diagram

Figure 2-1 is a simplified block diagram of the DIO316I representing the signal flow between the IP Module Logic Bus and I/O connectors.

On the left side of the diagram is the IP Module's Logic Bus connector through which all transfers between the IP Module carrier and the DIO316I's registers and data sources are conducted.

The block labeled "IP Module Logic Bus Interface Circuitry" contains all of the write/read registers and ports, ID PROM data, control/status registers, interrupt vector, interrupt control/status registers and interrupt engine, and IP Module sequence/control and data bus interface logic.

The block labeled "48 Channel Digital I/O Transceivers and Drivers" contains the 74FCT components, implemented with individual QSOP-packaged logic.

On the right side of the block diagram is the DIO316I's I/O connector, providing source/sink currents and input limiters for all 48 digital lines, and a ground reference.

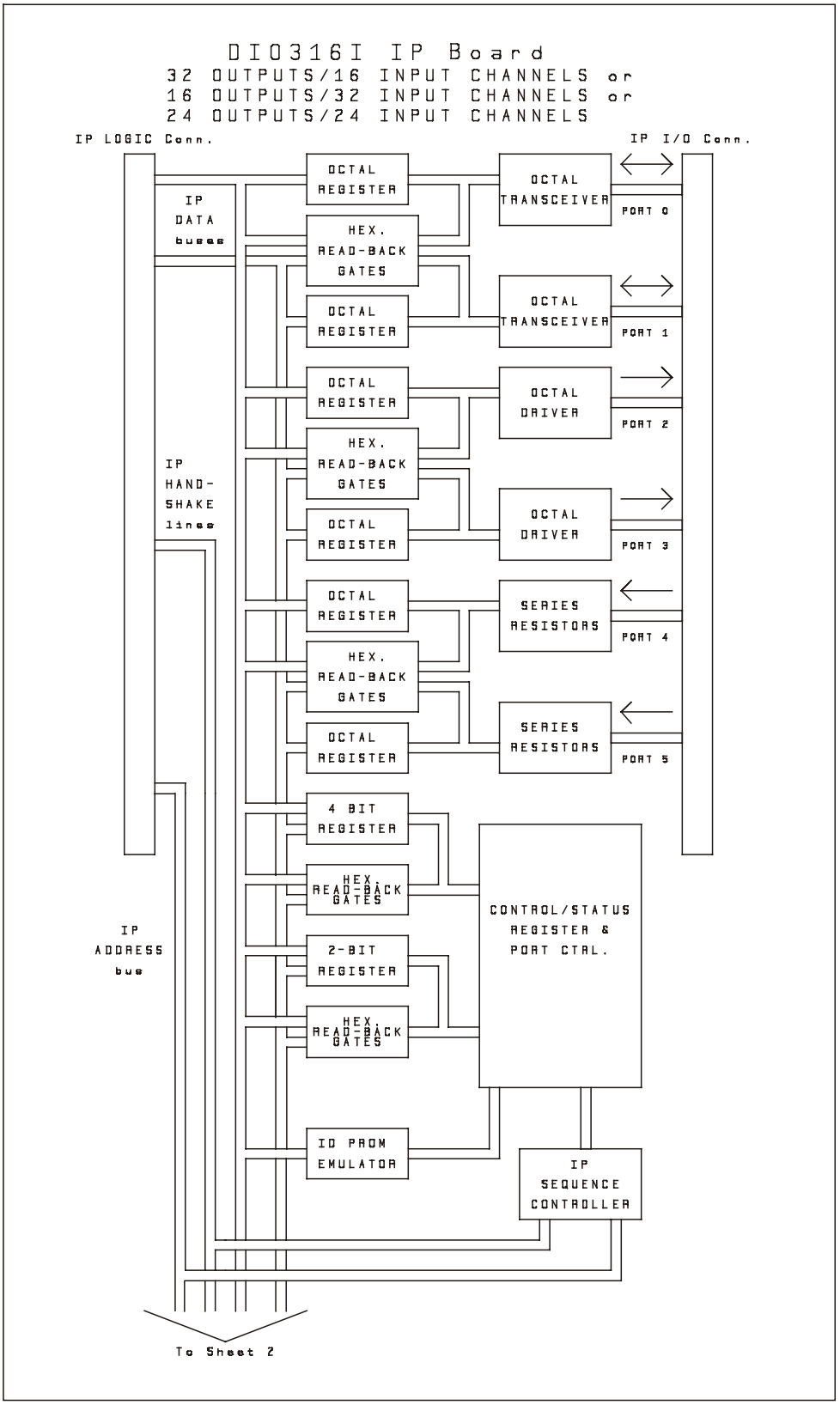


Figure 2-2 Block Diagram (Part 1)

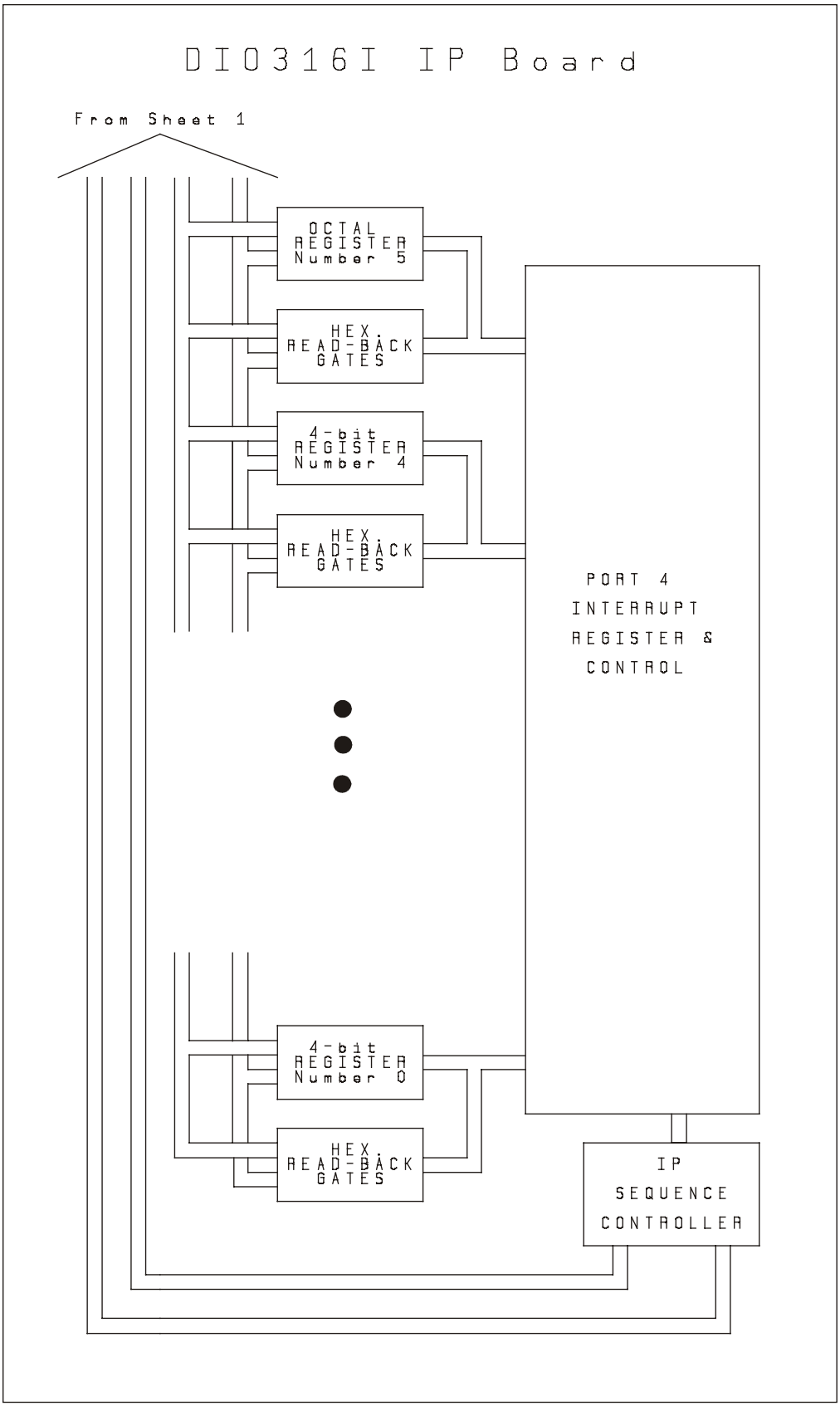


Figure 2-3 Block Diagram (Part 2)

Figure 2-2 and Figure 2-3 present a detailed block diagram of the DIO316I. The IP Logic Bus connector through which all host carrier transfers take place is on the left side. The six 8-bit data ports are paired into three 16-bit registers or "words". Each register contains two 8-bit ports or bytes, and a 16-bit tristateable gate for driving the IP Data bus (IPDbus) during I/O reads.

Ports 0 and 1 are either two 8-bit ports or one 16-bit transceiver register called Data Register 0. Ports 2 and 3 are directly connected to digital 74FCT541's as two 8-bit or one 16-bit output register called Data Register 1. Ports 4 and 5 are directly connected to the internal registers as two 8-bit ports or one 16-bit input register called Data Register 2. This architecture supports byte writes to either octal register, or a "word" write to both. All I/O port reads are performed only at the "word" width of 16 bits.

The IPDbus interface to the control registers is similar to that of the data ports, but lacks the octal data ports' interface. The registers' primary functions are maintenance of the TRI-STATE conditions for ports 0, 1, 2 and 3, and the direction of ports 0 and 1.

The port 4 interrupt control/status registers have a similar IP Module carrier interface, lacking the octal data ports' interface, except bits [3:0] of port 4. The register's only function is maintenance of the interrupt engine.

The ID PROM Emulator is the circuitry that presents the proper data patterns to the lower 8 bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers. Emulating the (never-changing) ID information in this way reduces parts count and costs, and increases system reliability with its associated Mean Time Between Failures (MTBF) value.

The blocks labeled "IP Sequence Controller" contain all of the control logic for performing orderly transfers between the DIO316I and its carrier. The power-up default logic for this board is included in this section.

2.5 Theory of Operation

The DIO316I was developed using VHDL and synthesis, targeted to an Altera EPLD, schematic-captured and integrated to standard logic devices, connectors and discrete components using Viewdraw by VIEWlogic and associated tools.

2.6 Components and Functions

2.6.1 Byte-Lane 0 Controller

The byte-lane 0 controllers provide all of the IP Module control and interface operations for the lower eight bits ([7:0]) of the 16 IP Module-Data-Bus bits (IPD[15:0]). These operations include the following:

- Registering the control registers
- Registering the interrupt control/status registers
- Emulating the ID PROM data fields for registering and driving three of the user's six 8-bit data ports.

The data ports are defined as I/O (or bi-directional) for port 0, output-only for port 2, and input-only for port 4. The byte-lane 0 controller also has a generic interrupt engine operating on the lowest four bits [3:0] of port 4.

2.6.2 Byte-Lane 1 Controller

The byte-lane 1 controller provides all of the IP Module control and interface operations for the higher eight bits ([15:8]) of the 16 IP Module Data Bus bits (IPD[15:0]). These operations include registering and driving three of the user's six 8-bit data ports. The data ports are defined as I/O (or bi-directional) port 1, output-only port 3, and input-only port 5.

2.6.3 Transceivers And Buffer/Line Drivers

The 74FCT245 transceivers and 74FCT541 buffer/line drivers provide the TRI-STATE isolation and the TTL-compatible source and sink current capabilities that are external to the Altera devices for ports 0 through 3.

2.6.4 Current-Limiting Protection

The 10 KΩ series resistors (R1-R16) on ports 4 and 5 provide extra current-limiting protection against electrostatic discharge/over voltage conditions beyond what is already in the Altera devices' input circuitry.

2.7 Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol.



CAUTION: Do NOT use gasoline or thinner solvents on this product.

3. INSTALLATION

3.1 Unpack the DIO316I

The contents of the DIO316I shipping packages are listed in Table 3-1:

Table 3-1 Contents of DIO316I Shipping Packages

Qty	Description
1	DIO316I Printed Circuit Assembly
1	DIO316I Hardware Reference *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number. (For example, BTMR-DIO316I).

3.2 Inspect the DIO316I

Examine the DIO316I to determine if any damage occurred during shipping.

3.3 Install the DIO316I



NOTE: The DIO316I is an Electrostatic Sensitive Device (ESD). Install the DIO316I on an anti-static workbench using good ESD practices to protect the IP Module and the host carrier boards.

The tools required for the DIO316I installation are listed in Table 3-2.

Table 3-2 DIO316I Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat-Head Screwdriver (Optional)

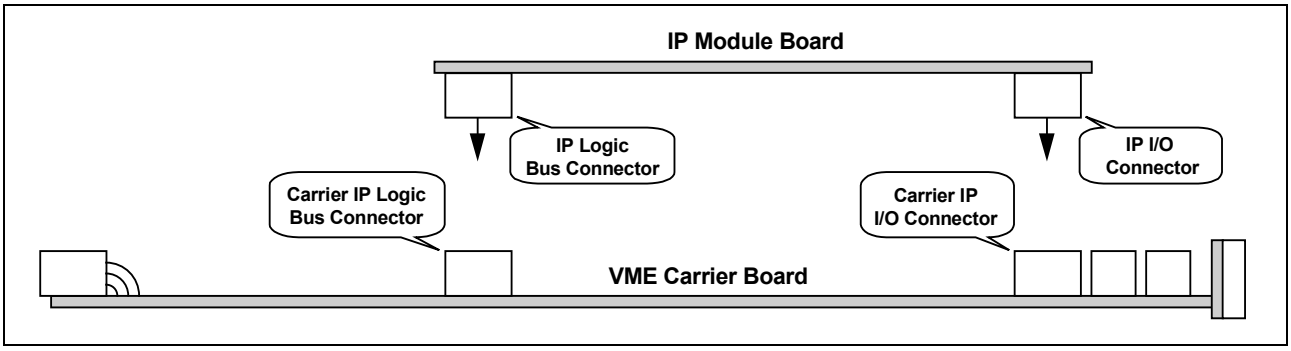


Figure 3-1 DIO316I Installed on a VME IP Module Carrier

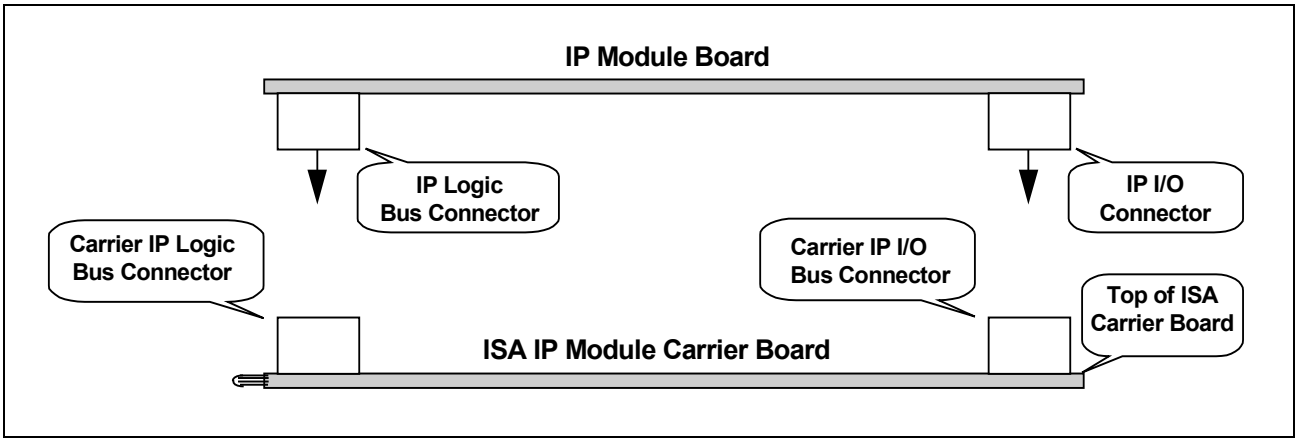


Figure 3-2 DIO316I Installed on an ISA IP Module Carrier

Figures 3-1 and 3-2 show the DIO316I installed on a VME IP Module carrier and on an ISA carrier, respectively.

The pin assignments for the IP Logic Bus connector are shown in Table 3-3. The signals in the left column are the original IP Module signal nomenclature, and the signals in the right column are those used by Systran Corp.

Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module carrier board User Manual for more information.

Referring to the appropriate figures and table described above, perform the following steps to install the DIO316I. The asterisk (*) denotes optional items.

1. Turn OFF all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD-controlled area where the DIO316I can be installed.
3. Remove the DIO316I from the shipping package and place it on the ESD bench.
4. Install the DIO316I onto the carrier board by applying adequate and equal pressure to the DIO316I board at both ends.
5. * Install four M2x5 mm flat-head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the DIO316I to the carrier board.

Table 3-3 IP Logic Bus Pin Assignments

Original IP Signal Names	IP Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP I/O Connector Pin Assignments

IP I/O Pin #	Signal Names
50	GND
49	No Connection
48	Port 5 Bit 0
47	Port 5 Bit 1
46	Port 5 Bit 2
45	Port 5 Bit 3
44	Port 5 Bit 4
43	Port 5 Bit 5
42	Port 5 Bit 6
41	Port 5 Bit 7
40	Port 4 Bit 0
39	Port 4 Bit 1
38	Port 4 Bit 2
37	Port 4 Bit 3
36	Port 4 Bit 4
35	Port 4 Bit 5
34	Port 4 Bit 6
33	Port 4 Bit 7
32	Port 3 Bit 0
31	Port 3 Bit 1
30	Port 3 Bit 2
29	Port 3 Bit 3
28	Port 3 Bit 4
27	Port 3 Bit 5
26	Port 3 Bit 6
25	Port 3 Bit 7
24	Port 2 Bit 0
23	Port 2 Bit 1
22	Port 2 Bit 2
21	Port 2 Bit 3
20	Port 2 Bit 4
19	Port 2 Bit 5
18	Port 2 Bit 6
17	Port 2 Bit 7
16	Port 1 Bit 0
15	Port 1 Bit 1
14	Port 1 Bit 2
13	Port 1 Bit 3
12	Port 1 Bit 4
11	Port 1 Bit 5
10	Port 1 Bit 6
9	Port 1 Bit 7
8	Port 0 Bit 0
7	Port 0 Bit 1
6	Port 0 Bit 2
5	Port 0 Bit 3
4	Port 0 Bit 4
3	Port 0 Bit 5
2	Port 0 Bit 6
1	Port 0 Bit 7

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4. PERFORMANCE

4.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Appendix A. The figures in this section are a collection of typical rise/fall, and board response times to various system stimuli and IP Module cycles.

4.2 Timing Measurements

Timing measurements were conducted on the DIO316I using an HP model 16500A Logic Analyzer with a 400 megasamples per second Digitizing Oscilloscope Module, model 16531A, plugged into slot E, and a 1 GHz Timing Master Module, model 16515A in slot C. The DIO316I was installed in the IP Module slot 'A' of a Motorola MVME-162-23 VME processor IP Module carrier board. Figure 4-1 shows the test configuration for the oscilloscope measurements, and Figure 4-2 shows the configuration for state timing measurements.

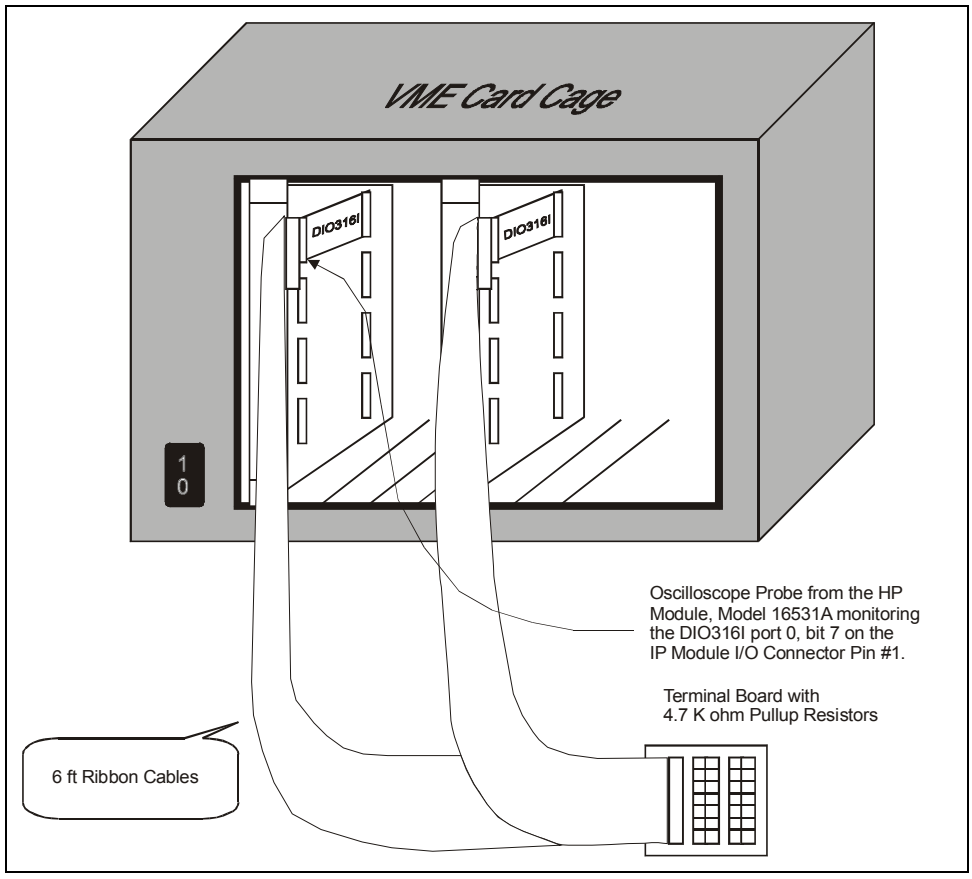


Figure 4-1 Test Configuration for the Oscilloscope Measurements

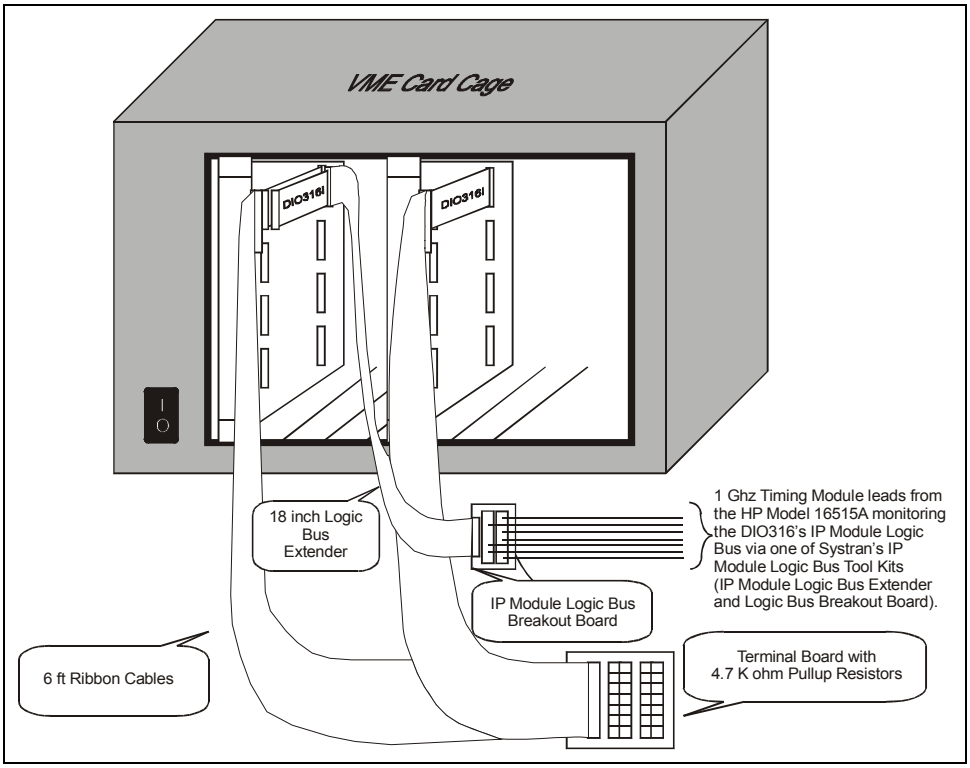


Figure 4-2 Test Configurations for the State Timing Measurements

4.3 Oscilloscope Measurements

For Figures 4-3 through 4-6, the measurements were made with the 400 MHz oscilloscope probe on Pin #1 of the DIO316I's I/O connector (which is port 0, bit 7). This output bit drives a load through six feet of standard 50-pin ribbon cable to a terminal board (with 4.7 K ohm pullup resistors to 5 Vdc) then back through another six-foot ribbon cable. Each figure indicates typical 90% through 10% ranges.

Figure 4-3 shows a typical digital output drive rise time (logic low to high, TPLH) in the 5½ nanosecond range.

Figure 4-4 shows a typical digital output drive fall time (logic high to low, TPHL) under 6 nanoseconds.

Figure 4-5 shows a typical digital output release time from a logic low to high impedance (TPLZ) rise time of about 400 nanoseconds, which is a function of the pullup resistors and the cable's load capacitance.

Figure 4-6 shows a typical digital output drive from a high impedance to a logic low (TPZL) fall time, which is again less than 6 nanoseconds, similar to the TPHL.

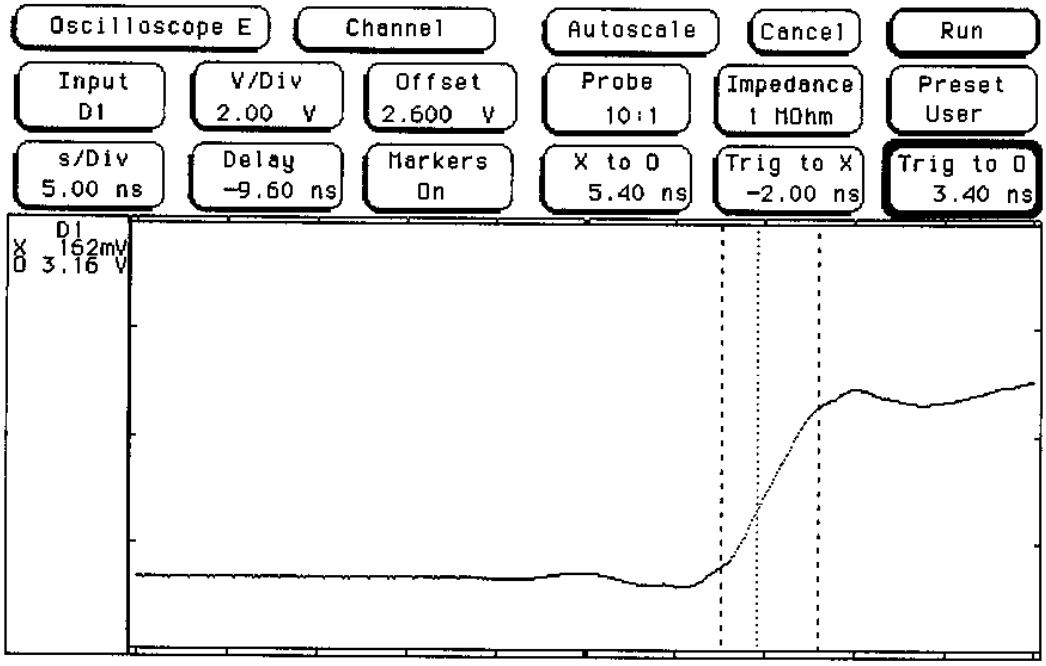


Figure 4-3 Typical Digital Output Drive Fall Time (Logic Low to High, TPLH)

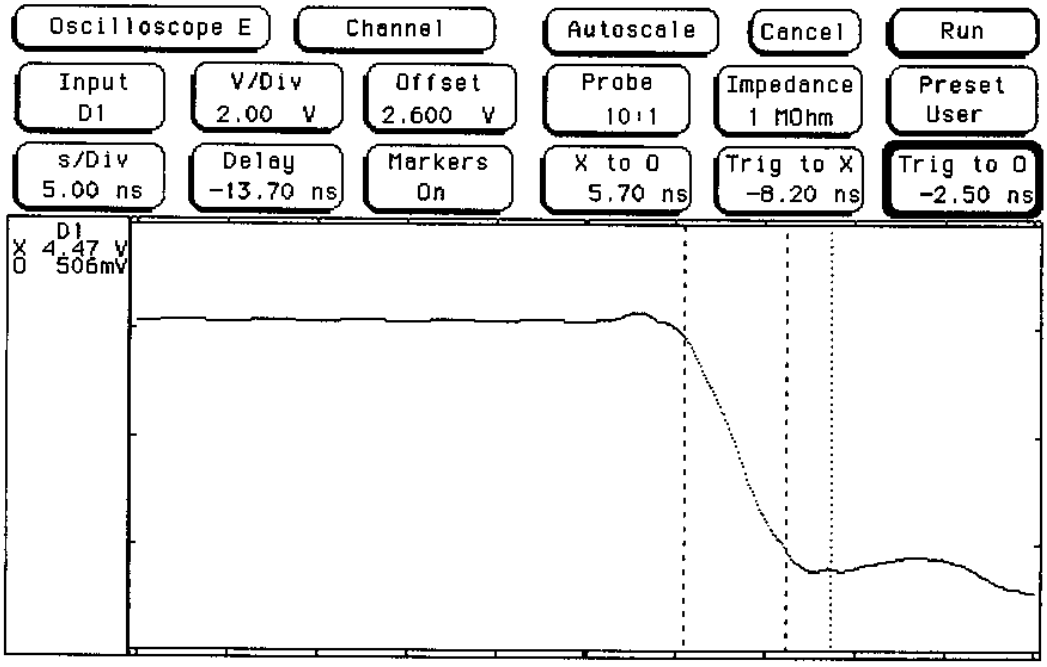


Figure 4-4 Typical Digital Output Drive Fall Time (Logic High to Low, TPHL)

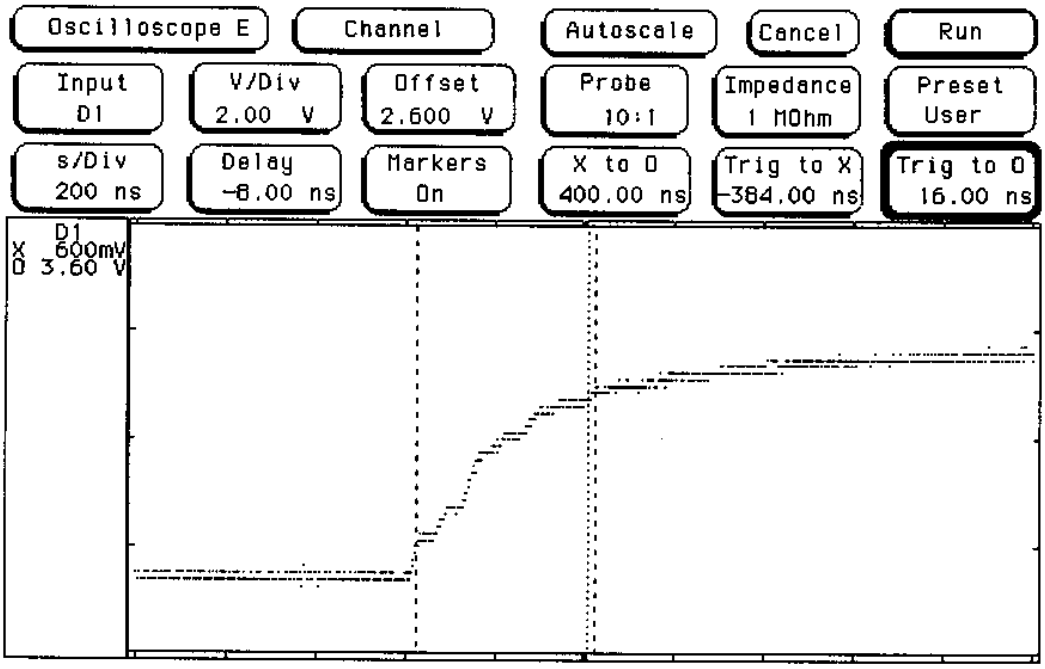


Figure 4-5 Typical Digital Output Release Time (Logic Low to High Impedance, TPLZ)

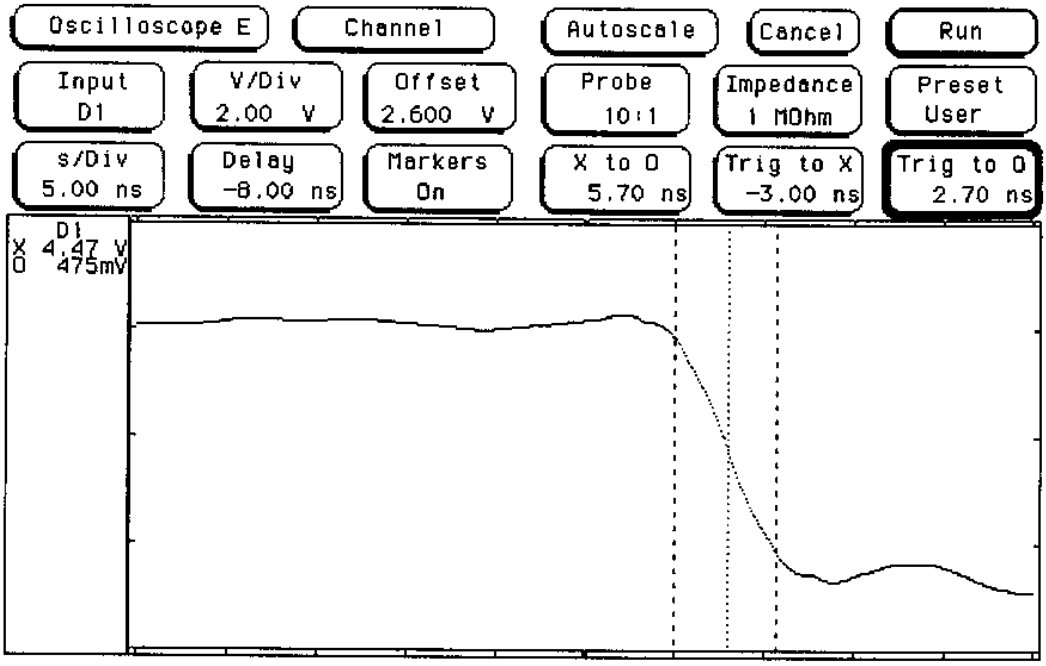


Figure 4-6 Typical Digital Output Drive (High Impedance to Logic Low,

4.4 State Timing Diagrams

The state waveforms shown in Figures 5-7 through 5-13 were made using the HP 1 GHz Timing Master Module and the Systran IP Logic Bus Extender (IPLBE) with the IP Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer‘s screen are active low, and are represented by a ‘/’ as the first character as opposed to the ‘N_’ used elsewhere, due to the limited amount of character spacing.

4.4.1 ID Read Cycle

Figure 4-7 is a complete DIO316I ID read cycle of IP Address 0x00. The signals of interest are /IDSEL, N_ACK, and the four IPD[3:0] signals. Figure 4-8 is a zoomed-in view of the DIO316I ID cycle driving the N_ACK and IPD[3:0] signals, showing a typical response time of less than 20 nanoseconds for driving these signals. The ANSI/ VITA 4-1995 Specification, page 65, requires these signals be driven within 40 nanoseconds of the rising edge of ICLK.

4.4.2 I/O Read Cycle

Figure 4-9 is a complete DIO316I I/O read cycle of IP Module Address 0x00. The signals of interest are /IOSEL, N_ACK, and the four IPD[3:0] signals.

Figure 4-10 is a zoomed-in view of the DIO316I IO read cycle driving the N_ACK and IPD[3:0] signals, showing a typical response time of less than 20 nanoseconds for driving these signals.

4.4.3 Interrupt Request

Figure 4-11 shows an interrupt request and a few microseconds later, an IP interrupt select cycle.

Figure 4-12 is a view of the DIO316I’s Interrupt Request signal (/INTRQ) being asserted 94 nanoseconds after the programmed event “Interrupt on port 4 bit 0 being a low level”, which is the P4B0IN signal label on the waveform diagram.



NOTE: Figure 4-12 is very important information for users concerned about system response time. Since the interrupt request signal is asserted by the DIO316I in less than 100 nanoseconds, the IP Module carrier board receives the interrupt request signal as fast as possible to begin its interrupt service routine.

4.4.4 Interrupt Select Cycle

Figure 4-13 is a view of a typical IP Interrupt Select Cycle, again with N_ACK and IPD[3:0] the signals of interest.

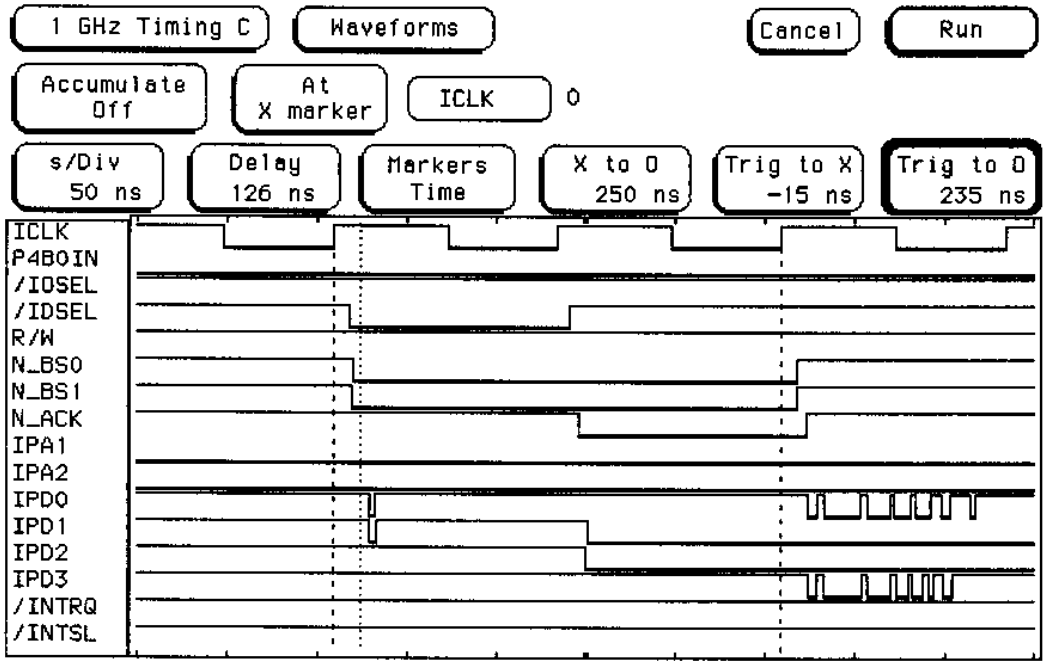


Figure 4-7 Complete DIO316I ID Read Cycle (IP Module Address 0x00)

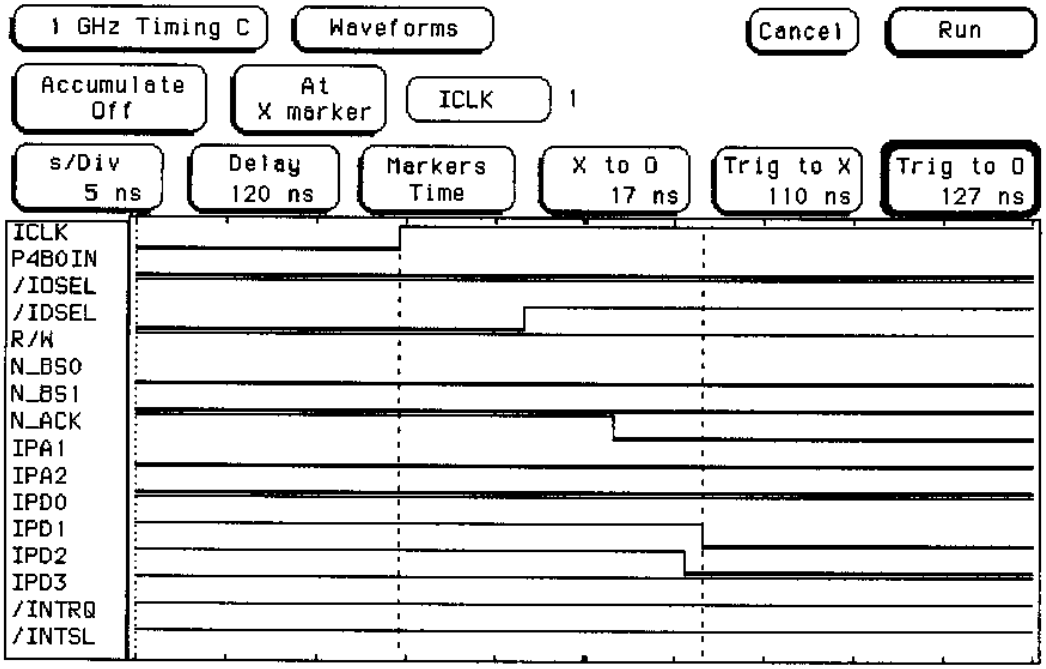


Figure 4-8 Zoomed-In View of DIO316I ID Cycle Driving N_ACK and IPD[3:0] Signals

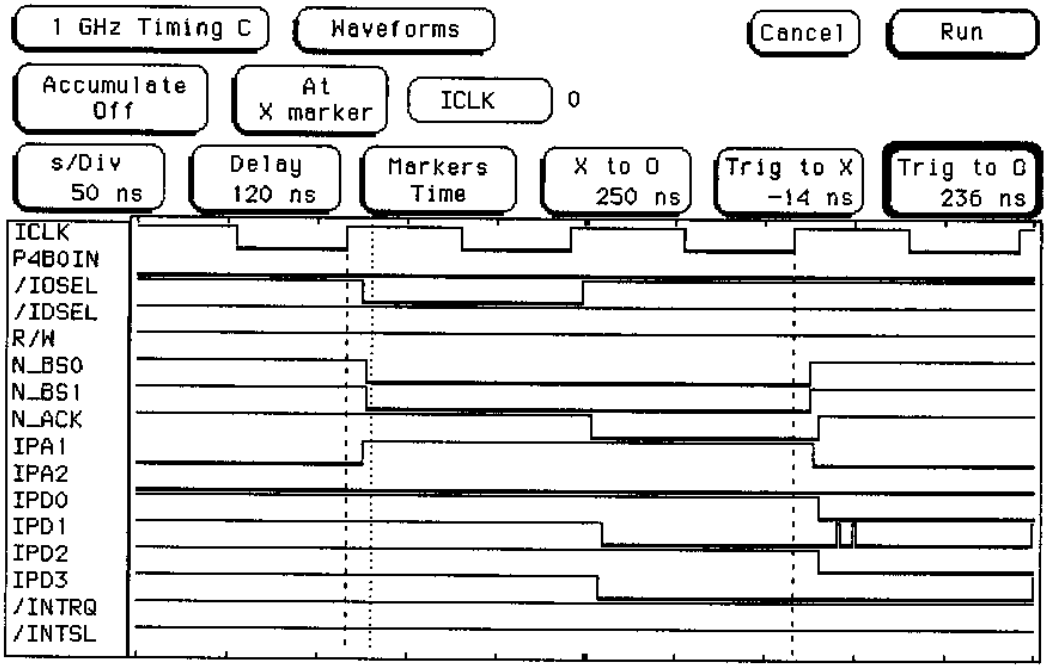


Figure 4-9 Complete DIO316I IO Read Cycle (IP Module Address 0x00)

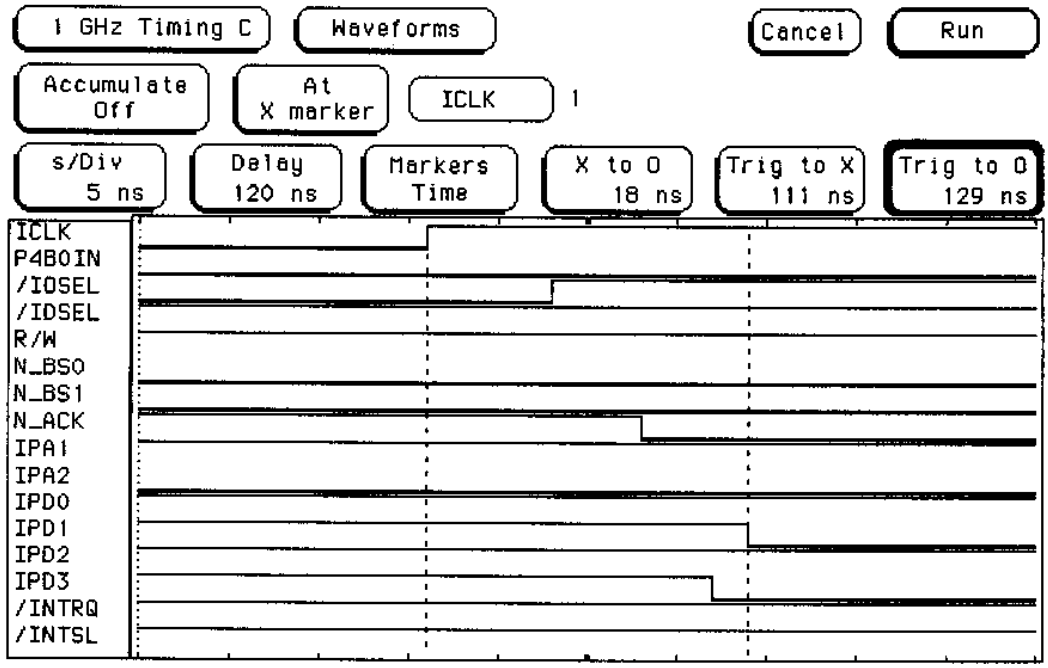


Figure 4-10 Zoomed-In View of DIO316I IO Read Cycle Driving N_ACK and IPD[3:0] Signals

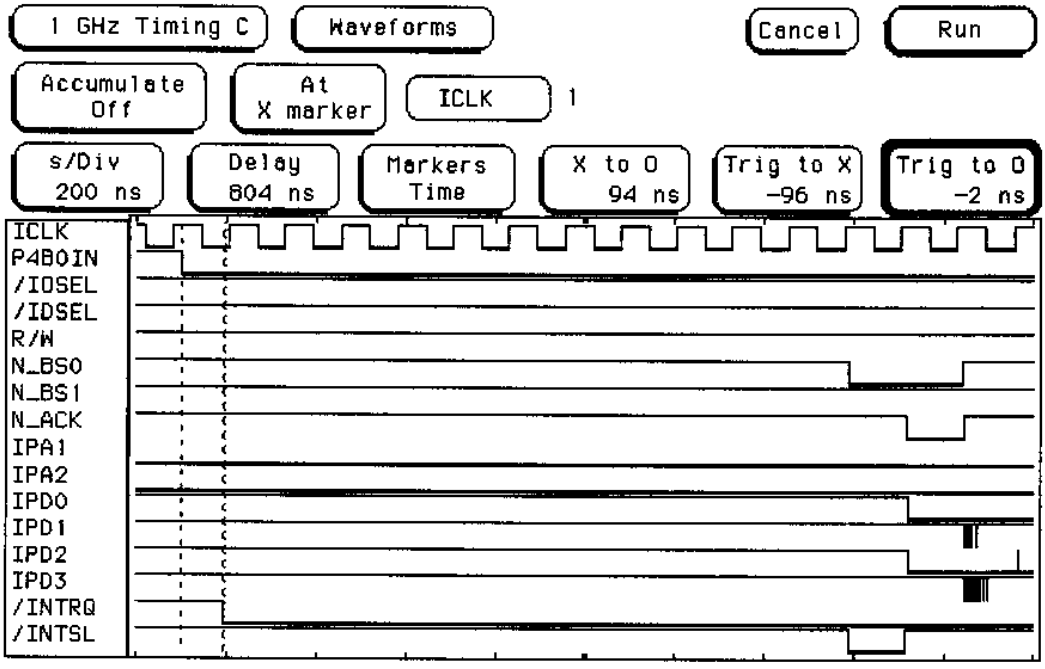


Figure 4-11 Interrupt Request Followed by an IP Interrupt Select Cycle

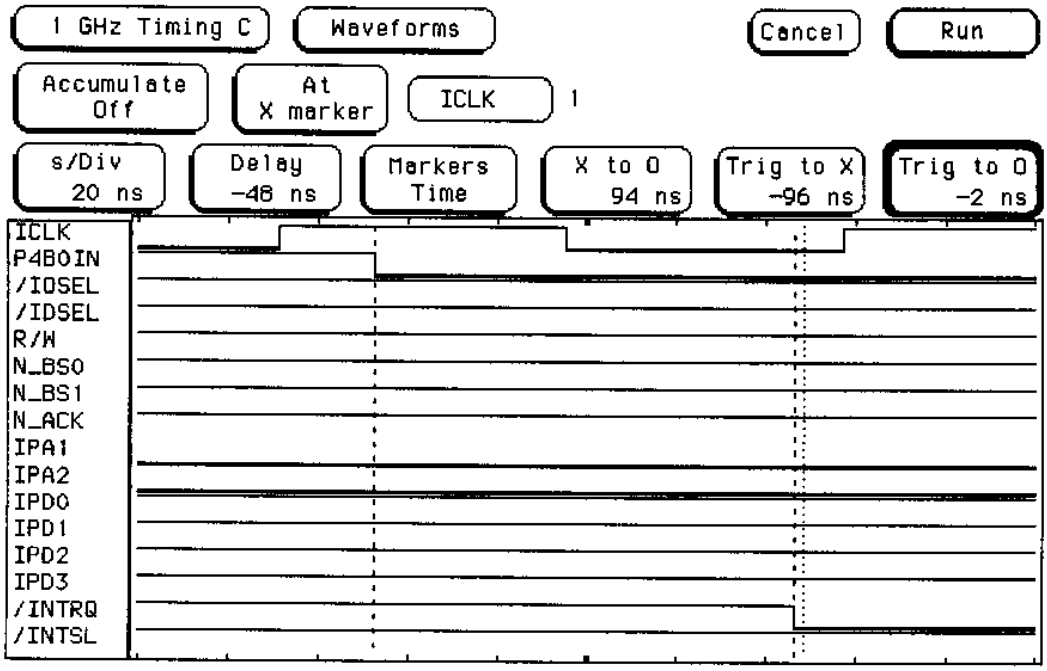


Figure 4-12 Interrupt Request Signal Asserted by DIO316I

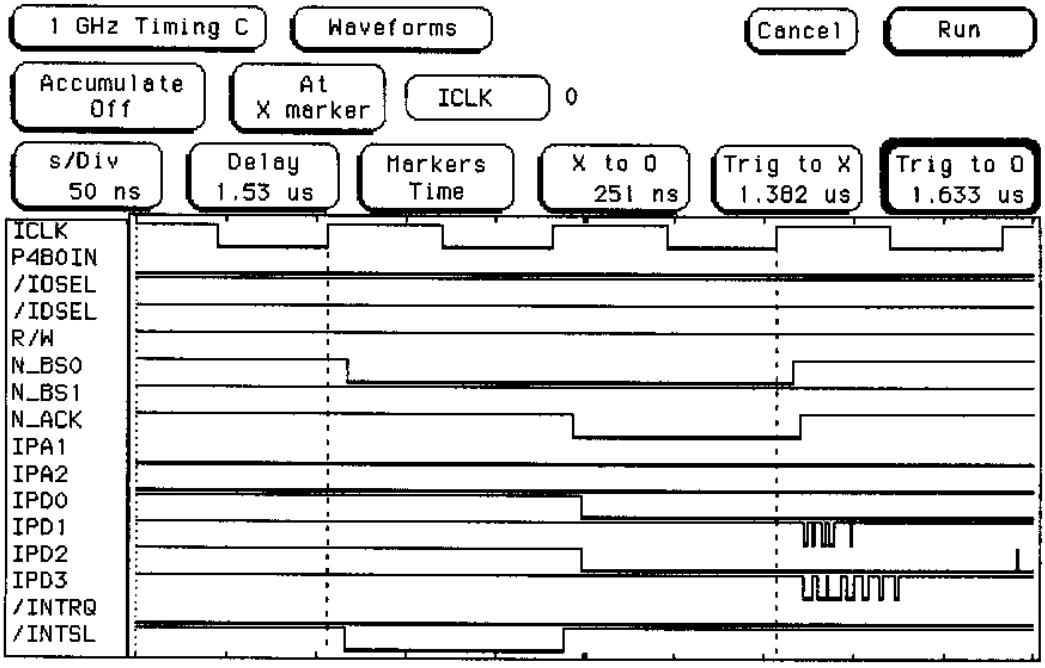


Figure 4-13 Typical IP Interrupt Select Cycle

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APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements ..... 1.800 inches x 3.900 inches x 0.303 inches (above board),
4.572 cm x 9.906 cm x 0.770 cm
Weight ..... 0.994 oz., 26.76 grams
Board thickness ..... 0.062 inches, 0.157 cm, nominally, (4 layer)

PROTOCOL

Clock rate ..... 8 MHz
Wait cycles ..... None on any transfer types
Hold cycles ..... Supported on all valid transfer types
Address decoding ..... Complete (no partial)
I/O transfers
- Writes 8-bit, 16-bit
- Reads 16-bit

I/O locations ..... Eleven, 16-bit
- Data Ports 3
- Control/Status 2
- Interrupt Control/Status 6
- Maximum read/write rate ..... 4 MTransfers/second, sustained

ID transfers ..... 8-bit read (only)
Zero-fill on upper byte
12 bytes, including CRC
- Systran's manufacturer's ID ..... 0x45, E ASCII
- DIO316I's model number ..... 0x63, c ASCII
- Cyclic Redundancy Check value 0xA6
- Maximum read rate ..... 4 MTransfers/second, sustained

Memory transfers ..... Not supported
Interrupt Vector transfers ..... 8-bit read on lower byte
Zero-fill on upper byte
- Maximum read rate ..... 4 MTransfers/second, sustained

Interrupt requests
- IP Module signal INTREQ0 is driven on programmed event
- IP Module signal INTREQ1 is not used

DMA activity ..... Not supported
Acknowledgment on unsupported transfer attempts ..... None generated
- Memory read and write
- ID write, and addresses beyond those needed for valid transfers

POWER REQUIREMENTS

Power: ..... +5 Vdc @ 130 mA (typical no load)

PERFORMANCE CHARACTERISTICS

Electrical Characteristics: Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

Supply voltage with respect to ground:

Minimum ..... -0.5 V
Maximum for digital ..... +7.0 V
I/O port signal's voltage
Minimum ..... -0.3 V
Maximum ..... +7.0 V

RECOMMENDED OPERATING CONDITIONS:

Supply voltage ..... +4.75 V → +5.25 V
I/O port signal's specification
Input rise time ..... 40 ns (maximum)
Input fall time ..... 40 ns (maximum)
Input voltage range ..... 0 V to supply voltage
Logic Interface ..... ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): ..... 0°C to +70°C
Temperature (no bias, storage): ..... -40°C to +150°C
Humidity (Non-condensing): ..... 5% to 95%
Vibration (Operating): ..... 10 G's RMS, 20→2000 Hz, random
Shock (Operating): ..... 50 G's maximum
Altitude (Operating): ..... 10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MTBF ..... 3,805,175 hours per MIL-HDBK-217F

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

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B.3 192-Channel Solid-State Relay Driver and Sense Board System B-2
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B.1 Overview

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the DIO316I IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 Solid-State Relay Driver and Monitor Board

In this application, up to 24 solid-state relays can be controlled and monitored simultaneously. Refer to Figure B-1 for a block diagram of this application of the DIO316I.

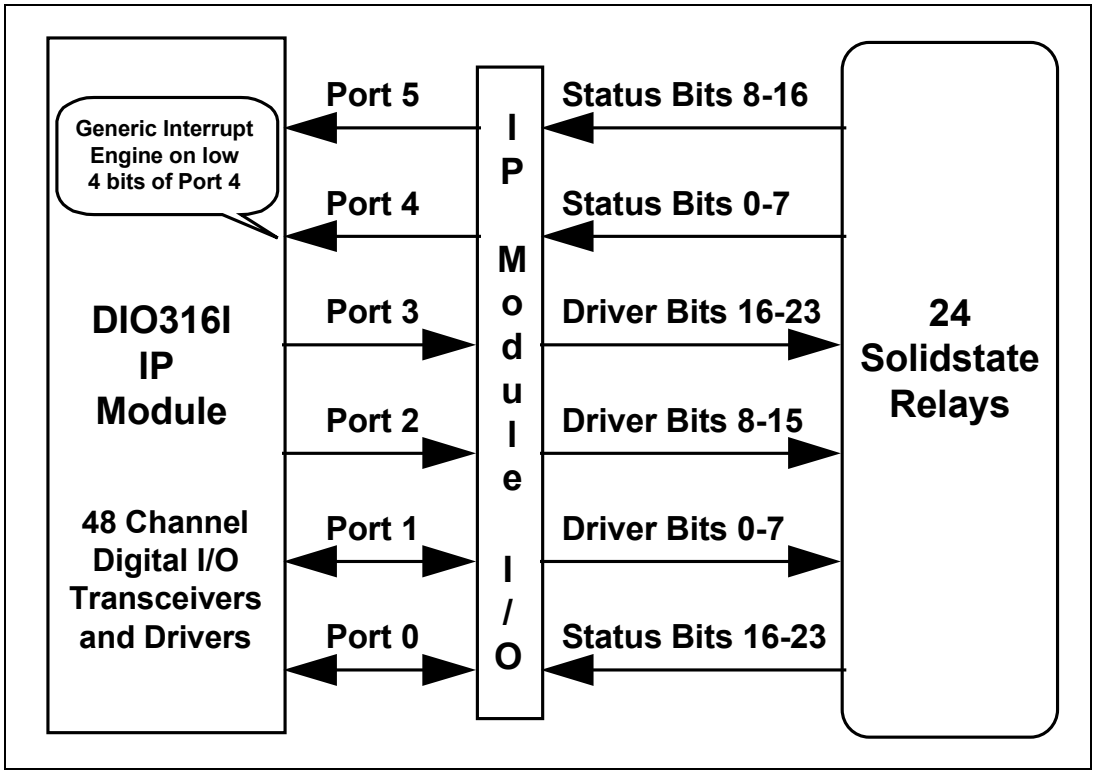


Figure B-1 DIO316I 24-Channel Solid-State Relay Driver

The DIO316I ports 1, 2, and 3 are the 24-relay driver output channels (bi-directional port 1 configured for outputs). Ports 0, 4, and 5 are the 24-relay status input channels (bi-directional port 0 configured for inputs). The status bits on the lower four bits of port 4 can be programmed for interrupts.

B.3 192-Channel Solid-State Relay Driver and Sense Board System

This application uses four DIO316Is as a 192-channel solid-state relay driver and sense board system on one IP Module Carrier board. The DIO316Is are configured for 96 digital outputs to drive one half of the relays, and 96 digital inputs to sense the other half of the relays. All of the solid-state relays can be controlled and monitored simultaneously via the IP Module Carrier board. Refer to Figure B-2 for a block diagram of this application of the DIO316I.

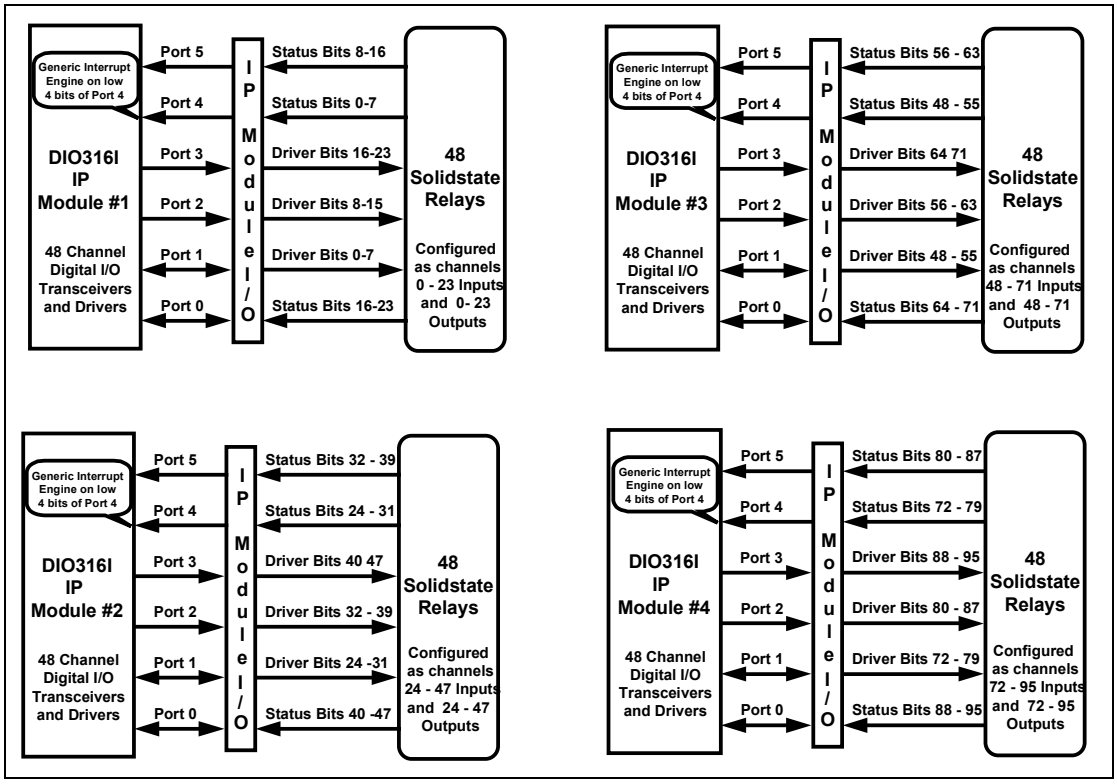


Figure B-2 Four DIO316Is as a 192-Channel Solid-State Relay System on a Single IP Module Carrier

On all four of the DIO316Is, ports 1, 2, and 3 are relay driver output channels (bi-directional port 1 configured for outputs), and ports 0, 4, and 5 are relay-sense input channels (bi-directional port 0 configured for inputs) for a total of 96 output, and 96 input channels. The solid-state relays can be AC or DC input (sense) and output (switch) configurations. Again, as with the application described in paragraph C.2, the lower four bits of port 4 on each DIO316I can be programmed for interrupts.

B.4 Keyboard (or keypad) Encoder

In this application, a B-row by 114-column keyboard matrix is configured using the DIO316I's ports 0, 1, 4, and 5; and two 1-by-4 joystick or trackball matrices using ports 0 and 5. Ports 2 and 3 are driver ports for 16 LED status indicators with an LED Enable Switch on port 5, bit 7. All of the key closures will be detected by driving one row signal active at a time, and then reading (or polling) the corresponding column matrix data. Figure B-3 describes the keyboard encoder matrix.

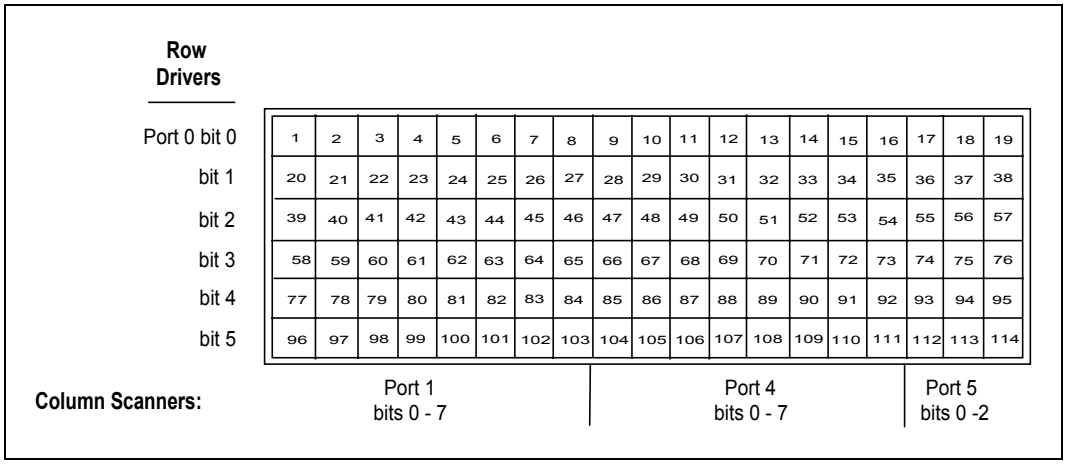


Figure B-3 DIO316I Keyboard Encoder Matrix

The keyboard encoder matrix is similar to a standard 101-key personal computer keyboard with two joystick/trackball input ports. The DIO316I port 0 is the output row driver (active low in this application), and ports 1, 4, and 5 are the input key closure detectors (with pull-up resistors in this application). Figure B-4 describes the joystick/trackball matrix.

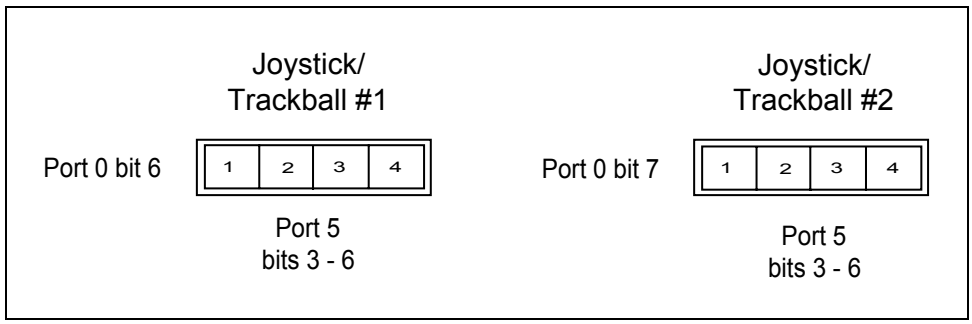


Figure B-4 Joystick or Trackball Matrices

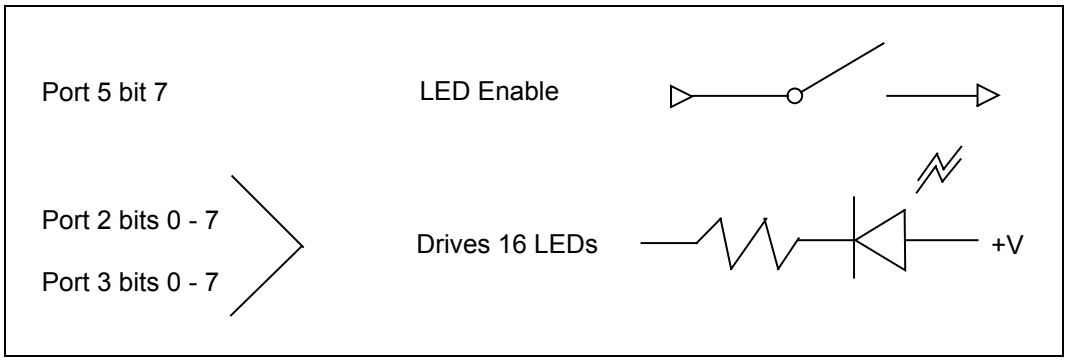


Figure B-5 LED-Enable Switch and Driver

As described in Figure B-5, ports 2 and 3 drive 16 status LEDs through series current-limiting resistors, and are enabled via a grounded switch (normally pulled high) on Port 5, bit 7.

Switch debouncing can be achieved via hardware or software corresponding to the desired matrix scanning frequency.

APPENDIX C

PROGRAMMING GUIDE

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C.1 Overview

This appendix describes the operation of the DIO316I from the software perspective, detailing the DIO316I registers and providing programming examples. A more detailed description of the hardware can be found in chapter 2: PRODUCT OVERVIEW and Appendix B: TYPICAL APPLICATIONS.

C.2 Description

The DIO316I is a 48-channel logic-level digital input/output card with the following ports:

- Two input-only ports
- Two output-only ports
- Two bi-directional ports

The bi-directional ports can be programmed to function as either input or output ports. All the output ports (both the output-only and the bi-directional ports programmed as output ports) have software programmable output-enable control. One of the input-only ports (port 4) has 4 bits (bits [3:0]) that can generate interrupts. The input condition that causes the interrupt can be programmed as low level, high level, rising edge, falling edge, or on-change.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by this function. This emulation saves space, lowers costs, improves reliability, and enables this IP Module to provide “no-wait” read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space results in no acknowledgement and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeros during valid ID read-only accesses.

Table C-1 is the DIO316I emulated ID Address Space PROM listing.

Table C-1 DIO316I ID Address Space Listing

IP Address	Description	Data Read
IPA = 0x00	ASCII 'I'	0x49
IPA = 0x01	ASCII 'P'	0x50
IPA = 0x02	ASCII 'A'	0x41
IPA = 0x03	ASCII 'C'	0x43
IPA = 0x04	SYSTRAN's ID	0x45
IPA = 0x05	DIO316I's Model Number	0x63
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0xA6

C.4 IP Module I/O Address Map

The DIO316I I/O Address Map shown in Table C-2 was designed with efficiently located data, control, and interrupt registers in the IP Module I/O address space (IPA = 0x00 → 0x0B). There are twelve 1B-bit-wide I/O addresses decoded, but only eleven are used at this time.

The first three locations (IPA = 0x00 → 0x02) are the data registers 0, 1, and 2, and may be viewed either as three 1B-bit (two data ports each) registers or as six 8-bit ports. Data register 0 contains data ports 1 and 0, data register 1 contains data ports 3 and 2, and data register 2 contains data ports 5 and 4.

The next two addresses (IPA = 0x03 → 0x04) are the control registers and are located in byte-lane 0. Control Register 0 (CR0) is the output-enable register for data ports 3, 2, 1, and 0. This register uses bits [3:0]. Each bit controls the port that has the same number (For example, bit 1 controls port 1). In CR0, bits [15:4] are not used and are read as zeros. Control Register 1 (CR1) is the direction register for data ports 1 and 0. This register uses bits [1:0]. Each bit controls the port that has the same number. In CR1, bits [15:2] are not used and are read as zeros. However, data ports 5 and 4 are input-only and have no corresponding control bits.

The next six addresses (IPA = 0x05 → 0x0A) are the interrupt control/status registers and are located in byte-lane 0. These registers perform the following functions:

Interrupt Register 0 (IR0) is the interrupt-enable register

- IR1 is the interrupt status register
- IR2 is the interrupt type register
- IR3 is the interrupt sense register
- IR4 is the interrupt on-change register
- IR5 is the interrupt vector register

In IR4, IR3, IR2, IR1 and IR0, bits [15:4] are not used, and in IR5, bits [15:8] are not used and are read as zeros. These registers use bits [3:0] the same way CR0 does, with each bit controlling the port that has the same number. IR5 uses bits [7:0] that are placed on the IPD[7:0] data lines during an IP Module interrupt cycle.

The last address, IPA = 0x0B, is part of the DIO316I's I/O address space, but has no function at this time, and is read as all zeros. (Refer to paragraph 4.8 for more details on register bit definitions.)

Table C-2 is the DIO316I I/O Address Map and contains the data ports, control registers, and interrupt registers.

Table C-2 DIO316I I/O Address Map

IP Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	Data Port 1	Data Port 0	Data Register 0 = Ports 1 & 0 8-bits each, bi-directional
IPA = 0x01	Data Port 3	Data Port 2	Data Register 1 = Ports 3 & 2 8-bits each, outputs only
IPA = 0x02	Data Port 5	Data Port 4	Data Register 2 = Ports 5 & 4 8-bits each, inputs only, w/Interrupts on port 4 bits [3:0]
IPA = 0x03	[XXXX,XXXX]	[XXXX] [3:0]	Control Register 0, (CR0) output enables for ports 3-0, 0=Disabled, 1=Enabled
IPA = 0x04	[XXXX,XXXX]	[XXXX] [1:0]	Control Register 1, (CR1) direction bits for ports 1-0, 2 bits, 0=Input, 1=Output
IPA = 0x05	[XXXX,XXXX]	[XXXX] [3:0]	Interrupt Reg. 0, (IR0) Int.-enable for port 4 bits, 4 bits, 0=Disabled, 1=Enabled
IPA = 0x06	[XXXX,XXXX]	[XXXX] [3:0]	Interrupt Reg. 1, (IR1) Int. Status Register, 4-bits, 0=No interrupt 1= Interrupt event happened
IPA = 0x07	[XXXX,XXXX]	[XXXX] [3:0]	Interrupt Reg. 2, (IR2) Int. Event Type, 4-bits, 0=Level, 1=Edge
IPA = 0x08	[XXXX,XXXX]	[XXXX] [3:0]	Interrupt Reg. 3, (IR3) Int. Event Sense, 4-bits, 0=Falling or Low, 1=Rising or High
IPA = 0x09	[XXXX,XXXX]	[XXXX] [3:0]	Interrupt Reg. 4, (IR4) Int. On-Change, 4-bits, Overrides all other Int. Registers, 0=Disabled, 1=Enabled
IPA = 0x0A	[XXXX,XXXX]	[7:0]	Interrupt Reg. 5, (IR5) Int. Vector Register, 8-bits
IPA = 0x0B	[XXXX,XXXX]	[XXXX,XXXX]	Reserved, Drives all 0's and N_ACK if read

NOTE: [X] means not used and is read as zero.

C.5 Power-Up and System Reset Defaults

All of the data ports, control registers, and interrupt registers default to all zeros (0x00) after power-up or a system reset. This in effect sets the bi-directional ports 0 and 1 as input ports, disables ports 2 and 3 output-enables, and disables all interrupts from port 4. Ports 4 and 5 will power-up to the logical state of their input signals.

C.6 Word Access Address Translation

Table C-3 shows the relationship between VME, ISA, and NuBus local bus addresses, and the IP Module address for word accesses.

In the table, the word BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VMEbus Address	ISA Bus Address	NuBus Address	IP Address
BASE + 0	BASE + 0	BASE + 2	IPA = 0x00
BASE + 2	BASE + 2	BASE + 6	IPA = 0x01
BASE + 4	BASE + 4	BASE + A	IPA = 0x02
BASE + 6	BASE + 6	BASE + E	IPA = 0x03
BASE + 8	BASE + 8	BASE + 12	IPA = 0x04
BASE + A	BASE + A	BASE + 16	IPA = 0x05
BASE + C	BASE + C	BASE + 1A	IPA = 0x06
BASE + E	BASE + E	BASE + 1E	IPA = 0x07
BASE + 10	BASE + 10	BASE + 22	IPA = 0x08
BASE + 12	BASE + 12	BASE + 26	IPA = 0x09
BASE + 14	BASE + 14	BASE + 2A	IPA = 0x0A
BASE + 16	BASE + 16	BASE + 2E	IPA = 0x0B

C.7 Byte Access Address Translation

Table C-4 shows the relationship between VME, ISA, and NuBus local bus addresses, and the IP Module address for byte accesses.

In the table, the word BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VMEbus Address	ISA Bus Address	NuBus Address	IP Address	Byte-Lane*
BASE + 0x1	BASE + 0x0	BASE + 0x3	IPA = 0x00	0
BASE + 0x0	BASE + 0x1	BASE + 0x2	IPA = 0x00	1
BASE + 0x3	BASE + 0x2	BASE + 0x7	IPA = 0x01	0
BASE + 0x2	BASE + 0x3	BASE + 0x6	IPA = 0x01	1
BASE + 0x5	BASE + 0x4	BASE + 0xB	IPA = 0x02	0
BASE + 0x4	BASE + 0x5	BASE + 0xA	IPA = 0x02	1
BASE + 0x7	BASE + 0x6	BASE + 0xF	IPA = 0x03	0
BASE + 0x6	BASE + 0x7	BASE + 0xE	IPA = 0x03	1
BASE + 0x9	BASE + 0x8	BASE + 0x13	IPA = 0x04	0
BASE + 0x8	BASE + 0x9	BASE + 0x12	IPA = 0x04	1
BASE + 0xB	BASE + 0xA	BASE + 0x17	IPA = 0x05	0
BASE + 0xA	BASE + 0xB	BASE + 0x16	IPA = 0x05	1
BASE + 0xD	BASE + 0xC	BASE + 0x1B	IPA = 0x06	0
BASE + 0xC	BASE + 0xD	BASE + 0x1A	IPA = 0x06	1
BASE + 0xF	BASE + 0xE	BASE + 0x1F	IPA = 0x07	0
BASE + 0xE	BASE + 0xF	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

C.8 Register Definitions

The DIO316I has eleven 1B-bit-wide registers: three data, two general control, and six interrupt related. Again the data registers may be viewed either as three 1B-bit (two data ports each) or as six 8-bit ports. The general control registers permit user selection of output enable and port direction control.

The interrupt-related registers allow the programming of interrupt signal type, sense, vector, and enable. These registers also provide the status of the four interrupt-capable inputs. Byte writes to any of these registers are non-destructive to adjacent bytes. The following paragraphs describe the registers in detail. The data register bit descriptions are shown in the associated tables.

The Read/Write (R/W) values in the definition tables indicate access. An “R” indicates read-only access, a “W“ indicates write-only access, and “RW” indicates both read and write access.

C.8.1 Data Register 0 Description (IPA = 0x00)

This 1B-bit read/write register is the data register for the pair of byte-wide bi-directional ports 0 and 1, with port 1 in byte-lane 1 and port 0 in byte-lane 0. These two 8-bit ports can also be viewed as a single 1B-bit register when both are programmed for the same direction. When written to, and programmed as an output, this register sets the output value of the ports. When written to, and programmed as an input, the write is ignored. When read, and programmed as an output port, the register returns the current value of the port. When read, and programmed as an input port, the register returns the state of the input pins. On power-up, ports 0 and 1 default to input ports, and this register reflects the logic state of the input pins.

Table C-5 Data Register 0 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	Din1B7	Din1B6	Din1B5	Din1B4	Din1B3	Din1B2	Din1B1	Din1B0	Din0B7	Din0B6	Din0B5	Din0B4	Din0B3	Din0B2	Din0B1	Din0B0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.

Din1B7 - Din1B0 : Bits 7 to 0 of the input data (the state of the input pins) for port 1.

Din0B7 - Din0B0 : Bits 7 to 0 of the input data for port 0.

C.8.2 Data Register 1 Description (IPA = 0x01)

This 1B-bit read/write register consists of the pair of byte-wide output ports 2 and 3, with port 3 in byte-lane 1 and port 2 in byte-lane 0. These two 8-bit ports can also be viewed as a single 1B-bit port. Writing to this register sets the output value of the ports. When read, the register returns the current value of the ports. On power-up, all bits are set to '0'.

Table C-6 Data Register 1 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

C.8.3 Data Register 2 Description (IPA = 0x02)

This 1B-bit read-only register is the data register for the pair of byte-wide input ports 4 and 5, with port 5 in byte-lane 1 and port 4 in byte-lane 0. These two 8-bit ports can also be viewed as a single 1B-bit port. Any write to this register is ignored. When read, it returns the state of the input pins. On power-up, all bits are set to the state of the input pins.

Table C-7 Data Register 2 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	Din5B7	Din5B6	Din5B5	Din5B4	Din5B3	Din5B2	Din5B1	Din5B0	Din4B7	Din4B6	Din4B5	Din4B4	Din4B3	DIn4B2	Din4B1	Din4B0

Din5B7 - Din5B0 : Bits 7 to 0 of the input data (the state of the input pins) for port 5.

Din4B7 - Din4B0 : Bits 7 to 0 of the input data for port 4.

C.8.4 CR0 - Output-Enable Control Register Description (IPA = 0x03)

This 1B-bit-wide read/write register selects the output-enable control for the output ports. The output-enable control can be selected on 8-bit port boundaries.

Table C-8 Output-Enable Control Register Bit Descriptions

Bit #	Bits 15 to 4	3	2	1	0
Bit Name	Not Used	P3 OE	P2 OE	P1 OE	P0 OE
R/W	Read as 0's Writes discarded	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0

Table C-9 Output-Enable Control Bit

OE Value	Output-Enable Selection per Port
0	Port outputs disabled
1	Port outputs enabled

C.8.5 CR1 - Port Direction Control Register Description (IPA = 0x04)

This 1B-bit-wide read/write register selects the port direction for the bi-directional ports 0 and 1. The port direction control can be selected on 8-bit port (octal) boundaries.

Table C-10 Port Direction Control Register Bit Descriptions

Bit #	Bits 15 to 2	1	0
Bit Name	Not Used	P1 Dir	P0 Dir
R/W	Read as 0's Writes discarded	RW	RW
Power-Up State	N/A	0	0

Table C-11 Port Direction Control Register Bit Descriptions

Bit #	Bits 15 to 2	1	0
Bit Name	Not Used	P1 Dir	P0 Dir
R/W	Read as 0's Writes discarded	RW	RW
Power-Up State	N/A	0	0

C.8.6 IR0 - Interrupt-Enable Control Register Description (IPA = 0x05)

This 1B-bit-wide read/write register enables/disables the interrupts for the interrupt-capable bits. The interrupt-capable bits are port 4, bits [3:0]. Interrupts can be enabled/disabled on a per-bit basis.

Table C-12 Interrupt-Enable Control Register Bit Descriptions

Bit #	Bits 15 to 4	3	2	1	0
Bit Name	Not Used	P4 B3 IE	P4 B2 IE	P4 B1 IE	P4 B0 IE
R/W	Read as 0's Writes discarded	RW	RW	RW	RW
Power-up State	N/A	0	0	0	0

Table C-13 Interrupt-Enable Control Bit

IE Value	Interrupt-Enable Selection per Bit
0	Interrupt disabled for bit X of port 4
1	Interrupt enabled for bit X of port 4

C.8.7 IR1 - Interrupt Status Register Description (IPA = 0x06)

This 1B-bit-wide read/write register provides the status for the interrupt-capable input bits. The interrupt-capable input bits are port 4, bits [3:0]. A bit is set in this register if the corresponding input pin meets the condition programmed for this pin (low level, high level, falling edge, rising edge, on change via IR2, IR3 and IR4). If a bit is set in this register, it is cleared by writing a '1' to that bit position. The status indication is valid whether the interrupt is enabled or disabled for the bit. This allows for polling of the interrupt status register even if the interrupt is disabled by IR0.

Table C-14 Interrupt Status Register Bit Descriptions

Bit #	Bits 15 to 4	3	2	1	0
Bit Name	Not Used	P4 B3 IS	P4 B2 IS	P4 B1 IS	P4 B0 IS
R/W	Read as 0's Writes discarded	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0

Table C-15 Interrupt Status Bit

IS Value	Interrupt Status per Bit
0	Input condition not detected for bit
1	Input condition detected for bit

C.8.8 Interrupt Input Condition Registers Description

The three registers listed below control the condition on the interrupt-capable input pins that causes the setting of the status bit for that input (and an interrupt if enabled):

- Edge/Level register
- High/Low register
- On-Change register

Table C-16 summarizes the input condition that corresponds to the settings in these registers. Each register is described in detail in subsequent paragraphs.

Table C-16 Interrupt Input Condition for Various Register Settings

Edge/Level Register	High/Low Register	On-Change Register	Resulting Interrupt Input Condition per Bit
0	0	0	Low Level
0	1	0	High Level
1	0	0	Falling Edge
1	1	0	Rising Edge
X	X	1	On-Change (rising or falling edge)

NOTE: "X" indicates "don't care"

C.8.9 IR2 - Interrupt-Type (Edge/Level) Register Description (IPA = 0x07)

This 1B-bit-wide read/write register, in conjunction with the high/low and the on- change registers, programs the condition on the input pin that causes an interrupt for the interrupt-capable bits. The interrupt-capable input bits are port 4, bits [3:0].

Table C-17 Interrupt Edge/Level Register Bit Descriptions

Bit #	Bits 15 to 4	3	2	1	0
Bit Name	Not Used	P4 B3 EL	P4 B2 EL	P4 B1 EL	P4 B0 EL
R/W	Read as 0's Writes discarded	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0

Table C-18 Interrupt Edge/Level Bit

EL Value	Edge/Level Condition per Bit
0	Level
1	Edge

C.8.10 IR3 - Interrupt Sense (High/Low) Register Description (IPA = 0x08)

This 1B-bit-wide read/write register, in conjunction with the edge/level and the on-change registers, programs the condition on the input pin that causes an interrupt for the interrupt-capable bits. The interrupt-capable input bits are port 4, bits [3:0].

Table C-19 Interrupt High/Low Register Bit Descriptions

Bit #	Bits 15 to 4	3	2	1	0
Bit Name	Not Used	P4 B3 HL	P4 B2 HL	P4 B1 HL	P4 B0 HL
R/W	Read as 0's Writes discarded	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0

Table C-20 Interrupt High/Low Bit

HL Value	High/Low Condition per Bit
0	Low - low level or falling edge
1	High - high level or rising edge

C.8.11 IR4 - Interrupt On-Change Register Description (IPA = 0x09)

This 1B-bit-wide read/write register, in conjunction with the edge/level and the high/low registers, programs the condition on the input pin that causes an interrupt for the interrupt-capable bits. The interrupt-capable input bits are port 4, bits [3:0]. A bit set in this register overrides the setting of the edge/level and high/low registers. The on-change condition is either a rising or falling edge (that is, any change of state).

Table C-21 Interrupt On-Change Register Bit Descriptions

Bit #	Bits 15 to 4	3	2	1	0
Bit Name	Not Used	P4 B3 OC	P4 B2 OC	P4 B1 OC	P4 B0 OC
R/W	Read as 0's Writes discarded	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0

Table C-22 Interrupt On-Change Bit

OC Value	On-Change Condition per Bit
0	Interrupt condition is determined by Edge/Level and High/Low registers
1	Interrupt condition is any change of state (rising or falling edge). Overrides the conditions set in the Edge/Level and High/Low registers

C.8.12 IR5 - Interrupt Vector Register Description (IPA = 0x0A)

This 1B-bit-wide read/write register contains the interrupt vector. Only the lower 8 bits are used. The upper 8 bits are read as zeros. This vector is presented on the IP Module data bus during an interrupt request transfer cycle.

Table C-23 Interrupt Vector Register Bit Descriptions

Bit #	Bits 15 to 8	7	6	5	4	3	2	1	0
Bit Name	Not Used	IV B7	IV B6	IV B5	IV B4	IV B3	IV B2	IV B1	IV B0
R/W	Read as 0's Writes discarded	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0	0	0	0	0

IVB7 - IVB0: The 8-bit interrupt vector

C.9 Programming Examples

The following examples illustrate how to program the DIO316I to achieve various operational modes. These four examples demonstrate how to do the following tasks:

- Control output-enable for output ports
- Control port direction for bi-directional ports
- Control and configure interrupt-capable input
- Perform interrupt service routine

C.9.1 Output-Enable Control Example

This example illustrates output-enable control. In this example the output-enable control for both ports (ports 2 and 3) are set the same; however, each 8-bit port can be individually controlled. Although this example uses only the dedicated output ports, the output-enable control illustrated here works the same for the bi-directional ports (ports 0 and 1) when they are configured as output ports.

- At power-up, all the data registers and the output-enable register are cleared (value of '0x0000').
- At power-up, the outputs are in the high-impedance state because they are disabled.
- Write '0x000C' to the output-enable register to enable the outputs for the two output-only ports (ports 2 and 3). The output pins corresponding to ports 2 and 3 should all be low, reflecting the '00's in the data register for ports 2 and 3.
- Write the word '0xFFFF' to data register 1 (or alternately write the byte '0xFF' to data ports 2 and 3). The outputs should now be high, reflecting the value of the data register for ports 2 and 3, which is all F's.
- Write any value to data register 1 (ports 2 and 3 data register). The outputs should reflect the value of these data registers.
- Write '0x0000' to the output-enable register. The outputs are now in the high-impedance state because the outputs are disabled.

C.9.2 Port Direction Control Example

This example illustrates port direction control for the two bi-directional ports (ports 0 and 1). In this example the port direction control for both ports are set the same; however, each 8-bit port can be individually controlled.



NOTE: When changing port direction from input to output, the current input data becomes the output data when the direction change occurs. As a precaution, ensure the output data is correct before enabling output. (See next paragraph)

For applications where changing port direction could cause a problem, the following sequence is recommended to effect the transition:

1. Disable the output-enable for the port while the port is still functioning as an input port.
2. Change the direction of the port to an output.
3. Write the desired output data to the data register.
4. Enable the output.

Following the above steps ensures that only the desired data is presented at the output pins.

EXAMPLE

- At power-up, all the data registers and the output-enable register are cleared (value of '0x0000').
- At power-up, the port direction control register is cleared (value of '0x0000', which corresponds to configuring the bi-directional ports (ports 0 and 1) as input ports).
- Read data register 0 (ports 0 and 1). The value read should reflect the states of the input pins for ports 0 and 1.
- Write '0x0003' to the port direction register to configure the bi-directional ports (ports 0 and 1) as output ports. Note that the outputs are not enabled yet (their power-up state is disabled).
- Write '0x0000'to data register 0 (ports 0 and 1 of data register).
- Write '0x0003' to the output-enable register to enable the outputs for the bi-directional ports. At this point, all the output pins should be low, reflecting the zeros in the port data registers.
- Write the word '0xFFFF' to data register 0 (or alternately write the byte '0xFF' to data ports 0 and 1). The outputs should now be high, reflecting the value of the data registers, which is all F's.
- Write '0x0000' to the port direction register to configure the bi-directional ports (ports 0 and 1) as input ports.

C.9.3 Interrupt Examples

This example illustrates the configuration and control for an interrupt-capable input. The interrupt-capable inputs are port 4, bits [3:0]. Although this example uses only bit 0, the same mechanism works for all four interrupt inputs. Each interrupt input can be individually configured. The common interrupt vector is the only connection between the four interrupt inputs.



NOTE: The detection of the selected input condition is independent of whether the interrupt is enabled or disabled. This allows polling of the interrupt status register to determine if the selected input condition was detected. For example, if bit 0 is programmed for on-change, the status register will indicate detection of a rising or falling edge regardless of whether the bit 0 interrupt is enabled.



NOTE: This example assumes a suitable ISR (Interrupt Service Routine) exists. An example ISR is shown in subsection C.9.4.

LOW-LEVEL INTERRUPT

- At power-up, the edge/level register is cleared (value of '0x0000', which corresponds to level).
- At power-up, the high/low register is cleared (value of '0x0000', which corresponds to low).
- At power-up, the on-change register is cleared (value of '0x0000', which means that the input condition defined by the edge/level and the high/low registers applies).
- At power-up, the interrupt-enable register is cleared (value of '0x0000', which corresponds to interrupt disabled. At this point, the input condition required to set the status bit (and generate an interrupt if the interrupt were enabled) is a low level.
- Write the desired 8-bit interrupt vector to the interrupt vector register.
- Write a '0x0001' to the interrupt-enable register. This enables the interrupt for bit 0. A low logic level applied to the port 4, bit 0 input pin generates an interrupt.

HIGH-LEVEL INTERRUPT

- Write a '0x0000' to the interrupt-enable register. This disables all interrupts
- Write a '0x0001' to the high/low register. At this point, the input condition required to set the status bit (and generate an interrupt if the interrupt is enabled) is a high level.
- Write a '0x0001' to the interrupt-enable register. This enables the interrupt for bit 0. A high logic level applied to the port 4, bit 0 input pin generates an interrupt.

RISING-EDGE INTERRUPT

- Write a '0x0000' to the interrupt-enable register. This disables all interrupts.
- Write a '0x0001' to the edge/level register. At this point, the input condition required to set the status bit (and generate an interrupt if the interrupt is enabled) is a rising edge
- Write a '0x0001' to the interrupt-enable register. This enables the interrupt for bit 0. A rising edge applied to the port 4, bit 0 input pin generates an interrupt.

FALLING-EDGE INTERRUPT

- Write a '0x0000' to the interrupt-enable register. This disables all interrupts.
- Write a '0x0000' to the high/low register. At this point, the input condition required to set the status bit (and generate an interrupt if the interrupt is enabled) is a falling edge.
- Write a '0x0001' to the interrupt-enable register. This enables the interrupt for bit 0. A falling edge applied to the port 4, bit 0 input pin generates an interrupt.

ON-CHANGE INTERRUPT

- Write a '0x0000' to the interrupt-enable register to disable all interrupts.
- Write a '0x0001' to the on-change register. At this point, the input condition required to set the status bit (and generate an interrupt if the interrupt is enabled) is a rising or falling edge. Note that setting the on-change bit overrides the setting of the edge/level and high/low registers
- Write a '0x0001' to the interrupt-enable register to enable the interrupt for bit 0. A rising or falling edge applied to the port 4, bit 0 input pin generates an interrupt.
- Write a '0x0000' to the interrupt-enable register to disable all interrupts.

C.9.4 Interrupt Service Routine Example

If the interrupt capability of the DIO316I is used, a suitable ISR must exist. This example describes some steps that the ISR should perform. The host-dependent details are left out since they will vary.

ISR ENTRY POINT:

- Read the interrupt status register. Test the bits to determine if any interrupts have occurred
- The interrupt usually indicates that some event-driven action is to be taken. If so, take the action associated with the detected interrupt(s). If the action taken must not be interrupted, disable higher priority interrupts while taking the action, then re-enable them.
- Remove the condition that caused the interrupt. If this is not practical to do from the ISR, disable the interrupt by clearing the enable bit for the interrupt in the interrupt-enable register, and set a flag indicating that some other process should clear the condition. If the condition is cleared outside the ISR, then the clearing process must also re-enable the interrupt.
- Clear the interrupt status register by writing a '1' to any bits set in the status register.
- Return from exception.

GLOSSARY

[x:y] ---------- Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (For example, Data bus [7:0] refers to the least significant eight bits).

byte ---------- 8 bits.

byte-lane ---------- 8 bits of a data bus on octal boundaries.

CAE ---------- Computer Aided Engineering.

doublewide ---------- An IP module that is twice the size of the singlewide board.

EPLD ---------- Erasable Programmable Logic Device.

ID PROM ---------- The circuitry that presents the proper data patterns to the low 8 bits of the IPDbus, with upper-byte zero fills during the ID (read) transfers.

IP Module ---------- Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O ---------- Input/Output.

IP Module logic bus ---------- A synchronous, 4 MTransfers/sec, 16- or 32-bit-wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6 bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 M words of memory space per IP Module.

IPDbus ---------- IP Module Data Bus.

ISR ---------- Interrupt Service Routine.

LSB ---------- Least Significant Bit.

MTBF ---------- Mean Time Between Failures.

ns, µs, ms ---------- Nanoseconds, microseconds, and milliseconds, respectively.

PC ---------- Personal Computer.

QSOP ---------- Quarter-sized Small Outline Packages.

singlewide ---------- A standard IndustryPack printed circuit board (3.9" by 1.8") with two 50-pin connectors.

VHDL ---------- Very high-speed integrated circuit Hardware Description Language.

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