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DUAL16CT - Dual 16-Bit Counter/Timer Board

USER MANUAL

Document No. B-T-MU-DUAL16CT-A-0-A1

FOREWORD

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GLOSSARY

[x:y]. Nomenclature designating a bit-range, where x is the left-most bit and y is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane. 8-bits of a data bus on octal boundaries.

CAE. Computer Aided Engineering.

doublewide. An IPack module that is twice the size of the singlewide board.

EPLD. Erasable Programmable Logic Device.

ID PROM. The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IndustryPack. Credit-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O. Input/Output.

IPack. Refers to the IndustryPack standard.

IPack logic bus. A synchronous, 8 Mbytes/sec, 16-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is a 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IPack module.

IPDbus. IPack Data Bus.

MTBF. Mean Time Between Failures.

ns, µs, ms. Nanoseconds, Microseconds, and Milliseconds respectively.

singlewide. An IPack printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

SOTC. Stop On Terminal Count. Control Register #1, bit 2.

Tristateable. Compatible with the TRI-STATE standard.

VHDL. Very high speed integrated circuit Hardware Description Language.

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1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for Systran's Dual 16-bit Counter/Timer IndustryPack (also called IPack) board, herein referred to as the DUAL16CT (two independent 16-bit counters) (part number BHAS-DUAL16CT).

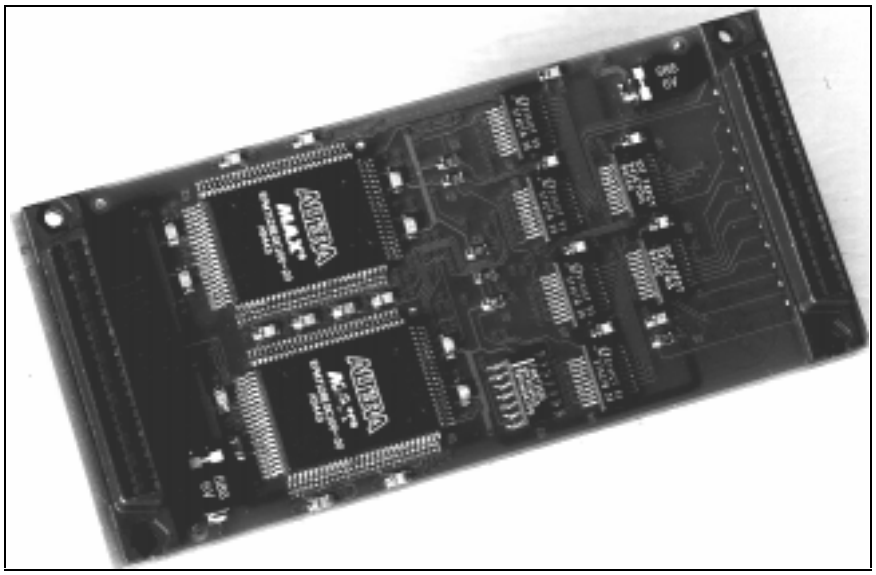


Figure 1-1 **DUAL16CT Board**

1.2 Scope

This reference manual covers the physical and operational description of the DUAL16CT, both from hardware and software perspectives. This document also contains detailed technical information about the DUAL16CT's performance characteristics, and a few typical applications. It is assumed that the reader has a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IPacks on their carrier(s) of choice. Citation of equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The DUAL16CT is a singlewide IPack board, conforming both mechanically and electrically to the IndustryPack specification, revision 0.7.1. The DUAL16CT board provides two, simple to use, completely independent 16-bit up counter/timers. Each counter/timer has seven 16-bit registers that determine its configuration and operation: one data, one control, one configuration, one terminal count, and three interrupt related. The board is a counter when using the external clock, and a timer when using one of the internal clock frequencies.

1.3.1 Features

- Concise, intuitive register set for easy programming
- Gateable internal clocks at 8 Mhz, 1 Mhz, and 125 Khz or external clocks up to 25 Mhz with terminal count or up to 50 Mhz as a totalizer
- Terminal count detect programmable via terminal count registers
- Rollover or Stop on terminal count
- Interrupt on terminal count
- Trigger outputs on terminal count (high and low pulses, or state toggle)
- True latched on the fly reading of count value (no re-read checking necessary)
- Timer enable, Clock enable, and counter reset control via software or I/O signals for multiple timer applications

1.4 Specifications

MECHANICAL: Singlewide IPack

- Measurements: 1.8000″ x 3.900″ x 0.303″ (above board),
  4.572 x 9.906 x 0.770 cm
- Weight: 0.9392 oz., 26.7 grams
- Board thickness: 0.062″, 0.157 cm, nominally, (4 layer)

PROTOCOL: Singlewide IPack Transfers

- 8 MHz clock rate
- No wait cycles on any transfer types
- Hold cycles supported on all valid transfer types
- Complete (no partial) address decoding
- I/O transfers: 8-, 16-bit writes 16-bit reads
- Fourteen, 16-bit I/O locations:
  - one data for each counter
  - one control for each counter
  - one configuration for each counter
  - one terminal count for each counter
  - three interrupt for each counter
  - Maximum read/write rate: 4 Mtransfers/second, sustained
- ID transfers: 8-bit read (only)
  - Zero-fill on upper byte
  - Twelve bytes, including CRC

  - Systran's manufacturer's ID = 45 *hex = E ASCII*
  - DUAL16CT's model number = 6B *hex*, = k *ASCII*
  - Cyclic Redundancy Check value = 0B *hex*
  - Maximum read rate: 4 Mtransfers/second, sustained
- Memory transfers:
  - Not supported
- Interrupt Vector transfers:
  - 8-bit read
  - Zero-fill on upper byte
  - Maximum read rate: 4 Mtransfers/second, sustained
- Interrupt requests:
  - IPack signal **INTREQ0** is driven on programmed event for counter #1
  - IPack signal **INTREQ1** is driven on programmed event for counter #2
- DMA activity:
  - None supported
- No acknowledgement on unsupported transfer attempts:
  - Memory read and write, ID write, and addresses beyond those needed for valid transfers
- Power-up Default Condition
  - All registers default to 0's (I/O read of 0000 *hex*), except the terminal count registers default to all 1's (1111 *hex*)
- No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS:

- Power: +5 Vdc @ 296 mA
  +12 Vdc @ 0 mA
  -12 Vdc @ 0 mA

PERFORMANCE CHARACTERISTICS:

- Electrical Characteristics: Refer to Section 5.0: PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

- Supply voltage with respect to ground: -0.5 V minimum, +7.0 V maximum

RECOMMENDED OPERATING CONDITIONS:

- Supply voltage: +4.75 V $\rightarrow$ +5.25 V
- Logic Interface: IndustryPack specification compliant carrier
- Environmental: see below

ENVIRONMENTAL SPECIFICATIONS:

- Temperature (Operating): 0°C to +70°C

- Temperature (no bias, storage): -40°C to +150°C
- Humidity (Non-condensing): 5% to 95%
- Vibration (Operating): 15 G's RMS (10→55 Hz)
- Shock (Operating): 50 G's maximum
- Altitude (Operating): 10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF):

- 4,608,295 hours per MIL-HDBK-217F

1.5 Related Products

- Software: 'C' library and OS-9® device driver routines with documentation.
- ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

1.6 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp. (This Synopsis is included in this document as Appendix A).

- SYSTRAN I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IndustryPack Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001-A-0-A1)

- *IndustryPack Logic Interface Specification Revision 0.7.1* published by Greenspring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.7 Ordering Process

To order SYSTRAN products, call (513) 252-5601. For additional product information you may call the above number, or send an E-Mail message to **info@systran.com**.

1.8 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes and distributes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct any programming questions, any concerns about the functional-fit of this product for your particular application, or any questions not answered satisfactorily by this document, to the factory at **(513)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance.

Refer to Section 7.0 for warranty and repair information.

1.9 Reliability

SYSTRAN Corporate policy is to provide the highest-quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

An integral part of SYSTRAN quality and reliability goals is customer feedback. Customers are encouraged to contact the factory with any questions or suggestions regarding unique quality requirements, or to obtain additional information about our programs. SYSTRAN's commitment to customers includes, but is not limited to:

- Professional and quick response to customer problems utilizing SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

SYSTRAN provides products and services that meet or exceed the best expectations of our customers.

- All products are tested using an Automatic Test Equipment system, with samplings for all product types taken through extended testing scenarios that include stress testing for voltage and temperature ranges beyond specifications.
- All products receive a predictive reliability rating based upon a calculated MTBF utilizing the MIL-HDBK-217F. Field failures are continuously logged and evaluated for potential failure modes and trends.
- Other environmental parameters are guaranteed by design, and not tested.
- Design reliability is ensured by methodology (top-down CAE design, VHDL, synthesis, extensive all-cases simulation, ALPHA build and test, and BETA testing if required) with full concurrent engineering practices throughout.

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2.0 DESCRIPTION



NOTE: The IPack signal references, transfer and cycle types discussed in this document are explained in detail in the *IndustryPack Logic Interface Specification Synopsis* included as Appendix A.

2.1 Block Diagram Description

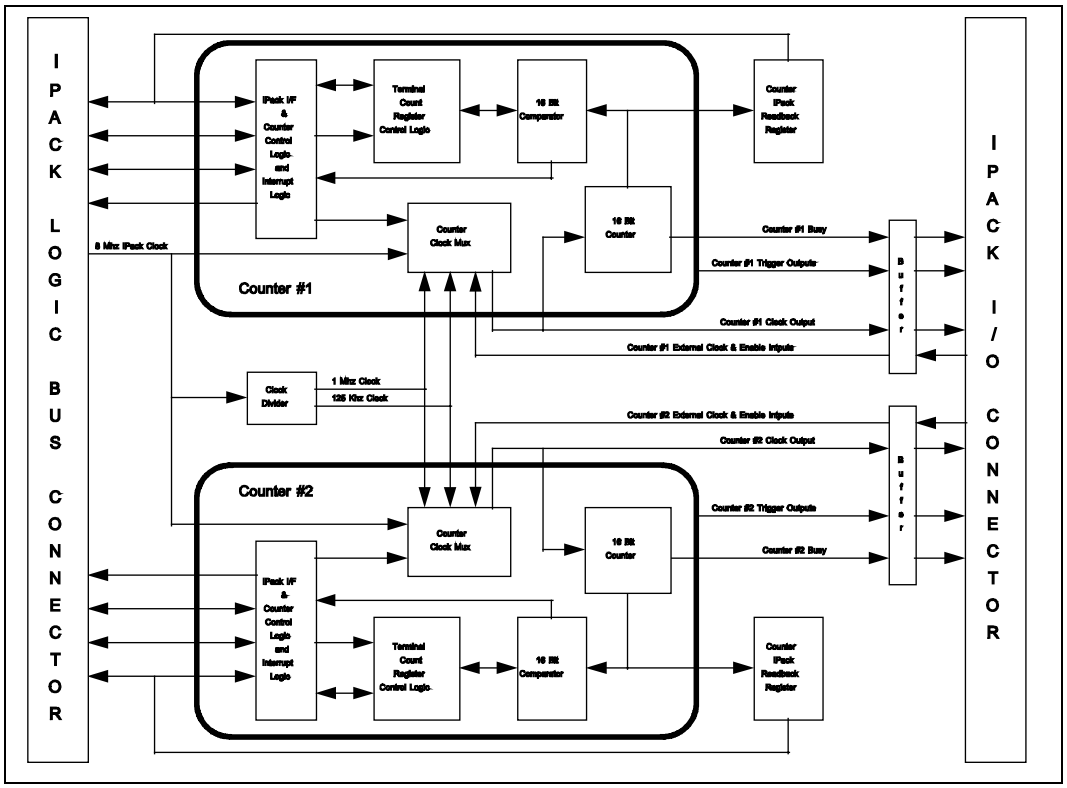


Figure 2-1 **DUAL16CT Block Diagram.**

Figure 2-1 is a simplified block diagram of the DUAL16CT representing the signal flow between the IPack Logic Bus and I/O connectors. On the left side is the IPack's Logic Bus connector through which all transfers between the IPack carrier and the DUAL16CT's registers and data sources are conducted. The blocks labeled "Counter #1 and Counter #2" contains all of the ID "PROM" data, and IPack transfer sequence/control and data bus interface logic, along with each 16-bit counter, terminal count comparators, and clock multiplexers for each counter. These blocks of circuitry are completely implemented with two EPLD devices. The blocks labeled "Counter IPack Readback Register" consist of two octal read-back data registers per counter. The block labeled "Clock Divider" divides down the 8 Mhz IPack clock to generate the 1 Mhz and 125 Khz internal

clocks. All of the control and external clock signals of both counters are buffered to the far-right block labeled “IPack I/O Connector”.



NOTE: The count value can be accessed while the counter is running by reading the data register via a normal I/O read cycle. When the data register is read, the entire 16-bit count value is latched into the data registers for an instantaneous snapshot of the count value. Just after the data register is read, the latches are released.

2.2 Detailed Description



NOTE: Refer to the DUAL16CT schematics located in Appendix B while reading this material since individual components are referenced by functional name, schematic reference designator, or industry-standard device part number.

The DUAL16CT was developed using VHDL and Synthesis, targeted to Altera EPLDs, schematic captured and integrated into standard logic devices, connectors and discrete components using Viewdraw by VIEWlogic and associated packages. This top-down design methodology is evident in the schematics and product design material presented in this document.

2.2.1 Schematics

For those readers not familiar with the top-down design methodology used for developing this IPack product, the following is a short travel-map through the schematics of the DUAL16CT.

There are four pages that comprise the schematic set. The first one, labeled “Top Level Schematic” is one of two top-level drawings composed of the IPack Logic, two netlisted generic blocks labeled “S_D16CT1” and “S_D16CT2”, four 74FCT574 registers, and a 74HCT393D dual 4-bit counter.

The second page is composed of two 74FCT541 buffers, nineteen capacitors, and a symbol for the printed circuit board, and the I/O (user's) connector. “Pushing-down” into each of the two generic blocks brings the reader to pages 3, and 4 (in the order cited above).

The “S_D16CT1” block (on page 1) consists of a single netlisted ALTERA EPM7128EQC100 device described on page B-3.

The “S_D16CT2” also consists of a single netlisted ALTERA EPM7128EQC100 device described on page B-4.

2.2.2 Components

IPACK LOGIC CONNECTOR

All IPack Logic Bus transfers take place across J1, the IPack Logic Connector, located on the left side of the block and schematic diagrams. The reader is referred to Appendix A for details about the signals on this connector, and their functions. Generally speaking, this IPack does not support DMA, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and writes to the I/O map.

PRIMARY ACTIVITY CONTROLLER

The DUAL16CT's primary activity controller is housed within the EPM7128EQC100 EPLDs located at U1 and U2 on the schematics. They serve as the IPack transfer sequence engine, whose responsibilities include:

- detection of valid I/O and ID transfer operations within their respective fully decoded address ranges, including the support of HOLD cycles when generated by a carrier
- ID PROM emulation data pattern generation for ID read transfers
- the I/O functions of write registration and read gating of the data/control register information

At power-up or any other form of “reset" operation, all of the I/O registers are cleared or reset, thereby clearing the counters and disabling them until specifically manipulated by an I/O write transfer.

COUNTER READ-BACK REGISTERS

The 74FCT574s are the counter read-back registers located at U5 and U7 for Counter #1, and U4 and U6 for Counter #2. They are for registering the counter’s data and driving the IPack data bus. U3 is a 74HCT393D and divides down the 8 MHz ICLK signal to provide the 1 Mhz and 125 KHz internal clock frequencies to each counter in U1 and U2.

BUFFERS

The 74FCT541 buffers (U10 and U13) buffer the output trigger and busy signals along with squaring up the input external clock, clock-enable and timer-enable signals for each counter to the user's I/O connector (J2).

2.2.3 Signal Descriptions

The following table shows the signal lines available at the I/O connector for each DUAL16CT counter:

Table 2-1 **I/O Signals for Each DUAL16CT Counter**

SIGNAL NAME	TYPE	SIGNAL DESCRIPTION
TIMER_EN(1,2)	Input	This is an external timer enable input (logic high = timer enable, logic low = disable). This signal, in conjunction with the Timer Enable bit in the control register, enables (run mode)/disables(setup mode) the timer. The Timer Enable bit must be set for this signal to enable the timer. This signal can be driven by the output of another timer for multi-timer applications such as variable period, variable duty cycle pulse generation. This signal is pulled-up so the timer is enabled if there is no connection.
EXT_CLOCK(1,2)	Input	This is the external clock input for each counter.
CLOCK_EN(1,2)	Input	This is an external clock enable/disable signal (logic high =enable, logic low=disable). This signal, in conjunction with the Clock Enable bit in the control register, enables /disables the clock. The Clock Enable bit must be set for this signal to enable the clock. This signal is pulled-up so the clock is enabled if there is no connection.
Trigpulse(1,2)	Output	This trigger signal powers up low then drives high for ~250 ns when each terminal count is reached.
Trigtoggle(1,2)	Output	This trigger signal powers up (or after a counter or system reset) high then toggles low when the terminal count is reached, then toggling state with each terminal count.
N_Trigpulse(1,2)	Output	This trigger signal powers up high then drives low for ~250 ns when each terminal count is reached.
N_Trigtoggle(1,2)	Output	This trigger signal powers up (or after a counter or system reset) low then toggles high when the terminal count is reached, then toggling state with each terminal count.
Busy(1,2)	Output	This signal is high when the counter/timer is counting, and low when the counter/timer is idle. This signal is provided for multi-counter/timer applications such as frequency measurement.

2.2.4 Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol. Do NOT use gasoline or thinner type solvents on this product.

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3.0 HARDWARE INSTALLATION

3.1 Unpacking the DUAL16CT

The contents of the DUAL16CT shipping packages are listed in 1:

Table 3-1 Contents of DUAL16CT Shipping Packages

QTY	DESCRIPTION
1	DUAL16CT Printed Circuit Assembly
1	DUAL16CT User Manual *

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals up to one per board are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR-DUAL16CT).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Visual Inspection of the DUAL16CT

Examine the DUAL16CT to determine if any damage occurred during shipping.

3.3 DUAL16CT Installation



NOTE: The DUAL16CT is an Electrostatic Sensitive Device (ESD), the hardware installation of the DUAL16CT must be conducted on a good anti-static workbench to protect the IPack and carrier boards. The IPack carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the DUAL16CT can be completed.

The DUAL16CT installation requires the following tools:

Table 3-2 DUAL16CT Installation Tools

QTY	DESCRIPTION
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

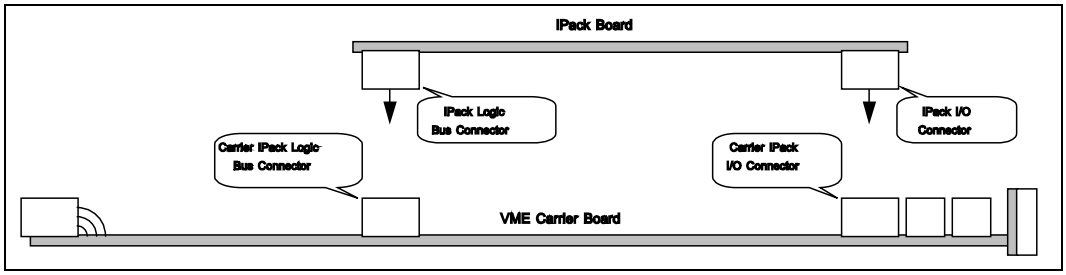


Figure 3-1 **Installation of the DUAL16CT on a VME IPack carrier board.**

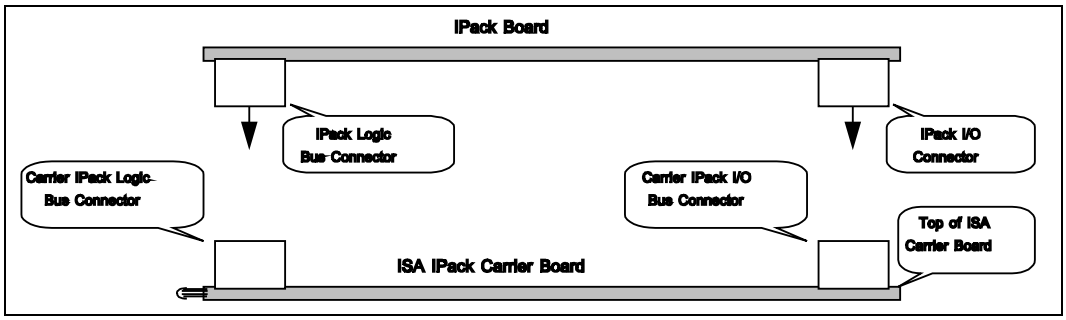


Figure 3-2 **Installation of the DUAL16CT on a ISA IPack carrier board.**

Figure 3-1 shows the DUAL16CT installed on a VME IPack carrier, and Figure 3-2 describes the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IPack Carrier board user's manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IPack carrier and move it to the ESD controlled area where the installation of the DUAL16CT can be made.
3. Remove the DUAL16CT from the shipping package and place it on the ESD bench.
4. Install the DUAL16CT onto the carrier board by applying adequate and equal pressure to the DUAL16CT board at both ends.

* 5. Install four M2x5mm flat head machine screws onto the IPack carrier's IPack connectors.

This completes the installation of the DUAL16CT to the carrier board.

Table 3-3 **IPack Logic Bus Pin Assignments**

Original IPack Signals Names	IPack Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 **IPack I/O Connector Pin Assignments**

IPack I/O Pin #	Signal Name
50	GND
49	Not Used
48	Not Used
47	Not Used
46	Not Used
45	Not Used
44	Not Used
43	Not Used
42	Not Used
41	Not Used
40	Not Used
39	Not Used
38	Not Used
37	Not Used
36	GND
35	N_TRIGTOGGLE2
34	GND
33	TRIGTOGGLE2
32	GND
31	N_TRIGPULSE2
30	GND
29	TRIGPULSE2
28	GND
27	BUSY2
26	GND
25	TIMER_EN2
24	GND
23	CLOCK_EN2
22	GND
21	EXT_CLOCK2
20	GND
19	GND
18	GND
17	GND
16	GND
15	N_TRIGTOGGLE1
14	GND
13	TRIGTOGGLE1
12	GND
11	N_TRIGPULSE1
10	GND
9	TRIGPULSE1
8	GND
7	BUSY1
6	GND
5	TIMER_EN1
4	GND
3	CLOCK_EN1
2	GND
1	EXT_CLOCK1

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4.0 PROGRAMMING GUIDE

This section of the manual describes the operation of the DUAL16CT from the software perspective, detailing the DUAL16CT registers and providing programming examples. A more detailed description of the hardware can be found in section 2.0: DESCRIPTION, and the application examples in section 6:0 TYPICAL APPLICATIONS.

4.1 Description

The DUAL16CT is a simple to use dual 16-bit counter/timer card. Each timer is completely independent with it's own register set and interrupts. Control signals and triggers are provided at the I/O connector for external monitor and control, such as multi-timer applications.

The DUAL16CT has fourteen 16-bit wide registers, seven per counter: one data register, one control register, one configuration register, one terminal count register, and three interrupt-related registers.

Counter values can be accessed while the counter is running by reading the data registers via a normal I/O read cycle. When read, the 16-bit count value is latched into the data register for an instantaneous snapshot of the count value. Just after the data register is read, the latches are released.

The control register allows gating of the clock signal and halt/run control of the timer. The configuration register provides selection of the clock source and the timer mode. The 16-bit terminal count value is initialized by writing to the terminal count register. The interrupt-related registers allow the programming of interrupt vector, interrupt enable, and provide interrupt status. Byte writes to any of these registers are not destructive to adjacent bytes.

4.2 IPack ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IPack to provide "no-wait" read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above 0C *hex*, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus timeout error on the carrier upon which this IPack resides.

The IPack ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

The following table is the DUAL16CT emulated ID Address Space PROM listing:

Table 4-5 **DUAL16CT ID Address Space Listing**

IPack ADDRESS	DESCRIPTION	DATA READ
IPA = 00 *hex*	ASCII "I"	49 *hex*
IPA = 01 *hex*	ASCII "P"	50 *hex*
IPA = 02 *hex*	ASCII "A"	41 *hex*
IPA = 03 *hex*	ASCII "C"	43 *hex*
IPA = 04 *hex*	SYSTRAN's ID	45 *hex*
IPA = 05 *hex*	DUAL16CT's Model Number	6B *hex*
IPA = 06 *hex*	Revision Level	30 *hex*
IPA = 07 *hex*	Reserved	00 *hex*
IPA = 08 *hex*	Low Byte Driver ID	00 *hex*
IPA = 09 *hex*	High Byte Driver ID	00 *hex*
IPA = 0A *hex*	Number of Bytes Used	0C *hex*
IPA = 0B *hex*	CRC	0B *hex*

4.3 IPack I/O Address Map

The DUAL16CT I/O Address Map was designed with efficiently located data, control, and interrupt registers in the IPack I/O address space (IPA= 00⇒0F *hex*). Addresses IPA= 00⇒07 *hex* are the I/O space for Counter #1 and Counter #2's I/O space is mirrored like Counter #1's in addresses IPA= 08⇒0F *hex*.

The first 16-bit register (IPA= 00 and 08 *hex*) are the counters #1 and #2 data registers and may be viewed as one 16-bit or two 8-bit registers.

The next addresses (IPA= 01⇒02 and 09⇒0A *hex*) are the control registers for each counter, and are located in byte-lane 0. Control Register 0 (CR0) is the "Timer Enable & Clock Enable" register and uses bits [1:0], with bit 1 controlling the Timer Enable and bit 0 controlling the Clock Enable for each counter, respectively. In CR0, bits [15:2] are not used and are read as '0's. Control Register 1 (CR1) is the "Stop On Terminal Count (SOTC)" bit and the "Clock Selection" register and uses bits [2:0], with bit 2 to control the SOTC and bits 1 and 0 for the clock selection. In CR1, bits [15:3] are not used and are read as '0's.

The next addresses (IPA= 03 and 0B *hex*) are the "Terminal Count" registers and may be viewed as one 16-bit or two 8-bit registers.

The next addresses (IPA= 04⇒06 and 0C⇒0E *hex*) are the interrupt control/status registers located in byte-lane 0. Interrupt Register 0 (IR0) is the "Interrupt Status" register, IR1 is the "Interrupt Enable" register, and both only use bit [0]. IR2 is the "Interrupt Vector" register and uses bits [7:0] and is placed on the IPD[7:0] data lines during an IPack Interrupt cycle. The last addresses (IPA= 07 and 0F *hex*) are in the DUAL16CT's I/O address space, but are not used, and when accessed will read as all zeros. Refer to the register bit definitions later in this Programming Guide for more details.

Table 4-2 is the DUAL16CT I/O Address Map and contains the data ports, control registers and interrupt registers:

Table 4-2 DUAL16CT I/O Address Map

IPack ADDRESS	BYTE-LANE 1	BYTE-LANE 0	DESCRIPTION
IPA = 00 *hex*	Data Bits [15:8]	Data Bits [7:0]	Counter #1 Data Register
IPA = 01 *hex*	[XXXX,XXXX]	[XXXX,XX] [1:0]	#1 Control Register 0, Timer Enable bit [1], Clock Enable bit [0], 0=Disabled & 1=Enabled
IPA = 02 *hex*	[XXXX,XXXX]	[XXXX,X] [2:0]	#1 Control Register 1, SOTC Enable bit [2], 0=Don't Stop, 1=Stop Clock Select bits [1:0] Internal 8 Mhz = 00 Internal 1 Mhz = 01 Internal 125 Khz = 10 External Clock = 11
IPA = 03 *hex*	Data Bits [15:8]	Data Bits [7:0]	#1 Terminal Count Register
IPA = 04 *hex*	[XXXX,XXXX]	[XXXX,XXX] [0]	#1 Interrupt Reg. 0, Int. Status Register bit, 0= No Interrupt, 1= SOTC reached
IPA = 05 *hex*	[XXXX,XXXX]	[XXXX,XXX] [0]	#1 Interrupt Reg. 1, Int. Enable bit, 0=Disabled & 1=Enabled
IPA = 06 *hex*	[XXXX,XXXX]	[7:0]	#1 Interrupt Reg. 2, Int. Vector Register, 8-bits
IPA = 07 *hex*	[XXXX,XXXX]	[XXXX,XXXX]	Not used.

Table 4-6 **DUAL16CT I/O Address Map**

Table 4-2 DUAL16CT I/O Address Map (Continued)

IPack ADDRESS	BYTE-LANE 1	BYTE-LANE 0	DESCRIPTION
IPA = 08 *hex*	Data Bits [15:8]	Data Bits [7:0]	Counter #2 Data Register
IPA = 09 *hex*	[XXXX,XXXX]	[XXXX,XX] [1:0]	#2 Control Register 0, Timer Enable bit [1], Clock Enable bit [0], 0=Disabled 1=Enabled
IPA = 0A *hex*	[XXXX,XXXX]	[XXXX,X] [2:0]	#2 Control Register 1, SOTC Enable bit [2], 0=Don't Stop, 1=Stop Clock Select bits [1:0] Internal 8 Mhz = 00 Internal 1 Mhz = 01 Internal 125 Khz = 10 External Clock = 11
IPA = 0B *hex*	Data Bits [15:8]	Data Bits [7:0]	#2 Terminal Count Register
IPA = 0C *hex*	[XXXX,XXXX]	[XXXX,XXX] [0]	#2 Interrupt Reg. 0, Int. Status Register bit, 0=No Interrupt, 1= SOTC reached
IPA = 0D *hex*	[XXXX,XXXX]	[XXXX,XXX] [0]	#2 Interrupt Reg. 1, Int. Enable bit, 0=Disabled 1=Enabled
IPA = 0E *hex*	[XXXX,XXXX]	[7:0]	#2 Interrupt Reg. 2, Int. Vector Register, 8-bits
IPA = 0F *hex*	[XXXX,XXXX]	[XXXX,XXXX]	Not used.

NOTE: [X] means the bit is not used.

4.4 Word Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-7 **Word Access Address Translation Table**

VME BUS ADDRESS	PC-AT BUS ADDRESS	NUBUS ADDRESS	IPack ADDRESS
BASE + 0	BASE + 0	BASE + 2	IPA=00 *hex*
BASE + 2	BASE + 2	BASE + 6	IPA=01 *hex*
BASE + 4	BASE + 4	BASE + A	IPA=02 *hex*
BASE + 6	BASE + 6	BASE + E	IPA=03 *hex*
BASE + 8	BASE + 8	BASE + 12	IPA=04 *hex*
BASE + A	BASE + A	BASE + 16	IPA=05 *hex*
BASE + C	BASE + C	BASE + 1A	IPA=06 *hex*
BASE + E	BASE + E	BASE + 1E	IPA=07 *hex*
BASE + 10	BASE + 10	BASE + 22	IPA=08 *hex*
BASE + 12	BASE + 12	BASE + 26	IPA=09 *hex*
BASE + 14	BASE + 14	BASE + 2A	IPA=0A *hex*
BASE + 16	BASE + 16	BASE + 2E	IPA=0B *hex*

4.5 Byte Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table 4-8 **Byte Access Address Translation Table**

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPack ADDRESS	BYTE-LANE*
BASE + 1	BASE + 0	BASE + 3	IPA=00 *hex*	0
BASE + 0	BASE + 1	BASE + 2	IPA=00 *hex*	1
BASE + 3	BASE + 2	BASE + 7	IPA=01 *hex*	0
BASE + 2	BASE + 3	BASE + 6	IPA=01 *hex*	1
BASE + 5	BASE + 4	BASE + B	IPA=02 *hex*	0
BASE + 4	BASE + 5	BASE + A	IPA=02 *hex*	1
BASE + 7	BASE + 6	BASE + F	IPA=03 *hex*	0
BASE + 6	BASE + 7	BASE + E	IPA=03 *hex*	1
BASE + 9	BASE + 8	BASE + 13	IPA=04 *hex*	0
BASE + 8	BASE + 9	BASE + 12	IPA=04 *hex*	1
BASE + B	BASE + A	BASE + 17	IPA=05 *hex*	0
BASE + A	BASE + B	BASE + 16	IPA=05 *hex*	1
BASE + D	BASE + C	BASE + 1B	IPA=06 *hex*	0
BASE + C	BASE + D	BASE + 1A	IPA=06 *hex*	1
BASE + F	BASE + E	BASE + 1F	IPA=07 *hex*	0
BASE + E	BASE + F	BASE + 1E	IPA=07 *hex*	1
BASE + 11	BASE + 10	BASE + 23	IPA=08 *hex*	0
BASE + 10	BASE + 11	BASE + 22	IPA=08 *hex*	1
BASE + 13	BASE + 12	BASE + 27	IPA=09 *hex*	0
BASE + 12	BASE + 13	BASE + 26	IPA=09 *hex*	1
BASE + 15	BASE + 14	BASE + 2B	IPA=0A *hex*	0
BASE + 14	BASE + 15	BASE + 2A	IPA=0A *hex*	1
BASE + 17	BASE + 16	BASE + 2F	IPA=0B *hex*	0
BASE + 16	BASE + 17	BASE + 2E	IPA=0B *hex*	1

* Byte-lane 1 not applicable for ID Space

4.6 Data Register Description (IPA = 00 and 08 *hex*)



NOTE: Counter values can be accessed while the counter is running by reading the data registers via a normal I/O read cycle. When read, the 16-bit count value is latched into the data register for an instantaneous snapshot of the count value. Just after the data register is read, the latches are released.

This register contains the 16-bit data value at IPA = 00 *hex* for Counter #1 and IPA = 08 *hex* for Counter #2. On power-up all bits are set to '0'.

Table 4-9 **Data Register Bit Descriptions**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D15-D0 : Bits 15 to 0 of the 16-bit data value.

4.7 Control Register 0 (CR0) Description (IPA = 01 and 09 *hex*)

This 16-bit read/write register is the counter/timer control register. There are two control bits in this register, the clock-enable bit, and the timer-enable bit. The clock- enable bit provides software controlled gating of the clock signal (either external or internal). The timer-enable bit controls whether the timer is in the run or setup mode. On power-up all bits are set to '0'.

Table 4-10 **Control Register Bit Descriptions**

Bit #	15 to 2	1	0
Bit Name	Not used	Timer Enable	Clock Enable
R/W	Read as 0's	RW	RW
Power-Up State	0	0	0

Clock Enable : Clock gating control - 1 = enable clock, 0 = disable clock.

Timer Enable : Counter/timer enable control - 1 = timer enabled (run mode), 0 = timer disabled (setup mode). When the SOTC bit (bit 2 in the configuration register) is set, the timer halts when the terminal count is reached. This timer enable bit, or the external Timer Enable signal must be toggled low, then high, to restart the timer when the SOTC is set and terminal count is reached.

4.8 Control Register 1 (CR1) Description (IPA = 02 and 0A *hex*)

This 16-bit read/write register is the counter/timer configuration register. There are two groups of bits in this register: the clock-select bits, and the stop-on-terminal-count bit. The clock-select bits select one of three internal clock frequencies or an external clock. On power-up all of the bits are cleared, with the internal 8 Mhz clock selected as the default.

Table 4-11 **Configuration Register Bit Descriptions**

Bit #	15 to 3	2	1	0
Bit Name	Not used	SOTC	CS1	CS0
R/W	Read as 0's	RW	RW	RW
Power-Up State	0	0	0	0

CS1-CS0 : Clock select bits (see table below)

Table 4-12 **Clock Select bits**

CS1	CS0	CLOCK SELECTION
0	0	Internal 8 Mhz clock
0	1	Internal 1 Mhz clock (default)
1	0	Internal 125 Khz clock
1	1	External clock

SOTC : Stop on Terminal Count bit - this bit determines if the counter stops when terminal count is reached, or rolls over to zero and keeps counting.
0 = don't stop on terminal count, 1 = stop on terminal count.

4.9 Terminal Count Register Description (IPA = 03 and 0B *hex*)

This register contains the 16-bit terminal count value. On power-up all bits are set to '1'.

Table 4-13 **Terminal Count Register Bit Descriptions**

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TC15-TC0 : Bits 15 to 0 of the 16-bit terminal count value.

4.10 Interrupt Status Register (IR0) Description (IPA = 04 and 0C *hex*)

This register contains the interrupt-status bit. This bit is set by the counter when the terminal count is reached. This bit indicates that the terminal count was reached whether the interrupt is enabled or not. Writing a '1' to this register clears the status bit. If the interrupt is enabled, an interrupt will occur when this bit sets, Counter #1 asserts INTREQ0 and Counter #2 asserts INTREQ1. On power-up this bit is set to 0.

Table 4-14 **Interrupt Status Register Bit Descriptions**

Bit #	15 to 1	0
Bit Name	Not used	Interrupt Status
R/W	Read as 0's	RW
Power-Up State	0	0

Interrupt Status - 1 = terminal count detected, 0 = terminal count not detected.

4.11 Interrupt Enable Register (IR1) Description (IPA = 05 and 0D *hex*)

This register contains the interrupt-enable bit. This bit enables/disables the generation of an interrupt request by the DUAL16CT when the terminal count is reached. On power-up this bit is set to 0.

Table 4-15 **Interrupt Enable Register Bit Descriptions**

Bit #	15 to 1	0
Bit Name	Not used	Interrupt En-able
R/W	Read as 0's	RW
Power-Up State	0	0

Interrupt Enable : Interrupt enable control - 1 = enabled, 0 = disabled.

4.12 Interrupt Vector Register (IR2) Description (IPA = 06 and 0E *hex*)

This register contains the interrupt vector. This 8-bit vector is presented to the IPack data bus during the Interrupt-Acknowledge transfer.

Table 4-16 **Interrupt Vector Register Bit Descriptions**

Bit #	15 to 8	7	6	5	4	3	2	1	0
Bit Name	Not used	IV7	IV6	IV5	IV4	IV3	IV2	IV1	IV0
R/W	Read as 0's	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0

IV7-IV0 : The 8-bit interrupt vector. On power-up all bits are set to 0.

4.13 Programming Examples

The following examples illustrate how to program the DUAL16CT device.

4.13.1 System Clock Example

This example uses a single timer to generate a periodic interrupt every 1 ms for system timekeeping.

Configuration:

Configuration Register

CS1-CS0 = 01 binary. This selects the internal clock at 1 Mhz.
SOTC = 0, don't stop on terminal count, rollover to '0' and keep counting.

Terminal Count Register

TC15-TC0 = 03E8 *hex* (1000 decimal)

Interrupt Vector Register

Load with the desired interrupt vector.

Interrupt Enable Register

Interrupt Enable = 1, the interrupt is enabled.

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register to a '1'. This starts the timer free running, and generates an interrupt every 1 ms. The interrupt service routine updates the system clock value and clears the Interrupt-Status bit in the Interrupt-Status Register by writing a '1' to it. No re-initialization of the timer is necessary because it is set up to free run.

4.13.2 Watchdog Timer Example

This example uses a single timer to implement a watchdog timer that times out after 10 ms if not serviced by the code. It is assumed that the trigger pulse output signal will be connected to the system reset circuitry.

Configuration:

Configuration Register

CS1-CS0 = 01 binary. This selects the internal clock at 1 Mhz.
SOTC = X, This is a don't care. If the timer times out the system will reset.

Terminal Count Register

TC15-TC0 = 2710 *hex* (10000 decimal)

Interrupt Vector Register

No initialization needed, interrupts not used in this example.

Interrupt Enable Register

Interrupt Enable = 0, the interrupt is disabled.

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register to a '1'. This starts the timer running. If the code clears then sets the Timer Enable bit in the Control Register before the 10 ms expires (resets the timer), no trigger pulse occurs. If the code fails to reset the timer before the 10 ms expires, the trigger pulse occurs, and the processor is reset (again, it is assumed that the trigger output drives the reset circuitry).

4.13.3 Square Wave Generator Example

This example uses a single timer to generate a 10 Khz square wave on the toggle output signal.

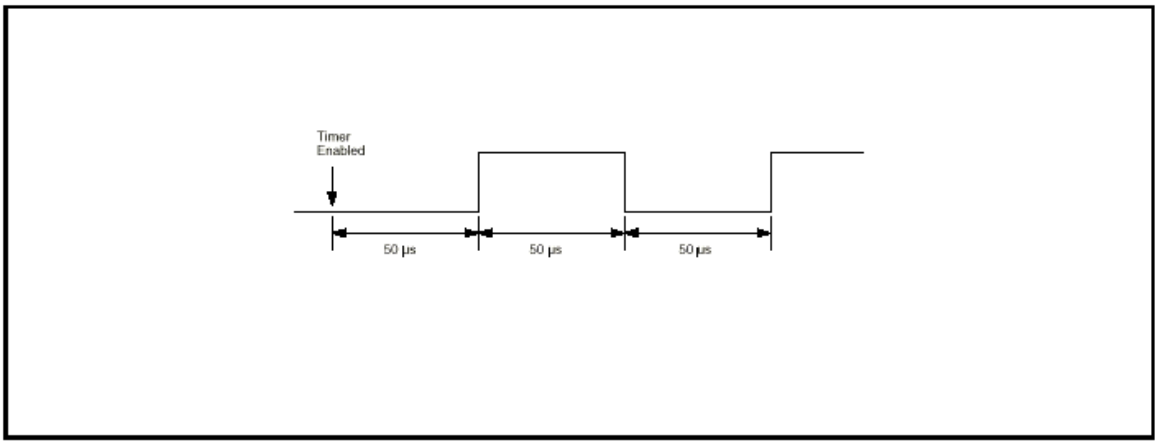


Figure 4-3 **Trigger Output Square Wave Example**

Configuration:

Configuration Register

CS1-CS0 = 01 binary. This selects the internal clock at 1 Mhz.
SOTC = 0, don't stop on terminal count, rollover to '0' and keep counting.

Terminal Count Register

TC15-TC0 = 0032 *hex* (50 decimal)

Interrupt Vector Register

No initialization needed, interrupts not used in this example.

Interrupt Enable Register

Interrupt Enable = 0, the interrupt is disabled.

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register to a '1'. This starts the timer running. Every 50 µs the trigger output toggles which generates a square wave (50% duty cycle). The timer will free run until disabled by clearing the Timer-Enable bit or pulling the Timer-Enable-input signal low.

4.13.4 Variable Period Variable Pulse Width Waveform Generator Example

This example uses both timers to generate a pulse with a 1 Khz period and a pulse width of 15 µs on the Busy signal output of Timer 2. Timer 1 is used to control the period, and Timer 2 is used to control the pulse width. The low-going Pulse-Trigger output of Timer 1 is connected to the Timer-Enable input of Timer 2.

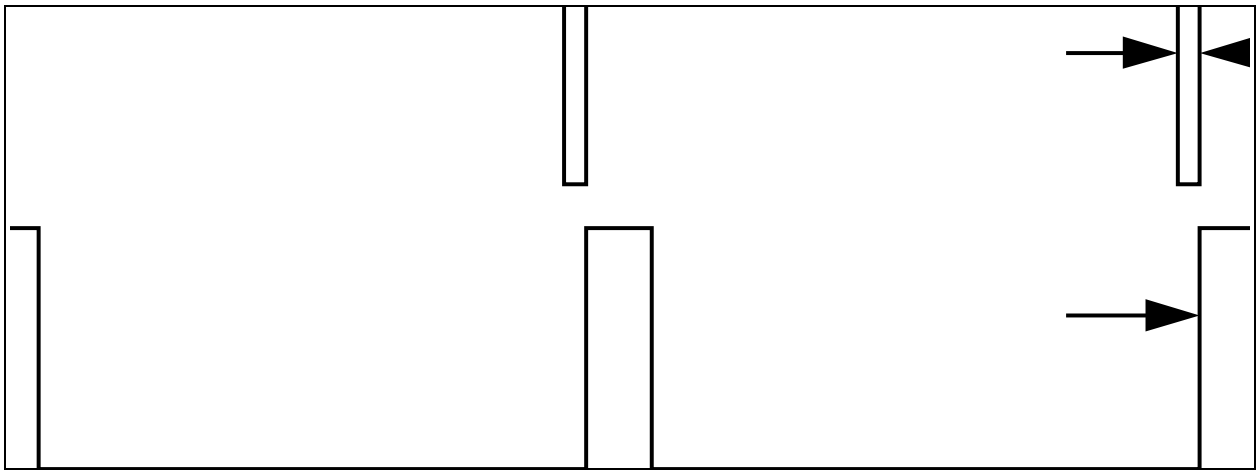


Figure 4-3 **Trigger and Busy signals for the Variable Period Variable Pulse Width Example**

Configuration for Timer 1 (period control):

Configuration Register

CS1-CS0 = 01 binary. This selects the internal clock at 1 Mhz.
SOTC = 0, don't stop on terminal count, rollover to '0' and keep counting.

Terminal Count Register

TC15-TC0 = 03E8 *hex* (1000 decimal)

Interrupt Vector Register

No initialization needed, interrupts not used in this example.

Interrupt Enable Register

Interrupt Enable = 0, the interrupt is disabled.

Configuration for Timer 2 (pulse width control):

Configuration Register

CS1-CS0 = 01 binary. This selects the internal clock at 1 Mhz.
SOTC = 1, stop on terminal count.

Terminal Count Register

TC15-TC0 = 000F *hex* (15 decimal)

Interrupt Vector Register

No initialization needed, interrupts not used in this example.

Interrupt Enable Register

Interrupt Enable = 0, the interrupt is disabled.

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register of both timers to '1'. This starts both timers running which generates the first pulse on the Busy output of Timer 2. Timer 2 times out in 15 µs (the pulse width) causing its Busy output to go low, and remains halted because the SOTC bit is set. When Timer 1 reaches its terminal count after 1 ms (the period), its trigger pulses low for 1 µs. Since the timer 1

trigger output is connected to the timer 2 Timer Enable input, this pulse resets Timer 2 and causes it to begin counting again. Timer 2 counts for 15 µs before reaching terminal count and while it is counting its Busy output is high.

In other words, the free running timer 1 (period control) triggers the one-shot Timer 2 (pulse width control) indefinitely until halted by the host. Therefore, the terminal count values of Timer 1 and Timer 2 can be varied to adjust the output waveform period and pulse width, respectively.

4.13.5 Precision Frequency Measurement Example

This example uses both timers to accurately measure the frequency of pulses. Timer 1 is used to control the time period over which the pulses are counted. Timer 2 is used as a counter with the pulse signal connected to its external clock input. The Busy output signal of Timer 1 is connected to the Clock Enable input of timer 2.

Configuration for Timer 1 (counting period control):
- Configuration Register
  - CS1-CS0 = 10 binary. This selects the internal clock at 125 Khz.
  - SOTC = 1, stop on terminal count.
- Terminal Count Register
  - TC15-TC0 = E848 *hex*.
  - So, the total terminal count is 1E848 *hex* (125,000 decimal)
- Interrupt Vector Register
  - No initialization needed, interrupts not used in this example.
- Interrupt Enable Register
  - Interrupt Enable = 0, the interrupt is disabled.

Configuration for Timer 2 (used as counter):
- Configuration Register
  - CS1-CS0 = 11 binary. This selects the external clock.
  - SOTC = 1, stop on terminal count.
- Terminal Count LSW Register
  - TC15-TC0 = FFFF *hex*.
  - The terminal count is set to the maximum so it doesn't interfere with the count. If the count reads all Fs, an overflow has occurred.
- Interrupt Vector Register
  - No initialization needed, interrupts not used in this example.
- Interrupt Enable Register
  - Interrupt Enable = 0, the interrupt is disabled.

Once configured, enable Timer 1 by setting its Timer-Enable and Clock-Enable bits in the Control Register to a 1. Timer 2 will not begin counting yet because its clock is gated off by the logic low Busy output of Timer 1. Now, enable Timer 2 by setting its Timer-Enable and Clock-Enable bits in the Control Register to a 1. Timer 1 will run for the programmed 1 second interval then stop. While Timer 1 is running, its Busy output is a logic high which enables the external clock of Timer 2. Thus, Timer 2 counts only during the 1 second period that Timer 1 is running. Since the clock gating is hardware controlled, no error is introduced by programmed I/O delays.

5. 0 PERFORMANCE

5.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration citied, and do not supplant the maximum and minimum envelopes presented in section 1: INTRODUCTION.

5.2 State Timing Diagrams

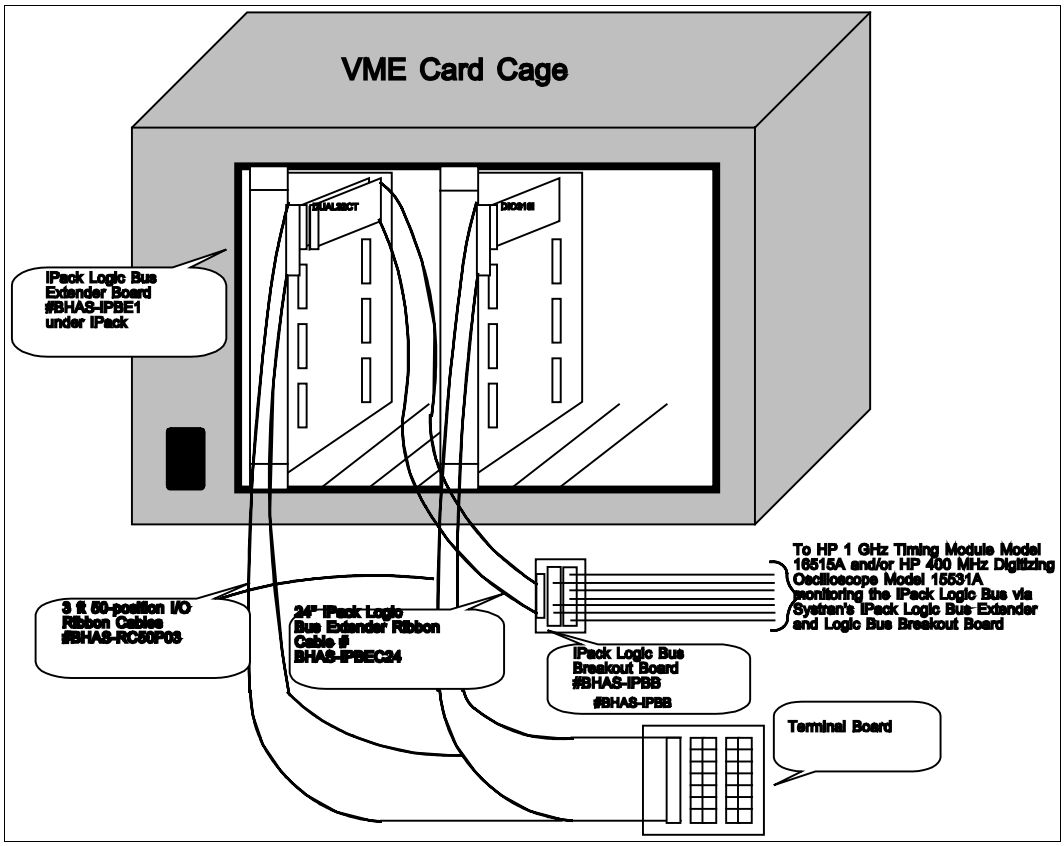


Figure 5-1 **IPack Test Configuration for State Timing Measurements**

5.3 ID Read Cycle

Figure 5-2 is a complete DUAL16CT ID read cycle. The signals of interest are /IDSEL, N_ACK, and the four IPD0-3 signals. Figure 5-3 is a zoomed in view of the DUAL16CT ID cycle driving the N_ACK and IPD0-3 signals; showing a typical response time of about 18 nanoseconds for driving these signals. The IPack Logic I/F Specification (Rev. 0.7.1, page 35) requires these signals be driven within 40 nanoseconds.

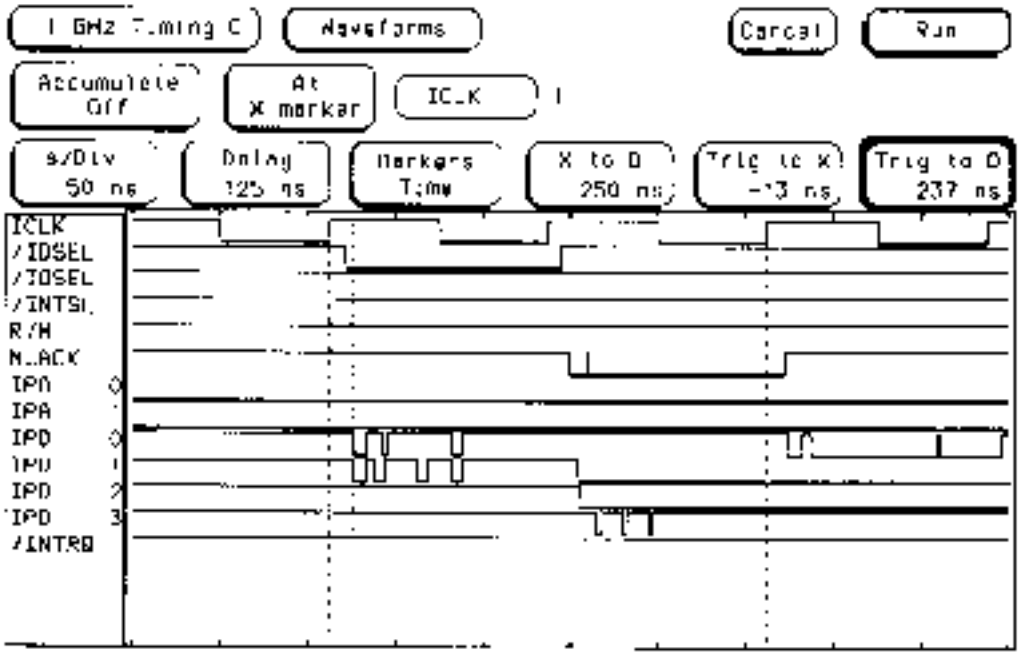


Figure 5-2 **Complete ID Read Cycle**

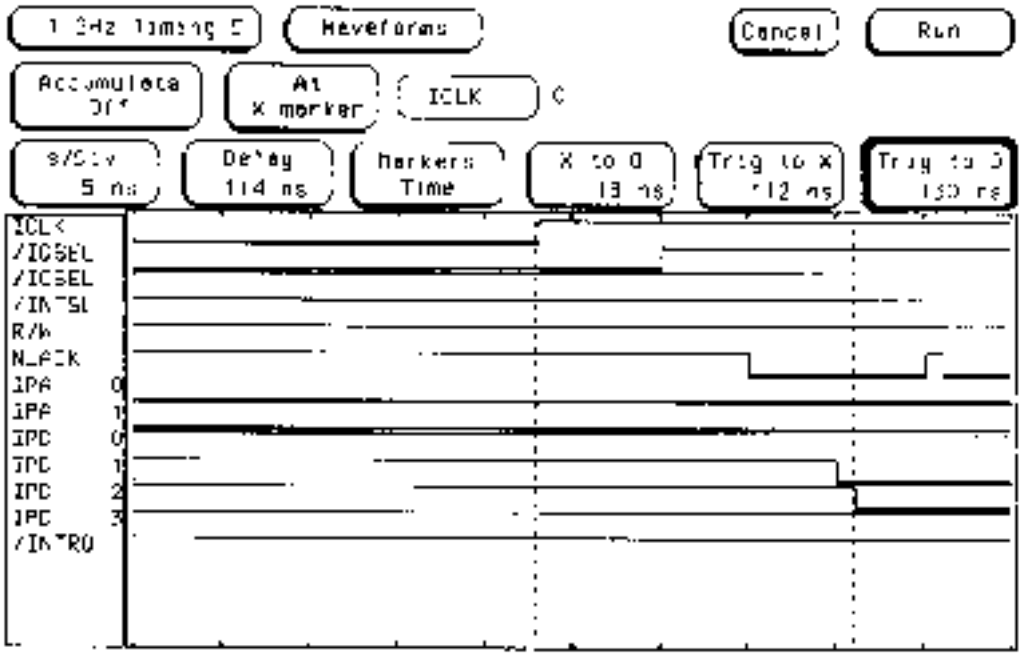


Figure 5-3 **Zoom-in View of ID Read Cycle Driving N_ACK and IPDO-3 Signals**

5.4 I/O Read Cycle

Figure 5-4 is a complete DUAL16CT I/O read cycle. The signals of interest are /IOSEL, N_ACK, and the four IPD0-3 signals. Figure 5-5 is a zoomed- in view of the DUAL16CT IO read cycle driving the N_ACK and IPD0-3 signals showing a typical response time of about 18 nanoseconds for driving these signals.

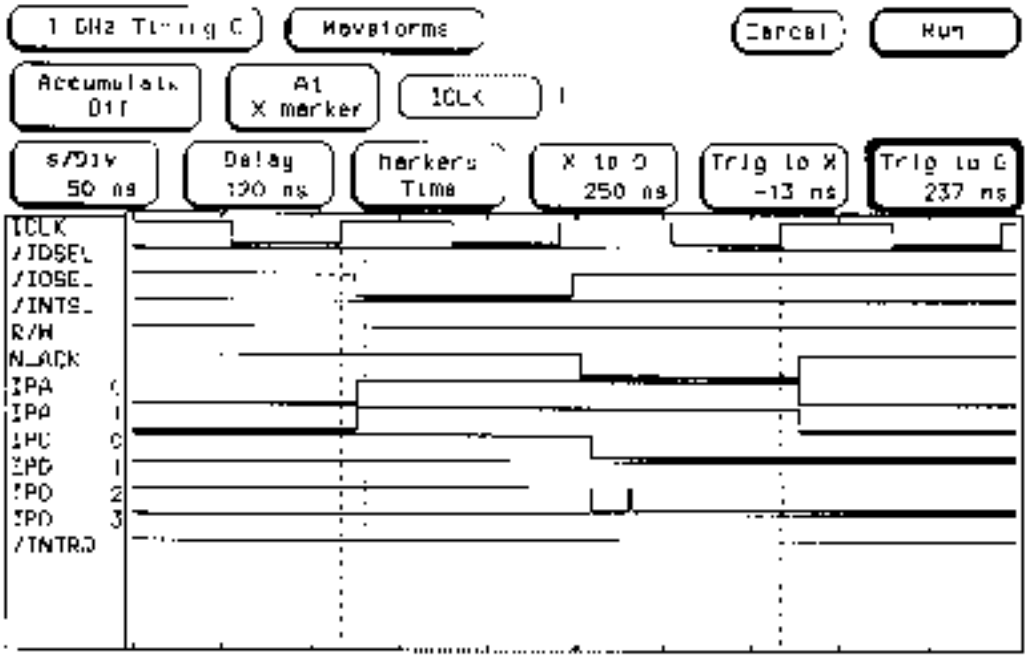


Figure 5-4 **Complete IO Read Cycle**

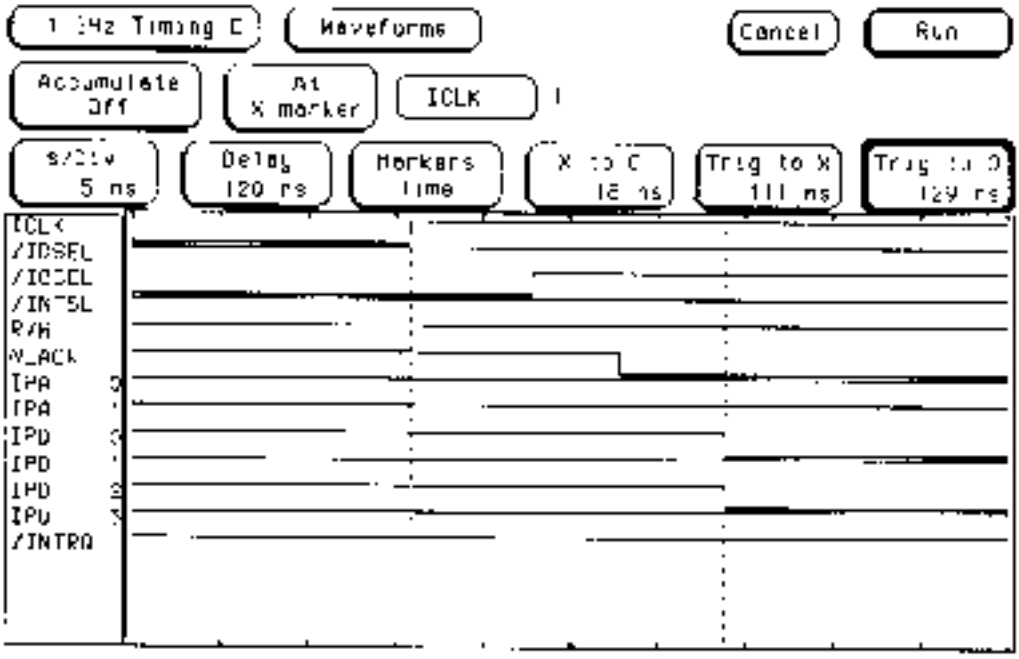


Figure 5-5 **Zoom-in view of IPO Read Cycle Driving N_ACK and IPD0-3 Signals**

5.5 Interrupt Request

Figure 5-6 shows an Interrupt Request, an IPack Interrupt Select Cycle, and later the resetting of the Interrupt Status bit..

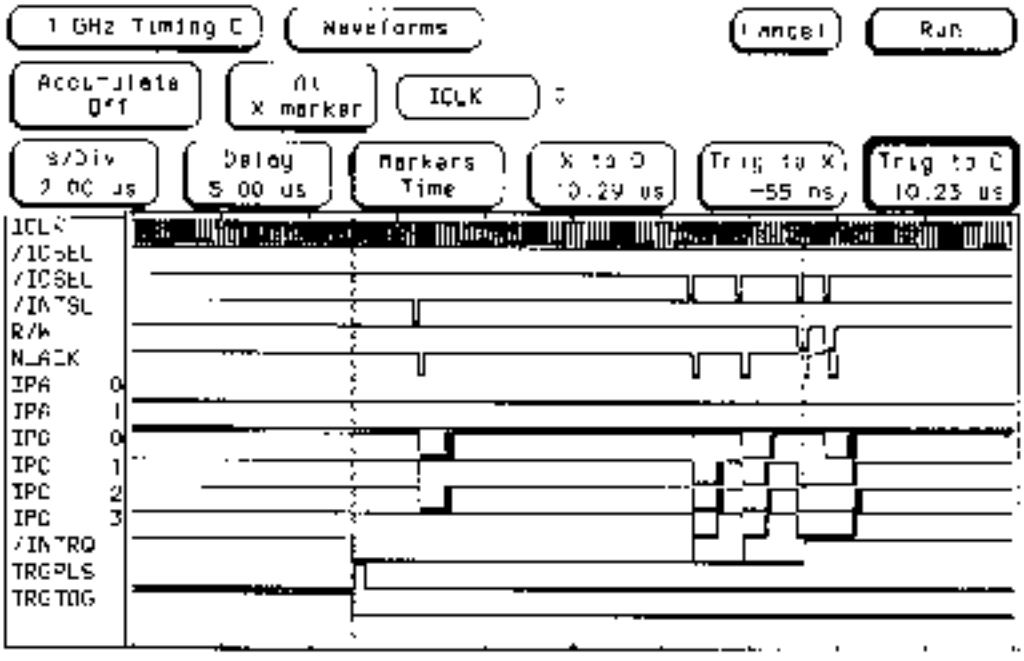


Figure 5-6 **Complete Interrupt Request and Service Routine**

5.6 OS-9 Interrupt Select Cycle

Figure 5-7 is a view of an OS-9 Interrupt Select cycle fetching the interrupt vector in less than 1.5 uSec. after the Interrupt Request signal (N_INTREQ0) was asserted

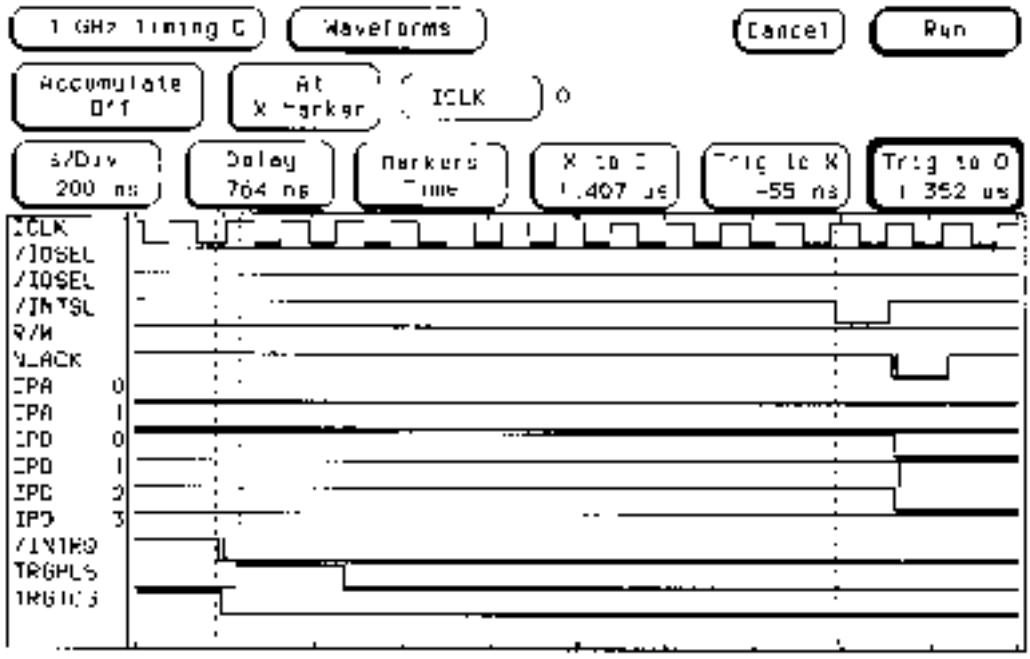


Figure 5-7 **OS-9 Responding With Interrupt Select Cycle in Less Than 1.5 µs**

5.7 TRIGPULSE Signal Asserted 40 ns

Figure 5-8 is a view of the DUAL16CT's TRIGPULSE signal asserted 40 nSec. after the terminal count and the Interrupt Request signal is reached.

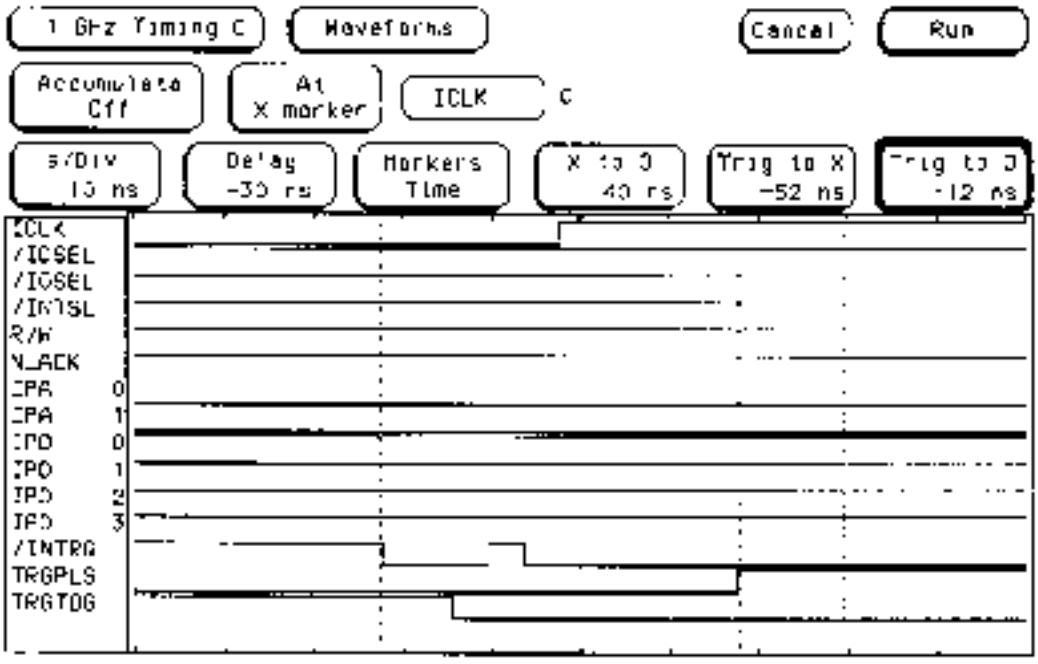


Figure 5-8 **TRIGPULSE Asserted 40 ns After Terminal Count and N_INTREQ0 is Reached**

5.8 I/O Write to Interrupt Status Register (IR0)

Figure 5-9 is a view of an I/O write to the Interrupt Status Register (IR0) reseting the the status bit and the N_INTREQ0 signal.

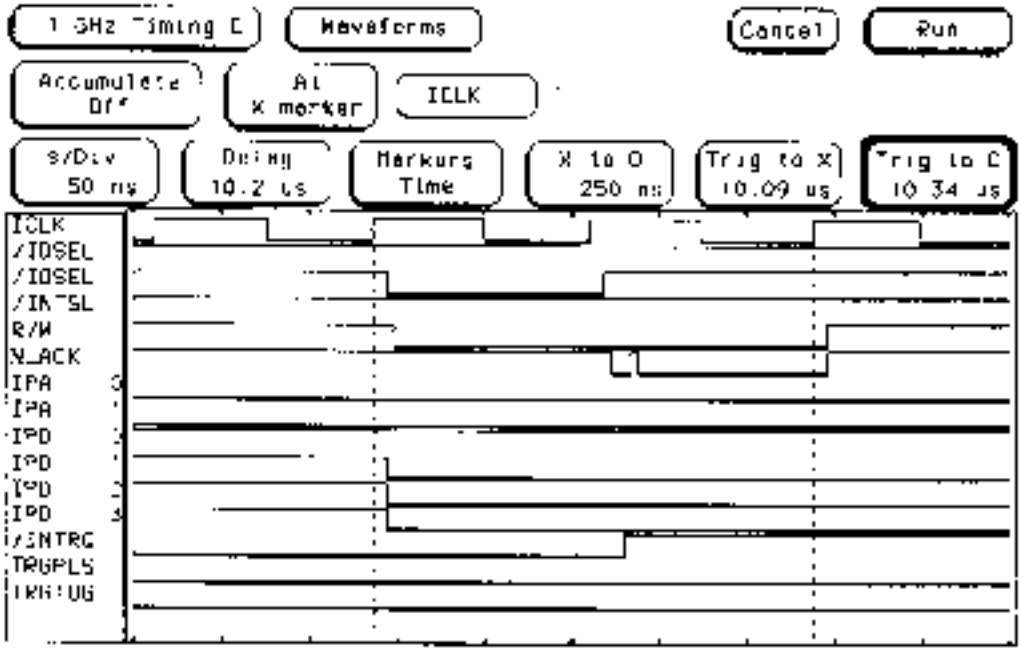


Figure 5-9 **I/O Write to the Interrupt Status Register (IRO) Resetting N_INTREQ0**

5.9 TRIGPULSE Signal Asserted (62 ns)

Figure 5-10 is a view of the DUAL16CT's TRIGPULSE signal asserted 62 nSec. after the rising edge an the External Clock signal.

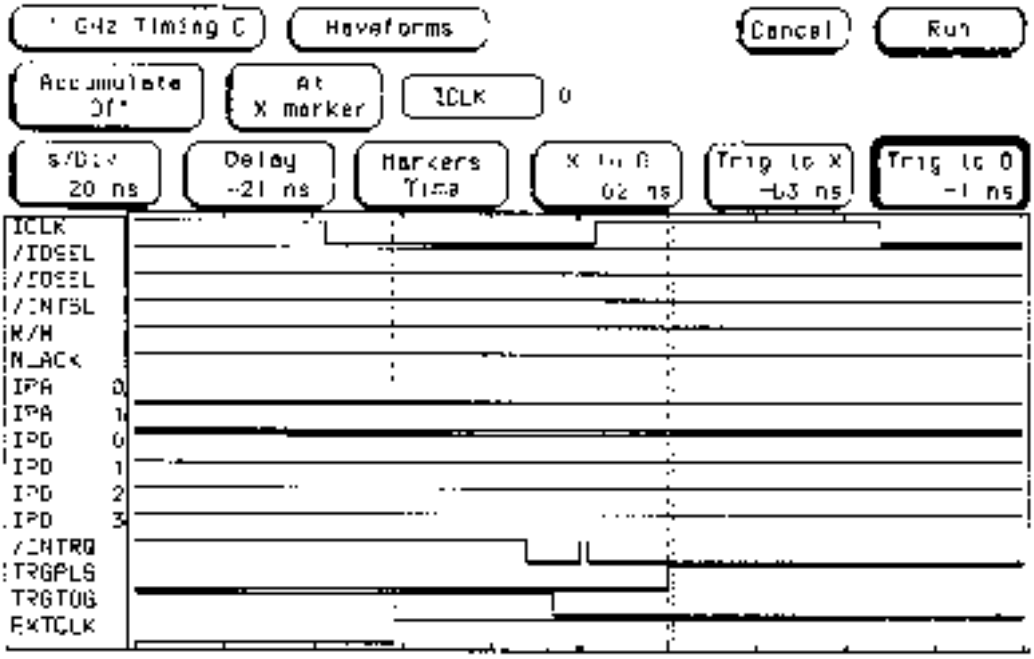


Figure 5-10 **TRIGPULSE Asserted 62 ns After rising Edge of External Clock**

6. 0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the DUAL16CT IPack to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the SYSTRAN team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and SYSTRAN reserves the right to modify submissions to provide for more generic appeal, when necessary.

The following typical applications were developed by using one or more counters on the DUAL16CT IPack. Most common configuration operations may be performed (within limits) by proper connections and software manipulations.

6.2 Variable Period Variable Pulse Width Waveform Generator Application

Figure 6-1 shows the DUAL16CT configured for a Variable Period Variable Pulse Width (VPVPW) Waveform Generator. This application example shows the hardware configuration for the programming example in section 4 of the same title.

In this example, both timers are used to generate signal pulse with a frequency of 1 Khz, and a pulse width of 15 µs on the BUSY2 output signal of timer 2 (pin 27 on the I/O connector). Timer 1 is used to control the period via the N_TRIGPULSE1 output signal (pin 11 on the I/O connector), and timer 2 is used to control the pulse width via the TIMER_EN2 input signal (pin 25 on the I/O connector). The low-going N_TRIGPULSE1 output of timer 1 is connected to the TIMER_EN2 input of timer 2.

Figure 6-2 shows the waveforms of the Trigger and Busy signals for the VPVPW example.

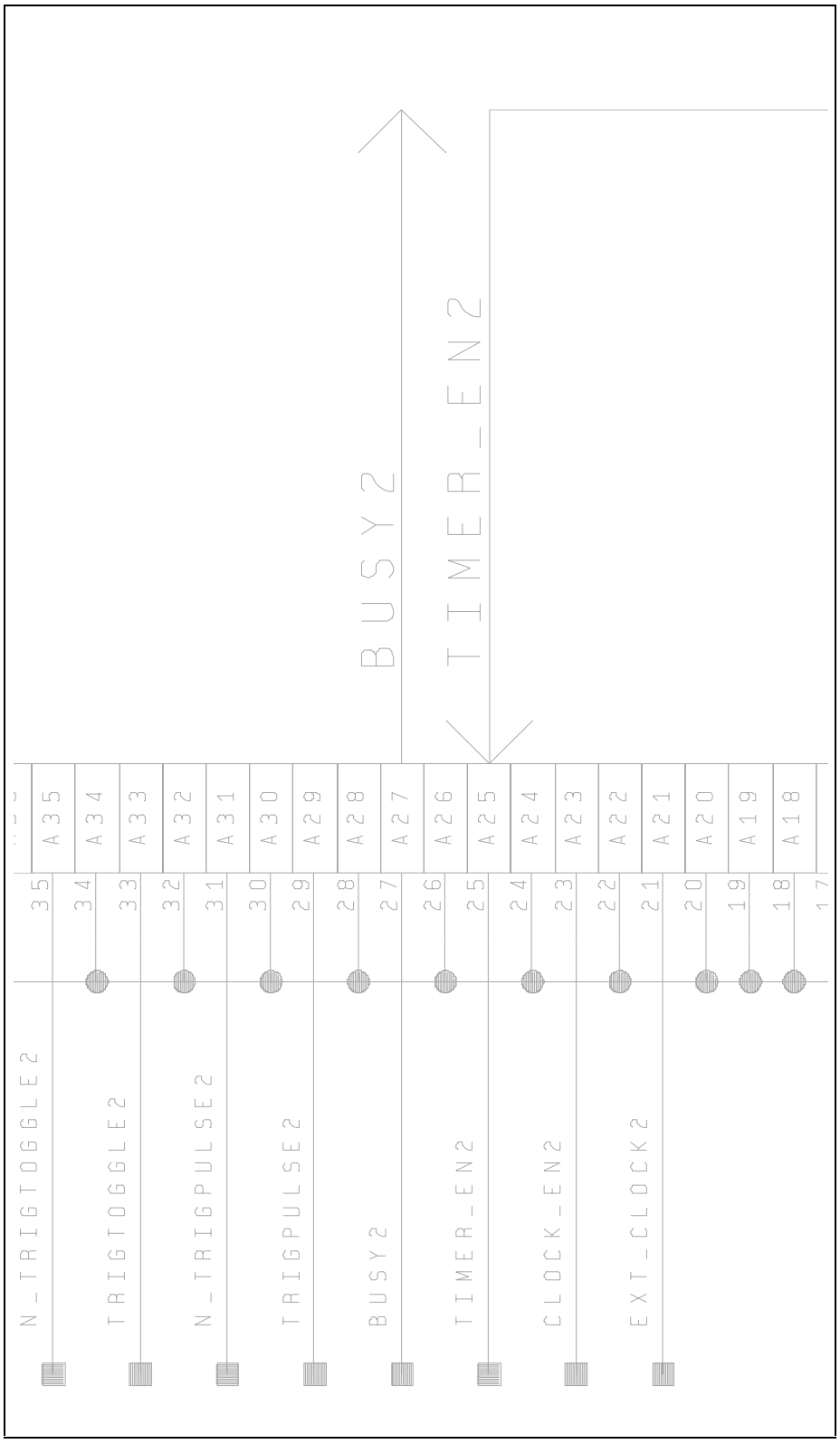


Figure 6-1 External Signal Connections for the VPVPW Application.

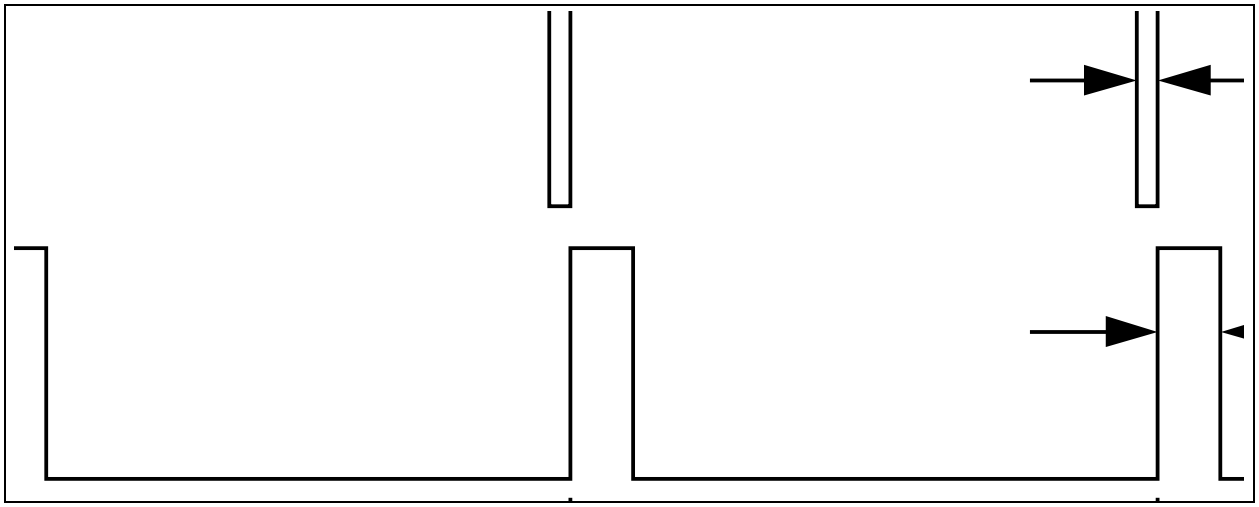


Figure 6-2 Trigger and Busy signals for the Variable Period Variable Pulse Width Example

6.3 Precision Frequency Measurement Application

Figure 6-3 shows the DUAL16CT configured for a Precision Frequency Measurement application example. This application example shows the hardware configuration for the programming example in section 4: PROGRAMMING GUIDE.

In this example, both timers are used to accurately measure the frequency of pulses. Timer 1 is used to control the time (or sample) period over which the pulses are counted. Timer 2 is used as a generic counter with the pulse signal connected to the EXT_CLOCK2 signal input (pin 21 of the I/O connector). The BUSY1 output signal of timer 1 (pin 7 of the I/O connector) is connected to the Clock-Enable input of timer 2 (pin 22 of the I/O connector) to create the sampling period.

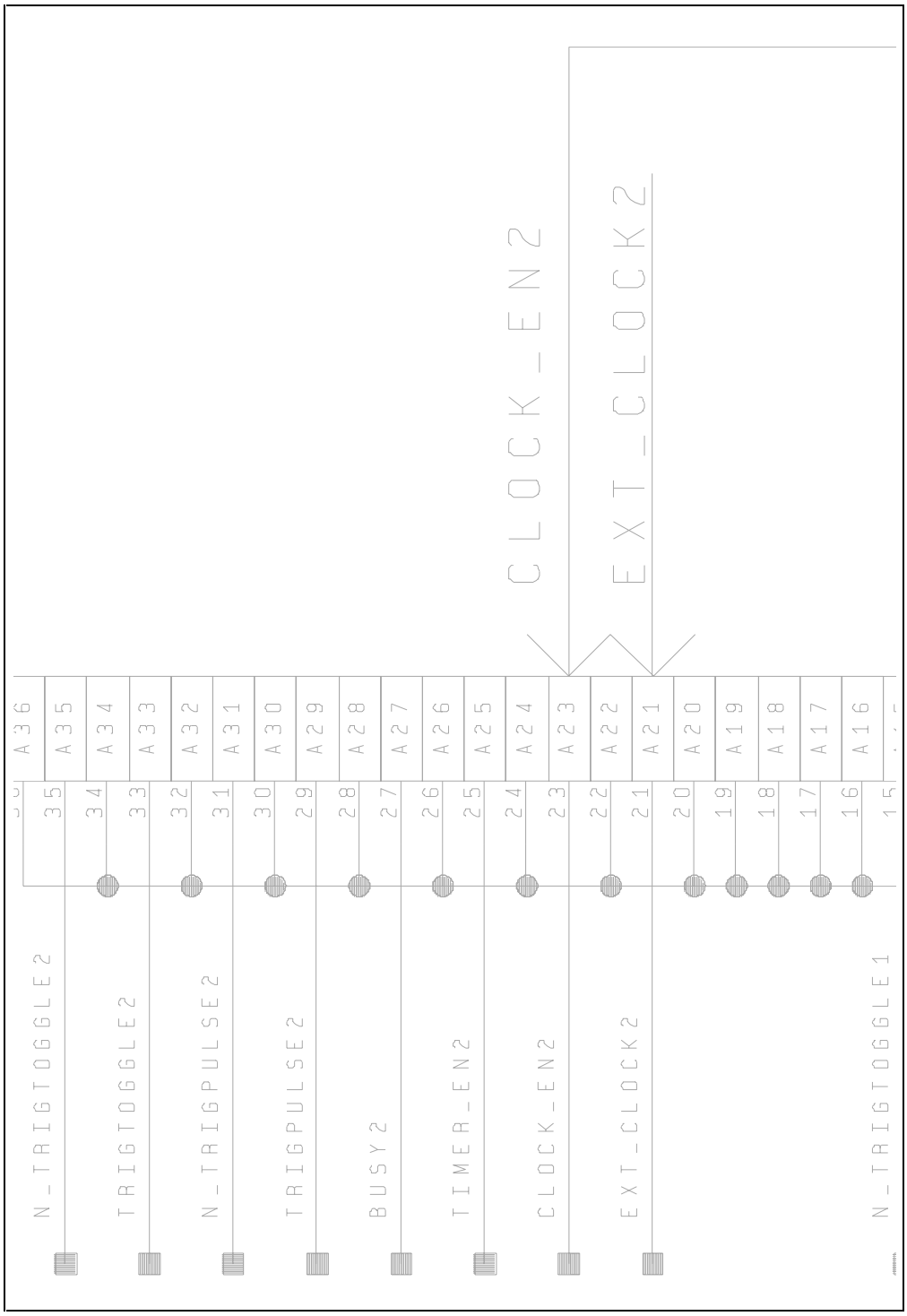


Figure 6-3 External Connections for the Precision Freq. Measurement Application

6.3.1 34-Bit Counter Application

Figure 6-4 shows the DUAL16CT configured for a 34-Bit Counter application example. This application example cascades the two counters to form a 34-bit counter.

In this example both counters are used as generic counters. Set both of them to use the external clock inputs. When the count of Counter #1 rolls over to a count of zero, the N_TRIGTOGGLE1 output signal (pin 15 of the I/O connector) goes high, clocking the EXT_CLOCK2 signal input (pin 21 of the I/O connector) as the 17th bit of Counter #1. When the count of Counter #2 rolls over to zero, the N_TRIGTOGGLE2 output signal (pin 35 of the I/O connector) goes high as the 34th bit of both counters.

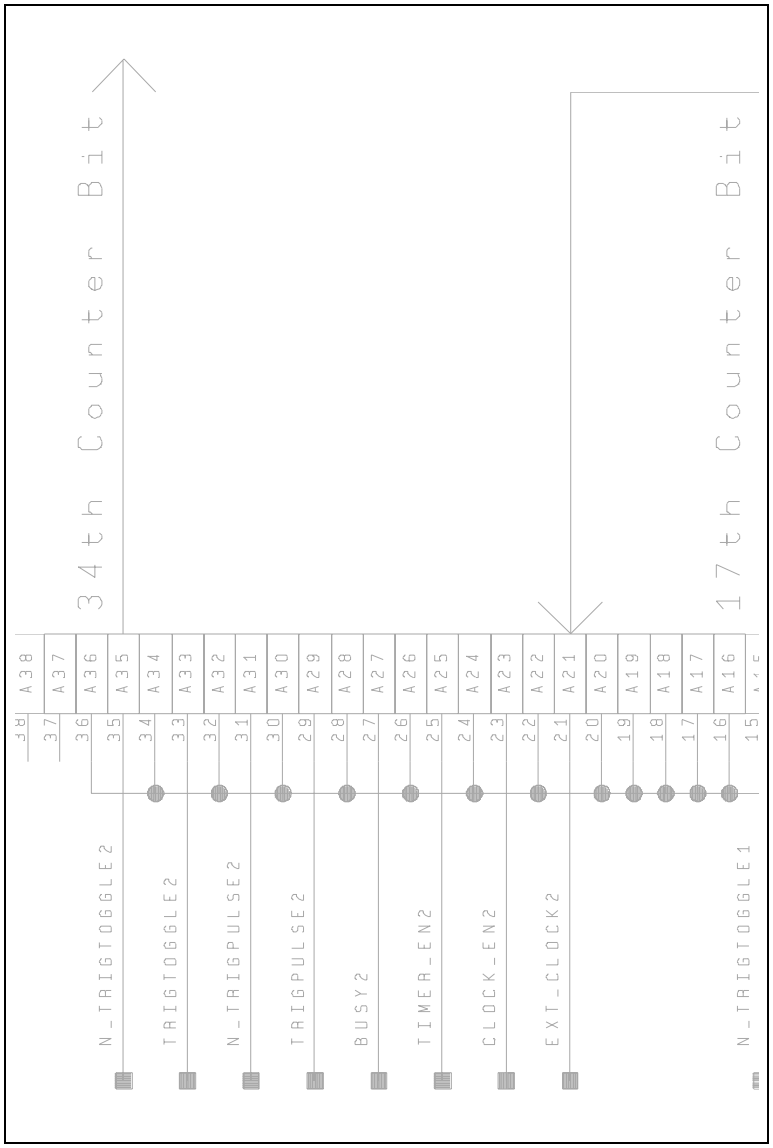


Figure 6-4 34-bit Counter Configuration

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APPENDIX A
IP Specification Synopsis

SYSTRAN CORPORATION'S

IP SPECIFICATION SYNOPSIS

of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:

This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small formfactor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general-purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high-speed (32 MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system-level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP" , and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8 MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a doublewide board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8 MHz-clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9″ by 1.8″ size allows for convenient modular placement of 1, 2, 4, 5, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME3U, Nubus, VME6U, ISA, "C" size VXIbus, and VME9U, as well as stand-alone (embedded processor) carriers of various sizes. A doublewide IP is 3.9″ by 3.6″ in size, and appears mechanically and electrically as two singlewide IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:

The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the "I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted-low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0 mA (logic low) in parallel with 30 ρF. All signals have a 10 KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK

This signal, ≡ CLK in the specification, is an 8 MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's logic connection is via pin 2. The loading is 6.0 mA (logic low) maximum in parallel with 30 ρF.

IPA[6:1] (Address bus)

These six lines, ≡ A1... A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for singlewide boards, and 32-bit data boundaries for doublewide boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as this is defined by individual select lines from the carrier.

IPD[15:0] (Data bus)

These sixteen lines, ≡ D00... D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus = IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For doublewide IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but may use IPD[15:0]. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET
This signal, ≡ RESET★ in the specification, is the asserted-low reset signal. The carrier is required to assert N_RESET for a minimum of 200 ms following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)
This signal, ≡ R/W★ in the specification, is the data-direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)
This signal, ≡ ACK★ in the specification, is the asserted-low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier-driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)
N_BS1 (high Byte Select)
These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted-low byte-select lines driven by the carrier to the IP to indicate which byte-lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low (odd) byte, IPD[7:0], while N_BS1 selects the high (even) byte, IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes, IPD[15:0], are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)
This signal, ≡ MemSel★ in the specification, is the asserted-low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. Doublewide IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)
This signal, ≡ IOSel★ in the specification, is the asserted-low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. Doublewide IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)
This signal, ≡ IntSel★ in the specification, is the asserted-low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. Doublewide IPs may respond with a-side only or b-side only transfers. A transfer involving both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)
This signal, ≡ IDSel★ in the specification, is the asserted-low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For doublewide IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)
N_INTREQ1 (INTerrupt REQuest #1)
These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are the asserted-low interrupt request signals driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each singlewide IP location. For doublewide IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:
The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin 34. Pin 36 is a reserved pin, as is pin 49. DMAEnd★ is found at pin 38. Error★ is found at pin 40; and Strobe★ is found at pin 46.

POWER/GROUND:
+5 volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero-volts reference, comes in pins 1, 25, 26, and 50; +12 volts is sourced via pin 23, and, -12 volts comes in pin 22.

CYCLE TYPES:
There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two (in the case of a doublewide IP) select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal(s). A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the (first) select cycle. Idle cycles are those between terminate and select cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:
There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:
Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both singlewide and doublewide IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:
The outside dimensions of a singlewide IP are 1.800″ by 3.900″, +.000/-.020″. The outside dimensions of a doublewide IP are 3.600″ by 3.900″ , +.000/-.020″ . There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the logic interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8″ by 3.188″ between the connectors for a singlewide IP, and 3.6″ by 3.188″ for a doublewide IP. The maximum height of components on the IP is 0.315″ , with components exceeding 0.250″ in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush-cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500 VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high-shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70° C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40° C up to +85° C.

ADDITIONAL INFORMATION:
The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 181 Constitution Drive, Menlo Park, CA 94025.

IndustryPack is a registered trademark of GreenSpring Computers, Inc.

MEMORY TRANSFERS: CYCLE TABLES

CYCLE:	MEM WRITE NO HOLDS NO WAITS			MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS						MEM WRITE 1 HOLD 3 WAITS									DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15:0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH @ END OF:			◇					◇			◇											◇					

CYCLE:	MEM READ NO HOLDS NO WAITS			MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS						MEM READ 1 HOLD 3 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15:0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND:

* IPD[15:0] = IPA[22:7] during the SELECT cycle, and is used for data for all other cycles.

X DON'T CARE

Z HIGH IMPEDANCE

1 HIGH STATE, +5v

0 LOW STATE, GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPack

◇ IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

ID TRANSFERS: CYCLE TABLES

CYCLE:	ID READ NO HOLDS NO WAITS			ID READ NO HOLDS 2 WAITS					ID READ 3 HOLDS NO WAITS					ID READ 1 HOLD 3 WAITS							ID READ 2 HOLDS 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7:0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	0	1	✓	
N_IDSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1			✓

GENERAL LEGEND:

X DON'T CARE

Z HIGH IMPEDANCE

1 HIGH STATE, +5v

0 LOW STATE, GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPack

INT TRANSFERS: CYCLE TABLES

CYCLE:	INT READ NO HOLDS NO WAITS			INT READ NO HOLDS 3 WAITS					INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS						INT READ 1 HOLD 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	TERM	IDLE	IPack	CARRIER
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	X		✓
IPD[7:0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	←	X	Z	Z	Z	←	←	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

* IPA1 CAN BE IGNORED IF ONLY ONE INTERRUPT IS SUPPORTED (must be at LEVEL 0).

** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH.

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

I/O TRANSFERS: CYCLE TABLES

CYCLE:	I/O WRITE NO HOLDS NO WAITS				I/O WRITE NO HOLDS 3 WAITS						I/O WRITE 2 HOLDS NO WAITS									I/O WRITE 3 HOLDS 1 WAIT						DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	IDLE	SELECT	WT&HLD	HOLD	HOLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPD[15:0]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1			✓
N_BS#	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X			✓
DATA LATCH @ END OF:			◇						◇			◇											◇					

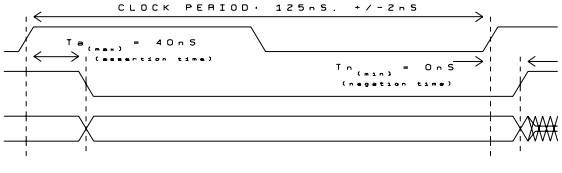
CYCLE:	I/O READ NO HOLDS NO WAITS				I/O READ NO HOLDS 2 WAITS						I/O READ 3 HOLDS NO WAITS					I/O READ 2 HOLDS 3 WAITS						I/O READ 3 HOLDS 2 WAITS						DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WT&HLD	WAIT	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15:0]	X	Z	←	X	Z	Z	Z	←	X	Z	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←	✓	
IPR/N_W	X	1	1	X	1	1	1	1	X	1	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1		✓

GENERAL LEGEND:

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE: +5v
- 0 — LOW STATE: GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPack
- ◇ — IPack LATCHES AT END OF CYCLE

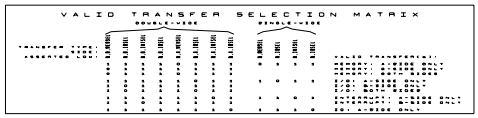
WAITS ARE INVOKED BY THE IPACK.
HOLDS ARE INVOKED BY THE CARRIER
SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

VALID TRANSFER SELECTION MATRIX



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B-T-SH-IPACKSUM-A-0-A3 (11/13/96)

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APPENDIX B

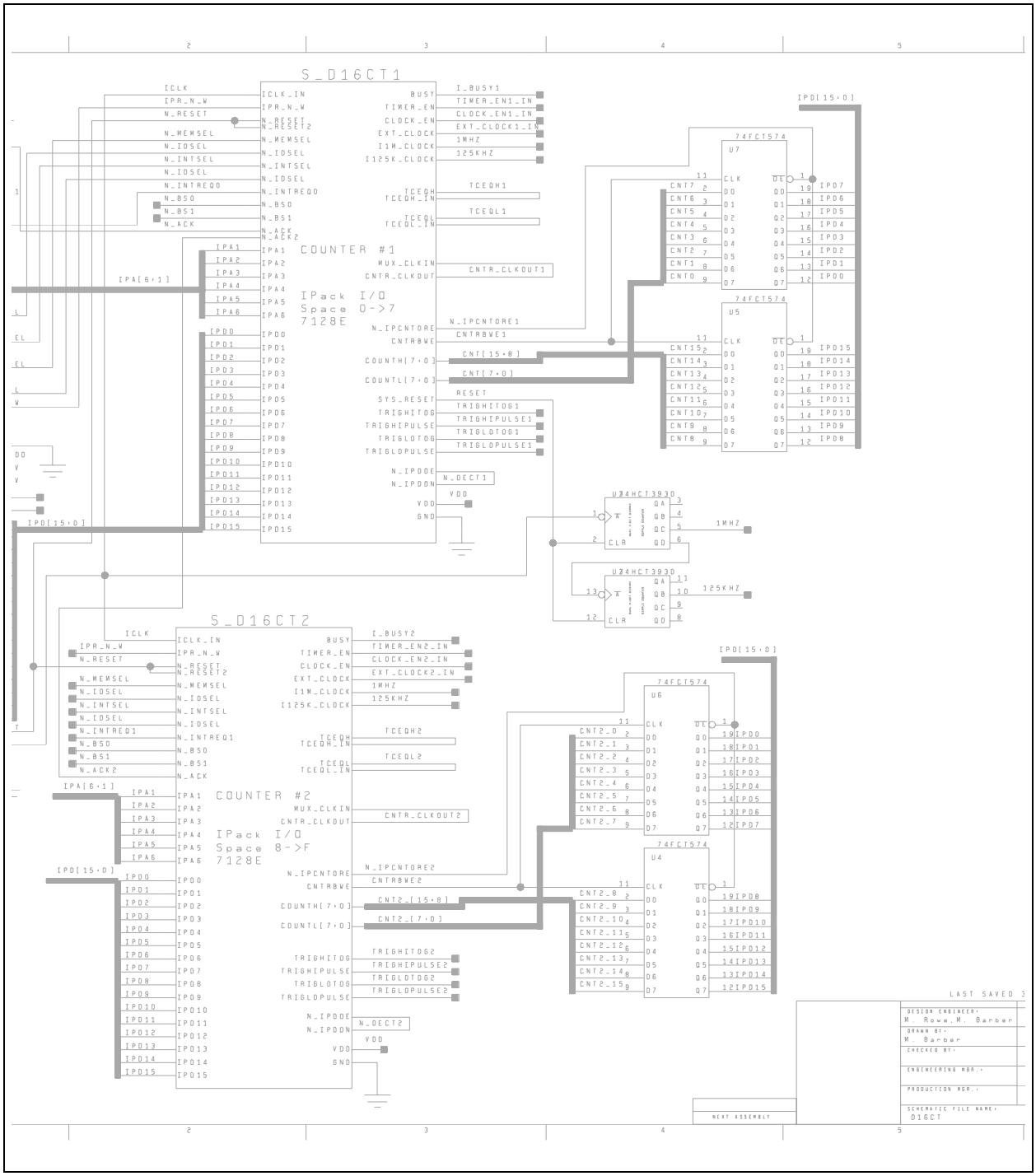


Figure B-1 Schematic #1

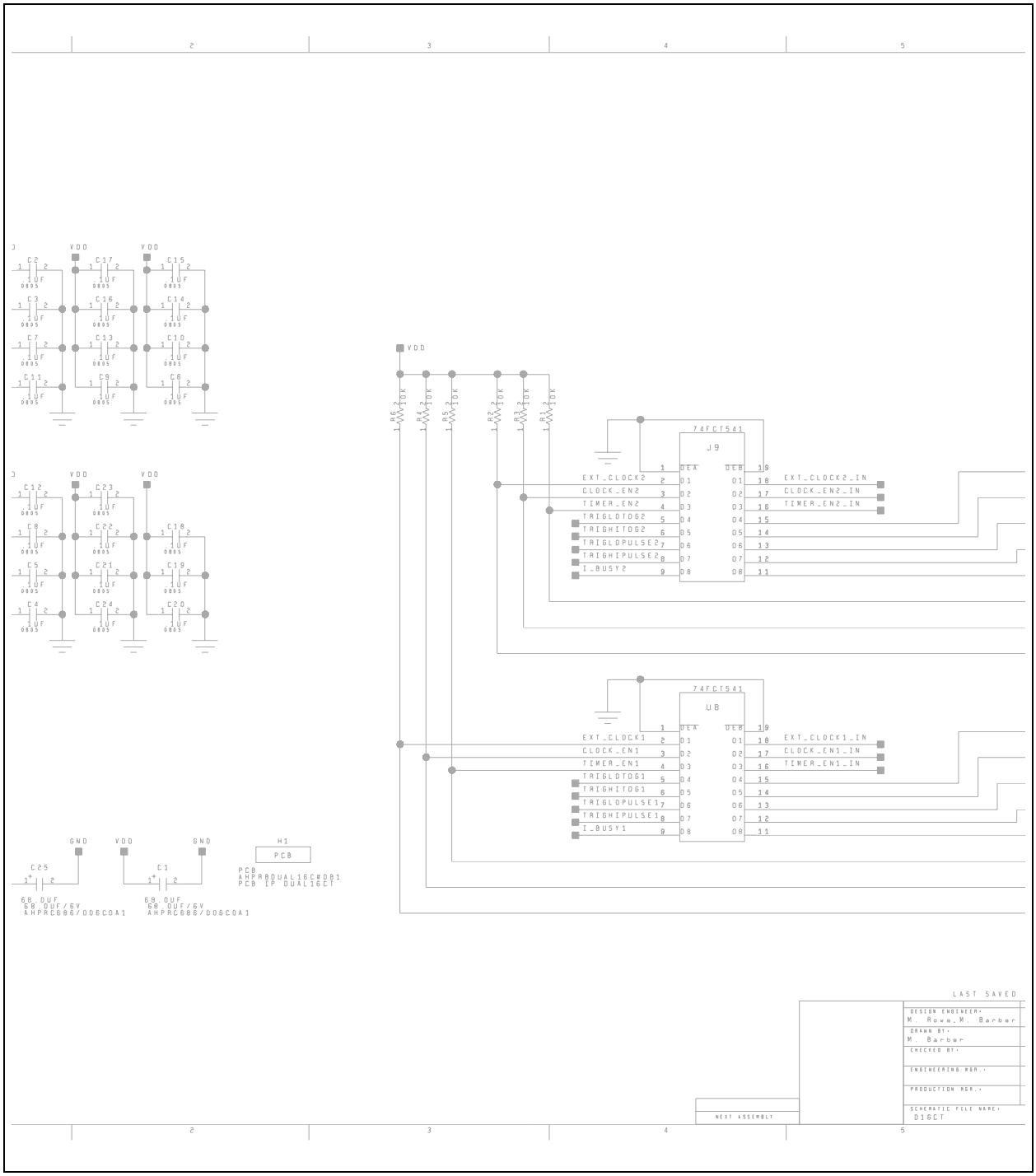


Figure B-2 Schematic #2

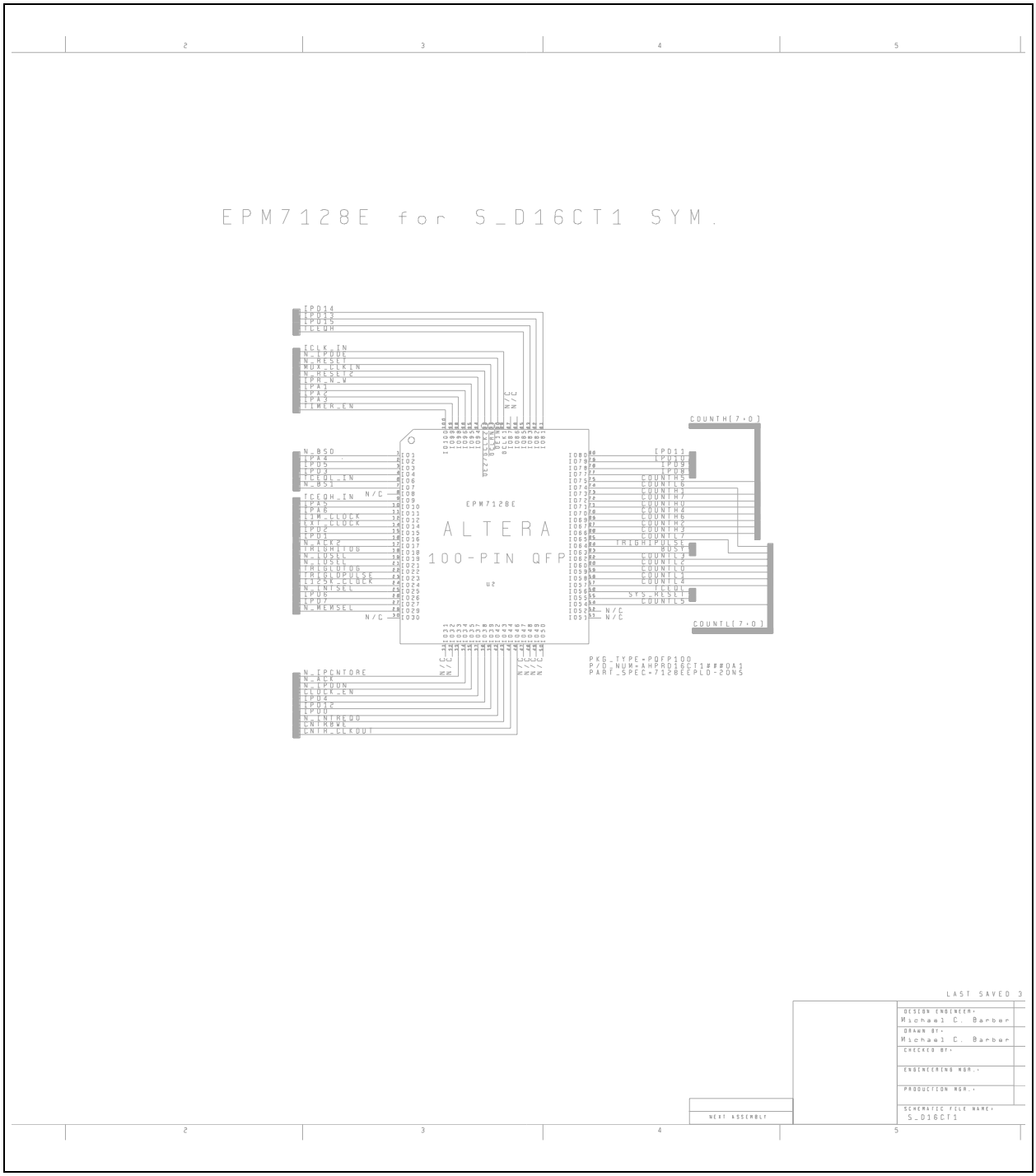


Figure B-3 Schematic #3

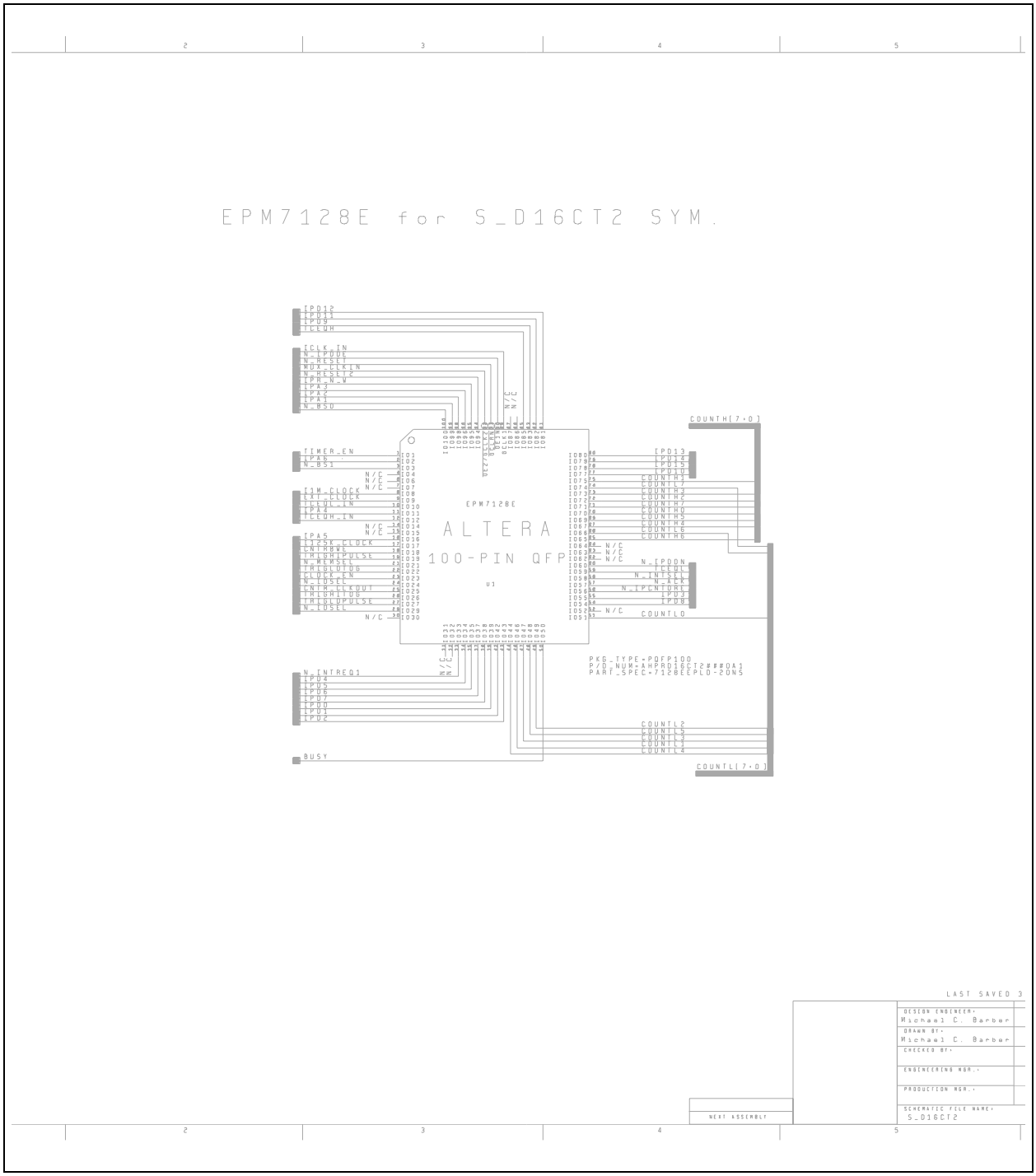


Figure B-4 Schematic #4

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