

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

DUAL32CT

Dual 32-Bit
Counter/Timer IP Module
Hardware Reference

Document No. B-T-MR-DUAL32CT-A-0-A3

FOREWORD

The information in this document has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies. Systran reserves the right to make changes without notice.

Systran makes no warranty of any kind with regard to this printed material including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose.

© Copyright 2001 Systran Corporation. All rights reserved.

Systran® is a registered trademark of Systran Corporation.

ALTERA® and Altera® are registered trademarks of Altera Corporation
HP® is a registered trademark of the Hewlett-Packard Corporation
Motorola® is a registered trademark of the Motorola Corporation.
NuBus™ is a trademark of Texas Instruments, Inc.
OS-9® is a registered trademark of Microware Systems Corporation
TRI-STATE® is a registered trademark of National Semiconductor Corporation
VIEW*logic*® is a registered trademark of Innoveda, Inc. (formerly Viewlogic Systems, Inc.)

ALTERA: Code © 2001, Systran Corporation, All Rights Reserved. The code (programs) contained in this product are proprietary to Systran Corporation and copying or other use of the bit-stream programs, except as expressly authorized by Systran Corporation, are expressly prohibited.

Any reference made within this document to equipment from other vendors does not constitute an endorsement of their product(s).

Revised: October 18, 2001

Systran Corporation
4126 Linden Avenue
Dayton, OH 45432-3068 USA
(800) 252-5601(U.S. only)
(937) 252-5601

FCC

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

As a component part of another system, this information technology product has no direct function and is therefore not subject to applicable European Union directives for Information Technology equipment.

TABLE OF CONTENTS

1. INTRODUCTION 1-1
- 1.1 How to Use This Manual 1-1
- 1.2 Scope 1-1
- 1.3 Style Conventions 1-1
- 1.4 Related Publications 1-1
- 1.5 Quality Assurance 1-1
- 1.6 Technical Support 1-2
- 1.7 Ordering Process 1-3

2. PRODUCT OVERVIEW 2-1
- 2.1 Overview 2-1
  - 2.1.1 Features 2-1
- 2.2 Block Diagram Description 2-2
- 2.3 Detailed Description 2-3
  - 2.3.1 Components 2-3
  - 2.3.2 Signal Descriptions 2-4
  - 2.3.3 Cleaning 2-5

3. INSTALLATION 3-1
- 3.1 Unpack the DUAL32CT 3-1
- 3.2 Visually Inspect the DUAL32CT 3-1
- 3.3 Install the DUAL32CT 3-1

4. PERFORMANCE 4-1
- 4.1 Overview 4-1
- 4.2 State Timing Diagram 4-1
  - 4.2.1 ID Read Cycle 4-2
  - 4.2.2 I/O Read Cycle 4-3
  - 4.2.3 Interrupt Request 4-4
  - 4.2.4 OS-9 Interrupt Select Cycle 4-5
  - 4.2.5 TRIGPULSE Signal Asserted (100 ns) 4-6
  - 4.2.6 I/O Write To Interrupt Status Register (IR0) 4-7
  - 4.2.7 TRIGPULSE Signal Asserted (122 ns) 4-8

APPENDICES

APPENDIX A – SPECIFICATIONS A-1
APPENDIX B – TYPICAL APPLICATIONS B-1
APPENDIX C – PROGRAMMING GUIDE C-1
GLOSSARY GLOSSARY-1
INDEX INDEX-1

FIGURES

Figure 2-1 DUAL32CT Board....2-1
Figure 2-2 DUAL32CT Block Diagram....2-2
Figure 3-1 Installation of the DUAL32CT on a VME Carrier Board....3-2
Figure 3-2 Installation of the DUAL32CT on an ISA Carrier Board....3-2
Figure 4-1 IP Module Test Configuration for Oscilloscope and State Timing Measurements....4-1
Figure 4-2 Complete ID Read Cycle....4-2
Figure 4-3 Zoom-In View of ID Read Cycle Driving N_ACK and IPD0-3 Signals....4-2
Figure 4-4 Complete I/O Read Cycle....4-3
Figure 4-5 Zoom-In View of I/O Read Cycle Driving N_ACK and IPD0-3 Signals....4-3
Figure 4-6 Complete Interrupt Request and Service Routine....4-4
Figure 4-7 OS-9 Responding With Interrupt Select Cycle in Less Than 1.5 µs....4-5
Figure 4-8 TRIGPULSE Asserted 100 ns After Reaching Terminal Count and Generating N_INTREQ0....4-6
Figure 4-9 I/O Write to the Interrupt Status Register (IR0) Resetting N_INTREQ0....4-7
Figure 4-10 TRIGPULSE Asserted 122 ns After Rising Edge of External Clock....4-8

TABLES

Table 2-1 I/O Signals for Each DUAL32CT Counter....2-4
Table 3-1 DUAL32CT Shipping Package contents....3-1
Table 3-2 DUAL32CT Installation Tools....3-1
Table 3-3 IP Module Logic Bus Pin Assignments....3-3
Table 3-4 IP Module I/O Connector Pin Assignments....3-4

1. INTRODUCTION

1.1 How to Use This Manual

This is a reference manual for Systran's Dual 32-bit Counter/Timer IP Module board, referred to in this manual as the DUAL32CT (Two independent 32-bit counters), part number BHAS-DUAL32CT.

1.2 Scope

This manual covers the physical and operational description of the DUAL32CT, from both hardware and software perspectives. This manual also contains detailed technical information about the DUAL32CT's performance characteristics, and a few typical applications. You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IP Modules on your carrier(s) to effectively use this manual.

1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*
- Data types are italicized. For example, *int*
- Function parameters are bolded. For example, **Action**
- Path names are italicized. For example, *utility/sw/cfg*
- File names are bolded. For example, **config.c**
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***
- Hexadecimal values are written with a "0x" precfix. For example, 0x7e
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/). For example, /SYNC
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded.

```
ls
file1           file2               file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.4 Related Publications

- Systran *DUAL32CT Software Library Manual* (Doc. No. B-T-ML-DUAL32CT).
- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Module Bus Onboard the Motorola MVME162 Controller*.
- *ANSI/VITA 4-1995* published by VMEbus International Trade Association, 7825 Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA.

1.5 Quality Assurance

Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product

delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.6 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: support@systran.com
- Fax: (937) 252-1349
- World Wide Web address: www.systran.com

1.7 Ordering Process

To learn more about Systran products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: info@systran.com
- World Wide Web address: www.systran.com

This page intentionally left blank

2. PRODUCT OVERVIEW

2.1 Overview

The DUAL32CT is a singlewide IP Module board, conforming both mechanically and electrically to American National Standard for IP Modules (*ANSI/VITA 4-1995*) specification. The DUAL32CT board provides two easy, completely independent 32-bit upcounters or timers. Each counter/timer has nine 16-bit registers that determine its configuration and operation: two data, one control, one configuration, two terminal count, and three interrupt related. The board is a counter when using the external clock, and a timer when using one of the internal clock frequencies.

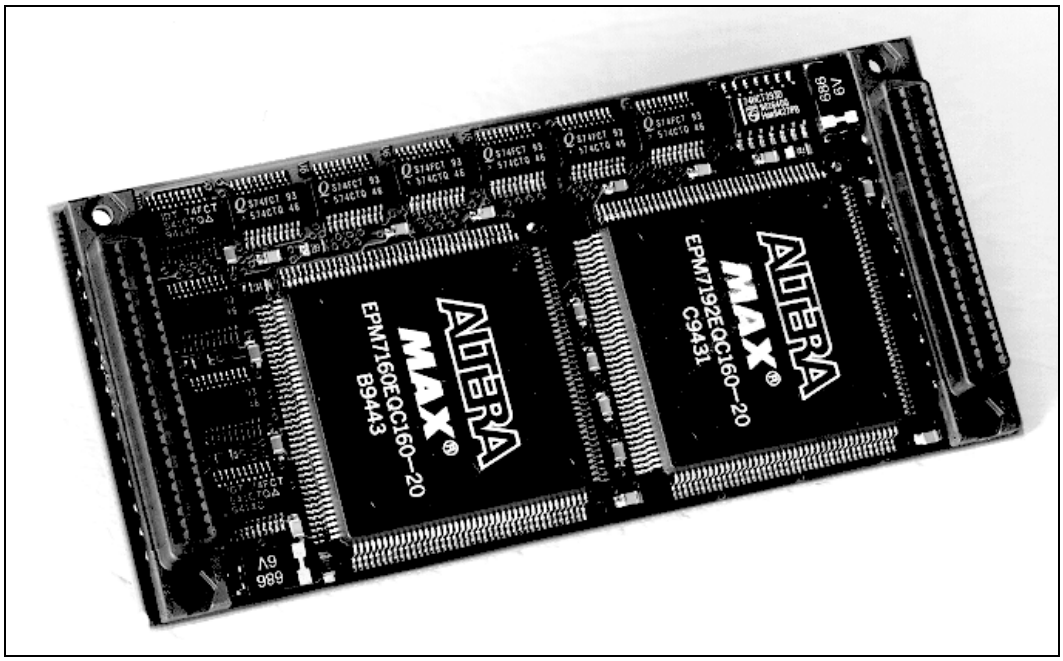


Figure 2-1 DUAL32CT Board

2.1.1 Features

- Concise, intuitive register set for easy programming
- Gatable internal clocks at 8 MHz, 1 MHz, and 125 KHz or external clocks up to 25 MHz with terminal count, or up to 50 MHz as a totalizer
- Terminal count detect programmable via terminal count registers
- Rollover or Stop on terminal count
- Interrupt-on terminal count
- Trigger-outputs on terminal count (high and low pulses, or state toggle)
- True latched on-the-fly reading of count value (no re-read checking necessary)
- Timer enable, clock enable, and counter reset control via software or I/O signals for multiple-timer applications

2.2 Block Diagram Description

Figure 2-2 is a simplified block diagram of the DUAL32CT representing the signal flow between the IP Module Bus and the I/O connectors. On the left side of the diagram is the IP Module Bus connector through which all transfers between the IP Module carrier and the DUAL32CT's registers and data sources are conducted. The blocks labeled "Counter #1 and Counter #2" contain all of the ID PROM data, and IP Module transfer sequence/control and data bus interface logic, along with each 32-bit counter, terminal count comparators, and clock multiplexers for each counter. These blocks of circuitry are completely implemented with two EPLD devices. The blocks labeled "Counter IP Module Readback Register" consist of four octal read-back data registers per counter. The block labeled "Clock Divider" divides down the 8 MHz IP Module clock to generate the 1 MHz and 125 KHz internal clocks. All of the control and external clock signals of both counters are buffered to the far-right block labeled "IP Module I/O Connector".

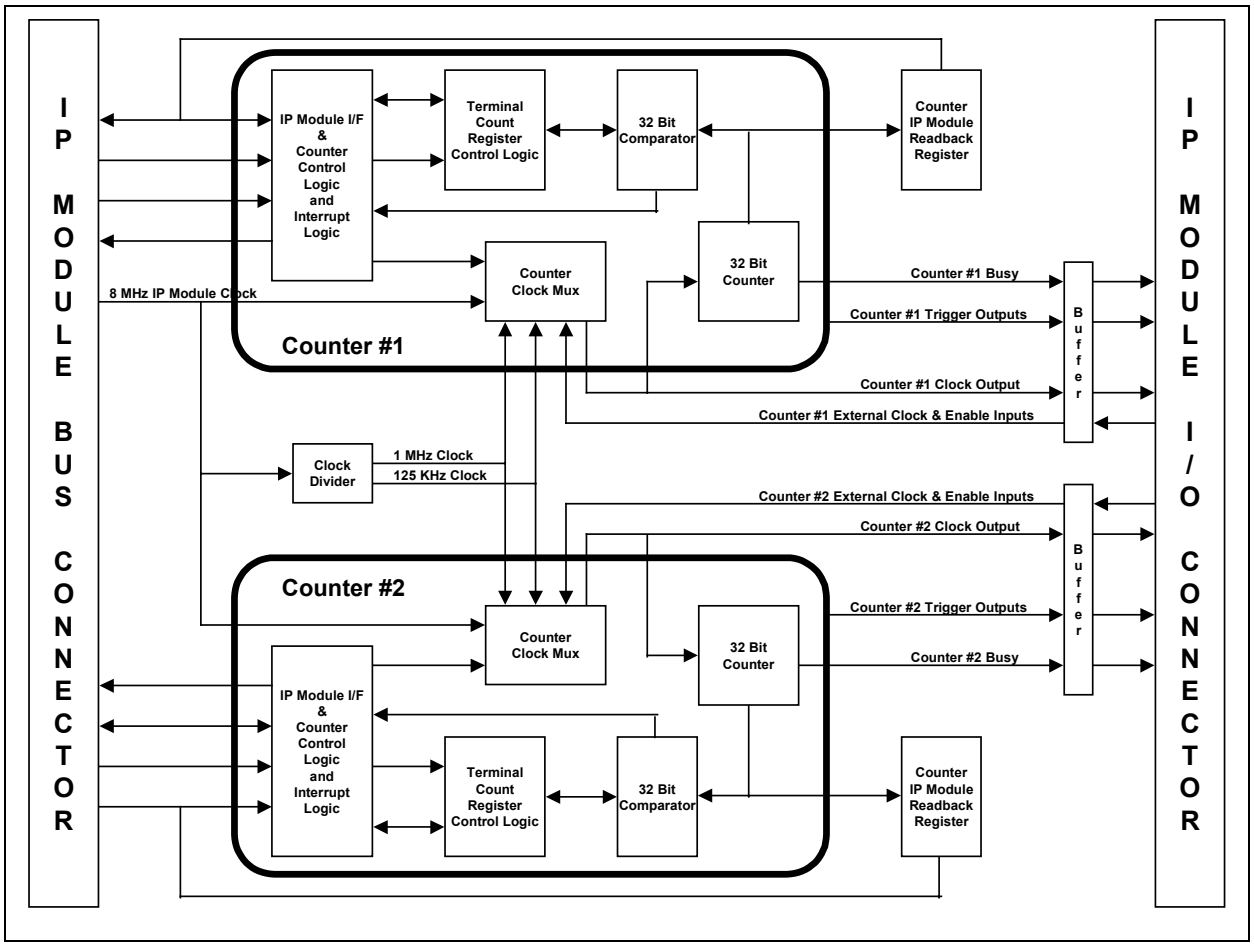


Figure 2-2 DUAL32CT Block Diagram

NOTE: You can access the count value while the counter is running by reading the MSW then the LSW data registers via normal I/O read cycles. When you read the MSW data register, the entire 32-bit count value is latched into the MSW and LSW data registers for an instantaneous snapshot of the count value. When you read the LSW data register, the latches are released.

2.3 Detailed Description

The DUAL32CT was developed using VHDL and Synthesis, and was targeted to Altera EPLDs. The design was schematic-captured and integrated into standard logic devices, connectors, and discrete components using Viewdraw by VIEWlogic and associated packages. This top-down design methodology is evident in the product design material in this document.

2.3.1 Components

IP MODULE BUS CONNECTOR

All IP Module bus transfers occur across J1, the IP Module Connector, located on the left side of the block diagram (Figure 2-2). This IP Module does not support DMA and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and writes to the I/O map.

PRIMARY ACTIVITY CONTROLLER

The DUAL32CT's primary activity controller is housed within the EPM7160EQC160 EPLDs. The controller serves as the primary IP Module transfer sequence engine, with the following responsibilities:

- Detect valid I/O and ID transfer operations within their respective fully-decoded address ranges, including the support of HOLD cycles when generated by a carrier
- Generate ID PROM emulation data patterns for ID read transfers
- I/O write registration and read gating of the data/control register information

At power-up or any other form of "reset" operation, all of the I/O registers are cleared or reset, thereby clearing the counters and disabling them until specifically manipulated by an I/O write transfer.

COUNTER READ-BACK REGISTERS

The 74FCT574s are the counter read-back registers located at U2, 5, 6, and 7 for Counter #1, and U8, 9, 11, and 12 for Counter #2. They register the counter's data and drive the IP Module data bus. U1 is a 74HCT393D and divides down the 8 MHz ICLK signal to provide the 1 MHz and 125 KHz internal clock frequencies to each counter in U3 and U7.

BUFFERS

The 74FCT541 buffers (U10 and U13), buffer the output trigger and busy signals along with squaring up the input external clock, clock-enable and timer-enable signals for each counter to the user's I/O connector (J2).

2.3.2 Signal Descriptions

The following table shows the signal lines available at the I/O connector for each DUAL32CT counter:

Table 2-1 I/O Signals for Each DUAL32CT Counter

Signal Name	Type	Signal Description
TIMER_EN(1,2)	Input	This is an external timer-enable input (logic high=timer enable, logic low=disable). This signal, in conjunction with the Timer-Enable bit in the control register, enables (run mode)/disables (setup mode) the timer. You may also asynchronously reset the timer by toggling this signal low, then high. You may drive this signal by the output of another timer for multi-timer applications such as variable period and variable duty-cycle pulse generation. This signal is pulled-up so the timer is enabled if there is no connection.
EXT_CLOCK(1,2)	Input	This is the external clock input for each counter. The counter counts on the rising edge of the clock.
CLOCK_EN(1,2)	Input	This is an external clock enable/disable signal (logic high=enable, logic low=disable). This signal, in conjunction with the Clock- Enable bit in the control register, enables/disables the clock. The Clock-Enable bit must be set for this signal to enable the clock. This signal is pulled-up so the clock is enabled if there is no connection.
Trigpulse (1,2)	Output	This trigger signal powers up low then drives high for ~250 ns when each terminal count is reached.
Trigtoggle (1,2)	Output	This trigger signal powers up (or after a counter or system reset) high then toggles low when the terminal count is reached, then toggling state with each terminal count.
N_Trigpulse (1,2)	Output	This trigger signal powers up high then drives low for ~250 ns when each terminal count is reached.
N_Trigtoggle (1,2)	Output	This trigger signal powers up (or after a counter or system reset) low then toggles high when the terminal count is reached, then toggling state with each terminal count.
Busy(1,2)	Output	This signal is high when the counter/timer is counting, and low when the counter/timer is idle. This signal is provided for multi-counter/timer applications such as frequency measurement.

2.3.3 Cleaning

In the unlikely event that this product requires cleaning after delivery, most solvents that are based on Fluorine, Chlorine, Aqueous, and Alcohol are safe to use.



CAUTION: Do NOT use gasoline or thinner type solvents to clean this product.

This page intentionally left blank

3. INSTALLATION

3.1 Unpack the DUAL32CT

Table 3-1 lists the contents of the DUAL32CT shipping package.

Table 3-1 DUAL32CT Shipping Package contents

Qty	Description
1	DUAL32CT Printed Circuit Assembly
1	DUAL32CT Hardware Reference*

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case you need to return the board.

* One manual is shipped for each board ordered. You may purchase extra manuals by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR-DUAL32CT).

3.2 Visually Inspect the DUAL32CT

Inspect the DUAL32CT to determine if any damage occurred during shipping.

3.3 Install the DUAL32CT

The DUAL32CT installation requires the tools listed in Table 3-2.



NOTE: The DUAL32CT is an Electrostatic Sensitive Device (ESD). Install the DUAL32CT on an anti-static workbench to protect the IP Modules and the host carrier board.

Table 3-2 DUAL32CT Installation Tools

Qty	Description
1	ESD static control kit/ground strap/etc.
1	Standard flat-head screwdriver (optional)

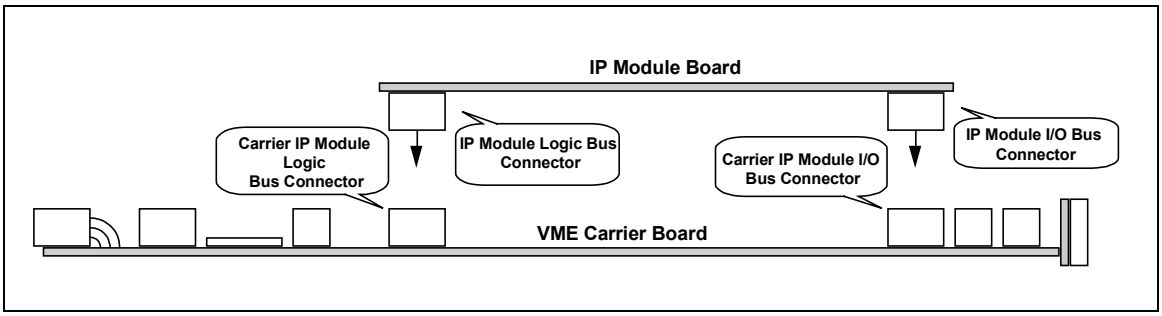


Figure 3-1 Installation of the DUAL32CT on a VME Carrier Board

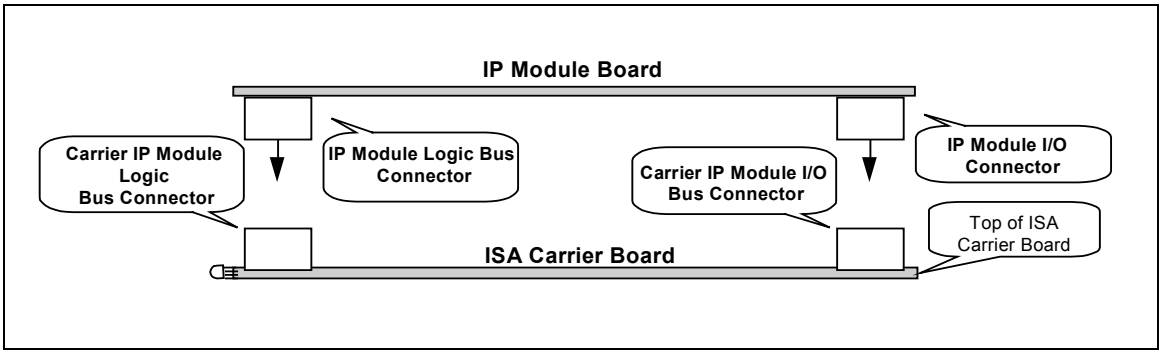


Figure 3-2 Installation of the DUAL32CT on an ISA Carrier Board

Figure 3-1 shows how to install the DUAL32CT on a VME IP Module carrier, and Figure 3-2 shows how to install the board on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are the original IP Module signal names, and the signals on the right are the Systran signal names.

Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board hardware reference manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. An asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD-controlled area where you can install the DUAL32CT.
3. Remove the DUAL32CT from the shipping package and place it on the anti-static mat.
4. Install the DUAL32CT onto the carrier board by applying adequate and equal pressure to the DUAL32CT board at both ends.

*5. Install four M2x5mm flat head machine screws onto the carrier's IP Module connectors.

This completes the installation of the DUAL32CT to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signal Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Name
50	GND
49	Not Used
48	Not Used
47	Not Used
46	Not Used
45	Not Used
44	Not Used
43	Not Used
42	Not Used
41	Not Used
40	Not Used
39	Not Used
38	Not Used
37	Not Used
36	GND
34	GND
33	TRIGTOGGLE2
32	GND
31	N_TRIGPULSE2
30	GND
29	TRIGPULSE2
28	GND
27	BUSY2
26	GND
25	TIMER_EN2
24	GND
23	CLOCK_EN2
22	GND
21	EXT_CLOCK2
20	GND
19	GND
18	GND
17	GND
16	GND
15	N_TRIGTOGGLE1
14	GND
13	TRIGTOGGLE1
12	GND
11	N_TRIGPULSE1
10	GND
9	TRIGPULSE1
8	GND
7	BUSY1
6	GND
5	TIMER_EN1
4	GND
3	CLOCK_EN1
2	GND
1	EXT_CLOCK1

4. PERFORMANCE

4.1 Overview

This section provides several sets of empirical data that present typical performance parameters beyond what we provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Appendix A.

4.2 State Timing Diagram

The state waveforms for Figures 4-2 through 4-10 were made using the HP 1-GHz Timing Master Module and the Systran IP Module Logic Bus Extender (IPLBE) with the IP Module Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer's screen are active low, and are represented by a '/' as the first character as opposed to the 'N'_used elsewhere, due to the limited amount of character spacing.

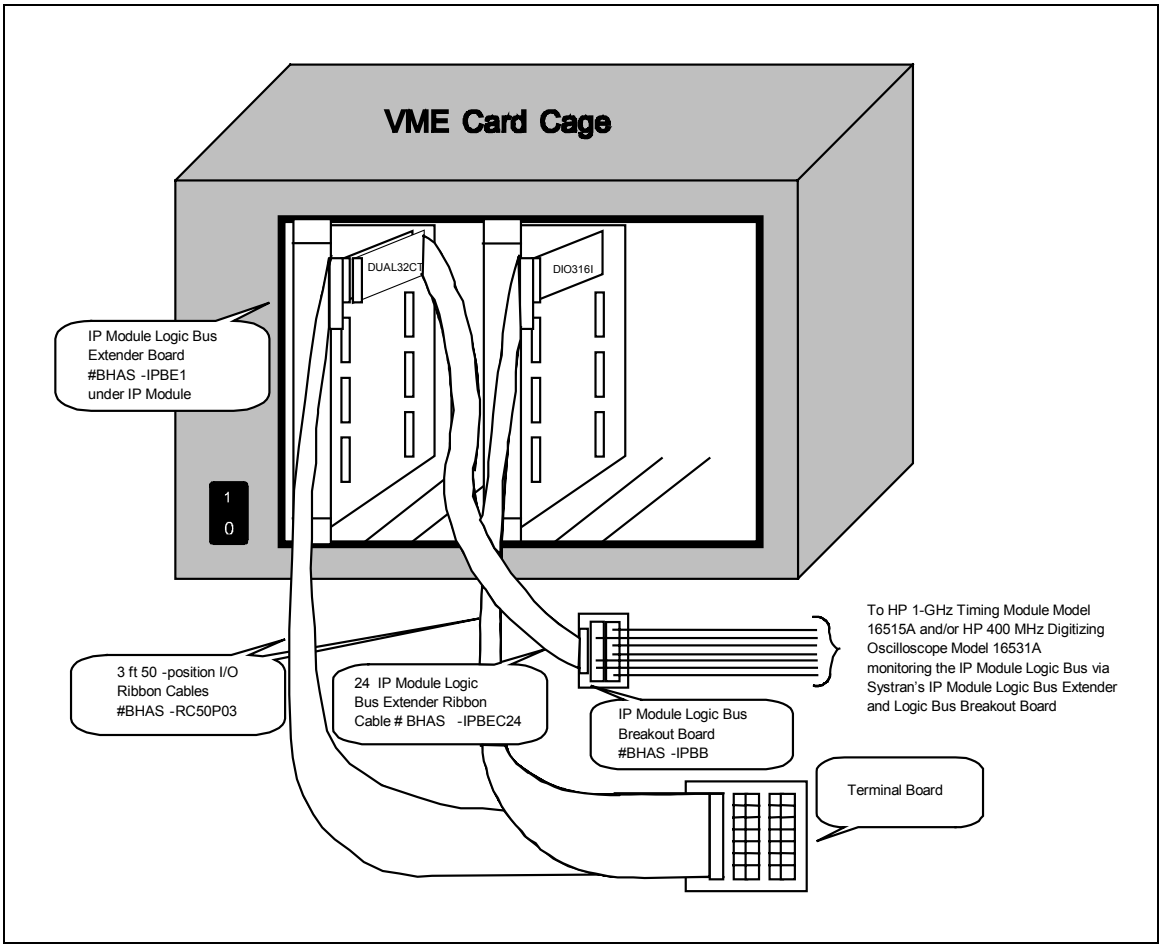


Figure 4-1 IP Module Test Configuration for Oscilloscope and State Timing Measurements

4.2.1 ID Read Cycle

Figure 4-2 is a complete DUAL32CT ID read cycle. The signals of interest are /IDSEL, N_ACK, and the four IPD0-3 signals. Figure 4-3 is a zoomed-in view of the DUAL32CT ID cycle driving the N_ACK and IPD0-3 signals showing a typical response time of about 18 ns for driving these signals.

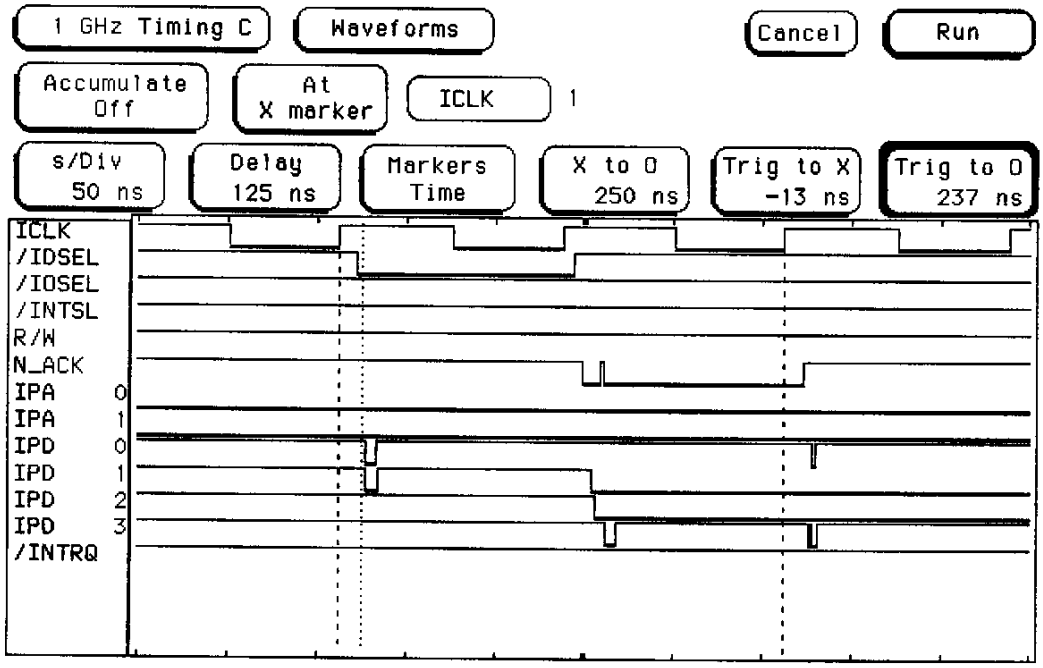


Figure 4-2 Complete ID Read Cycle

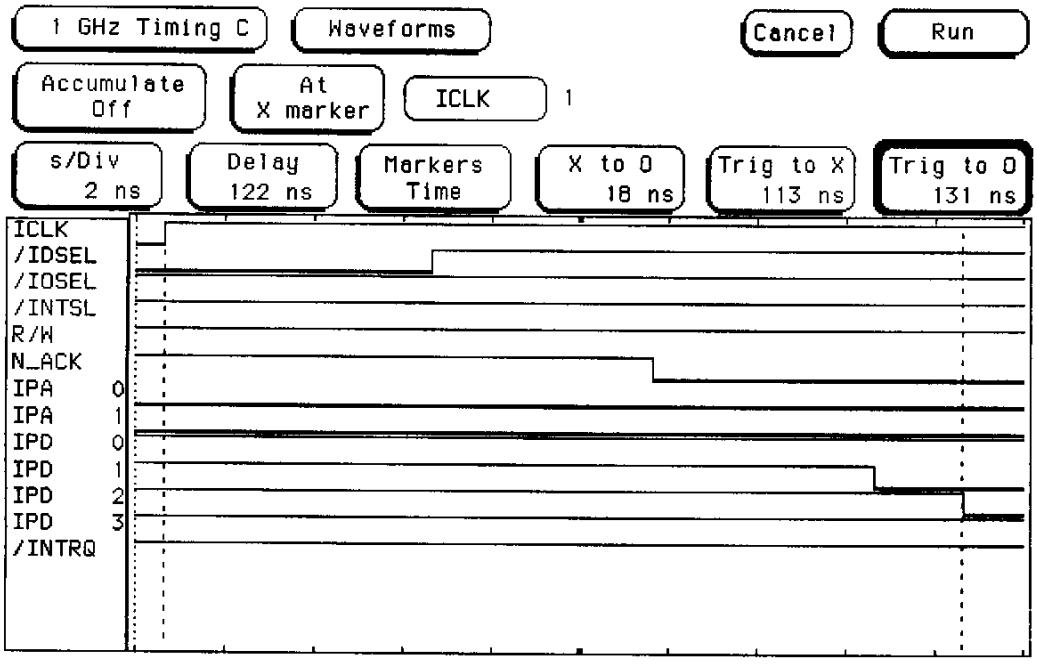


Figure 4-3 Zoom-In View of ID Read Cycle Driving N_ACK and IPD0-3 Signals

4.2.2 I/O Read Cycle

Figure 4-4 is a complete DUAL32CT I/O read cycle. The signals of interest are /IOSEL, N_ACK, and the four IPD0-3 signals. Figure 4-5 is a zoomed-in view of the DUAL32CT I/O read cycle driving the N_ACK and IPD0-3 signals showing a typical response time of about 16 ns for driving these signals.

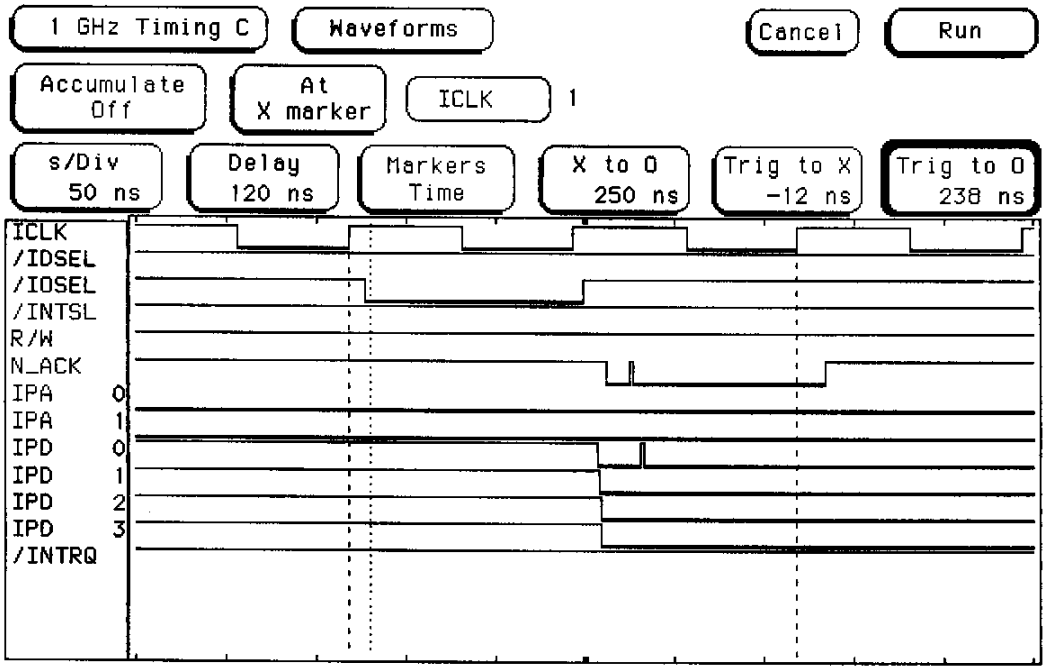


Figure 4-4 Complete I/O Read Cycle

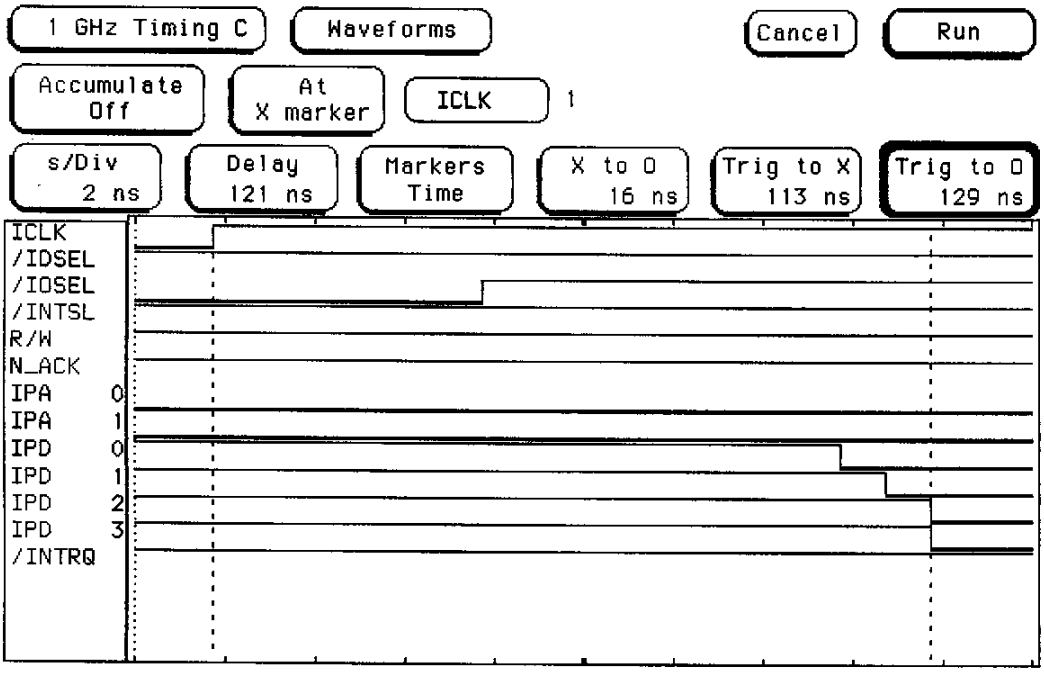


Figure 4-5 Zoom-In View of I/O Read Cycle Driving N_ACK and IPD0-3 Signals

4.2.3 Interrupt Request

Figure 4-6 shows an Interrupt Request, and IP Module Interrupt Select Cycle, and later, the resetting of the Interrupt Status bit.

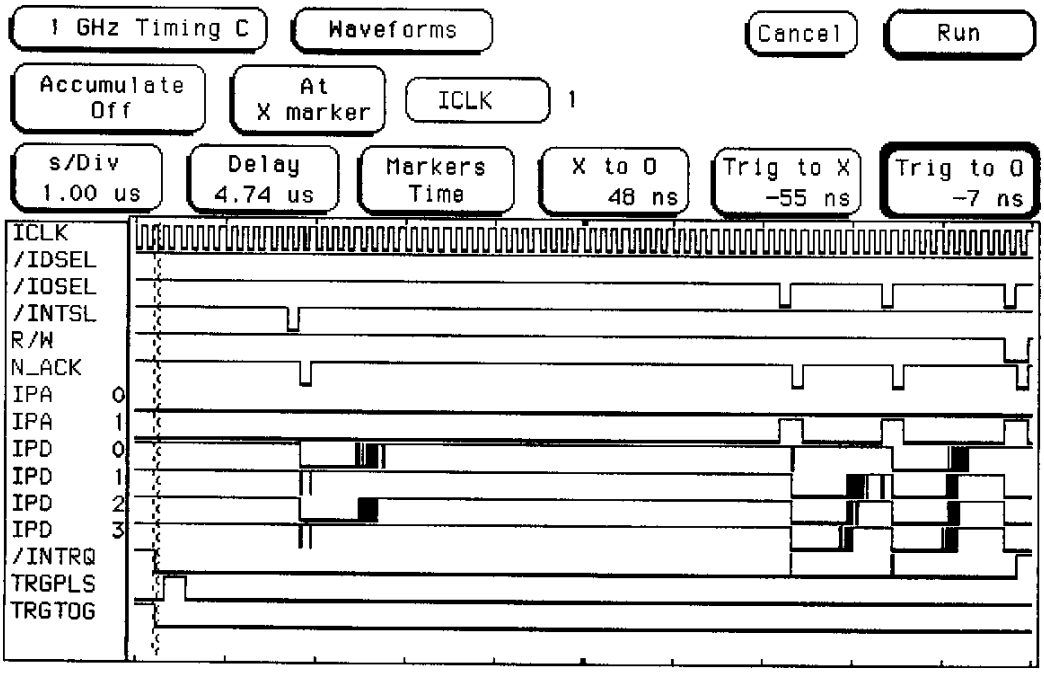


Figure 4-6 Complete Interrupt Request and Service Routine

4.2.4 OS-9 Interrupt Select Cycle

Figure 4-7 is a view of an OS-9 Interrupt Select cycle fetching the interrupt vector in less than 1.5 µs after the Interrupt Request signal (N_INTREQ0) was asserted.

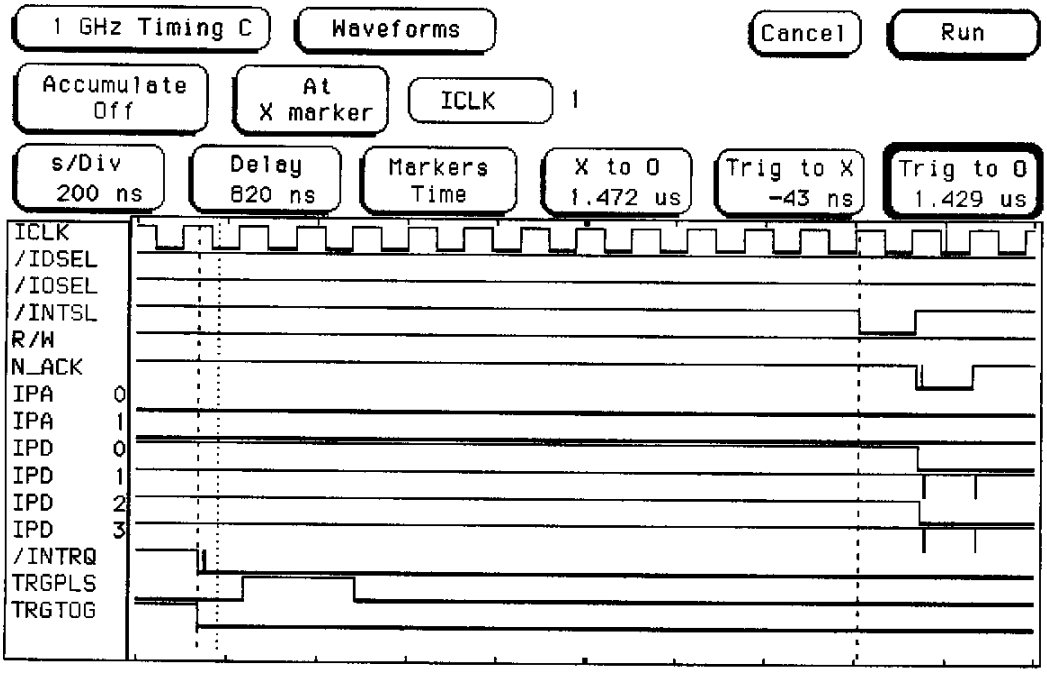


Figure 4-7 OS-9 Responding With Interrupt Select Cycle in Less Than 1.5 µs

4.2.5 TRIGPULSE Signal Asserted (100 ns)

Figure 4-8 is a view of the DUAL32CT's TRIGPULSE signal asserted 100 ns after the DUAL32CT reaches the terminal count and generates an Interrupt Request signal.

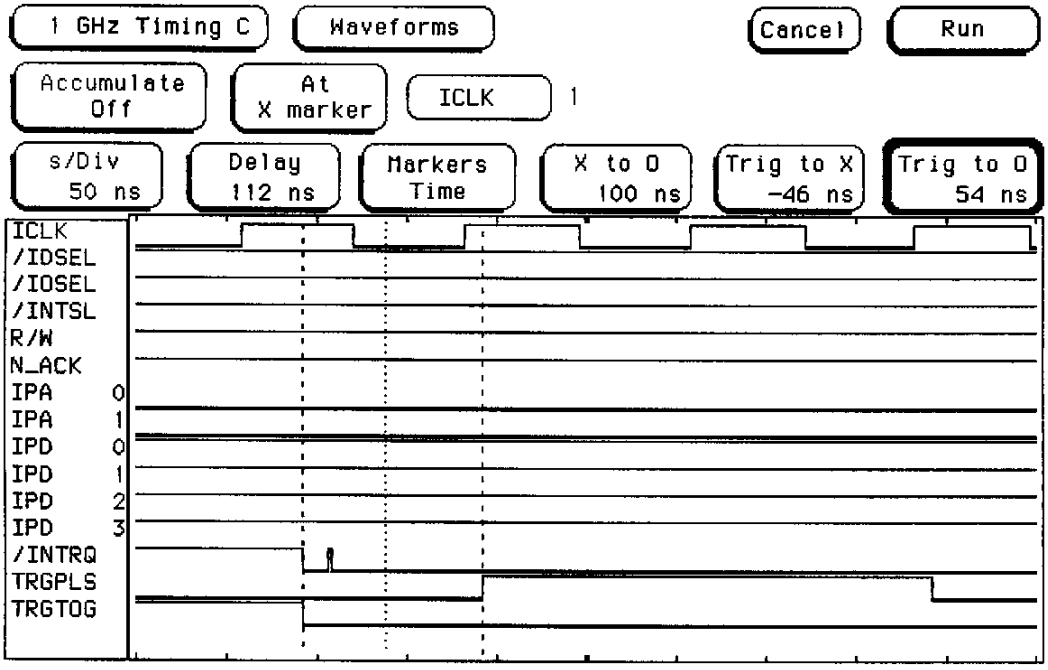


Figure 4-8 TRIGPULSE Asserted 100 ns After Reaching Terminal Count and Generating N_INTREQ0

4.2.6 I/O Write To Interrupt Status Register (IR0)

Figure 4-9 is a view of an I/O write to the Interrupt Status Register (IR0) resetting the status bid and the N_INTREQ0 signal.

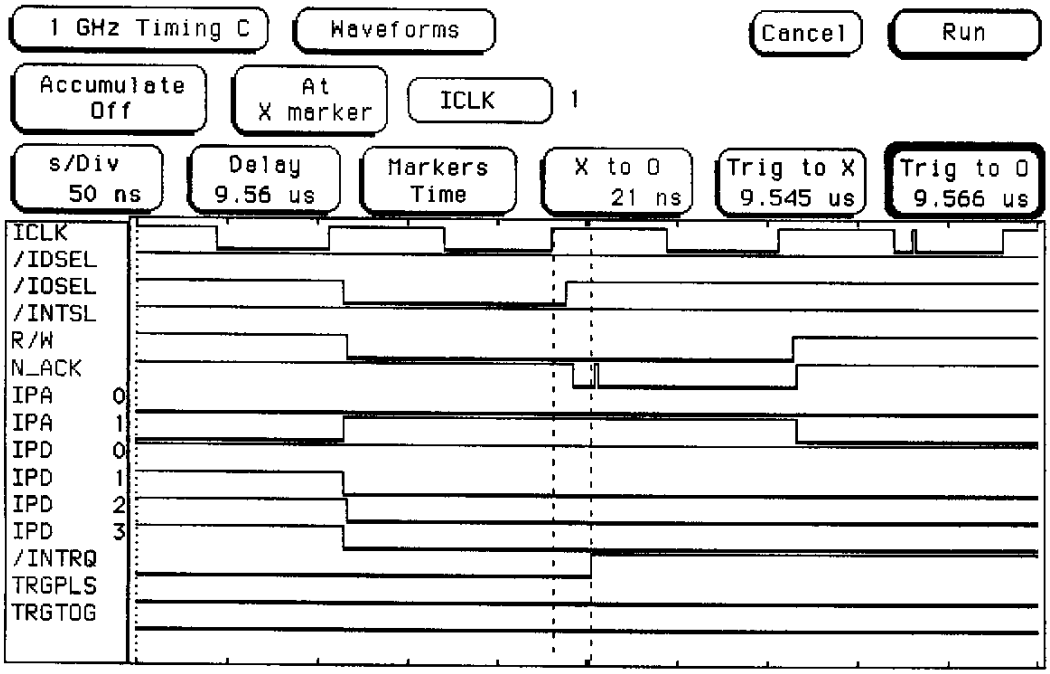


Figure 4-9 I/O Write to the Interrupt Status Register (IR0) Resetting N_INTREQ0

4.2.7 TRIGPULSE Signal Asserted (122 ns)

Figure 4-10 is a view of the DUAL32CT's TRIGPULSE signal asserted 122 ns after the rising edge of the External Clock signal.

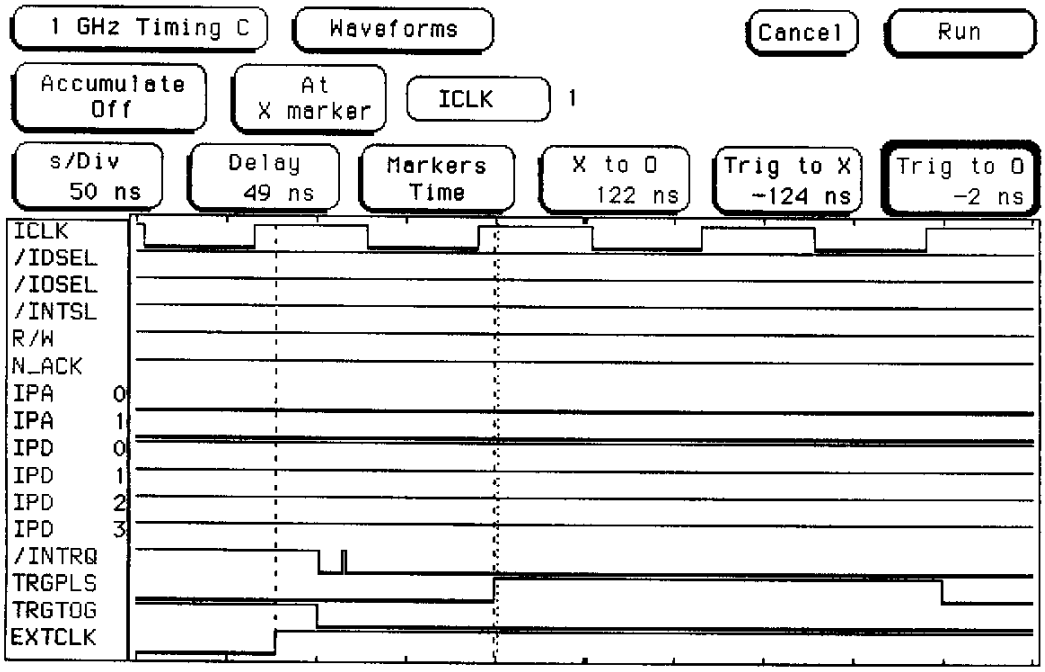


Figure 4-10 TRIGPULSE Asserted 122 ns After Rising Edge of External Clock

APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements ..... 1.800 inches x 3.900 inches x 0.303 inches (above board),
4.572 cm x 9.906 cm x 0.770 cm
Weight ..... 1.267 oz., 35.93 grams
Board thickness ..... 0.062 inches, 0.157 cm, nominally, (6 layers)

PROTOCOL

Clock rate ..... 8 MHz
Wait cycles ..... None on any transfer types
Hold cycles ..... Supported on all valid transfer types
Address decoding ..... Complete (no partial)
I/O transfers
- Writes 8-bit, 16-bit
- Reads 16-bit

I/O locations ..... Eighteen, 16-bit
- Configuration ..... 1 per counter
- Control ..... 1 per counter
- Data ..... 2 per counter
- Terminal Count ..... 2 per counter
- Interrupt ..... 3 per counter
- Maximum read/write rate ..... 4 MTransfers/second, sustained

ID transfers ..... 8-bit read (only)
Zero-fill on upper byte
12 bytes, including CRC
- Systran's manufacturer's ID ..... 0x45, E ASCII
- DUAL32CT's model number ..... 0x66, f ASCII
- Cyclic Redundancy Check value 0x01
- Maximum read rate ..... 4 MTransfers/second, sustained

Memory transfers ..... Not supported
Interrupt Vector transfers ..... 8-bit read
Zero-fill on upper byte
- Maximum read/write rate ..... 4 MTransfers/second, sustained

Interrupt Requests
- Drives IP Module signal **INTREQ0** on programmed event for counter #1
- Drives IP Module signal **INTREQ1** on programmed event for counter #2

DMA activity ..... Not supported
Acknowledgment on unsupported transfer attempts ..... None generated
- Memory read and write
- ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

All registers default to '0's (I/O read of 0x00000000), except the terminal count registers default to all '1's (0x11111111)
No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS

Power: ..... +5 Vdc @ 360 mA
+12 Vdc @ 0 mA
-12 Vdc @ 0 mA

PERFORMANCE CHARACTERISTICS

Electrical Characteristics ..... Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

Supply voltage with respect to ground:
Minimum ..... -0.5 V
Maximum ..... +7.0 V

RECOMMENDED OPERATING CONDITIONS:

Supply voltage: ..... +4.75 V → +5.25 V
Logic Interface ..... ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating) ..... 0°C to +70°C
Temperature (no bias, storage) ..... -40°C to +150°C
Humidity (Non-condensing) ..... 5% to 95%
Vibration (Operating) ..... 15 G's RMS (10→55 Hz)
Shock (Operating) ..... 50 G's maximum
Altitude (Operating) ..... 10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MIL-HDBK-217F ..... 756,216 hours
Bellcore ..... 1,526,911 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

TABLE OF CONTENTS

B.1 Applications B-1
B.2 Variable-Period-Variable-Pulse-Width Waveform-Generator Application B-1
B.3 Precision-Frequency-Measurement Application B-3
B.3.1 66-Bit Counter Application B-5

FIGURES

Figure B-1 External Signal Connection for the VPVPW Application B-2
Figure B-2 Trigger and Busy Signals for the Variable-Period Variable-Pulse-Width Example B-3
Figure B-3 External Connections for the Precision Frequency Measurement Application B-4
Figure B-4 66-Bit Counter Configuration B-6

B.1 Applications

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the DUAL32CT IP Module to solve a problem. This section may be revised periodically to include new application ideas for all users to consider. You can help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

We developed the following typical applications for using both counters on the DUAL32CT IP Module. However, you can use a single counter/timer to perform many common configuration operations.

B.2 Variable-Period Variable-Pulse-Width Waveform-Generator Application

Figure B-1 shows the DUAL32CT configured for a Variable-Period Variable-Pulse-Width (VPVPW) Waveform Generator. This application example shows the hardware configuration for the programming example of the same title in Appendix C.

In this example, both timers generate signal pulses with a frequency of 1 kHz, and the BUSY2 output signal of Timer 2 (pin 27 on the I/O connector) has a pulse width of 15 µs. Timer 1 controls the period via the N_TRIGPULSE1 output signal (pin 11 on the I/O connector), and Timer 2 controls the pulse width via the TIMER_EN2 input signal (pin 25 on the I/O connector). The low-going N_TRIGPULSE1 output of timer 1 is connected to the TIMER_EN2 input of Timer 2.

Figure B-2 shows the waveforms of the Trigger and Busy signals for the VPVPW example.

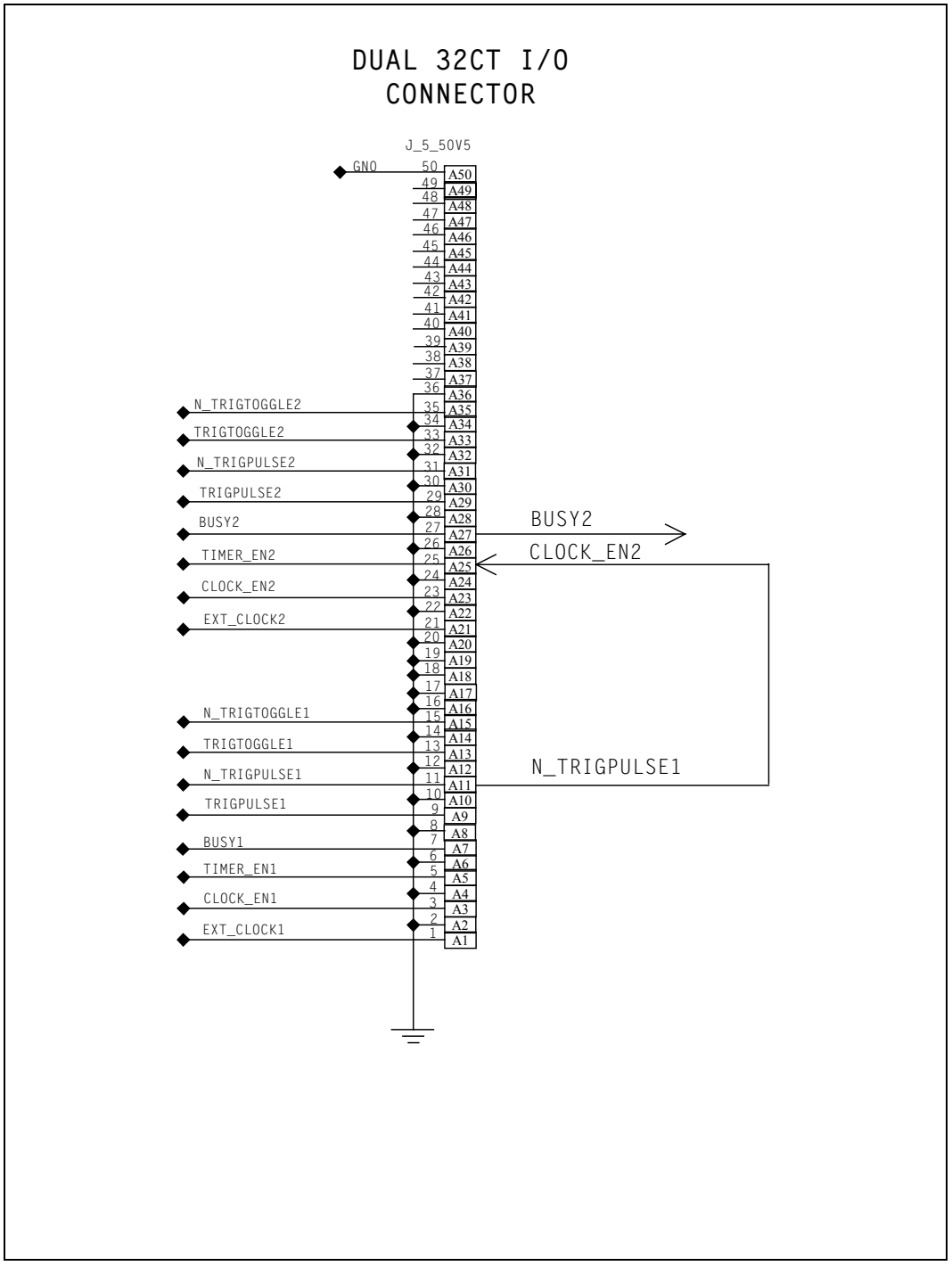


Figure B-1 External Signal Connection for the VPVPW Application

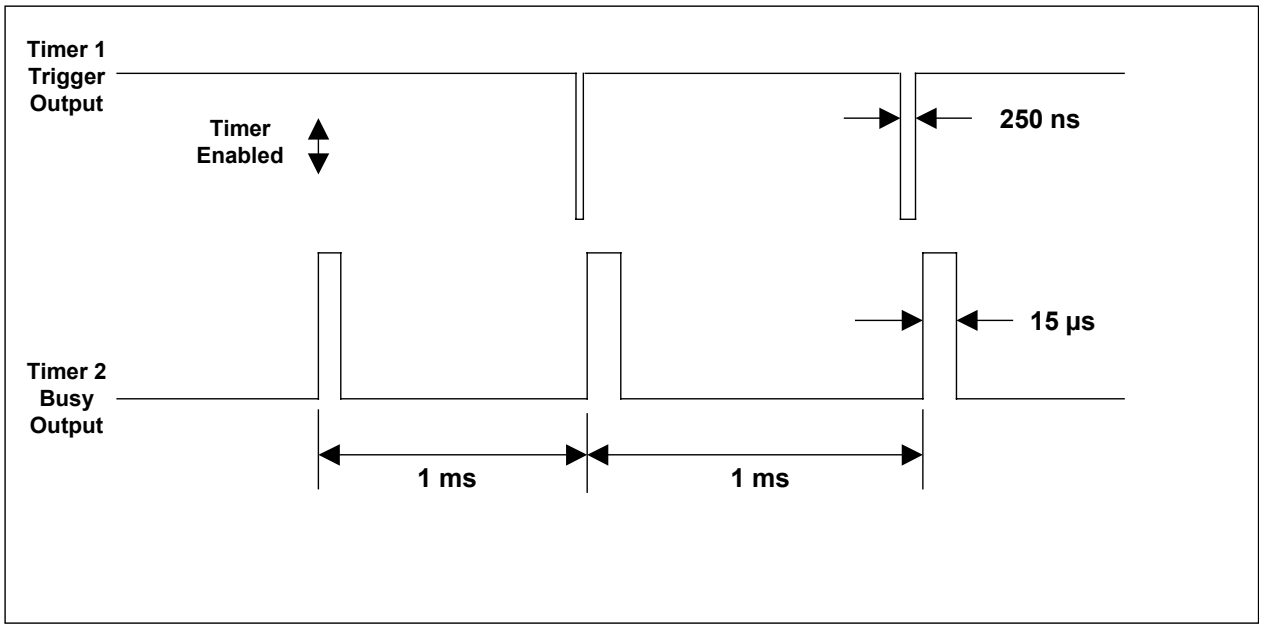


Figure B-2 Trigger and Busy Signals for the Variable-Period Variable-Pulse-Width Example

B.3 Precision-Frequency-Measurement Application

Figure B-3 shows the DUAL32CT configured for a Precision-Frequency-Measurement application example. This application example shows the hardware configuration for the programming example of the same title in Appendix C.

In this example, both timers are used to accurately measure the frequency of pulses. Timer 1 controls the time (or sample) period over which the pulses are counted. Timer 2 acts as a generic counter and connects the pulse signal to the EXT_CLOCK2 signal input (pin 21 of the I/O connector). The BUSY1 output signal of Timer 1 (pin 7 of the I/O connector) is connected to the Clock Enable input of Timer 2 (pin 23 of the I/O connector) to create the sampling period.

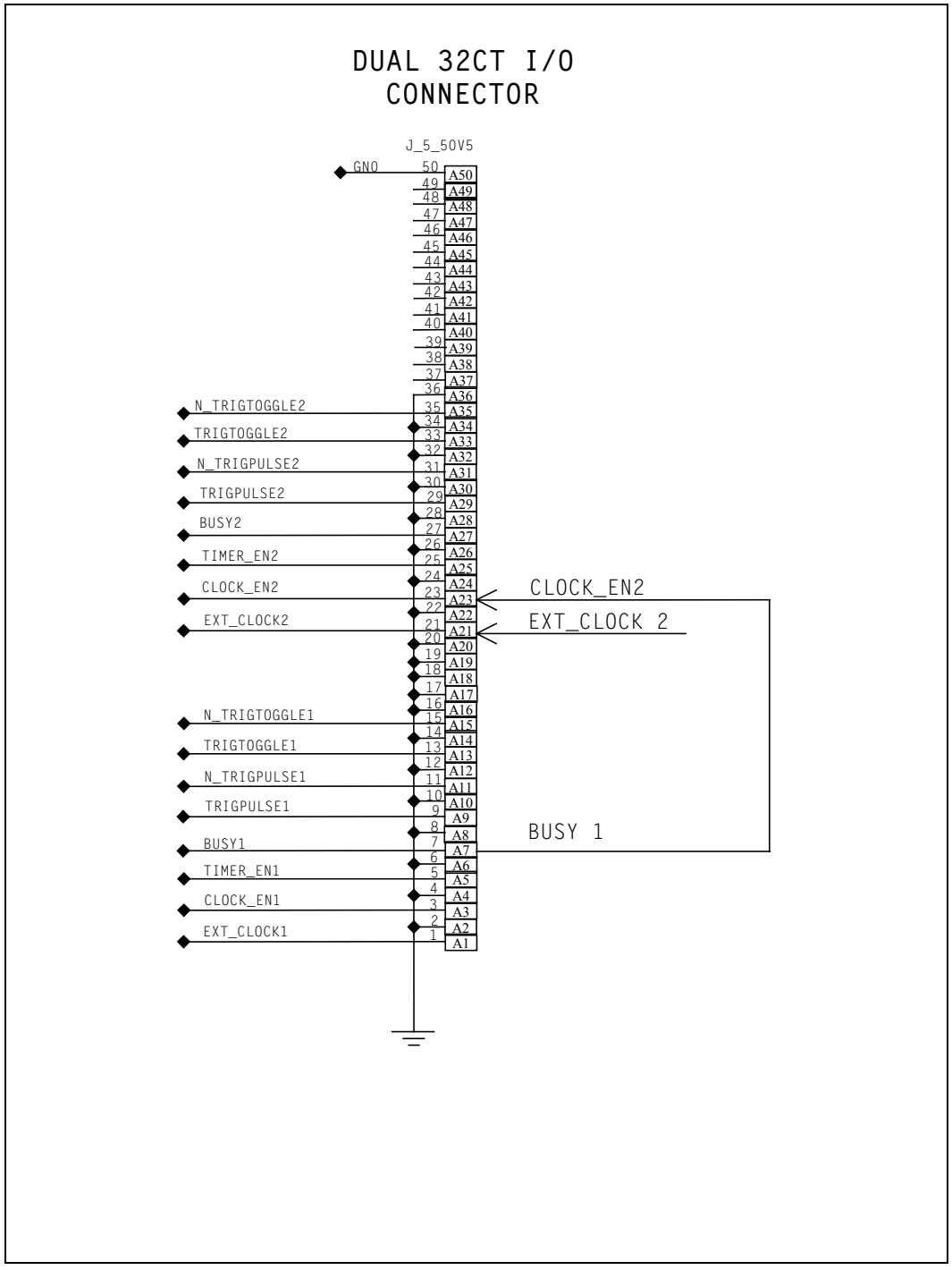


Figure B-3 External Connections for the Precision Frequency Measurement Application

B.3.1 66-Bit Counter Application

Figure B-4 shows the DUAL32CT configured for a 66-bit counter application example. This application example cascades the two counters to form a 66-bit counter.

In this example, both counters are used as generic counters and are both set to use the external clock inputs. When the count of Counter #1 rolls over to a count of zero, the N_TRIGTOGGLE1 output signal (pin 15 of the I/O connector) goes high, clocking the EXT_CLOCK2 signal input (pin 21 of the I/O connector) as the 33rd bit of Counter #1. When the count of Counter #2 rolls over to a count of zero, the N_TRIGTOGGLE2 output signal (pin 35 of the I/O connector) goes high as the 66th bit of both counters.

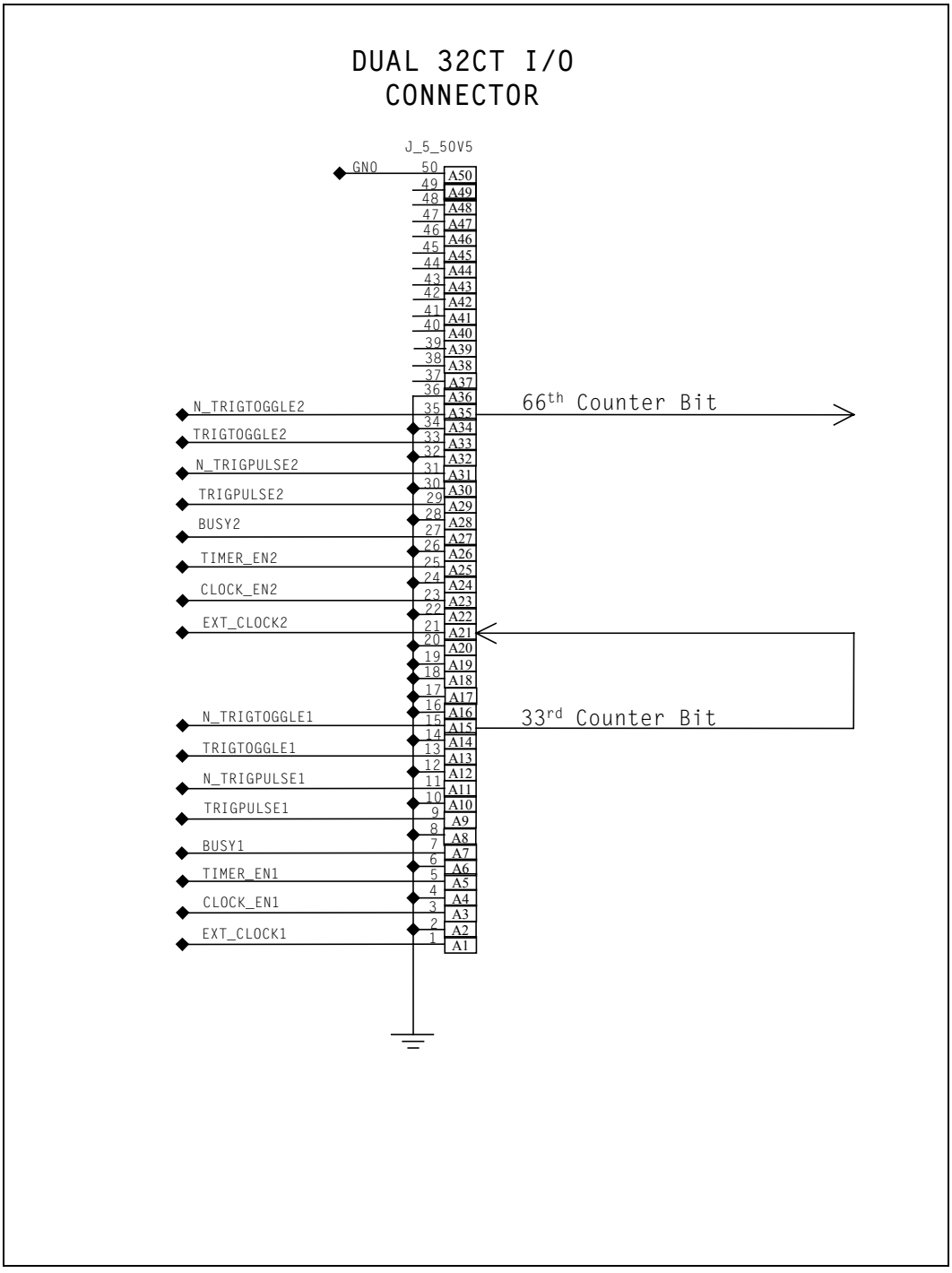


Figure B-4 66-Bit Counter Configuration

APPENDIX C

PROGRAMMING GUIDE

TABLE OF CONTENTS

C.1 Introduction C-1
C.2 Description C-1
C.3 IP Module ID PROM Listing C-1
C.4 IP Module IO Address Map C-2
C.5 Word Access Address Translation C-5
C.6 Byte Access Address Translation C-6
C.6.1 Data Register MSW Description (IPA = 0x00 and 0x10) C-7
C.6.2 Data Register LSW Description (IPA = 0x01 and 0x11) C-7
C.6.3 Control Register 0 (CR0) Description (IPA = 0x02 and 0x12) C-8
C.6.4 Control Register 1 (CR1) Description (IPA = 0x03 and 0x13) C-9
C.6.5 Terminal Count MSW Register Description (IPA = 0x04 and 0x14) C-10
C.6.6 Terminal Count LSW Register Description (IPA = 0x05 and 0x15) C-10
C.6.7 Interrupt Status Register (IR0) Description (IPA = 0x06 and 0x16) C-11
C.6.8 Interrupt Enable Register (IR1) Description (IPA = 0x07 and 0x17) C-11
C.6.9 Interrupt Vector Register (IR2) Description (IPA = 0x08 and 0x18) C-12
C.7 Programming Examples C-12
C.7.1 System Clock Example C-12
C.7.2 Watchdog Timer Example C-13
C.7.3 Square-Wave Generator Example C-14
C.7.4 Variable-Period Variable-Pulse-Width Waveform-Generator Example C-15
C.7.5 Precision Frequency Measurement Example C-16

FIGURES

Figure C-1 Trigger Output for Square-Wave Example C-14
Figure C-2 Trigger and Busy Signals for the Variable Period Variable Pulse Width Example..... C-15

TABLES

Table C-1 DUAL32CT ID Address Space Listing..... C-2
Table C-2 DUAL32CT I/O Address Map C-3
Table C-3 Word Access Address Translation C-5
Table C-4 Byte Access Address Translation Table..... C-6
Table C-5 Data MSW Register Bit Descriptions..... C-7
Table C-6 Data LSW Register Bit Descriptions..... C-7
Table C-7 Control Register Bit Descriptions..... C-8
Table C-8 Control Register Bit Descriptions..... C-9
Table C-9 Clock-Select Bits..... C-9
Table C-10 Terminal Count MSW Register Bit Description..... C-10
Table C-11 Terminal Count LSW Register Bit Description..... C-10
Table C-12 Interrupt Status Register Bit Descriptions C-11
Table C-13 Interrupt Enable Register Bit Descriptions..... C-11
Table C-14 Interrupt Vector Register Bit Descriptions C-12

C.1 Introduction

This section of the manual describes the operation of the DUAL32CT from the software perspective, detailing the DUAL32CT registers and providing programming examples. For a more detailed description of the hardware, see Chapter 2 and Appendix B.

C.2 Description

The DUAL32CT is an easy-to-use dual 32-bit counter/timer card. Each timer is completely independent with its own register set and interrupts. Control signals and triggers are provided at the I/O connector for external monitor and control, such as for multi-timer applications.

The DUAL32CT has eighteen 16-bit wide registers, nine per timer. The nine timer registers are: two data (making up the 32-bit count), one control, one configuration, two terminal count (making up the 32-bit terminal count), and three interrupt-related.

The count value can be accessed while the counter is running by reading the MSW then the LSW data registers via normal I/O read cycles. When the MSW data register is read, the DUAL32CT latches the entire 32-bit count value into the MSW and LSW data registers for an instantaneous snapshot of the count value. When the LSW data register is read, the DUAL32CT releases the latches.

The control register allows gating of the clock signal and halt/run control of the timer. The configuration register provides selection of the clock source and the timer mode. You initialize the 32-bit terminal count value by writing to the terminal count MSW and LSW registers. The interrupt-related registers allow you to program the interrupt vector, and interrupt enable, and provide you the interrupt status. Byte writes to any of these registers are not destructive to adjacent bytes.

C.3 IP Module ID PROM Listing

The ID PROM function is emulated because of the never-changing information it presents. Emulating saves space, lowers costs, improves reliability, and enables this IP Module to provide “no-wait” read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) results in no acknowledgement, and its subsequent bus-timeout error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

The following table is the DUAL32CT emulated ID Address Space PROM listing:

Table C-1 DUAL32CT ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII “I”	0x49
IPA = 0x01	ASCII “P”	0x50
IPA = 0x02	ASCII “A”	0x41
IPA = 0x03	ASCII “C”	0x43
IPA = 0x04	Systran’s ID	0x45
IPA = 0x05	DUAL32CT’s Model Number	0x66
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0x01

C.4 IP Module IO Address Map

The DUAL32CT I/O Address Map has efficiently located data, control, and interrupt registers in the IP Module I/O address space (IPA= 0x00⇒0x11F). Addresses IPA= 0x00⇒0xF are the I/O space for Counter #1, and Counter #2’s I/O space is mirrored like Counter #1’s in addresses IPA= 0x10⇒0x1F.

The first two 16-bit registers (IPA= 0x00⇒0x01 and 0x10⇒0x11) are the counters #1 and #2 data registers and you may view them as two 16-bit or four 8-bit registers. The next addresses (IPA= 0x02⇒0x03 and 0x12⇒0x13) are the control registers for each counter, and are located in byte-lane 0.

Control Register 0 (CR0) is the “Timer Enable & Clock Enable” register and uses bits [1:0], with bit [1] controlling the Timer Enable and bit [0] controlling the Clock Enable for each counter, respectively. The DUAL32CT does not use bits [15:2] in CR0. If you read these bits, they read as zeroes. Control Register 1 (CR1) is the “Stop On Terminal Count (SOTC)” bit and the “Clock Selection” register and uses bits [2:0], with bit [2] to control the SOTC and bits [1] and [0] for the clock selection. The DUAL32CT does not use bits [15:3] in CR1. If you read those lots, they read as zeroes. The next addresses (IPA= 0x04⇒0x05 and 0x14⇒0x15) are the “Terminal Count” registers and you may view them as two 16-bit or four 8-bit registers.

The next addresses (IPA= 0x06⇒0x08 and 0x16⇒0x18) are the interrupt control/status registers located in byte-lane 0. Interrupt Register 0 (IR0) is the “Interrupt Status” register, IR1 is the “Interrupt Enable” register, and both only use bit [0]. IR2 is the “Interrupt Vector” register and uses bits [7:0]. The DUAL32CT places these bits on the IPD[7:0] data lines during an IP Module Interrupt cycle.

The last addresses (IPA= 0x09⇒0x0F and 0x19⇒0x1F) are NOT in the DUAL32CT's I/O address space, and will result in a bus error if accessed. Refer to the register bit definitions later in this Programming Guide for more details.

Table C-2 is the DUAL32CT I/O Address Map and contains the data ports, control registers and interrupt registers:

Table C-2 DUAL32CT I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	Data Bits [31:24]	Data Bits [23:16]	Counter #1 Data Register Most Significant Word
IPA = 0x01	Data Bits [15:8]	Data Bits [7:0]	Counter #1 Data Register Least Significant Word
IPA = 0x02	[XXXX,XXXX]	[XXXX,XX] [1:0]	Counter #1 Control Register 0, Timer Enable bit [1], Clock Enable bit [0], 0=Disabled 1=Enabled
IPA = 0x03	[XXXX,XXXX]	[XXXX,X] [2:0]	Counter #1 Control Register 1, SOTC Enable bit [2], 0=Don't Stop 1=Stop Clock Select bits [1:0] Internal 8MHz = 00 Internal 1 MHz = 01 Internal 125 KHz = 10 External Clock = 11
IPA = 0x04	Data Bits [31:24]	Data Bits [23:16]	Counter #1 Terminal Count Register Most Significant Word
IPA = 0x05	Data Bits [15:8]	Data Bits [7:0]	Counter #1 Terminal count Register Least Significant Word
IPA = 0x06	[XXXX,XXXX]	[XXXX,XXX] [0]	Counter #1 Interrupt Register 0, Interrupt Status Register bit, 0=No Interrupt, 1=SOTC reached
IPA = 0x07	[XXXX,XXXX]	[XXXX,XXX] [0]	Counter #1 Interrupt Register 1, Interrupt Enable bit, 0=Disabled 1=Enabled
IPA = 0x08	[XXXX,XXXX]	[7:0]	Counter #1 Interrupt Register 2, Interrupt Vector Register, 8 bits
IPA= 09⇒0x0F	[XXXX,XXXX]	[XXXX,XXXX]	Not Used



NOTE: [X] means the bit is not used.

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x10	Data Bits [31:24]	Data Bits [23:16]	Counter #2 Data Register
IPA = 0x11	Data Bits [15:8]	Data Bits [7:0]	Counter #2 Data Register
IPA = 0x12	[XXXX,XXXX]	[XXXX,XX] [1:0]	Counter #2 Control Register 0, Timer Enable bit [1], Clock Enable bit [0], 0=Disabled 1=Enabled
IPA = 0x13	[XXXX,XXXX]	[XXXX,X] [2:0]	Counter #2 Control Register 1, SOTC Enable bit [2], 0=Don't Stop 1=Stop Clock Select bits [1:0] Internal 8MHz = 00 Internal 1 MHz = 01 Internal 125 KHz = 10 External Clock = 11
IPA = 0x14	Data Bits [31:24]	Data Bits [23:16]	Counter #2 Terminal Count Register
IPA = 0x15	Data Bits [15:8]	Data Bits [7:0]	Counter #2 Terminal count Register
IPA = 0x16	[XXXX,XXXX]	[XXXX,XXX] [0]	Counter #2 Interrupt Register 0, Interrupt Status Register bit, 0=No Interrupt, 1=SOTC reached
IPA = 0x17	[XXXX,XXXX]	[XXXX,XXX] [0]	Counter #1 Interrupt Register 1, Interrupt Enable bit, 0=Disabled 1=Enabled
IPA = 0x18	[XXXX,XXXX]	[7:0]	Counter #2 Interrupt Register 2, Interrupt Vector Register, 8 bits
IPA= 19⇒0x1F	[XXXX,XXXX]	[XXXX,XXXX]	Not Used



NOTE: [X] means the bit is not used.

C.5 Word Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation

VMEBus Address	PC-AT Bus Address	NUBUS Address	IP Module Address
BASE + 0x00	BASE + 0x00	BASE + 0x02	IPA=0x00
BASE + 0x02	BASE + 0x02	BASE + 0x06	IPA=0x01
BASE + 0x04	BASE + 0x04	BASE + 0x0A	IPA=0x02
BASE + 0x06	BASE + 0x06	BASE + 0x0E	IPA=0x03
BASE + 0x08	BASE + 0x08	BASE + 0x10	IPA=0x04
BASE + 0x0A	BASE + 0x0A	BASE + 0x16	IPA=0x05
BASE + 0x0C	BASE + 0x0C	BASE + 0x1A	IPA=0x06
BASE + 0x0E	BASE + 0x0E	BASE + 0x1E	IPA=0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA=0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA=0x09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA=0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA=0x0B

C.6 Byte Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VMEBus Address	PC-AT Bus Address	NUBUS Address	IP Module Address	Byte-Lane*
BASE + 0x01	BASE + 0x00	BASE + 0x03	IPA=0x00	0
BASE + 0x00	BASE + 0x01	BASE + 0x02	IPA=0x00	1
BASE + 0x03	BASE + 0x02	BASE + 0x07	IPA=0x01	0
BASE + 0x02	BASE + 0x03	BASE + 0x06	IPA=0x01	1
BASE + 0x05	BASE + 0x04	BASE + 0x0B	IPA=0x02	0
BASE + 0x04	BASE + 0x05	BASE + 0x0A	IPA=0x02	1
BASE + 0x07	BASE + 0x06	BASE + 0x0F	IPA=0x03	0
BASE + 0x06	BASE + 0x07	BASE + 0x0E	IPA=0x03	1
BASE + 0x09	BASE + 0x08	BASE + 0x13	IPA=0x04	0
BASE + 0x08	BASE + 0x09	BASE + 0x12	IPA=0x04	1
BASE + 0x0B	BASE + 0x0A	BASE + 0x17	IPA=0x05	0
BASE + 0x0A	BASE + 0x0B	BASE + 0x16	IPA=0x05	1
BASE + 0x0D	BASE + 0x0C	BASE + 0x1B	IPA=0x06	0
BASE + 0x0C	BASE + 0x0D	BASE + 0x1A	IPA=0x06	1
BASE + 0x0F	BASE + 0x0E	BASE + 0x1F	IPA=0x07	0
BASE + 0x0E	BASE + 0x0F	BASE + 0x1E	IPA=0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA=0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA=0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA=0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA=0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA=0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA=0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA=0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA=0x0B	1

* Byte-lane 1 not applicable for ID Space

C.6.1 Data Register MSW Description (IPA = 0x00 and 0x10)



NOTE: You can access the count value while the counter is running by reading the MSW then the LSW data registers via normal I/O read cycles. When you read the MSW data register, the DUAL32CT latches the entire 32-bit count value into the MSW and LSW data registers for an instantaneous snapshot of the count value. When you read the LSW data register, the DUAL32CT releases the latches.

This register contains the MSW (most significant word) of the 32-bit data value at IPA=0x00 Counter #1 and IPA = 0x10 for Counter #2. On power-up all bits are set to '0.'

Table C-5 Data MSW Register Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	D 31	D 30	D 29	D 28	D 27	D 26	D 25	D 24	D 23	D 22	D 21	D 20	D 19	D 18	D 17	D 16
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D31 – D16: Bits [31] to [16] (the MSW) of the 32-bit data value.

C.6.2 Data Register LSW Description (IPA = 0x01 and 0x11)

This register contains the LSW (least significant word) of the 32-bit data value. On power-up all bits are set to '0.'

Table C-6 Data LSW Register Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D15-D0: Bits [15] to [0] (the LSW) of the 32-bit data value.

C.6.3 Control Register 0 (CR0) Description (IPA = 0x02 and 0x12)

This 16-bit read/write register is the counter/timer control register. There are two control bits in this register, the clock-enable bit, and the timer-enable bit. The clock-enable bit provides software-controlled gating of the clock signal (either external or internal). The timer-enable bit controls whether the timer is in the run or setup mode. On power-up all bits are set to '0.'

Table C-7 Control Register Bit Descriptions

Bit #	15 to 2	1	0
Bit Name	Not used	Timer Enable	Clock Enable
R/W	Read as 0's	RW	RW
Power-Up State	0	0	0

Clock Enable: Clock gating control – '1' = enable clock, '0' = disable clock.

Timer Enable: Counter/timer-enable control – '1' = timer enabled (run mode), '0' = timer disabled (setup mode). When the SOTC bit (bit 2 in Control Register 1) is set, the timer halts when the terminal count is reached. You must toggle this timer-enable bit, or the external Timer-Enable signal low, then high, to restart the timer when the SOTC is set and the timer reaches terminal count. You may also asynchronously reset the timer by toggling the timer-enable bit or external timer-enable signal low, then high.

C.6.4 Control Register 1 (CR1) Description (IPA = 0x03 and 0x13)

This 16-bit read/write register is the counter/timer configuration register. There are two groups of bits in this register: the clock-select bits, and the stop-on-terminal-count bit. The clock-select bits select one of three internal clock frequencies or an external clock. On power-up all of the bits are cleared, with the internal 8 MHz clock selected as the default.

Table C-8 Control Register Bit Descriptions

Bit #	15 to 3	2	1	0
Bit Name	Not used	SOTC	CS1	CS0
R/W	Read as 0's	RW	RW	RW
Power-Up State	0	0	0	0

CS1-CS0: Clock-select bits (see table below).

Table C-9 Clock-Select Bits

CS1	CS0	Clock Selection
0	0	Internal 8 MHz clock (default)
0	1	Internal 1 MHz clock
1	0	Internal 125 KHz clock
1	1	External clock

SOTC: Stop-on-Terminal-Count bit – this bit determines if the counter stops when terminal count is reached, or rolls over to zero and keeps counting. '0' = don't stop on terminal count, '1' = stop on terminal count.

C.6.5 Terminal Count MSW Register Description (IPA = 0x04 and 0x14)

This register contains the MSW of the 32-bit terminal count value. On power-up all bits are set to '1.'

Table C-10 Terminal Count MSW Register Bit Description

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	TC 31	TC 30	TC 29	TC 28	TC 27	TC 26	TC 25	TC 24	TC 23	TC 22	TC 21	TC 20	TC 19	TC 18	TC 17	TC 16
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TC31-TC16: Bits [31] to [16] (the MSW) of the 32-bit terminal count value.

C.6.6 Terminal Count LSW Register Description (IPA = 0x05 and 0x15)

This register contains the LSW of the 32-bit terminal count value. On power-up all bits are set to '1.'

Table C-11 Terminal Count LSW Register Bit Description

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	TC 15	TC 14	TC 13	TC 12	TC 11	TC 10	TC 9	TC 8`	TC 7	TC 6	TC 5	TC 4	TC 3	TC 2	TC 1	TC 0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TC15-TC0: Bits [15] to [0] (the LSW) of the 32-bit terminal count value.

C.6.7 Interrupt Status Register (IR0) Description (IPA = 0x06 and 0x16)

This register contains the interrupt status bit. The counter sets this bit when it reaches the terminal count. This bit indicates that the counter reached the terminal count whether the interrupt is enabled or not. Writing a '1' to this register clears the status bit. On power-up this bit is set to '0.' If the interrupt is enabled, an interrupt will occur when this bit sets. Counter #1 asserts INTREQ0 and Counter #2 asserts INTREQ1.

Table C-12 Interrupt Status Register Bit Descriptions

Bit #	15 to 1	0
Bit Name	Not used	Interrupt Status
R/W	Read as '0's	RW
Power-Up State	0	0

Interrupt Status: '1' = terminal count detected, '0' = terminal count not detected.

C.6.8 Interrupt Enable Register (IR1) Description (IPA = 0x07 and 0x17)

Table C-13 Interrupt Enable Register Bit Descriptions

Bit #	15 to 1	0
Bit Name	Not used	Interrupt Enable
R/W	Read as '0's	RW
Power-Up State	0	0

Interrupt Enable: '1' = enabled, '0' = disabled.

C.6.9 Interrupt Vector Register (IR2) Description (IPA = 0x08 and 0x18)

This register contains the interrupt vector. This 8-bit vector is presented to the IP Module data bus during the Interrupt Acknowledge Transfer.

Table C-14 Interrupt Vector Register Bit Descriptions

Bit #	15 to 8	7	6	5	4	3	2	1	0
Bit Name	Not Used	IV7	IV6	IV5	IV4	IV3	IV2	IV1	IV0
R/W	Read as '0's	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0

IV7 – IV0: The 8-bit interrupt vector. On power-up all bits are set to '0'.

C.7 Programming Examples

The following examples illustrate how to program the DUAL32CT device.

C.7.1 System Clock Example

This example uses a single timer to generate a periodic interrupt every 1 ms for system timekeeping.

```
Configuration:
       Configuration Register
              CS1-CS0 = '01' binary. This selects the internal
                                    clock at 1 MHz.
              SOTC = '0', don't stop on terminal count, rollover
                           to zero and keep counting
       Terminal Count MSW Register
              TC31-TC16 = 0x0000
       Terminal Count LSW Register
              TC15-TC0 = 0x03E8(1000 decimal)
       Interrupt Vector Register
              Load with the desired interrupt vector
       Interrupt Enable Register
              Interrupt Enable = 1, the interrupt is enabled
```

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register to a '1.' This starts the timer free running, and generates an interrupt every 1 ms. The interrupt service routine updates the system clock value and clears the Interrupt Status bit in the Interrupt Status Register by writing a '1' to it. No re-initialization of the timer is necessary because it is set up to free run.

C.7.2 Watchdog Timer Example

This example uses a single timer to implement a watchdog timer that times out after 10 ms if not serviced by the code. This assumes the trigger pulse output signal is connected to the system-reset circuitry.

```
Configuration:
       Configuration Register
              CS1-CS0 = '01' binary. This selects the internal
                                    clock at 1 MHz.
              SOTC = X, This is a don't care. If the timer times
                        out the system will reset
       Terminal Count MSW Register
              TC31-TC16 = 0x0000
       Terminal Count LSW Register
              TC15-TC0 = 0x2710 (10000 decimal)
       Interrupt Vector Register
              No initialization needed, interrupts not used in
              this example
       Interrupt Enable Register
              Interrupt Enable = 0, the interrupt is disabled
```

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register to a '1.' This starts the timer running. If the code clears then sets the Timer-Enable bit in the Control Register before the 10 ms expires (resets the timer), no trigger pulse occurs. If the code fails to reset the timer before the 10 ms expires, the trigger pulse occurs, and the processor is reset (again, we assume that the trigger output drives the reset circuitry).

C.7.3 Square-Wave Generator Example

This example uses a single timer to generate a 10 KHz square wave on the toggle output signal.

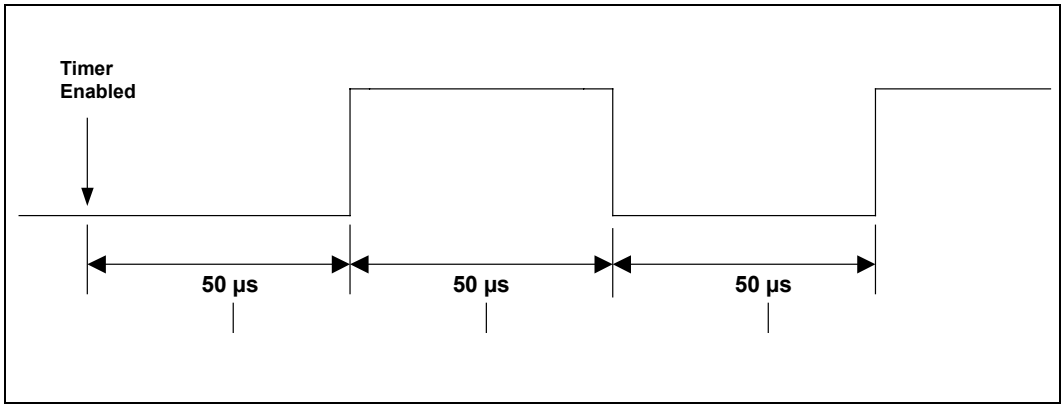


Figure C-1 Trigger Output for Square-Wave Example

```
Configuration:
          Configuration Register
                CS1-CS0 = '01' binary. This selects the internal
                                       clock at 1 MHz
                SOTC = '0', don't stop on terminal count, rollover
                             to zero and keep counting
          Terminal Count MSW Register
                TC31-TC16 = 0x0000
          Terminal Count LSW Register
                TC15-TC0 = 0x0032 (50 decimal)
          Interrupt Vector Register
                No initialization needed, interrupts not used in
                this example
          Interrupt Enable Register
                Interrupt Enable = 0, the interrupt is disabled
```

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register to a '1.' This starts the timer running. Every 50 µs the trigger output toggles generating a square wave (50% duty cycle). The timer will free-run until disabled by clearing the Timer-Enable bit or pulling the Timer-Enable input signal low.

C.7.4 Variable-Period Variable-Pulse-Width Waveform-Generator Example

This example uses both timers to generate a pulse with a 1 ms period and a pulse width of 15 µs on the Busy signal output of timer 2. Timer 1 controls the period, and used timer 2 controls the pulse width. The low-going Pulse Trigger output of timer 1 is connected to the Timer-Enable input of timer 2.

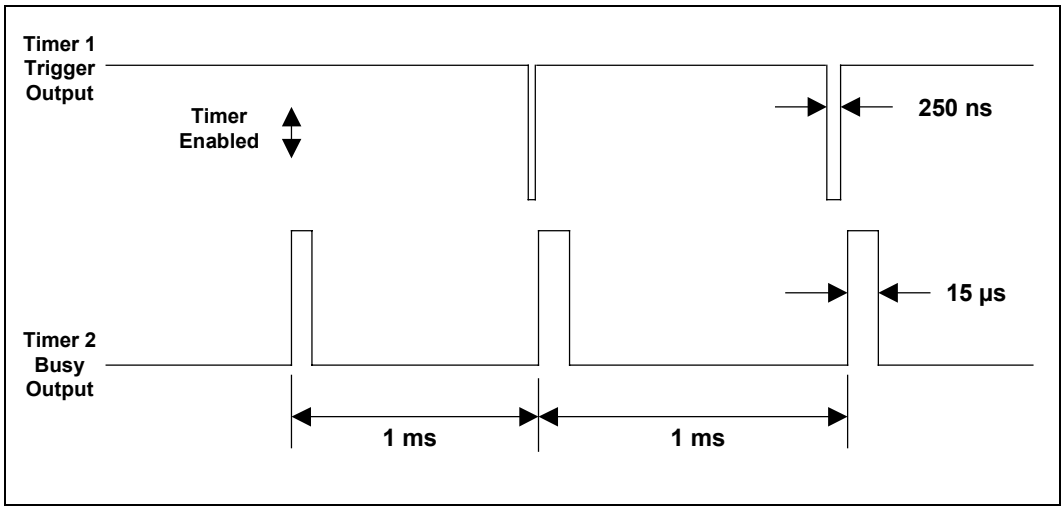


Figure C-2 Trigger and Busy Signals for the Variable Period Variable Pulse Width Example

```
Configuration for timer 1 (period control):
          Configuration Register
                CS1-CS0 = '01' binary. This selects the internal
                                       clock at 1 MHz.
                SOTC = '0', don't stop on terminal count, rollover
                             to 0 and keep counting
          Terminal Count MSW Register
                TC31-TC16 = 0x0000
          Terminal Count LSW Register
                TC15-TC0 = 0x03E8 (1000 decimal)
          Interrupt Vector Register
                No initialization needed, interrupts not used in
                this example
          Interrupt Enable Register
                Interrupt Enable = 0, the interrupt is disabled

   Configuration for timer 2 (pulse width control):
          Configuration Register
                CS1-CS0 = '01' binary. This selects the internal
                                       clock at 1 MHz
                SOTC = '1', stop on terminal count

          Terminal Count MSW Register
                TC31-TC16 = 0x0000
          Terminal Count LSW Register
                TC15-TC0 = 0x000F (15 decimal)
          Interrupt Vector Register
                No initialization needed, interrupts not used in
                this example
          Interrupt Enable Register
                Interrupt Enable = 0, the interrupt is disabled
```

Once configured, set the Timer-Enable and Clock-Enable bits in the Control Register of both timers to a '1.' This starts both timers running which generates the first pulse on the Busy output of timer 2. Timer 2 times out in 15 µs (the pulse width) causing its Busy output to go low and remains halted because the SOTC bit is set. When timer 1 reaches

its terminal count after 1 ms (the period), its trigger pulses low for 250 ns. Since the timer 1 trigger output is connected to the timer 2 Timer-Enable input, this pulse resets timer 2 and causes it to begin counting again. Timer 2 counts for 15 µs before reaching terminal count and while it is counting, its Busy output is high. To rephrase, the free- running timer 1 (period control) triggers the one-shot timer 2 (pulse width control) indefinitely until halted by the host. Therefore, you can vary the terminal count values of timer 1 and timer 2 to adjust the output waveform period and pulse width, respectively.

C.7.5 Precision Frequency Measurement Example

This example uses both timers to accurately measure the frequency of pulses. Timer 1 controls the time period during which the counter counts the pulses. We used Timer 2 as a counter with the pulse signal connected to its external clock input. The Busy output signal of timer 1 is connected to the Clock-Enable input of timer 2.

```
Configuration for timer 1 (counting period control):
       Configuration Register
              CS1-CS0 = '10' binary. This selects the internal
                                     clock at 125 KHz.
              SOTC = '1', stop on terminal count
       Terminal Count MSW Register
              TC31-TC16 = 0x0001
       Terminal Count LSW Register
              TC15-TC0 = 0xE848
              So, the total terminal count is 0x1E848
              (125,000 decimal)
       Interrupt Vector Register
              No initialization needed, interrupts not used in
              this example
       Interrupt Enable Register
              Interrupt Enable = 0, the interrupt is disabled

Configuration for timer 2 (used as counter):
       Configuration Register
              CS1-CS0 = '11' binary. This selects the external
                                     clock
              SOTC = '1', stop on terminal count
       Terminal Count MSW Register
              TC31-TC16 = 0xFFFF

       Terminal Count LSW Register
              TC15-TC0 = 0xFFFF
              The terminal count is set to the maximum so it
              doesn't interfere with the count. If the count
              reads all '0xF's, an overflow has occurred
       Interrupt Vector Register
              No initialization needed, interrupts not used in
              this example
       Interrupt Enable Register
              Interrupt Enable = 0, the interrupt is disabled
```

Once configured, enable timer 2 by setting its Timer-Enable and Clock-Enable bits in the Control Register to a '1.' Timer 2 will not begin counting yet because its clock is gated off by the logic low Busy output of timer 1. Now, enable timer 1 by setting its Timer-Enable and Clock-Enable bits in the Control Register to a '1.' Timer 1 will run for the programmed 1-second interval then stop. While timer 1 is running, its Busy output is logic high which enables the external clock of timer 2. Thus, timer 2 counts only during the 1-second period that timer 1 is running. Since the clock gating is hardware controlled, no error is introduced by programmed I/O delays.

GLOSSARY

[x:y] ---------- Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit (for example, Data bus [7:0] refers to the least significant eight bits).

aperture---------- A region or set of addresses.

byte-lane ---------- Eight bits of a data bus on octal boundaries.

CSR ---------- Control and Status Register.

doublewide ---------- An IP Module that is twice the size of the singlewide board.

EPLD ---------- Erasable Programmable Logic Device.

IP Module---------- Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable, plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP Module logic bus ---------- A synchronous, 4 MTransfers/second, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

ISR ---------- Interrupt Service Routine, Interrupt Status Register, or Interrupt Steering Register

MTBF ---------- Mean Time Between Failures.

ns, µs, ms ---------- Nanoseconds, microseconds, and milliseconds respectively.

singlewide ---------- An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

SOTC ---------- Stop on Terminal Count

VHDL ---------- Very high-speed integrated circuit Hardware Description Language.

This page intentionally left blank.

INDEX

A

address decoding A-1
address space C-2, C-3
applications 2-1

B

base address C-5, C-6
bus-timeout error C-1
busy signals 2-3, B-1

C

carrier board 1-1, 2-3, 3-1, 3-2, 3-3, A-2, C-1
cleaning 2-5
clock enable 2-1, 2-3, B-3, C-2, C-3, C-4, C-8
clock gating C-17
clock gating control C-8
clock rate A-1
comparators 2-2
connector 2-2, 2-3, 2-4, 3-3, B-1, B-3, B-5, C-1
control register 2-3, 2-4, C-1, C-2, C-3, C-8
control signals C-1
control/status registers C-2
counter #1 ..... B-5, C-2, C-3, C-7, C-11
counter #2 ..... B-5, C-2, C-4, C-7, C-11
counter enable C-8
counter reset 2-1
counter/timer B-1, C-1, C-8, C-9
counters B-1, B-5, C-2

D

data bus interface 2-2
data ports C-3
data register 2-2, C-1, C-2, C-3, C-4, C-7
DMA 2-3, A-1

E

Electrostatic Sensitive Device 3-1
emulation 2-3, C-1
enable/disable 2-4
EPLD Altera device 2-2
external clock 2-1, 2-2, 2-3, 2-4, B-5, C-9, C-16, C-17
external clock signal 4-8

F

free run C-12, C-14
frequency measurement 2-4

H

hold cycles A-1
humidity A-2

I

I/O address map C-2, C-3
I/O locations A-1
I/O read 2-2, 4-3, A-1, C-1, C-7
I/O registers 2-3
I/O transfer 2-3, A-1
I/O write 2-3, 4-7
ID address space C-1, C-2
ID PROM 2-2, 2-3, C-1
ID read 2-3, 4-2, C-1
ID transfer 2-3, A-1
ID write A-1
installation 3-2, 3-3
internal clock 2-1, 2-3, C-9
interrupt 2-1, 4-5, C-1, C-2, C-3, C-11, C-12, C-13, C-14, C-15, C-16
interrupt enable C-1
interrupt enable register C-11, C-12, C-13, C-14, C-15, C-16
interrupt request A-1
interrupt request signal 4-5, 4-6
interrupt status C-1, C-2, C-1, C-2, C-3, C-4, C-11, C-12
interrupt status register 4-7, C-3, C-4, C-11, C-12
interrupt vector C-1
interrupt vector register C-3, C-4, C-12, C-13, C-14, C-15, C-16
interrupt vector transfers A-1
interrupt-related register C-1
IP Module 1-1, 2-1, 2-2, 2-3, 3-1, 3-2, 3-3, 3-4, 3-5, 4-1, 4-4, A-1, B-1, C-1, C-2, C-3, C-5, C-6, C-12
  singlewide 2-1
IP Module carrier 2-2, 3-2, 3-3

L

logic analyzer 4-1
  snapshot 2-2, C-7

M

manuals 3-1
measurements A-1
memory transfers A-1
memory 2-3
MTBF A-2
multiplexer 2-2

N

N_ACK 4-2

O

output trigger 2-3

P

pin assignments 3-3
power..... A-2, C-7, C-8, C-9, C-10, C-11, C-12
power-up.... 2-3, C-7, C-8, C-9, C-10, C-11, C-12
primary activity controller..... 2-3
processor reset C-13
programming 2-1, B-1, B-3, C-1
pulse width B-1, C-15, C-16

R

register.....2-1, 2-2, 2-3, C-1, C-2, C-3, C-7, C-8, C-9, C-10, C-11, C-12
registers
  terminal count..... 2-1
reset the timer C-8, C-13
response time.....4-2, 4-3
rising edge 2-4, 4-8
rollover 2-1

S

sampling period.....B-3
signal flow 2-2
singlewide..... 2-1
snapshot.....C-1
square wave C-14
state waveforms..... 4-1
status bit C-11
supply voltage A-2

T

temperature A-2
terminal count registers.....A-1
terminal count 2-1, 2-2, 2-4, 4-6
timer 1 ..... B-1, B-3, C-15, C-16
timer 2 ..... B-1, B-3, C-15, C-16
timer enable..... C-2, C-3, C-4, C-8
timer mode C-1
timer registers.....C-1
timer 2-1, 2-3, 2-4, B-1, B-3, C-15, C-16
transfer sequence engine 2-3
transfers.....2-2
trigger pulse output signal.....C-13
trigger pulse C-13
trigger signal 2-4, B-1

W

wait cycles.....A-1
watchdog timer.....C-13
waveform generator B-1
weight.....A-1

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP