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RAMplex™

RX78/RX78e
PCI, PMC, CPCI & VMEbus
Hardware Reference

Document No. E-T-MR-78PCPMCP-A-0-A4

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1. INTRODUCTION

1.1 How To Use This Manual

1.1.1 Purpose

This document is a reference manual for the RAMplex RX78 and RX78e PCI, PMC, CompactPCI (CPCI), and VME network interface cards (NIC). It provides a physical and functional description of the RAMplex NIC and describes how to unpack, set up, install and operate the hardware. Hereafter in this manual, "RAMplex" will refer to both RX78 and RX78e unless otherwise noted. CompactPCI is referred to as CPCI.

1.1.2 Scope

This information is intended for RAMplex systems designers, engineers and network installation personnel. You need at least a systems level understanding of general computer processing, memory and hardware operation, and specific host processor characteristics to effectively use this manual.

1.1.3 Style Conventions

- Hexadecimal values are written with a "0x" prefix: for example, 0x03FF.
- Switch, signal and jumper abbreviations are in capital letters; for example, RSW1, J5, etc.

1.2 Related Information

- *EZ SCRAMWare Programmer's Reference Guide*
  (Doc. No. E-T-ML-PROGREF)—A collection of routines to assist RAMplex users with application development.
- *RAMplex Mini Hub Hardware Reference Manual*
  (Doc. No. E-T-MR-RXMINI)—The RAMplex Mini Hub provides for RAMplex Network ring integrity and fault isolation for up to eight nodes.
- *Shared Memory Network Monitor User Manual*
  (Doc. No. D-T-MU-SMNETMON)—The Network Monitor is a tool for measuring and diagnosing network performance.

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- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

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2. NETWORK OVERVIEW

2.1 Overview

This chapter provides an overview of a generic RAMplex network, including brief descriptions of its major characteristics.

2.2 RAMplex Network

The RAMplex network is a real-time communications network, based on a replicated, shared-memory concept. Each host processor on the network has access to its own local copy of shared memory that is updated over a high-speed ring network. The network is optimized for high-speed data transfer among multiple computers. The protocol is a register-insertion methodology and multiple nodes can transmit data simultaneously. There is no master node, and all nodes have equal priority for network bandwidth. The message protocol is designed specifically for real-time applications where data may be passed very rapidly.

The RAMplex network doesn't require supporting network protocol or system software, nor network-dependent application software. Additionally, the RAMplex network has the following features:

- A ring topology with 77.76 Mbit/s line transmission rate.
- 256-node capacity on each ring.
- Low and deterministic network latency.
- Easy to use shared memory interface.
- Network error detection.
- 1024 network interrupts for node synchronization.

2.3 Shared Memory

The RAMplex network is a broadcast shared-memory network. Each computer on the network has a local copy of all data passed to the network computers. The network protocol is implemented in the RAMplex hardware and therefore no software overhead is required to share data with other nodes or retrieve data from the network. Once the shared memory has been initially mapped to the software application, it can be accessed like normal memory. Writes to shared memory automatically update the corresponding memory locations of all other network nodes. Reads from the shared memory will return the value present in the local shared memory without requiring any network traffic. This allows data to be easily shared between computers without the overhead of complex network protocols or message passing software. Figure 2-1 illustrates the RAMplex network operation.

When an application writes to a RAMplex shared memory, the network card automatically generates a network packet that circulates around the network ring. When each node receives a packet, it automatically updates the shared memory with the new value. A packet can contain up to 64 bytes of data. This packet travels around the network updating each node with the correct memory value. When the originating node receives the packet, it removes the packet from the network. Unique Node ID's are used for message removal.

In normal operation, a write to the RAMplex network card updates the local on-card shared memory and then automatically transmits a network packet, which is replicated around the network ring updating the memory on all other network nodes. The RAMplex network can also be used in Write-Me-Last mode. When configured in this mode, a write to the network card will transmit the network packet, but the local on-card shared memory is only updated after all other network nodes have been updated. This mode is described further in section 2.7.

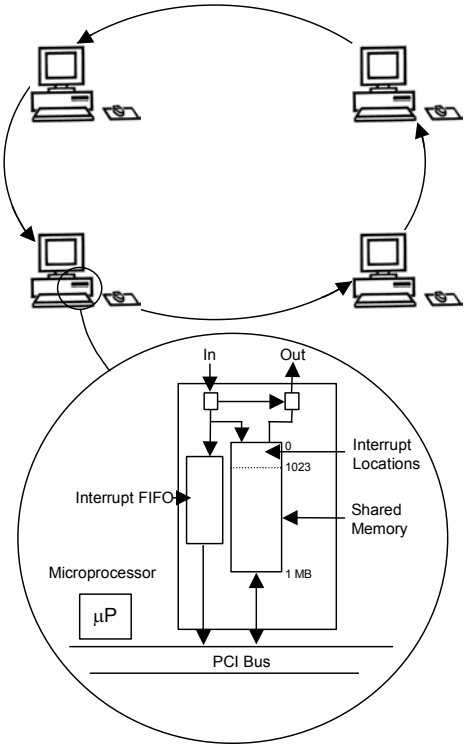


Figure 2-1 RAMplex Network Operation

2.4 Network Ring

The RAMplex network is a ring topology network. Data is transmitted at a rate of 77.76 Mbits/s over fiber-optic cables. Due to the network speed and packet size, the network can accommodate over 930,000 packets passing by each node every second. A RAMplex network can accommodate up to 256 nodes per network ring.

2.5 Error Detection

The RAMplex network automatically checks all incoming network packets for errors. These errors include signaling errors (for example; missing transitions, parity error, or framing error) or insufficient power from the previous transmitter. If an error is detected, the corresponding packet is automatically removed from the network.

2.6 Interrupts

RAMplex uses interrupts for two purposes:

- To interrupt other nodes for application synchronization
- To notify the processor if an error was detected on the local node

These interrupts are known as network data interrupts and error interrupts, respectively.

2.6.1 Network Data Interrupts

The first type of interrupt is a network data interrupt. The first 1024 locations of RAMplex memory are interrupt locations. Any write to the first 1024 memory locations will cause an interrupt message to be sent on the network. Any nodes that have network interrupts enabled will generate an interrupt when an interrupt message is received. A FIFO is used to buffer the interrupt messages received on a node. The interrupt service routine (ISR) will typically call a user-supplied interrupt handler, which will dequeue the entries from the interrupt FIFO. The interrupt FIFO contains the addresses of the interrupt locations that were sent by other nodes on the network.

Writes to the first 1024 memory locations, which cause network interrupts, still update shared memory on all nodes in normal shared-memory fashion. It behaves as the rest of the RAMplex shared memory with the added ability that any nodes who have network interrupts enabled will receive an interrupt when other nodes write to the interrupt locations. Having 1024 interrupt locations gives the system designer a great deal of flexibility in inter-nodal synchronization and notification of asynchronous events. Since the interrupt locations can be read like normal shared memory, each interrupt location can be used as an "interrupt vector," which contains specific information (user-defined) on the interrupt event.

For example, location 3 (the third longword of RAMplex memory) could be designated as synchronization location for a cyclical simulation. One node acting as the system timer will write to this location on a pre-determined interval (for example, every 10 ms). The other nodes have network interrupts enabled and will generate an interrupt when the location is written to. When the nodes receive the interrupt, they could read the interrupt location if necessary (indicating the number of the simulation frame sequence for example) and perform whatever processing is dictated by the specific application.

Writes to the first 1024 locations always generate an interrupt message. However, each node must enable network interrupts in order for interrupt message to actually assert a local interrupt when these messages are received. Each node can decide whether to enable network interrupts via a software routine. If enabled, any network interrupt message asserts a local interrupt and the address of the location that was written to will be stored in an interrupt FIFO.

2.6.2 Network Error Interrupts

Network error interrupts allow a node to be notified when a network error or condition occurs. The error interrupts can be selectively enabled via software. When enabled, an interrupt will be generated if the specific condition occurs. The software can be used to identify and clear the occurring condition.

Table 2-1 Network Error Interrupts

Error Condition	Cause
Transmit FIFO Full:	More data coming from the host to the network than the network can absorb. When the Transmit FIFO is full, host writes will be automatically held off by the NIC until the Transmit FIFO is no longer full.
Transmit FIFO Not empty:	This does not represent any type of error condition, but rather a report on the state of the Transmit FIFO. When this occurs, there is at least one message in the FIFO waiting to be sent on the network. This is typical during normal operation.
Transmit FIFO 7/8 Full:	The Transmit FIFO is backing up and is more than 7/8 full. This can occur when the network load if high.
Interrupt FIFO Full:	The Interrupt FIFO is full. Interrupt messages are being generated at a rate which the local application cannot handle.
Protocol Violation:	There has been a signaling error at this physical layer. Missing transitions, a parity error, or a framing error can cause it.
Carrier Detect:	The receiver does not detect enough output from the previous transmitter. This is usually an indication that a "upstream" node is powered-off, a fiber-optic cable has become disconnected, or there is dust/dirt where the fiber-optic cable connections have been made.
Bad Message:	The hardware has detected an error in the message packet received on the network. If this error persists, it is an indication that a hardware problem may exist.
Receiver Overflow:	The Receive FIFO has received more data that the node is able to process. This condition may indicate a hardware problem.
Transmit Retry:	The message returned to the originating node with bit errors. The message is automatically retransmitted indefinitely until it returns without bit errors. This occurs when the node is operating in error-correction mode and the network operation is not error free.
Transmit Retry Time-out:	The message did not return to the originating node within the specified time-out value. The message is automatically retransmitted indefinitely until it returns without error. This occurs when the node is operating in error-correction mode and the network operation in not error free or the specified time-out value was too low for the specific network configuration.

2.7 Write-Me-Last Mode

The Write-Me-Last mode of operation allows the originating node to be the last node in the ring to have the data deposited to its memory. This can be useful for synchronization. This means that when the host performs a write to the RAMplex shared memory, the data is not immediately written to the host node's memory, but is first sent to the other nodes on the network. When the message returns to the originating node it is written to shared memory, and is then removed from the network ring.

Therefore, host-originated data written to shared memory travels the ring updating the RAMplex node memories. Upon returning to the originating node, the node writes the data to its own shared memory as the last node on the ring. The application can write the value to shared memory and continue reading until the new value is read-back. This guarantees the data is now available on all other nodes. While this is not required for most applications, it can be useful in certain scenarios. Write-Me-Last Mode can be enabled via software.

2.8 Data Filter

Many implementations of shared memory tend to rewrite data values to memory that have not actually changed. In order to reduce network traffic, the RAMplex card compares the new value with the old value of data to avoid sending unchanged data values out on the network. This feature is a type of data filtering and can be enabled without affecting node latency while improving network throughput. Data filtering can be enabled via software.



CAUTION: The use of data filtering can cause unexpected results (as a result of outstanding network traffic) when used in conjunction with the Write-Me-Last mode. It is recommended that the two modes not be used together.

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3. PRODUCT OVERVIEW

3.1 Overview

This chapter provides an overview of the RAMplex cards.

NOTE: The RAMplex network is NOT hardware-compatible with Systran's SCRAMNet Classic, SC150, or SC150e family of network cards.

3.2 RAMplex Cards

3.2.1 RAMplex PCI Card

CAUTION: Check with the host computer manufacturer to find out which slots are available for third party PCI memory cards before installing the RAMplex network card into any system. Installing any type of PCI card in a non-standard PCI slot may result in serious damage to the host machine and/or PCI card.

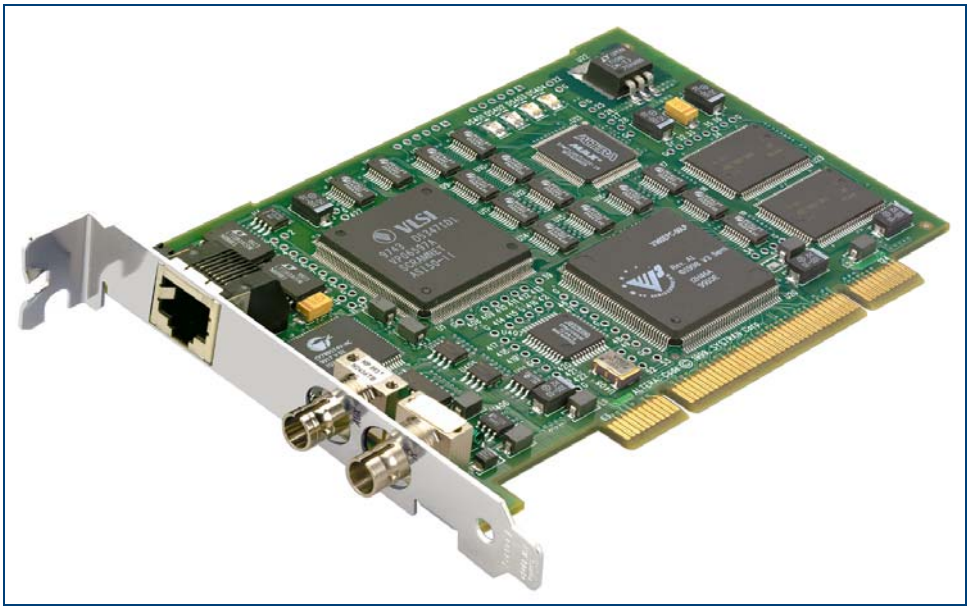


Figure 3-1 RAMplex PCI Card

The RAMplex PCI card offers the following features:

- RAMplex network interface.
- 32-bit PCI interface, maximum bus speed of 33 MHz.
- Supports PCI interrupt INTA.
- Compatible with Universal (both +5.0 V and +3.3 V) PCI signaling levels.
- Occupies a single PCI Short Card slot.
- 820 nm fiber-optic interface.
- Maximum node separation of 300 meters.

- 2 MB of on-card shared-memory.
- Sustained 3.4 MB/s network data transfer rate (RX78).
- Sustained 7.8 MB/s network data transfer rate (RX78e).
- On-card DMA controller.

3.2.2 RAMplex PMC Card

CAUTION: Check with the host computer manufacturer to find out which slots are available for third party PCI memory cards before installing the RAMplex network card into any system. Installing any type of PCI card in a non-standard PCI slot may result in serious damage to the host machine and/or PCI card.

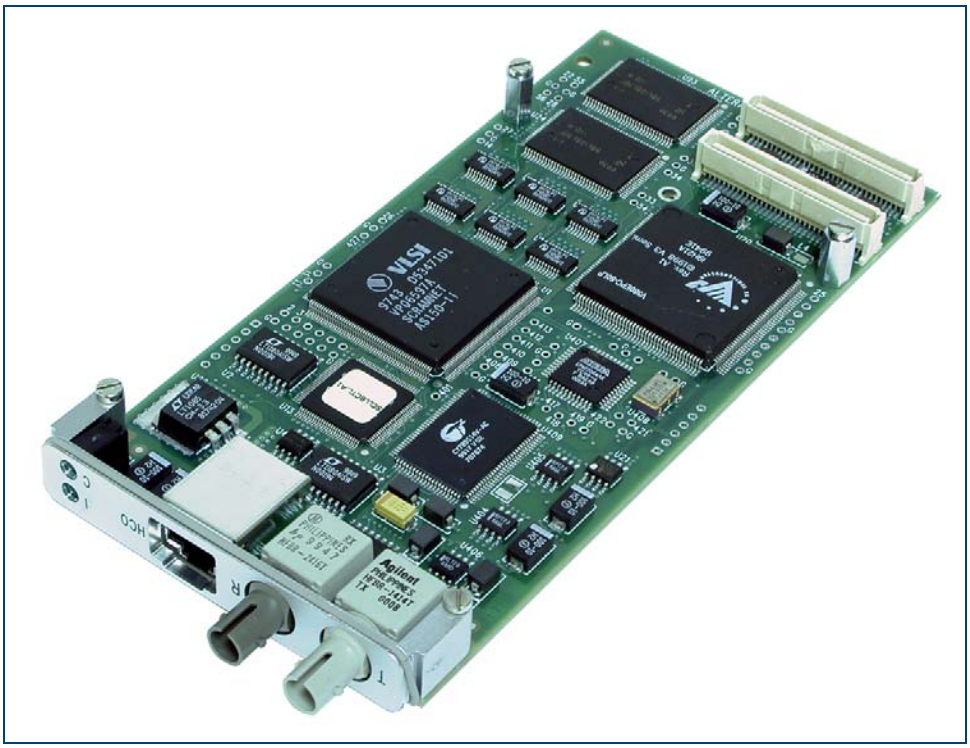


Figure 3-2 RAMplex PMC Card

The RAMplex PMC card offers the following features:

- RAMplex network interface
- 32-bit PCI interface, maximum bus speed of 33 MHz
- Supports PCI interrupt INTA
- Compatible with Universal (both +5.0 V and +3.3 V) PCI signaling levels
- 820 nm fiber-optic interface
- Maximum node separation of 300 meters
- 2 MB of on-card shared-memory
- Sustained 3.4 MB/s network data transfer rate (RX78)
- Sustained 7.8 MB/s network data transfer rate (RX78e)
- On-card DMA controller

3.2.3 RAMplex CPCI Card

NOTE: The 3U CompactPCI card provides a RAMplex network interface in a single 32-bit 33 MHz CPCI slot in the CompactPCI system.

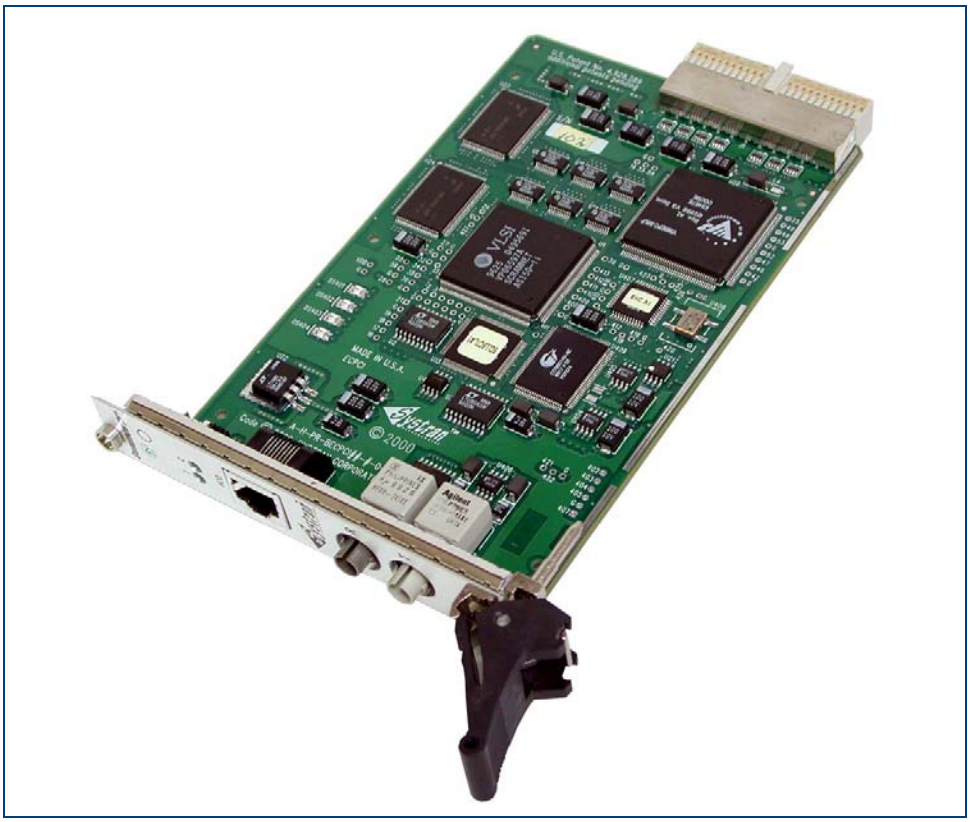


Figure 3-3 RAMplex CPCI Card

The RAMplex CPCI card offers the following features:

- RAMplex network interface.
- 32-bit PCI interface, maximum bus speed of 33 MHz.
- Supports PCI interrupt INTA.
- Compatible with Universal (both +5.0 V and +3.3 V) PCI signaling levels.
- Occupies a single 3U or 6U CPCI slot.
- 820 nm fiber-optic interface.
- Maximum node separation of 300 meters.
- 2 MB of on-card shared-memory.
- Sustained 3.4 MB/s network data transfer rate (RX78).
- Sustained 7.8 MB/s network data transfer rate (RX78e).
- On-card DMA controller.
- Includes both 3U and 6U front panels.

3.2.4 RAMplex VME Card

See Appendix C for information about the RAMplex VME card using the RAMplex PMC card with the VMETRO MIDAS-20 VME carrier board

3.3 Product Features

3.3.1 Compatibility

The RAMplex RX78 and RX78e are software and hardware compatible products. However, the RX78e supports a higher throughput by increasing the size of the data from 4 bytes to up to 64 bytes in the network message, increasing the network efficiency and throughput. The RX78e may automatically combine data written to the network with sequentially incrementing 32-bit writes. This allows the network throughput to be increased from 3.4 MB/s to 7.8 MB/s. The actual network traffic is a function of the type of nodes on the network and the type of traffic patterns introduced by these nodes.

3.3.2 DMA

While the RAMplex network card is typically accessed via normal memory reads and writes (PIO accesses), this product also supports direct memory access (DMA). The RAMplex NIC has an on-card DMA controller. Once programmed, the DMA controller can transfer data from system memory to RAMplex memory or from RAMplex memory to system memory. By transferring data without host intervention, this frees the host processor for other tasks such as processing data. The DMA is also capable of transferring data out of shared memory into system memory at a much faster rate than most processors could achieve with PIO operations. Library software routines may be called to configure the DMA controller.

One feature of the RAMplex network is that it can be used like normal memory after configuration. However, using DMA requires more considerations in the organization of the shared memory. The ideal scenario is when data is read from and written to shared memory in relatively large blocks of sequential data. The system architect can decide to use the typical PIO approach with RAMplex shared memory, to use DMA to transfer data to/from the shared memory, or a combination of the two approaches depending on the particular application.

3.3.3 Prefetching

The RAMplex NIC uses prefetching to optimize read performance from shared memory. The on-card controller speculates that additional read transfers will occur and performs burst reads from shared memory to fill the FIFO with data from subsequent locations. This can dramatically increase the PIO read performance when reads from shared memory are performed sequentially. While performing sequential reads will result in faster read performance, the system architect can design the application to read shared memory however and whenever it is necessary or appropriate. Many systems read from the shared memory in a “random” fashion.

To maintain data coherency, the on-card controller is configured so that writes have priority over reads, and to prevent write data from remaining in the FIFO. There is one scenario that needs to be recognized. If an application reads from a location and at a much later time reads from the subsequent location without having performed any other writes or reads, the read value returned will be from the prefetch FIFO which may not be correct if the shared memory has since been updated. Most applications are not written in this fashion; they typically benefit from prefetching, even if the data is mostly “randomly” accessed. If the system designer is concerned about data coherency in the situation outlined above, on-card prefetching can be disabled via software.



NOTE: Many modern computers use prefetching to optimize system performance. While the RAMplex card's on-card prefetching may be disabled, the microprocessor and/or on-card controller may also prefetch data. The use of prefetching and/or ability to disable prefetching at other levels in the system is system dependent.

3.4 Connectors

3.4.1 Tx and Rx

The Tx and Rx connectors are used for physical connection to the RAMplex network. The Tx connector is the network transmitter output for the RAMplex NIC. It is labeled "T" on the faceplate. The Rx connector is the network receiver input. It is labeled "R" on the faceplate.

3.4.2 Hub Control Output

The Hub Control Output connector is a proprietary interface reserved for future use.

3.5 LEDs

3.5.1 Carrier Detect Led

The green Carrier Detect LED is ON when there is a valid transmit light from the previous RAMplex node into this node's receiver. Assuming at least one node is inserted in the ring, the ring integrity is NOT valid if the fiber-optic cables are connected and the Carrier Detect LED is OFF. This condition indicates improper fiber-optic cabling or problems with the down-line node's transmitter(s). This LED is labeled "C" on the faceplate.



NOTE: On a system power-up, a message from any node on the ring may be necessary to establish the carrier.

3.5.2 Insert Led

The green Insert LED is ON when the node is inserted into the RAMplex network ring. A node is inserted when it is electrically placed on the network for the purpose of transmitting and receiving messages. This LED is labeled “I” on the faceplate shown in Figure 3-4 through Figure 3-7.

RAMPLEX PCI CARD

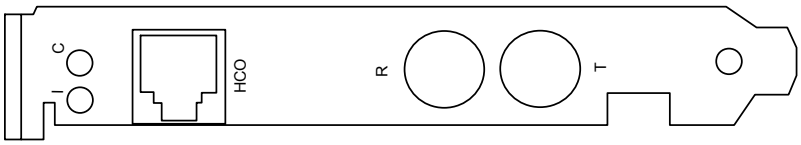


Figure 3-4 RAMplex PCI Faceplate

RAMPLEX PMC CARD

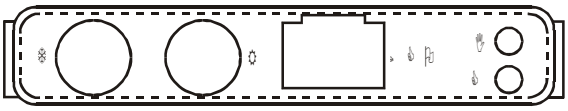


Figure 3-5 RAMplex PMC Faceplate

RAMPLEX CPCI CARD

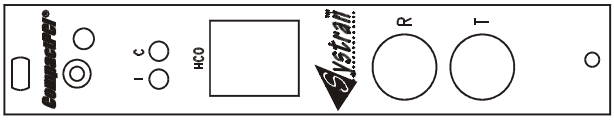


Figure 3-6 RAMplex 3U Faceplate



Figure 3-7 RAMplex 6U Faceplate

3.5.3 Factory LEDs

There are also four green surface mount LEDs located on the RX78 NIC. These LEDs are used for factory-level testing. These LEDs have no significance during normal product operation.

3.6 Options

3.6.1 Part Number

The RAMplex card part number is in the form:

H-AS-EPCIN02M-20 (Standard PCI w/2 MB RAM)
H-AS-EPCIE02M-20 (Enhanced PCI w/2 MB RAM)

where:

Code	Definition
H	Hardware
AS	Top Level Assembly
EXXXN	Standard RX78 Series Card
	PCI = PCI card
	PMC = PMC card
	CPC = CPCI card
	VME = VME card
EXXXE	Enhanced RX78 Series Card
	PCI = PCI card
	PMC = PMC card
	CPC = CPCI card
	VME = VME card
YYY	**Memory (bytes)**
	02M = 2 MB
20	**Transmission Media.** Standard FO media

3.6.2 Fiber-Optic Cables

Fiber-optic cables may be purchased from Systran or third parties. The recommended fiber-optic cable is 62.5/125 micron core multi-mode fiber-optic cable with ST connectors. Contact Systran regarding the availability of fiber-optic cables.

3.6.3 Hubs

The RAMplex Mini Hub is useful in applications where fault-tolerance or network reconfiguration is necessary. See the *RAMplex Mini Hub Hardware Reference Manual* for more details. Contact Systran regarding the availability of these products.

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4. INSTALLATION

4.1 Installation

This chapter describes the installation of the RAMplex card. Installation requires the following steps:

- Unpack the card.
- Visually inspect the card.
- Install the card.
- Configure and connect cabling.

4.2 Unpack the Card

Perform the following steps to unpack the card:



CAUTION: Exercise care regarding the static environment. Use an anti-static mat connected to a wristband when handling or installing the RAMplex card.

1. Remove the anti-static bag from the carton.
2. Remove the host card from its anti-static bag encased in anti-static foam.
3. Open the anti-static bag and remove the host card.

Save the shipping material in case the RAMplex card needs to be returned.

The optional fiber-optic cables, and RAMplex Mini Hub is shipped in separate cartons.

4.3 Visually Inspect the Card

Check the card for any damage that may have occurred during shipping. In the event that any shipping damage has occurred, call Systran Technical Support.

4.4 Install the Card

Node configuration is pre-set or defined in the configuration file. Therefore, after the card has been inspected it is ready to be installed.



CAUTION: Make certain that the power to the host computer is OFF.

1. Remove the bulkhead cover plate where the RAMplex host card will be.
2. (**RAMplex CPCI only**) Select the 3U or 6U faceplate. To replace the 3U faceplate with the 6U faceplate:

   Using a standard Phillips-head screwdriver, remove the two holding screws, remove the 3U faceplate, position the 6U faceplate on the card, and reinsert the holding screws.

3. (**RX78 PMC only**) Mount the PMC card on a motherboard, adapter, or carrier board.

   Slide the card into a desired peripheral bus slot while applying enough force to ensure a tight fit into the backplane connector. After insertion, use a standard Phillips-head screwdriver to secure the faceplate onto the frame of the computer chassis.
4. Connect the Transmitter and Receiver fiber-optic cables to the RAMplex NIC.

4.5 Configure and Connect Cabling

4.5.1 Fiber-optic Configuration

The basic RAMplex network communication architecture consists of RAMplex cards tied together by fiber-optic cable in a ring configuration. The maximum recommended distance between each node of the network using this configuration is 300 meters. The recommended fiber-optic cable is 62.5/125 micron core multi-mode fiber cable with ST connectors.

4.5.2 Fiber-optic Cables

The optional fiber-optic cables are shipped in a separate carton. The fiber-optic cables are to be attached to the connectors on the RAMplex card. Remove the rubber boots on the fiber-optic transmitter and receiver as well as the ones on the fiber-optic cables. These rubber boots should be replaced when cables are not in use or in the event the node must be returned to the factory.

It is important the ends of the fiber-optic cable be kept clean. If there is an exceptional amount of light-power loss experienced, the cable ends should be inspected for cleanliness. Alcohol-based fiber-optic cleaning pads are available to remove minor contaminants such as dust and dirt.

Figure 4-1 is a representation of a fiber-optic connector.

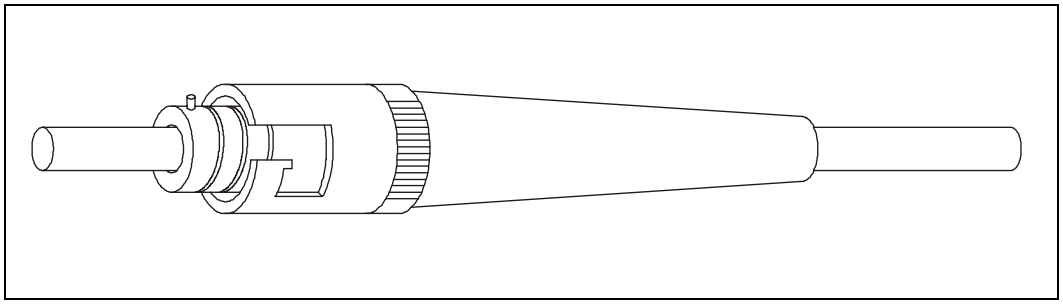


Figure 4-1 Fiber-optic ST Connector

4.5.3 Fiber-optic Connection

There are two types of “bayonet” fiber-optic connectors used on ST fiber-optic cables. The newer type is made by 3M and is smaller than the AT&T ST connector. Install the connector by pushing it onto the card connection and twisting the connector to the right (clockwise) to engage the blade. Remove it by pressing the metal sleeve toward the card and twisting to the left (counter-clockwise) to disengage the blade.

The primary difference between the connector types is that the AT&T connector provides a “locking” mechanism. Before it can engage or disengage the blade on the card connection, the plastic boot must be unscrewed at least ¼ inch and then retightened.

The fiber-optic cable transmitter of the up-stream node is connected to the receiver of the down-stream node. Data flows from the transmitter of one node to the receiver of the next node as described below in Figure 4-2.

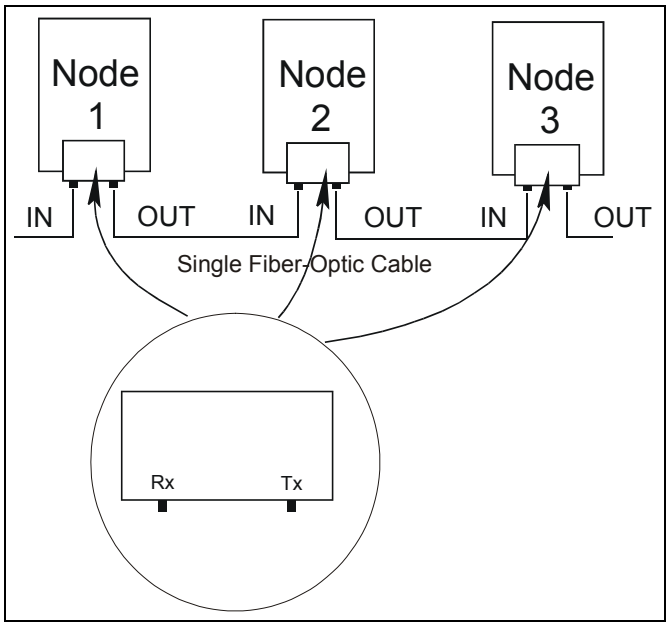


Figure 4-2 RX78 Fiber-Optic Connections

FIBER-OPTIC CABLE PRECAUTIONS

Fiber-optic cables are made of glass and may break if crushed or bent in a loop with less than a 2-inch radius.

Perform a visual check of the cable ends before inserting into the transmitter/receiver connector. If debris is inserted into the transmitter/receiver connector it may not be possible to clean it out or could result in damage to the transmitter or receiver lens. Hair, dirt and dust can interfere with the light signal transmission.

Use an alcohol-base wipe to clean cable ends.

4.6 Maintenance

No routine maintenance is required for the RAMplex general-purpose nodes beyond host computer system requirements. Network fiber-optic cabling connectors should be inspected periodically.

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5. OPERATION

5.1 Overview

This chapter describes RAMplex operations.

5.2 Node IDs

Regardless of the network topology, the network administrator or system architect must ensure that each node used on the network has a unique node ID. Typically, the node ID is set using a software routine.



CAUTION: Unpredictable results may occur if two cards have the same Node ID (see Troubleshooting section).

5.3 Memory Considerations

RAMplex memory becomes part of host system memory. Therefore, any limitations on application program size and data variable size for host system memory also apply to RAMplex memory.

For most modern computer architectures using cache memories to improve system performance, the RAMplex network card can affect performance. The problem may arise because the RX78 is mapped in host memory space and can be updated by memory writes on other nodes without the system's knowledge. Although the use of caching is system dependent, configure your computer so host memory space is not cached. However, if you disable all cashing on your system, you will see a considerable decrease in system performance. Fortunately, it is usually not necessary to totally disable all caching on a system.



NOTE: Most personal computers do not cache host memory space. If there is any question, check with the manufacturer to determine if host memory space is cached and, if so, what mechanism can be used to disable it.

Similarly, many compilers perform optimizations to improve code performance and/or reduce code size. As a result, a compiler can eliminate accesses to RAMplex memory because it does not know the memory can be changed without its knowledge and it may eliminate necessary code. You need to consider this issue when designing applications. For example, if writing in the 'C' programming language, you should use the "volatile" declarator with variables, pointers, and arrays that access RAMplex memory to prevent the compiler from optimizing these accesses. This is a much better approach than disabling all compiler optimizations.

5.4 8-bit and 16-bit Accesses

The RAMplex NIC supports 8-bit, 16-bit (shortword), and 32-bit (longword) PCI transfers. However, since every write to shared memory initiates network traffic, a 32-bit variable transferred a byte at a time will require four network messages. Similarly, four

byte writes to the same longword interrupt location would generate four separate interrupts to the same longword address. Therefore, 32-bit transfers maximize PCI bus and RAMplex network usage. (There are no issues with byte swapping since the RAMplex network is only offered on little-endian PCI buses). Finally, if an 8- or 16-bit write occurs from the host system, then the 32-bit word that contains that 8- or 16-bit write is sent on the network. Therefore, it is important that other nodes do not simultaneously modify other 8- or 16-bit segments within that 32-bit word.



NOTE: Since the RAMplex network is a longword (32-bit) oriented shared memory, interrupts will occur when any of the four bytes associated with a longword are accessed. The interrupt FIFO contains the longword address. If each of the four bytes of an interrupt location are written into as byte accesses, then four interrupts to the same longword address will be generated. Likewise, if each word of an interrupt location is written into as 16-bit shortwords, then two interrupts to the same longword address will be generated.

5.5 Network Time-out Value

The RAMplex network has an optional error-correction capability. If you select this mode, the originating node retransmits network packets if the packets have errors when the originating node removes them from the network. This will also occur if the originating node does not receive the packet within a specified period of time. You must specify a time-out period for the error-correction operation. The time-out period is based on the number of nodes in the network ring and the total length of cable used. The recommended value for the Network Time-out is:

```
#NODES IN RING * 1.2 + (TOTAL LENGTH OF CABLE IN METERS / 96) +1
```

This number should be rounded up to the nearest integer. You can program the transmit retry time-out value through a software routine.

5.6 Latency

Latency is a measure of network data transfer delay, and is a hidden performance factor in the system design of real-time networked applications. For example, the network interface circuitry and the propagation delay of the fiber-optic cabling introduce delays in the transfer of data among computers on the RAMplex network.

5.6.1 Types of Latency

TRANSMIT LATENCY

The transmit latency is the time necessary to send a packet onto the network after a shared memory write access is performed. For an idle network, the transmit latency is 995 ns. For a non-idle network, the transmit latency may increase as the node may have to wait to insert the packet onto the network.

PASS-THROUGH LATENCY

The pass-through latency is the time necessary to retransmit an upstream node's packet. If a node retransmits a packet but is not transmitting its own packet when the upstream packet arrives, the pass-through latency is 625 ns. If a node retransmits a packet and is already transmitting its own packet when the upstream packet arrives, it finishes transmitting its packet before it can retransmit the upstream packet. In this case, the pass-through latency could be up to 1686 ns.

RECEIVE LATENCY

The receive latency is the measure of time necessary to update shared memory when an incoming packet arrives. The receive latency is 995 ns.

NETWORK LATENCY

The network latency is the time it takes after a write to shared memory to send the packet around the ring and remove it at the source. This includes the time it takes for all nodes on the network to be updated with the new data. On an idle network, the network latency can be approximated with the following formula:

```
NETWORK LATENCY = 1.99 µs + (N-1)*0.625 µs + L*5 µs/km
```

where:

N is the number of nodes on the network
L is the total length of network cabling used in kilometers



NOTE: This formula does not include any delays as a result of using a hub, which would include the time necessary to synchronize and retransmit the received signal through a hub.

5.6.2 Data Transfer

While the RAMplex network appears as a shared-memory system, it is still a data network. The RAMplex network includes a series of FIFO buffers to collect data changes until they are transmitted to the other nodes. The Transmit FIFO and the Interrupt FIFO are both 1024 messages in length. These numbers may become significant when performing data transfers of large blocks of data in a short period of time.

5.7 Throughput Performance

5.7.1 Network Throughput

When using the RAMplex RX78 card, the network supports a maximum network throughput of 3.4 MB/s. When using the RAMplex RX78e card, the network throughput is 7.8 MB/s. When a single node is transmitting data, the node can utilize all of the network bandwidth, assuming the host CPU can offer the data at that rate. When multiple nodes are transmitting data, the network throughput will be shared among the transmitting nodes.

5.7.2 Host Throughput

Host throughput is the measure of how fast an application can access RAMplex shared memory on a sustained basis. Host throughput performance numbers are system dependent and will vary from system to system. Variables affecting performance are the software application (including direction and nature of memory accesses), system platform (including microprocessor and PCI controller), RAMplex PCI access speeds, and RAMplex network traffic.

Writes to RAMplex shared memory initiate network traffic and therefore are influenced by the amount of traffic on the network. While reads from RAMplex do not initiate network traffic, they require access to the on-card shared memory and are also influenced by the amount of traffic on the network. Reads can occur at a faster rate than the network can sustain—this allows additional time for the host system to process network data.



NOTE: Systran Corporation offers a network analysis tool that measures throughput latency performance. See the *Shared Memory Network Monitor User Manual* for more information.

5.8 EZ SCRAMWare

The EZ SCRAMWare software library is a collection of basic functions designed to help engineers in application development. These high-level routines allow applications to work with the RAMplex products by providing the required accesses. You can access the EZ SCRAMWare Interface Library routines from any user-written program. The *EZ SCRAMWare Programmer Reference Guide* describes how to use these features.

5.8.1 Map the Hardware

The first step in programming the hardware is to map the card into the host system as a physical device. Although this process is specific to each host platform environment, the EZ SCRAMWare application programming interface (API) library routines perform this physical mapping for the host environment. The driver can allocate memory up to 32 MB for a single hardware device.

5.8.2 Unique Physical Interfaces

The hardware interrupts and other physical interfaces are host-system specific and must be recognized by the host system for proper hardware operations. The EZ SCRAMWare routine *snInit()* performs all the necessary mapping functions. EZ SCRAMWare's other functions allow you to access and set up the card, and to perform other necessary operations.

5.8.3 Map Multiple Devices

The EZ SCRAMWare API library supports multiple hardware devices from within a single user application. All API functions take the first parameter as the card number. Card numbers are assigned in the order of the driver scanning the PCI bus. If the card is not found on the system during any access, the function returns an error.

5.9 Testing/Troubleshooting

5.9.1 RAMplex PCI

Problem:	Solution:
The hardware installation fails	–The RAMplex host card is not installed into a standard PCI slot. (This check should have been performed before installing the RAMplex PCI host card into any slots).
The carrier detect LED is not on.	–Make sure all nodes connected to the network are powered-on, and cabled correctly. –Swap out damaged cables
The system does not boot correctly	–Reset the card and double-check cable connections. –If problems persist, call Systran Customer Support at (800) 252-5601 for assistance.
Any other problems	–Call Systran Customer Support at (800) 252-5601 for assistance

5.9.2 RAMplex PMC

Problem:	Solution:
The hardware installation fails	–The RAMplex host card is not installed into a standard PMC slot. (This check should have been performed before installing the RAMplex PMC host card into any slots).
The carrier detect LED is not on.	–Ensure all nodes connected to the network are powered-on, and cabled correctly. –Swap out damaged cables.
The system does not boot correctly	–Reset the card and double-check cable connections. –If problems persist, call Systran Customer Support at (800) 252-5601 for assistance.
Not all nodes receive memory updates	–Ensure all Node ID's are unique. –Check for broken fiber-optic cable.
High network latency	–Ensure all Node ID's are unique, and –Ensure all Transmit and Receive Node ID's are the same. –Check for broken fiber-optic cable.
Any other problems	–Call Systran Customer Support at (800) 252-5601 for assistance.

5.9.3 RAMplex CPCI

Problem:	Solution:
The hardware installation fails	–The RAMplex host card is not installed into a standard CPCI peripheral slot. (This check should have been performed before installing the RAMplex CPCI host card into any slots).
The carrier detect LED is not on.	–Make sure all nodes connected to the network are powered-on, and cabled correctly. –Swap out damaged cables
The system does not boot correctly	–Reset the card and double-check cable connections. –If problems persist, call Systran Customer Support at (800) 252-5601 for assistance.
Any other problems	–Call Systran Customer Support at (800) 252-5601 for assistance

5.9.4 RAMplex VME

Refer to the RAMplex PMC card and Appendix C for troubleshooting information.

APPENDIX A

SPECIFICATIONS

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FIGURES

Figure A-1 PCI Dimensions A-2
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Figure A-3 CPCI Dimensions A-6

A.1 RAMplex PCI

A.1.1 Hardware Specifications

Hardware Compatibility: ..... PCI local bus specification, rev. 2.1
Physical Dimensions:
- PCI Card..... 3.695" x 5.430"

Weight:
- PCI Card..... 0.206 lb.

PCI Bus Speed ..... 0-33 MHz
PCI Bus Width..... 32 Bits
PCI Signaling Levels ..... Universal (+5 V and +3.3 V support)
PCI Interrupt Line..... INTA
PCI Vendor ID: 0x11B0
PCI Device ID:..... 0x4750
PCI Subsystem Vendor:..... 0x1387
PCI Subsystem ID:..... 0x5302
Electrical Requirements:..... +4.75 to +5.25 VDC, 1.5 Amps max.
Temperature Range
- Storage: ..... -40° to +70°C
- Operation:..... 0° to +60°C

Humidity Range:
- Storage ..... 0% to 95% (noncondensing)
- Operating..... 10% to 90% (noncondensing)

Network Line Transmission Rate: ..... 77.76 million bits/second
Maximum Nodes on Network Ring:..... 256
Error Correction:..... Available in PLATINUM mode only
Maximum Node Separation:
- Standard Fiber:..... 300 meters
- Factory installed memory:..... 2 MB

RX78 Effective Network Bandwidth:..... 3.4 MB/s
RX78e Effective Network Bandwidth:..... 7.8 MB/s
Latency:
- Pass-through latency: ..... 625 ns
- Transmit latency:..... 995 ns (idle network)
- Receive latency: ..... 995 ns
- Transmission media delay (fiber-optic): .... 5 ns/m

Mean Time Between Failures (MTBF): ..... 247,947 hours

A.1.2 Card Dimensions

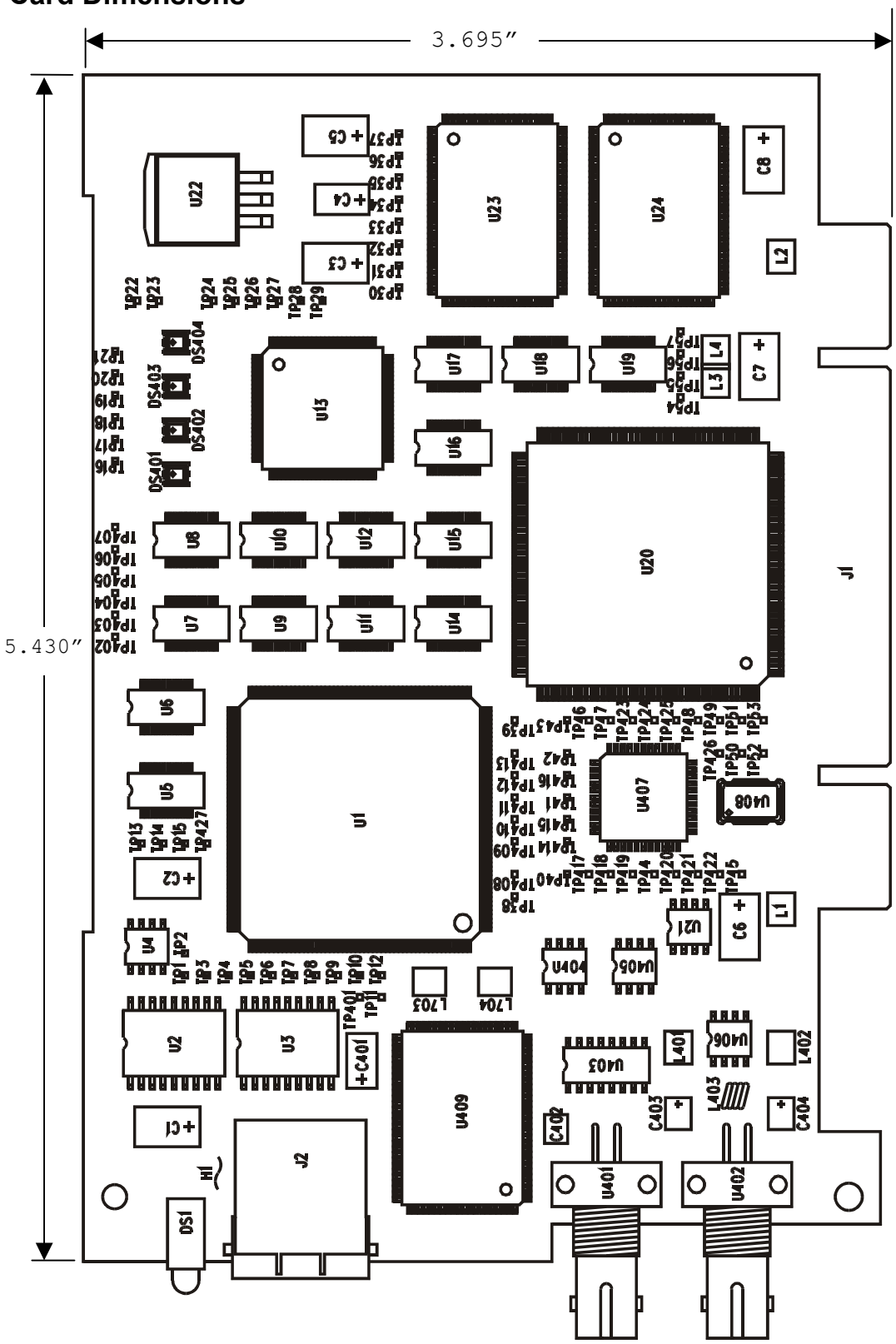


Figure A-1 PCI Dimensions

A.2 RAMplex PMC

A.2.1 Hardware Specifications

Hardware Compatibility:	PCI local bus specification, rev. 2.1 Draft standard for a common mezzanine card family: CMC (IEEE P1386/Draft 2.0) Draft standard physical and environmental layers for PCI Mezzanine cards: PMC (IEEE P1386/Draft 2.0)
Physical Dimensions:	
PMC Card	2.91" x 5.86"
Weight:	
PMC Card	0.2 lb.
PMC Bus Speed	0-33 MHz
PMC Bus Width	32 Bits
PMC Signaling Levels	Universal (+5 V and +3.3 V support)
PMC Interrupt Line	INTA
PMC Vendor ID:	0x11B0
PMC Device ID:	0x4750
PMC Subsystem Vendor:	0x1387
PMC Subsystem ID:	0x5302
Electrical Requirements:	+4.75 to +5.25 VDC, 1.5 Amps max.
Temperature Range	
Storage:	-40° to +70°C
Operation:	0° to +60°C
Humidity Range:	
Storage	0% to 95% (noncondensing)
Operating	10% to 90% (noncondensing)
Network Line Transmission Rate:	77.76 million bits/second
Maximum Nodes on Network Ring:	256
Error Correction:	Available in PLATINUM mode only
Maximum Node Separation:	
Standard Fiber:	300 meters
Factory installed memory:	2 MB
RX78 Effective Network Bandwidth:	3.4 MB/s
RX78e Effective Network Bandwidth:	7.8 MB/s
Latency:	
Pass-through latency:	625 ns
Transmit latency:	995 ns (idle network)
Receive latency:	995 ns
Transmission media delay (fiber-optic):	5 ns/m
Mean Time Between Failures (MTBF):	247,947 hours

A.2.2 Card Dimensions

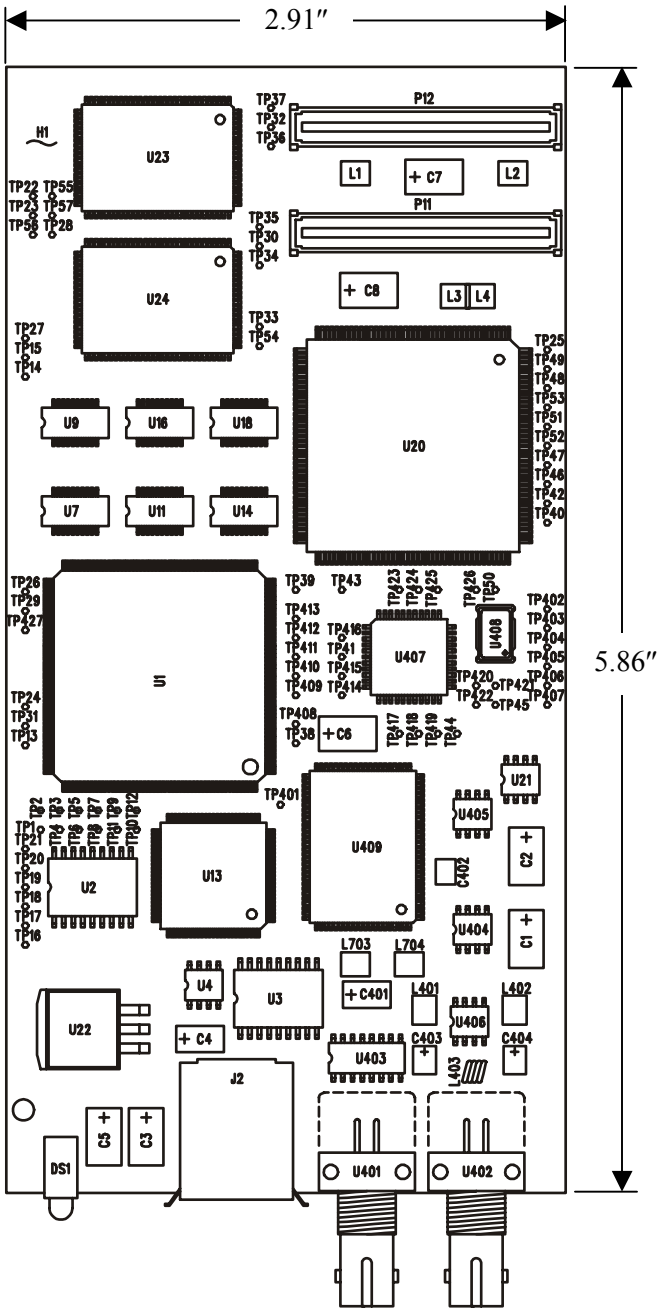


Figure A-2 PMC Dimensions

A.3 RAMplex CPCI

A.3.1 Hardware Specifications

Hardware Compatibility:	PCI local bus specification, rev. 2.1 CompactPCI specification PICMG 2.0 R3.0
Physical Dimensions:	
CPCI Card	3.937" x 6.369"
Weight:	
CPCI Card	0.32 lb w/3U faceplate 0.40 lb w/6U faceplate
PCI Bus Speed	0-33 MHz
PCI Bus Width	32 Bits
PCI Signaling Levels	Universal (+5 V and +3.3 V support)
PCI Interrupt Line	INTA
PCI Vendor ID:	0x11B0
PCI Device ID:	0x4750
PCI Subsystem Vendor:	0x1387
PCI Subsystem ID:	0x5302
Electrical Requirements:	+4.75 to +5.25 VDC, 1.5 Amps max.
Temperature Range	
Storage:	-40° to +70°C
Operation:	0° to +60°C
Humidity Range:	
Storage	0% to 95% (noncondensing)
Operating	10% to 90% (noncondensing)
Network Line Transmission Rate:	77.76 million bits/second
Maximum Nodes on Network Ring:	256
Error Correction:	Available in PLATINUM mode only
Maximum Node Separation:	
Standard Fiber:	300 meters
Factory installed memory:	2 MB
RX78 Effective Network Bandwidth:	3.4 MB/s
RX78e Effective Network Bandwidth:	7.8 MB/s
Latency:	
Pass-through latency:	625 ns
Transmit latency:	995 ns (idle network)
Receive latency:	995 ns
Transmission media delay (fiber-optic):	5 ns/m
Mean Time Between Failures (MTBF):	235,364 hours

A.3.2 Card Dimensions

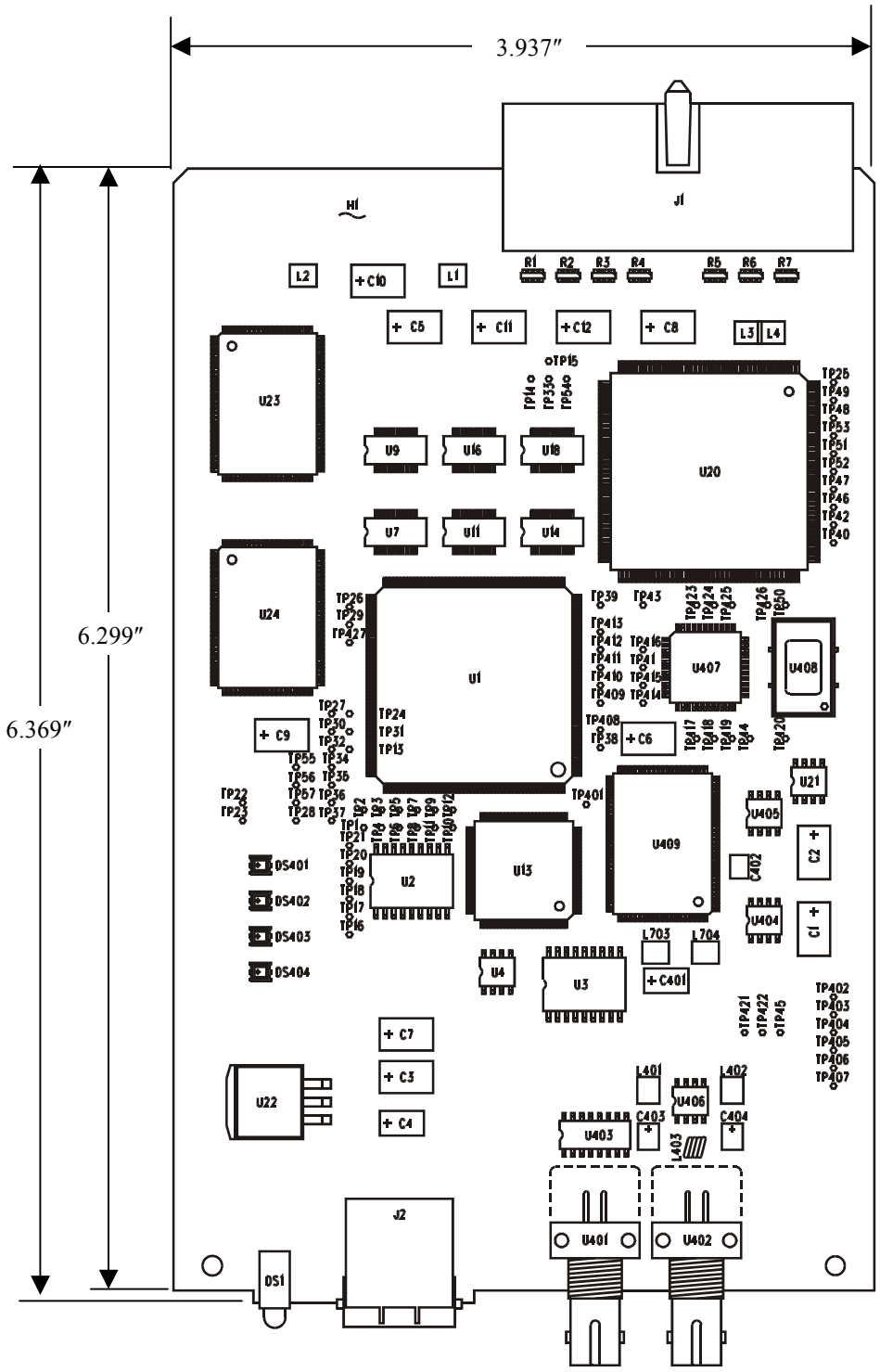


Figure A-3 CPCI Dimensions

A.4 RAMplex VME

A.4.1 Hardware Specifications

Refer to VMETRO *MIDAS-20 User's Guide* for specification information.

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APPENDIX B

CONFIGURATION AIDS

NETWORK CONFIGURATION DATA SHEET

NODE ID	HOST MACHINE	BUS	MEMORY SIZE	Card SERIAL #

APPENDIX C

RAMplex VME USING RAMplex PMC AND VMETRO MIDAS-20 VME CARRIER

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FIGURES

Figure C-1 MIDAS-20 Card with RAMplex PMC Cards C-1

C.1 Overview

This appendix describes the use and setup for the RAMplex VME using the RAMplex PMC card and VMETRO MIDAS-20 carrier board.

C.2 Related Documentation

You should be familiar with the VMETRO *MIDAS-20 User's Guide* in order to use these products. This manual provides a minimal set of information for easier configuration. In addition the *Universe User Manual* from Tundra Semiconductor Corporation gives a detailed description of the Universe Register Set.

C.3 Setup

The MIDAS-20 is a PMC carrier for the VMEbus and contains two PMC card slots with slot 1 as the default card slot for the RAMplex card (see Figure C-1).

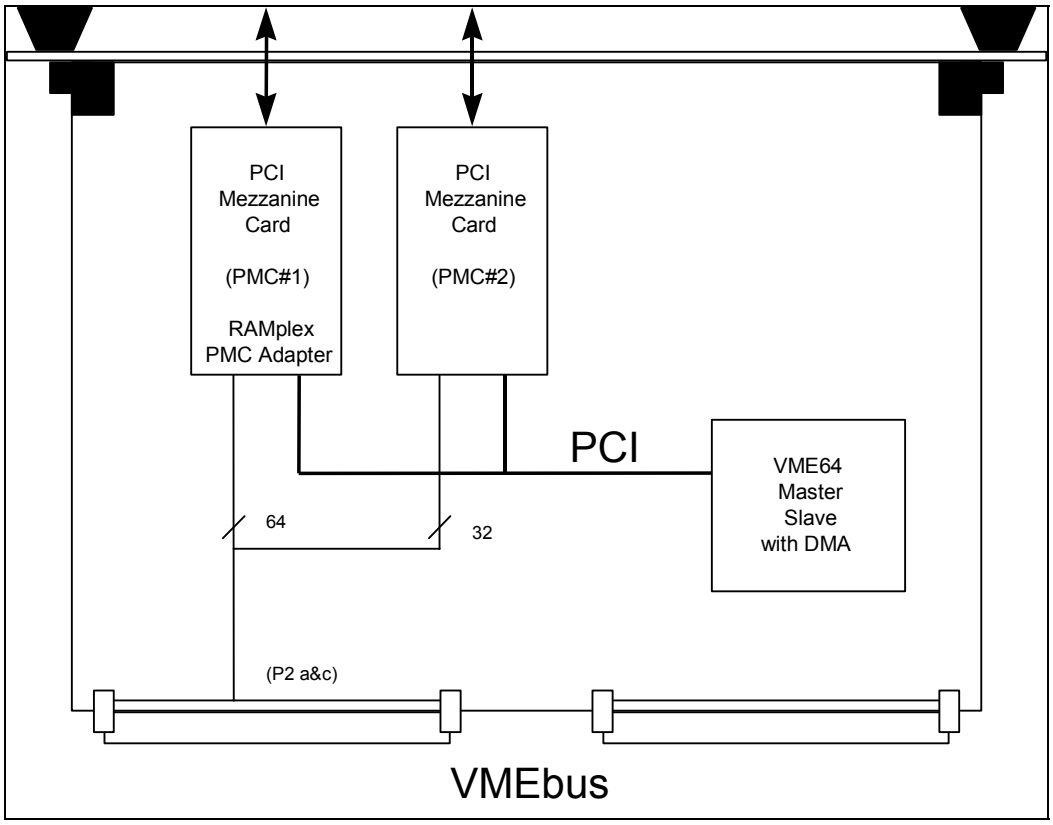


Figure C-1 MIDAS-20 Card with RAMplex PMC Cards

C.4 MIDAS-20 Card Settings

The Universe chip has a number of configuration registers to be initialized by the host processor. Prior to the host initialization, the switch jumpers on the MIDAS-20 card must be configured to define the operation of the card.

The switch and jumpers on the MIDAS-20 card determine the card options and the memory addresses in the VME space. These settings must be configured correctly so there is no overlap of address space for any other cards on the VMEbus. The VME Register Access Image (VRAI) determines the address of the Universe registers. The Universe registers can then be programmed to provide access to RAMplex PCI configuration registers. Table C-1 shows the important VME addresses after the Universe and V3 register sets have been set up.

Table C-1 VME Starting Addresses

Device Accessed	VME Starting Address
Universe register set	MIDAS-20 VRAI
V3 register set (PMC slot #1)	MIDAS-20 VRAI + 0x8000 + 0x2800
RAMplex CSRs	MIDAS-20 VRAI + 0x810000
RAMplex Memory	MIDAS-20 VRAI + 0x10000

Table C-2 contains the recommended switch and jumper settings on the MIDAS-20 using VME register access image address size A32.

Table C-2 MIDAS-20 Card Settings

Jumper or DIP Switch	Position
VME Register Access Image (VRAI)	Enabled
VME Register Access Image Address Size	A32
VME64 Auto-Slot ID (AUTO ID)	Disabled
SYSFAIL* Assertion (S FAIL)	Disabled
VME Register Access Base Address (BASE ADDR)	Base address of any free 9 MB block of VME A32 addresses

C.5 Register Configuration

For any transfers to the RAMplex PMC adapter, the Universe VME interface acts as a VMEbus Slave and the PCI interface acts as a PCI Master. In this example, the Universe register set is mapped to A32 at 0x10000000 (0x10 is set on the VRAI Base Address DIP switch). The VME Slave Images in the Universe register set are configured to provide access to RAMplex PCI configuration space (V3 registers). Next, the V3 register set is accessed and configured (VME address 0x1000a800 for PMC Slot #1 in this example) to allow access to RAMplex memory and CSRs.

C.6 RAMplex Card Settings

All examples assume that the RAMplex card's memory is accessed at VME address 0x104010000. The RAMplex CSR VME address is at 0x10810000. The RAMplex PMC card's CSRs are always at a 0x800000 (8 MB) offset from the RAMplex memory base address. Both RAMplex memory and RAMplex CSRs generally reside in the same VME address space.

The VME A32 space is used in these examples for both RAMplex memory and CSRs.

C.7 Unique Node ID

Most applications require each RAMplex Node in a ring to have a unique node ID. The RAMplex EEPROM can be programmed (CSR3 and CSR4) to ensure that each node will have a unique node ID upon power-up. The RAMplex sample applications allow the node ID to be set in the **scrcfg.dat** file or in **scrhwd.h** if the NO_CONFIG option is used. See Chapter 8 of the Systran *EZ SCRAMWare Programmer Reference Guide* for details.

C.8 Universe VME-PCI Bridge Configuration

The first step in obtaining access to the RAMplex PMC card is to configure the Universe registers. This section will describe the necessary steps for configuration of the Universe registers using the 'C' language. The byte order of the host must be taken into account and the data written to the Universe registers may have to be byte-swapped.

1. Obtain a pointer variable to the Universe register set. The way in which this is accomplished will be specific to the host system. For example, on most UNIX systems a device driver may have to be written to obtain this access or the *mmap()* call may be used to get user access to the VMEbus. For this example assume that **ucsr** points to the Universe register set. The following definitions are also assumed:

```
#define    VRAI_BASE_ADDRESS       0x10000000
#define    SCR_PCI_BASE_ADDRESS    0x20000000

unsigned long volatile* ucsr;
```

2. Enable Universe Bus Master, Memory and IO access:

```
ucsr[0x1] = 0x7;
```

3. Set Maximum Retries to infinity and VMEbus Request Level 2:

```
ucsr[0x100] = 0x00800000;
```

4. Set VME slave image 0 to map to RAMplex PCI configuration space (V3 registers) where 0x14000000 is the VRAI Base Address:

```
ucsr[0x3C1] = VRAI_BASE_ADDRESS - 0x08000000 + 0x8000;
ucsr[0x3C2] = VRAI_BASE_ADDRESS - 0x08000000 + 0xD000;
```

5. Set VME slave image 0 to address 0 on the PCI bus. The translation offset register is added to asserted VME addresses when the slave image is accessed.

Any PCI addresses resulting from this translation that are greater than 0xFFFFFFFF roll over to PCI address 0:

```
ucsr[0x3C3] = 0xFFFFFFFF - (VRAI_BASE_ADDRESS - 0x08000000
              + 0x8000) + 1;
ucsr[0x3C0] = 0x80F20002;
```

6. Set VME slave image 1 to map to RAMplex memory and CSRs

```
ucsr[0x3C6] = VRAI_BASE_ADDRESS - 0x08000000 + 0x10000;
ucsr[0x3C7] = VRAI_BASE_ADDRESS - 0x08000000 + 0x900000;
```

7. Set VME slave image 1 to issue correct addresses of RAMplex on PCI bus:

```
ucsr[0x3C8] = 0xFFFFFFFF - ((VRAI_BASE_ADDRESS- 0x08000000
+
              0x10000) - SCR_PCI_BASE_ADDRESS) + 1;
ucsr[0x3C5] = 0xE0F20000;
```

8. Set address of Universe registers on PCI bus:

```
ucsr[0x4] = 0x08000000;
```

C.9 V3 Register Configuration

The RAMplex PCI registers can be configured once the Universe registers are correctly set up. This section contains steps to set up the RAMplex PCI registers (V3) assuming the following definitions:

```
#define    SCR_PCI_BASE_ADDRESS    0x20000000

unsigned long volatile* v3_ptr;
unsigned short volatile* v3_short_ptr;
```

where **v3_ptr** and **v3_short_ptr** both point to the RAMplex PCI Configuration register set. These pointers can generally be set as an offset to the **ucsr** pointer above as follows:

```
v3_ptr = (unsigned long volatile*)((unsigned long)ucsr +
0x8000 +
          0x2800);
v3_short_ptr = (unsigned short volatile*)v3_ptr;
```

1. Enable RAMplex Bus Master, Memory and IO access:

```
v3_ptr[0x1] = 0x7;
```

2. Clear the lock on the SYSTEM register to change aperture 0

```
v3_short_pci[0x3C] = 0xA05F;
```

3. Set aperture 0 to same PCI address that we set in Universe VME slave image 1 above and set prefetch enable:

```
v3_ptr[0x5] = SCR_PCI_BASE_ADDRESS | 0x8;
```

4. Enable the lock on the SYSTEM register:

```
v3_short_ptr[0x3C] = 0xC400;
```

5. Set MAP register for Aperture 0. Eight-bit byte swapping is turned on here for a big-endian host. If the host is little-endian, write 0x00008043:

```
v3_ptr[0x10] = 0x00008243;
```

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GLOSSARY

card ..... A printed circuit card (PCB). It is a collection of electronic components.

data filter ..... To reduce network traffic, RAMplex compares a new data value written to RAMplex memory with the old value to avoid sending unchanged data values out on the network.

deterministic ..... Completely predictable packet transit time from application to application.

direct memory access ..... (DMA) transfer. An I/O transfer conducted by a device controller which accesses memory directly and, as a result, can transfer a large volume of data without requiring processor intervention for each unit amount. Contrast with programmed I/O (PIO) transfer.

cache ..... To improve the speed of access to data by moving it one stage nearer the CPU. This is very temporary storage as the data may stay in the cache for a few milliseconds or less.

FIFO ..... A data storage method; First In First Out. Also refers to the specific storage area; Transmit FIFO, Interrupt FIFO, etc.

upstream packet ..... A packet that is in (passing through) a node other than the one of origin.

interrupt ..... Asynchronous notification of an event.

ISR ..... Interrupt service routine. A routine executed when a device interrupt occurs.

longword ..... Four bytes (32 bits) of data.

loopback ..... A test that loops the outgoing signal back to its source.

NIC ..... Network Interface Card

latency, pass-through ..... The time required to retransmit an upstream node's packet.

latency, receive ..... The measure of time necessary to update shared memory when an incoming packet arrives.

latency, transmit ..... The time required to send a packet onto the network after a shared memory write access is performed.

packet ..... A message that travels on the network..

PIO ..... Programmed I/O transfer. An I/O transfer, primarily conducted by a driver program, that requires processor intervention after each byte or word is transferred. Contrast with Direct Memory Access (DMA) transfer.

prefetch ..... To bring data into a higher-speed storage or memory before it is actually processed. See **cache**.

protocol violation ..... A signal error at the physical layer (fiber) resulting from noise on the transmission lines or a result of hardware failure. This violation can be any one of the following:

- Missing transition for two clock periods on either line
- Parity error
- Framing error

retry ..... A hardware failure condition reported when the first attempt to send a packet around the network has resulted in some type of bit error. The packet is retransmitted indefinitely by the originating node until

it is received correctly by the originating node. Valid only in error correction mode.

retry time-out ..... A hardware failure condition reported when the first attempt to send a packet around the network is not received by the originating node within the time out period. The packet is retransmitted indefinitely by the originating node until it is received correctly by the originating node. Valid only in error-correction mode.

Rx..... Abbreviation for receive or receiver.

shared memory ..... Memory physically located on the network card. This dual-ported memory is accessible by the host and the network. A host write to shared memory results in a transmitted write to all network nodes at the same relative location.

shortword..... 16 bits. Also referred to as halfword.

time-out..... Also network time-out. The elapsed time before a native packet will be retransmitted. The time-out must be a non-zero value.

Tx..... Abbreviation for transmit or transmitter.

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