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RELAY16

16-Channel Electromechanical
Form-C Relay Board
Hardware Reference

Document No. B-T-MR-RELAY16#-A-0-A2

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Revised: July 16, 2001

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CE

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TABLE OF CONTENTS

1. INTRODUCTION 1-1
- 1.1 How to Use This Manual 1-1
  - 1.1.1 Purpose 1-1
  - 1.1.2 Scope 1-1
  - 1.1.3 Conventions 1-1
- 1.2 Related Information 1-1
- 1.3 Quality Assurance 1-2
- 1.4 Technical Support 1-2
- 1.5 Ordering Process 1-3

2. PRODUCT OVERVIEW 2-1
- 2.1 Overview 2-1
- 2.2 Features 2-1
- 2.3 Related Products 2-1
- 2.4 Block Diagram Description 2-2
- 2.5 Detailed Description 2-2
  - 2.5.1 RELAY16 Components 2-2
  - 2.5.2 Relay Details 2-4
  - 2.5.3 Contacts 2-4
  - 2.5.4 High Frequency 2-5
  - 2.5.5 Relay Construction 2-5
  - 2.5.6 Relay Contact Protection 2-6
- 2.6 RELAY16 Cleaning 2-7

3. INSTALLATION 3-1
- 3.1 Unpack the RELAY16 3-1
- 3.2 Inspect the RELAY16 3-1
- 3.3 Install the RELAY16 3-1

4. PERFORMANCE 4-1
- 4.1 Overview 4-1
- 4.2 Performance Measurements 4-2
- 4.3 IP Module Access Times 4-2
- 4.4 Relay Attack and Release Times 4-4
- 4.5 Contact Bounce Times 4-5

APPENDICES

APPENDIX A – SPECIFICATIONS A-1
APPENDIX B – TYPICAL APPLICATIONS B-1
APPENDIX B – PROGRAMMING GUIDE C-1
GLOSSARY GLOSSARY-1
INDEX INDEX-1

FIGURES

Figure 2-1 Relay16 Board 2-1
Figure 2-2 RELAY16 Simplified Block Diagram 2-2
Figure 2-3 RELAY16 Layout 2-3
Figure 3-1 Installation of the RELAY16 on a VME IP Module Carrier Board 3-2
Figure 3-2 Installation of the RELAY16 on a ISA IP Module Carrier Board 3-2
Figure 4-1 IP Module Test Configuration for Oscilloscope and State Timing Measurements 4-1
Figure 4-2 Typical Logic State Analyzer Snapshot of an ID Transfer 4-3
Figure 4-3 Typical Relay Attack/Release Times 4-4
Figure 4-4 Typical Contact Bounce Times 4-6

TABLES

Table 3-1 Contents of RELAY16 Shipping Packages 3-1
Table 3-2 RELAY16 Installation Tools 3-2
Table 3-3 IP Module Logic Bus Pin Assignments 3-4
Table 3-4 IP Module I/O Connector Pin Assignments 3-5
Table 4-1 IP Module Access Times 4-3
Table 4-2 Relay Attack/Release Times 4-5
Table 4-3 Contact Bounce Times 4-5

1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's 16-channel electromechanical relay IP Module board, referred to as the RELAY16, which contains 16 independent contact sets (part number BHAS-RELAY16).

1.1.2 Scope

This reference manual covers the physical and operational description of the RELAY16, both from hardware and software perspectives. This manual also contains detailed technical information about the RELAY16's performance characteristics, and some typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2               file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)

- ANSI/VITA 4-1995 published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA. Phone: 480-951-8866, FAX: 480-951-0720, E-mail: info@vita.com, URL: www.vita.com
- Systran Corporation: www.systran.com

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Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

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Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to

offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments (including software), contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: **(937) 252-5601** or **(800) 252-5601**
- E-mail: **support@systran.com**
- Fax: **(937) 252-1349**
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2. PRODUCT OVERVIEW

2.1 Overview

The RELAY16 is a singlewide IP Module board, conforming both mechanically and electrically to the *ANSI/VITA 4-1995 American National Standard for IP Modules.* For a typical quad-IP Module carrier, it can provide up to 64 independent sets of form-C relay contacts for a single slot on a computer bus backplane, or be mixed with other IP Modules for a more customized, modular I/O system solution.

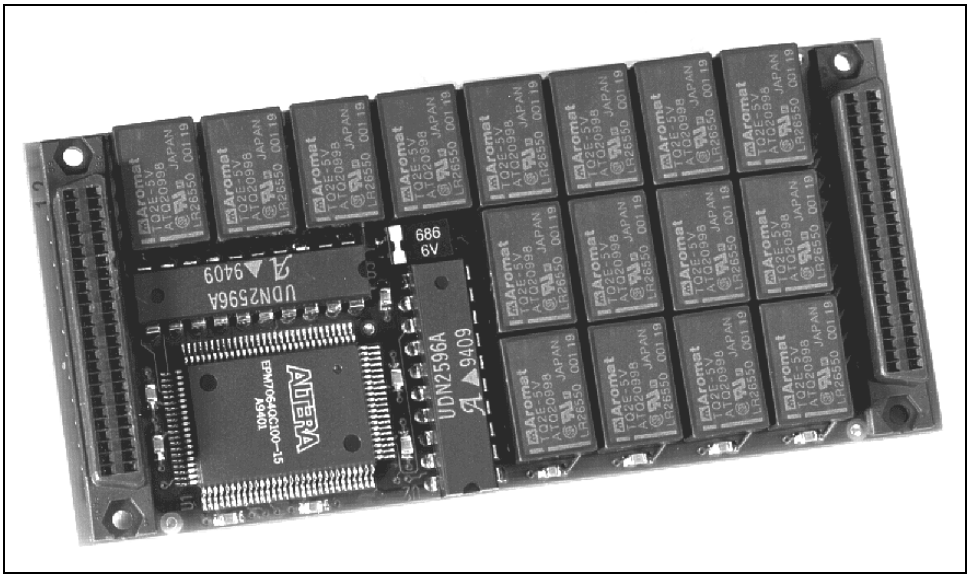


Figure 2-1 Relay16 Board

2.2 Features

- 16 (mechanical) relays, featuring SPDT (form C) contacts.
- Only one, 16-bit, write/read-back register with no wait states.
- Maximum current carrying capacity of 1 Amp per channel (limited by IP Module I/O connector, and not the relays)
- Ultra-small size ⇒ highest possible density
- Pair of form-C contacts in parallel per relay minimizing bounce, sharing current carrying paths, with reduced (apparent) contact resistance
- Integrated transient-suppression diodes for cleaner power
- Relays have UL/CSA rating, and high isolation (FCC) surge voltage rating, and have good shock and vibration resistance specifications.

2.3 Related Products

- Software: 'C' library and OS-9 device driver routines with documentation.

2.4 Block Diagram Description

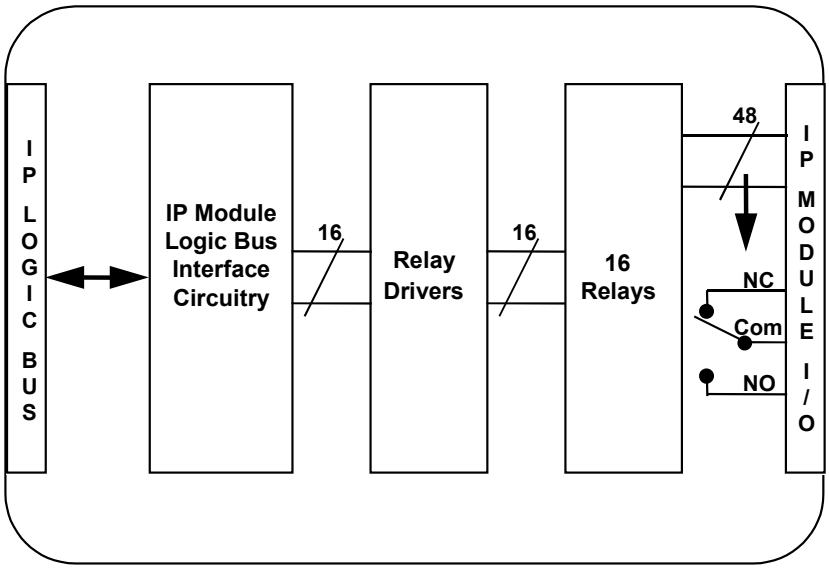


Figure 2-2 RELAY16 Simplified Block Diagram

Due to the simplicity of this product, there is only a simplified block diagram of the RELAY16, as presented in Figure 2-2. On the left side is the IP Module's Logic Bus connector through which all transfers between the IP Module carrier and the RELAY16's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface Circuitry" contains the write/read-back data register, the ID "PROM" data, and IP Module transfer sequence/control and data bus interface logic. This block of circuitry is completely implemented with a single EPLD device.

The (next right) block labeled "Relay Drivers" consists of a pair of octal saturated (non-Darlington) sink drivers with built-in, per collector, transient suppression clamp diodes for limiting the counter-EMF when de-energizing the relays.

The (next right) block labeled "16 Relays" consists of sixteen, polarized, electromechanical relays, each with a pair of form'C' contacts wired in parallel, forming a "common", "normally open", and "normally closed" triad set of contacts each. These 48 relay contacts are directly connected to the far-right block (connector) labeled "IP Module I/O".

2.5 Detailed Description

The RELAY16 was developed using VHDL and Synthesis, targeted to Altera EPLDs, schematic captured and integrated into standard logic devices, connectors and discrete components using Viewdraw by VIEWlogic and associated packages. This top-down design methodology is evident in the product design material presented in this document.

2.5.1 RELAY16 Components

All IP Module Logic Bus transfers take place across J1, the IP Module Logic Connector, located on the left side of the block diagram. Refer to the ANSI/VITA 4-1995 specification for details about the signals on this connector, and their functions. This IP Module does not support DMA or Interrupts, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and writes to the one location I/O map.

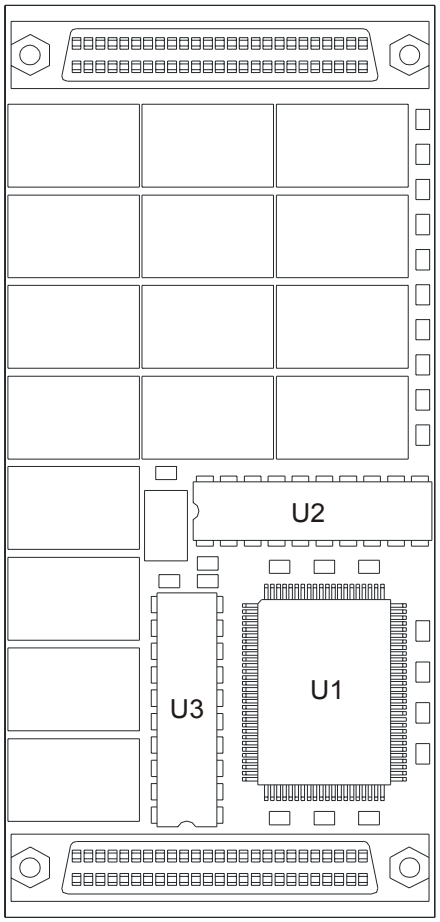


Figure 2-3 RELAY16 Layout

The RELAY16's primary activity controller is housed within the EPM7064QC100 EPLD located at U1 in Figure 2-3. It serves as the IP Module transfer sequence engine, whose responsibilities include: detection of valid I/O and ID transfer operations within their respective, fully decoded address ranges, including the support of HOLD cycles when generated by a carrier; ID PROM emulation data pattern generation for ID read transfers; and the I/O functions of write registration and read gating of the 16-bits of relay state/drive information. Since the relay drivers appear as logical buffers and the relays themselves need a sinking ground path to be enabled, the EPLD performs inversion of the I/O data to turn on the relays. In other words, writing a logic one to a specific I/O bit location provides a ground to its relay to turn it on. At power-up or any other form of "reset" operation, all of the I/O registers are cleared, thereby turning off all relays until specifically manipulated by an I/O write transfer.

The relay drivers, located at U2 and U3 in Figure 2-3, provide 16 channels of saturated (non-Darlington) open collector transistors that provide a ground path for their attached relays. As cited above, they provide a non-inverting buffer function, with per-transistor output transient-suppression diodes, 50 V minimum output breakdown voltage for extra-reliable over-voltage protection, 300 mA sinking current capacities for extra-reliable over-current protection, standard NPN outputs providing very low collector-emitter voltage drops for consistent and reliable relay pull-in performance characteristics over a wide temperature range, with DIP packages containing copper lead-frames for improved thermal characteristics.

The relays themselves have many characteristics, and a complete understanding of what can and cannot be done with them in typical applications is desirable. Many of the interface and drive requirements have been handled in the design of the interface. There are many other elements to cover, most involving the actual contacts and their connections, some involving overall mechanical-related characteristics. Additional hints for usage can be found in Appendix B.

2.5.2 Relay Details

The purpose of this short subsection is to provide some additional background material as it relates to proper usage of this product, and clarification of terminology used in the specifications portion of this document.

Most of the coil-related technical issues have been resolved by design. These include features like: coil resistance, nominal operating current and power, nominal and maximum continuous coil voltage, the release or drop-out voltage, and the pull-in or pick-up voltage. It is this last element, and to a lesser degree the second-to-last element, that was identified in the above text concerning the type of relay drive transistor used, and why it was used.

2.5.3 Contacts

The rated switching power value (30 watts for DC, 62.5 Volt-Amps for AC resistive load) is the product of the switching voltage multiplied by the switching current, and is lower than the maximum voltage and maximum current product which can be handled with steady-state closed contacts. If the maximum DC switching voltage (110 Vdc) appears across the open relay contacts, this means that the maximum current must be less than 272 mA for safe contact closure. If the maximum switching current of one ampere is applied through the contacts, then the maximum DC switching voltage is 30 Vdc. A similar condition exists for the AC switching power specification.

The maximum carrying current for this product happens to be identical to the switching current. Normally, relays can carry more current than they can safely switch. This is true for these relays, as well. However, since the maximum "carrying" current of the I/O connector pins is one ampere, the maximum carrying current for the relays share this limitation. Normally the temperature rise through the contacts and its effect on other sensitive relay components limit the current capacity for all relays.

The minimum switching current and voltage specifications (10 μA, 10 mVdc) are those which can be reliably switched by the gold-clad silver contacts given the contact pressure, wiping action, ambient conditions, and the sealed-body characteristics of the relays used on this product.

The initial, maximum contact resistance specification of 50 mΩ from the relay's specification sheet is a conservative value. From performance qualification curves, the initial contact resistance spanned 29 → 38 mΩ, with the maximum value of 50 mΩ occurring after 150,000 operations running at a 20 cycles/minute rate with a load of 1 ampere at 30 Vdc being switched. For a load of 0.5 ampere at 125 Vac resistive, the contact resistance after 100,000 operations only reached a maximum of 38 mΩ from a starting span of 29 → 32 mΩ.

The silver contact material provides the highest electrical and thermal conductivity of all metals, exhibiting low contact resistance. The gold cladding, with its excellent corrosion resistance, is pressure welded onto the silver contact for uniform thickness and the nonexistence of pinholes.

2.5.4 High Frequency

No technical information is available concerning the capacitance between open contacts, between open contacts and the coil, or between closed contacts and the coil. However, performance curves do present additional information that provide the user with indications as to how well these relays perform in various high frequency applications.

ISOLATION

The first parameter of interest is that of isolation. High frequency signals leak through the stray capacitance across the contacts, even if they are opened. This leakage is called isolation loss, and is expressed in decibels (dB). It is the logarithm of the magnitude ratio of the signal generated by the leak with respect to the input signal, and the larger the number the better the isolation. Performance curves show that 70 dB of isolation is exhibited at 1 MHz, ≈ 50 dB at 25 MHz, ≈ 40 dB at 100 MHz, ≈ 30 dB at 200 MHz, down to ≈ 15 dB at 1 GHz.

INSERTION LOSS

The second high-frequency parameter of interest is insertion loss, a lumped element commonly including resistance, self-induction, dielectric losses, as well as reflections due to mismatches in circuit impedances. This loss is typically expressed in dB, and its pure loss magnitude expression is always best with the smallest value. Performance curves show that high frequency insertion losses range from ≈ 0.05 dB at 10 MHz (and below), ≈ 0.1 dB at 100 MHz, ≈ 0.2 dB at 250 MHz, ≈ 0.4 dB at 700 MHz, to a maximum of ≈ 0.6 dB at 1 GHz.

VOLTAGE STANDING WAVE RATIO (VSWR)

The last high frequency parameter of interest is that of the voltage standing wave ratio (VSWR). High frequency resonance is generated from the interference between the input signal and reflected wave signal, and is the ratio of maximum value to minimum value (a value of 1 ≡ no reflected wave). The performance curves indicate that the VSWR ≈ 1.1 at 300 MHz, ≈ 1.2 at 400 MHz, ≈ 1.3 at 600 MHz, and ≈ 1.45 at 1 GHz.



NOTE: These specifications are for the relay itself, and do not include variations caused by their mounting on its IP Module printed circuit board, I/O connecter, the interconnecting board traces, or the IP Module's carrier and neighborhood boards (if mounted in card slots).

2.5.5 Relay Construction

There are five major components to each relay used on this product. The body block provides the assembly structure with pre-soldered leads and stationary contacts, within which most other components are mounted. The relay coil consists of special, high heat resistant copper wire on a form that surrounds the iron core, which also has a special heat-resistant coating. These relays achieve their super-sensitivity (and polarization) and relatively high switching speeds with the mechanical advantage of an embedded, permanent magnet. The armature block assembly consists of high conductivity and heat-resistant actuator springs with multiple twin crossbar moving contacts of silver alloy with gold cladding. The entire assembly is covered with a high heat resistant top casing of the "sealed" type.

There are several casing types available for relays for protection against dust, flux, contaminating environments, automatic cleaning, etc. One classification includes: dust

cover, flux-resistant, sealed, and metallic hermetic sealed. The sealed type used on this product totally excludes the ingress of contaminants by way of a sealing resin compound applied to the body block/top casing interface that also fills the terminals and base. The constituent components are annealed for physical and chemical stability, which drives off residual volatiles in the plastics, insuring a contaminant free environment inside the sealed relay for a more stable contact resistance over life.



NOTE: There is an exchange of gas molecules through the plastic cover over time that can only be circumvented by using a much more expensive hermetic seal type relay.



CAUTION: These relays are NOT recommended for explosion-proof applications. Use of the hermetic seal type relay is the only solution for such applications.

Due to the permanent magnet polarization architecture used in these relays, care should be exercised in the placement of this board in close proximity to strong, external magnetic fields, such as those found near power transformers, large magnets (some motors, speakers, etc.) since operational characteristics may be affected.

2.5.6 Relay Contact Protection

When the relay contacts of this product are used to switch inductive loads, such as other relay coils, motors, transformer primaries/secondaries, clutches, lamp ballasts, valves, solenoids, etc., it is always important to protect the contacts by absorbing the voltage surges induced when these loads are switched off. This counter EMF is usually in the hundreds, and sometimes thousands of volts range, and is the primary contributor to contact failure via oxidation, or welding in extreme cases. There are many ways of accomplishing this task; some good, some accepted and not very good, and some never-to-be-used techniques.

The use of a capacitor in parallel with the relay contacts in series with an inductive load is effective in arc suppression as the relay contacts open. However, the contacts are susceptible to welding since energy is stored in the capacitor when the contacts open and discharge current flows from the capacitor when the relay contacts are closed. The similar protection technique of placing a capacitor in parallel with the load has similar results. While useful in minimizing arc across the relay contacts as they open, the contacts are susceptible to welding since charging current flows to the capacitor when the relay contacts close.

A safer, acceptable technique involves placing a series resistance in the capacitor leg of the circuits described above. This technique requires a good understanding of the load characteristics, or a lot of test/experimentation. A general guide for resistor and capacitor selections might be to select a resistance such that there is approximately $0.5 \rightarrow 1.0\Omega$ per volt across the open contacts, and about $0.5 \rightarrow 1.0\mu F$ per ampere of current through the closed contacts.



NOTE: If the RC network is across the relay contact (instead of across the load) then care must be taken that the load impedance is significantly smaller than that of the RC network for AC applications. The RC network could lengthen the release time of a relay-type load for applications with the RC network in parallel with the load.

For DC applications (not easy to accomplish for AC circuits) a diode can be placed in parallel with the inductive load to protect the relay contacts against excessive counter EMF conditions and their resultant failure modes. This is accomplished by connecting the diode's cathode to the positive load connection, and the anode to the negative load connection. The diode should have a reverse breakdown voltage rating of at least ten times the circuit voltage with a forward current rating at least as large as the load current. Also, this diode protection scheme lengthens the relay-type release time significantly (typically 5 to 10 times normal).

A simple modification to the last (diode) protection scheme speeds up the release time significantly. By connecting a zener diode between the anode of the "regular" diode and the negative load connection (zener's anode → diode's anode; zener's cathode → load's negative connection) the relay contacts are protected and maintain good response characteristics. The zener diode's "zener voltage" should be about the same as the load's supply voltage. This is a DC application-only protection scheme.

A highly recommended scheme that works well for all DC and AC applications for inductive loads involves the placement of a varistor in parallel with the inductive load. The use of a varistor only slightly increases the release time.

Obviously, not all loads are primarily inductive in nature. Lamps, and capacitive loads present an inverse problem. Relay contacts must supply massive amounts of start-up or in-rush current when turning on these kinds of loads. Large currents flowing through "closing" contacts often result in welded (together) contacts. The most common technique for protecting relay contacts for loads with high in-rush current characteristics is to place inductance (choke, coil) and/or resistance in series with the load to limit the initial turn-on current to a level that the relay contacts can safely handle.

Some typical, very generalized, in-rush current to running current ratios might be:

- Purely resistive load ≈ 1
- Sodium vapor lamp load ≈ 1 → 3
- Mercury vapor lamp load ≈ 3 → 5 (for up to 5 minutes)
- Motor loads ≈ 5 → 10 (for up to 500 ms)
- Transformer loads ≈ 5 → 15
- Incandescent lamp and solenoid loads ≈ 10 → 20 (for up to 300 ms)
- Capacitive loads ≈ 20 → 40 (for up to 33 ms).

It is important to place the protection circuitry as close to the load or the relay contacts as is physically possible to maximize protection. Increased distances will diminish the effectiveness of the protection devices due to increased impedances caused by connection wires. If long wires must be used, it is recommended that series resistance is included to counter the effects of the increased circuit capacitance added by the wiring.

2.6 RELAY16 Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol.



CAUTION: Do NOT use gasoline or thinner type solvents on this product.

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3. INSTALLATION

3.1 Unpack the RELAY16

The contents of the RELAY16 shipping packages are listed in Table 3-1:

Table 3-1 Contents of RELAY16 Shipping Packages

Qty	Description
1	RELAY16 Printed Circuit Assembly
1	RELAY16 Hardware Reference manual *

The printed circuit assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR-RELAY16).

3.2 Inspect the RELAY16

Examine the RELAY16 to determine if any damage occurred during shipping.

3.3 Install the RELAY16



NOTE: The DID48 is an Electrostatic Sensitive Device (ESD). Install the DID48 on an anti-static workbench using good ESD practices to protect the IP Module and its host carrier board.

The RELAY16 installation requires the following tools:

Table 3-2 RELAY16 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

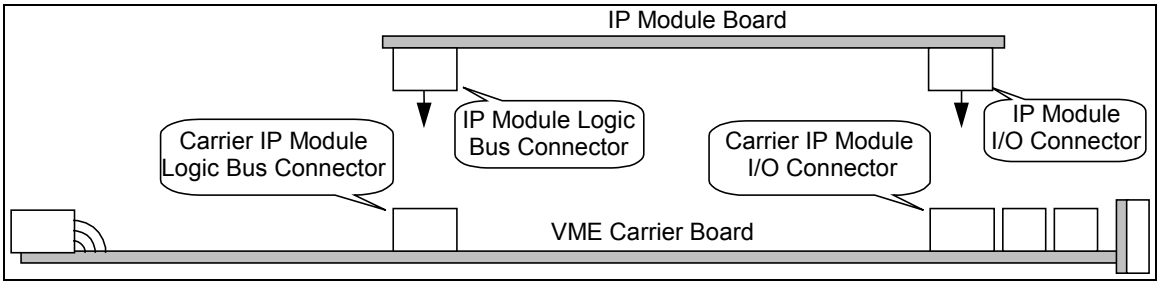


Figure 3-1 Installation of the RELAY16 on a VME IP Module Carrier Board

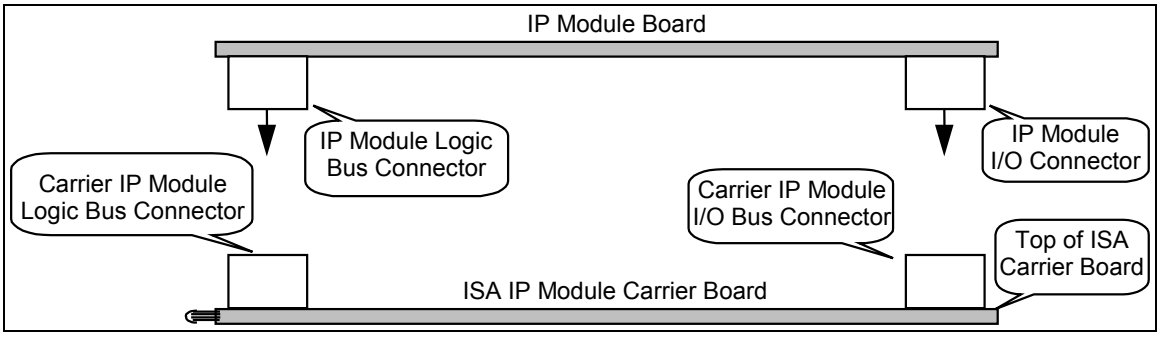


Figure 3-2 Installation of the RELAY16 on a ISA IP Module Carrier Board

Figure 3-1 shows how the RELAY16 is installed on a VME IP Module carrier, and Figure 3-2 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board user's manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (∗) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the installation of the RELAY16 can be made.
3. Remove the RELAY16 from the shipping package and place it on the ESD bench.
4. Install the RELAY16 onto the carrier board by applying adequate and equal pressure to the RELAY16 board at both ends.

∗5. Install four M2x5 mm flat head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the RELAY16 to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Name
50	GND
49	Not Used
48	RNO15
47	RCOM15
46	RNC15
45	RNO14
44	RCOM14
43	RNC14
42	RNO13
41	RCOM13
40	RNC13
39	RNO12
38	RCOM12
37	RNC12
36	RNO11
35	RCOM11
34	RNC11
33	RNO10
32	RCOM10
31	RNC10
30	RNO9
29	RCOM9
28	RNC9
27	RNO8
26	RCOM8
25	RNC8
24	RNO7
23	RCOM7
22	RNC7
21	RNO6
20	RCOM6
19	RNC6
18	RNO5
17	RCOM5
16	RNC5
15	RNO4
14	RCOM4
13	RNC4
12	RNO3
11	RCOM3
10	RNC3
9	RNO2
8	RCOM2
7	RNC2
6	RNO1
5	RCOM1
4	RNC1
3	RNO0
2	RCOM0
1	RNC0

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4. PERFORMANCE

4.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration citied, and do not supplant the maximum and minimum envelopes presented in Appendix A, SPECIFICATIONS.

The figures in this section are a collection of typical rise/fall, and board response times to various system stimuli and IP Module cycles.

4.2 Timing Measurements

Timing measurements were conducted on the RELAY16 using an HP model 16500A Logic Analyzer with a 1 GHz Timing Master Module, model 16515A in slot C. The RELAY16 was installed in the IP Module slot 'A' of a Motorola MVME-162-01 VME processor IP Module carrier board. Figure 4-1 shows the test configuration for the oscilloscope and state timing measurements.

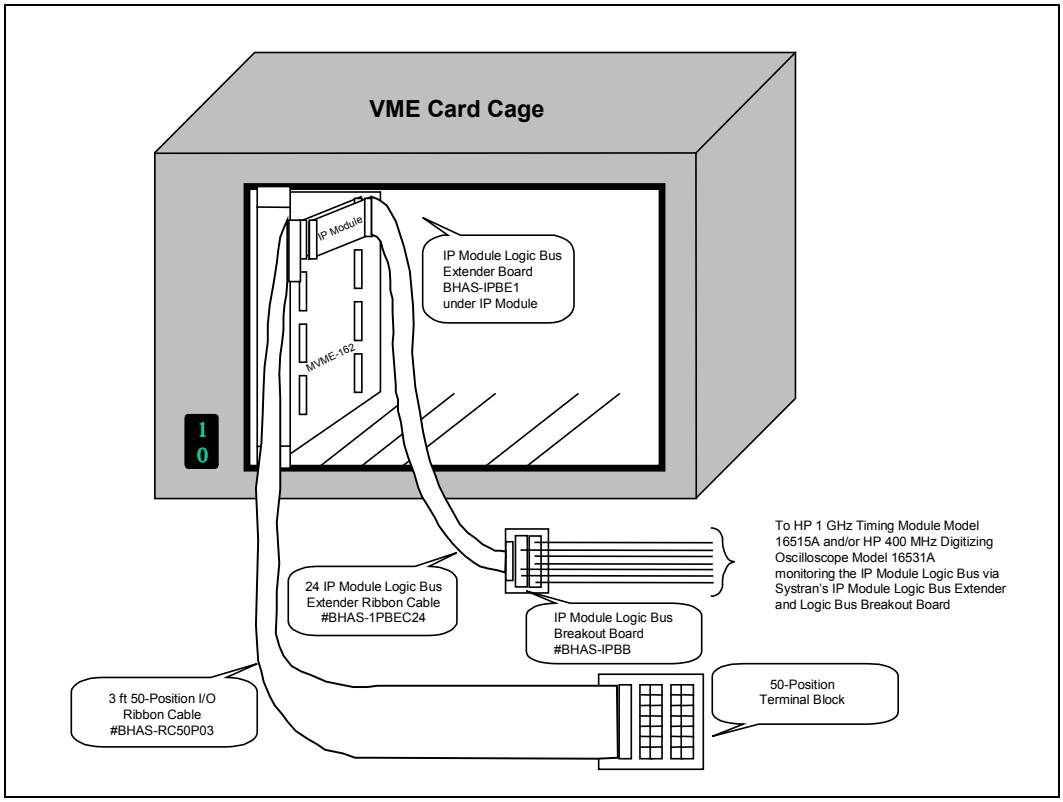


Figure 4-1 IP Module Test Configuration for Oscilloscope and State Timing Measurements

4.3 Performance Measurements

There are three basic sets of performance measurements being presented:

- IP Module access times
- Relay attack and release times
- Contact break-to-make and bounce times

A representative analyzer snapshot is presented for each type of measurement, and all values are tabulated.



NOTE: These measurement are typical results at room temperature for the unit under test, and consequently do not represent "worst case" specification.

All signals, except "RCOM0", were retrieved from the IP Module Logic Bus Breakout Board (BHAS-IPLBB) as shown in Figure 4-1. On the 50-position terminal block at the end of the three-foot I/O cable, pins #1 and #3 were grounded to pin #50, and pin #2 (RCOM0) was pulled high to an external +5 Vdc power source through a 1 KΩ resistor. This permitted the recording of make-to-break times for the Form 'C' tests, Forms 'A' and 'B' contact tests.

The normally closed contact at pin #1 was opened (disconnected from ground at pin #50) for tests in the Form 'A' configuration, and the normally open contact at pin #3 was opened for tests in the Form 'B' configuration.

4.4 IP Module Access Times

Figure 4-2 presents a typical logic state analyzer snapshot of an ID transfer. The first rising edge of ICLK is the beginning of the ID select cycle. The second rising edge of ICLK is the start of the termination cycle when this IP Module drives the IPD bus (only IPD0 is shown), and asserts the N_ACK signal. Table 4-1 shows the IP Module access times.



NOTE: The IPD bus has weak pull-ups on its signal lines that eventually float high a couple of ICLK cycles following the end of the 125 ns termination cycle.

This IP Module tristates its IPD bus drivers at the same time it negates N_ACK.

Table 4-1 IP Module Access Times

Parameter/Event	Typical Time (ns)
↑ ICLK to ⧄ IPD0 High Impedance to Logic Low	15
↑ ICLK to ↓ N_ACK (Assertion)	9
↑ ICLK to ↑ N_ACK (Negation)	9

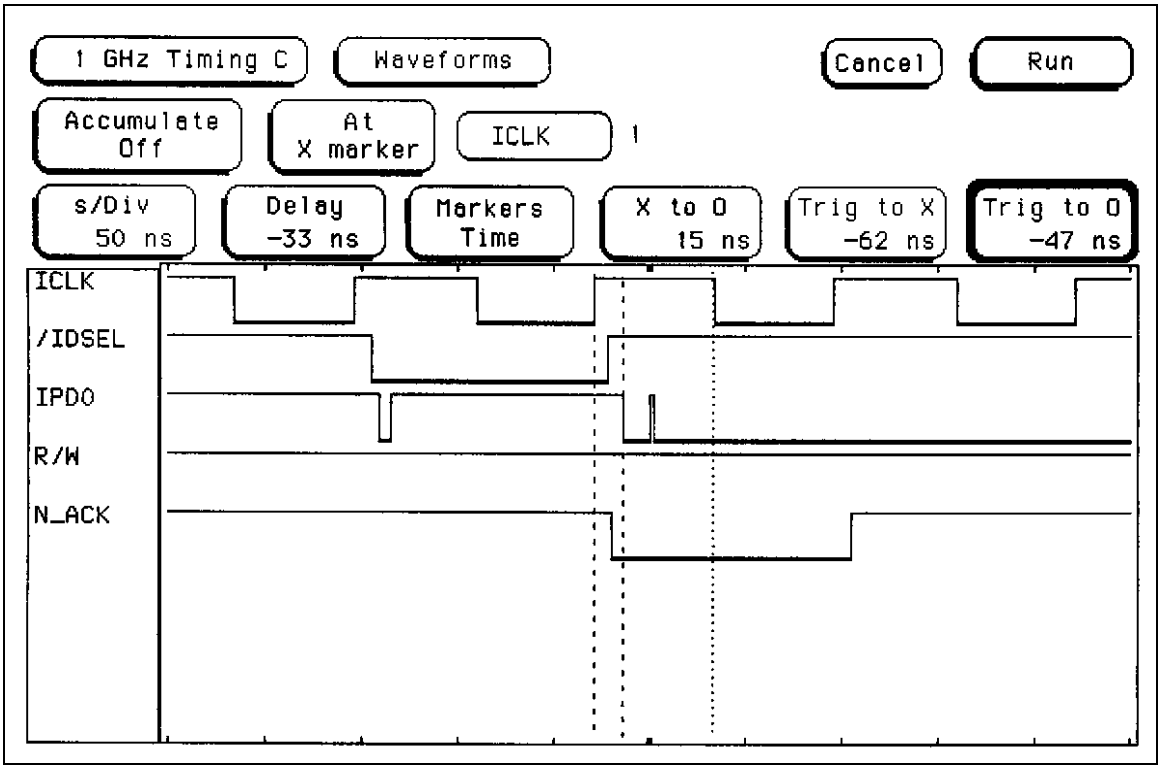


Figure 4-2 Typical Logic State Analyzer Snapshot of an ID Transfer

4.5 Relay Attack and Release Times

Figure 4-3 presents one of six typical logic state analyzer snapshots that capture the relay's attack and release times (see Table 4-2), including relay driver delays (typically 3 µs ON and OFF), excluding contact bounce. Stacked "worst case" delays for the driver/relay pairs from their respective specification sheets yield 3.002 µs maximum for turn-ON and 3.003 µs maximum for turn-OFF times, excluding contact bounce.

The second set of signal assertions (just to the right of the left time marker in Figure 4-3) are those captured during the automatic read/verify operation performed after the write that caused the relay to change states.

The typical times cited in the following table are those from the rising edge of ICLK at the end of the termination cycle (when the I/O register is modified) until the first make-or-break event (depending upon contact configuration), excluding contact bounce.

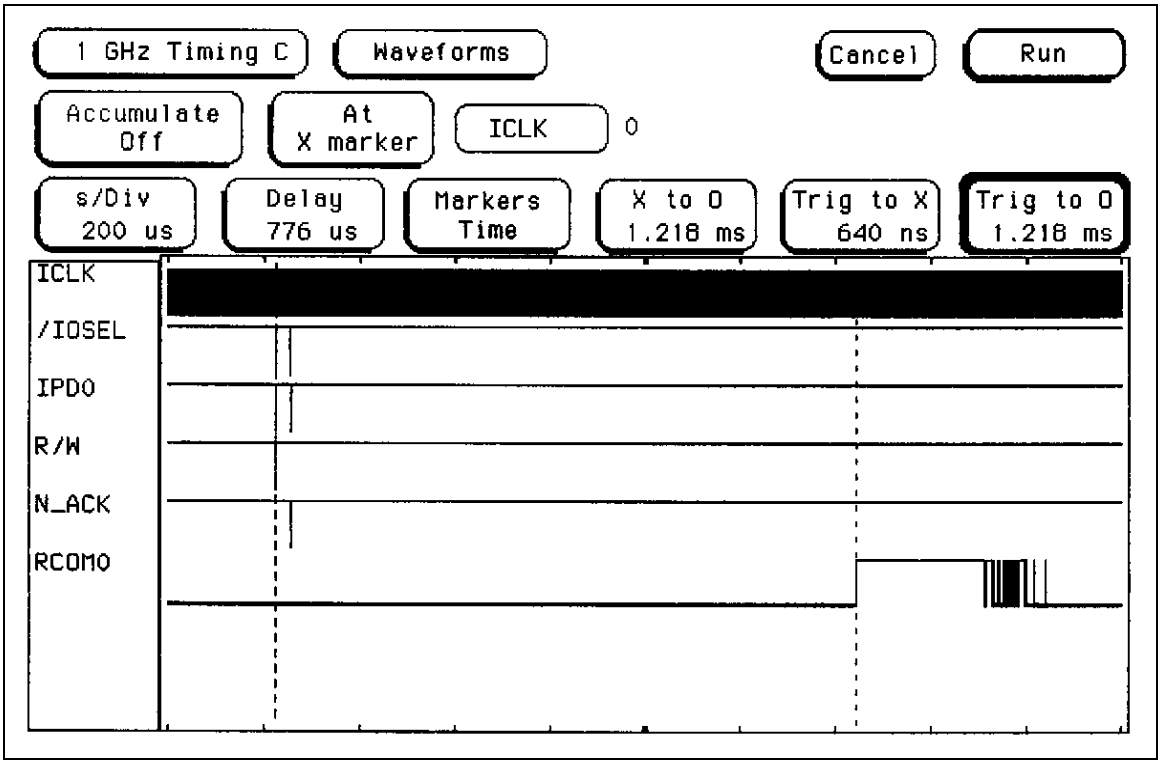


Figure 4-3 Typical Relay Attack/Release Times

Table 4-2 Relay Attack/Release Times

Contact Configuration		Turning Relay	Typical Time To First Make/Break (ms)	
Form 'A'	SPST - NO	ON	(MAKE)	1.746
Form 'A'	SPST - NO	OFF	(BREAK)	1.213
Form 'B'	SPST - NC	ON	(BREAK)	1.533
Form 'B'	SPST - NC	OFF	(MAKE)	1.534
Form 'C'	SPDT - *	ON	(BREAK)	1.494
Form 'C'	SPDT - *	OFF	(BREAK)	1.218

* BREAK-BEFORE-MAKE

4.6 Contact Bounce Times

Figure 4-4 presents one of six typical logic state analyzer snapshots (of just the relay common signal) that capture the contact bounce times (see Table 4-3). The small size, low mass, and polarized characteristics of these relays provide faster attack and release times, and less bounce time than many prior-art relays. Depending on size and mechanical design, contact bounce times approaching 10 ms is not uncommon. The bounce times presented approach those that are typical for dry reed relays, even though the attack and release times are significantly different.



NOTE: There was no measurable "break" bounce time (less than or equal to 1 ns).

Table 4-3 Contact Bounce Times

Contact Configuration	Turning relay	Event timed		Typical time (µs)
Form 'A'	ON	MAKE	First to last closure	137.0
Form 'A'	OFF	BREAK	Break bounce	0.0
Form 'B'	ON	BREAK	Break bounce	0.0
Form 'B'	OFF	MAKE	First to last closure	94.0
Form 'C'	ON	BREAK	To first MAKE	237.2
Form 'C'	ON	MAKE	First to last closure	103.0
Form 'C'	OFF	BREAK	To first MAKE	267.2
Form 'C'	OFF	MAKE	First to last closure	108.0

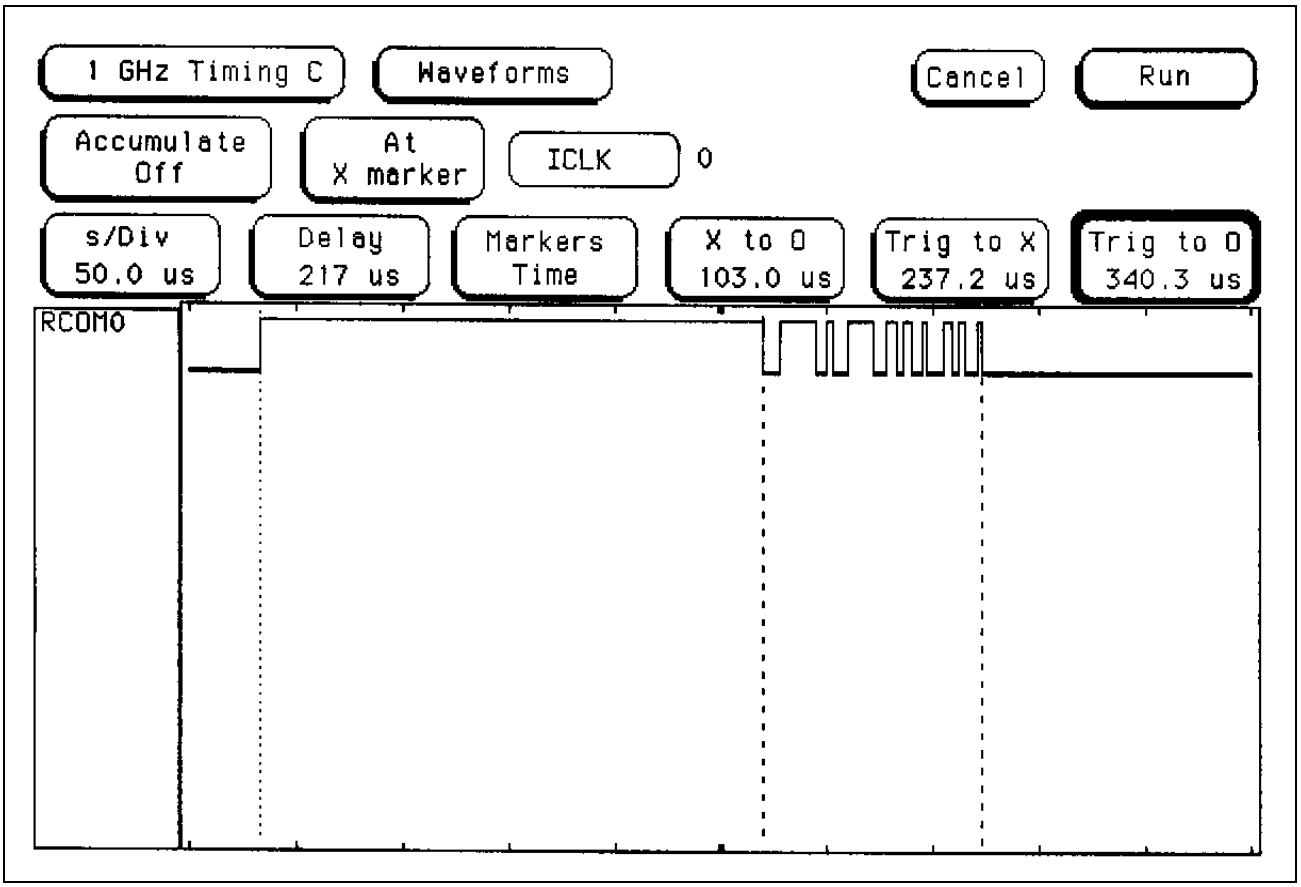


Figure 4-4 Typical Contact Bounce Times

APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements	1.800 inches x 3.900 inches x 0.303 inches (above board), 4.572 cm x 9.906 cm x 0.770 cm
Weight	1.87 oz., 52.36 grams
Board thickness	0.062 inches, 0.157 cm, nominally, (4 layer)

PROTOCOL

Clock rate	8 MHz
Wait cycles	None on any transfer types
Hold cycles	Supported on all valid transfer types
Address decoding	Complete (no partial)
I/O transfers	
Writes	8-bit, 16-bit
Reads	16-bit
I/O locations	One, 16-bit
Maximum read/write rate	4 MTransfers/second, sustained
ID transfers	8-bit read (only) Zero-fill on upper byte 12 bytes, including CRC
Systran's manufacturer's	ID = 0x45, = E ASCII
DAC128V's model number	0x64, = d ASCII
Cyclic Redundancy Check value	0xE2
Maximum read rate	4 MTransfers/second, sustained
Memory transfers	Not supported
Interrupt Vector transfers	Not supported
Interrupt requests	None generated
DMA activity	Not supported
Acknowledgment on unsupported transfer attempts	None generated

Memory read and write
Interrupt read
ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

All relays de-energized (I/O read of '0x0000')
No access permitted or acknowledged during RESET

POWER REQUIREMENTS

Power:	+5 Vdc @ 58 mA (typ., all relays OFF) +5 Vdc @ 476 mA (typ., all relays ON) +12 Vdc @ 0 mA -12 Vdc @ 0 mA

PERFORMANCE CHARACTERISTICS

Electrical Characteristics: Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

Supply voltage with respect to ground:
- Minimum.....-0.5 V
- Maximum.....+7.0 V

I/O connected relay contacts
- Maximum switching power.....30 watts, 62.5 VA (resistive load)
- Maximum switching voltage.....110 Vdc, 125 Vac
- Maximum switching current .....10 μA, 10 mVdc

UL/CSA rating on contacts..... 1 A @ 30 Vdc
0.3 A @ 110 Vdc
0.5 A @ 125 Vac
- UL standard.....E57521
- CSA standard.....LR26550

RECOMMENDED OPERATING CONDITIONS:

Supply voltage .....+4.75 V → +5.25 V
Logic Interface.....ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): .....0°C to +70°C
Temperature (no bias, storage): .....-40°C to +85°C
Humidity (Non-condensing): .....5% to 95%
Vibration (Operating): .....15 G's RMS (10→55 Hz)
Shock (Operating): .....50 G's maximum
Altitude (Operating): .....10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MTBF .....37,480 hours per MIL-HDBK-217F

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

TABLE OF CONTENTS

B.1 Overview B-1
B.2 A Short Glossary Of Contact Applications B-1
B.2.1 Single-Pole-Single-Throw B-2
B.2.2 Single-Pole-Double-Throw B-2
B.2.3 Make-Before-Break Transfer B-3
B.2.4 Two Relays—Break-Make-Break Transfer B-4
B.2.5 Two Relays—Make-Make Transfer B-4
B.2.6 Two Relays—Break-Break Transfer B-4
B.2.7 Two Relays—Break-Break-Make Transfer B-4
B.2.8 Two Relays—Make-Break-Make Transfer B-6
B.2.9 Three Relays—Make-Make-Break Transfer B-6
B.2.10 Two Relay—Center-Off Transfer B-7
B.2.11 Two Relays—Break-Make-Make Transfer B-7
B.2.12 Two Relays—Double Make COA Transfer B-9
B.2.13 Two Relays—Double Break COA Transfer B-9
B.2.14 Two Relays—Double-Break-Double-Make COA Transfer B-9
B.2.15 Two Relays—Double-Make Transfer B-11
B.2.16 Two Relays—Double-Break Transfer B-11
B.2.17 Two Relays—Double-Break-Double-Make Transfer B-11
B.2.18 Electricians Parallel Application B-13

FIGURES

Figure B-1 RELAY16 Form ‘C’ Contacts Block Diagram B-1
Figure B-2 RELAY16 Form ‘A’ and ‘B’ Applications B-2
Figure B-3 RELAY16 Form ‘C’, ‘D’ and ‘E’ Applications B-3
Figure B-4 RELAY16 Form ‘F’, ‘G’ and ‘H’ Applications B-5
Figure B-5 RELAY16 Form ‘I’ and ‘J’ Applications B-6
Figure B-6 RELAY16 Form ‘K’ and ‘L’ Applications B-8
Figure B-7 RELAY16 Form ‘U', ‘V’ and ‘W’ Applications B-10
Figure B-8 RELAY16 Form ‘X’, ‘Y’ and ‘Z’ Applications B-12
Figure B-9 Electricians Parallel Application B-14

B.1 Overview

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the RELAY16 IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 A Short Glossary Of Contact Applications

These typical applications were developed by using one or more contact sets on the RELAY16 IP Module. Most of the common relay configuration operations can be performed (within limits) by proper connections and software manipulations.



NOTE: Unless otherwise noted, initial conditions are for all relays to be in their OFF position (as shown).

The "pause" time referenced in many of the applications is dependent upon the physical constraints imposed by contact transitioning and the associated bounce/settling time, as well as the intended application, sometimes with deliberate delays.

Figure B-1 shows the basic building blocks that are the 'C' form contacts available on the I/O connector of the RELAY16.

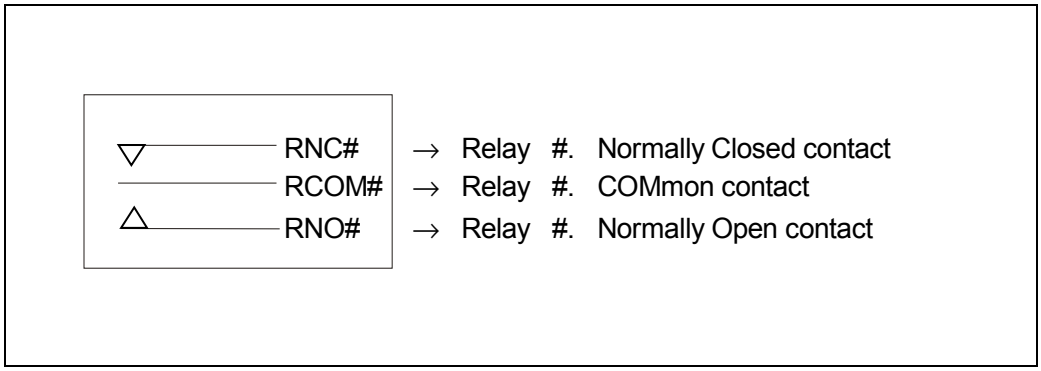


Figure B-1 RELAY16 Form 'C' Contacts Block Diagram

The common and normally closed contacts are connected when the relay is in its de-energized or OFF state (logic '0' in the RELAY16's register). Up to three sets of these contacts are required to emulate some of the more complex contact "forms."

B.2.1 Single-Pole-Single-Throw

Figure B-2 presents Form 'A' and Form 'B' configurations of the RELAY16 contacts. The Form A diagram shows one relay in a single-pole-single-throw (SPST) - normally-open (ON) configuration. The relay is turned ON or energized to "Make" connection between the C (common) and the A (normally-open) contacts. The relay is turned OFF or de-energized to "Break" connection between the C and the A contacts. The Form B diagram shows one relay in a single-pole-single-throw (SPST)—normally closed (NC) configuration. The relay is turned ON or energized to "Break" connection between the C (common) and the A (normally-closed) contacts. The relay is turned OFF or de-energized to "Make" connection between the C and the A contacts.

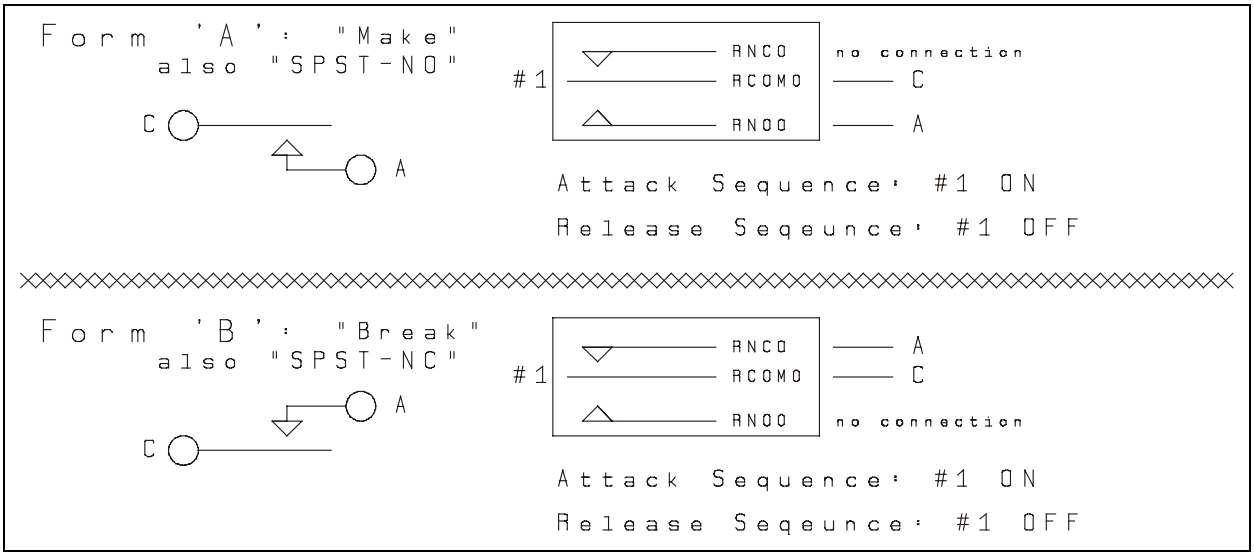


Figure B-2 RELAY16 Form 'A' and 'B' Applications

Figure B-3 presents Forms 'C,' 'D' and 'E' configurations of the RELAY16 contacts.

B.2.2 Single-Pole-Double-Throw

The Form C diagram shows one relay in a single-pole-double-throw (SPDT) break-before-make configuration. The relay is turned ON or energized to "Break" connection between the C (common) and the A (normally-closed) contacts, and then "Make" connection between the C (common) and the B (normally-open) contacts. The relay is turned OFF or de-energized to "Break" connection between the C and the B contacts and then "Make" connection between the C and the A contacts. The "Break" time before "Make" is approximately 1.5 ms for the RELAY16.

B.2.3 Make-Before-Break Transfer

The Form 'D' diagram shows two relays in a make-before-break continuity transfer configuration. The attack sequence is: Relay #2 is turned ON or energized to "Make" connection between the C (common) and the B (normally-open) contacts, and after a pause Relay #1 is turned ON to "Break" connection between the C (common) and the A (normally-closed) contacts. The release sequence is: Relay #1 is turned OFF or

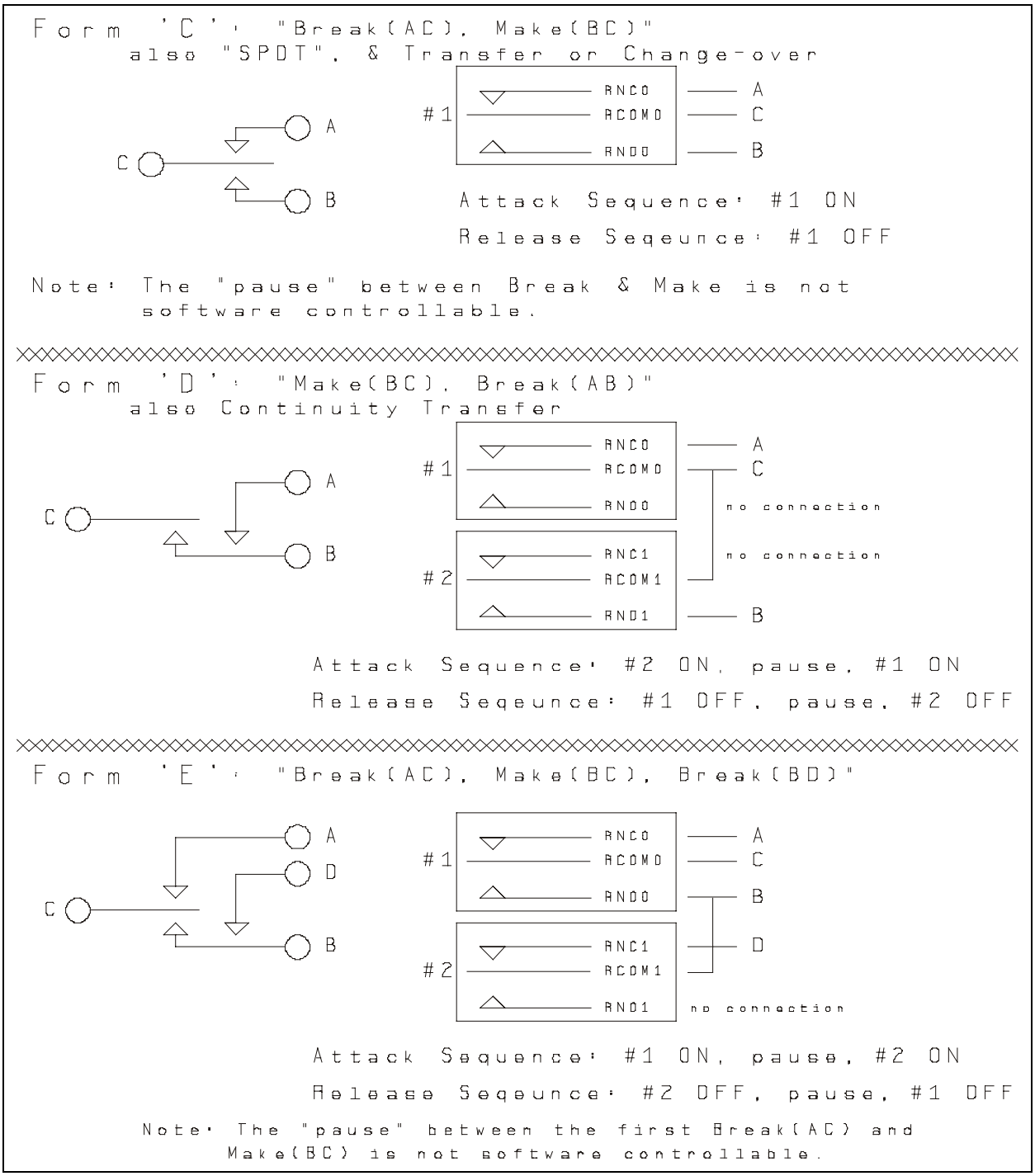


Figure B-3 RELAY16 Form 'C', 'D' and 'E' Applications

de-energized to “Make” connection between the C and the A contacts, and after a pause Relay #2 is turned OFF to “Break” connection between the C and the B contacts.

B.2.4 Two Relays—Break-Make-Break Transfer

The Form ‘E’ diagram uses two relays to perform a break-make-break transfer. The attack sequence is: Relay #1 is turned ON or energized to “Break” connection between the C (common) and the A (normally-closed) contacts and “Make” the C and B (normally-open) connection. Then after a pause Relay #2 is turned ON to “Break” the B and D contact connection.

The release sequence is: Relay #2 is turned OFF or de-energized to “Make” connection between the B and D contacts, and after a pause Relay #1 is turned OFF to first “Break” the B and C connections, and then to “Make” connection between the A and C contacts.

B.2.5 Two Relays—Make-Make Transfer

Figure B-4 presents Forms ‘F’, ‘G’ and ‘H’ configurations of the RELAY16 contacts.

The Form F diagram uses two relays to perform a make-make transfer. The attack sequence is: Relay #1 is turned ON or energized to “Make” the C (common) and A (normally-open) connection, and after a pause Relay #2 is turned ON to “Make” the A and B contact connection. The release sequence is: Relay #2 is turned OFF or de-energized to “Break” connection between the A and B contacts, and after a pause Relay #1 is turned OFF to “Break” connection between the A and C contacts.

B.2.6 Two Relays—Break-Break Transfer

The Form G diagram uses two relays to perform a break-break transfer. The attack sequence is: Relay #1 is turned ON or energized to “Break” the B (common) and A (normally-closed) connection, and after a pause Relay #2 is turned ON to “Break” the B and C contact connection. The release sequence is: Relay #2 is turned OFF or de-energized to “Make” connection between the B and C contacts, and after a pause Relay #1 is turned OFF to “Make” connection between the A and B contacts.

B.2.7 Two Relays—Break-Break-Make Transfer

The Form H diagram uses two relays to perform a break-break-make transfer. The attack sequence is: Relay #1 is turned ON or energized to “Break” the B (common) and A (normally-closed) connection, and after a pause Relay #2 is turned ON to “Break” the B and C contact connection and “Make” the C and D connection. The release sequence is: Relay #2 is turned OFF or de-energized to “Break” connection between the C and D contacts and to “Make” connection between the B and C contacts, and after a pause Relay #1 is turned OFF to “Make” connection between the A and B contacts.

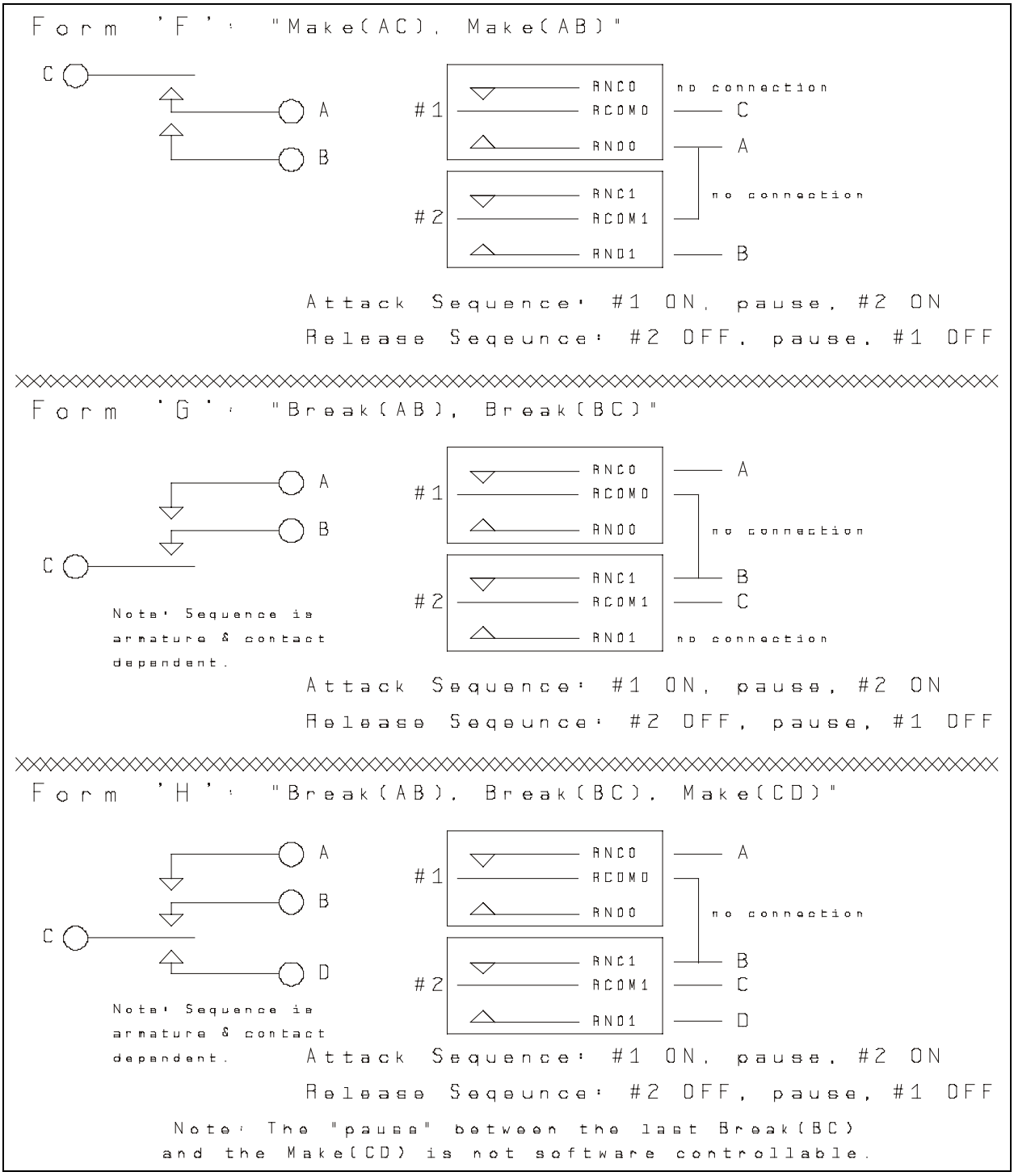


Figure B-4 RELAY16 Form 'F', 'G' and 'H' Applications

B.2.8 Two Relays—Make-Break-Make Transfer

Figure B-5 presents Forms 'I' and 'J' configurations of the RELAY16 contacts.

The Form I diagram uses two relays to perform a make-break-make transfer. The attack sequence is: Relay #1 is turned ON or energized to "Make" the B (common) and C (normally-open) connection, and after a pause Relay #2 is turned ON to "Break" the A and B contact connection and "Make" the B and D connection. The release sequence is: Relay #2 is turned OFF or de-energized to "Break" connection between the B and D contacts and to "Make" the connection between the A and B contacts, and after a pause Relay #1 is turned OFF to "Break" connection between the B and C contacts.

B.2.9 Three Relays—Make-Make-Break Transfer

The Form J diagram uses three relays to perform a make-make-break transfer. The attack sequence is: Relay #1 is turned ON or energized to "Make" the A (common) and C

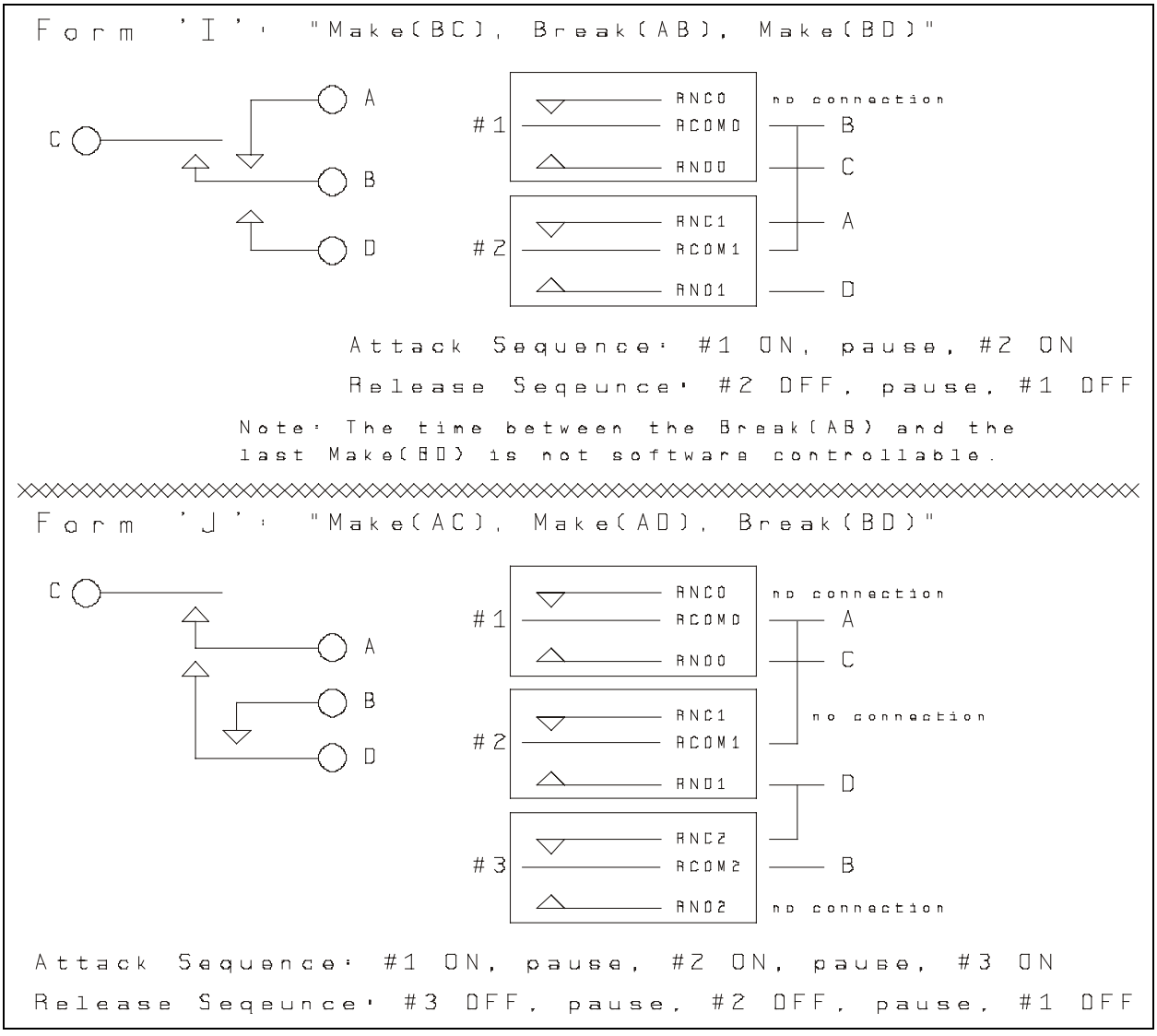


Figure B-5 RELAY16 Form 'I' and 'J' Applications

(normally-open) connection, and after a pause Relay #2 is turned ON to "Make" the A (common) and D (normally-open) connection, and after another pause Relay #3 is turned ON to "Break" the B (common) and D (normally-closed) connection. The release sequence is: Relay #3 is turned OFF or de-energized to "Make" connection between the B and D contacts, and after a pause Relay #2 is turned OFF to "Break" connection between the A and D contacts and after another pause Relay #1 is turned OFF to "Break" connection between the A and C contacts.

B.2.10 Two Relay—Center-Off Transfer

Figure B-6 presents Forms 'K' and 'L' configurations of the RELAY16 contacts.

The Form K diagram uses a two-relay configuration for a "Center Off SPST" transfer. The sequencing for this Form K configuration is order dependent. To achieve an "OFF" state, both relays must be turned OFF or de-energized. To connect contacts C and A, turn 'ON' or energize Relay #1 only. If a connection between contacts C and B is desired, Relay #1 must be turned OFF or de-energized before Relay #2 is turned ON to "Make" the B and C contact connection. If a connection between contacts B and C exists (Relay #2 is ON), and it is desired instead to have contacts A and C connected, then Relay #2 must be turned OFF before Relay #1 is turned ON to "Make" the A and C contact connections.



NOTE: Before any connection is made, always turn both relays OFF first. Also, for a Form K configuration, the user's software should ensure against the possibility of both relays #1 and #2 being turned ON simultaneously unless the A and B circuits can tolerate being shorted together.

B.2.11 Two Relays—Break-Make-Make Transfer

The Form L diagram uses two relays to perform a break-make-make transfer. The attack sequence is: Relay #1 is turned ON or energized to "Break" the A (normally-closed) and C (common), and "Make" the C and B (normally-open) connection. After a pause, Relay #2 is turned ON or energized to "Make" connection between the B and D contacts. The release sequence is: Relay #2 is turned OFF or de-energized to "Break" connection between the B and D contacts, and after a pause, Relay #1 is turned OFF to "Break" connection between the B and C contacts, and "Make" the connection between the A and C contacts.

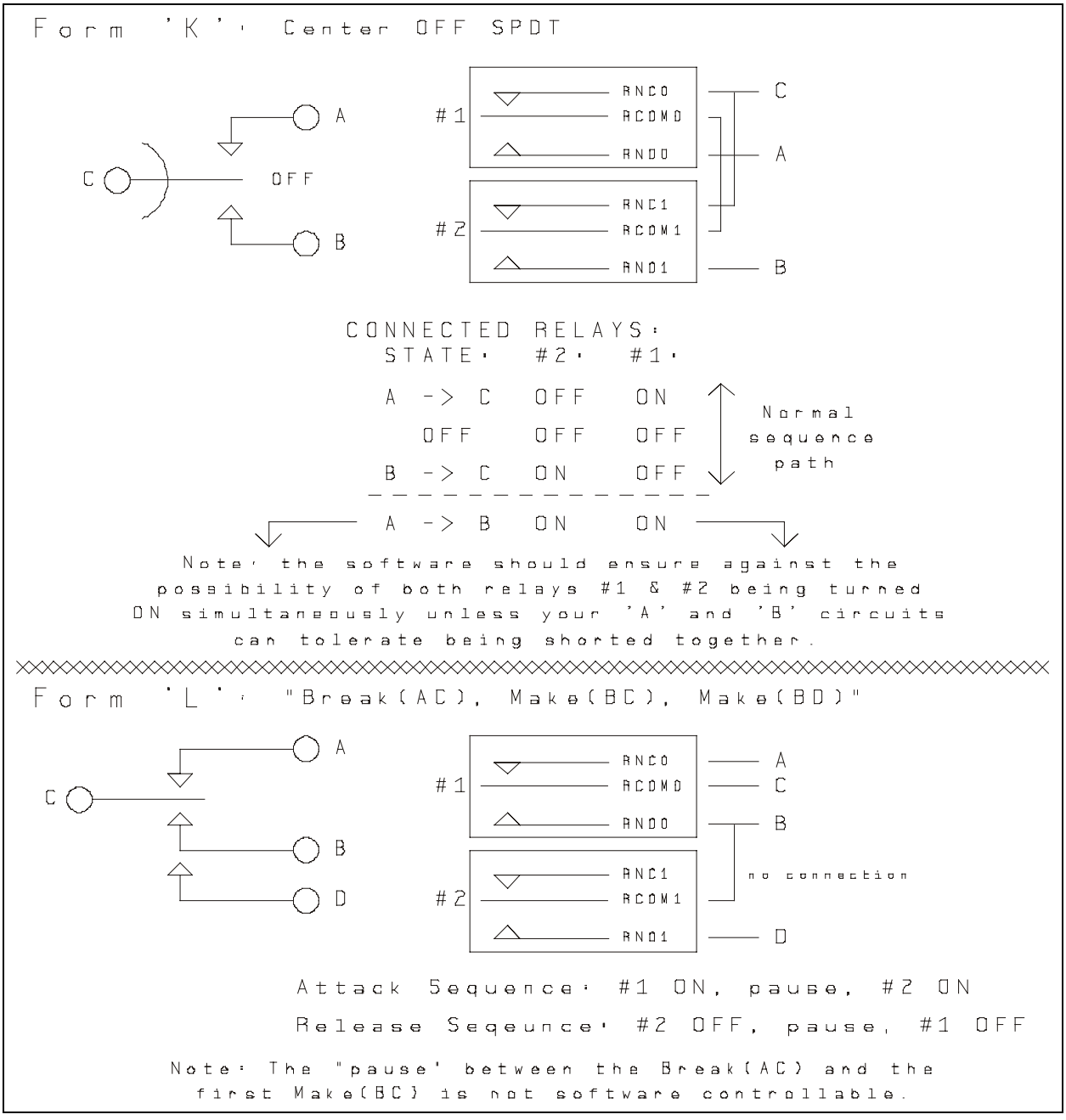


Figure B-6 RELAY16 Form 'K' and 'L' Applications

B.2.12 Two Relays—Double Make COA Transfer

Figure B-7 presents Forms ‘U’, ‘V’ and ‘W’ configurations of the RELAY16 contacts. The Form U diagram uses a two-relay configuration for a double-make (contact on arm) transfer. Simultaneously turning both relays ON or energizing them results in connection of circuits A and B via the C (common) contacts. Simultaneously turning both relays OFF or de-energizing both relays disconnects all three circuits A, B, and C.

B.2.13 Two Relays—Double Break COA Transfer

The Form V diagram uses a two-relay configuration for a double-break (contact on arm) transfer. Simultaneously turning both relays ON or energizing them results in disconnection of circuits A and B and the C (common) contacts. Simultaneously turning both relays OFF or de-energizing both relays connects all three circuits A, B, and C.

B.2.14 Two Relays—Double-Break-Double-Make COA Transfer

The Form W diagram uses a two-relay configuration for a double-break-double-make (contact on arm) transfer. Simultaneously turning both relays ON or energizing them results in connection of circuits D and E via the C (common) contact, and disconnects circuits A and B via the C (common) contact. Simultaneously turning both relays OFF or de-energizing both relays disconnects all three circuits C, D, and E, and then connects contacts A, B, and C (about 1.5 ms later).

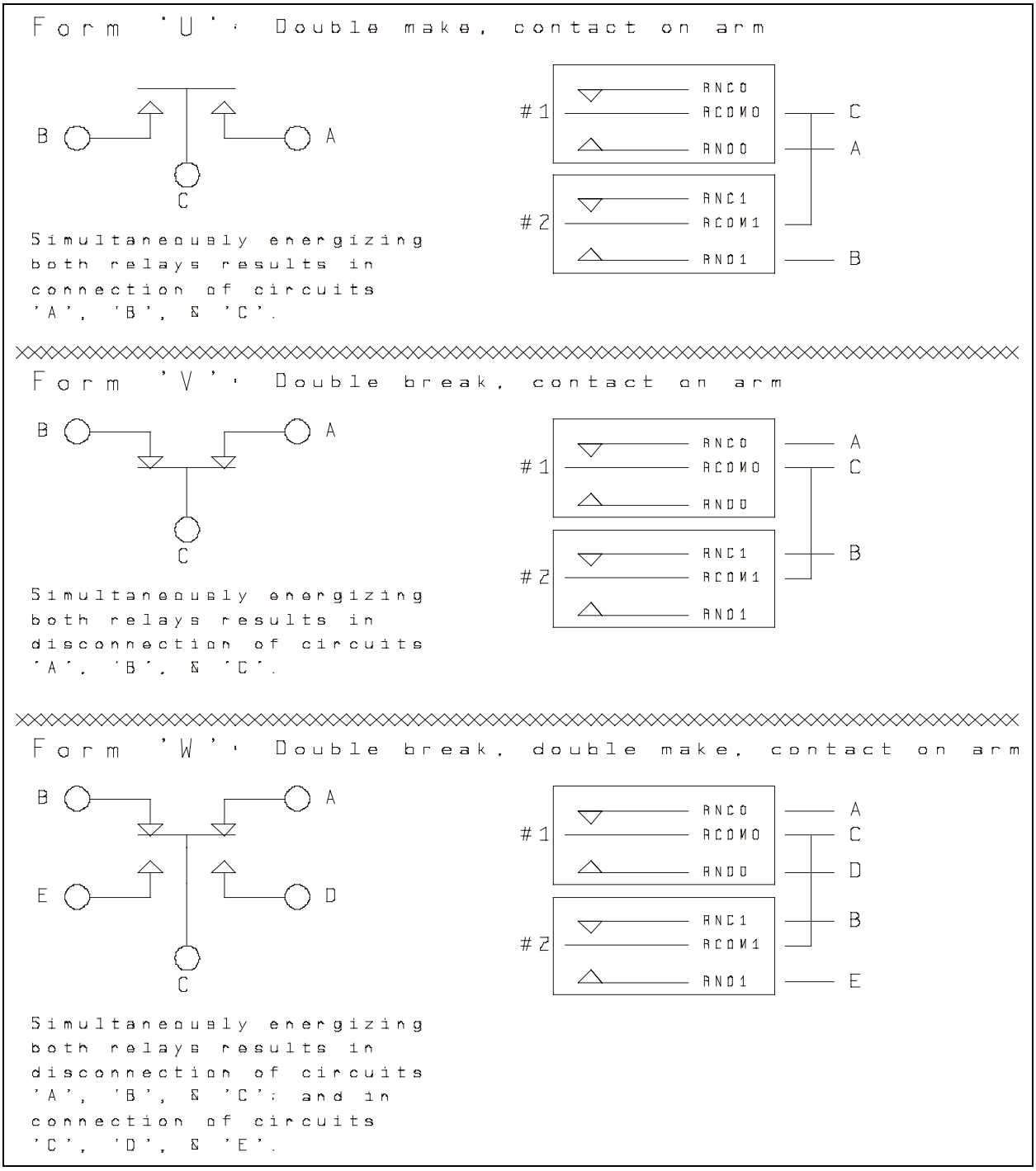


Figure B-7 RELAY16 Form 'U', 'V' and 'W' Applications

B.2.15 Two Relays—Double-Make Transfer

Figure B-8 presents Forms ‘X,’ ‘Y’ and ‘Z’ configurations of the RELAY16 contacts.

The Form ‘X’ diagram uses a two-relay configuration for a double-make transfer. Simultaneously turning both relays ‘ON’ or energizing them results in connection of circuits A and B contacts. Simultaneously turning both relays ‘OFF’ or de-energizing them results in disconnection of circuits A and B contacts.

B.2.16 Two Relays—Double-Break Transfer

The Form ‘Y’ diagram uses a two relay configuration for a double-break transfer. Simultaneously turning both relays ‘ON’ or energizing them results in disconnection of circuits A and B contacts. Simultaneously turning both relays ‘OFF’ or de-energizing them connects the circuits A and B contacts.

B.2.17 Two Relays—Double-Break-Double-Make Transfer

The Form ‘Z’ diagram uses a two relay configuration for a double-break-double-make transfer. By simultaneously turning both relays ‘ON’ or energizing them results in a disconnection of contacts A and B, followed by a connection of contacts D and E. Simultaneously turning ‘OFF’ or de-energizing both relays results in (first) the disconnection of contacts D and E, followed by the connection of contacts of A and B.

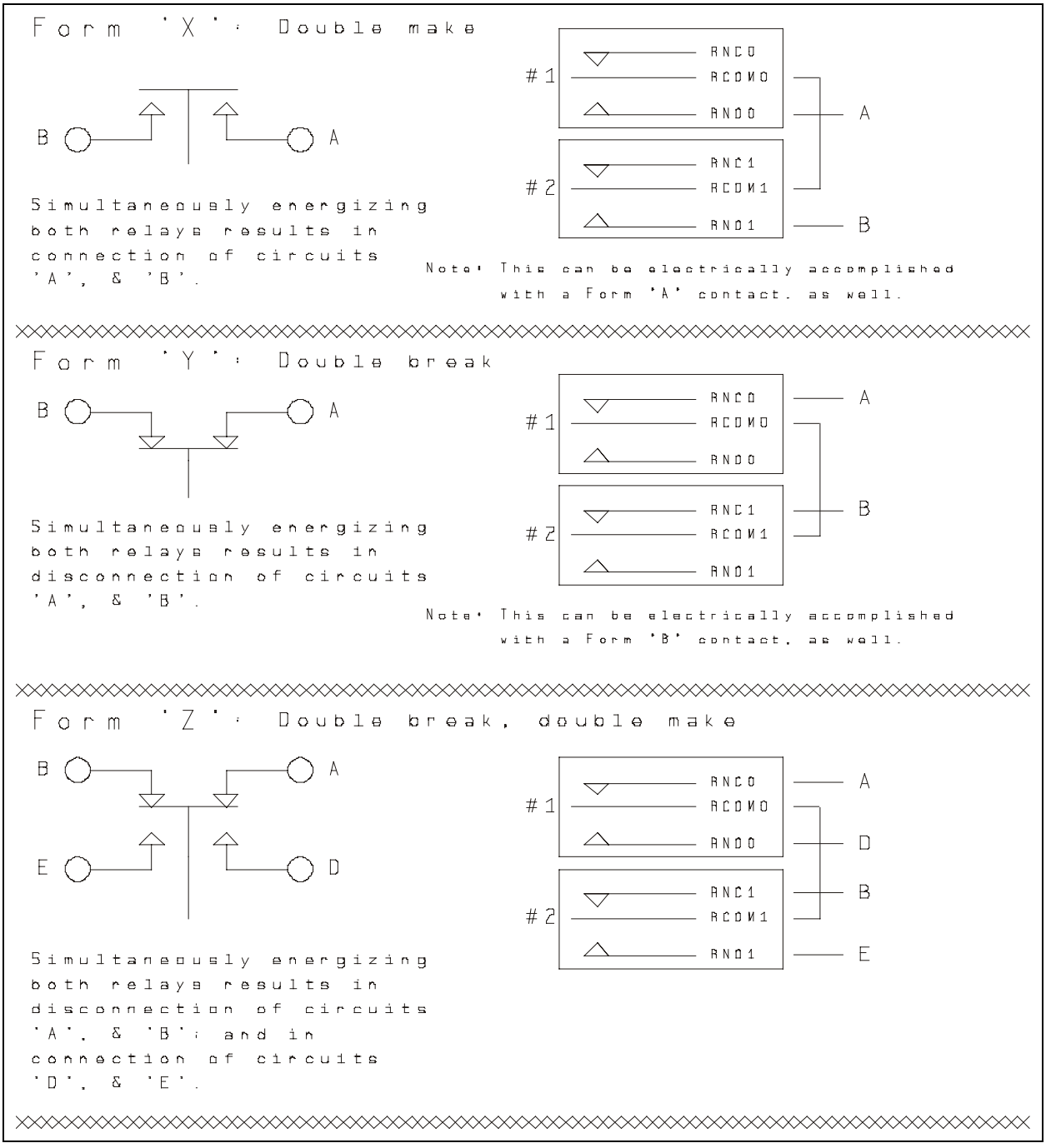


Figure B-8 RELAY16 Form 'X', 'Y' and 'Z' Applications

B.2.18 Electricians Parallel Application

The following "wiring" application shows a technique that could replace wall switches for light control with computer control. While the RELAY16's 4-way solution is drawn using relays in a single RELAY16 IP Module, a more practical solution would involve three separate RELAY16 boards controlled by three different light users.

The top half of Figure B-9 shows how an electrician might modify a 3-way electrical circuit to make it a 4-way electrical circuit by adding one DPDT switch (and more wire) to make it possible to turn a shared lamp ON and OFF from any of three different wall switches.

The bottom half of Figure B-9 shows how to wire four relays up to three different RELAY16 boards to accomplish the same task using computer control.

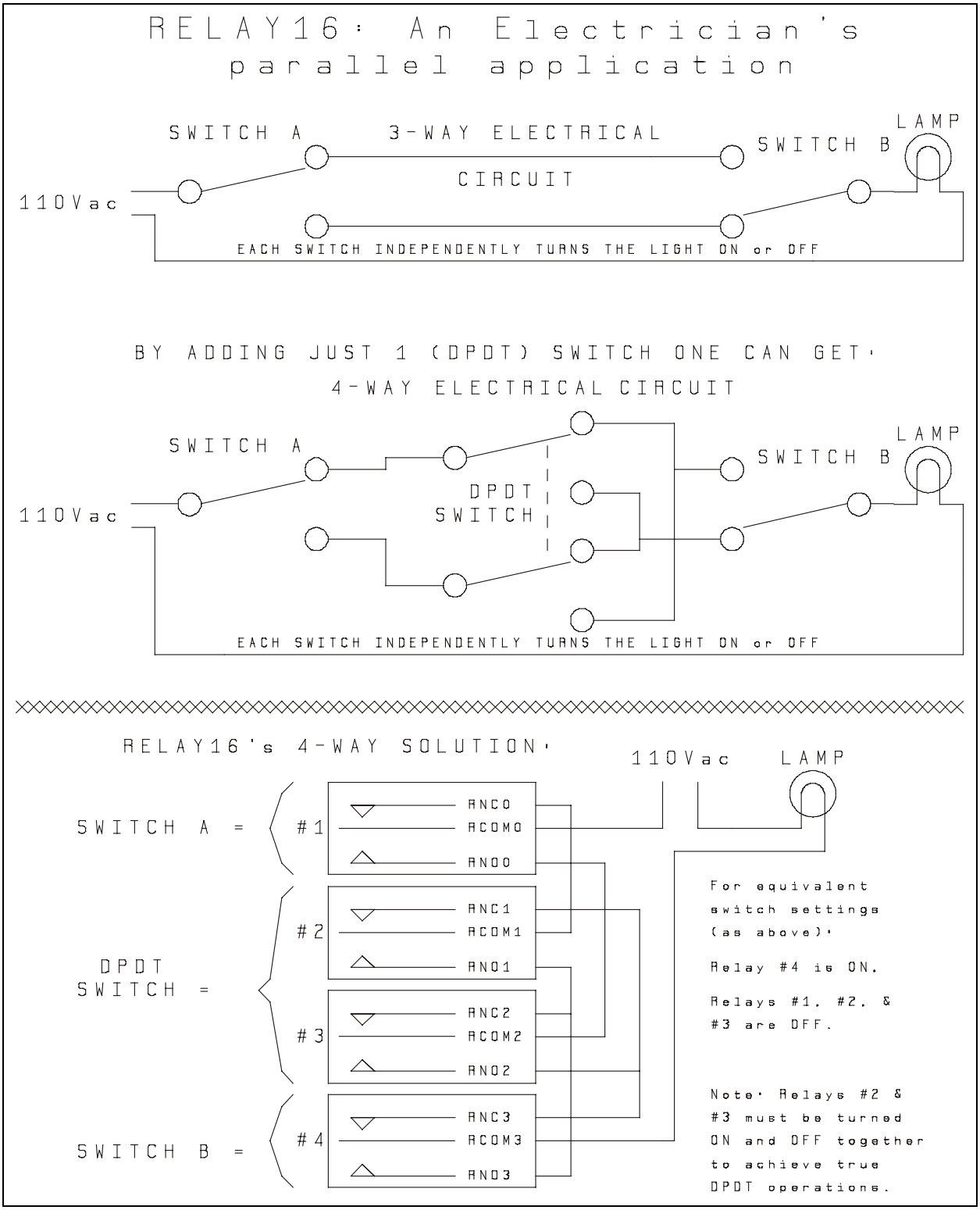


Figure B-9 Electricians Parallel Application

APPENDIX C

PROGRAMMING GUIDE

TABLE OF CONTENTS

C.1 Overview C-1
C.2 Description C-1
C.3 IP Module ID PROM Listing C-1
C.4 IP Module I/O Address Map C-2
C.5 Word Access Address Translation C-3
C.6 Byte Access Address Translation C-4
C.7 Data Register Bit Description (IPA = 0x00) C-5
C.8 Programming Example C-6

TABLES

Table C-1 RELAY16 ID Address Space Listing C-2
Table C-2 RELAY16 I/O Address Map C-2
Table C-3 Word Access Address Translation Table C-3
Table C-4 Byte Access Address Translation Table C-4
Table C-5 Data Register Bit Descriptions C-5

C.1 Overview

This section of the manual describes the operation of the RELAY16 from the software perspective, detailing the RELAY16 registers and providing programming examples. A more detailed description of the hardware can be found in Chapter 2, PRODUCT OVERVIEW, and appendix B, TYPICAL APPLICATIONS.

C.2 Description

The RELAY16 is an easy-to-use IP Module with 16 SPDT mechanical relays. All 16 relays are controlled (energized/de-energized) by writing to a single 16-bit register. When a relay is de-energized, the normally closed contacts are closed, and the normally open contacts are open. When a relay is energized, the normally closed contacts are open, and the normally open contacts are closed.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IP Module to provide “no-wait” read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus timeout error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

Table C-1 is the RELAY16 emulated ID Address Space PROM listing:

Table C-1 RELAY16 ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII “I”	0x49
IPA = 0x01	ASCII “P”	0x50
IPA = 0x02	ASCII “A”	0x41
IPA = 0x03	ASCII “C”	0x43
IPA = 0x04	Systran’s ID	0x45
IPA = 0x05	RELAY16’s Model Number	0x64
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0xE2

C.4 IP Module I/O Address Map

The RELAY16’s I/O Address Map contains a single register in the IP Module I/O space (IPA = 0x00).



NOTE: The address detector circuitry is fully decoded. Therefore, any attempt to access IPA addresses at and above 0x01 will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IP Module resides.

Table C-3 is the RELAY16 I/O Address Map and contains the data register:

Table C-2 RELAY16 I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	Data Bits [15:8]	Data Bits [7:0]	Data Register 16-bits

C.5 Word Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VMEbus Address	PC-AT Bus Address	NuBus Address	IP Module Address
BASE + 0x0	BASE + 0x0	BASE + 0x2	IPA = 0x00
BASE + 0x2	BASE + 0x2	BASE + 0x6	IPA = 0x01
BASE + 0x4	BASE + 0x4	BASE + 0xA	IPA = 0x02
BASE + 0x6	BASE + 0x6	BASE + 0xE	IPA = 0x03
BASE + 0x8	BASE + 0x8	BASE + 0x12	IPA = 0x04
BASE + 0xA	BASE + 0xA	BASE + 0x16	IPA = 0x05
BASE + 0xC	BASE + 0xC	BASE + 0x1A	IPA = 0x06
BASE + 0xE	BASE + 0xE	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x1A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B

C.6 Byte Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VMEbus Address	PC-AT Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 0x1	BASE + 0x0	BASE + 0x3	IPA = 0x00	0
BASE + 0x0	BASE + 0x1	BASE + 0x2	IPA = 0x00	1
BASE + 0x3	BASE + 0x2	BASE + 0x7	IPA = 0x01	0
BASE + 0x2	BASE + 0x3	BASE + 0x6	IPA = 0x01	1
BASE + 0x5	BASE + 0x4	BASE + 0xB	IPA = 0x02	0
BASE + 0x4	BASE + 0x5	BASE + 0xA	IPA = 0x02	1
BASE + 0x7	BASE + 0x6	BASE + 0xF	IPA = 0x03	0
BASE + 0x6	BASE + 0x7	BASE + 0xE	IPA = 0x03	1
BASE + 0x9	BASE + 0x8	BASE + 0x13	IPA = 0x04	0
BASE + 0x8	BASE + 0x9	BASE + 0x12	IPA = 0x04	1
BASE + 0xB	BASE + 0xA	BASE + 0x17	IPA = 0x05	0
BASE + 0xA	BASE + 0xB	BASE + 0x16	IPA = 0x05	1
BASE + 0xD	BASE + 0xC	BASE + 0x1B	IPA = 0x06	0
BASE + 0xC	BASE + 0xD	BASE + 0x1A	IPA = 0x06	1
BASE + 0xF	BASE + 0xE	BASE + 0x1F	IPA = 0x07	0
BASE + 0xE	BASE + 0xF	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

* Byte-lane 1 not applicable for ID Space

C.7 Data Register Bit Description (IPA = 0x00)

The RELAY16 has one 16-bit-wide register with each bit corresponding to a relay. The RELAY16 supports word (16-bit) reads, and word and byte (8-bit) writes. Byte writes are non-destructive to the adjacent byte. On power-up all bits are set to zero (all relays de-energized). The register is described in detail below.

Table C-5 Data Register Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	RL 15	RL 14	RL 13	RL 12	RL 11	RL 10	RL 9	RL 8	RL 7	RL 6	RL 5	RL 4	RL 3	RL 2	RL 1	RL 0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-up state	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RL15 - RL0 : These bits control the energization of relays 15 to 0. Bit 0 corresponds to relay 0, bit 1 to relay 1, ... , bit 15 to relay 15. If the bit is set to 0 the corresponding relay is de-energized. If the bit is set to 1, the relay is energized.

C.8 Programming Example

The following example illustrates how to program the RELAY16 device. In the power-up state, all of the relays are all de-energized. As previously stated, if a relay is de-energized, the normally closed contacts are closed, and the normally open contacts are open. If a relay is energized, the normally closed contacts are open, and the normally open contacts are closed.

- At power-up the data register value is ‘0x0000’ corresponding to all relays de-energized.
- Write ‘0x0001’ to the data register.
- Relay 0 is now energized, all other relays are de-energized.
- Write ‘0x8000’ to the data register.
- Relay 15 is now energized, all other relays are de-energized.
- Write ‘0x00FF’ to the data register.
- Relays 0 to 7 are now energized, relays 8 to 15 are de-energized
- Write ‘0xFF00’ to the data register.
- Relays 8 to 15 are now energized, relays 0 to 7 are de-energized.
- Write ‘0xFFFF’ to the data register.
- All relays are now energized.
- Write ‘0x0000’ to the data register.
- All relays are now de-energized.

GLOSSARY

[x:y] ---------- Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane ---------- 8-bits of a data bus on octal boundaries.

CAE ---------- Computer Aided Engineering.

dB ---------- Decibels.

doublewide ---------- An IP Module that is twice the size of the singlewide board.

EPLD ---------- Erasable Programmable Logic Device.

ID PROM ---------- The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IP Module ---------- Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O ---------- Input/Output.

IP Module logic bus ---------- A synchronous, 8 MB/sec, 16-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

IPDbus ---------- IP Module Data Bus.

MTBF ---------- Mean Time Between Failures.

ns, µs, ms ---------- Nanoseconds, microseconds, and milliseconds, respectively.

SPDT ---------- single pole, double throw.

singlewide ---------- An IP Module printed circuit board (3.9” by 1.8"). Each module has two 50-pin connectors.

VHDL ---------- Very high-speed integrated circuit Hardware Description Language.

VSWR ---------- Voltage Standing Wave Ratio.

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INDEX

A

address detector circuitry C-2
ANSI/VITA 4-1995 ..... 1-2, 2-2
arc suppression 2-6

B

backplane 2-1
base address C-3, C-4
board response times 4-1
bounce times 4-2, 4-5
buffer 2-3

C

carrier board 1-1, 2-3, 2-5, 3-1, 3-2, 3-3, A-2, C-1, C-2
circuit capacitance 2-7
cleaning 2-6, 2-7
connector 2-1, 2-2, 2-4, 3-2, A-2, B-1
contact bounce 4-4, 4-5
contact failure 2-6

D

data bus interface 2-2
data register 2-2, C-2, C-5, C-6
diode protection 2-7
DMA activity A-1

E

electromechanical relay 1-1
electrostatic sensitive device 3-1
EMF 2-2, 2-6, 2-7
emulation 2-3, C-1, C-2
environmental A-2
EPLD Altera device 2-2, 2-3

G

gold cladding 2-4, 2-5

I

I/O address map C-2
I/O read A-1
I/O write 2-3
ID address space C-1, C-2
ID PROM 2-3, C-1
ID read 2-2, 2-3, C-1
ID write A-1
inductive loads 2-6, 2-7
interrupt vector transfers A-1
IP Module 1-1, 2-1, 2-2, 2-3, 2-5, 3-1, 3-2, 3-3, 4-1, 4-2, 4-3, A-1, B-1, B-13, C-1, C-2, C-3, C-4
IP Module carrier 2-1, 2-2, 3-1, 3-2, 3-3, 4-1

L

load impedance 2-6
logic analyzer
snapshot 4-2

M

magnet polarization 2-6
manual 1-1
manuals 3-1
maximum carrying current 2-4
memory transfers A-1
MTBF A-2

P

pin assignments 3-2
power requirements A-1
power-up 2-3, C-5, C-6
protocol A-1

R

read rate A-1
read/write rate A-1
register 2-1, 4-4, B-1, C-1, C-2, C-5
release time 2-6, 2-7, 4-2, 4-4, 4-5
rising edge 4-2, 4-4

S

series resistance 2-6, 2-7
silver contact material 2-4
single-pole-double-throw B-2
single-pole-single-throw B-2
singlewide 2-1
sinking current 2-3
snapshots 4-4, 4-5
specifications 2-1, 2-4, 2-5
surge voltage A-2
switching current 2-4, A-2
switching power A-1
switching voltage A-1

T

thermal characteristics 2-3
timing measurements 4-1
tristate 4-2

V

varistor 2-7

Z

zener diode 2-7

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