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PCISC5

PCI Slave 5-Slot IP Module Carrier
Hardware Reference

Document No. B-T-MR-PCISC5##-A-0-A8



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1. INTRODUCTION

1.1 How to Use This Manual

This is a reference manual for the Systran PCISC5 PCI Slave 5-slot IP Module Carrier herein referred to as the PCISC5 board, part number BHAS-PCISC5.

1.2 Scope

This manual covers the physical and operational description of the PCISC5, from both hardware and software perspectives. This manual also contains detailed technical information about the PCISC5 performance characteristics, and a few typical applications. You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IP Modules on your carrier(s) to effectively use this manual.

1.3 Style Conventions

- Called functions are italicized. For example, OpenConnect()
- Data types are italicized. For example, int
- Function parameters are bolded. For example, Action
- Path names are italicized. For example, utility/sw/cfg
- A bit-range is designated by [x:y] where "x" is the left-most bit and "y" is the right-most bit. (For example, data bus [7:0] refers to the least significant eight bits).
- File names are bolded. For example, config.c
- Path file names are italicized and bolded. For example, utility/sw/cfg/config.c
- Hexadecimal values are written with a "0x" precfix. For example, 0x7e
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/). For example, /SYNC
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded.

```
ls
file1          file2             file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.4 Related Publications

- PCI Local Bus Specification Rev. 2.1- PCI Special Interest Group
- American National Standard for IP Modules, version ANSI/VITA 4-1995 - Published by the VMEbus International Trade Assoc. 7825 E. Gelding Dr. Suite 104, Scottsdale AZ. 85260-0720
- QuickLogic Headquarters, 1277 Orleans Drive, Sunnyvale, CA 94089-1138, USA, Telephone: + (408) 990-4000, Fax: + (408) 990-4040

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- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

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2. PRODUCT OVERVIEW

2.1 Overview

The Systran PCISC5 Slave 5-slot IP Module Carrier board (part number BHAS-PCISC5) is a PCI (PC/AT) slave add-in board that supports five singlewide IP Modules, two doublewide IP Modules with one singlewide or one doublewide with three singlewide IP Modules. The PCISC5 supports 8 MHz IP transfers of ID, I/O, Interrupt Acknowledge and Memory for all slots. The PCISC5's PCI interface design is compliant with the PCI bus specification V2.1 and the IP interface is designed in accordance with the *American National Standard for IP Modules* (ANSI/VITA 4-1995) specification.

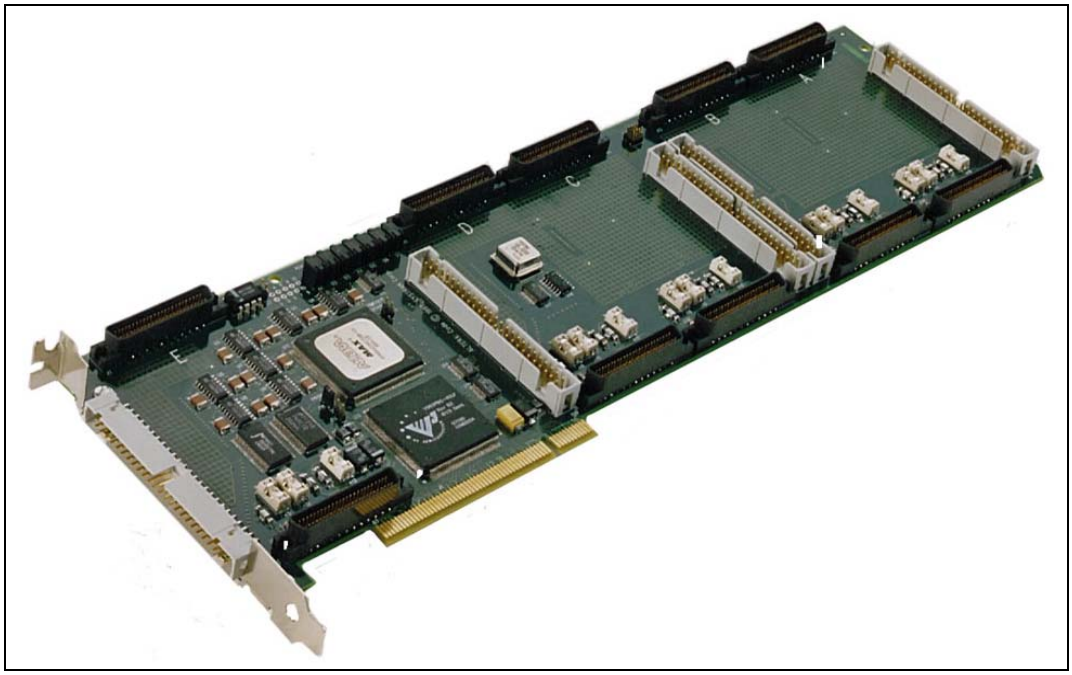


Figure 2-1 PCISC5 Board

The PCISC5 design does not insert IP hold cycles. This guarantees the highest throughput possible for this PCI-to-IP Module bus-coupling carrier. The PCISC5 provides up to 250 I/O points (50 per IP) per PCI slot with the area under three of the IP Modules as a solid ground plane to provide "quiet" operating conditions for sensitive analog IP Modules. LEDs on the PCISC5 provide diagnostic information on accesses to the IPs, the PCISC5 local registers, and an IP acknowledgment signal. The PCISC5 has a very easy-to-use and flexible PCI interrupt capability where the individual interrupts from each IP Module can be programmed to assert a common interrupt request to the PCI bus.

2.1.1 Features

- Up to 250 I/O points in a single, PCI slot.
- I/O, ID, INT and MEM transfers on all slots with no HOLD cycles inserted.
- Precise PCI local memory map for easy access to IP Modules and local registers.

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- Board base address automatically configured by system BIOS at power-up.
- Supports five singlewide IPs, or any combination of doublewide and singlewide cards adding up to five slots.
- Each of 10 IP interrupt requests (two per IP Module slot) can individually assert a common PCI interrupt.
- Local bus interface time-out can be enabled via software.
- Board is memory mapped via a memory aperture size in the PCI bridge.
- Independent field-replaceable fuses, and 'T'-type filters are used for the +5, +12, and -12 V power feeding each IP.
- Seven IP/Carrier Access and IP Acknowledge indicators (with pulse stretchers).
- Pure ground plane under three of five IP Modules (slots A, B and C) for "quiet" operation.
- Posts IP error signals as status.
- Supports writes to ID space.
- Resets individual IP Modules via software.
- Five "standard" I/O ribbon cable connections.
- Supports five "strobe" connections (one per slot).

2.2 Functional Description

2.2.1 Memory Mapping Scheme

The mapping scheme for the ID and I/O address spaces on all five IP Modules as well as the carrier's on-board CSRs are all made at fixed addresses relative to the board base address, which is contained in the PCI Configuration Space Registers. These registers are found inside the V962PBC PCI Bridge IC (U13 on the PCISC5). For more information on these registers, contact QuickLogic as shown in Section 1.4 Related Publications.

IP Module memory accesses are performed relative to base addresses set within an aperture register in the Configuration Space and on-board address decoding. Memory size as well as base address is controlled by the aperture settings. Chapter 3, INSTALLATION and Appendix B, PROGRAMMING GUIDE, discuss the memory mapping in more detail.

2.2.2 PciCfg Utility

The **PciCfg** Utility facilitates the modification of the PCI configuration EEPROM on up to 16 installed IP Carriers on a single machine. This software allows for quick, easy disabling or enabling of the IP module memory space. If the IP memory space is disabled, the carrier occupies much less PCI memory space. Instructions for installation and use of the **PciCfg** program disk are included in Appendix E, PCICFG UTILITY FOR PCI-BASED CARRIERS of this manual. The **PciCfg** Utility software is provided with this manual in a sleeve on the inside back cover.

2.2.3 ID Transfers

IP Module ID transfers are supported as 8-bit or 16-bit local transfers. ID transfers are performed by a byte or word read/write operation of the slot IP Module ID address space from the PCI Bus. The ID ROM values are located every other byte at IP Module odd-byte locations (IP Module byte-lane 0). For 8-bit reads the even byte is discarded. The ID

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ROM area allows read or write accesses to support future IP Modules requiring writes to the ID address space.

The IP Module data bus has been made big endian to be compatible with VME. Since PCI is 32-bit little endian, accesses to the IP Modules occur for PCI even addresses on four byte boundaries only. On PCI, the odd byte is the upper byte (D15 through D8) and the even byte is the lower byte (D0 through D7). For this reason, on 16-bit reads and writes, the IP Module odd byte is transferred on the PCI even byte, and the IP Module even byte is transferred on the PCI odd byte. Single-byte transfers are performed on PCI even addresses only and access the IP Module odd byte.

2.2.4 I/O Transfers

IP Module I/O transfers are supported as 8-bit or 16-bit PCI transfers. I/O transfers are performed by a byte or word read or write operation of the slot IP Module I/O address space from the PCI Bus.

2.2.5 Interrupt Transfers

Interrupts are requested by the IP Module by assertion of N_INTREQ0 or N_INTREQ1. An independent Local-to-PCI interrupt circuit handles each of these IP Module interrupt request lines which asserts the interrupt request line INTA# to the PCI bus. This provides a minimum delay in asserting the interrupt request to the platform CPU.

In detail, the hardware and firmware in the PCISC5 are configured such that any of 11 interrupts (Intreq0 and Intreq1 from each of five IP Modules and a time-out interrupt) will generate an INTB# input to the on-board PCI bridge which will generate an INTA# to the PCI bus. The INTB# from the IP Interface controller will only be generated if enabled to do so in software. Interrupts are disabled upon power-up to prevent a possible interrupt cycle from occurring until the system becomes stable. Upon completion of power-up, bits in the Control Register on the PCISC5 can then be set to enable IP and time-out interrupts.

2.2.6 Interrupt Configuration

The interrupt-select tiers in Figure 2-2 show the interrupt “flow” from the IP Modules to the PCI bus.

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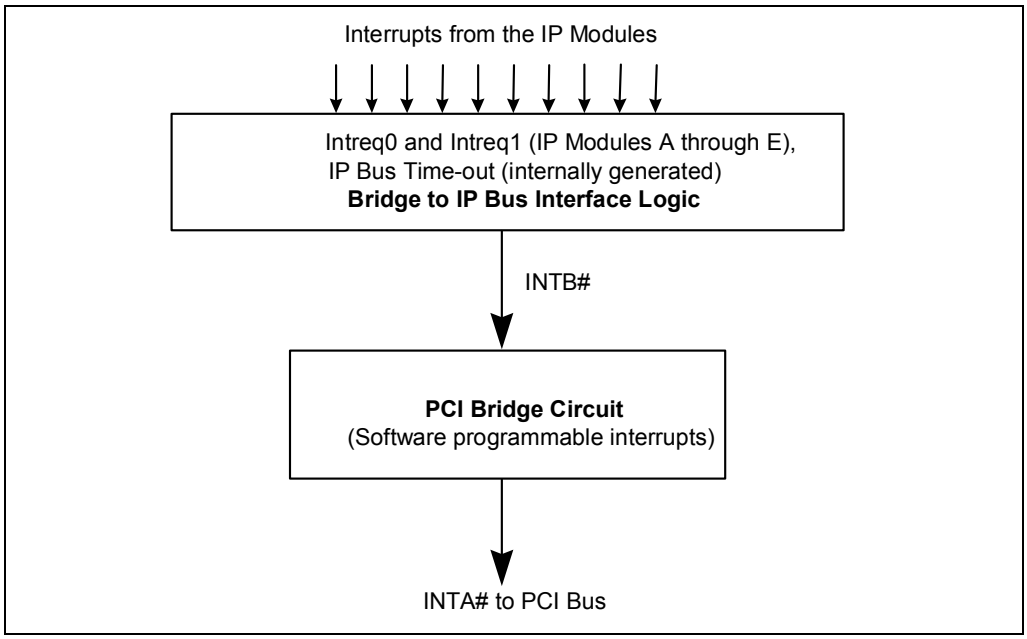


Figure 2-2 Interrupt-Select Tiers

2.2.7 Diagnostic LEDs

The PCISC5 has seven diagnostic LEDs (D1 – D7) as shown in Figure 3-3. The LEDs on the board labeled "A", "B", "C", "D", "E" and "CRA" (D7, D6, D5, D4, D3, and D2, respectively), indicate when a READ or WRITE transaction is attempted to one on the five IP Modules or a carrier register. LED (D1) labeled "ACK" indicates an acknowledgment by the IP Module of the attempted access. This scheme provides independent verification of the access and the acknowledgment.

2.2.8 IP Module Reset

Independent or simultaneous resetting of the IP Modules is facilitated through writes to the Reset register. Monitoring of the pulse-stretched reset signals is made possible by reading the Reset register. See Appendix B, PROGRAMMING GUIDE, for a detailed description of this register.

2.2.9 Error Status

Monitoring of the IP Module ERROR signals is made possible by reading the Error Status register. See Appendix B, PROGRAMMING GUIDE, for a detailed description of this register.

2.2.10 Strobe Signals

The IP Module STROBE signals can be connected via an 8-pin header (J21).

2.2.11 Power Supply Filtering

Independent 'T'-type filters are used for the +5 V, +12 V, and -12 V power feeding each IP Module. This arrangement provides superior power supply filtering.

2.2.12 Fuses

Independent field-replaceable fuses are used for the +5 V, +12 V, and -12 V power feeding each IP Module. This provides superior short-circuit protection.

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NOTE: Replacement fuses can be purchased directly from Littelfuse, Inc. Phone (708) 829-0400.

1 Amp Fuse Manufacturer's Part Number R451001
2 Amp Fuse Manufacturer's Part Number R451002.

2.3 Theory of Operation

2.3.1 Block Diagram Description

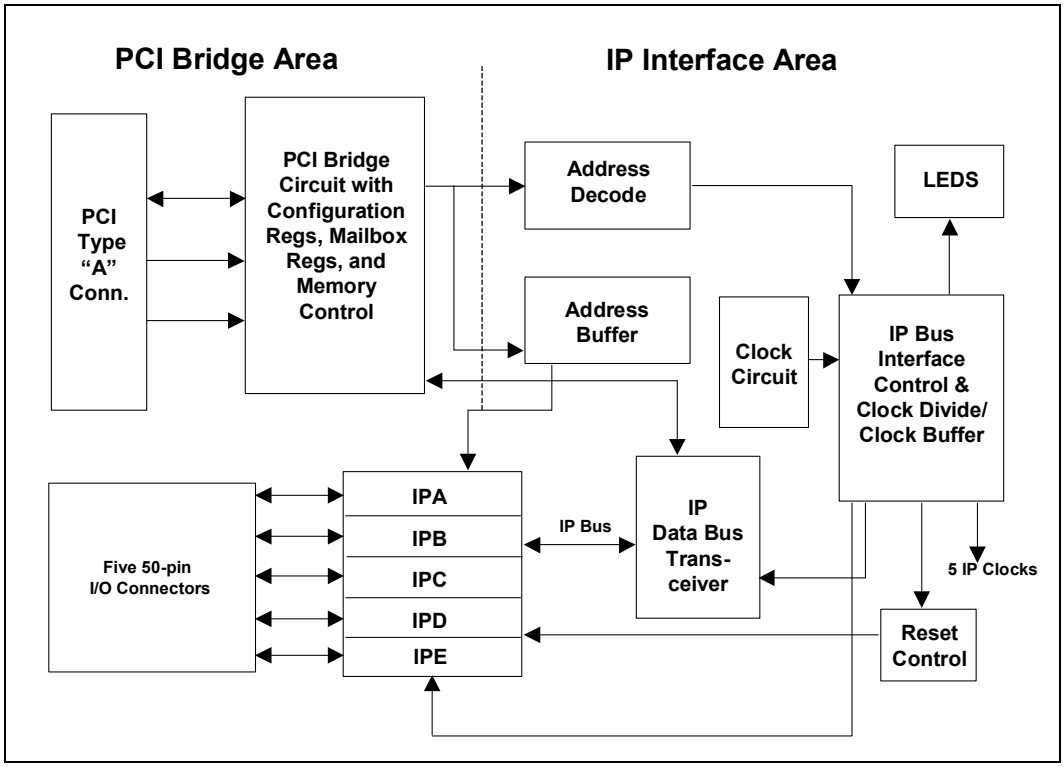


Figure 2-3 PCISC5 Block Diagram

Figure 2-2 is a simplified block diagram of the PCISC5 representing the signal flow between the PCI bus, IP Module Logic Bus and the IP Module I/O connectors. On the left side of the diagram is the PCI bus connector through which all transfers between the host computer and the Bridge registers, CSR registers or IP Modules flow. The PCI bus transfers **do not** insert any IP Module hold cycles into the accesses to the IP Modules.

The block labeled "ADDRESS DECODE" handles decoding of the aperture address generated from the bridge circuit. This circuit determines which select strobe to generate to a particular IP Module based on the address bits LA31 through LA2.

The block labeled "ADDRESS BUFFER" provides the common IP address bits IPA1 through IPA6 to all the IP Modules as well as address bits 7 through 22 during the select cycle for memory transactions.

The block labeled "IP DATA BUS TRANSCEIVER" allows for buffering between the PCI bridge device; and the IP Module data bus where the IP Interface Control controls direction on, and enabling to the bus.

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The block labeled “IP BUS INTERFACE CONTROL” provides timing and control of the data flow between the PCI bus bridge and the IP Module bus. It also provides control of the address buffers such that the IP Module data bus will contain an address only during the select cycle of a memory transfer. This block also has a programmable time-out circuit that prevents the local side of the PCI bridge circuit from “hanging.” This block will also produce the reset pulses for the IP Modules and the required synchronous select cycles for ID, I/O, Interrupt Acknowledge and Memory transactions.

The RESET CONTROLLER (Reset Cont.) block consists of a bank of pulse stretchers that convert the narrow trigger from the reset register in the IP INTERFACE CONTROL part to a 200 ms pulse for each of the IP Modules. The wide pulses will then be synchronized to the IP bus clock such that they will be deasserted synchronously.

The “LEDS” block contains pulse stretchers and seven LEDs to indicate transaction attempts to each of five IP Modules and the on board CSR registers as well as an acknowledge indicator.

The “CLOCK CIRCUIT” block consists of a 16 MHz oscillator, divider flip-flop and low-skew buffers to allow a separate clock for each IP Module.

The block labeled “PCI BRIDGE CIRCUIT” consists of a large-scale IC that provides an interface between the PCI bus and the interface to the IP Module bus.

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3. INSTALLATION

3.1 Unpack the PCISC5

Table 3-1 lists the contents of the PCISC5 shipping packages.

Table 3-1 Contents of PCISC5 Shipping Packages

Qty	Description
1	PCISC5 Printed Circuit Assembly
2	Surface mount spare fuses (one-1 Amp, one-2 Amp)
1	PCISC5 Hardware Reference *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR- PCISC5).

3.2 Visually Inspect the PCISC5

Examine the PCISC5 to determine if any damage occurred during shipping.

3.3 Install the PCISC5



NOTE: The PCISC5 is an Electrostatic Sensitive Device (ESD). Install the PCISC5 on an anti-static workbench to protect the IP Modules and carrier board.

The tools required for the PCISC5 installation are listed in Table 3-2.

Table 3-2 PCISC5 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)
1	Standard Phillips Screwdriver

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3.3.1 Installation of IP Modules on the PCISC5

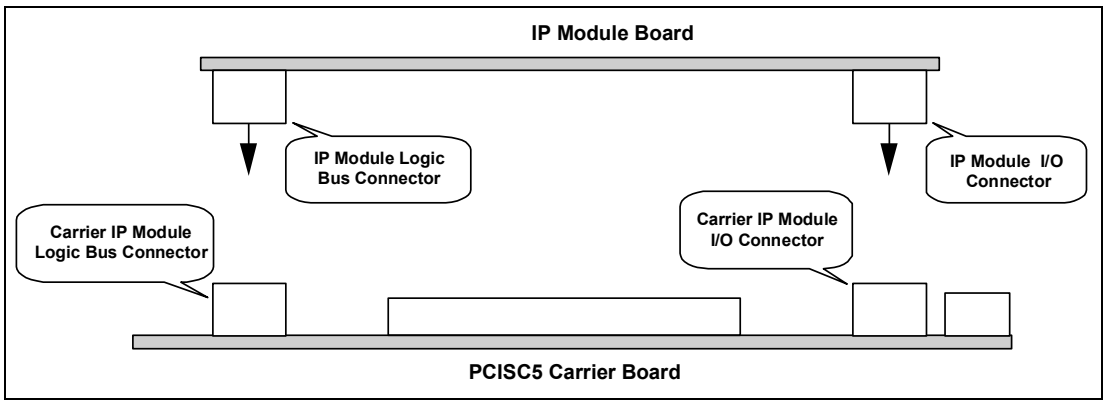


Figure 3-1 Installation of an IP Module on the PCISC5

Referring to the appropriate figures and table described below, perform the following steps in removing the PCISC5 from its shipping container (or from an existing installation) and installing IP Modules. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the PCISC5 from its shipping container and move it to the ESD-controlled area where the installation of the IP Module(s) can be made.

*2a Remove the PCISC5 from the PC if modifications are necessary, and move it to an ESD controlled area where the installation or changing of IP Modules can be made.

3. Set the Time-out-disable jumper (J20) and the EEPROM Write Protect Jumper (J17) to the desired positions. Also, set the Board Present Jumpers (J18, J19) to a position that will best reflect power draw of the board. This setting will be dependent on the amount of power necessary to run the IP Modules installed onto the carrier. The default setting shipped will assume 15 W usage.
4. Install the IP Module(s) onto the carrier board by applying adequate and equal pressure to the IP Module(s) at both ends and on the PCISC5 board.

*5. Install four M2x5mm flat head machine screws onto the IP Module's connectors.

*6. Install I/O cables necessary onto PCISC5.

7. Install the PCISC5 into desired PCI slot of a PC or PCI backplane and fasten the PCISC5 mounting bracket to the unit using the screw provided with the computer, and a Phillips head screwdriver.

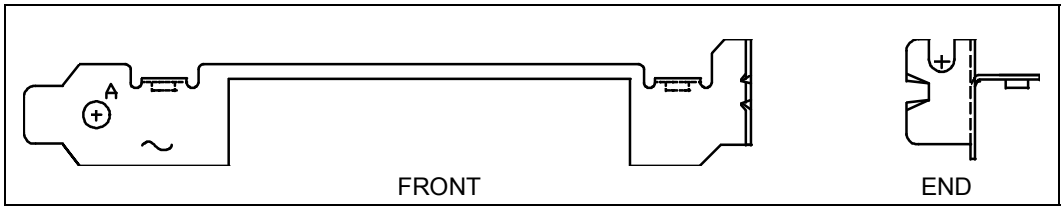


Figure 3-2 PCISC5 Faceplate

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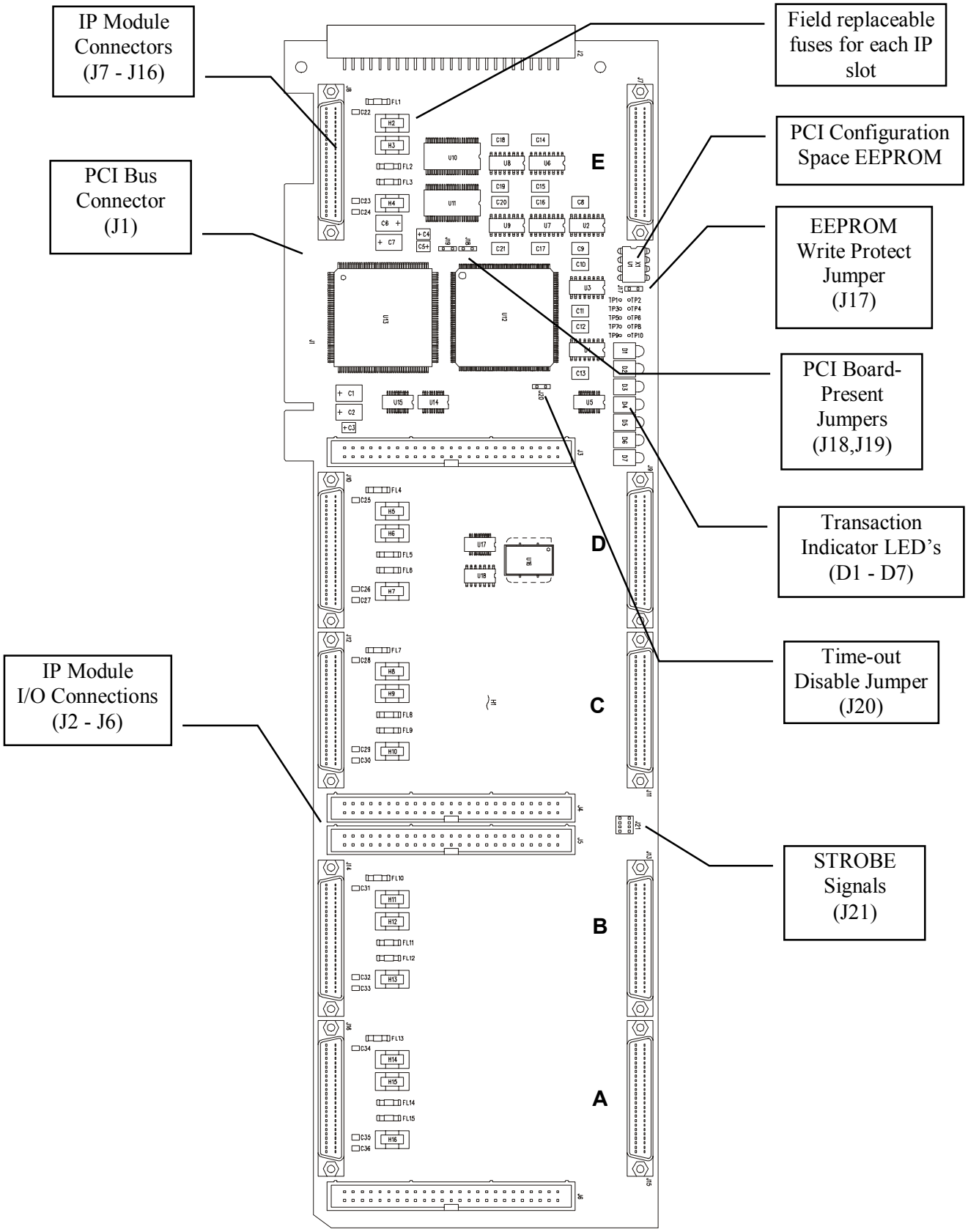


Figure 3-3 PCISC5 Mechanical Assembly

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3.3.2 PCISC5 PCI Base Address

The PCISC5 PCI board base address is set by the system BIOS using values pre-programmed by the EEPROM in slot U1. A memory aperture between the PCI bus and the IP Module bus is set up in the bridge IC by the BIOS using the required aperture size from the EEPROM. This memory size is large enough to encompass the I/O, ID and memory accesses of up to 8 MB for all five IP Modules as well as on board control and status registers. Note that all address locations accessed on the PCISC5 are on four-byte boundaries, therefore 128 MB of space has been allowed for the PCISC5.



NOTE: The mapped PCI memory space on a standard PC is controlled by the system BIOS and is not normally controlled by the user. Attempts to change the base address of the PCISC5 after power-up should be done so with caution. The amount of memory space required for the PCISC5 is provided by the EEPROM upon power-up. This space can be disabled, if necessary, by using the information in Appendix E PCICFG UTILITY FOR PCI-BASED CARRIERS.

Refer to Appendix B Programming Guide for details of PCI accesses to the PCISC5 on-board registers or IP Modules.

The PCISC5 memory base addresses are set in hardware for all IP Modules as below:

- PCI Base + 0x0100 0000 for the first location of IP A Memory.
- PCI Base + 0x0200 0000 for the first location of IP B Memory.
- PCI Base + 0x0300 0000 for the first location of IP C Memory.
- PCI Base + 0x0400 0000 for the first location of IP D Memory.
- PCI Base + 0x0500 0000 for the first location of IP E Memory.

ACCESS EXAMPLE

Assume it is desired to access the fourth memory location on IP Module C. This would be address 0x0000 000C (four byte boundary) on IP Module C. This equates to address 0x0300 0000 + 0x0000 000C or 0x0300 000C being accessed from the host system. If the BIOS system gives the PCISC5 a base address of, say, 0xF800 0000, then the address on the PCI bus when ~FRAME is asserted will be 0xFB00 0000. The bridge IC on the PCISC5 will strip away the PCI base address and present 0x0300 000C to the IP bus controller. The controller in turn will decode the upper address bits and begin a memory transaction to address 0x0000 000C on IP Module C.

Accesses to I/O, ID and interrupt acknowledge cycles are done in exactly the same manner. For base addresses to these areas, refer to Table B-1 in Appendix B.

3.3.3 Installation of I/O Cables

Users familiar with the VMESC5 and related products will notice right away that the form factor of and setup for a PCI IP Module carrier is different. Although the cabling for a PCI carrier may not be as convenient as that for VME, it is potentially more attractive since the cables will protrude from the rear of the unit rather than the front. The cables can be installed as described in the following paragraphs and in Figure 3-4.

The PCISC5 provides easy access to each IP Module I/O connector by allowing a direct connection to a 50-pin flat header. For IP Module E, access can be made directly at the rear panel of the PC through the mount bracket while access for IP Modules A through D headers can easily be provided for with ribbon connectors as described below.

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Each PCISC5 IP Module I/O connector pin number directly corresponds to each IP Module I/O pinout (that is, a one-to-one relationship with pin 50 connected to pin 50 down to pin 1 connected to pin 1).

On the PCISC5:

- Connector J3 is for IP Module slot “D” and is located near the transaction indicator LEDs.
- Connector J4 is for IP Module slot “C” and is located next to J5 and the strobe connector J21.
- Connector J5 is for IP Module slot “B” and is located next to J4 and the strobe connector J21.
- Connector J6 is for IP Module slot “A” and is located at the end of the board furthest from the mounting bracket.

To install cables for slots A through D, push the end of the ribbon cable with the female sockets into the male headers on the PCISC5 while noting the position of the notch on the female socket. Push until the connector is snugly fitted into the header. If possible, dress the ribbon cables such that there is a minimum thickness of ribbon cable lying between the PCISC5 and any neighboring interface card plugged into the PC or backplane. This is best done by installing the cable into IP slot “D” first (if necessary) and following with “C”, “B” and then “A” (if necessary).

The cables can then be stacked against J2 through the mounting bracket and the board then plugged into the slot after the cables have been dressed through.

Tagging each cable with a unique code using adhesive labels or permanent ink marker is recommended.



NOTE: Use of ribbon cables with strain relief clamps at the socket ends is not recommended unless no interface board will be inserted next to the component side of the PCISC5. This is due to tight spacing between installed IP Modules and any interface board plugged in next to the PCISC5.

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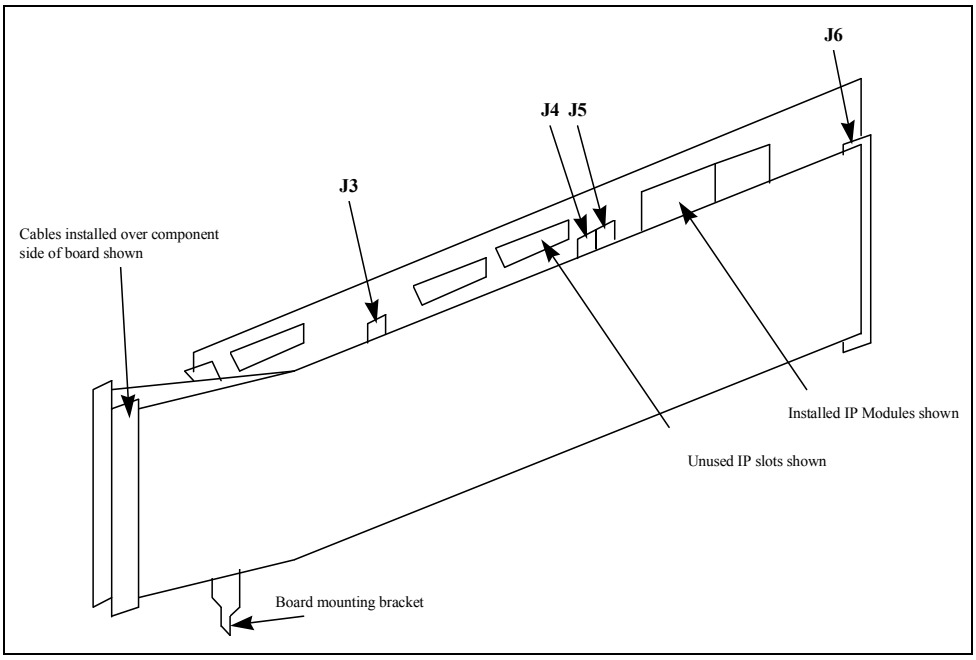


Figure 3-4 I/O Cable Installation

3.4 PCISC5 IP Module STROBE Connector

IP Module Logic Bus connector has a signal called "$\overline{\text{STROBE_X}}$" and is user-defined by the IP Module Logic Bus Specification. On the PCISC5, each of the strobe signals is provided through J21 with the IP Module slot "A" strobe signal on pin #1, "B" on pin #2, "C" on pin #3, "D" on pin #4, "E" on pin #5, and pins #6, #7 and #8 grounded, as indicated in Table 3-3. Each of the strobe signals on the PCISC5 is pulled-up to +5 V via 10 kΩ resistors. The strobe connector (J21) is located between the I/O connectors for IP Modules "B" and "C" near the top of the circuit board.

Table 3-3 PCISC5 STROBE Connector Pin Assignments

Pin Number	Signal Name
1	$\overline{\text{STROBE_A}}$
2	$\overline{\text{STROBE_B}}$
3	$\overline{\text{STROBE_C}}$
4	$\overline{\text{STROBE_D}}$
5	$\overline{\text{STROBE_E}}$
6	GROUND
7	GROUND
8	GROUND

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3.5 Time-out Jumper



NOTE: The PCISC5 is shipped with the time-out feature **disabled**. Verify that an IP Module selected for use on the PCISC5 produces the correct acknowledge signal before placing it on the carrier. In addition, verify that the software address used for accessing an IP Module on the PCISC5 agrees with the physical address of the IP Module in the system. Attempting to access an IP Module that is either not physically present or not correctly addressed on the PCISC5, or is faulty, could cause an endless string of PCI retries.

Although the PCI bus allows a maximum number of clock cycles before a retry, it is still possible for an incorrectly addressed IP Module to "hang" the local side of the bridge IC by not returning an acknowledge signal. Consequently, there is a potential for a wrongly addressed, faulty or missing IP Module to cause an endless string of PCI retries unless the carrier produces its own local time-out to release the bus.

In other cases, it may not be desirable for the carrier to abort a transaction. For example, when used for diagnostic purposes or for use as an IP Module with a very high number of specified wait states. For this reason, the PCISC5 allows a jumper-selectable enable/disable of the Time-out feature. The enable/disable selection determines the time-out operation for **all** IP Module positions on the PCISC5—either the time-out feature is enabled for all positions or it is disabled for all positions.

To **enable** the time-out feature, remove the shunt from header J20 (factory default) and set the TO_EN bit in the Carrier Control Register to a '1'. The PCISC5 will now abort any transaction to an IP Module after a maximum of 29 wait states (slightly less than four microseconds) if the selected IP Module fails to assert an acknowledge. After this time has elapsed, any data returned to the PCI bus is invalid.

To **disable** the time-out feature, place the shunt across both pins on J20 (or leave the shunt for header J20 off and set the TO_EN bit in the Carrier Control Register to a '0'). The PCISC5 will now allow an indefinite number of IP Module wait states.

3.6 PCI Board Present Jumpers

The PCI Board Present Jumpers (J18 and J19) are shipped with a default value of 15 watts required power. For systems that implement it, this will determine two things: the approximate power consumption of the board, and whether or not a board is plugged in at all. If IP Modules plugged into the PCISC5 are known to consume a great deal of power, the jumper shunts can be changed for a setting of 25 watts. For all possible settings, refer to Table 3-4.

Table 3-4 PCI Board Present Jumper Settings

Present #1 (J19)	Present #2 (J18)	Configuration
Out	Out	No board present
In	Out	Board present - 25 W max.
Out	In	Board present - 15 W max.
In	In	Board present - 7.5 W max.

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3.7 V3 EEPROM Write Protect Jumper

Jumper J17 enables/disables the write protect for the configuration EEPROM (U1) used to load the V3 chip PCI configuration registers upon power-up. The factory setting for J17 is write-protect enabled (no shunt installed). Normally, it will not be necessary to modify the configuration EEPROM. However, the EEPROM may be altered if necessary by installing a shunt to J17 that allows write-access to the EEPROM. Note that this jumper is used in the procedure called out in Appendix E, PCICFG UTILITY FOR PCI-BASED CARRIERS.

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3.8 PCI Bus Connector Pinout

Table 3-5 provides pin assignments for all PCI bus signals.

Table 3-5 PCI Bus Pin Assignments

PCI Bus P1/P2	Pin #	PCI Bus Signal	ISC Bus P1/P2	Pin #	PCI Bus Signal
A1	1	N/C	B1	63	-12V
A2	2	+12V	B2	64	N/C
A3	3	N/C	B3	65	GND
A4	4	J1-B4	B4	66	J1-A4
A5	5	+5V	B5	67	+5V
A6	6	~INTA	B6	68	+5V
A7	7	N/C	B7	69	N/C
A8	8	+5V	B8	70	N\C
A9	9	N/C	B9	71	PRSNT#1
A10	10	+5V	B10	72	N/C
A11	11	N/C	B11	73	PRSNT#2
A12	12	GND	B12	74	GND
A13	13	GND	B13	75	GND
A14	14	N/C	B14	76	N/C
A15	15	~PCIRST	B15	77	GND
A16	16	+5V	B16	78	PCICLK
A17	17	~GNT	B17	79	GND
A18	18	GND	B18	80	~REQ
A19	19	N/C	B19	81	+5V
A20	20	AD30	B20	82	AD31
A21	21	+3.3V	B21	83	AD29
A22	22	AD28	B22	84	GND
A23	23	AD26	B23	85	AD27
A24	24	GND	B24	86	AD25
A25	25	AD24	B25	87	+3.3V
A26	26	IDSEL	B26	88	~C/BE3
A27	27	+3.3V	B27	89	AD23
A28	28	AD22	B28	90	GND
A29	29	AD20	B29	91	AD21
A30	30	GND	B30	92	AD19
A31	31	AD18	B31	93	+3.3V
A32	32	AD16	B32	94	AD17
A33	33	+33V	B33	95	~C/BE2
A34	34	~FRAME	B34	96	GND

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PCI Bus P1/P2	Pin #	PCI Bus Signal
A35	35	GND
A36	36	~TRDY
A37	37	GND
A38	38	~STOP
A39	39	+3.3V
A40	40	N/C
A41	41	N/C
A42	42	GND
A43	43	PAR
A44	44	AD15
A45	45	+3.3V
A46	46	AD13
A47	47	AD11
A48	48	GND
A49	49	AD9
A50	50	KEYWAY
A51	51	KEYWAY
A52	52	~C/BE0
A53	53	+3.3V
A54	54	AD6
A55	55	AD4
A56	56	GND
A57	57	AD2
A58	58	AD0
A59	59	+5V
A60	60	N/C
A61	61	+5V
A62	62	+5V

ISC Bus P1/P2	Pin #	PCI Bus Signal
B35	97	~IRDY
B36	98	+3.3V
B37	99	~DEVSEL
B38	100	GND
B39	101	N/C
B40	102	~PERR
B41	103	+3.3V
B42	104	~SERR
B43	105	+3.3V
B44	106	~C/BE1
B45	107	AD14
B46	108	GND
B47	109	AD12
B48	110	AD10
B49	111	GND
B50	112	KEYWAY
B51	113	KEYWAY
B52	114	AD8
B53	115	AD7
B54	116	+3.3V
B55	117	AD5
B56	118	AD3
B57	119	GND
B58	120	AD1
B59	121	+5V
B60	122	N/C
B61	123	+5V
B62	124	+5V

NOTE: All 3.3 V pins are connected to the same decoupling capacitor. These pins are not otherwise connected on the PCISC3.

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3.9 IP Module Logic Bus Connector Pinout

Table 3-6 shows the pin assignments for each IP Module Logic Bus connector. The signals on the left side of the table are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. The upper case "X" in the Systran signal name represents the "A", "B", "C", "D" or "E" mnemonic for any of the five IP Module slots for all pertinent control signals.

Table 3-6 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names	Bussed or Unique	P = Pulled Up Via 10 kΩ Resistor
GND	50	GND	GND	GND
Reserved	49	RESERVED1	U	P
Ack*	48	$\overline{\text{ACK_X}}$	U	P
A6	47	IPA6	B	
Strobe*	46	$\overline{\text{STROBE_X}}$	U	P
A5	45	IPA5	B	
Intreq1*	44	$\overline{\text{INTREQ_X1}}$	U	P
A4	43	IPA4	B	
Intreq0*	42	$\overline{\text{INTREQ_X0}}$	U	P
A3	41	IPA3	B	
Error*	40	$\overline{\text{ERROR_X}}$	U	P
A2	39	IPA2	B	
DMAEnd*	38	$\overline{\text{DMAEND_X}}$	U	P
A1	37	IPA1	B	
Reserved	36	RESERVED2	U	P
IOSel*	35	$\overline{\text{IOSEL_X}}$	U	
DMAck0*	34	$\overline{\text{DMACK_X}}$	U	P
IntSel*	33	$\overline{\text{INTSEL_X}}$	U	
DMAReq1	32	$\overline{\text{DMAREQ_X1}}$	U	P
MemSel*	31	$\overline{\text{MEMSEL_X}}$	U	
DMAReq0	30	$\overline{\text{DMAREQ_X0}}$	U	P
IDSel*	29	$\overline{\text{IDSEL_X}}$	U	
R/W*	28	R/W_X	B	
+5V	27	+5VDC	+5 Vdc	+5 Vdc
GND	26	GND	GND	GND
GND	25	GND	GND	GND
+5V	24	+5VDC	+5 Vdc	+5 Vdc
+12V	23	+12VDC	+12 Vdc	+12 Vdc
-12V	22	-12VDC	-12 Vdc	-12 Vdc
BS1*	21	$\overline{\text{BS_X1}}$	B	
BS0*	20	$\overline{\text{BS_X0}}$	B	
D15	19	DATA_X15	B	P

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Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names	Bussed or Unique	P = Pulled Up Via 10 kΩ Resistor
D14	18	DATA_X14	B	P
D13	17	DATA_X13	B	P
D12	16	DATA_X12	B	P
D11	15	DATA_X11	B	P
D10	14	DATA_X10	B	P
D9	13	DATA_X9	B	P
D8	12	DATA_X8	B	P
D7	11	DATA_X7	B	P
D6	10	DATA_X6	B	P
D5	9	DATA_X5	B	P
D4	8	DATA_X4	B	P
D3	7	DATA_X3	B	P
D2	6	DATA_X2	B	P
D1	5	DATA_X1	B	P
D0	4	DATA_X0	B	P
Reset*	3	$\overline{\text{RESET_X}}$	U	
CLK	2	ICLK_X	B	
GND	1	GND	GND	GND



NOTE: The IP Module data bus, usually defined as IPD[15:0] for all of our IP Modules, is a subset of the information that appears on these signal lines. Since carrier register information also uses these signal lines, the bus was defined as the "PCISC5 Local Data Bus" designated as DATA_X[15:0].

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APPENDIX A

SPECIFICATIONS

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A.1 Specifications

MECHANICAL

Measurements	13.344 inches x 4.200 inches, 33.894 cm x 10.668 cm
Weight	7.9 oz, 223.96 grams
Board thickness	0.062 inches, 0.157 cm, nominally, (8 layers)

POWER-UP DEFAULT CONDITION

No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS

Power (No IPs installed):	+5 Vdc (±5%)	@	260 mA
	+12 Vdc	@	24 mA
	-12 Vdc	@	22 mA



NOTE: The PCI bus ground and IP Module ground are not isolated through this board.

PERFORMANCE CHARACTERISTICS

Electrical Characteristics	Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS

Supply voltage with respect to ground:	Minimum	Maximum
+0.5 Vdc	-0.5 Vdc	+7.0 Vdc
+12.0 Vdc	Dependent on the IP Modules installed	
-12.0 Vdc	Dependent on the IP Modules installed	

RECOMMENDED OPERATING CONDITIONS:

Supply voltage with respect to ground	+4.75 Vdc to +5.25 Vdc
Logic Interface	ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating)	0°C to +70°C
Temperature (no bias, storage)	-40°C to +85°C
Humidity (Non-condensing)	5% to 95%
Vibration (Operating)	10 G's RMS (10→55 Hz)
Shock (Operating)	50 G's maximum
Altitude (Operating)	10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MIL-HDBK-217F	225,290 hours
Bellcore 332, Issue 6	630,519 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

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APPENDIX B

PROGRAMMING GUIDE

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B.1 Overview

This section of the manual describes the operation of the PCISC5 from the software perspective, detailing the PCISC5 registers and the overall mapping and addressing scheme for the board, and provides programming examples. A more detailed description of the hardware can be found in chapter 2, PRODUCT OVERVIEW, chapter 3 INSTALLATION, and application concepts are discussed in Appendix D, TYPICAL APPLICATIONS.

B.2 Description

The PCISC5 is an easy-to-use PCI slave card that holds five singlewide, three singlewide and one doublewide, or one singlewide and two doublewide IP Modules. In addition to providing access to the I/O and ID space of the IP Modules via the PCI Bus, the PCISC5 has ten locations to perform interrupt acknowledge cycles on the IP Modules, and four on-board control/status registers.

B.3 PCI Configuration Space

The PCISC5, like all PCI-compliant devices, contains an address space specifically devoted to device identification, as well as memory and I/O configuration. For a comprehensive listing of the configuration register space contents, see the information presented in Table D-1.

B.4 Board Base Address

The PCISC5 uses 128 MB of PCI memory space for I/O, I/D, control/status registers, and memory space. By default, all of the 128 MB of local bus address space are accessible by the host via PCI memory space in a single aperture. Other configurations are possible. Contact Systran for information regarding additional setups for memory space other than those mentioned in Appendix E, PCICFG UTILITY FOR PCI-BASED CARRIERS.

B.5 Address Map

The IP Module I/O and ID, and the carrier's control, status, and general-purpose registers, reside at a fixed relative address from the PCISC5 base address.

Table B-1 shows the complete memory map for the board.

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Table B-1 PCISC5 Address Map

Address Space or Register Name	Local Address (relative to board base address)	Size
IP Module A I/O	Base + 0x000	128 bytes*
IP Module A ID	Base + 0x100	128 bytes*
IP Module B I/O	Base + 0x200	128 bytes*
IP Module B ID	Base + 0x300	128 bytes*
IP Module C I/O	Base + 0x400	128 bytes*
IP Module C ID	Base + 0x500	128 bytes*
IP Module D I/O	Base + 0x600	128 bytes*
IP Module D ID	Base + 0x700	128 bytes*
IP Module E I/O	Base + 0x800	128 bytes*
IP Module E ID	Base + 0x900	128 bytes*
IP Module Reset Register	Base + 0xA00	5 bits
Error Status Register	Base + 0xA04	5 bits
Carrier Control Register	Base + 0xA08	4 bits
IP Module A IRQ0 Register	Base + 0xB00	8 bits
IP Module A IRQ1 Register	Base + 0xB04	8 bits
IP Module B IRQ0 Register	Base + 0xB08	8 bits
IP Module B IRQ1 Register	Base + 0xB0C	8 bits
IP Module C IRQ0 Register	Base + 0xB10	8 bits
IP Module C IRQ1 Register	Base + 0xB14	8 bits
IP Module D IRQ0 Register	Base + 0xB18	8 bits
IP Module D IRQ1 Register	Base + 0xB1C	8 bits
IP Module E IRQ0 Register	Base + 0xB20	8 bits
IP Module E IRQ1 Register	Base + 0xB24	8 bits
Interrupt Steering Register	Base + 0xB28	11 bits
IP Module A Memory Base	Base + 0x100 0000	8 MB*
IP Module B Memory Base	Base + 0x200 0000	8 MB*
IP Module C Memory Base	Base + 0x300 0000	8 MB*
IP Module D Memory Base	Base + 0x400 0000	8 MB*
IP Module E Memory Base	Base + 0x500 0000	8 MB*

* This denotes the actual number of bytes used by the respective address space. For each 32-bit memory location, only the lower 16 bits are actually used. The PCISC5 and any installed IP Modules are typically accessed via 8-bit or 16-bit operations. If 32-bit operations are used, the upper 16 bits should be discarded by software.

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B.6 Register Descriptions

The PCISC5 registers can be accessed as byte (8-bit) or word (16-bit) values. The unused bits are driven as 0's on reads. All unused bits are discarded on writes. The hexadecimal addresses for the registers shown below are relative to the board base address and are in the WORD format for word and byte accesses, respectively.

B.7 Word Access Address Translation

The following table shows the relationship between PCI space addresses and the IP Module address for word accesses. In the table, BASE represents the I/O, ID, and memory base address. All addresses are in hexadecimal.



NOTE: By default, the PCI_BASE0 aperture's byte swapping is disabled by the appropriate bits in the PCI_MAP0 register. If these bits are changed to implement byte swapping in the PCI interface, the following table will no longer be correct.

Table B-2 Word Access Address Translation Table

PCI bus Address	IP Module Address
BASE + 0x00	IPA = 0x00
BASE + 0x04	IPA = 0x01
BASE + 0x08	IPA = 0x02
BASE + 0x0C	IPA = 0x03
BASE + 0x10	IPA = 0x04
BASE + 0x14	IPA = 0x05
BASE + 0x18	IPA = 0x06
BASE + 0x1C	IPA = 0x07
BASE + 0x20	IPA = 0x08
BASE + 0x24	IPA = 0x09
BASE + 0x28	IPA = 0x0A
…	…
BASE + 0xFC	IPA = 0x3F

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B.8 Byte Access Address Translation

The following table shows the relationship between PCI space addresses and the IP Module address for byte accesses. In the table, BASE represents the I/O, ID, and memory base address. All addresses are in hexadecimal.



NOTE: By default, the PCI_BASE0 aperture's byte swapping is disabled by the appropriate bits in the PCI_MAP0 register. If these bits are changed to implement byte swapping in the PCI interface, the following table will no longer be correct.

Table B-3 Byte Access Address Translation Table

PCI bus Address	IP Module Address	Byte Lane*
BASE + 0x00	IPA = 0x00	0
BASE + 0x01	IPA = 0x00	1
BASE + 0x04	IPA = 0x01	0
BASE + 0x05	IPA = 0x01	1
BASE + 0x08	IPA = 0x02	0
BASE + 0x09	IPA = 0x02	1
BASE + 0x0C	IPA = 0x03	0
BASE + 0x0D	IPA = 0x03	1
BASE + 0x10	IPA = 0x04	0
BASE + 0x11	IPA = 0x04	1
…	…	…
BASE + 0xFC	IPA = 0x3F	0
BASE + 0xFD	IPA = 0x3F	1

* Byte-lane 1 not applicable for ID Space

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B.8.1 Reset Register (0xA00)

Setting one of the bits RES_E through RES_A to '1' asserts the corresponding IP Module's reset line. The bits can be set individually by writing a '1' to that bit or simultaneously with a single write of '0x1F'. When set, a one-shot is triggered supplying a minimum 200 ms reset pulse as required by the IP Module specification. When read, these bits return the status of the corresponding IP Module's reset line (a '0' means the IP Module is not being reset, a '1' means it is in a reset condition).

Table B-4 Reset Register Bit Description

Bit #	B15-B5	B4	B3	B2	B1	B0
Bit Name	Not Used	RES_E	RES_D	RES_C	RES_B	RES_A
R/W	Reads '0's Writes discarded	R/W	R/W	R/W	R/W	R/W
Power-up State	N/A	0	0	0	0	0

NOTE: RES_E – RES_A: Reset bits for IP Module slots E to A.

B.8.2 Error Status Register (0xA04)

These bits indicate the state of the corresponding IP Module $\overline{\text{ERROR_X}}$ signal (pin #40 on a given IP Module). If the $\overline{\text{ERROR_X}}$ signal is asserted (active low) for a particular IP Module, then the corresponding ERR_X bit will be set to a '1'. If the error signal is not asserted, then the corresponding bit will be cleared.

Table B-5 Error Status Register Bit Description

Bit #	B15-B5	B4	B3	B2	B1	B0
Bit Name	Not Used	ERR_E	ERR_D	ERR_C	ERR_B	ERR_A
R/W	Reads '0's Writes discarded	R	R	R	R	R
Power-up State	N/A	State of IP Module E ERR* Signal	State of IP Module D ERR* Signal	State of IP Module C ERR* Signal	State of IP Module B ERR* Signal	State of IP Module A ERR* Signal

NOTE: ERR_E – ERR_A: Error Status bits for IP Module slots E to A.

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B.8.3 Carrier Control Register (0xA08)

This register contains bits that are used to enable interrupts and implement the time-out function on the PCISC5. Table B-6 shows the bits in the Carrier Control register. A brief description of each bit follows.

- The IP_INT_EN bit must be set to '1' to enable IP Module interrupt requests to assert a PCI interrupt. This is necessary to prevent interrupts from occurring before the application software has installed an appropriate interrupt service routine.
- The TO_EN bit is used to enable the time-out function. When this bit is set to '1' and the time-out jumper J20 is in the enabled position(shunt removed), the carrier completes the local bus transaction after 30 IP Module clock cycles have elapsed from the start of an IP Module access. This time-out feature is used to prevent the local bus of the PCISC5 from "locking up" if an IP Module access fails.
- The TO_INT_EN bit is used in conjunction with the TO_EN bit to generate a PCI interrupt when a time-out occurs. When this bit is set to '1' and the time-out jumper J20 is in the enabled position (shunt removed), a PCI interrupt will be generated to alert the software that an IP Module access was unsuccessful.
- The TO_STAT bit indicates if a time-out occurred. This bit is set to a '0' when an IP Module access is successful and it is set to a '1' when a time-out occurs.

Table B-6 Carrier Control Register Bit Description

Bit #	B15-B4	B3	B2	B1	B0
Bit Name	Not Used	TO_STAT	TO_INT_EN	TO_EN	IP_INT_EN
R/W	Reads '0's Writes discarded	R	R/W	R/W	R/W
Power-up State	N/A	0	0	0	0



NOTE: If an IP Module that asserts more than 28 wait states is used, the time-out feature should not be enabled.

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B.8.4 Interrupt Vector Registers for IP Modules A through E (0xB00 through 0xB24)

The ten interrupt vector registers (two per IP Module) are 8-bit, read-only registers. When one of these registers is read, an appropriate interrupt acknowledge cycle is performed on the corresponding IP Module. These registers reflect the vector driven on the IP Module data bus during the appropriate interrupt acknowledge cycle. These registers are useful for IP Modules that have a ROAK (release on acknowledge) interrupt mechanism, as the PCI interrupt cycle is not vectored, unlike some other buses (for example, VME). This means a ROAK-type IP Module will need to use these registers to clear the interrupt source. Software for RORA (release on register access) IP Modules will typically not use these registers.

Table B-7 Interrupt Vector Registers

Address	Interrupt Vector Register	Address	Interrupt Vector Register
Base + 0xB00	IP Module 'A' Intreq0	Base + 0xB04	IP Module 'A' Intreq1
Base + 0xB08	IP Module 'B' Intreq0	Base + 0xB0C	IP Module 'B' Intreq1
Base + 0xB10	IP Module 'C' Intreq0	Base + 0xB14	IP Module 'C' Intreq1
Base + 0xB18	IP Module 'D' Intreq0	Base + 0xB1C	IP Module 'D' Intreq1
Base + 0xB20	IP Module 'E' Intreq0	Base + 0xB24	IP Module 'E' Intreq1

B.8.5 Interrupt Steering Register (0xB28)

The Interrupt Steering Register is an 11-bit register consisting of an interrupt-status bit for each of the two interrupt-request lines for all five IP Modules, and one local time-out status bit. This register is typically read in the Interrupt Service Routine to determine which interrupt source(s) is (are) being asserted. A table of the bits in the Interrupt Steering Register is shown below. A write to this register will clear a pending time-out-interrupt request.

Table B-8 Interrupt Steering Register

Bit #	B15-B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	TO_INT	IRQ 1 E	IRQ 0 E	IRQ 1 D	IRQ 0 D	IRQ 1 C	IRQ 0 C	IRQ 1 B	IRQ 0 B	IRQ 1 A	IRQ 0 A
R/W	Reads '0's Writes discarded	R/W	R	R	R	R	R	R	R	R	R	R
Power -up State	N/A	0	0	0	0	0	0	0	0	0	0	0

NOTE: Each bit will be a '1' when the corresponding interrupt is set.

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B.9 Programming Examples

The following examples illustrate how to program the PCISC5 to achieve various operational modes.

B.9.1 Reset Example

This example resets one, then all five IP Modules, and then monitors the reset signals to determine when they are de-asserted. Setting a bit in the reset register causes a one-shot to assert the corresponding IP Module reset signal (the one-shot asserts the reset signal for approximately 240 ms). The reset signal can then be monitored by reading the Reset register to determine when it is de-asserted.

- Write '0x01' to the Reset register. This resets the IP Module in slot A by asserting the IP Module A reset signal.

LOOP1:

- Read the Reset register.
- If bit 0 is set then go to LOOP1.
- Write '0x1F' to the Reset register. This resets all five IP Module by asserting their corresponding reset signals.

LOOP2:

- Read the Reset register.
- If any of bits [5:0] are set then go to LOOP2.

B.9.2 Interrupt Initialization Example

Interrupts in the PCI-based system are sensed by the platform at an active-low level with the PCI INA# interrupt-request line remaining at a logic-low until the system CPU has accessed any necessary registers and removed the interrupt source. On the PCISC5, interrupts are disabled at power-up and must remain disabled until the entire system is properly initialized. After this, IP Module interrupts and time-out interrupt can then be enabled by writing the appropriate bits to the Control Register on the PCISC5. The interrupt line from the PCISC5 (PCI INTA#) is asserted from any one of the eleven possible sources. Ten of the sources are from N_INTREQ0 and N_INTREQ1 from each of the five IP Modules and the eleventh source is from a time-out interrupt-status bit that is set in the IP Module interface controller. The status of these interrupt requests can be determined by a read of the Interrupt Steering Register on the PCISC5.

An example is given in Appendix D, TYPICAL APPLICATIONS.

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APPENDIC C

PERFORMANCE

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C.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Appendix A, SPECIFICATIONS.

C.2 State Timing Diagrams

The PCISC5 test configuration consisted of a typical IBM-type Personal Computer (hereafter referred to as a PC/AT), with a standard VGA monitor and keyboard. A Systran IP Module Logic Bus Extender board #BHAS-IPBE2 was used along with a 24-inch ribbon connector #BHAS-IPBEC24, and an IP Module Logic Bus Breakout Board #BHAS-IPBB. While the extender/breakout boards provided a means for connecting the IP Module bus signals, a Corelis PI-PCI64 extender board was used to connect most of the PCI bus signals. The waveforms that follow were printed from files created on an HP16500B logic analyzer and show all pertinent signals for the local side of the PCI bridge IC and for the IP Module bus. Note that the actual PCI bus signals are not shown in the diagrams since they are asynchronous to and totally decoupled from the local bus (33 MHz vs. 8 MHz) and since the PCI bus may issue an indeterminate number of retries for each local transaction. Figure C-1 is a diagram of the test setup.

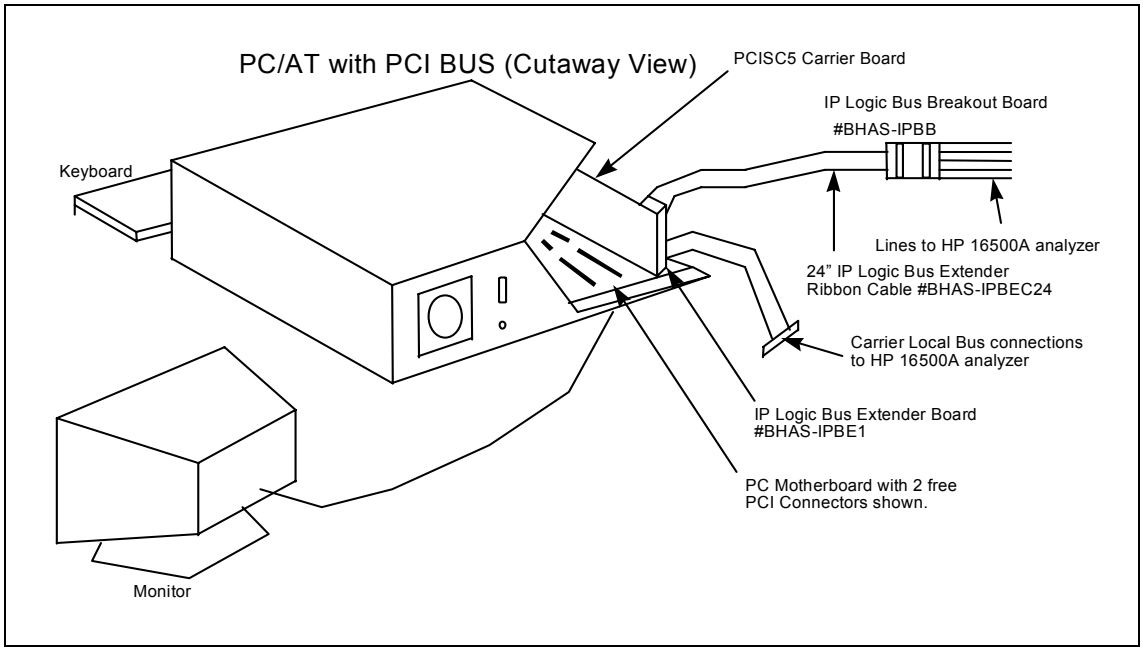


Figure C-1 Performance Test Equipment Configuration

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C.2.1 CSR Read Cycle

Figure C-2 shows the pertinent signals active during a typical read from the on-board CSRs for the PCISC5. During a read of the PCISC5 IP Reset register, the IP Module-specific control signals are all in their quiescent state while the PCI bridge local side bus signals will be active. Shown below is a 16-bit register read transaction from the reset register at location Base + 0xA00. Most of the action occurs toward the center portion of the diagram.

The transaction begins when the PCI master begins a transaction with a valid address and bus commands (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction to the CSR register. Note that the read/write control signal, W_NR is low indicating a read, and that both byte strobe BE0 and BE1 are active-low indicating a 16-bit transaction. After one internal wait state, the carrier's control circuits then assert an NREADY to the bridge circuit indicating that valid data is now available and that the transaction can be completed. The process from the assertion of NADS to the de-assertion of NREADY is about three local clock cycles or about 375 ns.

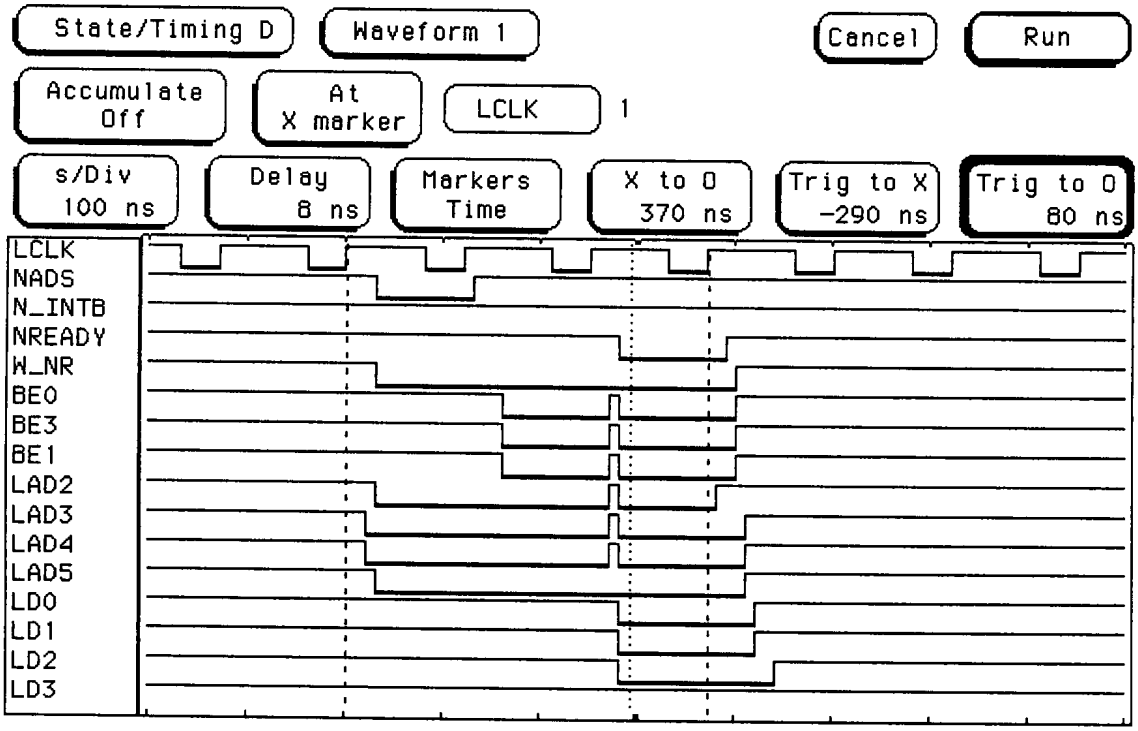


Figure C-2 CSR Read Cycle (IP Reset Register) at 0xA00

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C.2.2 CSR Write Cycle

Figure C-3 shows the pertinent signals active during a typical write to the on-board CSRs for the PCISC5. Shown below is an 8-bit register write transaction to the IP Reset Register at location Base + 0xA00. Most of the action occurs toward the center portion of the diagram.

The transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction to the CSR register. Note that the read/write control signal, W_NR is high indicating a write and that only byte strobe BE0 is active low indicating an 8-bit transaction. After one internal wait state, the carrier's control circuits then assert an NREADY to the bridge circuit indicating that valid data will now be received and that the transaction can be completed. The process from the assertion of NADS to the de-assertion of NREADY is about three local clock cycles or about 375 ns.

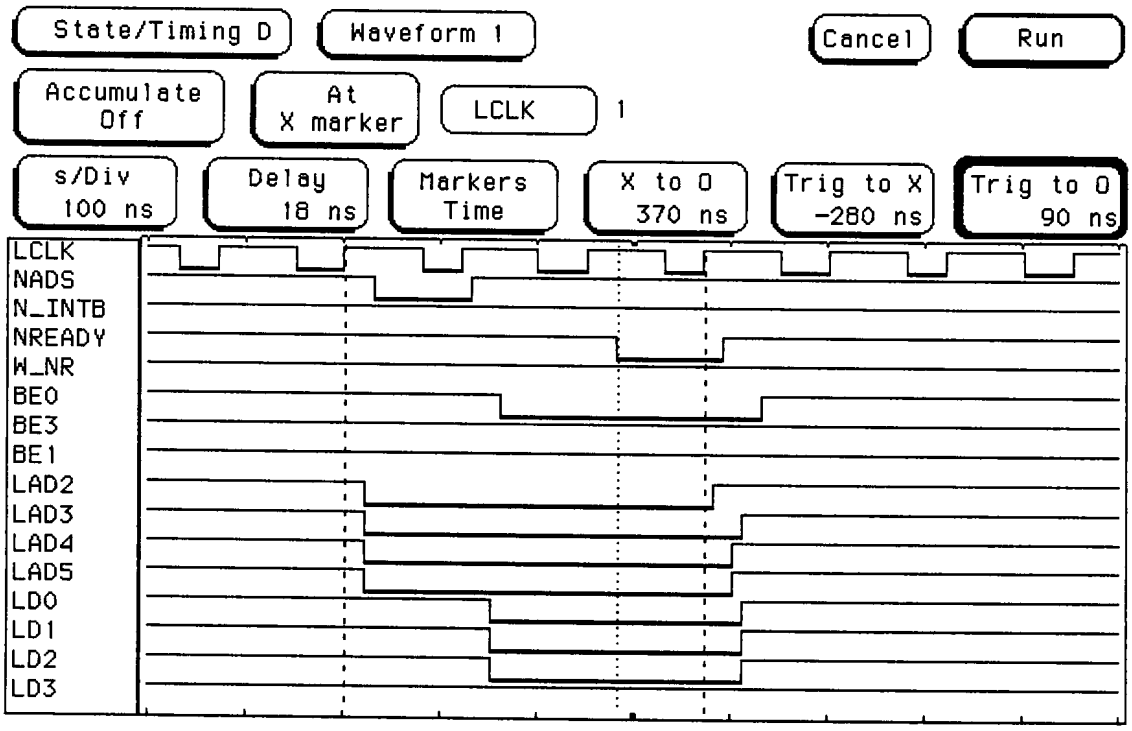


Figure C-3 CSR Write Cycle (IP Reset Register) at 0xA00

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C.2.3 I/O Write Cycle

Figure C-4 shows the pertinent signals that are active during a write to the I/O space on each of the five IP Modules on the PCISC5. Unlike CSR transactions, both the PCI bridge local side signals and the IP Module-specific signals are active during this type of transaction. An I/O write transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 will then assert a local address strobe, NADS, which begins the transaction. After a one-clock delay to allow the byte strobes from the bridge circuit to become valid, the IP interface control circuitry asserts an IOSEL to the selected IP Module along with valid data and byte strobes in less than 40 ns. The IP bus read/write signal shown, R_N_W, is also valid within 40 ns of the local clock and is low in this case for a write. The IP Module in this case asserts no-wait states such that N_ACK is returned to the PCISC5 on the next clock cycle and the transaction ends with an immediate assertion of NREADY (N_RDY on the diagram) to the PCI bridge circuit.

From the beginning to end of the local-to-IP Module transaction, four clock cycles occur. This equates to about 500 ns. The actual latency on the PCI bus will be somewhat longer since one or more retries may be forced by the PCI bridge IC on the PCISC5. Note that the PCISC5 asserts no hold states on any transaction to any IP Module.

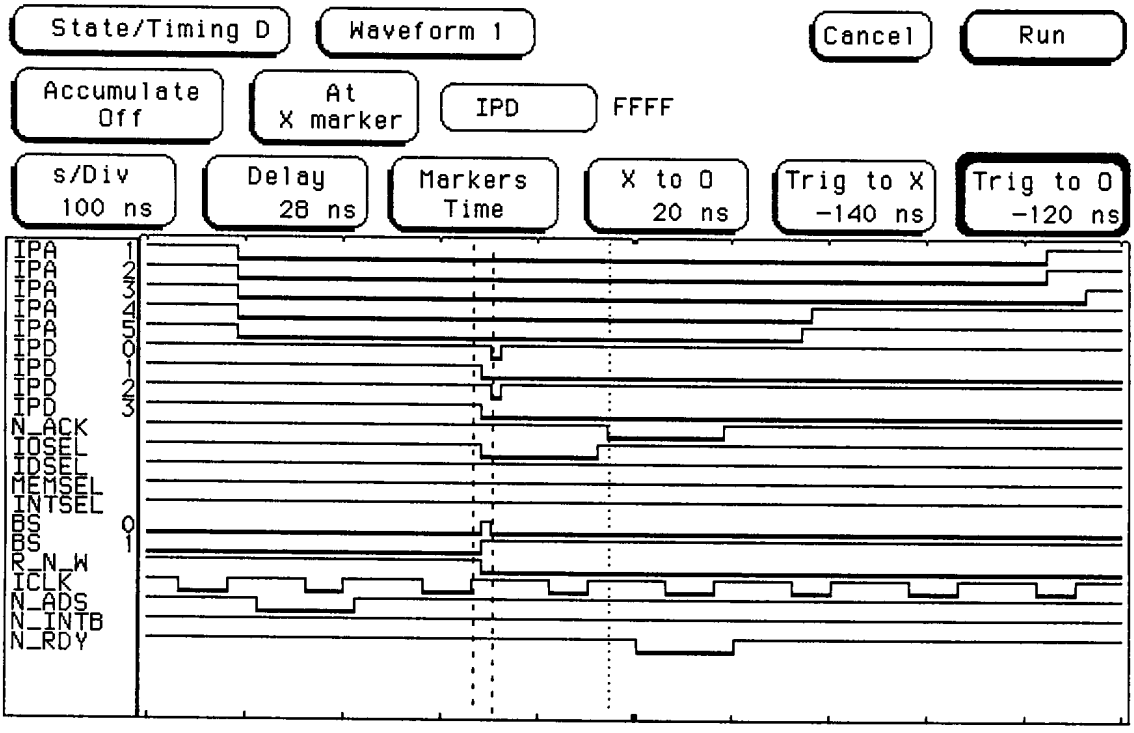


Figure C-4 I/O Write Cycle No-wait States

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C.2.4 I/O Read Cycle

Figure C-5 shows the pertinent signals that are active during a read from the I/O space on each of the five IP Modules on the PCISC5. Unlike CSR transactions, both the PCI bridge local side signals and the IP Module-specific signals are active during this type of transaction. An I/O read transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction. After a one-clock delay to allow the byte strobes from the bridge circuit to become valid, the IP interface control circuitry asserts an IOSEL to the selected IP Module along with valid byte strobes in less than 40 ns. The IP bus read/write signal shown, R_N_W, is also valid within 40 ns of the local clock and is high in this case for a read. The IP Module in this case asserts no-wait states such that N_ACK is returned to the PCISC5 on the next clock cycle and the transaction ends with an immediate assertion of NREADY (N_RDY on the diagram) to the PCI bridge circuit.

From the beginning to end of the local-to-IP Module transaction, four clock cycles occur. This equates to about 500 ns. The actual latency on the PCI bus will be somewhat longer since one or more retries may be forced by the PCI bridge IC on the PCISC5.

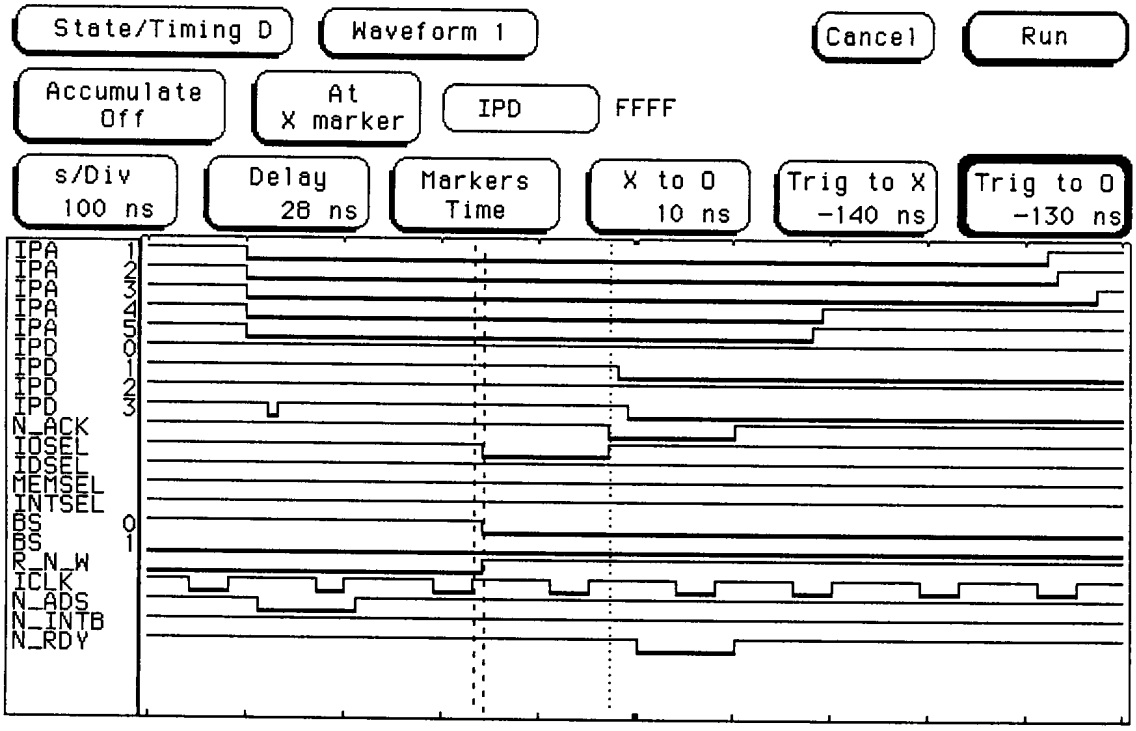


Figure C-5 I/O Read Cycle No-wait States

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C.2.5 ID Read Cycle

Figure C-6 shows the pertinent signals that are active during a read from the ID space on each of the six IP Modules on the PCISC5. Unlike CSR transactions, both the PCI bridge local side signals and the IP Module-specific signals are active during this type of transaction. An ID read transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction. After a one-clock delay to allow the byte strobes from the bridge circuit to become valid, the IP interface control circuitry asserts an IDSEL to the selected IP Module along with valid byte strobes in less than 40 ns. The IP bus read/write signal shown, R_N_W, is also valid within 40 ns of the local clock and is high in this case for a read. The IP Module in this case asserts no-wait states such that N_ACK is returned to the PCISC5 on the next clock cycle and the transaction ends with an immediate assertion of NREADY (N_RDY on the diagram) to the PCI bridge circuit.

From the beginning to end of the local-to-IP Module transaction, four clock cycles occur. This equates to about 500 ns. The actual latency on the PCI bus will be somewhat longer since one or more retries may be forced on the PCISC5 by the PCI bridge IC

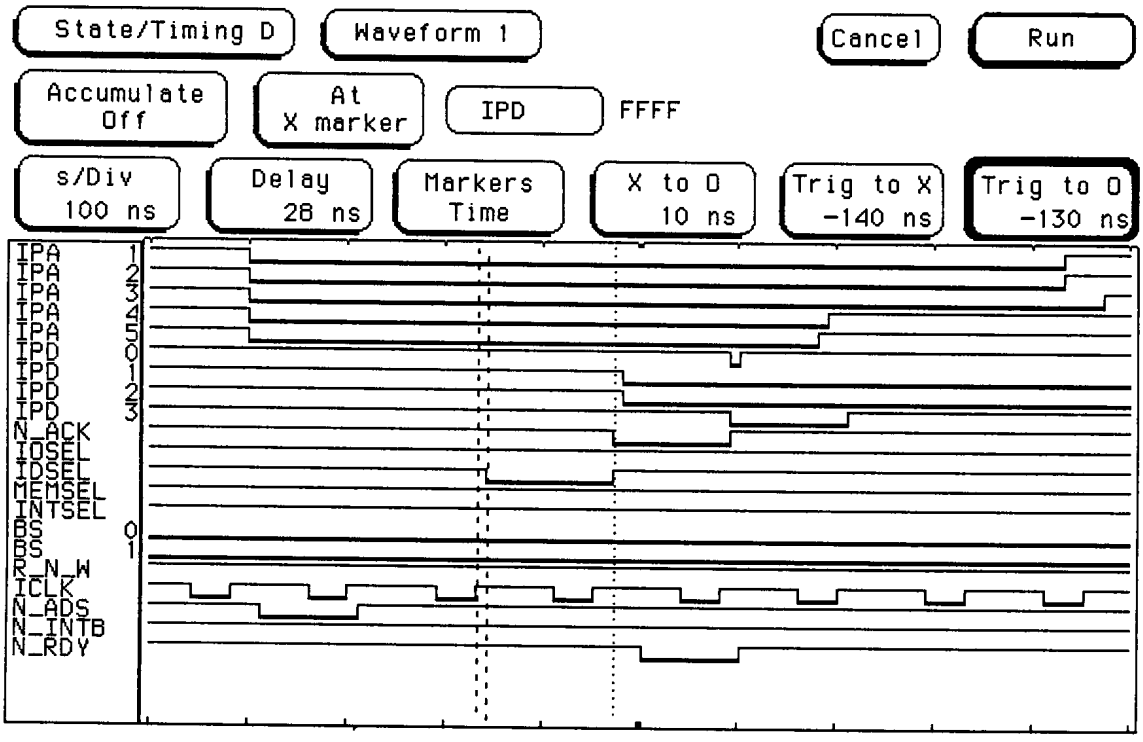


Figure C-6 ID Space Read Cycle With No-wait States

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C.2.6 ID Write Cycle

Figure C-7 shows the pertinent signals that are active during a write to the ID space on each of the six IP Modules on the PCISC5. Unlike CSR transactions, both the PCI bridge local side signals and the IP Module specific signals are active during this type of transaction. An ID write transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction. After a one-clock delay to allow the byte strobes from the bridge circuit to become valid, the IP interface control circuitry asserts an IDSEL to the selected IP Module along with valid data and byte strobes in less than 40 ns. The IP bus read/write signal shown, R_N_W, is also valid within 40 ns of the local clock and is low in this case for a write. The IP Module in this case asserts two wait states such that N_ACK is returned to the PCISC5 on the third clock cycle following the select cycle when the transaction ends with an immediate assertion of NREADY (N_RDY on the diagram) to the PCI bridge circuit.

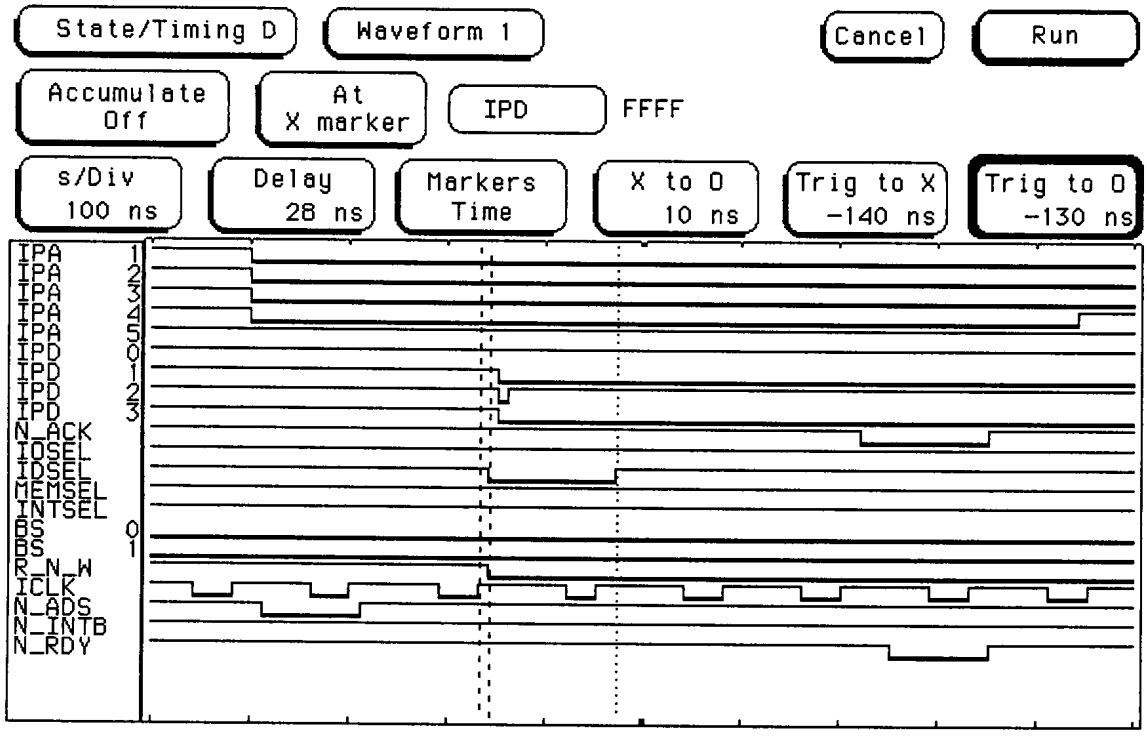


Figure C-7 ID Space Write Cycle With Two IP Wait States

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C.2.7 Memory Write Cycle

Figure C-8 shows the pertinent signals that are active during a write to the IP memory space on each of the five IP Modules on the PCISC5. Unlike CSR transactions, both the PCI bridge local side signals and the IP Module-specific signals are active during this type of transaction.

A memory write transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction. After a one-clock delay to allow the byte strobes from the bridge circuit to become valid, the IP interface control circuitry asserts a MEMSEL to the selected IP Module along with valid data and byte strobes in less than 40 ns. The IP bus read/write signal shown, R_N_W, is also valid within 40 ns of the local clock and is low in this case for a write. The IP Module in this case asserts no-wait states such that N_ACK is returned to the PCISC5 on the next clock cycle and the transaction ends with an immediate assertion of NREADY (N_RDY on the diagram) to the PCI bridge circuit.

From the beginning to end of the local-to-IP Module transaction, four clock cycles occur or about 500 ns. The actual latency on the PCI bus will be somewhat longer since one or more retries may be forced on the PCISC5 by the PCI bridge IC.

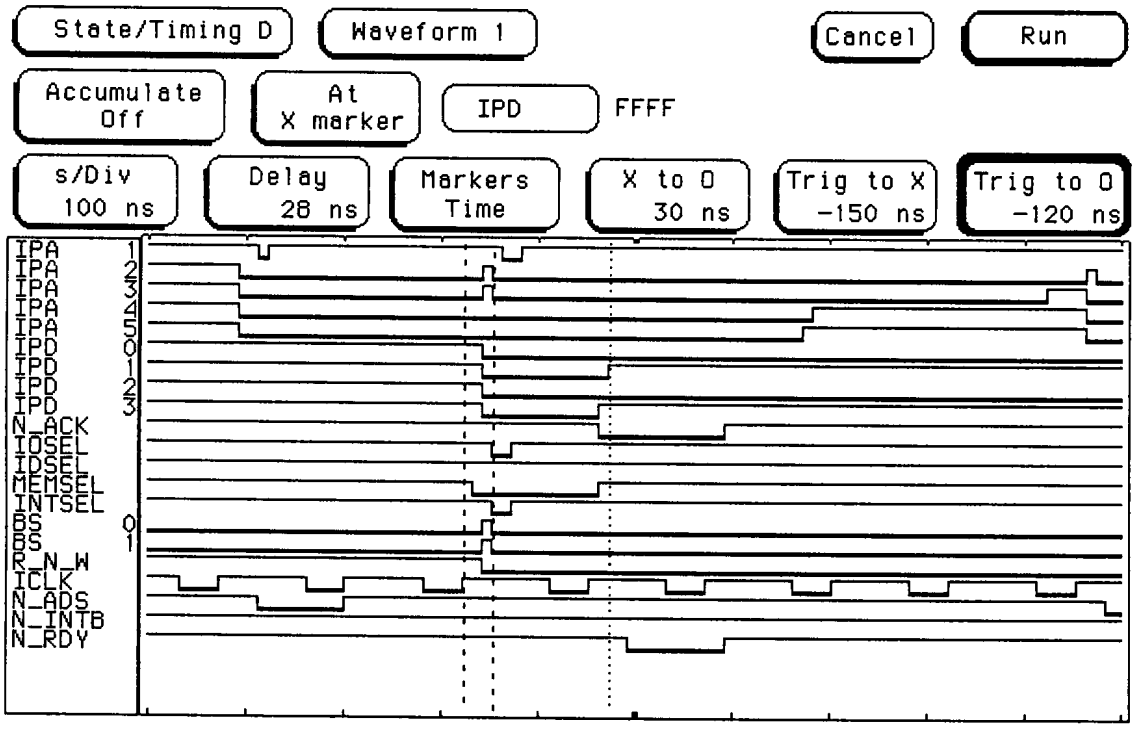


Figure C-8 Memory Write Cycle With No-wait States

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C.2.8 Memory Read Cycle

Figure C-9 shows the pertinent signals that are active during a read of the IP memory space on each of the five IP Modules on the PCISC5. Unlike CSR transactions, both the PCI bridge local side signals and the IP Module-specific signals are active during this type of transaction.

A memory read transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction. After a one-clock delay to allow the byte strobes from the bridge circuit to become valid, the IP interface control circuitry asserts a MEMSEL to the selected IP Module along with valid byte strobes in less than 40 ns. The IP bus read/write signal shown, R_N_W, is also valid within 40 ns of the local clock and is high in this case for a read. The IP Module in this case asserts no-wait states such that N_ACK is returned to the PCISC5 on the next clock cycle and the transaction ends with an immediate assertion of NREADY (N_RDY on the diagram) to the PCI bridge circuit.

From the beginning to end of the local-to-IP Module transaction, four clock cycles occur. This equates to about 500 ns. The actual latency on the PCI bus will be somewhat longer since one or more retries may be forced on the PCISC5 by the PCI bridge IC.

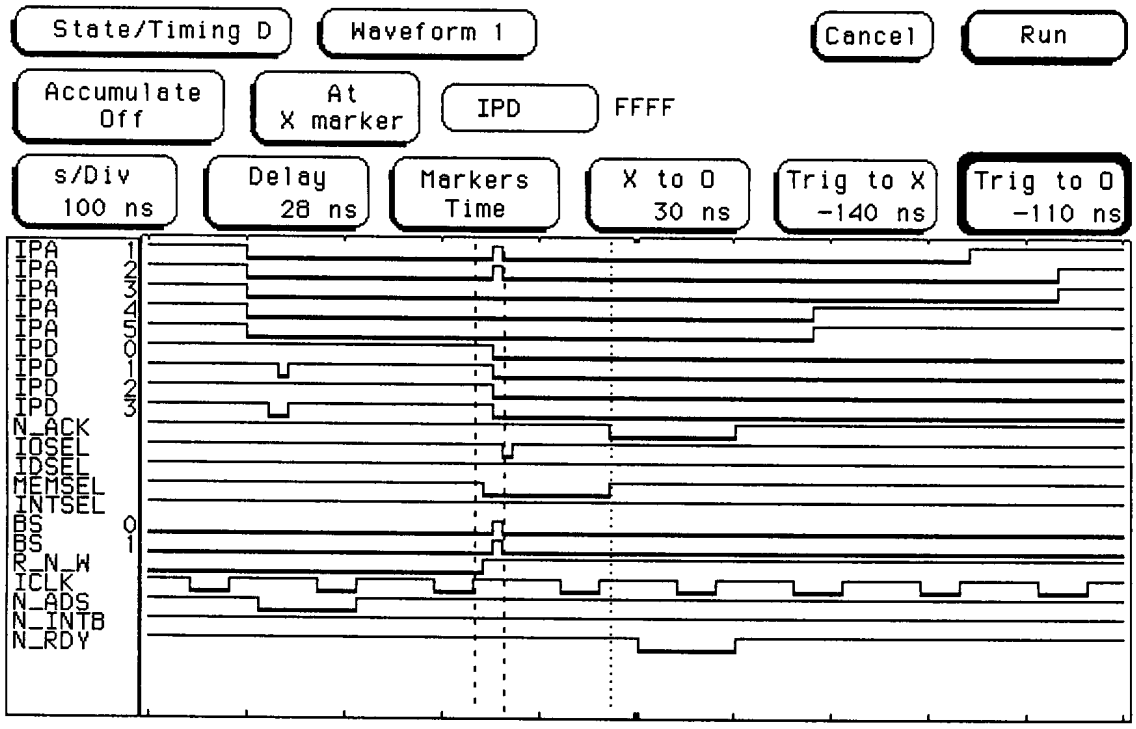


Figure C-9 Memory Read Cycle With No-wait States

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C.2.9 Interrupt Request/Time-out

Figure C-10 shows an attempted read of an IP memory space on one of the IP Modules on the PCISC5 where the read is to a non-existent memory location. This causes the IP Module to ignore the transaction and not generate a N_ACK. With the Time-out disable jumper off of J20 and bit one of the Carrier Control Register set, the time-out circuitry in the IP interface controller generates an NREADY (N_RDY) after a maximum number of wait states as follows:

The attempted memory read transaction begins when the PCI master begins a transaction with a valid address and bus command (not shown). The PCI bridge circuit on the PCISC5 then asserts a local address strobe, NADS, which begins the transaction. After a one-clock delay to allow the byte strobes from the bridge circuit to become valid, the IP interface control circuitry asserts a MEMSEL to the selected IP Module along with valid byte strobes. The IP bus read/write signal shown, R_N_W, also becomes valid and is high in this case for a read. The IP Module in this case does not respond with a N_ACK. The internal timer then allows 30 clock cycles to occur before asserting an N_READY (N_RDY on the diagram) to release the PCI bridge local bus. In addition, if the time-out interrupt enable bit (bit two in the Carrier Control Register) is set, a time-out condition will immediately cause an assertion of N_INTB to the PCI bridge circuit, which will then assert an interrupt to the PCI bus to indicate an error has occurred

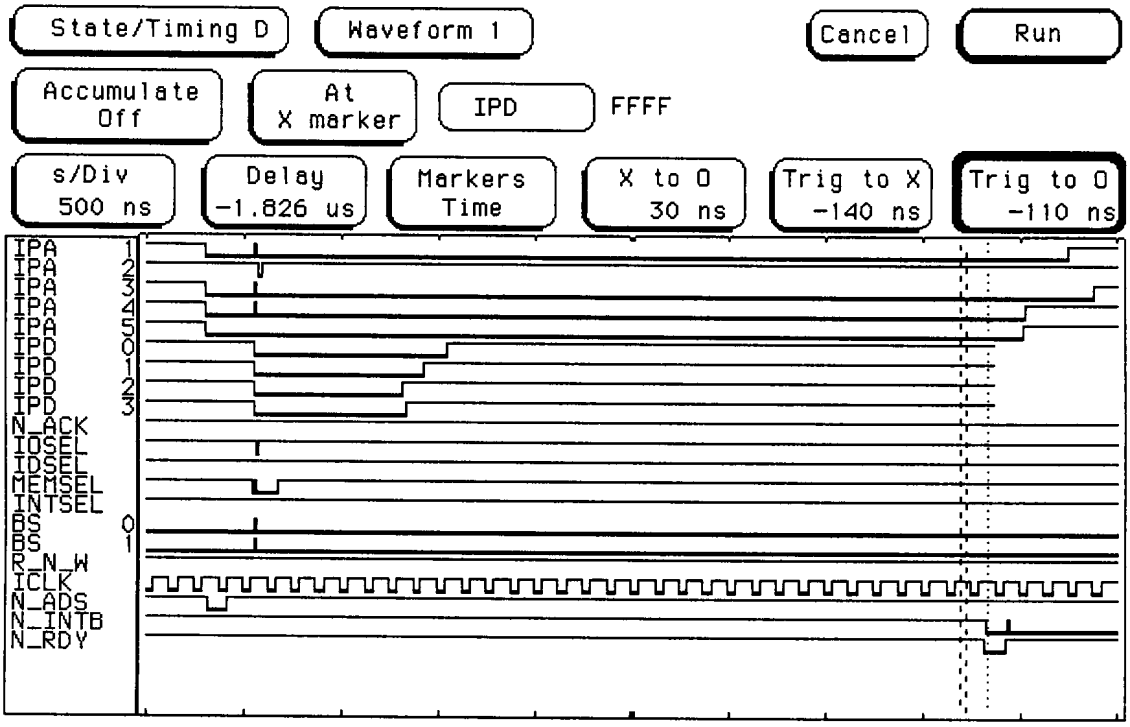


Figure C-10 Interrupt Request Generation on IP Module Time-out

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APPENDIX D

TYPICAL APPLICATIONS

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D.1 Applications

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the PCISC5 Slave Carrier to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas. Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

D.2 Typical Software Considerations in PC Environments

The use of the PCISC5 may initially appear complex due to the many options provided by the PCI-interface chip QuickLogic 962PBC-B2 (hereafter referred to as "PBC") on the PCISC5. Fortunately, most of the registers are initialized by the on-board EEPROM and/or the system BIOS and are consequently transparent to the user. Typically, the only PBC registers used by user software are the following: PCI_IO_BASE, PCI_BASE0, PCI_BPARAM, and PCI_INT_STAT. The following examples discuss how these registers may be used to access the PCISC5 and handle interrupts appropriately. This description is generic and does not specifically discuss operating system-specific implementation issues.

1. Verify that a PCI compliant BIOS is present on the system board.
2. Verify that at least one PCISC5 is present in the system. The Device ID and Vendor ID are typically used for this purpose. For each PCISC5 card found in the system, perform steps 3-5.
3. Perform a 32-bit read of the PCI_IO_BASE register. The result obtained by masking off the lower 8 bits (AND with 0xFFFFFF00) of this value is the base address used to access the PBC's internal registers. For this discussion, this address will be designated **PCISC5_Config_Pointer**. This base address should be used for all subsequent accesses to the PBC.
4. Perform a 32-bit read of the PCI_BASE0 register (**PCISC5_Config_Pointer** + 0x14). The result obtained by masking off the lower 8 bits of this value is the base address used to access the PCISC5 registers and the IP Modules (see Appendix B for the entire address map). For this discussion, this address will be designated **PCISC5_IP_Space_Pointer**. This base address should be used for all subsequent accesses to the IP Modules or the PCISC5's registers.
5. Perform a 32-bit read of the PCI_BPARAM register (**PCISC5_Config_Pointer** + 0x3C). The lower 8 bits of this value denote the interrupt line that will be used by the PCISC5 during interrupts. For an x86-based computer, a valid interrupt line will be in the range 0 though 15. Use this value when installing an Interrupt Service Routine because the system has been configured to generate this level of interrupt to the microprocessor when the PCISC5 asserts its interrupt request.
6. IP Modules or PCISC5 internal registers can now be accessed as appropriate by using appropriate offsets from the board base address (**PCISC5_IP_Space_Pointer)**, as listed in Appendix B.

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NOTE: Steps 1 though 3 are platform and/or operating-system specific. For instance, BIOS calls (or higher-level API) may be used to perform steps 1-3. After the **PCISC5_Config_Pointer** is determined in step 3, do not continue to use BIOS calls to access the hardware because they must not be invoked from an Interrupt Service Routine



NOTE: Do not overwrite the values in the PCI_IO_BASE, PCI_BASE0, or PCI_BPARAM registers, as initialized by the BIOS. These values cannot be simply changed without having potential effects on the operability of the PCISC5 due to the "plug-and-play" nature of PCI.

D.3 Typical Interrupt Handling in a PC Environment

The previous example illustrated how to access the PCI interface chip's internal registers, the PCISC5's registers, and any installed IP Modules. This example will demonstrate how interrupts can be handled using the PCISC5.

- Upon initialization of program, save the current address of the currently installed Interrupt Service Routine (if any) for applicable interrupt line. The interrupt line used by the PCISC5 was determined in Step 5 of the previous example.
- Install the desired ISR for the appropriate interrupt line.
- Initialize the applicable programmable interrupt controller (8259A-type device)
- Enter the main loop of program here.
- During program's termination routine, restore the old ISR before exiting.

The following is a suggested ISR for the PCISC5:

- If applicable for ISR, set the programmable interrupt controller (PIC) to enable higher-priority interrupts to preempt this ISR.
- Read the steering register (**PCISC5_IP_Space_Pointer** + 0xB28) to verify that the interrupt was asserted from the PCISC5.
- If not, call the previous ISR at this interrupt line, if any, and exit.
- If one or more interrupts from the PCISC5, service appropriately.

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The following is a typical routine, which prioritizes the IP Module interrupt requests in the following order:

IP Module A Interrupt Request 0 through IP Module E Interrupt Request 1.

```
Read Steering Register
"AND" result with 0x7FF
if (non-zero)
       while result non-zero
              if (bit 0 set)
                     handle IPA - IRQ0
                     clear source
              else if (bit 1 set)
                     handle IPA - IRQ1
                     clear source
              .
              .
              .

              else if (bit 9 set)
                     handle IPE - IRQ 1
                     clear source
              reread the steering register and "AND" result with 0x7FF
       Perform 32-bit read of PCI_INT_STAT (PCISC5_Config_Pointer)
       Write this value back to PCI_INT_STAT to clear interrupt from PBC
       Issue "end-of-interrupt" command to PIC
else
       call previous ISR if exists
return from exception
```



NOTE: When processing of the interrupt(s) source(s) is complete, read the PCI_INT_STAT register and write this value immediately back to the register to clear the interrupt from the PCI interface chip. Disable the Compiler optimization to avoid removal of this code.

D.4 962PBC Register Map

As mentioned in previous sections, the PCI_IO_BASE, PCI_BASE0, PCI_BPARAM, and PCI_INT_STAT registers in the PBC Configuration space are necessary to access the PCISC5. Since the above registers represent a small subset of the entire PBC space, Table D-1 provides a complete listing of the PBC registers as initialized by the on-board EEPROM. For a more detailed description of each register, contact V3 Semiconductor at the address specified in section 1.4, Related Information.

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Table D-1 PBC Default Register Values

Name	Width	Offset	Value As Set by EEPROM
PCI_VENDOR	16 bits	0x00	0x1387
PCI_DEVICE	16 bits	0x02	0x4901
PCI_CMD	16 bits	0x04	0x0000
PCI_STAT	16 bits	0x06	0xF080
PCI_CC_REV	32 bits	0x08	0x08800000
PCI_HDR_CFG	32 bits	0x0C	0x00000000
PCI_IO_BASE	32 bits	0x10	0x00000000
PCI_BASE0	32 bits	0x14	0x00000000
PCI_BASE1	32 bits	0x18	0x00000000
PCI_SUB_VENDOR	16 bits	0x2C	0x0000
PCI_SUB_ID	16 bits	0x2E	0x0000
PCI_ROM	32 bits	0x30	0x00000000
PCI_BPARAM	32 bits	0x3C	0x00000100
PCI_MAP0	32 bits	0x40	0x00000073
PCI_MAP1	32 bits	0x44	0x00000070
PCI_INT_STAT	32 bits	0x48	0x00000000
PCI_INT_CFG	32 bits	0x4C	0x00020002
LB_BASE0	32 bits	0x54	0x00000060
LB_BASE1	32 bits	0x58	0x00000060
LB_MAP0	16 bits	0x5E	0x0006
LB_MAP1	16 bits	0x62	0x0006
LB_SIZE	32 bits	0x68	0x00000000
LB_IO_BASE	16 bits	0x6E	0x0000
FIFO_CFG	16 bits	0x70	0x0A00
FIFO_PRIORITY	16 bits	0x72	0x0F0F
FIFO_STAT	16 bits	0x74	0x0000
LB_ISTAT	8 bits	0x76	0x00
LB_IMASK	8 bits	0x77	0x00
SYSTEM	16 bits	0x78	0xC400

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APPENDIX E

PCICFG UTILITY FOR PCI-BASED CARRIERS

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E.1 Overview

PCs are continuing to become popular IP module carrier platforms. PCI is currently the primary PC local bus standard and is widely used as slots on a PC motherboard or as the CompactPCI form factor. One reason for such popularity is the "plug-and-play" nature of PCI-BIOS. However, the way PC BIOS systems map add-in card memory tends to differ from one system to another and in some cases can be problematic. Some add-in boards can be ignored or can cause a system to "hang" if they require a greater amount of memory to operate than the particular BIOS allows.

E.2 Purpose

The **PciCfg** utility allows quick and easy modification of the PCI configuration EEPROM. The modification entails an enable or disable of the memory space of the IP carrier. When memory space is disabled, only one megabyte of system space is required to place the carrier which allows proper operation in systems with a "memory sensitive" BIOS. However, if memory space is necessary, it can be enabled, which will require an additional 32 MB to 128 MB depending on which PCI-based carrier is in use.

E.3 Product Coverage

This software was designed for use with the following Systran PCI-based IP module carriers:

- BHAS-PCISC5
- BHAS-PCISC3
- BHAS-CPCISC4
- BHAS-CPCISC2



NOTE: This software is not intended for use with Systran's VME-based IP carriers or with any competitor's carrier.

E.3.1 OS Platform

This software operates under Windows NT 4.0. It was not designed to operate from another version of Windows or from DOS.

E.4 Hardware Installation

The **PciCfg** utility supports up to 16 installed IP Module carrier cards on a single machine. The cards to be configured are inserted into any available PCI or CPCI slots on the host system. Once the software is installed, cards may be inserted or removed and the software will automatically identify changes upon reboot.

It will also be necessary to install a jumper plug across the header connected to the write-protect-disable function on the carrier's EEPROM. The location of the jumper header for each carrier is listed below:

BHAS-PCISC5 ..... Install a plug across J17 located next to the EEPROM in the upper-left end of the board with the mounting bracket facing left.

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BHAS-PCISC3 ..... Install a plug across J9 located next to the EEPROM in the upper-right end of the board with the mounting bracket facing left.

BHAS-CPCISC4..... Install a plug across J3 located above the EEPROM in the lower-left end of the board with the panel and I/O connectors facing away.

BHAS-CPCISC2..... Install the plug across both pins on J3 located in the lower-right end of the board with the panel and I/O connectors facing away.



NOTE: The **PciCfg** program will be blocked from re-programming the EEPROM if the jumper is not properly installed.

E.5 Software Installation

The **PciCfg** utility is distributed on a standard 3.5" diskette. To install, insert the diskette into the host computer's removable-diskette drive. Select "Run" from the Windows NT "Start" menu and type the following in the Open edit box.

```
a:setup
```

The **PciCfg** installation utility will guide you through the setup process. Upon completion, the host system must be rebooted and PciCfg is then ready for operation.

E.6 Software Operation

To run **PciCfg**, select the appropriate icon in the **PciCfg** group of the Windows NT start menu. This brings up the main application window as shown in Figure E-1.

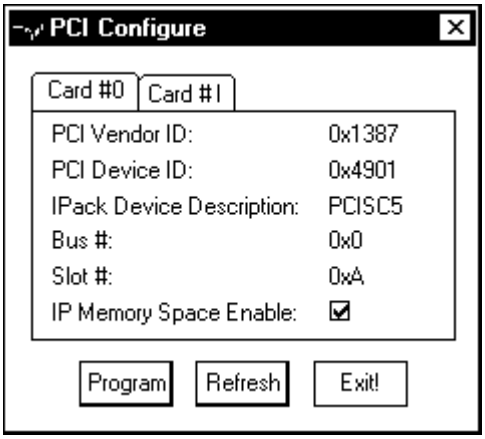


Figure E-1 Application Main Window

The main window displays the information for the first Systran IP Module carrier card found on the system. To display other devices installed on the system, simply select the appropriate "Card #" tab at the top of the window.

Various device characteristics are displayed for the selected card including PCI vendor and device ID, Systran IP Module model number as well as the PCI bus and slot numbers.

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In addition to the general PCI information, a selection checkbox is provided to turn off the IP Memory Space. To disable, de-select the checkbox and press the **Program** button. This reconfigures the PCI EEPROM on the selected device, effectively disabling the IP Memory Space. The host system must then be powered down and rebooted for the new settings to take effect.

The **Refresh** button on the main display window re-reads the selected devices EEPROM and refreshes the display. The **Exit** button closes **PciCfg**.

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GLOSSARY

Aperture ----------A region or set of addresses.

Byte-lane ----------Eight bits of a data bus on octal boundaries.

CSR ----------Control and Status Register.

Doublewide ----------An IP Module that is twice the size of the singlewide board.

EPLD ----------Erasable Programmable Logic Device.

IP Module----------Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP Module logic bus ----------A synchronous, 4 MTransfers/sec, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

ISR ----------Interrupt Service Routine

MTBF----------Mean Time Between Failures.

ns, µs, ms----------Nanoseconds, microseconds, and milliseconds, respectively.

Singlewide ----------An IP Module printed circuit board (3.9 inches by 1.8 inches). Each module has two 50-pin connectors.

VHDL----------Very high-speed integrated circuit Hardware Description Language.

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