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ISASC6

ISA Slave 6-slot IP Module Carrier
Hardware Reference

Document No. B-T-MR-ISASC6##-A-0-A4

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1. INTRODUCTION

1.1 How To Use This Manual

1.1.1 Purpose

This is a reference manual for the Systran ISASC6 ISA Slave 6-slot IP Module Carrier herein referred to as the ISASC6 board, part number BHAS-ISASC6.

1.1.2 Scope

This reference manual covers the physical and operational description of the ISASC6, both from hardware and software perspectives. This reference manual also contains detailed technical information about ISASC6 performance characteristics, and a few typical applications. A general understanding of computer processing, software and/or hardware applications experience; and a working knowledge of using IP Modules is necessary to effectively use this manual.

1.1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2              file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- *American National Standard for IP Modules (ANSI/VITA4 – 1995)* published by the VMEbus International Trade Association, 7825 Gelding Dr., Suite 104, Scottsdale, AZ 85260, Telephone: (602) 951-8866

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2. PRODUCT OVERVIEW

2.1 Overview

The Systran ISASC6 Slave 6-slot IP Module Carrier board (part number BHAS-ISASC6) is an ISA (PC/AT) slave add-in board that supports six singlewide IP Modules, three doublewide IP Modules, two doublewide and two singlewide, or one doublewide and four singlewide IP Modules. The ISASC6 supports 8 MHz IP Module transfers of ID, I/O, and Interrupt for all slots, and Memory on two slots. The ISASC6's ISA bus interface is a common ISA bus 8/16-bit add-in board interface (there is no real published ISA bus interface standard).

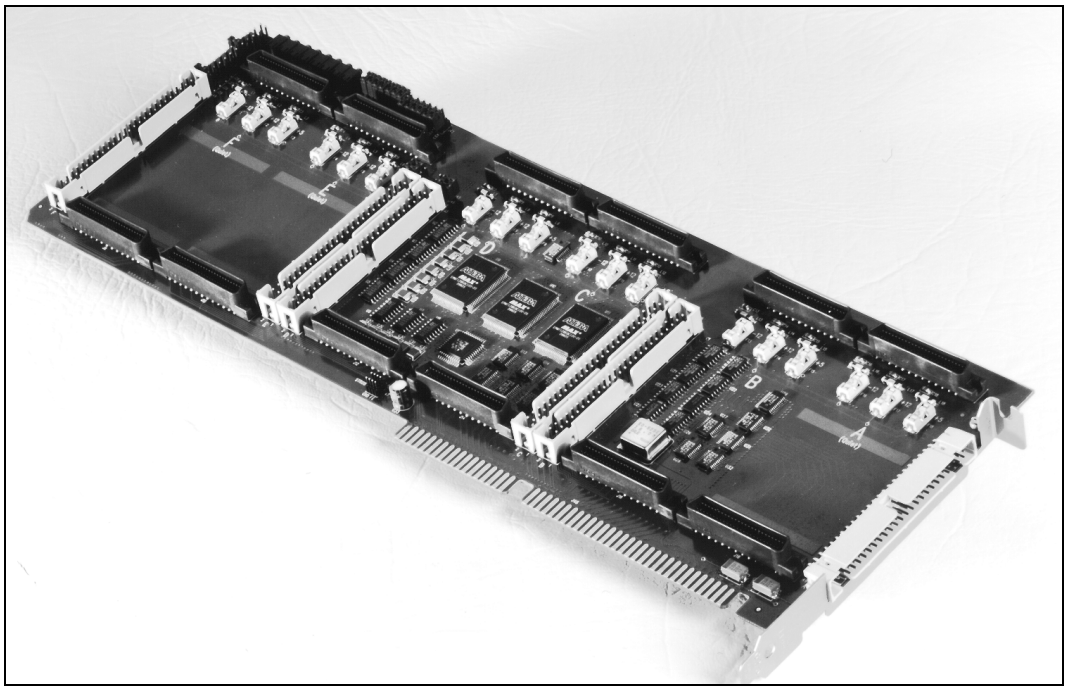


Figure 2-1 ISASC6 Board

The IP Module interface was developed using guidelines in the American National Standard for IP Modules (ANSI/VITA 4-1995) specification. For specific information regarding this specification, contact the VMEbus International Trade Association (VITA) as described in Section 1.2.

The ISASC6 encompasses a super-synchronous design that does not insert IP Module hold cycles. This guarantees the highest throughput possible for this ISA-to-IP bus-coupling carrier. The ISASC6 provides up to 300 I/O points (50 per IP Module) per ISA slot with the area under three of the IP Modules as a solid ground plane to provide "quiet" operating conditions for sensitive analog IP Modules. LEDs on the ISASC6 provide diagnostic information on accesses to the IP Modules, the ISASC6 local registers, and an IP Module acknowledgment signal. The ISASC6 has a very easy-to-use and flexible ISA-interrupt capability where the individual interrupts from each IP Module can be programmed to assert an available ISA interrupt-request signal.

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2.2 Features

- Up to 300 I/O points in a single, ISA (PC/AT) slot.
- I/O, ID, INT (on all slots), and MEM (on slots A and B) transfers with no HOLD cycles inserted.
- Precise and intuitive ISA memory map for easy access to IP Modules and local registers.
- Board base address jumper-selectable for I/O, ID and register.
- Supports six singlewide IP Modules, three doublewide IP Modules, or any combination.
- Each of 12 IP Module interrupt requests (two per IP Module slot) can individually assert ISA interrupt levels.
- Selectable ISA bus interface time-out.
- Can be mapped above 1 MB in ISA memory space on 2 KB boundaries with 8/16-bit even byte/word data transfers.
- IP memory can be mapped above 1 MB on boundaries of memory size.
- Independent field-replaceable fuses, and 'T'-type filters are used for the +5, +12, and -12 V power feeding each IP Module.
- Eight IP Module/Carrier Access and IP Module Acknowledge indicators (with pulse stretchers).
- Pure ground plane under three of six IP Modules (slots A, E and F) for "quiet" operation.
- IP slots A and B memory transfers are configured via memory size and base address registers for each slot.
- Resets individual IP Modules via software.
- Three 8-bit General-purpose registers.
- Posts IP Module error signals as status.
- Supports writes to ID space.
- Software-controlled resets to individual IP Modules.
- Six "standard" I/O ribbon cable connections.
- Supports six "strobe" connections (one per slot).



NOTE: The extended implementation of write-transfer capability over the full ID addressing space for this product is over and above that described in the specification.

2.3 Functional Description

2.3.1 Memory Mapping Scheme

The mapping scheme for the ID and I/O address spaces on all six IP Modules as well as the carrier's on-board CSRs are all made at fixed addresses relative to a jumper-selectable board base address. The IP Module address space is mapped into the uppermost region of the ISA 16 MB address space.

IP Module memory accesses are performed relative to base addresses set in the on-board CSR's. Memory size as well as base address is programmed into the CSRs. Section 3, INSTALLATION, and Appendix C, PROGRAMMING GUIDE, discuss the memory mapping in more detail.

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2.3.2 ID Transfers

IP Module ID transfers are supported as 8-bit or 16-bit ISA transfers. ID transfers are performed by a byte or word read/write operation of the slot IP Module ID address space from the ISA Bus. The ID PROM values are located every other byte at IP Module odd-byte locations (IP Module byte-lane 0). For word-reads the even byte is discarded. The ID PROM area allows read or write accesses to support future IP Modules requiring writes to the ID address space.

The IP Module data bus has been made big-endian to be compatible with VME. Since ISA is little endian, accesses to the IP Modules occur for ISA even addresses only. On ISA, the odd byte is the upper byte (D15 - D8) and the even byte is the lower byte (D0 - D7). For this reason, on 16-bit reads and writes, the IP Module odd byte is transferred on the ISA even byte, and the IP Module even byte is transferred on the ISA odd byte. Single-byte transfers are performed on ISA even addresses only and access the IP Module odd byte. Single-byte transfers to the IP Module even byte are not supported on this carrier.

2.3.3 I/O Transfers

IP Module I/O transfers are supported as 8-bit or 16-bit ISA transfers. I/O transfers are performed by a byte or word read or write operation of the slot IP Module I/O address space from the ISA Bus. IP Module even single-byte reads are not supported.

2.3.4 Interrupt Transfers

Interrupts are requested by the IP Module by assertion of N_INTREQ0 or N_INTREQ1. An independent ISA interrupter handles each of these IP Module-interrupt-request lines and asserts one of two prioritized ISA-interrupt-request lines. This provides a minimum delay in asserting the interrupt request to the platform CPU.

Selection of one of two available interrupt lines depends solely on the configuration of the board interrupt-select jumpers as outlined in Table 2-1. Both interrupt-request lines from IP Module A through IP Module C (a total of six) produce **Intq0** which feeds J45 and J46 while both requests from IP Modules D through F (a total of six) produce **Intq1** which feeds jumpers J43 and J44. These jumpers can be configured to allow either resulting request line access to ISA interrupt group IRQ8 – 15 or group IRQ1 – 7. Two separate batteries of jumpers allow configuration of the two **Intq** lines to select one ISA interrupt each from either group. This is demonstrated in Table 2-1.

Table 2-1 Interrupt Jumper Positions

Group Select Jumpers				(IP Modules A-C, both requests)	(IP Modules D-F, both requests)
J45	J46	J43	J44		
out	out	out	out	None	None
out	out	out	in	None	hi group
out	out	in	out	None	lo group
out	in	out	out	hi group	None
out	in	out	in	hi group	hi group
out	in	in	out	hi group	lo group
in	out	out	out	lo group	None
in	out	out	in	lo group	hi group
in	out	in	out	lo group	lo group

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Hi Group Jumper no. vs. Interrupt	Lo Group Jumper no. vs. Interrupt
J19 – IRQ15	J25 – IRQ7
J20 – IRQ14	J26 – IRQ6
J21 – IRQ12	J27 – IRQ5
J22 – IRQ11	J28 – IRQ4
J23 – IRQ10	J29 – IRQ3
J24 – IRQ 9	

EXAMPLE

To connect **Intreq1** from IP Module B to ISA interrupt line IRQ6, set the following jumpers "in":

- J45 to set IP Modules A through C to the Lo group, and
- J26 to select IRQ6 within the Lo group.



NOTE: While it is possible to set one IP Module range to both "hi" and "lo" group, it is not recommended if only one interrupt is selected.

2.3.5 Interrupt Configuration

The interrupt-select tiers in Figure 2-2 show the interrupt-select "flow" from the IP Modules to the ISA bus

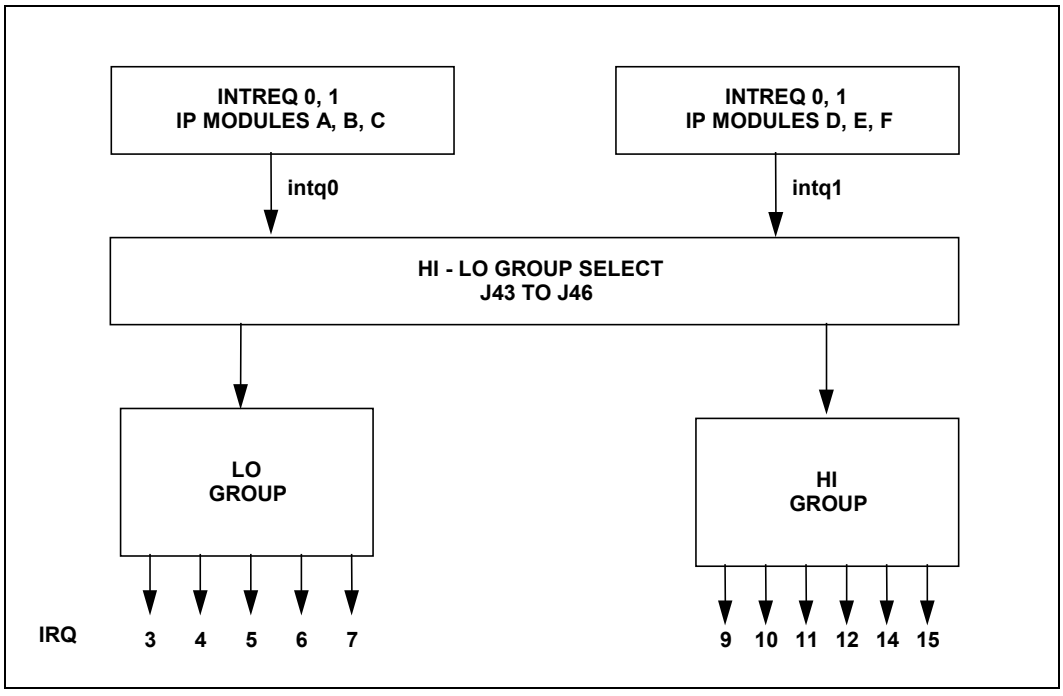


Figure 2-2 Interrupt-Select Tiers

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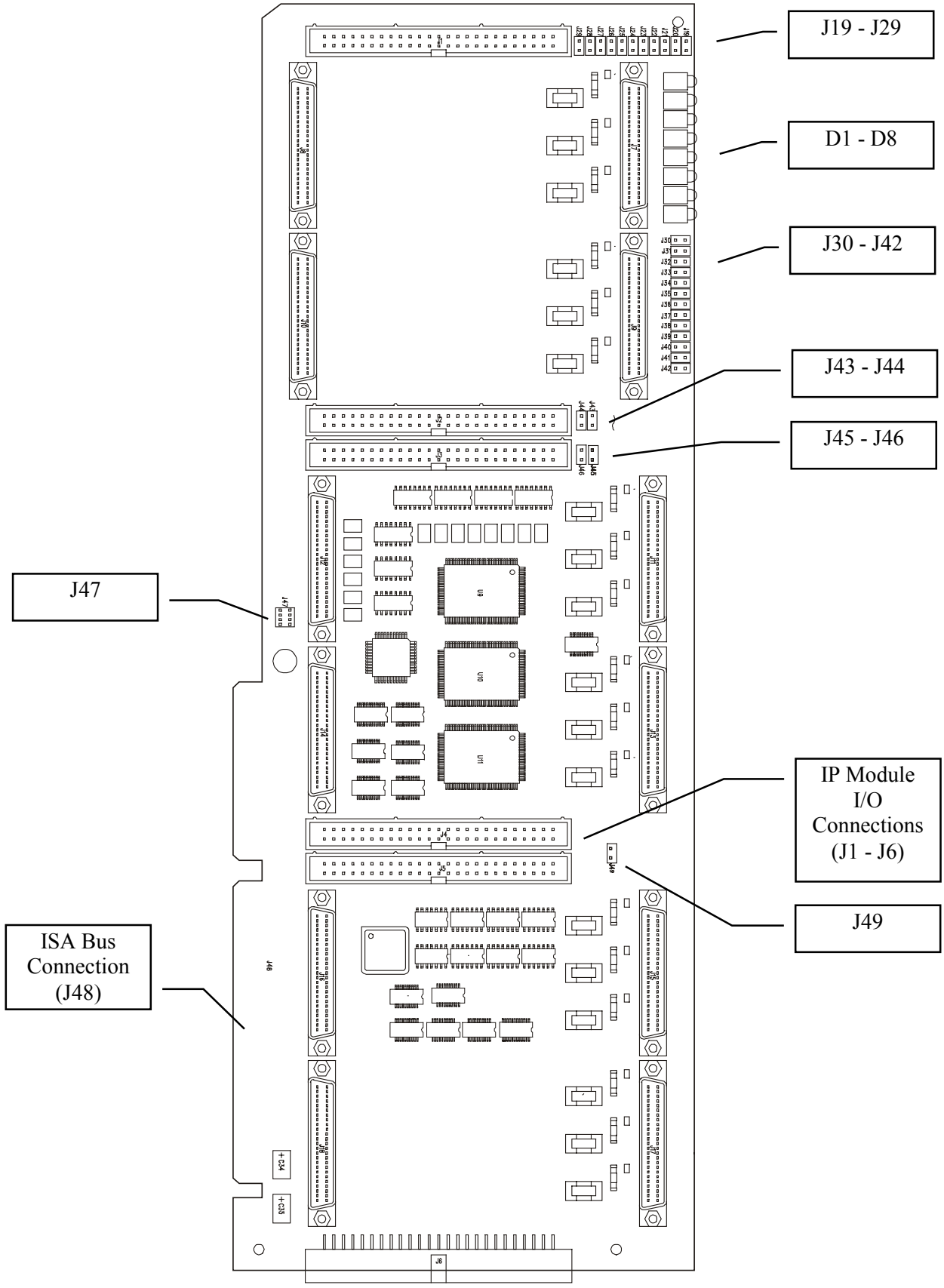


Figure 2-3 ISASC6 Mechanical Assembly

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2.3.6 General-Purpose Registers

There are three 8-bit, general-purpose, user-defined registers. For information about the addresses and format of these registers, see Section C.5.8.

2.3.7 Diagnostic LEDs

The ISASC6 has eight diagnostic LEDS (D1 - D8) as shown in Figure 2-3. Seven of the LEDs, labeled “A”, “B”, “C”, “D”, “E”, “F” and “CRA”, indicate when a read or write access is attempted to one of the six IP Module slots or the carrier registers. The eighth LED, labeled “ACK”, indicates an acknowledgment by the IP Module or the ISASC6 of the attempted access. This scheme provides independent verification of the access and the acknowledgment.

2.3.8 IP Module Reset

Independent or simultaneous resetting of the IP Modules is facilitated through writes to the Reset register. Monitoring of the pulse-stretched reset signals is made possible by reading the Reset register. See Appendix C, PROGRAMMING GUIDE, for a detailed description of this register.

2.3.9 Error Status

Monitoring of the IP Module ERROR signals is made possible by reading the Error Status register. See Appendix C, PROGRAMMING GUIDE, for a detailed description of this register.

2.3.10 Strobe Signals

The IP Module STROBE signals can be connected via an 8-pin header (J47).

2.3.11 Power Supply Filtering

Independent ‘T’-type filters are used for the +5 V, +12 V, and -12 V power feeding each IP Module. This arrangement, while costing a little more, provides superior power supply filtering.

2.3.12 Fuses

Independent field-replaceable fuses are used for the +5 V, +12 V, and -12 V power feeding each IP Module. Although this arrangement costs a little more, it provides superior short-circuit protection.



NOTE: Replacement fuses can be purchased directly from Littelfuse, Inc. Phone (708) 829-0400.

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2.4 Theory of Operation

2.4.1 Block Diagram Description

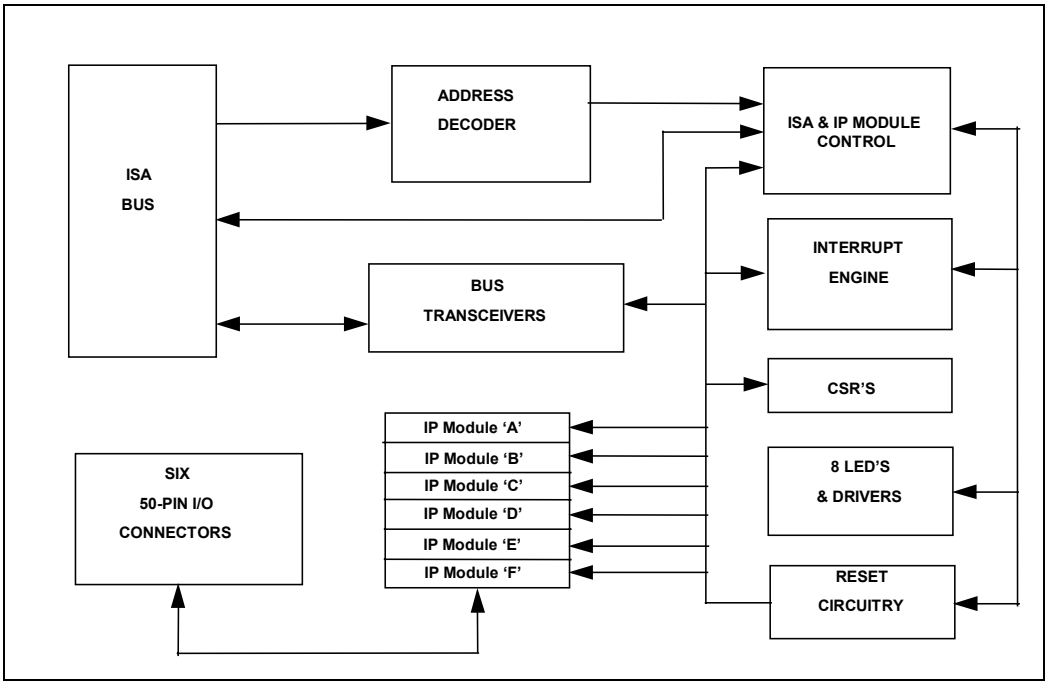


Figure 2-4 ISASC6 Block Diagram

Figure 2-4 is a simplified block diagram of the ISASC6 representing the signal flow between the ISA bus, IP Module Logic Bus and the IP Module I/O connectors. On the left side of the diagram is the ISA bus connector through which all transfers between the host computer and the ISASC6's registers or IP Modules are conducted. The ISA bus transfers do not insert any IP Module HOLD cycles into the accesses to the IP Modules.

The block labeled "ADDRESS DECODER" handles decoding of the ISA address. The block labeled "ISA & IP MODULE CONTROL" handles the transfer of data between the ISA and both the ISASC6 CSRs and the IP Modules.

2.4.2 Functional Logic Module Overview

The ISASC6 board has VHDL models divided into four functional blocks:

- The Data Transfer Engine (DTE) controls the flow of data from ISA to the IP Modules.
- The Board Address Mapper (BAM) determines whether a memory transaction is desired, or an IP Module or CSR access. This entity also informs the ISA bus that the carrier is capable of 16-bit transactions.
- The Interrupt Engine (INT) controls the flow of interrupts from the IP Modules to the ISA bus and provides mapping to the vector registers in the IP Modules as well as a steering register to ISA to indicate which line from which IP Module is causing the interrupt.
- The Reset Controller asserts software-controlled resets to the IP Modules as directed by the host as well as at power-up.

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2.4.2.1 ISA6DTE Module

DATA TRANSFER ENGINE (DTE)

The DTE handles the transfer of data between the ISA bus and the IP Modules. It monitors the HIT signals from the address decoders to determine when a transfer is to take place. The ISA control signals and address lines provide the rest of the transfer information. The DTE asserts the appropriate IP Module ID or I/O select line and executes an IP Module synchronous transfer. The DTE is implemented using combinational logic and four state machines. The state machines include:

- One for ISA Read cycles from the local control and status registers
- One for ISA Write cycles to the local control and status registers
- One for IP Module I/O and ID Read cycles
- One for IP Module I/O and ID Write cycles

Specifically, the IP Module Read-state machine will place the data on the ISA bus upon detection of the appropriate IP Module acknowledge signal N_ACK. The Write-state machine will latch the data from the ISA bus and then deassert N_IOCHRDY upon detection of the appropriate IP Module N_ACK signal.

This part is also responsible for controlling reads and writes to the memory space (up to 8 Megabytes) on both IP Module slots A and B. In addition, this part ensures that write data is "posted" from ISA to the IP Modules and that there is ample setup time for ISA on reads from the IP Modules.

REGISTERS

The DTE module also contains the General-purpose registers. See Appendix C, PROGRAMMING GUIDE, for a detailed description of these registers.

2.4.2.2 ISA6INT Module

ISA INTERRUPT ENGINE

This module detects any of twelve interrupt requests from six IP Modules and asserts them to the ISA interrupt select section of the board as follows: Interrupts 0 and 1 on IP Modules A through C are detected as **Intq0** while interrupts 0 and 1 on IP Modules D through F are detected as **Intq1**. These two board interrupts are then jumper-selected (see Table 2-1 and Figure 2-3) to cause two different ISA interrupts to occur. Use of either interrupt is optional and whether use of both is desired will depend on the applications for the individual IP Modules on the carrier. The contents of the interrupt steering register indicate if interrupts have been generated by any IP Modules on the ISASC6, reflecting the state of each IP Module's N_INTREQ0 and N_INTREQ1 signals. See section B.3 for details of an ISR.

When the host detects one of the selected interrupts, it reads the interrupt steering register in the ISA6INT module to determine which IP Module is causing an interrupt, as well as which interrupt is active on that particular IP Module. Once the exact source of the active interrupt is known, the host places the IP Module vector address out on the ISA bus for that particular request and reads the contents of the vector register. The ISA platform will normally handle the prioritization of interrupts should more than one occur.



NOTE: Choose the interrupts on the ISA bus with caution. Verify which interrupts are in use before selecting the lines for the ISASC6.

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2.4.2.3 ISA6BAM Module

ISA BOARD ADDRESS MAPPER

This module detects ISA host accesses to local ISASC6 Board Registers and IP Module I/O and ID spaces as well as accesses to IP Module "A" memory or IP Module "B" memory. An address-detect (HIT) signal corresponding to one of these address spaces is asserted when a matching address is detected.

This module detects the incoming ISA address bits from bit 23 down to bit 0 and performs all of the following:

1. Checks to ensure that bit 0 is low, indicating an access to an even location. Odd address accesses are not supported on this carrier.
2. For I/O, I/D and CSR accesses, the address mapper decodes the upper thirteen ISA address bits for a match to the jumper selects on the board. If there is a match, an N_BAMATCH signal is generated which is required for the transfer state machines to run.
3. For memory transactions, the address mapper compares the upper eight incoming address bits to the contents of the address size registers and base address registers and then generates N_MEMAMATCH or N_MEMBMATCH mattering on which enable bit is set in the memory enable register. These two memory-cycle enables are required for the state machines to run an IP Module memory cycle.

2.4.2.4 ISA6RST Module

RESET CONTROLLER

This module provides outputs to the reset pins on the IP Modules based on pulse-stretching one-shots which, in turn, provide synchronous, 200-millisecond (or more) resets to the six IP Modules. These resets occur on power-up, from the computer's reset button or from software control. Any one or more of the IP Modules can be reset from the software at any time.

This module also has a reset status register, which can provide diagnostic information should a reset line become "hung" (See paragraph C.5.1 for details).

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3. INSTALLATION

3.1 Unpack the ISASC6

Table 3-1 lists the contents of the ISASC6 shipping packages.

Table 3-1 Contents of ISASC6 Shipping Packages

Qty	Description
1	ISASC6 Printed Circuit Assembly
2	Surface mount spare fuses (one-1 Amp, one-2 Amp)
1	ISASC6 Hardware Reference*

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR-ISASC6).

3.2 Visually Inspect the ISASC6

Examine the ISASC6 to determine if any damage occurred during shipping.

3.3 Install the ISASC6



NOTE: The ISASC6 is an Electrostatic Sensitive Device (ESD). Install the ISASC6 on an anti-static workbench to protect the IP Modules and carrier board.

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The tools required for the ISASC6 installation are listed in Table 3-2.

Table 3-2 ISASC6 Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

3.3.1 Installation of IP Modules on the ISASC6

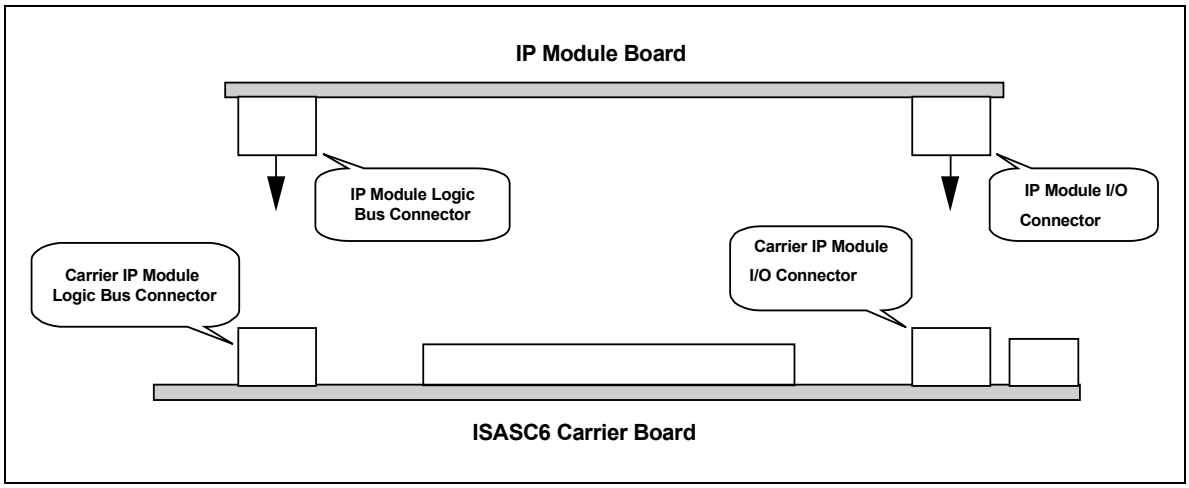


Figure 3-1 Installation of an IP Module on the ISASC6

Referring to the appropriate figures and table described below, perform the following steps in removing the ISASC6 from its shipping container (or from an existing installation) and installing IP Modules. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.

2a. Remove the ISASC6 from its shipping container and move it to the ESD-controlled area where the installation of the IP Module(s) can be made.

*2b. Remove the ISASC6 from the ISA bus connector and move it to the ESD-controlled area where the installation of the IP Module(s) can be made.

3. Set the ISA bus base address on the J30 - J42, jumpers (see Figure 3-2 and Figure 3-3). Set the interrupt group jumpers J43 - J46 and the ISA interrupt jumpers J19 - J29 to the desired settings (see Table 2-1 and Figure 3-4). Also, set the Time-out jumper J49 to its desired position (see Figure 3-2 and 3-4).

4. Install the IP Module(s) onto the carrier board by applying adequate and equal pressure to the IP Module(s) at both ends and the ISASC6 board.

*5. Install four M2x5mm flat head machine screws onto the IP Module's connectors.

*6. Install I/O cables necessary onto ISASC6.

7. Install the ISASC6 into desired ISA slot of a PC or ISA backplane.

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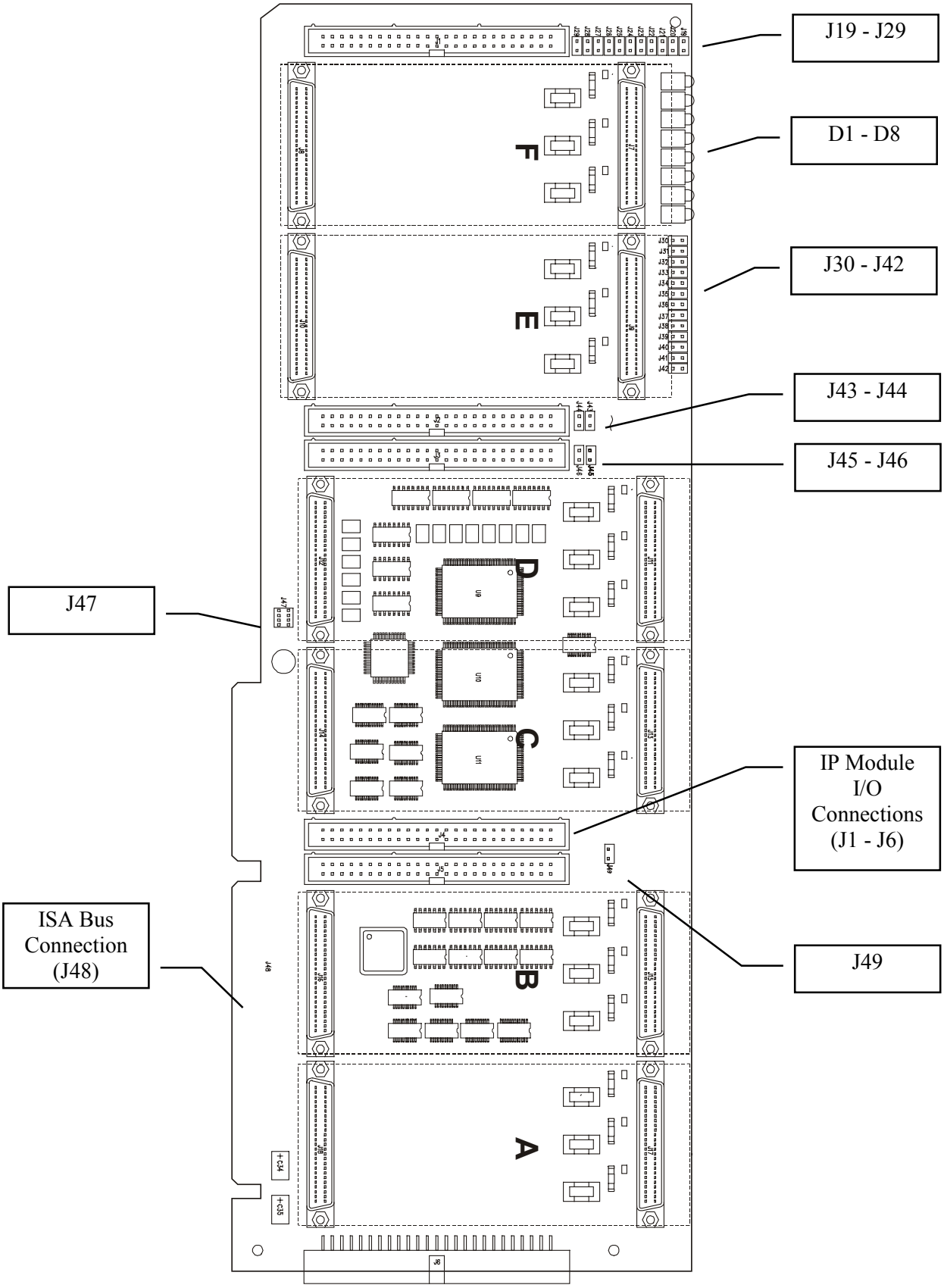


Figure 3-2 ISASC6 Mechanical Assembly

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3.3.2 ISASC6 ISA Base Address

The ISASC6 ISA board base address is set with thirteen jumpers J30 - J42, corresponding to ISA address bits A11 to A23, respectively. Refer to Figure 3-3 and Figure 3-4 for the placement of Jumpers J30 - J42 on the ISASC6.

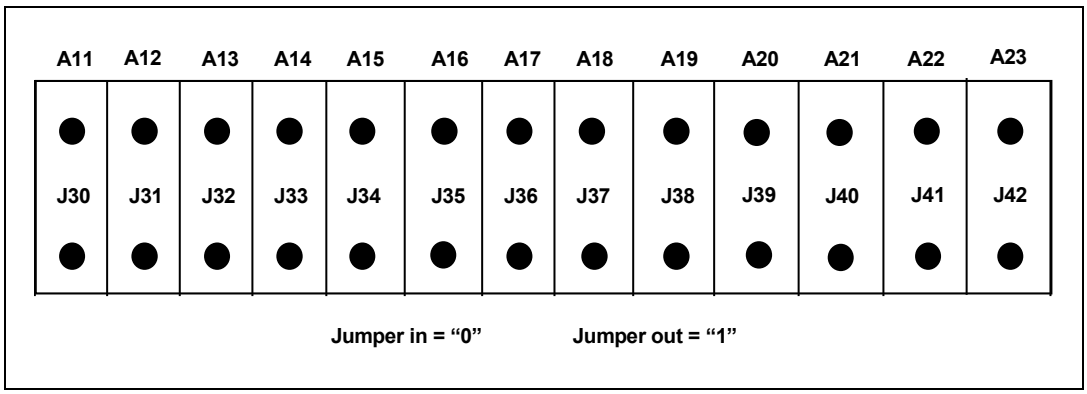


Figure 3-3 ISASC6 Jumpers J30 - J42

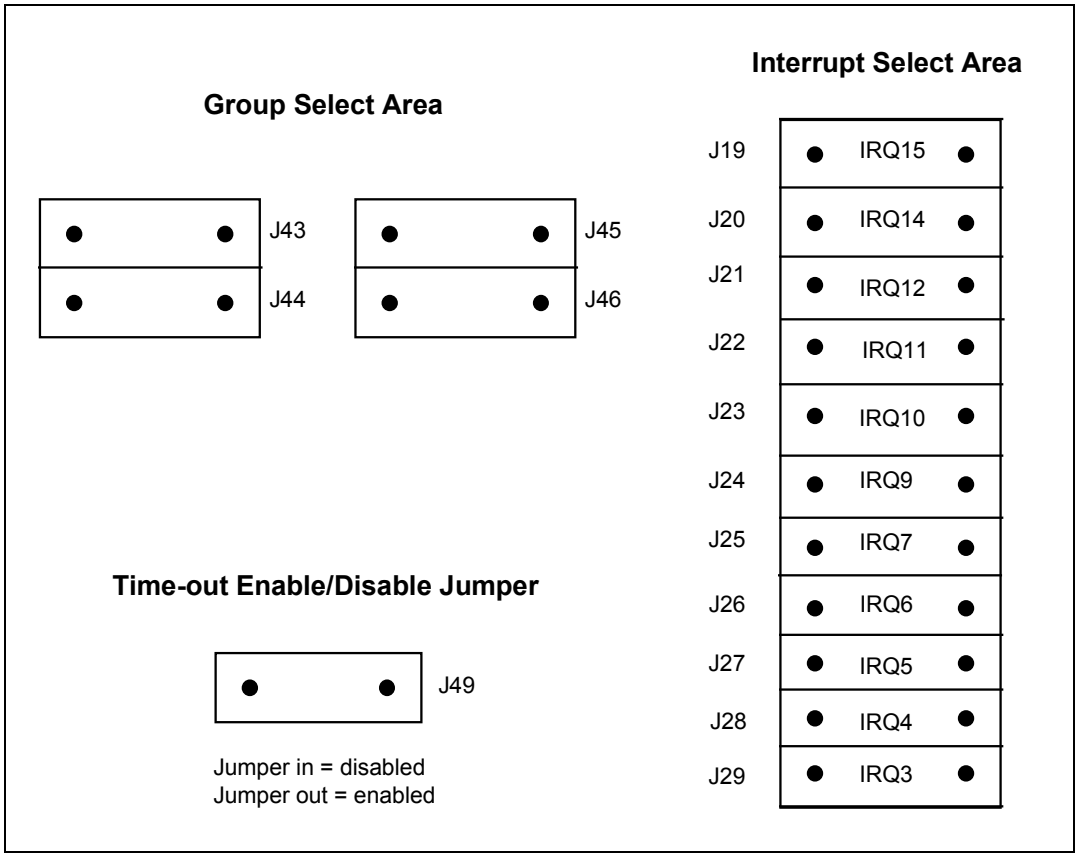


Figure 3-4 ISASC6 Interrupt Jumpers Group-Select and Interrupt-Select/Time-out Disable

Placing a jumper across both posts corresponds to a logic low, or "0", for that address bit. Removing the jumper, or storing it on a single post, corresponds to a logic high, or "1", for that address bit.

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NOTE: The mapped memory space on the standard PC is located from 0x000000 to 0xFFFFFF. In this case, if all jumpers were installed on the ISASC6, it would show up beginning at address 0x000XXX. If all jumpers except J42, corresponding to A23, were installed, the ISASC6 would show up at 0x800XXX.

Refer to Appendix C, PROGRAMMING GUIDE, for details of ISA accesses to the ISASC6 on-board registers or IP Modules.

The ISASC6 memory base addresses for IP Modules A and B are mapped into the ISA 16 megabyte memory space by the programming of CSRs as opposed to the setting of jumpers on the board. These CSRs are as follows:

- ISA Base + 0x702 = IP Module Memory A Size Register (7 bits)
- ISA Base + 0x704 = IP Module Memory A Base Address Register (8 bits)
- ISA Base + 0x706 = IP Module Memory B Size Register (7 bits)
- ISA Base + 0x708 = IP Module Memory B Base Address Register (8 bits)

For the Base Address Registers, the eight bits represent the uppermost bits (A23 down to A16) of the ISA address bus. This allows programming granularity for memory location down to 64 KB. The seven bits for the Memory Size Registers are filled with "ones" from the least-significant bit to the most-significant bit in order from smallest to largest memory size. The least-significant bit represents 64 KB while the most-significant represents 4 MB such that if someone wanted 1 MB configuration, they would set all bits lower than the 1 MB bit high or to "0001111" in binary (0x0F). With all seven size bits set high, the maximum size of 8 MB is specified.

PROGRAMMING EXAMPLE

Assume it is desired to configure the ISASC6 carrier to allow a 512 KB memory in IP Module slot A and a 2 MB memory in IP Module slot B and to give them separate apertures in the memory mapping space. The following values would be written into the configuration registers:

1. A 0x07 would be written to Base + 0x702 to configure IP Module memory A for 512 KB.
2. A 0x80 could be written to Base + 0x704 to place memory A at about the center of the ISA memory space.
3. A 0x1F would be written to Base + 0x706 to configure IP Module memory B for 2 MB.
4. A 0x90 could be written to Base + 0x708 to place memory B 1 MB above memory A. This would leave a 512 KB "gap" between them.

NOTE: Selected base addresses should be placed on boundaries according to the size of the memory. For instance, a 512 KB memory should be placed at 0x800000, 0x880000, 0x900000, etc. A 2 MB board could be placed at 0x800000, 0xA00000, 0xC00000, etc. Although this carrier will support IP Modules with 8 MB memory, their use could cause unpredictable results since ISA addresses in the range 0xFE0000 to 0xFFFFFF may also be used for BIOS EPROM.

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To "turn on" or execute a memory transfer, Base + 0x700 is then written with one of two codes:

- 0x01 to turn on IP Module memory for slot A
- 0x02 to turn on IP Module memory for slot B

To "turn off" the memory enables, write a 0x00 to Base + 0x700. A 0x03 can be written to this location to enable both memories provided that their programmed address windows do not overlap.

A memory transfer can then take place to any address within the specified window programmed into the above registers.



NOTE: To avoid conflicts on the ISA bus:

1. Do not program the memory-mapped IP Module space for I/O, I/D and interrupts below about 0x200000 or above 0xFC0000 since conflicts may occur with platform activities.
2. Do not program either memory space for IP Module A or IP Module B in the space occupied by address jumpers J30-J42 since this is reserved for IP Module I/O, I/D, interrupts and CSRs. The region defined by the board address jumpers is only 2 KB.
3. Ensure that no other boards inserted into the ISA backplane are memory-mapped into the selected areas for this IP carrier.

3.3.3 I/O Cables Installation

The ISASC6 provides easy access to each IP Module I/O connector by allowing a direct connect to the 50-pin flat header (J6) at the rear panel of the PC through the mount bracket while access for IP Module B through F headers can easily be provided for with ribbon connectors as described below.

Each ISASC6 IP Module I/O connector pin number directly corresponds to each IP Module I/O pinout (that is, a one-to-one relationship with pin 50 connected to pin 50 down to pin 1 connected to pin 1).

On the ISASC6:

- Connector J6 is for IP Module slot "A" and is facing the rear panel of the PC.
- Connector J5 is for IP Module slot "B" and is located between IP Modules B and C.
- Connector J4 is for IP Module slot "C" and is located next to J5.
- Connector J3 is for IP Module slot "D" and is located between IP Module slots D and E.
- Connector J2 is for IP Module slot "E" and is located next to J3.
- Connector J1 is for IP Module slot "F" and is located at the end of the board near IP Module F.

3.4 ISASC6 IP Module STROBE Connector

IP Module Logic Bus connector has a signal called "N_STROBE" and is user-defined by the IP Module Logic Bus Specification. On the ISASC6, each of the strobe signals is provided through J47 with the IP Module slot "A" strobe signal on pin #1 and slot "B" on pin #2 with "C" on pin #3, "D" on pin #4, "E" on pin #5, "F" on pin #6, and pins #7 and

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#8 grounded, as indicated in Table 3-3. Each of the strobe signals on the ISASC6 is pulled-up to +5 V via 10 KΩ resistors. The strobe connector (J47) is located at the center left of Figure 3-2 ISASC6 Assembly Drawing (which is at the bottom of the ISASC6 when installed).

Table 3-3 ISASC6 STROBE Connector Pin Assignments

Pin Number	Signal Name
1	N_STROBE_A
2	N_STROBE_B
3	N_STROBE_C
4	N_STROBE_D
5	N_STROBE_E
6	N_STROBE_F
7	GROUND
8	GROUND

Table 3-4 shows the pin assignments for the ISA Bus connector (J48).

Table 3-5 shows the pin assignments for each IP Module Logic Bus connector.

3.5 Time-out Jumper

Unlike the VME Bus, ISA does not provide a time-out function through the platform, whereby the bus master will allow a specified maximum number of wait states before terminating the transaction and freeing the bus. Consequently, there is a potential for a misaddressed, faulty or missing IP Module to hang the ISA Bus unless the carrier produces its own time-out to release the bus.

In other cases, you may not want the carrier to abort a transaction for diagnostic purposes or you may want to limit the number of IP Module of specified wait states. For this reason, the ISASC6 time-out feature is jumper-selectable (see Figure 3-4).

- With the time-out jumper (J49) in the 'out' (storage) position, the ISASC6 aborts any transaction to any of the six IP Modules after a maximum of 29 wait states or slightly less than four microseconds if the selected IP Module fails to assert an acknowledge. After this time has elapsed, the data returned to the ISA Bus will be 0xFFFF, which could be shown as erroneous data.
- With the jumper in the 'in' (shorted) position, the time-out feature is disabled which allows an indefinite period of time for IP Module wait states.



NOTE: The ISASC6 is shipped with time-out **enabled** (the shunt at J49 is not installed). Disabling the time-out is not recommended if a known faulty IP Module on the carrier will be accessed by software, or if a known potential address mismatch could occur to any IP Module. Fill the carrier with IP Modules, which can be properly accessed by system software before disabling the time-out feature.

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Table 3-4 ISA Bus Pin Assignments

ISA Bus P1/P2	Pin #	ISA Bus Signal
A1	1	N/C
A2	2	SD7
A3	3	SD6
A4	4	SD5
A5	5	SD4
A6	6	SD3
A7	7	SD2
A8	8	SD1
A9	9	SD0
A10	10	NI_IOCHRDY
A11	11	N/C
A12	12	N/C
A13	13	N/C
A14	14	N/C
A15	15	SA16
A16	16	SA15
A17	17	SA14
A18	18	SA13
A19	19	SA12
A20	20	SA11
A21	21	SA10
A22	22	SA9
A23	23	SA8
A24	24	SA7
A25	25	SA6
A26	26	SA5
A27	27	SA4
A28	28	SA3
A29	29	SA2
A30	30	SA1
A31	31	SA0
B1	32	GND
B2	33	ISA_RESET
B3	34	VDD
B4	35	IRQ9
B5	36	N/C
B6	37	N/C
B7	38	-12 V
B8	39	N/C
B9	40	+12 V
B10	41	GND
B11	42	N/C
B12	43	N/C
B13	44	N/C
B14	45	N/C
B15	46	N/C
B16	47	N/C
B17	48	N/C
B18	49	N/C

ISC Bus P1/P2	Pin #	ISA Bus Signal
B19	50	N/C
B20	51	N/C
B21	52	IRQ7
B22	53	IRQ6
B23	54	IRQ5
B24	55	IRQ4
B25	56	IRQ3
B26	57	N\C
B27	58	N/C
B28	59	BALE
B29	60	VDD
B30	61	N/C
B31	62	GND
C1	63	NI_SBHE
C2	64	LA23
C3	65	LA22
C4	66	LA21
C5	67	LA20
C6	68	LA19
C7	69	LA18
C8	70	LA17
C9	71	NI_MEMR
C10	72	NI_MEMW
C11	73	SD8
C12	74	SD9
C13	75	SD10
C14	76	SD11
C15	77	SD12
C16	78	SD13
C17	79	SD14
C18	80	SD15
D1	81	NI_MEMCS16
D2	82	N/C
D3	83	IRQ10
D4	84	IRQ11
D5	85	IRQ12
D6	86	IRQ15
D7	87	IRQ14
D8	88	N/C
D9	89	N/C
D10	90	N/C
D11	91	N/C
D12	92	N/C
D13	93	N/C
D14	94	N/C
D15	95	N/C
D16	96	VDD
D17	97	N/C
D18	98	GND

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Table 3-5 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names	Bussed or Unique	X = Pulled Up Via 10 KΩ Resistor
GND	50	GND	GND	GND
Reserved	49	RESERVED1	U	X
Ack*	48	N_IPxACK	U	X
A6	47	IPA6	B	
Strobe*	46	N_STROBE_x	U	X
A5	45	IPA5	B	
Intreq1*	44	N_IPxINTREQ1	U	X
A4	43	IPA4	B	
Intreq0*	42	N_IPxINTREQ0	U	X
A3	41	IPA3	B	
Error*	40	N_IPxERROR	U	X
A2	39	IPA2	B	
DMAEnd*	38	N_DMAEND	U	X
A1	37	IPA1	B	
Reserved	36	RESERVED2	U	X
IOSel*	35	N_IPxIOSEL	U	
DMAck0*	34	N_DMACK0	U	X
IntSel*	33	N_IPxINTSEL	U	
DMAReq1	32	N_DMAREQ1	U	X
MemSel*	31	N_IPxMEMSEL	U	X
DMAReq0	30	N_DMAREQ0	U	X
IDSel*	29	N_IPxIDSEL	U	
R/W*	28	V_WRITE	B	
+5V	27	+5VDC	+5 Vdc	+5 Vdc
GND	26	GND	GND	GND
GND	25	GND	GND	GND
+5V	24	+5VDC	+5 Vdc	+5 Vdc
+12V	23	+12VDC	+12 Vdc	+12 Vdc
-12V	22	-12VDC	-12 Vdc	-12 Vdc
BS1*	21	N_BS1	B	
BS0*	20	N_BS0	B	
D15	19	ILD15	B	X
D14	18	ILD14	B	X
D13	17	ILD13	B	X
D12	16	ILD12	B	X
D11	15	ILD11	B	X
D10	14	ILD10	B	X
D9	13	ILD9	B	X
D8	12	ILD8	B	X
D7	11	ILD7	B	X
D6	10	ILD6	B	X
D5	9	ILD5	B	X
D4	8	ILD4	B	X
D3	7	ILD3	B	X
D2	6	ILD2	B	X
D1	5	ILD1	B	X
D0	4	ILD0	B	X
Reset*	3	N_IPxRESET	U	
CLK	2	ICLK_x	B	
GND	1	GND	GND	GND

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The signals on the left side of the table are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. The lower case "x" in the Systran signal name represents the "A" or "B" mnemonic for each IP Module slot for memory transfers, or "A", "B", "C", "D", "E" or "F" for I/O, ID, or interrupt transfers.



NOTE: The IP Module data bus, usually defined as IPD[15:0] for all of our IP Modules, is a subset of the information that appears on these signal lines. Since carrier register information also uses these signal lines, the bus was defined as the "ISASC6 Local Data Bus" designated as ILD[15:0].

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4. PERFORMANCE

4.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. A Systran TESTIP was installed in slot "A" of the ISASC6. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Appendix A, SPECIFICATIONS.

4.2 State Timing Diagrams

The ISASC6 test configuration consisted of a typical IBM-type Personal Computer (hereafter referred to as a PC/AT), with a standard VGA monitor and keyboard. A Systran IP Module Logic Bus Extender board #BHAS-IPBE2 was used along with a 24-inch ribbon connector #BHAS-IPBEC24, and an IP Module Logic Bus Breakout Board #BHAS-IPBB. While the extender/breakout boards provided a means for connecting the IP Module bus signals, a Catalyst PC/AT200 extender board was used to connect most of the ISA bus signals. The waveforms that follow were printed from files created on an HP16500B logic analyzer and show all pertinent signals for both the ISA bus and the IP Module bus. A diagram of the test setup is shown below.

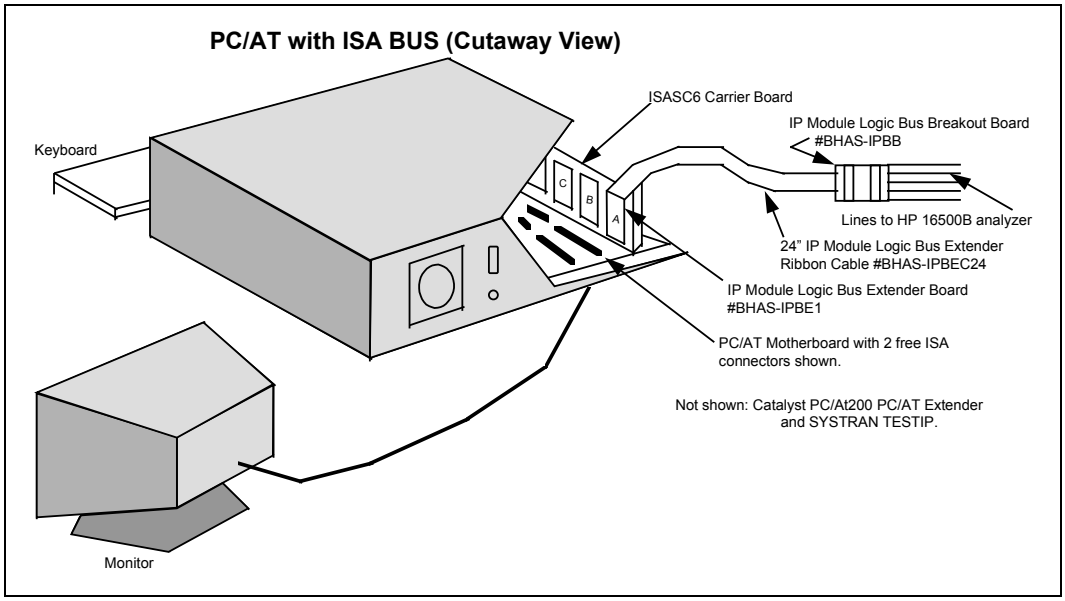


Figure 4-5 Performance Test Equipment Configuration

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4.2.1 CSR Read Cycle

Figure 4-6 shows the pertinent signals active during a read from the on-board CSRs for the ISASC6. During a read or write of the ISASC6 CSR registers, the IP Module-specific control signals will all be in their quiescent state while the ISA bus signals will be active. Shown below is an 8-bit register read transaction from the reset register at location Base + 0x600. Most of the action occurs toward the center-left portion of the diagram.

The transaction begins when the ISA platform asserts the bus address latch signal BALE and the ISASC6 asserts an MCS16 signal to inform the platform that it is capable of 16-bit transactions, even though the transaction to the reset register is an 8-bit one. The platform then asserts the MEMR command signal, which, when sensed by the ISASC6 as a transaction to a CSR, starts the register read transfer state machine. The register transfer state machine then asserts IOCHRDY (IOCHRD on the diagram) to insert wait states until the register can be read. IOCHRDY is then removed and the transaction completed when MEMR is deasserted from the platform. The process from the start of the clock cycle in which BALE is asserted to the end of the clock cycle where MEMR is removed is typically four ISA clock cycles or about 500 ns.

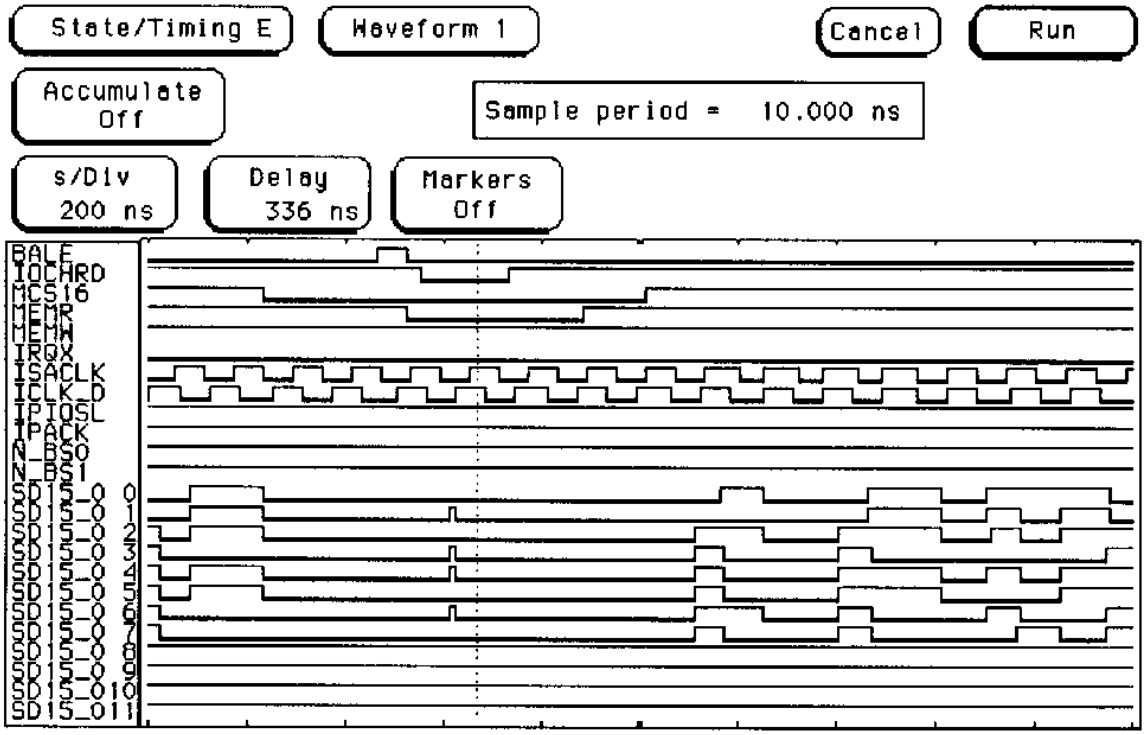


Figure 4-6 CSR READ

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4.2.2 CSR Write Cycle

Figure 4-7 shows the pertinent signals active during a write to the on-board CSRs for the ISASC6. Shown below is an 8-bit register write transaction to the memory 'A' size register at location Base + 0x702. Most of the action occurs toward the center portion of the diagram.

The transaction begins when the ISA platform asserts the bus address latch signal BALE and the ISASC6 asserts an MCS16 signal to inform the platform that it is capable of 16-bit transaction even though the transaction to the memory 'A' size register is an 8-bit one. The platform then asserts the MEMW command signal, which, when sensed by the ISASC6 as a transaction to a CSR, starts the register write transfer state machine. The register transfer state machine then asserts IOCHRDY (IOCHRD on the diagram) to insert wait states until the register can be written. IOCHRDY is then removed and the transaction completed when MEMW is deasserted from the platform. The process from the start of the clock cycle in which BALE is asserted to the end of the clock cycle where MEMW is removed is, as for the read cycle, four ISA clock cycles or about 500 ns.

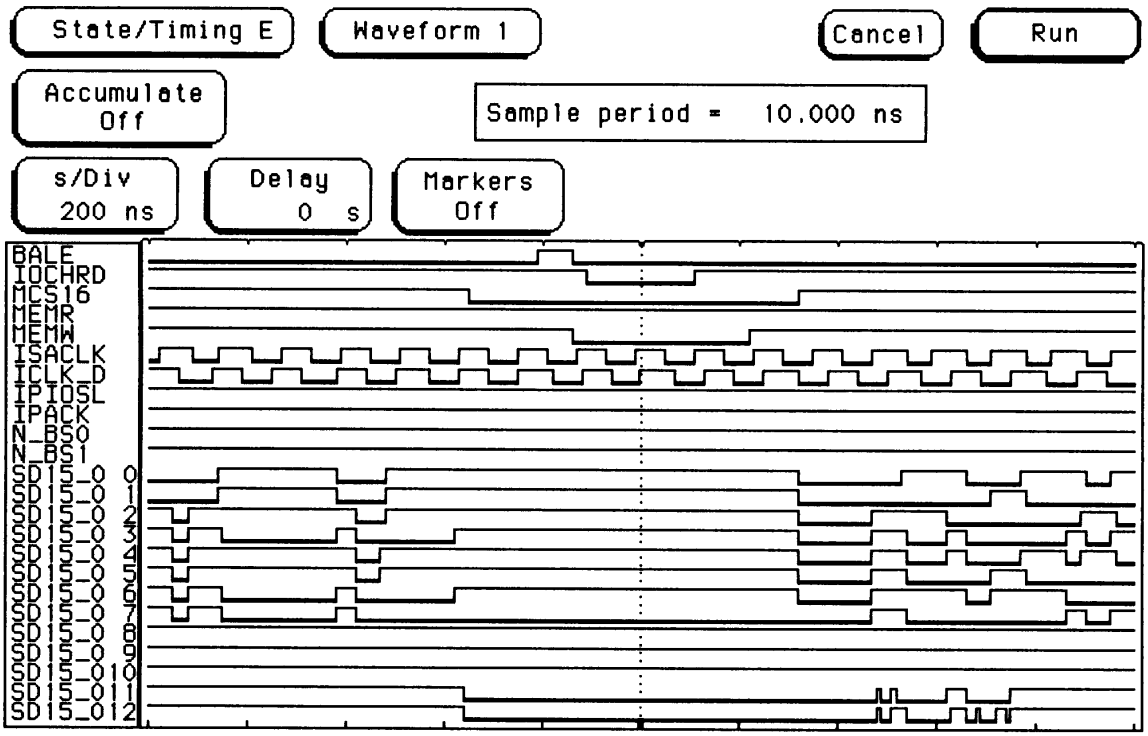


Figure 4-7 CSR WRITE

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4.2.3 I/O Write Cycle

Figure 4-8 shows the pertinent signals that are active during a write to the I/O space on each of the six IP Modules on the ISASC6. Unlike CSR transactions, both the ISA signals and the IP Module-specific signals are active during this type of transaction. An I/O write transaction begins when the ISA bus address strobe BALE is asserted by the platform and the ISASC6 responds with an assertion of MCS16 to the platform to establish the fact that it is capable of 16-bit transactions. The platform then asserts the MEMW command for a write transaction, which, when sensed by the ISASC6 address decoder as a transaction to I/O space on a given IP Module, starts the IP Module write state machine. The IP write state machine then asserts IOCHRDY (IOCHRD in the diagram) to insert ISA bus wait states and then asserts an IPIOSL shown in the diagram to the IP Module pointed to by the address decoder.

Since the ISASC6 asserts no hold cycles, the actual IP Module transaction can take as little as two IP clock cycles (one for the Select cycle and one for the Terminate cycle) if the IP Module asserts no wait states. When the IP Module sends back an IPACK signal, the state machine completes the write and then removes the IOCHRDY signal to the platform to complete the cycle. The platform will then remove the MEMW command and be ready for the next cycle. The process from the clock cycle in which BALE is asserted by the platform until the MEMW is removed from the platform is about five ISA clock cycles or about 625 ns.

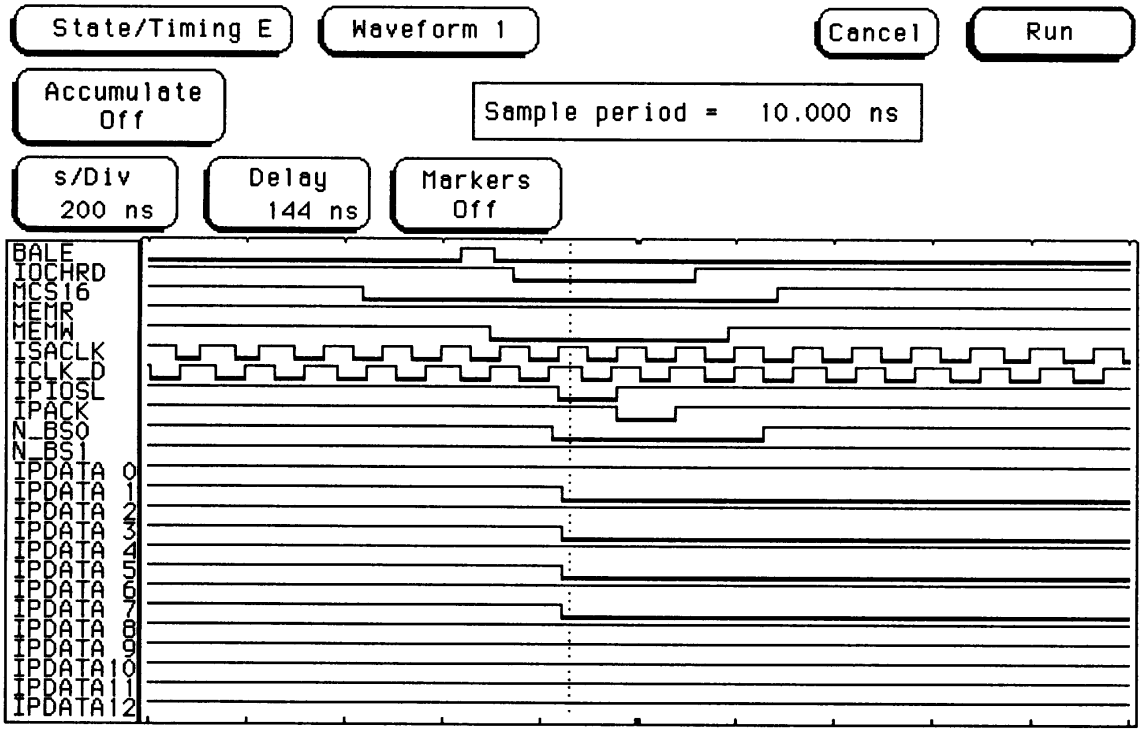


Figure 4-8 I/O WRITE

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4.2.4 I/O Read Cycle

Figure 4-9 shows the pertinent signals that are active during a read from the I/O space on each of the six IP Modules on the ISASC6. Unlike CSR transactions, both the ISA signals and the IP Module-specific signals are active during this type of transaction. An I/O read transaction begins when the ISA bus address strobe BALE is asserted by the platform and the ISASC6 responds with an assertion of MCS16 to the platform to establish the fact that it is capable of 16-bit transactions. The platform then asserts the MEMR command for a read transaction, which, when sensed by the ISASC6 address decoder as a transaction to I/O space on a given IP Module, starts the IP Module read state machine. The IP read state machine then asserts IOCHRDY (IOCHRD in the diagram) to insert ISA bus wait states and then asserts an IPIOSL shown in the diagram to the IP Module pointed to by the address decoder.

Since the ISASC6 asserts no hold cycles, the actual IP Module transaction can take as little as two IP clock cycles (one for the Select cycle and one for the Terminate cycle) if the IP Module asserts no wait states. When the IP Module sends back an IPACK signal, the state machine completes the read and then removes the IOCHRDY signal to the platform to complete the cycle. The platform will then remove the MEMR command and be ready for the next cycle. The process from the clock cycle in which BALE is asserted by the platform until the MEMR is removed from the platform is about five ISA clock cycles or about 625 ns.

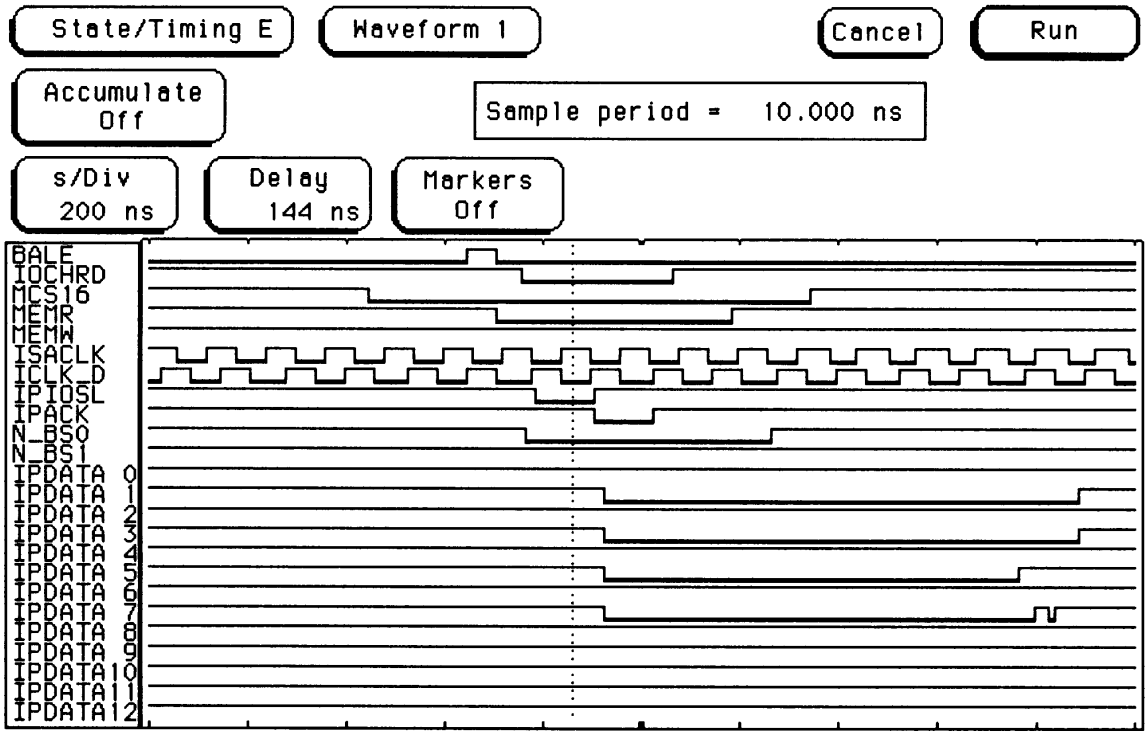


Figure 4-9 I/O READ

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4.2.5 ID Read Cycle

Figure 4-10 shows the pertinent signals that are active during a read from the ID space on each of the six IP Modules on the ISASC6. Unlike CSR transactions, both the ISA signals and the IP Module-specific signals are active during this type of transaction. An ID read transaction begins when the ISA bus address strobe BALE is asserted by the platform and the ISASC6 responds with an assertion of MCS16 to the platform to establish the fact that it is capable of 16-bit transactions. The platform then asserts the MEMR command for a read transaction, which, when sensed by the ISASC6 address decoder as a transaction to ID space on a given IP Module, starts the IP Module read state machine. The IP read state machine then asserts IOCHRDY (IOCHRD in the diagram) to insert ISA bus wait states and then asserts an IPIDSL shown in the diagram to the IP Module pointed to by the address decoder.

Since the ISASC6 asserts no hold cycles, the actual IP Module transaction can take as little as two IP clock cycles (one for the Select cycle and one for the Terminate cycle) if the IP Module asserts no wait states. When the IP Module sends back an IPACK signal, the state machine completes the read and then removes the IOCHRDY signal to the platform to complete the cycle. The platform will then remove the MEMR command and be ready for the next cycle. The process from the clock cycle in which BALE is asserted by the platform until the MEMR is removed from the platform is about five ISA clock cycles or about 625 ns.

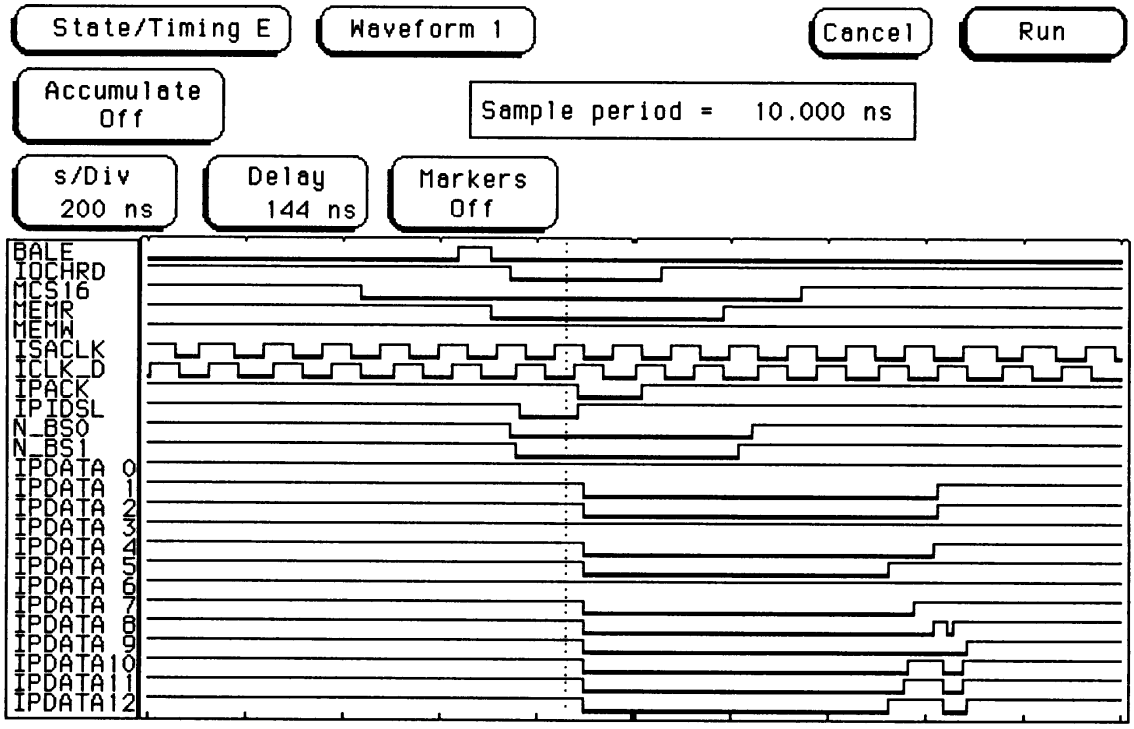


Figure 4-10 ID Space READ

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4.2.6 ID Write Cycle

Figure 4-11 shows the pertinent signals that are active during a write to the ID space on each of the six IP Modules on the ISASC6. Unlike CSR transactions, both the ISA signals and the IP Module specific signals are active during this type of transaction. An ID write transaction begins when the ISA bus address strobe BALE is asserted by the platform and the ISASC6 responds with an assertion of MCS16 to the platform to establish the fact that it is capable of 16-bit transactions. The platform then asserts the MEMW command for a write transaction, which, when sensed by the ISASC6 address decoder as a transaction to ID space on a given IP Module, starts the IP Module write state machine. The IP write state machine then asserts IOCHRDY (IOCHRD in the diagram) to insert ISA bus wait states and then asserts an IPIDSL in the diagram to the IP Module pointed to by the address decoder.

Since the ISASC6 asserts no hold cycles, the actual IP Module transaction can take as little as two IP clock cycles (one for the Select cycle and one for the Terminate cycle) if the IP Module asserts no wait states. When the IP Module sends back an IPACK signal, the state machine completes the read and then removes the IOCHRDY signal to the platform to complete the cycle. The platform will then remove the MEMW command and be ready for the next cycle. The process from the clock cycle in which BALE is asserted by the platform until the MEMW is removed from the platform is about five ISA clock cycles or about 625 ns.

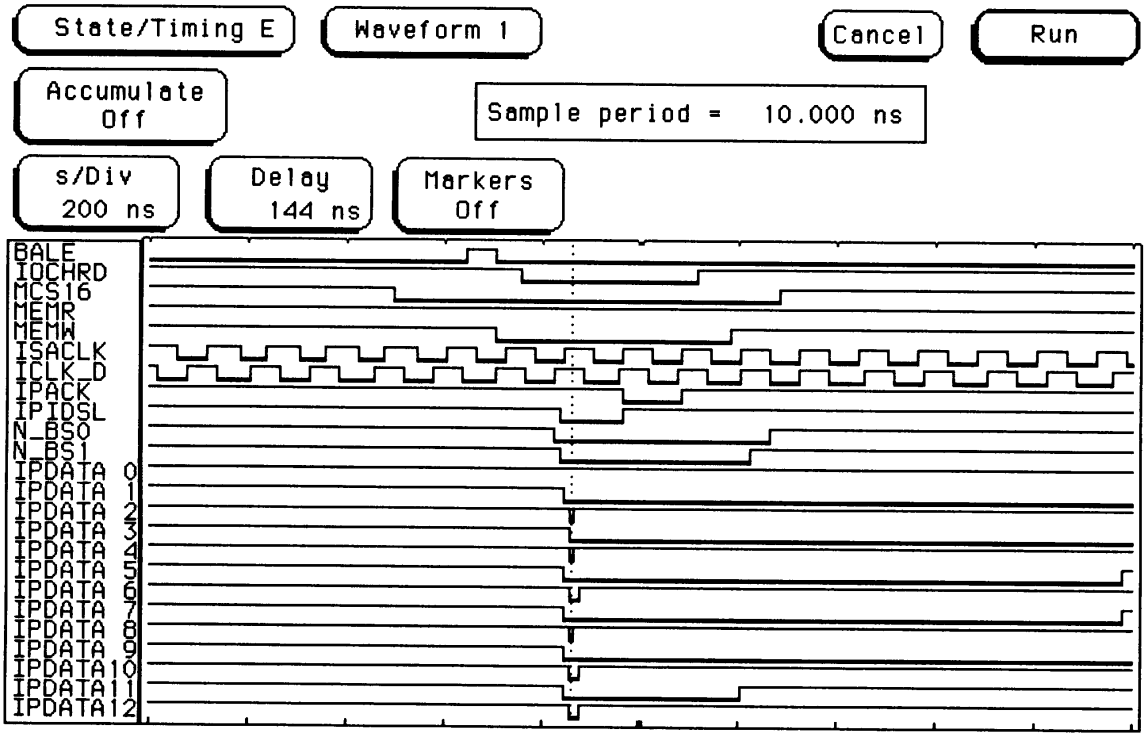


Figure 4-11 ID Space WRITE

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4.2.7 Memory Write Cycle

Figure 4-12 shows the pertinent signals that are active during a write to the memory space on IP Modules A and B on the ISASC6 with the memory select signal MEMXSL in the diagram applying to IP Module slots A and B only. A memory write transaction begins when the ISA bus address strobe BALE is asserted by the platform and the ISASC6 responds with an assertion of MCS16 to the platform to establish the fact that it is capable of 16-bit transactions. The platform then asserts the MEMW command for a write transaction, which, when sensed by the ISASC6 address decoder as a memory address within the bounds for either IP Module A or B, starts the IP Module write state machine. The IP write state machine then asserts IOCHRDY (IOCHRD in the diagram) to insert ISA bus wait states and then asserts a MEMXSL per the diagram to the IP Module pointed to by the address decoder.

Since the ISASC6 asserts no hold cycles, the actual IP Module transaction can take as little as two IP clock cycles (one for the Select cycle and one for the Terminate cycle) if the IP Module asserts no wait states. When the IP Module sends back an IPACK signal, the state machine completes the read and then removes the IOCHRDY signal to the platform to complete the cycle. The platform will then remove the MEMW command and be ready for the next cycle. The process from the clock cycle in which BALE is asserted by the platform until the MEMW is removed from the platform is about five ISA clock cycles or about 625 ns. For 16-bit memories, therefore, the potential transfer rate with a one-clock idle cycle between transactions is about 2.7 megabytes per second.

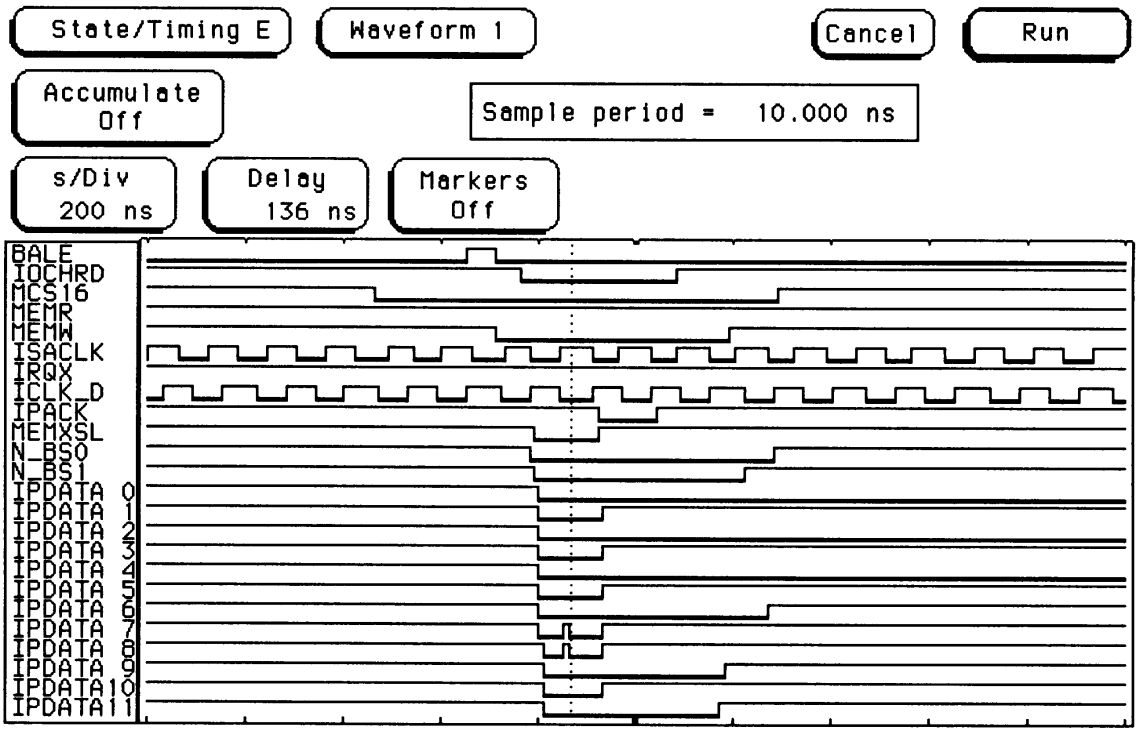


Figure 4-12 Memory Write

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4.2.8 Memory Read Cycle

Figure 4-13 shows the pertinent signals that are active during a read from the memory space on IP Modules A and B on the ISASC6 with the memory select signal MEMXSL in the diagram applying to IP Module slots A and B only. A memory read transaction begins when the ISA bus address strobe BALE is asserted by the platform and the ISASC6 responds with an assertion of MCS16 to the platform to establish the fact that it is capable of 16-bit transactions. The platform then asserts the MEMR command for a read transaction, which, when the ISASC6 address decoder as a memory address within the bounds for either IP Module A or B, starts the IP Module read state machine. The IP read state machine then asserts IOCHRDY (IOCHRD in the diagram) to insert ISA bus wait states and then asserts a MEMXSL in the diagram to the IP Module pointed to by the address decoder.

Since the ISASC6 asserts no hold cycles, the actual IP Module transaction can take as little as two IP clock cycles (one for the Select cycle and one for the Terminate cycle) if the IP Module asserts no wait states. When the IP Module sends back an IPACK signal, the state machine completes the read and then removes the IOCHRDY signal to the platform to complete the cycle. The platform will then remove the MEMR command and be ready for the next cycle. The process from the clock cycle in which BALE is asserted by the platform until the MEMR is removed from the platform is about five ISA clock cycles or about 625 ns. For 16-bit memories, therefore, the potential transfer rate with a one-clock idle cycle between transactions is about 2.7 megabytes per second.

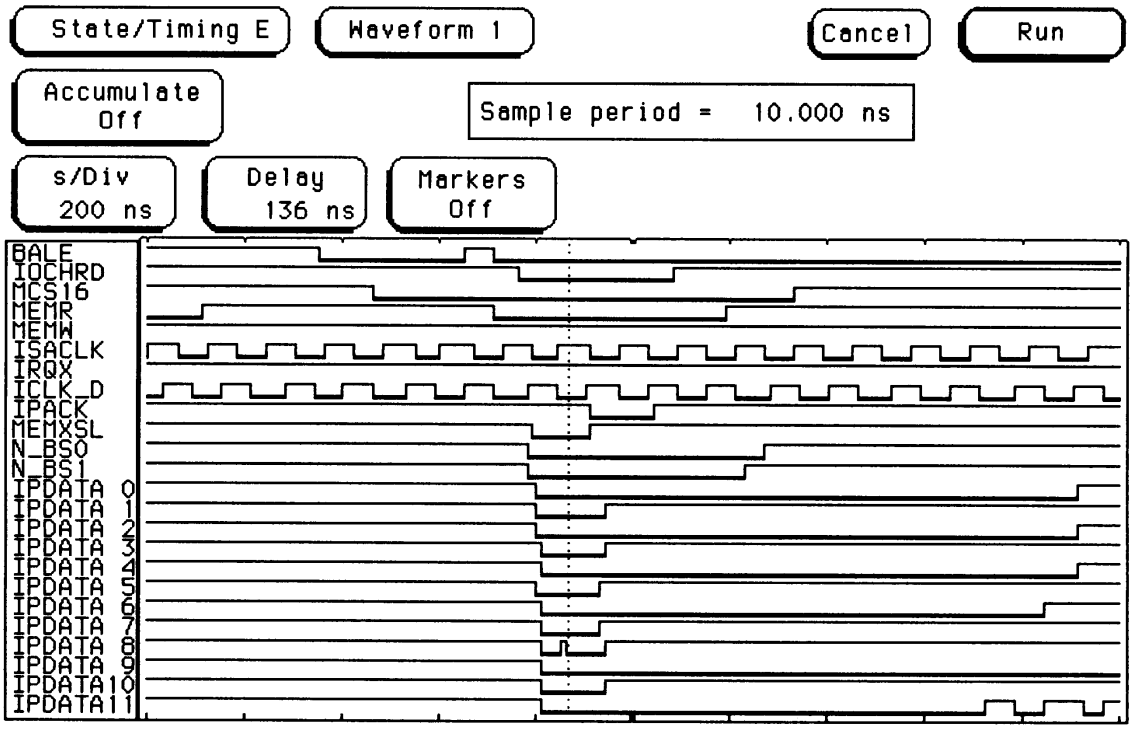


Figure 4-13 Memory Read

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4.2.9 Interrupt Request

Figure 4-14 shows all the pertinent signals that are active during the generation of an interrupt request to the ISA bus as a result of an **Intreq0** or **Intreq1** being asserted from any of the six IP Modules. Interrupt generation occurs when the interrupt control register is written to on the IP Module with control bits set to generate one or both interrupts. On the ISASC6, this can be done by a write to the IP Module interrupt control register (address location 0x3D on the Systran TESTIP). Interrupt generation begins when the ISA bus address strobe BALE is asserted by the platform and the ISASC6 responds with an assertion of MCS16 to the platform to establish the fact that it is capable of 16-bit transactions. The platform then asserts the MEMW command for a write transaction, which, when sensed by the address decoder as an I/O transaction, starts the IP Module write state machine. The IP write state machine then asserts IOCHRDY (IOCHRD in the diagram) to insert ISA bus wait states and then asserts an IPIOSL in the diagram to the IP Module pointed to by the address decoder.

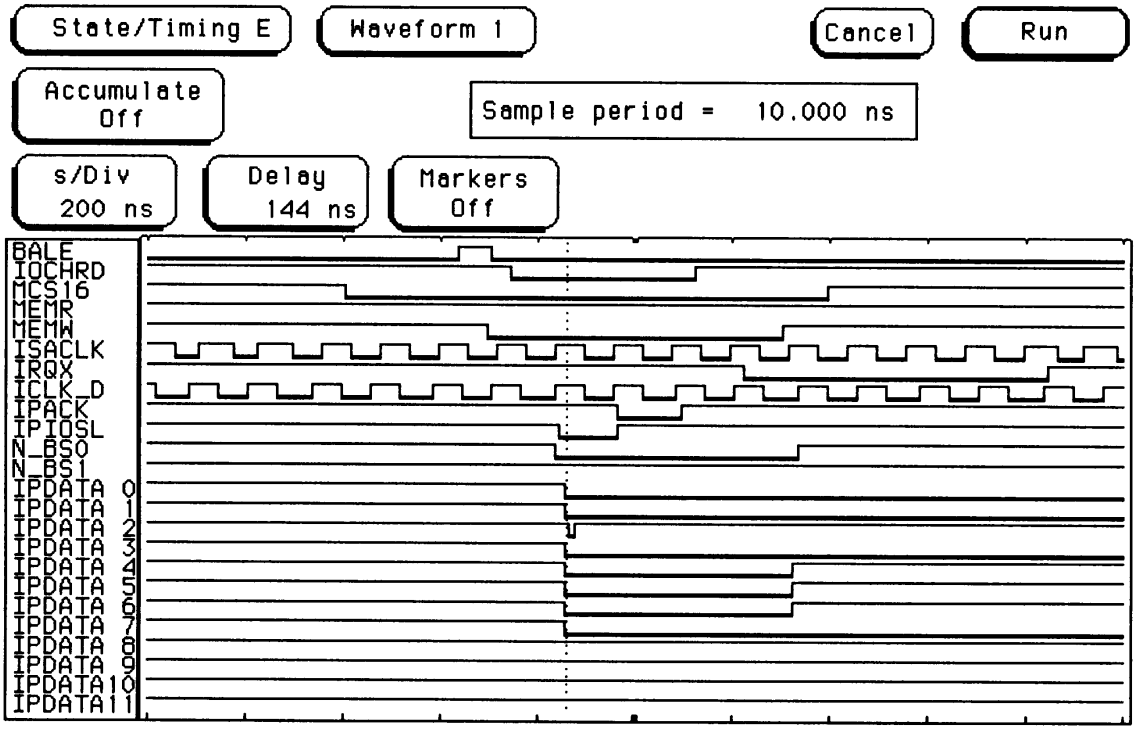


Figure 4-14 Interrupt Request

Since the ISASC6 asserts no hold cycles, the actual IP Module transaction can take as little as two IP clock cycles (one for the Select cycle and one for the Terminate cycle) if the IP Module asserts no wait states. When the IP Module sends back an IPACK signal, the state machine completes the write and then removes the IOCHRDY signal to the platform to complete the cycle. As the platform removes the MEMW command, the IP Module which now has the interrupt-enable bit set will immediately generate an interrupt causing an IRQX to the ISA bus to be generated on the next ISA clock cycle. Interrupts, therefore, are generated very quickly, usually within one IP Module clock cycle of a completed write to the interrupt control register.

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NOTE: This scenario uses the TESTIP IP Module, which is used for functional validation of an IP Module carrier, and is not representative of a typical application where an interrupt is caused by an asynchronous external event.

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APPENDIX A

SPECIFICATIONS

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A.1 Specifications

MECHANICAL

Measurements ..... 13.345 inches x 4.8 inches
Weight ..... 8.392 oz., 238 grams (includes back panel)
Board thickness ..... 0.062 inches, 0.157 cm, nominally, (6 layers)

POWER REQUIREMENTS

Power (no IP Modules installed): ..... +5 Vdc (±5%) @ 0.65 A (Maximum)
+12 Vdc @ 0.0 A
-12 Vdc @ 0.0 A



NOTE: The ISA bus ground and IP Modules' ground are not isolated through this board.

PERFORMANCE CHARACTERISTICS

Electrical Characteristics..... Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

+5 Vdc supply voltage with respect to ground:
Minimum ..... -0.5 V
Maximum ..... +7.0 V
+12 Vdc supply voltage with respect to ground:
Dependent on IP Modules installed.
-12 Vdc supply voltage with respect to ground:
Dependent on IP Modules installed.

RECOMMENDED OPERATING CONDITIONS:

Supply voltage with respect to ground: ..... +4.75 V → +5.25 V

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): ..... 0°C to +70°C
Temperature (Storage): ..... -40°C to +85°C
Humidity (Non-condensing): ..... 5% to 95%
Vibration (Operating): ..... 10 G's RMS, 10→55 Hz, random
Shock (Operating): ..... 50 G's maximum
Altitude (Operating): ..... 10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MIL-HDBK-217F ..... 340,679 hours
Bellcore 332, Issue 6..... 418,546 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

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APPENDIX B

TYPICAL APPLICATIONS

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B.1 Applications

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the ISASC6 Slave Carrier to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 Typical ISA Setup

Anyone familiar with the VMESC5 and related products will notice right away that the form factor of and setup for an ISA IP Module carrier is different. Although the cabling for an ISA carrier may not be as convenient as that for VME, it is potentially more attractive since the cables protrude from the rear of the unit rather than the front. Plug the cables onto the board as shown in Figure B-1 and as discussed in Section 3.3.3.

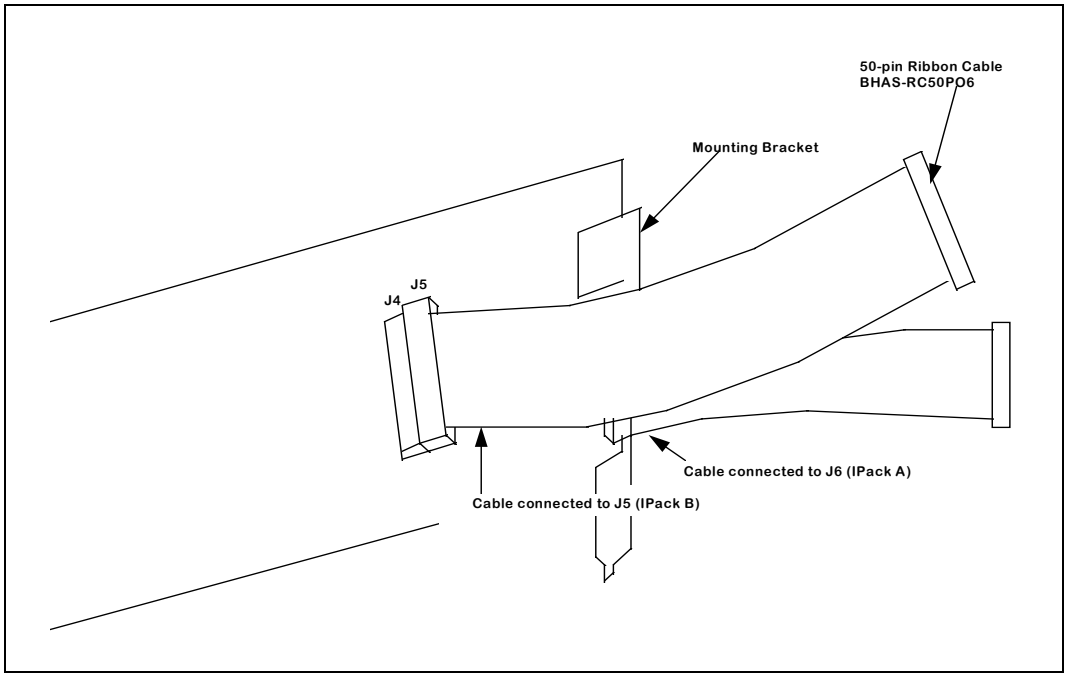


Figure B-1 Typical ISA Setup



NOTE: IP Module A connector, J6, allows direct access through the board mounting bracket while IP Modules B through F allow connection along the component-side of the board using 50-pin flat ribbon cables such as Systran Part No. BHAS-RC50P03 (3-foot cable) or Systran Part No. BHAS-RC50P06 (6-foot cable).

The cables for IP Modules B through F should be inserted through the rectangular hole in the rear of the ISA machine cabinet before the ISASC6 is installed into the slot. The cables can then be stacked against J6 through the mounting bracket and the board then plugged into the slot. Finally, the cables can be plugged into J1 - J5.

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NOTE: If six IP Modules are used on the ISASC6 it may be necessary to leave one blank slot in the computer to allow for the thickness of the five flat ribbon cables of IP Module slots B through F.

Tagging each cable with a unique code using adhesive labels or permanent ink marker is recommended.

B.3 Typical Interrupt Servicing for the ISASC6

For the following procedure, assume that IP Modules A through C have been set to IRQ5 on the ISA bus and that IP Modules D through F have been set to IRQ10 on the ISA bus.

- Upon initialization of program, save the current interrupt service routine (ISR) information.
- Install ISR A_C for IRQ5.
- Install ISR D_F for IRQ10.
- Initialize both programmable-interrupt controllers (8259A-type devices).
- Enter the main loop of the program here.
- At the end of the main program loop, restore the old interrupt service routines before exiting.

The ISR for the ISASC6 could be written similar to the following:

- Upon entering the ISR, set the programmable interrupt controller to enable higher-priority interrupts to preempt this ISR.
- Read the steering register (CSR Address Base + 698) to determine if one or more interrupts have occurred.
- The ISR for A_C will “and” 0x3F with the value read from the steering register for masking purposes. The ISR for D_F will “and” 0xFC0 with the value read from the steering register for the same reason.
- The following is a typical routine:

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```
while (any bit set)
        if (bit 0 set)
             handle IPA - IRQ0
             clear source
        else if (bit 1 set)
             handle IPA - IRQ1
             clear source
        else if (bit 2 set)
             handle IPB - IRQ0
             clear source
                   .
                   .
                   .
        else if (bit 5 set)
             handle IPC - IRQ1
             clear source
        reread steering register
        ISR for A_C will “and” 3Fh with the value read from
          the steering register as before.
        ISR for D_F will “and” FC0 with the value read from
          the steering register as before.
              signal end-of-interrupt to the PIC
return from exception
```


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APPENDIX C

PROGRAMMING GUIDE

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C.1 Overview

This appendix describes the operation of the ISASC6 from the software perspective, detailing the ISASC6 registers and the overall mapping and addressing scheme for the board, and provides programming examples. A more detailed description of the hardware can be found in Chapter 2, PRODUCT OVERVIEW and Chapter 3, INSTALLATION, and application concepts are discussed in appendix B, TYPICAL APPLICATIONS.

C.2 Description

The ISASC6 is an easy-to-use ISA slave card that holds six singlewide, four singlewide and one doublewide, two singlewide and two doublewide, or three doublewide IndustryPack modules. In addition to providing access to the I/O and ID space of the IP Modules via the ISA Bus, the ISASC6 has three on-board control/status registers.

C.3 Board Base Address

The ISASC6 2 KB-wide I/O, I/D, and CSR space can be located anywhere above 0x200000 or below 0xFE0000 in the ISA memory space on 2 KB boundaries. This is accomplished using the ISA base address jumpers J30 through J42. See section 3.3.2 for details. The memory spaces for IP Modules A and B are set using programmable registers as specified in section 3.3.2.

C.4 Address Map

The IP Module I/O and ID, and the carrier's control, status, and general-purpose registers, reside at a fixed relative address from the ISASC6 base address. The Memory Base Register points to the base addresses for memory 'A' and memory 'B'.

Table C-1 shows the complete memory map for the board.

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Table C-1 ISASC6 Address Map

Address Space or Register Name	ISA Address (relative to board base address)	Size
IP Module A I/O	Base + 0x000	128 bytes
IP Module A ID	Base + 0x080	128 bytes
IP Module B I/O	Base + 0x100	128 bytes
IP Module B ID	Base + 0x180	128 bytes
IP Module C I/O	Base + 0x200	128 bytes
IP Module C ID	Base + 0x280	128 bytes
IP Module D I/O	Base + 0x300	128 bytes
IP Module D ID	Base + 0x380	128 bytes
IP Module E I/O	Base + 0x400	128 bytes
IP Module E ID	Base + 0x480	128 bytes
IP Module F I/O	Base + 0x500	128 bytes
IP Module F ID	Base + 0x580	128 bytes
IP Module Reset Register	Base + 0x600	6 bits
Error Status Register	Base + 0x602	6 bits
IP Module A IRQ0 Register	Base + 0x680	8 bits
IP Module A IRQ1 Register	Base + 0x682	8 bits
IP Module B IRQ0 Register	Base + 0x684	8 bits
IP Module B IRQ1 Register	Base + 0x686	8 bits
IP Module C IRQ0 Register	Base + 0x688	8 bits
IP Module C IRQ1 Register	Base + 0x68A	8 bits
IP Module D IRQ0 Register	Base + 0x68C	8 bits
IP Module D IRQ1 Register	Base + 0x68E	8 bits
IP Module E IRQ0 Register	Base + 0x690	8 bits
IP Module E IRQ1 Register	Base + 0x692	8 bits
IP Module F IRQ0 Register	Base + 0x694	8 bits
IP Module F IRQ1 Register	Base + 0x696	8 bits
Interrupt Steering Register	Base + 0x698	12 bits
IP Module Memory Enable Register	Base + 0x700	2 bits
IP Module A Memory Size Register	Base + 0x702	7 bits
IP Module A Memory Base Register	Base + 0x704	8 bits
IP Module B Memory Size Register	Base + 0x706	7 bits
IP Module B Memory Base Register	Base + 0x708	8 bits
General Purpose Register A	Base + 0x780	8 bits
General Purpose Register B	Base + 0x782	8 bits
General Purpose Register C	Base + 0x784	8 bits

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C.5 Register Descriptions

The ISASC6 registers can be accessed as byte (D8) or word (D16) values. When accessed as bytes, the odd byte is not driven by the carrier and its value is all '1's due to ILD[15:8] pull-up resistors. The unused bits in the even byte are driven as 0's on reads. All unused bits are discarded on writes. The hexadecimal addresses for the registers shown below are relative to the board base address and are in the WORD format for word and byte accesses, respectively.

C.5.1 Reset Register (0x600)

Setting one of the bits RES_F through RES_A to '1' asserts the corresponding IP Module's reset line. The bits can be set individually by writing a '1' to that bit or simultaneously with a single write of '0x3F'. When set, a one-shot is triggered supplying a minimum 200 ms reset pulse as required by the IP Module specification. When read, these bits return the status of the corresponding IP Module's reset line (a '0' means the IP Module is not being reset, a '1' means it is in a reset condition).

Table C-2 Reset Register Bit Description

Bit #	B15-B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	RES_F	RES_E	RES_D	RES_C	RES_B	RES_A
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W
Power-up State	N/A	0	0	0	0	0	0

NOTE: RES_F-RES_A: Reset bits for IP Module slots F to A.

C.5.2 Error Status Register (0x602)

These bits indicate the state of the corresponding N_IPxERROR signal (pin #40 on a given IP Module). If the N_IPxERROR* signal is asserted (active low) for a particular IP Module, then the corresponding ERR_x bit will be set to a '1'. If the N_IPxERROR signal is not asserted, then the corresponding bit will be cleared.

Table C-3 Error Status Register Bit Description

Bit #	B15-B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	ERR_F	ERR_E	ERR_D	ERR_C	ERR_B	ERR_A
R/W	Reads '1's Writes discarded	R	R	R	R	R	R
Power-up State	N/A	State of IP Module F ERR* Signal	State of IP Module E ERR* Signal	State of IP Module D ERR* Signal	State of IP Module C ERR* Signal	State of IP Module B ERR* Signal	State of IP Module A ERR* Signal

NOTE: ERR_F-ERR_A: Error Status bits for IP Module slots F to A.

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C.5.3 Interrupt Vector Registers for IP Modules A through F (0x680— 0x696)

The twelve interrupt-vector registers (two per IP Module) are 8-bit, read-only registers that latch the appropriate interrupt vector that is driven on the IP Module data bus during an interrupt-acknowledge cycle. The interrupt engine decodes the address from the ISA bus and selects the appropriate vector register from the IP Modules. Address bits A2 up to A4 are used to select which of six IP Modules will have an interrupt vector read, while bit A1 (per IP Module specification) is used to determine which of the two vectors on a given IP Module will be accessed.

Table C-4 Interrupt Vector Registers

Address	Interrupt Vector Register	Address	Interrupt Vector Register
Base + 0x680	IP Module 'A' Intreq0	Base + 0x682	IP Module 'A' Intreq1
Base + 0x684	IP Module 'B' Intreq0	Base + 0x686	IP Module 'B' Intreq1
Base + 0x688	IP Module 'C' Intreq0	Base + 0x68A	IP Module 'C' Intreq1
Base + 0x68C	IP Module 'D' Intreq0	Base + 0x68E	IP Module 'D' Intreq1
Base + 0x690	IP Module 'E' Intreq0	Base + 0x692	IP Module 'E' Intreq1
Base + 0x694	IP Module 'F' Intreq0	Base + 0x696	IP Module 'F' Intreq1

C.5.4 Interrupt Steering Register (0x698)

As mentioned in the above section, the Interrupt Steering register is first read by the ISR to determine which of the twelve IP Module interrupts is (are) being asserted. A 12-bit read-only register, it provides a bit for both interrupts on all six IP Modules installed onto the ISASC6. A table of the bits in the Interrupt Steering register is shown below.

Table C-5 Interrupt Steering Register

Bit #	B15-B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	IRQ1 F	IRQ0 F	IRQ1 E	IRQ0 E	IRQ1 D	IRQ0 D	IRQ1 C	IRQ0 C	IRQ1 B	IRQ0 B	IRQ1 A	IRQ0 A
R/W	Reads '1's Writes discarded	R	R	R	R	R	R	R	R	R	R	R	R
Power-up State	N/A	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: Each bit will be a '1' when the corresponding interrupt is set.

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C.5.5 Memory Enable Register (0x700)

The Memory Enable register is a 2-bit read/write register on the ISASC6 used to enable or disable the memory function for IP Modules A and B. A value of 0x00 written to this register will disable both IP Module memories. A value of 0x01 will enable only IP Module A memory, a value of 0x02 will enable only IP Module B memory, and a value of 0x03 will enable both.



NOTE: If both IP Module memories are to be enabled at one time, then set the base addresses and sizes of each memory such that their address ranges do not overlap.

Table C-6 Memory Enable Register

Bit #	B15-B2	B1	B0
Bit Name	Not Used	MEMORY B ENABLE	MEMORY A ENABLE
R/W	Reads '1's Writes discarded	R/W	R/W
Power-up State	N/A	0	0

NOTE: Each memory is enables when its corresponding bit = '1'

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C.5.6 Memory Size Register (0x702 and 0x706)

The Memory Size registers for IP Module A memory and IP Module B memory are 7-bit read/write registers used to set the required size for the address range in the 16 MB ISA memory map. Setting the size is accomplished by writing '1's' to all register bits below the bit representing the stated size of memory.

EXAMPLE:

To install a 2 MB memory IP Module into slot 'B', write '1's' to bit positions B4 down to B0 in register 0x706. This would be a write of 0x1F to location Base + 0x706.

Table C-7 Memory Size Register

Bit #	B15-B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	MEMSIZE 8M	MEMSIZE 4M	MEMSIZE 2M	MEMSIZE 1M	MEMSIZE 512K	MEMSIZE 256K	MEMSIZE 128K
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up State	N/A	0	0	0	0	0	0	0

NOTE: Memory size is set according to Table C-8. The default memory size is 64 KB.

Table C-8 Memory Size Table

Memory Size	Bit Settings (MSB to LSB)
8 MB	1111111
4 MB	0111111
2 MB	0011111
1 MB	0001111
512 KB	0000111
256 KB	0000011
128 KB	0000001
64 KB	0000000

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C.5.7 Memory Base Register (0x704 and 0x708)

The Memory Base register for IP Modules A and B is used to locate the memory space for each of the two IP Modules in the ISA 16 MB memory map. The eight bits of this register correspond to the eight most-significant bits of the ISA address bus from bit 23 down to bit 16. When memory transfers occur, an on-board address-compare circuit determines whether the address on the ISA bus is within the bounds set by this register and the memory size register explained above. If the bus address is within bounds, a transfer will occur to the IP Module memory specified by the enable register.

Table C-9 Memory Base Register (A&B)

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	ISA LA23	ISA LA22	ISA LA21	ISA LA20	ISA LA19	ISA LA18	ISA LA17	ISA SA16
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up State	N/A	0	0	0	0	0	0	0	0

C.5.8 General-purpose Registers A through C (0x780— 0x784)

General-purpose registers A to C are completely user-definable. These read/write registers can be used as a "scratch pad", shared memory, etc. See Appendix B, TYPICAL APPLICATIONS, for more application information regarding these registers.

Table C-10 General-purpose Register Bit Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	GPR7	GPR6	GPR5	GPR4	GPR3	GPR2	GPR1	GPR0
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up State		0	0	0	0	0	0	0	0

NOTE: GPR7-GPR0: The General-purpose Register byte value.

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C.6 Programming Examples

The following examples illustrate how to program the ISASC6 to achieve various operational modes.

C.6.1 Reset Example

This example resets one, then all six IP Modules, and then monitors the reset signals to determine when they are de-asserted. Setting a bit in the reset register causes a one-shot to assert the corresponding IP Module reset signal (the one-shot asserts the reset signal for approximately 240 ms). The reset signal can then be monitored by reading the Reset register to determine when it is de-asserted.

- Write '0x01' to the Reset register. This resets the IP Module in slot A by asserting the IP Module A reset signal.

LOOP1:

- Read the Reset register.
- If Bit 0 is set then go to LOOP1.
- Write '0x3F' to the Reset register. This resets all six IP Modules by asserting their corresponding reset signals.

LOOP2:

- Read the Reset register.
- If any of bits [5:0] are set then go to LOOP2.

C.6.2 Interrupt Initialization Example

Interrupts in the ISA based system are sensed by the platform as a low to high transition with the interrupt request line remaining at a logic high until the system CPU has accessed any necessary registers to service the interrupt. On the ISASC6, there are two jumper-selectable ISA interrupts available to drive the bus from the IP Module control logic. These interrupts are prioritized along with other interrupts on the bus by the platform interrupt controller.

An example is given in Appendix B, TYPICAL APPLICATIONS.

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GLOSSARY

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[x:y] ---------- Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the least significant eight bits).

aperture---------- A region or set of addresses.

byte-lane ---------- Eight bits of a data bus on octal boundaries.

CSR ---------- Control and Status Register.

doublewide ---------- An IP Module that is twice the size of the singlewide board.

EPLD ---------- Erasable Programmable Logic Device.

ID PROM ---------- The circuitry that presents the proper data pattens to the lower eight bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IP Module---------- Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP Module logic bus ---------- A synchronous, 4 MTransfers/sec, 16-bit-wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6 bits wide (22 bits wide in memory mode).

IPDbus---------- IP Module Data Bus.

ISR ---------- Interrupt Service Routine

MTBF ---------- Mean Time Between Failures.

ns, µs, ms ---------- Nanoseconds, microseconds, and milliseconds, respectively.

singlewide ---------- An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL ---------- Very high-speed integrated circuit Hardware Description Language.

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