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TRIDO48

Tristateable 48-Channel Digital Output IP Module Hardware Reference

Document No. B-T-MR-TRIDO48#-A-0-A3

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's tristateable, 48-channel digital output IP Module board, referred to as the TRIDO48 (Tristateable, Digital Output, 48 channels) part number BHAS-TRIDO48.

1.1.2 Scope

This reference manual covers the physical and operational description of the TRIDO48, both from hardware and software perspectives. This manual also contains detailed technical information about the TRIDO48's performance characteristics, and a few typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded.

```
c:\>ls
file1        file2           file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- Systran *TRIDO48 Software Library Manual* (Doc. No. B-T-ML-TRIDO48)
- Systran *TRIDO48 Software Library Manual for PCI/CPCI IP Carriers Using Windows NT 4.0* (Doc. No. B-T-ML-NTARP)
- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)
- *American National Standard for IP Modules (ANSI/VITA 4-1995)* published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite

104, Scottsdale, AZ 85260-3415 USA. Phone: 480-951-8866, FAX: 480-951-0720, E-mail: info@vita.com, URL: www.vita.com

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Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

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Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

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2. PRODUCT OVERVIEW

2.1 Overview

The TRIDO48 is a singlewide IP Module board, conforming both mechanically and electrically to the American National Standard for IP Modules (ANSI/VITA 4-1995) specification. For a typical quad-IP Module carrier, the TRIDO48 can provide up to 192 digital outputs through any single slot on a computer bus backplane, or can be mixed with other IP Modules for a more customized, modular I/O system solution. Figure 2-1 is a picture of the TRIDO48 board.

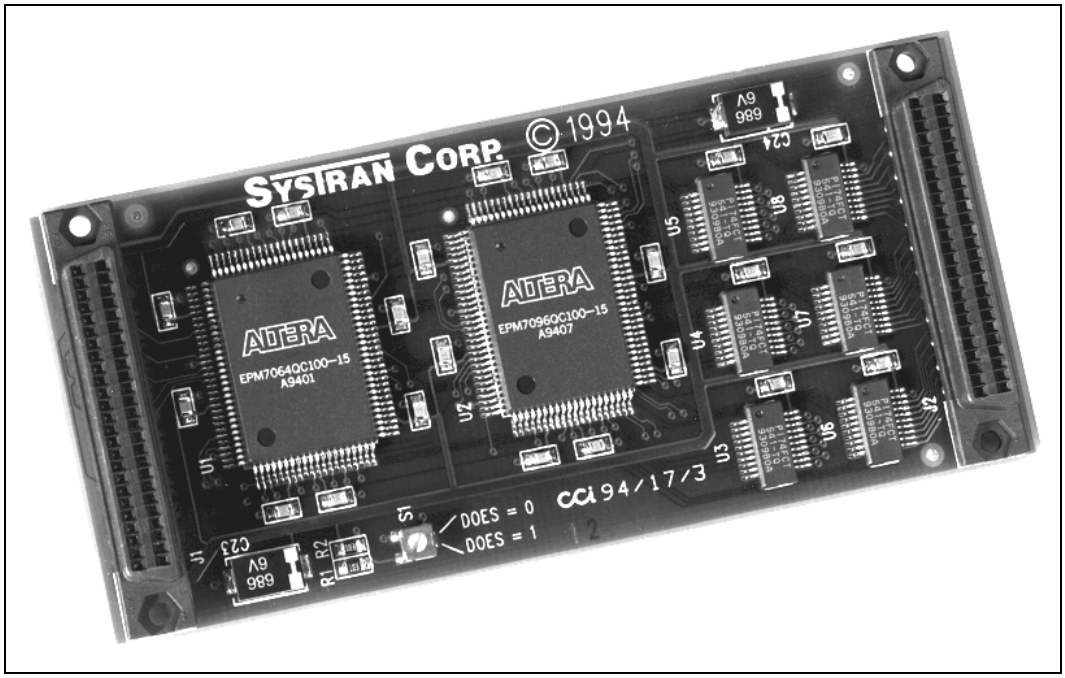


Figure 2-1 TRIDO48 Board

2.2 Features

- Six byte-wide ports that are individually tristateable via hardware and/or software.
- Board-level hardware status/control.
- External input to control TRI-STATE conditions on any of the six ports.
- External output of status on update of any of the ports.
- Switch-selectable power-up default of port impedance states.
- Common I/O connector pin-out.
- TTL outputs with per channel source/sink ratings of -15 mA and +64 mA, respectively.

2.3 Related Products

Software:

- 'C' library and OS-9 device-driver routines with documentation.
- Windows NT 4.0 library software with documentation.

2.4 Block Diagram Description

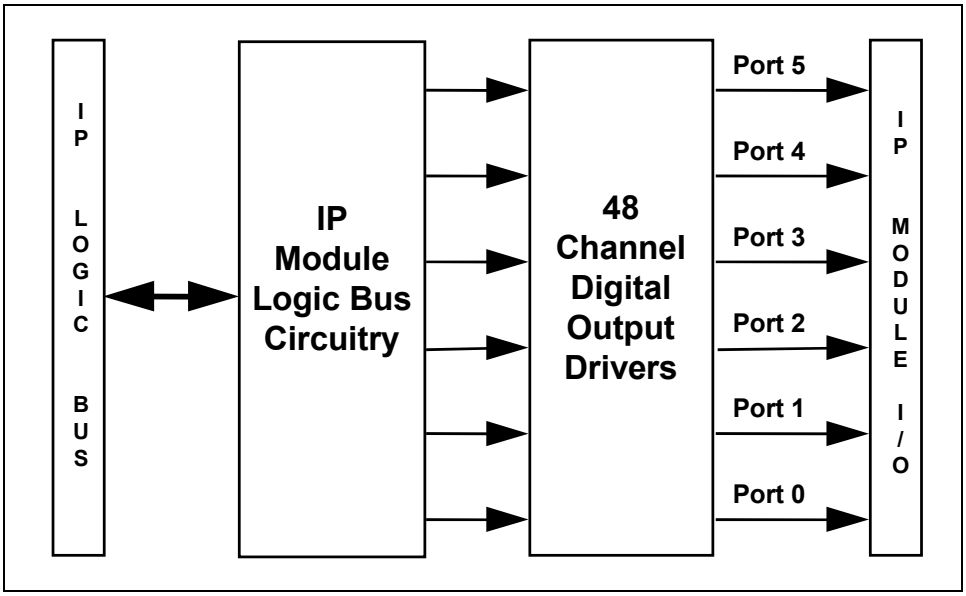


Figure 2-2 TRIDO48 Simple Block Diagram

Figure 2-2 is a simplified block diagram of the TRIDO48. On the left side of the diagram is the IP Module Logic Bus connector through which all transfers between the IP Module carrier and the TRIDO48's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface Circuitry" contains all of the write/read-back data registers, the ID PROM data, control/status register, external hardware handshake circuitry, port control line generators, and IP Module transfer sequence/control and data bus interface logic. The majority of this logic is implemented via a pair of EPLDs.

The block labeled "48 Channel Digital Output Drivers" contains the 74FCT tristateable drivers, implemented with individual logic devices, housed in quarter-sized small outline packages (QSOP). On the right side of the diagram is the TRIDO48 I/O connector, providing source and sink currents for all 48 digital lines, a ground reference, and the single control/status hardware handshake signal line.

Figure 2-3 presents a detailed block diagram of the TRIDO48. Again, on the left side is the IP Module's Logic Bus connector through which all host carrier transfers take place. The six 8-bit ports are paired-off into three 16-bit registers or "words." Each "word" contains two 8-bit registers, a 16-bit tristateable gate for driving the IP Data bus (IPDbus) during I/O reads, and a 16-bit driver port that directly feeds a pair of digital output driver 74FCT541's that are labeled "octal tristate gates." The architecture supports byte-writes to either octal register, or to both of them as 16-bit writes. All I/O register reads are performed at the "word" width of 16 bits, only.

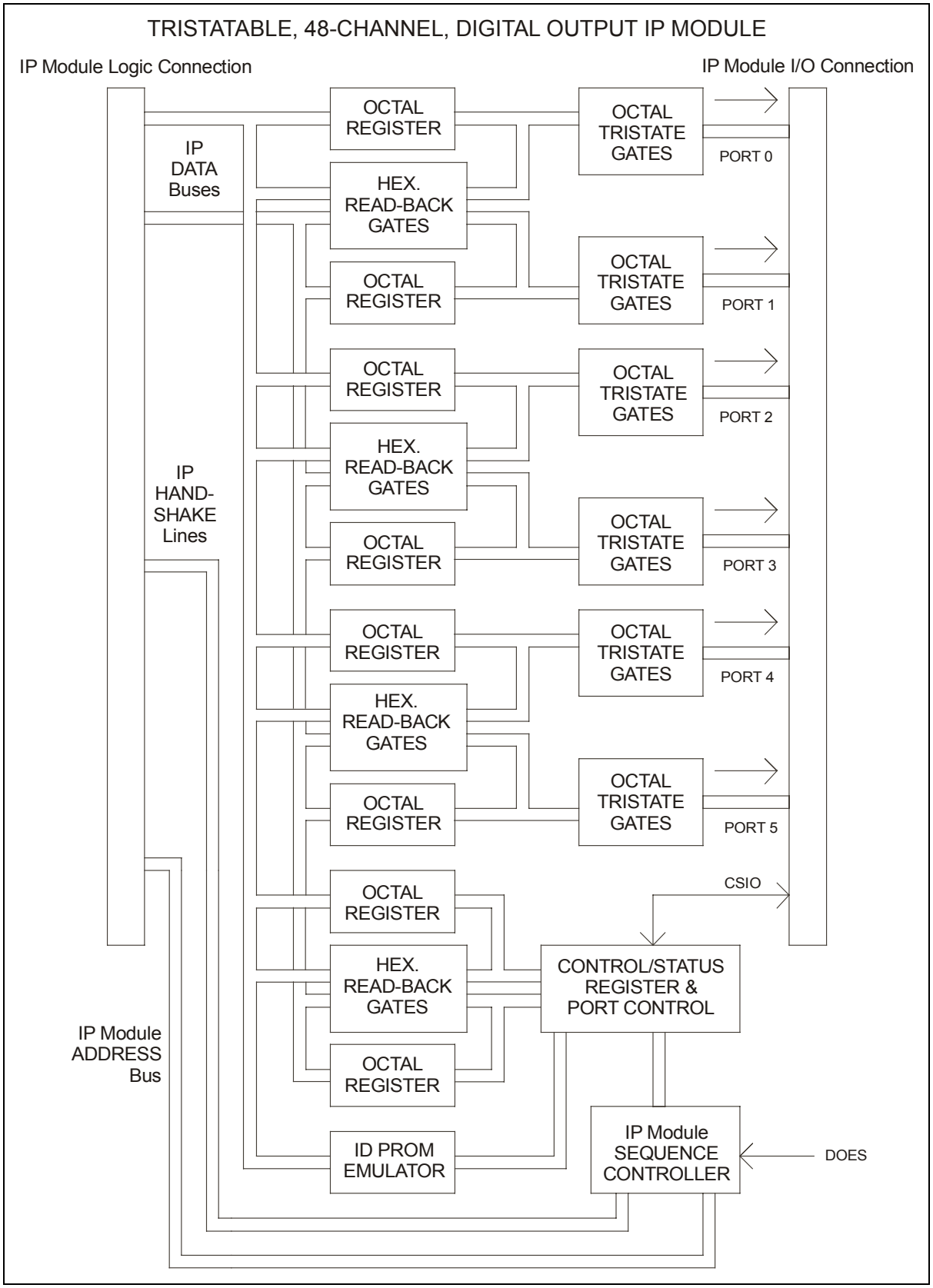


Figure 2-3 TRIDO48 Detailed Block Diagram

The control/status register has a similar IP Module carrier interface, lacking the octal TRI-STATE gate interface. The register's primary function is to maintain the TRI-STATE conditions of each of the individual 8-bit output ports, and the functionality of the single hardware handshake line, "CSIO" (**C**ontrol_**S**tatus_**I**nput_**O**utput).

The ID PROM Emulator is the circuitry that presents the proper data patterns to the lower 8 bits of the IPDbus, with upper-byte zero-fills, during the ID (read) transfers. Emulating the never-changing ID information in this way reduces parts count and costs, and increases system reliability with its associated MTBF value.

The last (bottom right) block contains all of the sequence control logic for performing orderly transfers between the TRIDO48 and its carrier. Included in this block is the power-up logic for this board. The signal entering the right of this block, labeled "DOES" (**D**efault_**O**utput_**E**nable_**S**tate), is used to preset 12 of the 16 bits of the control/status register for either enabling or disabling all of the output drivers during the initial power-up sequence. This signal is generated by the only on-board switch.

2.5 Detailed Description

The TRIDO48 was developed using VHDL and Synthesis, and targeted to Altera EPLDs. The design was schematic-captured and integrated to standard logic devices, connectors and discrete components using VIEWlogic CAE tools.

2.5.1 TRIDO48 Components

All IP Module Logic Bus transfers take place across J1, the IP Module Logic Connector, located on the left side of all block diagrams. Generally speaking, this IP Module does not support DMA or Interrupts, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and writes to a short, four-location I/O map.

PRIMARY ACTIVITY CONTROLLER

The TRIDO48's primary activity "CONTROLLER" is housed within the EPM7064QC100 EPLD located at U1. The controller serves as the primary IP Module transfer sequence engine, with the following responsibilities:

- Detect valid I/O and ID transfer operations within their respective fully decoded address ranges, including the support of HOLD cycles when generated by a carrier.
- Generate ID PROM emulation data patterns for ID read transfers.
- Port output-enable control circuitry with power-up default initialization circuits.
- Encode registration (for I/O writes) and IPDbus output-enable (for I/O reads) command lines for the BUSLINK module at U2.
- Perform necessary control and status operations for the CSIO handshake line that directly connects to the I/O connector at pin 49.

PRIMARY I/O CONTROLLER

The TRIDO48's primary I/O (non ID) data handling controller is the "BUSLINK" module contained within the EPM7096QC100 EPLD that is located at U2. The responsibility of this module is to serve as forty-eight write/read-back bits—with external encoding of what to do and when—coming from the controller (described above). This encoded control includes nine possible write combinations and three possible read combinations. The I/O write transfers, after being detected as valid, consist of any one of eight individual byte-wide writes, or as any one of three double-byte (16-bit word) writes,

but the read operations are always done as full-word accesses. The forty-eight digital outputs are driven from this device to the six port drivers.

PORT DRIVERS

The six byte-wide port drivers consist of 74FCT541 devices in QSOP packages, which are reference designators U8 through U3. These tristateable non-inverting buffers can source -15 mA and sink 64 mA. These buffers are driven by the BUSLINK module at U2 and their low/high impedance states are controlled by the CONTROLLER module at U1. The outputs of these buffers connect directly to the I/O connector at pins [48:1]. The pinout of the driver port designations are identical to many PC-based digital I/O cards, and are compatible with all of their various accessories (like: terminal blocks, electromechanical relay boards, DC and AC solid-state relays, etc.), allowing easy I/O transition interfacing and upgrade operations from PC-based I/O products.

DOES SWITCH

The DOES switch allows this IP Module to be powered up with all of the outputs enabled (switch open) or all of the outputs disabled (switch closed). The logic state of this input to the CONTROLLER module during the assertion of N_RESET determines the initial-ization state of the least significant twelve bits in the control/status register. If DOES is high, Control/Register bits 11 down to 0 (CR[11:0]) are set high; if DOES is low, CR[11:0] are cleared low. While this IP Module is pre-set as a ready-to-use simple digital output card (DOES is open = high) with all outputs enabled, certain applications may require that the outputs be disabled at power-up, until port-control software can properly exercise output enable/disable operations, as would be the case when several TRIDO48 boards emulate a tristateable, parallel communications bus.

CSIO LINE

The CSIO signal line is a multi-function handshake line that acts as either a control-input (power-up default), or as a status-output signal, as determined by bit 12 on the control register. As an input, in conjunction with CR[11:0], the CSIO can selectively control the high and low impedance states of each of the individual byte-lane drivers, with selectable sense control. For example, CSIO can turn on three byte-lanes and turn off the other three byte-lanes while in a high state, and then reverse this condition when placed in a low state. As an output, the CSIO can selectively provide a pulse output when any individual register or all registers are updated with new information. This feature is useful for generating interrupts to other system components. The CSIO also can be constantly "high" to emulate the pin-50 function found on similar PC-based digital cards.

2.5.2 DOES Switch Details

The DOES switch, located at reference S1, pre-configures the state of the board's output drivers during the power-up reset operations. When the switch is in the position labeled "DOES = 1" (fully counter-clockwise position), all six byte-lanes of the drivers are placed in their low-impedance (ON) states, which is the factory default position.

TRISTATE

If the feature of being able to tristate (place in high impedance) any or all of the byte-lane output drivers is used, as in bussing operations, then the output drivers should power-up in the high-impedance states (until software can begin running and control the port states). Setting the DOES switch in the "DOES = 0" (fully clockwise) position during power-up accomplishes this, and will prevent output state contention problems where

bussed signals from different TRIDO48 IP Modules attempt to simultaneously drive high and low states.

BUSSED APPLICATIONS

For bussed applications that reside in the same chassis or on a single (embedded processor) platform where all TRIDO48 IP Modules will be reset at the same time, the "DOES = 1" position can be used. Since all data bits are cleared to zero on power-up, the potential high versus low state-contention problem is circumvented, even though all output drivers will be enabled.

3. INSTALLATION

3.1 Unpack the TRIDO48

Table 3-1 TRIDO48 Shipping Package contents

Qty	Description
1	TRIDO48 Printed Circuit Assembly
1	TRIDO48 Hardware Reference*

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number. (For example: BTMR-TRIDO48).

3.2 Visually Inspect the TRIDO48

Examine the TRIDO48 to determine if any damage occurred during shipping.

3.3 Install the TRIDO48 Board



NOTE: Since the TRIDO48 is an Electrostatic Sensitive Device (ESD), the hardware installation of the TRIDO48 must be conducted on a good anti-static workbench to protect the IP Module and carrier boards. The IP Module carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the TRIDO48 can be installed.

The TRIDO48 installation requires the tools listed in Table 3-2.

Table 3-2 TRIDO48 Installation Tools

Qty	Description
1	ESD static control kit/ground strap/etc.
1	Standard flat-head screwdriver (optional)

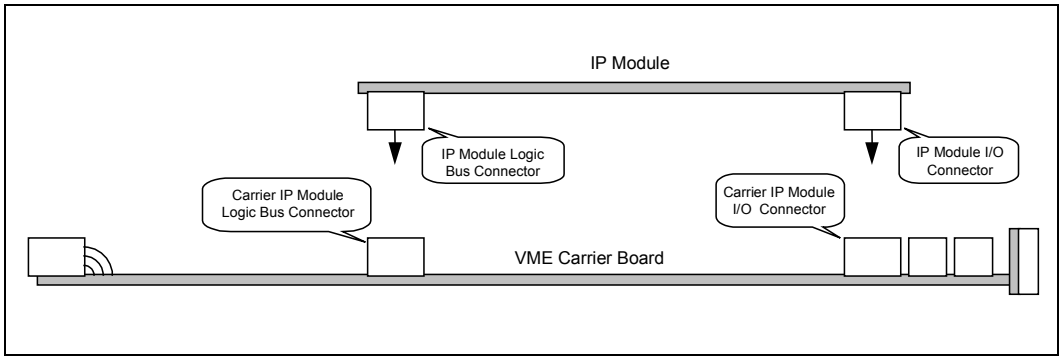


Figure 3-1 TRIDO48 Installed on a VME IP Module Carrier Board

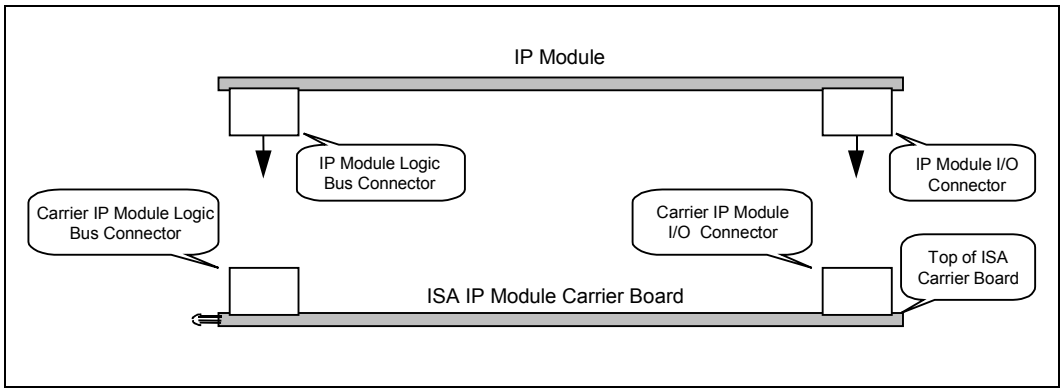


Figure 3-2 TRIDO48 Installed on an ISA IP Module Carrier Board

Figure 3-1 shows how the TRIDO48 is installed on a VME IP Module carrier, and Figure 3-2 shows the board installed on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran.

Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board user's manual for more information.

Referring to the appropriate figures and tables perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the TRIDO48 can be installed.
3. Remove the TRIDO48 from the shipping package and place it on the ESD bench.
4. Install the TRIDO48 onto the carrier board by applying adequate and equal pressure to the TRIDO48 board at both ends.

*5. Install four M2x5 mm flat-head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the TRIDO48 to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Name
50	GND
49	CSIO
48	Port 5 Bit 0
47	Port 5 Bit 1
46	Port 5 Bit 2
45	Port 5 Bit 3
44	Port 5 Bit 4
43	Port 5 Bit 5
42	Port 5 Bit 6
41	Port 5 Bit 7
40	Port 4 Bit 0
39	Port 4 Bit 1
38	Port 4 Bit 2
37	Port 4 Bit 3
36	Port 4 Bit 4
35	Port 4 Bit 5
34	Port 4 Bit 6
33	Port 4 Bit 7
32	Port 3 Bit 0
31	Port 3 Bit 1
30	Port 3 Bit 2
29	Port 3 Bit 3
28	Port 3 Bit 4
27	Port 3 Bit 5
26	Port 3 Bit 6
25	Port 3 Bit 7
24	Port 2 Bit 0
23	Port 2 Bit 1
22	Port 2 Bit 2
21	Port 2 Bit 3
20	Port 2 Bit 4
19	Port 2 Bit 5
18	Port 2 Bit 6
17	Port 2 Bit 7
16	Port 1 Bit 0
15	Port 1 Bit 1
14	Port 1 Bit 2
13	Port 1 Bit 3
12	Port 1 Bit 4
11	Port 1 Bit 5
10	Port 1 Bit 6
9	Port 1 Bit 7
8	Port 0 Bit 0
7	Port 0 Bit 1
6	Port 0 Bit 2
5	Port 0 Bit 3
4	Port 0 Bit 4
3	Port 0 Bit 5
2	Port 0 Bit 6
1	Port 0 Bit 7

4. PERFORMANCE

4.1 Overview

The figures and tables in this section are a collection of typical rise/fall, and board response times to various system stimuli and IP Module cycles.

Timing measurements were conducted on the TRIDO48 using an HP model 16500A Logic Analyzer with a 400 megasamples/sec Digitizing Oscilloscope Module, model 16531A, plugged into slot E, and a 1 GHz Timing Master Module, model 16515A in slot C. The TRIDO48 was installed in the IP Module slot 'A' of a Motorola MVME-162-01 VME processor IP Module carrier board. Figure 4-1 shows the test configuration for the oscilloscope and state timing measurements.

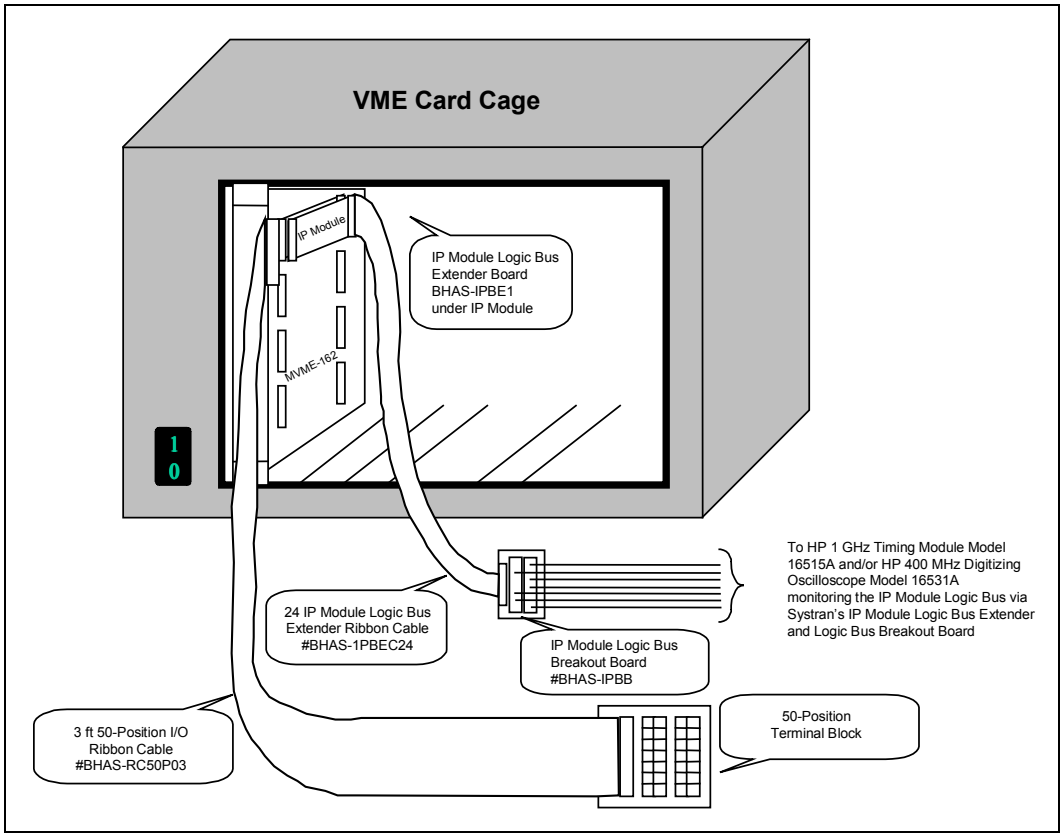


Figure 4-1 IP Module Test Configuration for Oscilloscope and State Timing Measurements

4.2 State Timing Diagram

Tables 4-1 and 4-2 present some typical timing values for various functions performed by the TRIDO48. It is important to note there were no loads attached to the three output lines monitored, which allowed some ringing to take place. Also, it provides different timing values for outputs coming from and going to high-impedance states when compared to the values presented in paragraph 4.4: “Output Driver Timing Measurements”.

Figure 4-2 ICLK Referred Timing

Parameter/Event	Typical Time (ns)
ICLK to Port Outputs	10
ICLK to Port Outputs	11
ICLK to CSIO (to a steady state)	7
ICLK to CSIO (to a steady state)	8
CSIO Typical Pulse Width	125
ICLK to CSIO (Pulse Output)	4
ICLK to Output High Impedance to Logic High	17
ICLK to N_ACK (Read data about the same)	9
ICLK to N_ACK	9

Figure 4-3 CSIO Controlled Outputs

Parameter/Event	Typical Time (ns)
CSIO to Output High Impedance to Logic High	21
CSIO to Output High Impedance to Logic High	25
CSIO to Output Logic High to High Impedance	152
CSIO to Output Logic High to High Impedance	143

The Logic State Diagram in Figure 4-2 is a typical representation of waveforms captured for the data tabulation. The state waveforms were made using the HP 1 GHz Timing Master Module with the Systran IP Module Logic Bus Extender (IPLBE) and an IP Module Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer‘s screen are active low, and are represented by a ‘/’ as the first character as opposed to the ‘N_’ used elsewhere, due to the limited amount of character spacing.

The “noise” in this diagram is caused by reflections due to unterminated ribbon cables, and high-impedance measurement interfaces. The open and floating lines are also responsible for some of the large state transition values.

The three I/O connector pins monitored for these tests, pins 8, 7, and 6, connect to bits 0, 1, and 2 of port 0, respectively; as modified by IPD0, IPD1, and IPD2 by I/O write transfers.

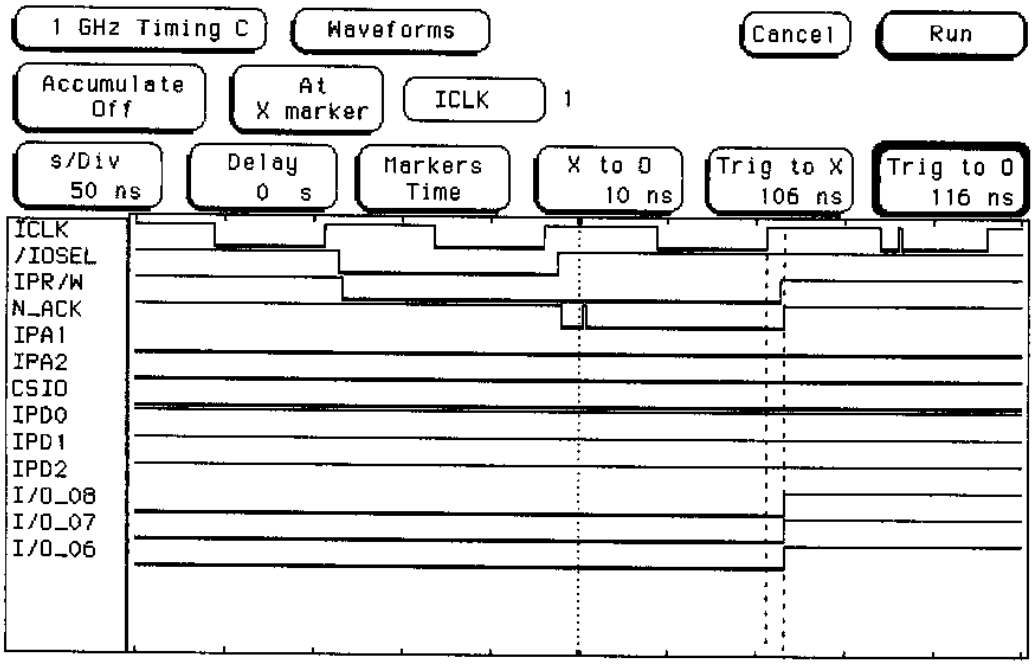


Figure 4-4 I/O Write to Ports 0 and 1: F’s → 0’s

4.3 Output Driver Performance Measurements

The measurements in Tables 4-3 and 4-4 were made using the HP 400 MHz Digitizing Oscilloscope Module with the oscilloscope probe on Pin #1 of the terminal block (which is the TRIDO48's I/O connector Port 0, Bit 7). This output bit is driving a load of three feet of standard 50-pin ribbon cable to a terminal block with various pullup resisters to +5 V and pulldown resistors to ground. The specification of the TRIDO48's output drivers are the Output High Voltage = +2.4 V (min.) at -15 mA, and the Output Low Voltage = +0.55 V(max.) at 64 mA. These tables show the TRIDO48's typical sourcing and sinking current measurements.

Figure 4-5 Source Currents (Load to Ground)

Test Load To Ground	Output High Voltage	Load Current	Notes
No Load	+3.80 V	0 A	No load connected
47.3 KΩ	+3.55 V	-75 µA	
5.56 KΩ	+3.45 V	-621 µA	
994 Ω	+3.30 V	-3.32 mA	
462 Ω	+3.18 V	-6.88 mA	
N/A	N/A	-15 mA	+2.4 V minimum by specification
99.6 Ω	+2.738 V	-27.5 mA	Operation beyond specification
47.4 Ω	+2.350 V	-49.6 mA	Operation beyond specification



NOTE: The differences in the number of decimal places of resolution of the measurements are due to the auto-scaling of the digital multimeter used.

Figure 4-6 Sink Currents (Load to Ground)

Test Load To Ground	Output High Voltage	Load Current	Notes
No Load	0.0 mV	0 A	No load connected
47.3 KΩ	+0.5 mV	102 µA	
5.56 KΩ	+4.5 mV	864 µA	
994 Ω	+25.1 mV	4.81 mA	
462 Ω	+53.9 mV	10.3 mA	
99.6 Ω	+244.8 mV	45.6 mA	
N/A	N/A	64 mA	+0.55 V by specification
47.4 Ω	+0.504 mV	90.0 mA	Operation beyond specification

These performance measurements only loaded one channel (of 48). They represent typical (not guaranteed) values, and were presented to confirm the ability to source and sink the specified currents of -15 mA and +64 mA, respectively.

4.4 Output Driver Timing Measurements

The test configuration consists of the TRIDO48 IP Module #108, port 0, bit 7 and CSIO, at the end of a 3-foot I/O cable with terminal block. Non-CSIO measurements were made from pin #1 where the load resistance was attached. Pin #49 performed the same functions for CSIO.

All timing values are referred to the 50% point of the rising edge of the ICLK signal. Measurement was made using an IPLBE, Type 1 extender board with a 3-foot extender cable ending with the IPLBB Bus Breakout Board. The cable length was chosen to minimize skew between the ICLK reference signal and the signal under test.

Figure 4-3 is a dual-trace digital storage oscilloscope figure that is typical of all the tabulated results. This particular "snapshot" shows the 16 ns required to go from a high-impedance state to a logic-low state with a 10.3 mA (Sink) load to +4.81 V.

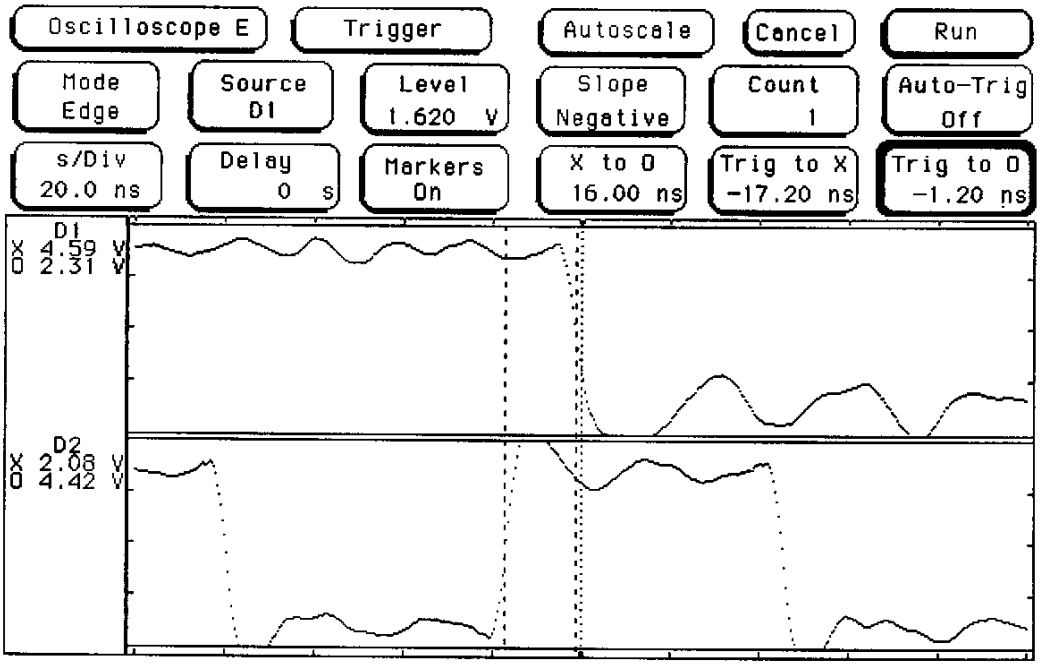


Figure 4-7 Typical High-Impedance State to Low-Logic State

Figure 4-8 Output Driver Timing Measurements

Parameter	Typical Timing	Test Conditions
Logic Low to High Impedance	24.0 ns @ Pin 1	10.3 mA sink to +4.81 V
	15.2 ns @ Pin 1	45.6 mA sink to +4.81 V
Logic High to High Impedance	20.8 ns @ Pin 1	-6.88 mA source to Ground
	12.8 ns @ Pin 1	-27.5 mA source to Ground
High Impedance to Logic Low	16.0 ns @ Pin 1	10.3 mA sink to +4.81 V
	16.4 ns @ Pin 1	45.6 mA sink to +4.81 V
High Impedance to Logic High	15.6 ns @ Pin 1	-6.88 mA source to Ground
	16.4 ns @ Pin 1	-27.5 mA source to Ground
Logic Low to Logic High	10.8 ns @ Pin 1	10.3 mA sink to +4.81 V
	10.4 ns @ Pin 1	45.6 mA sink to +4.81 V
	8.0 ns @ Pin 1	-6.88 mA source to Ground
	10.0 ns @ Pin 1	-27.5 mA source to Ground
Logic High to Logic Low	10.4 ns @ Pin 1	10.3 mA sink to +4.81 V
	10.8 ns @ Pin 1	45.6 mA sink to +4.81 V
	8.4 ns @ Pin 1	-6.88 mA source to Ground
	8.0 ns @ Pin 1	-27.5 mA source to Ground
↑ ICLK to ↑ CSIO	7.6 ns @ Pin 49	3.32 mA sink to Ground
↑ ICLK to ↑ CSIO	7.2 ns @ Pin 49	-4.81 mA source to +4.81 V
↑ ICLK to ↓ CSIO	6.0 ns @ Pin 49	3.32 mA sink to Ground
↑ ICLK to ↓ CSIO	6.8 ns @ Pin 49	-4.81 mA source to +4.81 V

Figure 4-4 is a typical ID read cycle of IPA = 0x00 using Systran's HP Logic Analyzer Toolkit, Type 1 (Systran part number BKDM-TKHPLA1) on the TRIDO48.

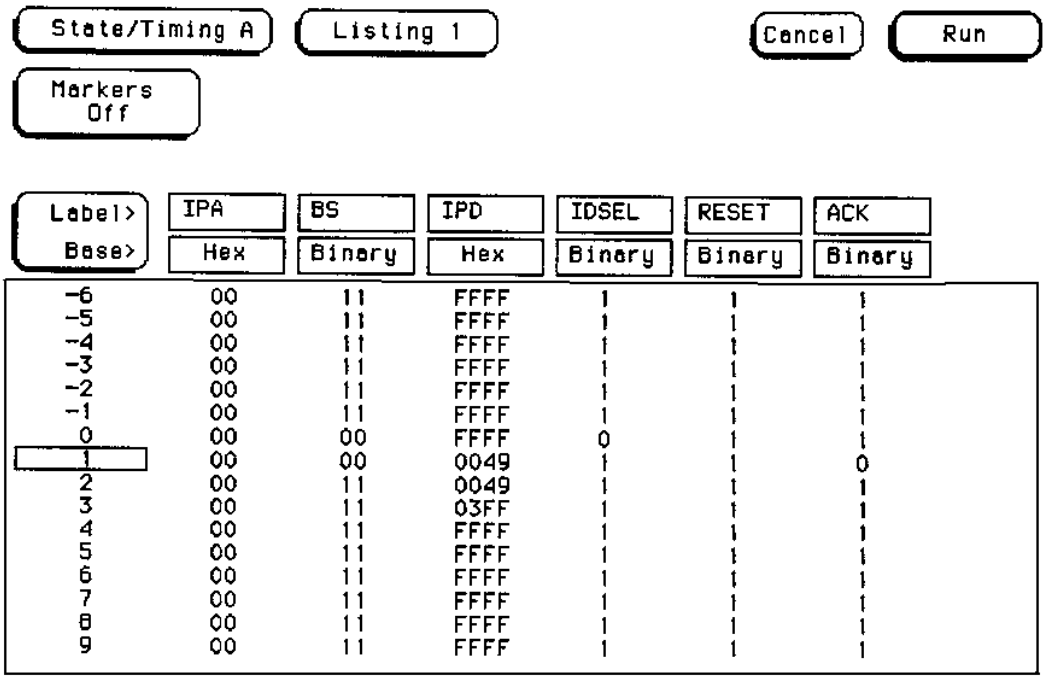


Figure 4-9 Typical State Timing Diagram

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APPENDIX A

SPECIFICATIONS

A.1 Specifications

HARDWARE COMPATIBILITY ..... American National Standard For IP Modules (ANSI/VITA 4-1995

MECHANICAL

Measurements ---------- 1.8000″ x 3.900″ x 0.303″ (above board), 4.572 x 9.906 x 0.770 cm
Weight ---------- 0.992 oz., 28.12 grams
Board thickness ---------- 0.062″, 0.157 cm, nominally, (4 layers)

PROTOCOL

Clock Rate ---------- 8 MHz
Wait Cycles ---------- None on any transfer types
Hold Cycles---------- Supported on all valid transfer types
Address Decoding ---------- Complete (no partial)
I/O transfers
- Writes ---------- 8-bit, 16-bit
- Reads ---------- 16-bit
- 16-bit registers ---------- Four (three for ports, one for control/status)
- Maximum read/write rate ---------- 4 MTransfers/second, sustained

ID transfers
- Read (only) ---------- 8-bit
- Zero-fill---------- Zero-fill on upper byte
- Data ---------- Twelve bytes, including Cyclic Redundancy Check (CRC)
- Systran manufacturer's ID---------- 0x45, = E ASCII
- TRIDO48's model number ---------- 0x62, = b ASCII
- CRC value ---------- 0xC7
- Maximum read rate ---------- 4 MTransfers/second, sustained

Memory transfers---------- Not supported
Interrupt vector transfers---------- Not supported
Interrupt requests ---------- None generated
DMA activity ---------- Not supported
Acknowledgement on
unsupported transfer attempts---------- None generated
- Memory read and write
- Interrupt read
- ID write, and addresses beyond those needed for valid transfers

POWER REQUIREMENTS

Power ---------- +5 Vdc at 119 mA (typical, no I/O loads)

PERFORMANCE CHARACTERISTICS

Electrical characteristics ---------- Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS

Supply voltage with respect to ground -- -0.5 V minimum, +7.0 V maximum
I/O port signals' voltage---------- -0.3 V minimum, +7.0 V maximum

RECOMMENDED OPERATING CONDITIONS

Supply voltage ---------- +4.75 V to +5.25 V

"CSIO" as input

Input rise time	40 ns maximum
Input fall time	40 ns maximum
Input voltage range	0 V to supply voltage
Logic interface	ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating)	0°C to +70°C
Temperature (No bias, storage)	-40°C to +150°C
Humidity (Noncondensing)	5% to 95%
Vibration (Operating)	10 G's RMS, 20→2001 Hz, random
Shock (Operating)	50 G's maximum, all axes
Altitude (Operating)	10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MIL-HDBK-217F	1,609,450 hours
Bellcore 332, Issue 6	1,843,288 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

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B.1 Applications

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the TRIDO48 IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 Custom Parallel Bus

Figure B-1 is an application example that is one of many possible configurations for using the TRIDO48 as an important element in the development of parallel communications in the form of a tristateable bus that does not conform to any particular computer or I/O bus specification. Since the TRIDO48 is capable of driving heavy loads, including fairly long ribbon cables exhibiting large capacitance characteristics, it is ideal for an application such as this.

Except for the loading constraints, there should be no reason why many more data sources (than the nine shown) could not be used in a scenario similar to that presented in Figure B-1. Additionally, many more data users (than the one shown) could be used in such a system configuration.



NOTE: The IP Module labeled “DID48" in this application is the Systran model BHAS-DID48 48-channel, discrete input IP Module.

It is recommended that the principle data user also maintain control over the system, including the TRIDO48 that acts as the bus controller. The example also cites the usage of CSIO as being asserted high for enabling the board whose drivers are actively sending data on the bus. This is just one possible scenario since bus-controlled assertions could have been reversed from those shown, or even the slightly more complex version of mixed assertion states could have been used.

Another variation could have included local software control where bus control communications is handled in a less direct form than that depicted.

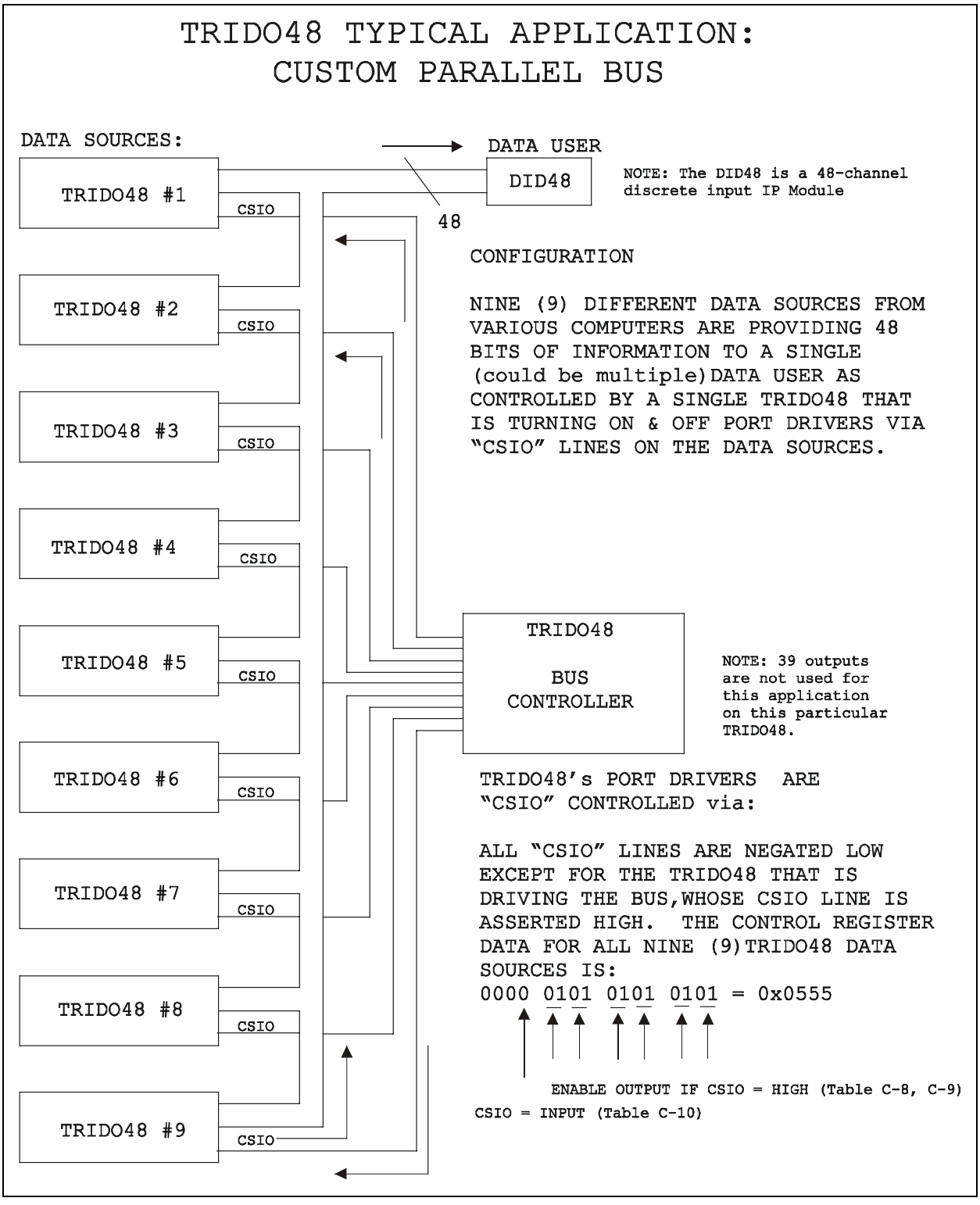


Figure B-1 Custom Parallel Bus

B.3 Seven-Segment Display Driver

Figure B-2 presents a display configuration that is a software programmer's delight. The TRIDO48 provides individual segment control so that special moving effects can be implemented. Full hexadecimal count/notation can be implemented, as well. Since the TRIDO48 is capable of sinking much more current than similar TTL output interface boards, it is also capable of controlling the high-brightness (and higher-current) LEDs. While it may be possible to vary the anodes' supply voltage, it must be done very carefully. Do not to take it so high that the cathodes' voltage exceeds the maximum safe potential that can exist on the port drivers' outputs.

Raising the supply voltage may also permit the LEDs to be slightly ON all the time. And if the LED's supply is taken lower, make sure the reverse voltage for the LEDs being used is not exceeded when the TRIDO48's outputs are in their high states (about +4 volts).

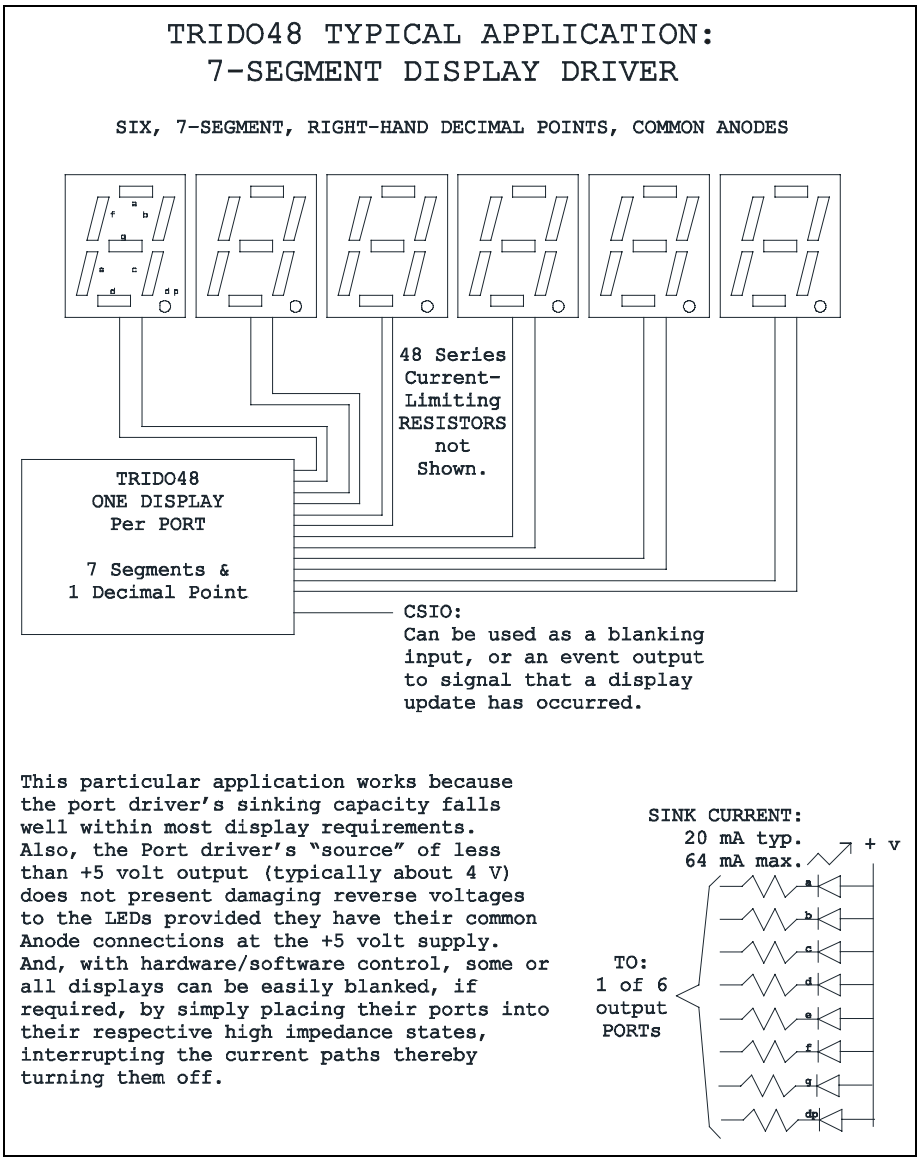


Figure B-2 Seven-Segment Display Driver

B.4 Sixteen-Segment Display Driver

Figure B-3 provides the natural extension from the seven-segment display driver application presented in Figure B-2

The significant differences are that these displays are capable of far more graphic representations (typically 64 characters), and there are not enough segment drivers to include decimal points. If the software code-writers liked Figure B-2, they are going to love this one. The final extension to figures B-2 and B-3 would be an application involving the common 5-by-7 dot matrix displays. This, of course, would utilize 35 (37 if you count left and right decimal points) drivers from a single TRIDO48. While some applications are possible; they may not always be practical.

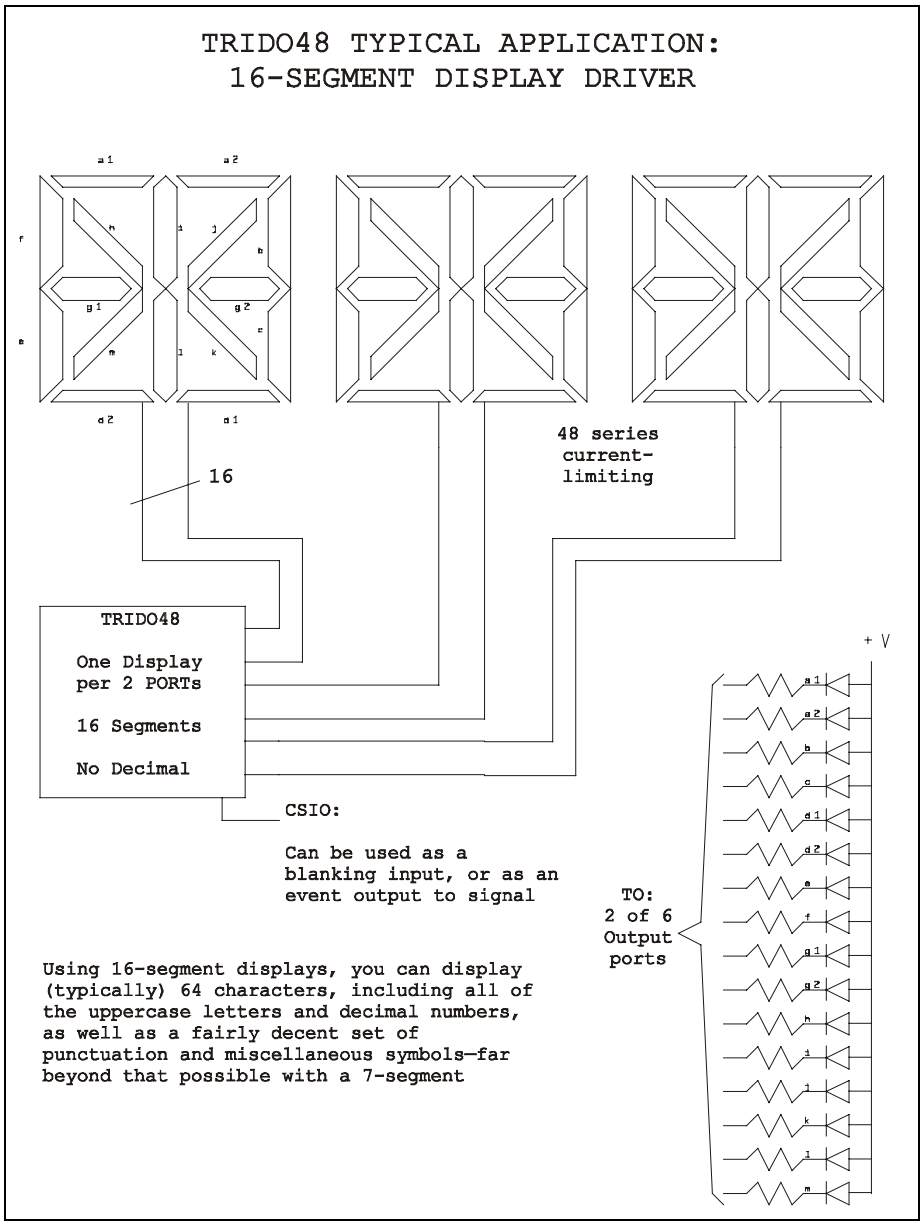


Figure B-3 Sixteen-Segment Display Driver

B.5 48 ER/SSR Relays

The I/O connector pinout on the TRIDO48 was selected to match the I/O pinouts found on many common digital I/O interface boards that are specifically designed to reside only in a Personal Computer. Figure B-4 (and Figure B-5) provide the most obvious reason why. There are many termination panels and external relay board options from other vendors that directly connect to the TRIDO48. This allows the interface selection of your choice, without being bound to a sole-source.

Figures B-4 and B-5 present applications where 48 electromechanical relays and 48 solid-state relays, respectively, are controlled by a single TRIDO48 IP Module.

Not shown is the possible configuration of having one each of the 24 relay-rack types, with either type being the first board in the daisy-chain configuration. As with most termination panels, these relay boards are large (17" by 4.5") and are mounted in metal enclosures or closets where most cable plant transitions take place. Because of the extra-drive capabilities of the TRIDO48 IP Module, the ribbon-cable connection can be further from the termination interface equipment than most similar TTL I/O interface boards can provide.

The plug-in relays depicted in Figure B-5 are standard devices from many sources, and include many other ranges than those presented in the diagram. An AC output solid-state relay will complete an AC circuit when the TRIDO48 board signal to the SSR is low. The AC circuit through the SSR will be open when the signal from the TRIDO48 is high. The significant advantage of the SSR usage is that the high voltage that may be present in either an AC or DC format never reaches the TRIDO48 because it is protected (isolated) by the SSR devices (up to 4,000 VAC).

Applications for both board formats include the ability to start small motors, switch large capacity motor-starter relays, electric appliances, turn on and off equipment of all types, valves, alarms, annunciator beacons and lights, etc.

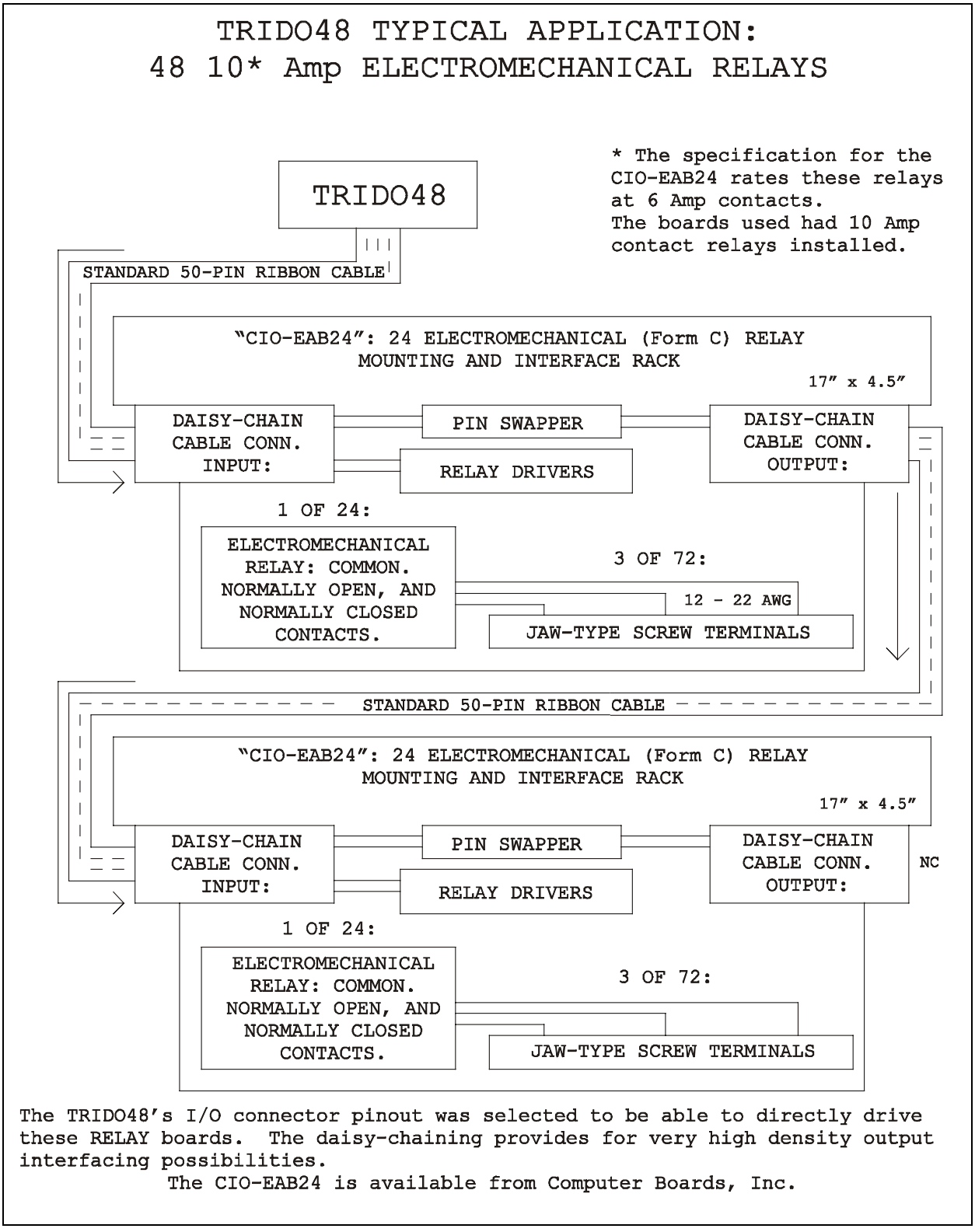


Figure B-4 48 10 Amp Electromechanical Relays

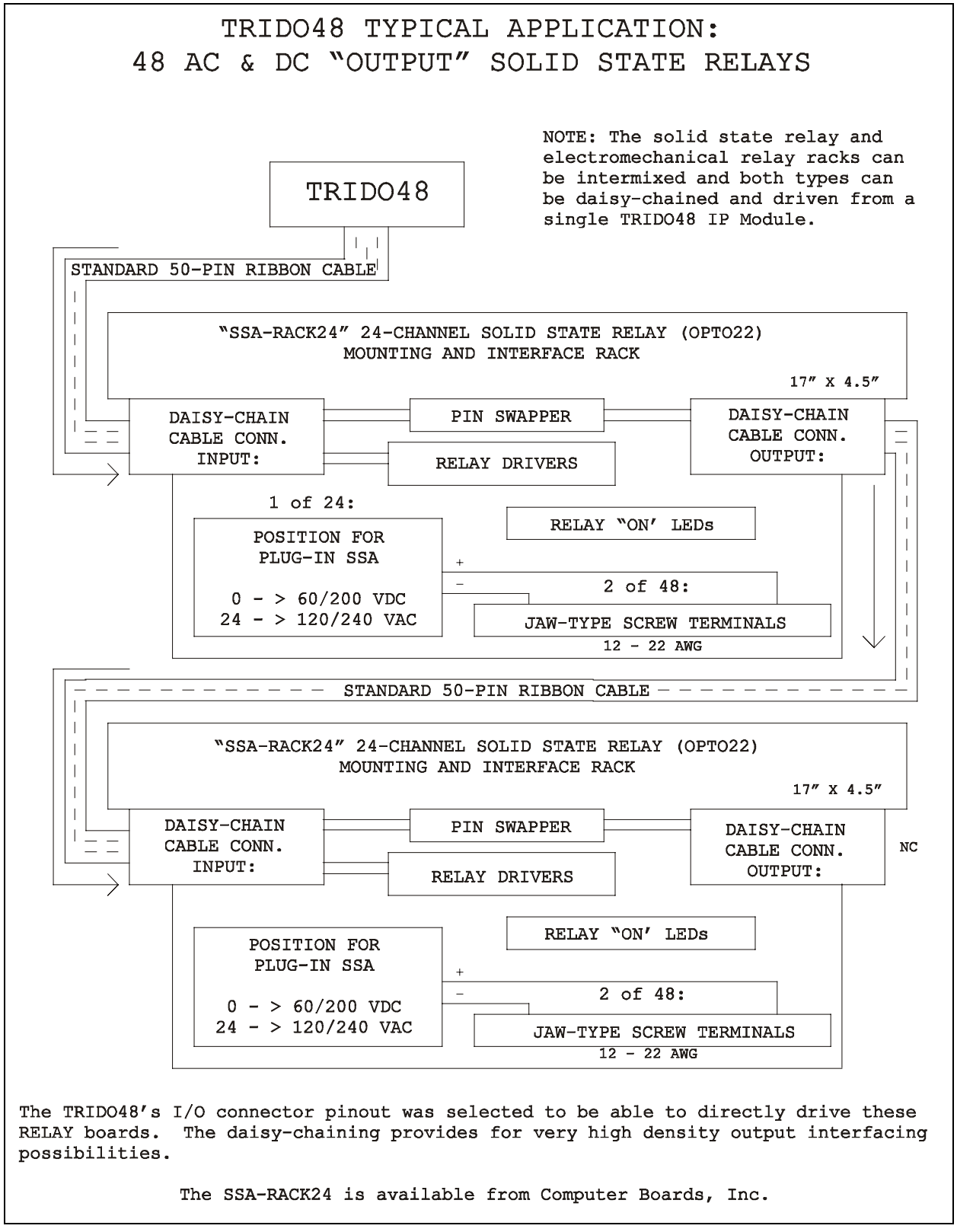


Figure B-5 48 AC and DC "Output" Solid-state Relays

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APPENDIX C

PROGRAMMING GUIDE

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C.1 Overview

This section of the manual describes the operation of the TRIDO48 from the software perspective, detailing the TRIDO48 registers and providing programming examples. A more detailed description of the hardware can be found in Chapter 2, PRODUCT OVERVIEW, and in Appendix B, TYPICAL APPLICATIONS.

C.2 Description

The TRIDO48 is a simple to use, tristateable, 48-channel, digital output card. The output-enable can be either hardware controlled via the CSIO signal or software controlled by user selection on byte boundaries. If hardware output-enable control is used, the polarity of the CSIO input logic can be further selected. If the CSIO line is not used for output-enable control, it may be configured as an output signal that generates a 125 ns pulse when selected ports are updated. Also, the default output-enable power-up state is switch-selectable.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IP Module to provide “no-wait” read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) results in no acknowledgement, and its subsequent bus-timeout error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

The TRIDO48 emulated ID Address Space PROM listing is shown in Table C-1.

Table C-1 TRIDO48 ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII “I”	0x49
IPA = 0x01	ASCII “P”	0x50
IPA = 0x02	ASCII “A”	0x41
IPA = 0x03	ASCII “C”	0x43
IPA = 0x04	Systran’s ID	0x45
IPA = 0x05	TRIDO48’s Model Number	0x62
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0xC7

C.4 IP Module IO Address Map

The TRIDO48’s I/O Address Map (Table C-2), containing the data ports, control registers, and interrupt registers of the TRIDO48, was designed with efficiently located data and control/status registers in the IP Module I/O space (IPA = 00 ⇒ 0x03*)*.



NOTE: The address detector circuitry is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x04 results in no acknowledgement and its subsequent bus-timeout error on the carrier where this IP Module resides.

Table C-2 TRIDO48 I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	Data Port 1	Data Port 0	Data Register 0 = Ports 1&0, 8-bits each
IPA = 0x01	Data Port 3	Data Port 2	Data Register 1 = Ports 3&2, 8-bits each
IPA = 0x02	Data Port 5	Data Port 4	Data Register 2 = Ports 5&4, 8-bits each
IPA = 0x03	[15:13]		Control Register 0, Bits 15-13 Config. CSIO Signal = 000 Pulse on Port 0 Update = 001 Pulse on Port 1 Update = 010 Pulse on Port 2 Update = 011 Pulse on Port 3 Update = 100 Pulse on Port 4 Update = 101 Pulse on Port 5 Update = 110 Pulse on any Port Update = 111 CSIO always High
	[12]		Bit 12 Controls the CSIO signal 0=Input, 1=Output
	[11	: 0]	Bits 11-0 Control the Output Enables in pairs for Ports 5 thru 0*, 00 = Port Outputs Disabled 01 = Port Outputs Enabled if CSIO = High 10 = Port Outputs Enabled if CSIO = Low 11 = Port Outputs Enabled

* i.e. Bits [11:10] for port 5, [9:8] for port 4, ... , and [1:0] for port 0

On power-up, all 48 data bits defined in following paragraphs are cleared to a zero-state, which is a logic-low (near ground potential) on the I/O connector's port lines, provided DOES = 1 (outputs are on).

The first location (IPA = 0x00) is the write-and-read-back Data Register 0 for the output ports 0 and 1. Port 0 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 1 resides on byte-lane 1 such that accesses occur on IPD[15:8]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 8-bit writes to byte-lane 1 only, 16-bit writes to both byte-lanes simultaneously, and 16-bit reads of both byte-lanes simultaneously.

The second location (IPA = 0x01) is the write-and-read-back Data Register 1 for the output ports 2 and 3. Port 2 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 3 resides on byte-lane 1 such that accesses occur on IPD[15:8]. Valid accesses to

and from this location include: 8-bit writes to byte-lane 0 only, 8-bit writes to byte-lane 1 only, 16-bit writes to both byte-lanes simultaneously, and 16-bit reads of both byte-lanes simultaneously.

The third location (IPA = 0x02) is the write-and-read-back Data Register 2 for the output ports 4 and 5. Port 4 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 5 resides on byte-lane 1 such that accesses occur on IPD[15:8]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 8-bit writes to byte-lane 1 only, 16-bit writes to both byte-lanes simultaneously, and 16-bit reads of both byte-lanes simultaneously.

The fourth location (IPA = 0x03) is the write-and-read-back Control Register for the control and status register (referred to as CR, and CR bits as CR# or CR[#:#]). There are eight (8) functional groupings of these bits that are defined in the following paragraphs.

C.4.1 Port 0 Control

Control bits 1 and 0 (CR[1:0]) determine the high versus low-impedance states of the output drivers for port 0.

For the bit combination of CR[1:0] = 00, the port 0 drivers are disabled (placed in a high-impedance state). This causes them to float, so another TRIDO48 IP Module board sharing the data lines in a bussed configuration can be subsequently enabled for driving the port lines.

For the bit combination of CR[1:0] = 01, the port 0 drivers are enabled (placed in a low-impedance state or turned on) if the CSIO signal line is driven to its logic-high state, and disabled if the CSIO input is driven to its logic-low state.

For the bit combination of CR[1:0] = 10, the drivers are disabled if the CSIO control input is driven to its logic-high state, and enabled if the CSIO input is driven to its logic-low state.

For the bit combination of CR[1:0] = 11, the output drivers are constantly enabled.

This bit mapping provides all possible combinations of software control (CR[1:0] = 00 or 11) and with complete hardware control with “sense” selection (CR[1:0] = 01 or 10) such that port enabling can be accomplished via hardware logic high or low states. The latter two combinations also provide the least significant bit of decoding for bus-enabling operations. A pair of ports on the same or different TRIDO48 IP Modules sharing common port lines can be inversely enabled and disabled simultaneously with a single CSIO control line as determined by CR[1:0] = 01 or = 10.

On power-up, CR[1:0] = 00 if the DOES switch = 0 (port 0 outputs OFF), and CR[1:0] = 11 if the DOES switch = 1 (port 0 outputs ON).

C.4.2 Port 1 Control

Control bits 3 and 2 (CR[3:2]) determine the high versus low-impedance states of the output drivers for port 1. For CR[3:2] = 00 the port 1 drivers are turned off. For CR[3:2] = 01, the drivers are enabled if CSIO is in a high state, and disabled if CSIO is in a low state. For CR[3:2] = 10, the drivers are disabled if CSIO is in a high state, and enabled if CSIO is in a low state. If CR[3:2] = 11, then the port 1 drivers are enabled.

On power-up, CR[3:2] = 00 if the DOES switch = 0, and CR[3:2] = 11 if the DOES switch = 1.

C.4.3 Port 2 Control

Control bits 5 and 4 (CR[5:4]) determine the high versus low-impedance states of the output drivers for port 2. For CR[5:4] = 00 the port 2 drivers are turned off. For CR[5:4] = 01, the drivers are enabled if CSIO is in a high state, and disabled if CSIO is in a low state. For CR[5:4] = 10, the drivers are disabled if CSIO is in a high state, and enabled if CSIO is in a low state. If CR[5:4] = 11, then the port 2 drivers are enabled.

On power-up, CR[5:4] = 00 if the DOES switch = 0, and CR[5:4] = 11 if the DOES switch = 1, for disabling and enabling port 2 drivers, respectively.

C.4.4 Port 3 Control

Control bits 7 and 6 (CR[7:6]) determine the high versus low-impedance states of the output drivers for port 3. For CR[7:6] = 00 the port 3 drivers are turned off. For CR[7:6] = 01, the drivers are enabled if CSIO is in a high state, and disabled if CSIO is in a low state. For CR[7:6] = 10, the drivers are disabled if CSIO is in a high state, and enabled if CSIO is in a low state. If CR[7:6] = 11, then the port 3 drivers are enabled.

On power-up, CR[7:6] = 00 if the DOES switch = 0, and CR[7:6] = 11 if the DOES switch = 1, for disabling and enabling port 3 drivers, respectively.

C.4.5 Port 4 Control

Control bits 9 and 8 (CR[9:8]) determine the high versus low-impedance states of the output drivers for port 4. For CR[9:8] = 00 the port 4 drivers are turned off. For CR[9:8] = 01, the drivers are enabled if CSIO is in a high state, and disabled if CSIO is in a low state. For CR[9:8] = 10, the drivers are disabled if CSIO is in a high state, and enabled if CSIO is in a low state. If CR[9:8] = 11, then the port 4 drivers are enabled.

On power-up, CR[9:8] = 00 if the DOES switch = 0, and CR[9:8] = 11 if the DOES switch = 1, for disabling and enabling port 4 drivers, respectively.

C.4.6 Port 5 Control

Control bits 11 and 10 (CR[11:10]) determine the ON versus OFF states of the output drivers for port 5. For CR[11:10] = 00 the port 5 drivers are turned off. For CR[11:10] = 01, the port 5 drivers are enabled if CSIO is in a high state, and disabled if CSIO is in a low state. For CR[11:10] = 10, the port 5 drivers are disabled if CSIO is in a high state, and enabled if CSIO is in a low state. If CR[11:10] = 11, then the port 5 drivers are turned on.

On power-up, CR[11:10] = 00 if the DOES switch = 0, and CR[11:10] = 11 if the DOES switch = 1, for disabling and enabling port 5 drivers, respectively.

C.5 CSIO Function Select

The control/status input/output handshake line acts primarily as a control input, and can serve as a status output if (and only IF) it is not needed as an input-control line. The bit combinations at CR[11:10], CR[9:8], CR[7:6], CR[5:4], CR[3:2], and CR[1:0] determine whether CSIO is needed for control input. If any of these pairs of bits have a bit pattern of '01' or '10' written into their registers, then CSIO is needed as a control input. If all of the port-enabling bit pairs have either '00' or '11' in their registers, then CSIO is not needed as an input and can be used as a STATUS OUTPUT signal.

The CSIO line does not automatically turn into an output-status line when it is not needed as an input-control signal. The user must deliberately write a logic one into CR[12] to turn the CSIO line into an output signal. If CR[11:0] needs CSIO as an input signal, an attempted write of a one into CR[12] will be bit-blocked (a valid I/O write transfer does take place), and CR[12] will remain a logic zero (denoting CSIO as an input).

Once CR[12] = 1, the output functionality of the CSIO signal is defined by CR[15:13].

The following possible scenarios illustrate the real-time manipulation of CR[12] and describe its operation:

- Assume that a TRIDO48 is powered-up and ready for use in its default condition (DOES = 1; all outputs ON). CR[12] has been set by a byte-lane 1 write and CR[15:13] are also set to a desired pattern (any pattern is valid for this application). During the use of this board, the application software decides that it needs to use CSIO as an input for a special usage of ports 1 and 0. A single byte-lane 0 write to CR[3:0] (actually CR[7:0]) can be performed to establish CSIO as an input. The hardware sequence controller logic for CR[12] will automatically convert this register's state from being set (a logic one) to being cleared (a logic zero) which converts CSIO from an output signal to a control input signal. A subsequent read of the control register would verify that CR[12] is now = 0.
- Given the final state of the previous example as a starting point, the following description provides the path required to convert the CSIO line for an input function to an output function. Unlike the previous example, where a single write establishes both the need and the conversion of CSIO from an output to an input, two write operations are required to convert CSIO from an (needed) input to an output. Note that this is true only if CSIO is needed as an input control signal for port-enable bit patterns of '01' or '10' in CR[11:0]. The first control register write must clear or set both bits in the port-enable bit pairs (to '00' or '11'). Only then can a second write be executed that will successfully set bit CR[12], turning CSIO into an output signal. Recall that an attempt to set bit CR[12] is bit-blocked if, during the write attempt, the CSIO is currently needed for an input-control signal in support of port-enabling functions.

C.6 Status Outputs

Once the CR[12] is successfully set, the CSIO is established as a status output (as opposed to a control input). The operation of this output signal is determined by one of eight possible bit combinations that are registered at CR[15:13]. These bit functions serve no purpose if CR[12] = 0.

For CR[15:13] = 000, the CSIO line will normally be at a logic-zero state. A 125 ns (logic-high) pulse will occur during the ICLK period following the termination cycle of a write transfer to port 0, regardless of whether it was a single or double byte access.

For CR[15:13] = 001, the CSIO line will normally be at a logic-zero state. A 125 ns (logic-high) pulse will occur during the ICLK period following the termination cycle of a write transfer to port 1, regardless of whether it was a single or double byte access.

For CR[15:13] = 010, the CSIO line will normally be at a logic-zero state. A 125 ns (logic-high) pulse will occur during the ICLK period following the termination cycle of a write transfer to port 2, regardless of whether it was a single or double byte access.

For CR[15:13] = 011, the CSIO line will normally be at a logic-zero state. A 125 ns (logic-high) pulse will occur during the ICLK period following the termination cycle of a write transfer to port 3, regardless of whether it was a single or double byte access.

For CR[15:13] = 100, the CSIO line will normally be at a logic-zero state. A 125 ns (logic-high) pulse will occur during the ICLK period following the termination cycle of a write transfer to port 4, regardless of whether it was a single or double byte access.

For CR[15:13] = 101, the CSIO line will normally be at a logic-zero state. A 125 ns (logic-high) pulse will occur during the ICLK period following the termination cycle of a write transfer to port 5, regardless of whether it was a single or double byte access.

For CR[15:13] = 110, the CSIO line will normally be at a logic-zero state. A 125 ns (logic-high) pulse will occur during the ICLK period following the termination cycle of a write transfer to any of the ports, regardless of whether it was a single or double byte access.

For CR[15:13] = 111, the CSIO line will always be at a logic-high state. This last function was included to emulate the state of +5 Vdc being delivered to pin 50 by many of the PC-based digital I/O cards, whose pinout the TRIDO48 matches. This “signal” should not be used as a power source for external logic.

C.7 Word Access Address Translation

Table C-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, the word BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VMEbus Address	PC-AT Bus Address	NuBus Address	IP Module Address
BASE + 0x00	BASE + 0x00	BASE + 0x02	IPA = 0x00
BASE + 0x02	BASE + 0x02	BASE + 0x06	IPA = 0x01
BASE + 0x04	BASE + 0x04	BASE + 0x0A	IPA = 0x02
BASE + 0x06	BASE + 0x06	BASE + 0x0E	IPA = 0x03
BASE + 0x08	BASE + 0x08	BASE + 0x12	IPA = 0x04
BASE + 0x0A	BASE + 0x0A	BASE + 0x16	IPA = 0x05
BASE + 0x0C	BASE + 0x0C	BASE + 0x1A	IPA = 0x06
BASE + 0x0E	BASE + 0x0E	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B

C.8 Byte Access Address Translation

Table C-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, the word BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VMEBus Address	PC-AT Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 0x01	BASE + 0x00	BASE + 0x03	IPA = 0x00	0
BASE + 0x00	BASE + 0x01	BASE + 0x02	IPA = 0x00	1
BASE + 0x03	BASE + 0x02	BASE + 0x07	IPA = 0x01	0
BASE + 0x02	BASE + 0x03	BASE + 0x06	IPA = 0x01	1
BASE + 0x05	BASE + 0x04	BASE + 0x0B	IPA = 0x02	0
BASE + 0x04	BASE + 0x05	BASE + 0x0A	IPA = 0x02	1
BASE + 0x07	BASE + 0x06	BASE + 0x0F	IPA = 0x03	0
BASE + 0x06	BASE + 0x07	BASE + 0x0E	IPA = 0x03	1
BASE + 0x09	BASE + 0x08	BASE + 0x13	IPA = 0x04	0
BASE + 0x08	BASE + 0x09	BASE + 0x12	IPA = 0x04	1
BASE + 0x0B	BASE + 0x0A	BASE + 0x17	IPA = 0x05	0
BASE + 0x0A	BASE + 0x0B	BASE + 0x16	IPA = 0x05	1
BASE + 0x0D	BASE + 0x0C	BASE + 0x1B	IPA = 0x06	0
BASE + 0x0C	BASE + 0x0D	BASE + 0x1A	IPA = 0x06	1
BASE + 0x0F	BASE + 0x0E	BASE + 0x1F	IPA = 0x07	0
BASE + 0x0E	BASE + 0x0F	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

*Byte-lane 1 is not applicable for ID Space

C.9 Register Definitions

The TRIDO48 has four 16-bit wide registers: three data and one control. The data registers may be viewed as either three 16-bit (two data ports each) or six 8-bit ports. The single control register allows user selection of output-enable control and port update trigger control. Byte writes to any of these registers are non-destructive to adjacent bytes. The registers are described in detail in this section. The data register bit descriptions are shown in the associated tables.



NOTE: In the "RW" row, "R" indicates read only, "W" indicates write only, and "RW" indicates both read and write bit operations.

C.9.1 Data Register 0 (IPA = 0x00)

This 16-bit read/write register is the data register for the 8-bit wide ports 0 and 1. These two 8-bit ports can also be viewed as a single 16-bit register. Writing to this register sets the output value of the ports. When read, the register returns the current value of the ports. On power-up, all bits are set to 0.

Table C-5 Data Register 0 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.

C.9.2 Data Register 1 (IPA = 0x01)

This 16-bit read/write register is the data register for the 8-bit wide output ports 2 and 3 with port 3 in byte-lane 1 and port 2 in byte-lane 0. These two 8-bit ports can also be viewed as a single 16-bit register. Writing to this register sets the output value of the ports. When read, the register returns the current value of the ports. On power-up, all bits are set to 0.

Table C-6 Data Register 1 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pn7- Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.

C.9.3 Data Register 2 (IPA = 0x02)

This 16-bit read only register is the data register for the 8-bit wide input ports 4 and 5 with port 5 in byte-lane 1 and port 4 in byte-lane 0. These two 8-bit ports can also be viewed as a single 16-bit register. Writing to this register sets the output value of the ports. When read, the register returns the current value of the ports. On power-up, all bits are set to 0.

Table C-7 Data Register 2 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

C.9.4 CR0 Output Enable Control Register (IPA = 0x03)

This 16-bit wide read/write register selects the output-enable control and the CSIO output pulse mode. The output-enable control can be selected on 8-bit port boundaries. The CSIO line can be used to generate a 125 ns output pulse when a port is updated. However, this option is only available if CSIO is not being used as an output-enable control gate. The power-up default state of the output-enable bits (OE1-OE0) take on the value of the DOES (default output enable state) switch.

Table C-8 Control Register Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	OP2	OP1	OP0	I/O	P50EI	P50E0	P40E1	P40E0	P30E1	P30E0	P20E1	P20E0	P10E1	P10E0	P00E1	P00E0
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	DOES	DOES	DOES	DOES	DOES	DOES	DOES	DOES	DOES	DOES	DOES	DOES

DOES = Default Output Enable State

Table C-9 0E1 - 0E0: Output Enable Control Bits

OE1	OE0	Output Enable Selection
0	0	Outputs disabled (regardless of CSIO state; that is, software control)
0	1	Outputs enabled if CSIO is high, disabled if CSIO is low
1	0	Outputs enabled if CSIO is low, disabled if CSIO is high
1	1	Outputs enabled (regardless of CSIO state; that is, software control)

Table C-10 I/O: CSIO Input/Output Control Bit

I/O	CSIO Input/Output Selection
0	CSIO is an input. It can be used as an output enable control line.
1	CSIO is an output. This can only be selected if CSIO is not being used as an input for controlling the output enable of a port.

Table C-11 OP2 - OP0: CSIO Output Pulse Control Bits

OP2	OP1	OP0	Output Pulse Mode Selection
0	0	0	CSIO pulse out on port 0 update (I/O bit, CR bit 12, must be high)*
0	0	1	CSIO pulse out on port 1 update (I/O bit must be high)*
0	1	0	CSIO pulse out on port 2 update (I/O bit must be high)*
0	1	1	CSIO pulse out on port 3 update (I/O bit must be high)*
1	0	0	CSIO pulse out on port 4 update (I/O bit must be high)*
1	0	1	CSIO pulse out on port 5 update (I/O bit must be high)*
1	1	0	CSIO pulse out on any register update (I/O bit must be high)*
1	1	1	CSIO output high (I/O bit must be high)*

* The pulse will occur for byte- or word-writes to these ports.

C.10 Programming Examples

The following examples illustrate how to program the TRIDO48 to achieve the various possible operational modes. It is assumed that the DOES switch is set to 0 (the power- up state of the output-enable control bits will be 00, outputs disabled, for all ports).

C.10.1 Software Output Enable Control Examples

This example illustrates software output-enable control. In this example the output-enable control for all the ports are set the same, however, each 8-bit port can be individually controlled.

- At power-up, the data registers are all cleared (value of 0x0000).
- Assuming DOES = 0, the control register is cleared (value of 0x0000).
- At this point, the outputs are in the high-impedance state because the outputs are disabled.
- Write 0x0FFF to the control register. The outputs should now reflect the value of the data registers (all zeros).
- Write any value to the data registers. The outputs should reflect the value of the data registers.
- Write ‘0x0000’ to the control register. The outputs are in the high-impedance state because the outputs are disabled.

C.10.2 Hardware (CSIO) Output Enable Control Example

This example illustrates hardware output-enable control via the CSIO input line. In this example the output-enable control for all the ports are set the same, however, each 8-bit port can be individually controlled.

- At power up, the data registers are all cleared (value of 0x0000).
- Assuming DOES = 0, the control register is cleared (value of 0x0000).
- At this point, the outputs are in the high-impedance state because the outputs are disabled.
- Write '0x0555' to the control register. The outputs will now be enabled when CSIO is high.
- Set the CSIO signal input high. The outputs should now reflect the value of the data registers.
- Set the CSIO signal input low. The outputs are in the high-impedance state because the outputs are disabled.
- Write '0x0AAA' to the control register. The outputs will now be enabled when CSIO is low.
- Set the CSIO signal input low. The outputs should now reflect the value of the data registers.
- Set the CSIO signal input high. The outputs are in the high-impedance state because the outputs are disabled.
- Write '0x0000' to the control register. The outputs are in the high-impedance state because the outputs are disabled.

C.10.3 CSIO Output Pulse Example

This example illustrates how the TRIDO48 can be configured to generate a 125 ns output pulse on the CSIO line when the selected port is updated. The output pulse occurs whether the outputs are enabled or disabled. CSIO can be configured as output only if it is not programmed to be used as an output-enable control input. The following example only modifies bits 15-12 of the control register while leaving bits 11-0 of the control register zeros. Any pair of these output-enable control bits (port n OE1-OE0) could also have a value of '11' binary when CSIO is being used as an output.

- At power-up, the data registers are all cleared (value of 0x0000).
- Assuming DOES = 0, at power up, the control register is cleared (value of 0x0000).
- Write '0x1000' to the control register. Any write to 8-bit port 0 will now generate a 125 ns output pulse on the CSIO line.
- Write '0x3000' to the control register. Any write to 8-bit port 1 will now generate a 125 ns output pulse on the CSIO line.
- Write '0x5000' to the control register. Any write to 8-bit port 2 will now generate a 125 ns output pulse on the CSIO line.
- Write '0x7000' to the control register. Any write to 8-bit port 3 will now generate a 125 ns output pulse on the CSIO line.
- Write '0x9000' to the control register. Any write to 8-bit port 4 will now generate a 125 ns output pulse on the CSIO line.
- Write '0xB000' to the control register. Any write to 8-bit port 5 will now generate a 125 ns output pulse on the CSIO line.
- Write '0xD000' to the control register. Any write to any register will now generate a 125 ns output pulse on the CSIO line.
- Write '0xF000' to the control register. The CSIO output is high.
- Write '0x0000' to the control register. The outputs are in the high-impedance state because the outputs are disabled.

GLOSSARY

[x:y] ---------- Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane ---------- Eight bits of a data bus on octal boundaries.

CAE ---------- Computer Aided Engineering.

CSIO ---------- control Status Input/Output handshake line.

DMA ---------- Direct Memory Access.

DOES ---------- Default Output-Enable State.

DPDT ---------- Double pole, double throw switch.

doublewide ---------- An IP Module that is twice the size of a singlewide board.

EPLD ---------- Erasable Programmable Logic Device.

ID PROM ---------- The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

I/O ---------- Input/Output.

IP Module ---------- Refers to the ANSI/VITA 4-1995 specification.

IP Module logic bus ---------- A synchronous, 4 MTransfers/sec, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

IPDbus ---------- IP Module Data Bus.

ISR ---------- Interrupt Service Routine.

MTBF ---------- Mean Time Between Failures.

net ---------- Schematic wire or node connection.

ns, µs, ms ---------- Nanoseconds, microseconds, and milliseconds respectively.

PC ---------- Personal Computer.

PCB ---------- Printed Circuit Board.

PROM ---------- Programmable Read Only Memory

QSOP ---------- Quarter-sized Small Outline Package.

singlewide ---------- An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

slew rate ---------- The rate of change in analog output in terms of volts/time.

SPST ---------- Single-pole, single-throw switch.

tristate ---------- To place in high impedance.

VHDL ---------- Very high-speed integrated circuit Hardware Description Language.

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