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User Guide

Power MIDAS C5000 Series
Single Board Computer

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Preface

Introduction

The VMETRO MIDAS C5000 series is a single-board computer (SBC) built in a 6U CompactPCI form factor based on the AMCC PPC440GX PowerPC processor. This document describes the C5000 hardware.

The chapters are summarized below:

- Product Overview: provides a brief description of the C5000.
- Installation and Hardware description: Installation procedures.
- Processor Subsystem: Describes the system surrounding Processor.
- PMC Subsystem
- CompactPCI Interface
- Miscellaneous Functions: information on JTAG Chain, Reset Network, Interrupt Routing, Power Supplies.
- Appendixes cover reference material for:
    - C5000 Capabilities relating to PICMG Specifications
    - PLD Registers
    - CompactPCI Pinout
    - PMC Connector Pinout
    - MBTF Values
    - Ordering Information, Technical Support, References

Style Conventions Used



Warning! Indicates important information that can affect the operation of your C5000

Note – This is information that will help you get the best performance.

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IEC Prefixes for binary multiples

Symbol	Name	Origin	Derivation	Size
Ki	Kibi	Kilo binary	kilo	1024 bytes
Mi	Mebi	Mega binary	mega	1 048 576 bytes
Gi	Gibi	Gig binary	giga	1 073 741 824 bytes

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Technical Support

Please see the section Technical Support at the end of this guide.

Related Documentation

We recommend reading the documentation in the order shown.

- User Guide (This document)
- Release Notes
- C5000 BSP User Guide.
- MIDAS Monitor User Guide

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Product Overview

The C5000 series is part of the next generation of boards in the MIDAS family. As for the previous generations, the C5000 series focuses on high-performance data buffering and flexible data flows between I/O ports. I/O ports are provided through front panel connectors and CompactPCI J1, J2 and J3 backplane connectors. Additional features are available on a RTM (Rear Transmission Module) board, which is connected to the C5000 through J3 and J5 backplane connectors.

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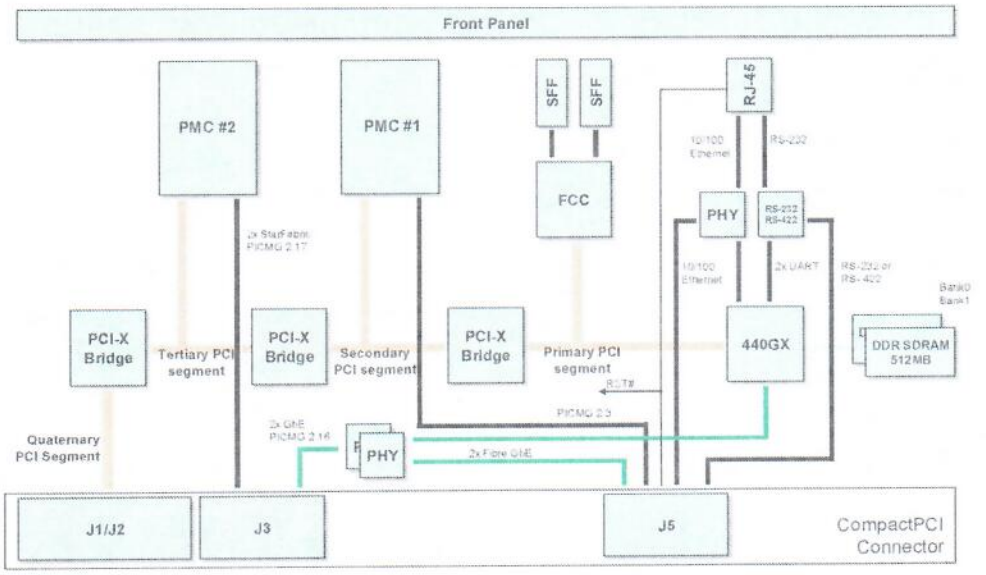
1.1 Main features:

- A PowerPC processor subsystem (440GX from AMCC) with up to 1024MiB local DDR-SDRAM memory and 32MiB of FLASH memory.
- Two standard 3.3V PPMC sites located on separate PCI segments (64-bit, 33/66MHz PCI, 66/100/133MHz PCI-X). In addition, PMC#1 can be MONARCH
- Dual 2Gib Fibre Channel I/O Controller (ISP2312 from QLOGIC) (Optical)
- Single 10/100 Ethernet port (front panel connector)
- One RS-232 port (included in front panel RJ-45 connector)
- One Reset input (included in front panel RJ-45 connector)
- Three PCI(-X)-to-PCI(-X) bridges which connects the different PCI segments together (PLX PCI6540)
- The C5000 can act as Slot one Controller
- Two Gigabit Ethernet ports (Node board) through CompactPCI packet switching backplane on J3 connector
- Two StarFabric links through CompactPCI backplane on J3 connector
- Support of both 3.3V and 5V CompactPCI signaling operation

Following features are provided on RTM (Rear Transition Module) board:

- Two 10/100/1000 Gigabit Ethernet ports (two front panel copper/optical connectors)
- Two StarFabric Interfaces according to PICMG 2.17 (four RJ-45 front panel connectors)
- One 10/100 Ethernet port (RJ-45 connector)
- One RS-232 (or optional one RS-422) port (LEMO connector)
- One PIM I/O board slot, in accordance to VITA36.
- One switch to reset the C5000 and RTM

FIGURE 1-1 *Main Components*



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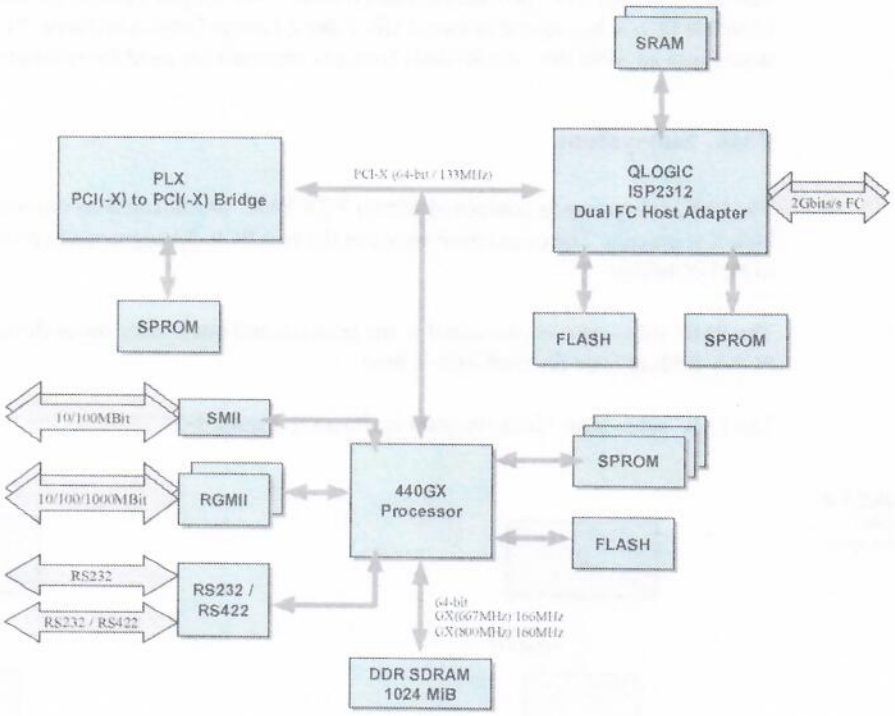
1.2 Main Components

Processor Subsystem

The processor subsystem is built around the AMCC 440GX integrated processor, the QLOGIC ISP2312 dual Fibre Channel I/O Controller and the PCI6540 PCIX-to-PCIX bridge. The Processor Subsystem is located on the Primary PCI segment (PCI-X).

The processor subsystem block diagram is shown in figure Figure 1-2:

FIGURE 1-2
Processor Subsystem



AMCC 440GX Embedded Processor

The AMCC 440GX provides a powerful PowerPC CPU core, a 1024MiB local DDR-SDRAM memory, a 32MiB FLASH memory, two 10/100/1000Mbps Ethernet connections, two 10/100Mbps Ethernet connections and one RS-232 connection or with the RTM board, both RS-232 and RS-422 are available.

Additionally the AMCC 440GX processor provides simple connectivity of additional peripheral devices through an external local bus. This is used for register access to the board PLD.

For debug purposes, JTAG and CPU control signals are provided to a connector for use with WindRivers VisionProbe tools. This allows CPU bring-up and boot before the FLASH is initialized and low-level software debug using the same tool.

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PCI6540 PCIX-to-PCIX Bridge

The PCI6540 provides a 64-bit PCI-X to PCI-X bridge designed for high performance, high availability applications, in PCI-X to PCI-X conversion, bus expansions, frequency conversions from faster PCI-X to slower PCI-X or from slower PCI-X to faster PCI-X bus, address remapping, high availability and universal system-to-system bridging.

The PLX bridge is normally used as a transparent bridge, with its primary interface connected to the Processor PCI-X Segment.

QLOGIC ISP2312 Dual Fibre Channel Host Adapter

The QLOGIC ISP2312 provides a dual-channel Fibre Channel processor which connects the 64-bit/133MHz PCI-X bus to one or two 2 Gib Fibre Channel Fabrics or loops. PCI boot configuration is stored into an SPROM; two SRAMs (one per channel) are used for run-time operations.

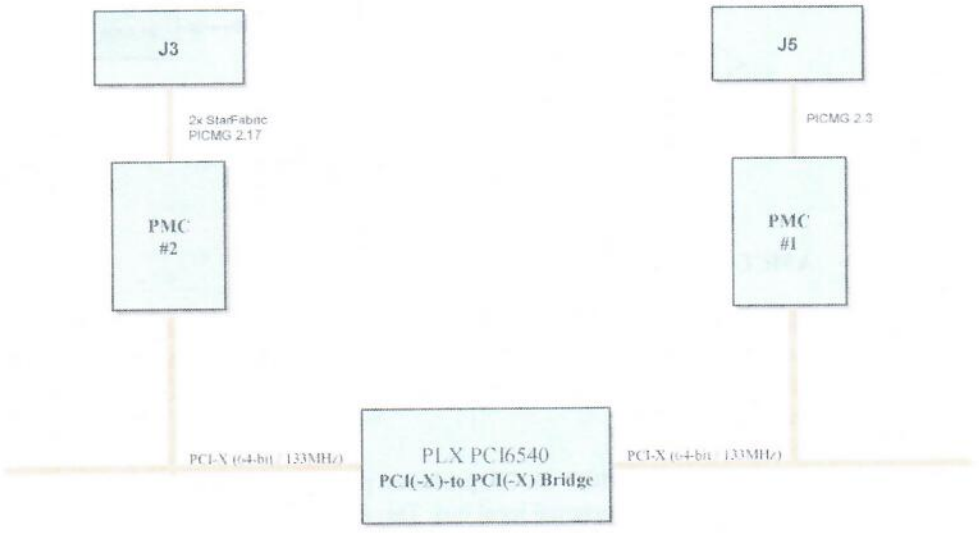
PMC Subsystem

The PMC subsystem is composed of two 3.3V PMC sites located on the Secondary and Tertiary PCI-X segments. The connection between the two PCI(-X) segments is provided by a PLX PCI-X to PCI-X bridge.

The PMC subsystem is connected to the primary and quaternary buses through two PLX PCI-X to PCI-X bridges (one for each PCI-X bus).

The PMC subsystem block diagram is shown in Figure 1-3:

FIGURE 1-3
PMC Subsystem



PMC Support

Each PMC site can operate in any of the following modes:

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- 33MHz, 32/64-bit PCI
- 66MHz, 32/64-bit PCI
- 66MHz, 32/64-bit PCI-X
- 100MHz, 32/64-bit PCI-X
- 133MHz, 32/64-bit PCI-X

PCI-X is supported according to the VITA 39 PCI-X Auxiliary Standard For PMCs and Processor PMCs.

Both PMC sites support either 3.3V or 5V signaling on VIO. The choice is determined by mounting options (resistors and voltage key/pin) and can only be modified by VMETRO. The default setting when shipped is 3.3V. The voltage key must always be mounted in the correct position to avoid severe hardware damage.

Both PMC sites support the Processor PMC features. PMC site #1 supports the MONARCH, IDSELB, GNTB and REQB signals.

PMC Power

See "Absolute Maximum Power Ratings" on page 16

Additional Connections

Additionally to the standard PCI-X buses, the PMC sites include the following connections:

- A connection between the P4 connector and the CompactPCI J5 connector. This connection follows the PICMG 2.3 standard (PMC on CompactPCI).
- A connection between the P4 connector and the CompactPCI J3 connector. This connection follows the PICMG 2.17 standard (StarFabric Specification).

CompactPCI Interface

A PLX PCI6540 bridge connects the Tertiary segment with the CompactPCI interface. This Quaternary PCI Segment segment is called the CompactPCI Segment . The CompactPCI Interface supports 3.3V and 5V signaling operation, therefore the board is not keyed.

The board is able to set the PCIXCAP and M66EN signals on the CompactPCI Segment with a configuration switch SW3.

Miscellaneous Functions

Board Interrupt Routing

The components on the C5000 board provide several interrupt sources and destinations. The primary interrupt destination is the AMCC 440GX processor. If PMC site #1 is populated with a Processor PMC - Monarch card then the PMC site may become an interrupt destination rather than a source. Configuration is made via dip-switches.

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Board Reset

Board reset has a number of possible sources and destinations. The primary sources of reset are the power-up reset controller and the reset button. Other sources are various software reset outputs from the processor, PCIX-to-PCIX bridges, and the PMC modules.

JTAG Interfaces

The JTAG chain is separated into three segments. One segment contains the CPLD devices, a second contains the AMCC 440GX processor and the last one contains the remaining JTAG capable chips.

It is possible to connect to only the segments that are appropriate for a specific software tool.

An adapter board is needed to connect to the correct taps of the chain, and to provide connectors that are compatible with the tools connector. For more information please contact VMETRO.

Temperature Sensors

Temperature sensors are very useful when monitoring applications during extreme conditions.

Several temperature sensors are located on the board in order to monitor the variation of temperature: one close to the bottom of the board, one close to the top of the board and two others located in the middle of the board.

The PowerPC processor communicates with the sensors via its second I2C bus. The type of component used is Maxim MAX1731.

These sensors require additional software, contact VMETRO for information.

Power Supplies (DC-DC converters)

The main source of power is the 5V supplied from the CompactPCI backplane. The following voltages are generated: 3.3V, 2.5V, 1.8V and 1.5V, 1.2V.

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Installation and Hardware description

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2.1 Before You Begin

Precautions in Handling and Storage



Static electricity can permanently damage your C5000. Prevent electrostatic damage by taking proper precautions.

- Make sure your body is grounded when coming into contact with the board by wearing an anti-static wrist strap.
- If an anti-static wrist strap is not available, touch a grounded surface, such as the bare metal chassis, before touching the C5000.
- Only leave the board on surfaces with controlled static characteristics, i.e. specially designed anti-static table covers.
- When handing the board to another person, first touch this person's hand, wrist etc. to discharge any static potential.
- Always store the board in an anti-static bag or other static resistant container.
- If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.

Inspection

Make sure that the C5000 model you have received is according to your purchase order. Check that all items are present according to your purchase order.

Note – You should also inspect the board to verify that no mechanical damage has occurred. Please report any discrepancies or damage to your distributor or to VMETRO immediately.

ESD Discharge Strip

The metal strip along the card edge (top side only) is for electrostatic-discharge. When a board is inserted into an enclosure, the ESD strip connects with an ESD clip on the card guide which is connected to chassis ground.

The ESD strip is separated into three segments to achieve a controlled discharge. The first segment is connected to the front panel through a 10M resistance to discharge any built up static from the board or user. The resistor is used to limit the amount of discharge current.

The second segment discharges the boards ground planes as it is inserted further into the carded; again through a 10M resistance. The final third segment has a direct connection to the front panel. This provides a discharge path as the backplane connectors engage and when the board comes to rest after being completely installed.

The third segment also provides a discharge path from the front panel to chassis ground when the entire system is assembled making it safe for handling and operation.

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2.2 Installing PMC Modules

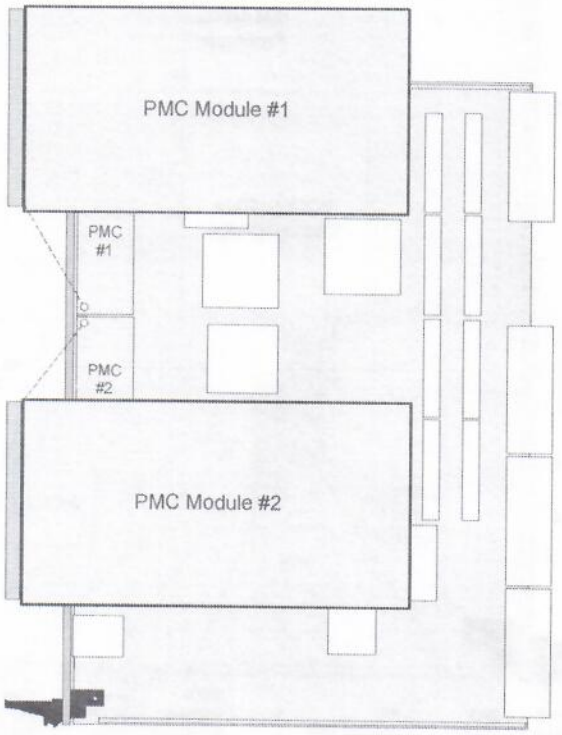
The C5000 is shipped with two PMC filler panels mounted in the front panel. They act as EMC shielding in unused PMC positions. Before installing a PMC module, the filler panel(s) must be removed. This is done by pushing them out from the backside of the front panel.

Four screws must be used to secure each PMC on the C5000 board.

> **Warning!** Be extremely careful when inserting screws to secure PMC modules. Touching component leads, or the printed circuit board itself, with a screwdriver may cause permanent damage to the board

Mounting of PMC modules #1 and #2 on the C5000 board:

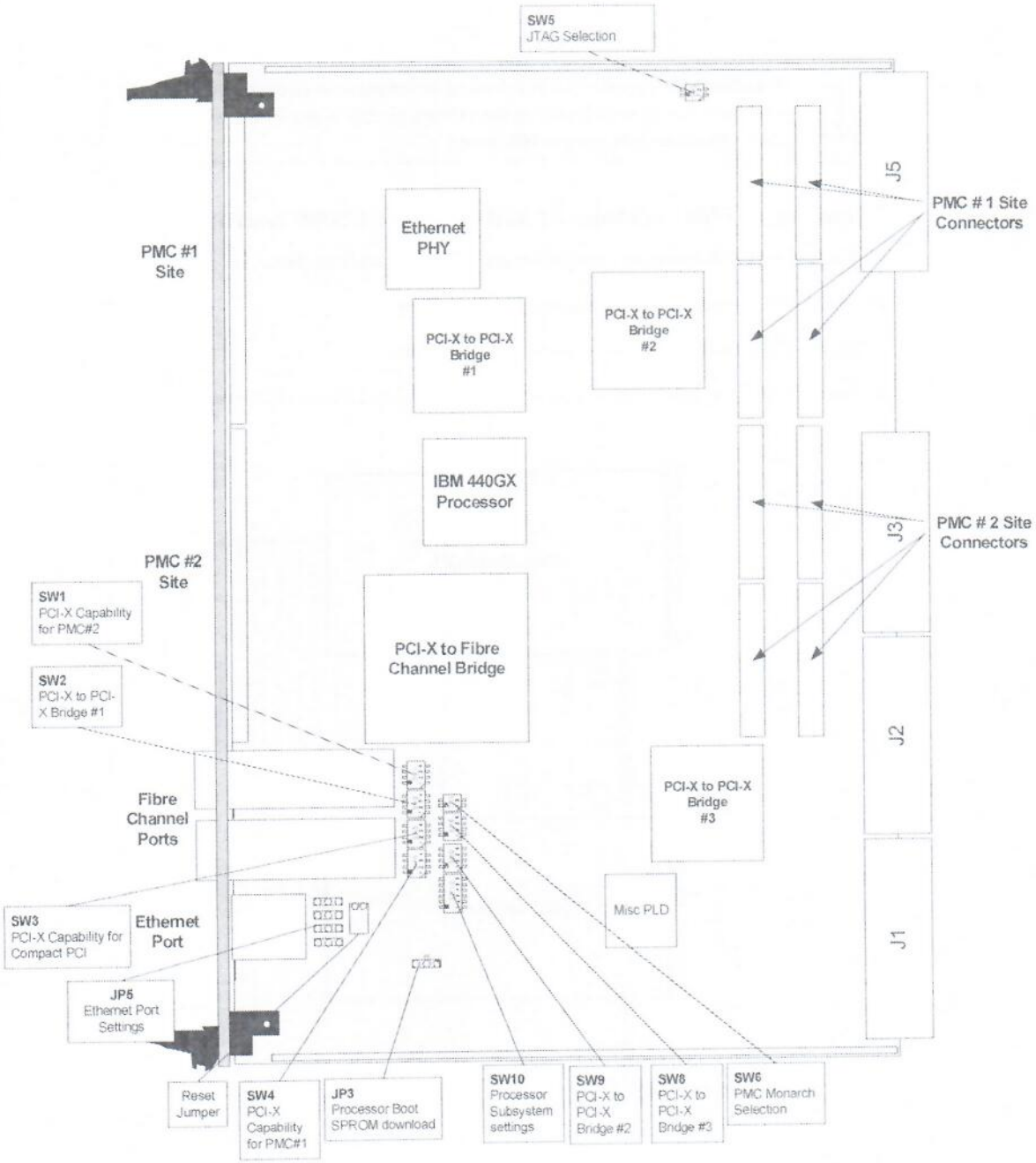
1. Place the C5000 board on a smooth static protected work surface.
2. Install PMC module #1 in the upper PMC position
3. Install PMC module #2 in the lower PMC position
4. Secure PMC modules with screws on the bottom side of the C5000 board



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2.3 Switches and Jumper Settings

FIGURE 2-1
Jumper Settings



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Default Jumper and Switch Settings

The factory settings of the jumpers and switches are shown in Table 2-1:

TABLE 2-1. **Default Jumper and Switch settings**

Jumper/switch	Default Position	Description
JP1		NOT IN USE
JP2		NOT IN USE
JP3	Removed	Processor Boot SPROM Download
JP4		NOT IN USE
JP5	All Jumpers Left	Ethernet/RS232/Reset. Default is Ethernet Only
		See "RJ45 Connector" on page 17 for details
SW1	All OFF	PMC#2 PCI-X Capability Selection
SW2	All ON	PCI-X to PCI-X Bridge Configuration (Bridge between Primary and Secondary PCI Segment)
SW3	3, 4: ON	CompactPCI Capability Selection 33MHz
	1, 2: OFF	
SW4	All OFF	PMC#1 PCI-X Capability Selection
SW5	1: OFF	JTAG Source Selection
	2: ON	
SW6	All OFF	PMC#1 Monarch Selection
SW8	1: OFF	PCI(-X)-to-PCI(-X) Bridge Configuration (Bridge between Tertiary and CompactPCI Segment)
	2, 3, 4: ON	
SW9	All ON	PCI(-X)-to-PCI(-X) Bridge Configuration (Bridge between Secondary and Tertiary PCI Segment)
SW10	1, 5, 6: ON	Processor Subsystem Configuration
	2, 3, 4: OFF	

DIP Switch Settings

PCI-X Capability Selection for PMC Slots

The PCI-X Capability Selection is performed using the switches SW1 and SW4.

- **Switch 1** configures PMC#2 bus

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- **Switch 4** configures PMC#1 bus

TABLE 2-2. PCI-X Capability Selection SW1(PMC#2) and SW4(PMC#1) settings

PCI(-X) Configuration	1	2	3	4
PCI-X / 133MHz	OFF	OFF	OFF	OFF
PCI-X / 100MHz	OFF	OFF	OFF	ON
PCI-X / 66MHz	ON	OFF	OFF	ON
PCI / 66MHz	ON	ON	OFF	ON
PCI / 33MHz	ON	ON	ON	ON

This switch sets the highest possible capability mode for the particular PCI/PCI-X segment. If the PMC installed indicates it's max capability as a lower mode, this lower mode will be chosen automatically.

PCI-X to PCI-X Bridges

- The PCIX-to-PCIX Bridge #1 is located between the processor subsystem and the rest of the board. It is configured using the switch SW2.
- The PCIX-to-PCIX Bridge #2 is located between the two PMC subsystems. It is configured using the switch SW9.
- The PCIX-to-PCIX Bridge #3 is located between the second PMC subsystem and the Compact PCI subsystem. It is configured using the switch SW8.

Each switch is has the settings described in Table 2-3.

TABLE 2-3. PCI-X to PCI-X Bridges SW2, SW9, SW8 settings

Switch	Function
1	Port Priority Boot
	The switch is connected to the P_BOOT pin on the bridge.
	Non-Transparent Mode: Primary port has boot priority when the switch is OFF Secondary port has boot priority when the switch is ON
	Transparent Mode: Not Used.
2	Serial EEPROM Access Enable
	ON enables the EEPROM accesses.
3	Transparent Mode Control
	Transparent mode when the switch is ON Non-transparent mode when the switch is OFF.
4	Serial EEPROM Write Enable
	ON enables the Serial EEPROM.

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TABLE 2-4. SW3 CompactPCI Capability Selection

	Switch			
MODE	1	2	3	4
PCI-X / 133MHz*	ON	OFF	OFF	OFF
PCI-X / 100MHz*	OFF	ON	OFF	OFF
PCI-X / 66MHz*	OFF	ON	OFF	ON
PCI / 66MHz	OFF	OFF	ON	OFF
PCI / 33MHz	OFF	OFF	ON	ON

*There is no PICMG standard defining support for PCI-X in Compact PCI systems, these are recommended settings only.

TABLE 2-5. SW5: JTAG Source Selection

Switch	Description
1	JTAG Source Selection
	ON: CompactPCI JTAG Interface
	OFF: Local JTAG Interface
2	JTAG Enable
	ON: JTAG enable
	OFF: JTAG disable

PMC Monarch Selection

The PMC Monarch Selection is done using the switch SW6.

TABLE 2-6. PMC Monarch Selection SW6 settings

Switch	Function
1	PMC#1 MONARCH Setup
	ON to setup the PMC#1 as MONARCH.

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Processor Subsystem

The Processor Subsystem is configured using the switch SW10.

TABLE 2-7. **Processor Subsystem SW10**

Switch	Function
1	Processor MFS Serial EEPROM Write Enable ON to write-enable the Processor MFS Serial EEPROM.
2	Processor Boot Serial EEPROM Write Enable ON enables write operations to the Processor Boot Serial EEPROM devices.
3	Processor Flash Write Enable OFF enables write operations to the Processor Flash.
4	Processor Flash Monitor Write Enable ON enables write operations to the Monitor area of the Processor Flash
5	Processor Boot ON to boot the processor from Flash. OFF to boot the processor from PCI.
6	Fibre Channel Flash Write Enable ON enables write operations to the Fibre Channel Flash devices.

Jumper Settings

This section describes the role and use of the configuration jumpers located on the board. JP1 and JP4 are NOT in use.

JP3: Processor Boot SPROM Download

During the board configuration, the two Processor Boot Serial EEPROM devices are written using jumper JP3. This jumper is not used during normal operations.

TABLE 2-8. **JP3 Processor Boot SPROM Download**

PIN 1	SCL
PIN 2	SDA
PIN 3	GND

JP5: Ethernet Port

See"RJ45 Connector" on page 17.

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2.4 Installing the C5000 into the Chassis

Slot Selection

You can install the C5000 board into any 3.3V or 5V CompactPCI slot in a 6U CompactPCI chassis.

The metal strip along the card edge is for electrostatic-discharge. Some chassis include a spring contact in the front of the board guide that connects the metal strip on the board to the chassis ground while the board is inserted.

Each of the two metal strips are connected to board signal ground through a 10K resistor

In accordance with the CompactPCI Specification, a C5000 main board installed a System Slot will act as the System Controller. Consequently, system controller functions are also enabled. Board compatibility glyphs are displayed on the backplane to indicate type of slot:

△ (triangle) for System Slot

○ (circle) for Peripheral Slot

Power Consumption



Warning! The C5000 hardware requires forced air-cooling for reliable operation. Commercial and Rugged Level 1 boards require 300lfm, Rugged Level 3 requires 600lfm. For Rugged Level 2 contact VMETRO.
Operation on extender boards is not recommended.

Typical values for power consumption are shown in Table 2-9. In Idle Mode, no processors are booting, and no data is transferred. In Active Mode, processors are booting and running memory tests.

Note – The numbers shown in Table 2-9 do **not** include any power drawn by PMC modules mounted on the board, **nor** increased system power consumption when driving the backplane.

When driving the CompactPCI bus, the system power consumption goes up, and the additional power is dissipated in the termination resistors of the CompactPCI bus. The amount of additional power depends on the CompactPCI bus traffic pattern and varies from TBA to TBA W.

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Although the C5000 board may increase the system power consumption by driving the CompactPCI bus, the additional power is not included in the numbers below, since the additional power is dissipated outside the board. Furthermore, the CompactPCI traffic pattern, and the C5000's share of the CompactPCI bus is highly application dependent.

TABLE 2-9. C5000 Power Consumption

Model	Idle Power Consumprion	Active Power Consumption
C5211-EFF	16 W	20 W

Absolute Maximum Power Ratings

The C5000 is a PMC carrier board and offers two indepented PMC sites. The absolute maximum ratings per PMC site are shown in the following table.

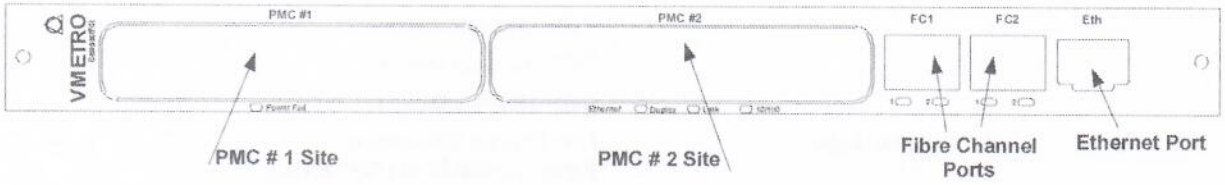
TABLE 2-10. Max. Power Supply

Voltage	max. Current
3.3V	3.5A
5.0V	2.5A
VIO	2A
12V	500mA
-12V	100mA

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2.5 Front Panel Connectors

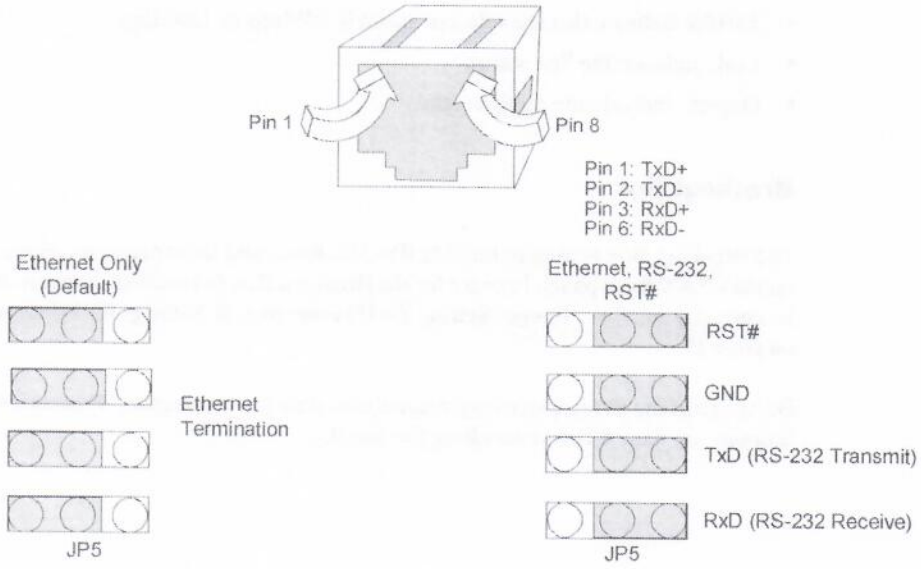
FIGURE 2-2 *Front Panel connections*



RJ45 Connector

The C5000 board has an RJ-45 type connector used for Ethernet, RS-232 and external Reset. By default, only the Fast Ethernet interface is used (Figure 2-3). To make use of RS-232 and Reset in addition to Ethernet, the jumpers must be changed as shown in Figure 2-3. The supplied Breakout Box(page 18) is necessary to access Ethernet, RS-232 and Reset.

FIGURE 2-3 *Jumper Setting for Ethernet only & Settings for Ethernet, RS-232 and Reset*



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TABLE 2-11. RJ-45 Jumper Pins

Pin	Jumper Settings	Function
1		TxD+ (Transmit Data +)
2		TxD- (Transmit Data -)
3		RxD+ (Receive Data +)
4	Left or Right	Left: Ethernet Termination Right: External Reset (RJ45 RST#)
5	Left or Right	Left: Ethernet Termination Right: Ground (GND)
6		RxD- (Receive Data -)
7	Left or Right	Left: Ethernet Termination Right: RS-232 Transmit Data
8	Left or Right	Left: Ethernet Termination Right: RS-232 Receive Data

The Ethernet LEDs loacted underneath the PMC #2 slot indicate the following:

- 10/100: indicate that the selected speed is 10Mbps or 100Mbps.
- Link: indicate the link status.
- Duplex: indicate the duplex status.

Breakout Box

The Breakout Box is used to provide RS-232, Reset and Ethernet connections via the RJ-45 Socket on the C5000 front panel. In order for the Breakout Box to function, Jumpers JP5, JP6 and JP7 must be correctly set. See "Jumper Setting for Ethernet only & Settings for Ethernet, RS-232 and Reset" on page 17.

Be aware of the Static Electricity precautions stated in the section "Precautions in Handling and Storage" on page 8 before handling the board.

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FIGURE 2-4 *Breakout Box used for RS232, Reset and Ethernet signalling.*

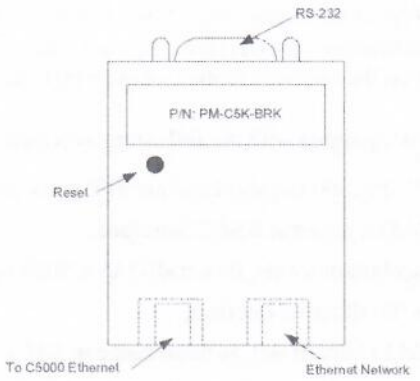


FIGURE 3. *Breakout Box used for RS232, Reset and Ethernet signalling.*

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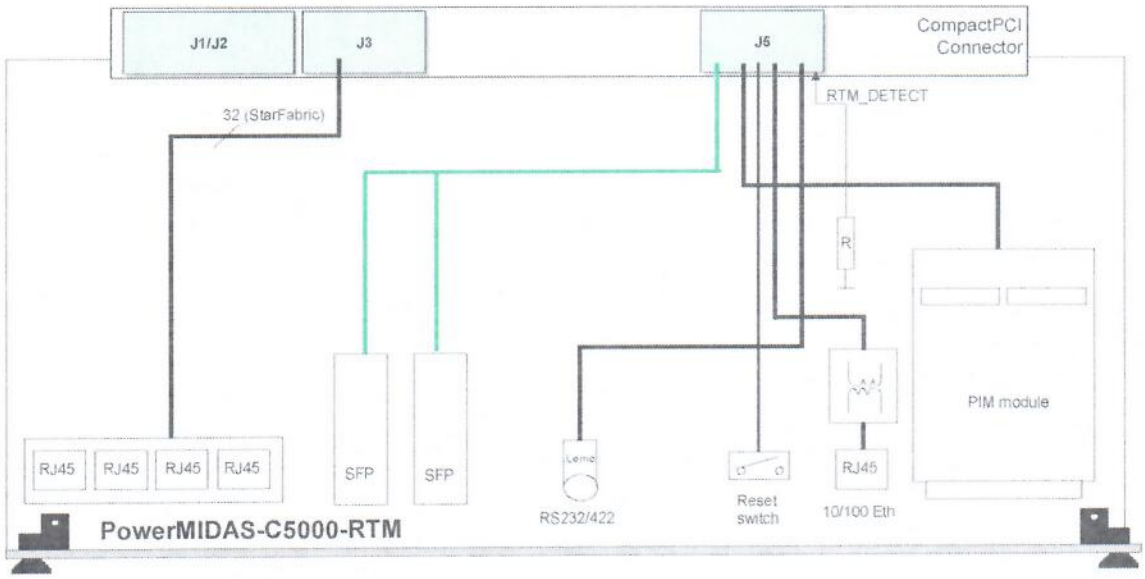
2.6 Rear Transition Module

The Rear Transition Module (RTM) is a Compact PCI I/O board that connects to a PowerMIDAS C5000 to extend the I/O interface. The connection to the PowerMIDAS C5000 is via the J3 and J5 connectors on the rear side of the Compact PCI backplane.

The board is equipped with the following interfaces:

- Two 10/100/1000 Gigabit Ethernet SFP ports (two front panel copper/optical connectors).
- One RS-232, optional RS422 interface.
- One reset button for the PowerMIDAS-C5000 board.
- One 10/100 Ethernet interface.
- One PIM I/O board slot, in accordance to VITA36.
- Optional - two StarFabric interfaces, PICMG 2.17 (four RJ45 front panel connectors).

FIGURE 2-1 *RTM Main Components*



Gigabit Ethernet Interface

Two Gigabit Ethernet interfaces are available on the front panel. Both fiber connectors and copper connectors (RJ45) can be plugged into this interface. The connectors provide a 2.125 Gb/s Ethernet interface.

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Two LEDS are used for each interface to indicate the following:

Colour	Meaning
Green	Rx
Yellow	Tx
Green	Link

RS-232/422 Interface

There is a second serial interface on the C5000 board that can only be used with the RTM board. This interface may either be RS-232 or RS-422 (mounting option made at factory on both the C5000 *and* the RTM board).

10/100 Ethernet Interface

The 10/100 Ethernet interface on the front panel has two LEDs indicating:

Green (rightmost position): Link/traffic indication.

Yellow (leftmost position) 10/100 indication

PIM I/O Interface

The PIM I/O slot is in accordanse to PMC I/O Standard, VITA36-19X. This interface is a connection to the 64 I/O signals on the PowerMIDAS-C5000 PMC#1, J4 connector. In addition, this interface provides the power voltages +5V, +3.3V, +12V, -12V.

Reset Switch

The front panel reset button causes a reset of the PowerMIDAS-C5000 board.

StarFabric Interface

StarFabric Link 0 and Link 1 are available on the front panel. Four RJ45 connectors are used for this interface. The two links are routed to the four RJ45 connectors as shown in Figure 2-2 the figure below:

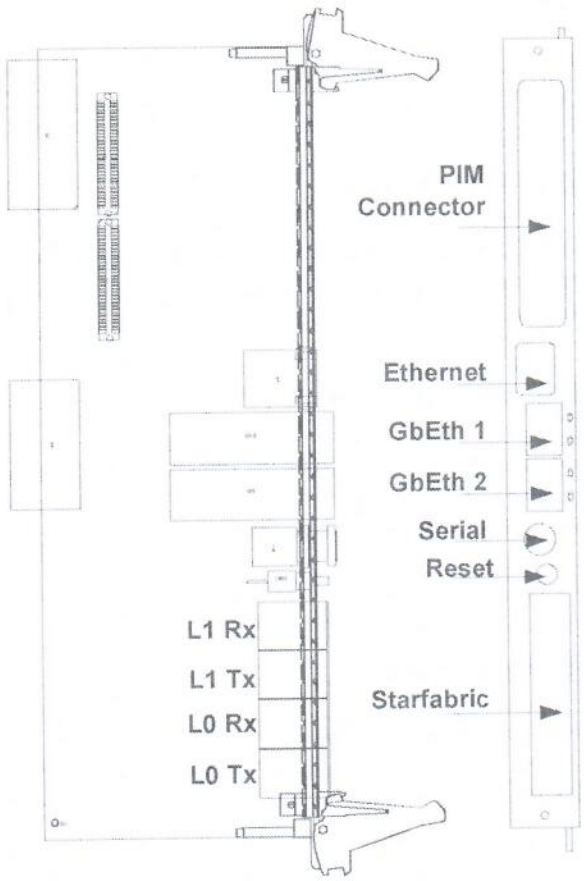


FIGURE 2-2 *StarFabrik LINK0 and LINK1 on the RJ45 connectors*

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Rear Transition Module and Front panel Layout

FIGURE 2-3
RTM & Front Panel Layout



Configuration

To verify that you have a link through the SFPs (Gigabit ethernet) and 10/100 Ethernet connectors:

1. Connect the Ethernet cables with the power off.
2. Turn on the power
3. For gigabit Ethernet, the "link" diode on the RTM should be on. For 10/100 Ethernet the yellow "10/100" LED should be on and the green "link" diode should flash to indicate link activity.

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Configuring the IP address of the Ethernet ports

There are two ways of doing this:

1. You can configure the boot parameters to use "emac1", "emac2" or "emac3" instead of "emac0" using the VxWorks command "bootChange". See the Network Interfaces section in the BSP User Guide.

   "emac0" is the front panel Ethernet connection.

   "emac1" is the fast Ethernet port on the RTM

   "emac2" is GbEth1 on the RTM

   "emac3" is GbEth2 on the RTM

   The boot parameters also specify the IP address which will be assigned.

2. Several Ethernet connection can be attached simultaneously in VxWorks. This can be done as follows for "emac3" for instance:

```
ipAttach(3,"emac")
ifMaskSet("emac3", 0xffffff00)
ifAddrSet("emac3", "192.168.50.2")
```

Using the serial port (RS232) on the RTM

VxWorks can be instructed to use the RS232 on the RTM by configuring CONSOLE_TTY to 1.

This is not default, so **config.h** needs to be changed and vxWorks recompiled.

The Monitor will then boot using the RS232 on the front panel, and VxWorks will start using the RTM console during bootup.

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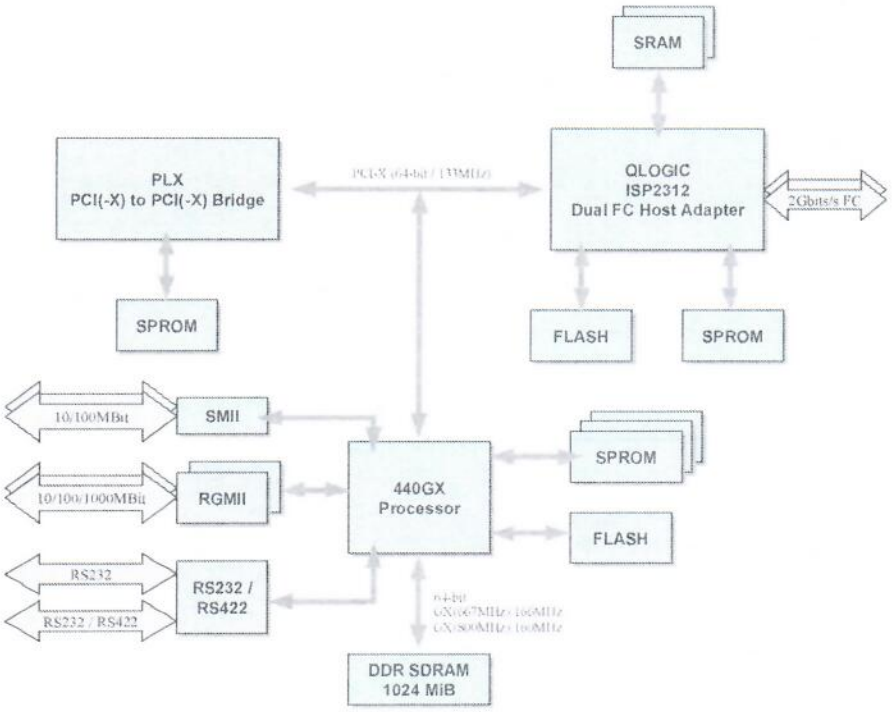
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Processor Subsystem

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3.1 Introduction

FIGURE 3-1
Processor Subsystem Block Diagram



Primary PCI Segment

The Primary PCI Segment is a 64-bit/133MHz PCI-X bus. There are three major devices located on the Primary PCI Segment:

1. AMCC 440GX processor. - This device has a built in arbiter which is used to arbitrate the Primary PCI Segment.
2. QLOGIC ISP2312 Dual FC Controller.
3. PCI6540 PCIX-to-PCIX bridge (via its primary side).

IDSEL Assignment

- AD[17] is used for the AMCC 440GX Processor IDSEL
- AD[18] is used for the PCI6540 PCIX-to-PCIX Bridge (Primary Side) IDSEL
- AD[19] is used for the QLOGIC ISP2312 PCIX-to-FC Bridge IDSEL

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3.2 AMCC 440GX PowerPC Embedded Processor

Designed specifically to address high-end embedded applications, the PowerPC 440GX (PPC440GX) provides a high-performance, low power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and lower power dissipation. This chip contains a high-performance RISC processor core, DDR SDRAM controller, PCI-X bus interface, Ethernet interface, controls for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

For more detailed information about the PowerPC 440GX, please refer to the PowerPC 440GX Embedded Processor Data Sheet and the PowerPC 440GX Embedded Processor User's Manual.

The C5210 has a processor running at 667MHz with memory chips running at 167MHz, The C5211 model has the processor running at 800MHz with the memory chips running at 160MHz.

Processor DDR-SDRAM Memory

The amount of DDR-SDRAM memory used is limited to 1024MiB using several 512Mb memory chips running at 166/160MHz.

UART and Serial Lines

The two UART I/O pins are connected to a multi-protocol transceiver which can handle 2Tx/2Rx RS-232 interface and a single RS-422 transceiver simultaneously.

The first UART (UART0) is used for one RS-232 line, which is connected to the RJ-45 connector on the front panel. The second UART (UART1) is configured as RS-232 by default and can be accessed via the RTM. (The signals are routed to CompactPCI J5 connector.) An RS-422 option can also be delivered. Contact VMETRO for details.

Ethernet Interfaces

All four processor Ethernet interfaces are connected:

- The first two Ethernet interfaces (10/100-TX) are connected to the Fast Ethernet Transceiver. The first Ethernet link is connected to the on-board RJ45 copper connector and the second is routed to the RTM.
- The second two Ethernet interfaces (10/100/1000Mbps) are connected to the CompactPCI backplane (PICMG 2.16) but can also be accessed through the RTM as either copper or optical interfaces.

Link Configuration

The four Ethernet links are configured the following way:

- The first two MAC interfaces are always configured as SMII (Serial Media Independent Interface). The media interfaces are always configured in the 10/100-TX mode

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- The third and fourth MAC interfaces are always configured as RGMII (Reduced Gigabit Media Independent Interface). The media interfaces are configured in the 10/100/1000 Base T mode of operation when connected to a copper connector and in the 1000-SX mode when connected to CompactPCI Packet Switching Backplane and in the 1000-SX mode when connected to a fiber connector on the RTM board.

Status LEDs for first EMAC

Three led pins are physically connected to LEDs:

- **Link:** LED 1 output pin is connected to a led in order to indicate the link status
- **10/100:** LED 2 output pin is connected to a led in order to indicate that the selected speed is 10Mbps or 100Mbps
- **Duplex:** LED 3 output pin is connected to a led in order to indicate the duplex status

The led signal lines for the second 10/100-TX port are routed to the RTM board. The LEDs are located on the RTM board itself.

FLASH

The FLASH is only used for storing the boot image(s). It can be entirely locked/unlocked using a configuration switch. See "Processor Subsystem SW10" on page 16.

I2C Devices

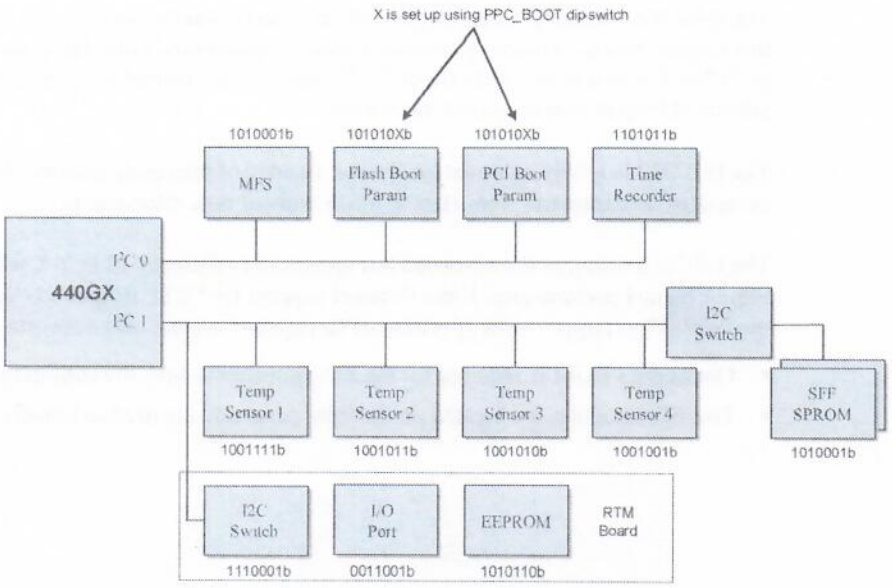
The 440GX PowerPC processor has access to the following devices on its primary I2C bus:

- Processor SPROM used to store the MFS.
- Processor SPROM used to store the PCI boot parameters.
- Processor SPROM used to store the FLASH boot parameters.
- Time and Event Recorder
- Devices located on RTM board

The 440GX PowerPC processor has access to the four temperature sensors on its secondary I2C bus. The following figure describes the processor I2C configuration:

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FIGURE 3-2
AMCC 440GX I2C Devices



Serial PROM Devices

There are three Serial Prom devices:

- One serial PROM is required for the processor to boot and load the configuration parameters.
- One SPROM is used to keep the processor from booting.
- A third serial EEPROM is used to store the MFS (Midas File System). Monitor and BSP boot behavior depending on parameter values held in the MFS.

Use of SPROM Devices should be under VMETRO guidance, some functions are already available in the BSP software.

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3.3 QLOGIC ISP2312 Dual Fibre Channel Controller

The ISP2312 is a highly integrated single-chip, dual-channel, bus master, Fibre Channel processor that targets storage, clustering, and networking applications. This chip connects a conventional PCI or PCI-X bus to one or two 1.062 or 2.125 Gbps Fibre Channel ports connected to fabric, single arbitrated loop or point-to-point topologies.

The ISP2312 is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention.

The ISP2312 balances the advanced bus speeds and efficiency of PCI-X with exceptional 2-Gbps Fibre Channel performance. Fibre Channel support for SCSI, IP, and VI (Virtual Interface) allows the ISP2312 to target a wide spectrum of storage and system area networks (SANs).

- One serial PROM is required for the FC controller to save the configuration.
- Two SFF modules are located on the front panel and are used to transfer data via Fibre Channel.

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3.4 PCI-X to PCI-X Bridges

The PLX6540 64-bit PCIX-to-PCIX bridge is designed for high performance, high availability applications, in PCI-X to PCI conversion, bus expansions, frequency conversions from faster PCI-X to slower PCI-X or from slower PCI-X to faster PCI-X bus, address remapping, high availability hot swap and universal system-to-system bridging. PCI6540 has sophisticated buffer management and buffer configuration options designed to provide customizable performance for very efficient PCIX-PCI conversion and processor bridging. PCI6540 allows up to 4KiB prefetch during read and timed FIFO flush management.

Power-up / Reset Configuration Options

Many options of the PCI6540 can be configured at power-up or reset. Because most of the options can be modified using software, only a few options are connected to dip-switches.

Application Modes

On the CompactPCI Segment the board can be used for the system slot or peripheral slot in a CompactPCI backplane. The bridge senses the type of slot and configures itself as Transparent or Non-Transparent, as appropriate. In the system slot the board is operating as a host and the bridge operates in Transparent mode.

All other bridges support Non-Universal Transparent and Non-Universal Non-Transparent modes. Currently, only Non-Universal Transparent mode is supported.

In non-transparent mode you can choose which port has boot priority using a dip-switch (controls P_BOOT signal).

EEPROM

At boot-up, an external EEPROM can be used by the PCI6540 to initialize its internal registers. The EEPROM auto-load process is only initiated when the primary reset input is deasserted. Data is always downloaded from address 0. Hosts accesses are only allowed when the download process is completed (bit EEPAUTO status is 0).

A dip-switch is used to control the use of the EEPROM at start-up.

Secondary Port Arbiter Setup

As the only built-in arbiter present on the secondary PCI bus, the PCI6540 internal arbiter is used to arbitrate.

Primary Interface

The primary interface of this bridge is connected to the Primary PCI Segment and is 64-bit 133MHz PCI-X only.

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Secondary Interface

The secondary interface of the PCI6540 is connected to the first PMC site (PMC#1) and the primary interface of another PCI6540 bridge.

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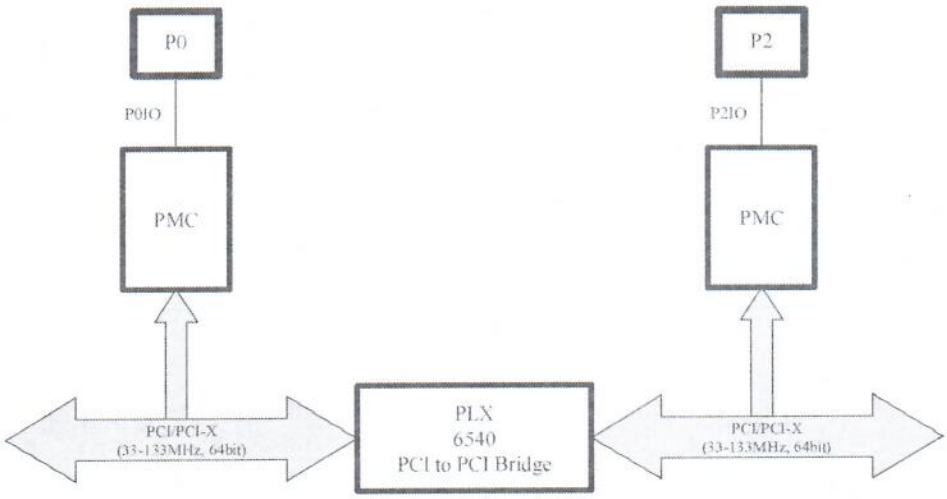
PMC Subsystem

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4.1 Introduction

The PMC subsystem is composed of two 3.3V signalling PMC sites and is located on two PCI(-X) segments called the Secondary and Tertiary PCI Segments. The connection between the two PCI(-X) segments is provided by a PCI-X to PCI-X bridge.

FIGURE 4-1 *PMC Subsystem Block Diagram*



The factory settings of the board switch configuration allows the bus frequency of the PCI-X segments to be automatically configured to the frequency used by a PMC card insterted into it, and by the limitation set with dip-switches 1 and 4. See "PCI-X Capability Selection for PMC Slots" on page 17.

PMC Power

See "Absolute Maximum Power Ratings" on page 16

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4.2 Secondary and Tertiary PCI Segments

PCI Mode and Speed Configuration

The PCIXCAP and M66EN pins of a PMC module determine which clock speed and protocol (PCI vs. PCI-X) can be used on the segment. There are five detectable modes of operation: 33/66MHz PCI and 66/100/133MHz PCI-X. These two signals are used by the PMC to inform the host of it's capability. The C5000 will use the the highest common mode between the C5000 switch settings and the installed PMC board..

Note – Even if PMCs can only signal that they are either 66 or 133 MHz compliant in PCI-X mode, the host may decide to run 133 MHz capable boards at a lower frequency (typically 100MHz) if the total number of loads is too high for the system to achieve 133MHz operations.

Configuration switches can be used to:

- Ground the PCIXCAP signal to force PCI operations, or pull low to inhibit 100/133 MHz operations by configuration switches.
- The M66EN signal can also be grounded through in order to inhibit 66MHz PCI operations.
- Select between 133 and 100 MHz as the maximum operating frequency.

The detected PCIXCAP/M66EN/dip-switches values determine the frequency of the clock generator for the segment. Table 2-9 on page 17 for dip-switch settings.

Arbitration

Secondary and Tertiary PCI Segments

The built-in PCI-X arbiter of the PCI6540 PCIX-to-PCIX Bridge is used. The arbiter provides two REQ/GNT pairs to the PMC to support a dual device PPMC.

IDSEL Assignment

Secondary PCI Segment

- AD[17] is used for the PMC#1 IDSEL
- AD[18] is used for the PMC#1 IDSELB
- AD[19] is used for the PCI6540 P2P Secondary Side IDSEL (PCI6540 located in the Processor Subsystem)
- AD[20] is used for the PCI6540 P2P Primary Side IDSEL (PCI6540 located between the Secondary and Tertiary PCI Segments)

Tertiary PCI Segment

- AD[17] is used for the PMC#2 IDSEL
- AD[18] is used for the PMC#2 IDSELB

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- AD[19] is used for the PCI6540 P2P Secondary Side IDSEL (PCI6540 located between the Secondary and Tertiary PCI Segments)
- AD[20] is used for the PCI6540 P2P Primary Side IDSEL (PCI6540 closer to the Extension Subsystem)

Processor PMC Support

The Processor PMC standard adds several extensions to the PMC standard:

- **Support for a second PCI device**: Support for a second device requires an additional REQ/GNT pair and an additional IDSEL signal. This is implemented by using an additional REQ/GNT pair from the PCI bus arbiter and connecting the extra IDSEL signal to an unused AD line
- **Support for System Processor in the PPMC site (Monarch)**: Support for having the system processor in the PPMC site is partially supported. The MONARCH# signal is controlled by a configuration switch, and allows the PPMC to detect that it should be the system processor. When MONARCH# is active, interrupts are routed to the PPMC site input signals rather than from the PPMC site (output signals).

Note – The Monarch PPMC is also responsible for PCI bus enumeration in the system if the P2P Bridge on the primary bus is in Non-Transparent Mode or the embedded AMCC 440GX processor is not permitted to boot.

Only the first PMC site (PMC#1) includes support for the MONARCH feature.

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4.3 PCI6540 PCIX-to-PCIX Bridge

This Bridge has been discussed in "PCI-X to PCI-X Bridges" on page 31. What follows are details appropriate for this particular bridge.

Power-up / Reset Configuration Options

PCI-X Capability

Both primary and secondary interfaces can be run in PCI or PCI-X modes. See "PCI-X Capability Selection for PMC Slots" on page 11.

Secondary Port Arbiter Setup

As the only built-in arbiter present on the secondary PCI bus, the PCI6540 internal arbiter is used to arbitrate.

Primary Interface

The primary interface of this bridge is connected to the secondary interface of the Secondary PCI Segment bridge and to the first PMC site (PMC#1).

Secondary Interface

The secondary interface of this bridge is connected to the second PMC site (PMC#2) and the primary interface of another PCI6540 bridge.

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4.4 PMC to CompactPCI Connections

PMC #1-P4 to CompactPCI J5

In addition to the standard PCI(-X) bus, the PMC #1 site includes a connection between its P4 connector and the CompactPCI J5 connector. This connection follows the PICMG 2.3 standard (PMC on CompactPCI).

TABLE 4-1. PICMG 2.3 Routing

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J5	22	GND	PMC1-1	PMC1-2	PMC1-3	PMC1-4	PMC1-5
J5	21	GND	PMC1-6	PMC1-7	PMC1-8	PMC1-9	PMC1-10
J5	20	GND	PMC1-11	PMC1-12	PMC1-13	PMC1-14	PMC1-15
J5	19	GND	PMC1-16	PMC1-17	PMC1-18	PMC1-19	PMC1-20
J5	18	GND	PMC1-21	PMC1-22	PMC1-23	PMC1-24	PMC1-25
J5	17	GND	PMC1-26	PMC1-27	PMC1-28	PMC1-29	PMC1-30
J5	16	GND	PMC1-31	PMC1-32	PMC1-33	PMC1-34	PMC1-35
J5	15	GND	PMC1-36	PMC1-37	PMC1-38	PMC1-39	PMC1-40
J5	14	GND	PMC1-41	PMC1-42	PMC1-43	PMC1-44	PMC1-45
J5	13	GND	PMC1-46	PMC1-47	PMC1-48	PMC1-49	PMC1-50
J5	12	GND	PMC1-51	PMC1-52	PMC1-53	PMC1-54	PMC1-55
J5	11	GND	PMC1-56	PMC1-57	PMC1-58	PMC1-59	PMC1-60
J5	10	GND	PMC1-61	PMC1-62	PMC1-63	PMC1-64	

The pairs of nets are differential and have a differential impedance of 100ohms. These nets do not have any termination on C5000.

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TABLE 4-2. PICMG 2.3 Differential Pairs.

Name Of Matched Pair	Nets	
PMC1_PAIR1	PMC1_IO[1]	PMC1_IO[3]
PMC1_PAIR2	PMC1_IO[2]	PMC1_IO[4]
PMC1_PAIR3	PMC1_IO[5]	PMC1_IO[7]
PMC1_PAIR4	PMC1_IO[6]	PMC1_IO[8]
PMC1_PAIR5	PMC1_IO[9]	PMC1_IO[11]
PMC1_PAIR6	PMC1_IO[10]	PMC1_IO[12]
PMC1_PAIR7	PMC1_IO[13]	PMC1_IO[15]
PMC1_PAIR8	PMC1_IO[14]	PMC1_IO[16]
PMC1_PAIR9	PMC1_IO[17]	PMC1_IO[19]
PMC1_PAIR10	PMC1_IO[18]	PMC1_IO[20]
PMC1_PAIR11	PMC1_IO[21]	PMC1_IO[23]
PMC1_PAIR12	PMC1_IO[22]	PMC1_IO[24]
PMC1_PAIR13	PMC1_IO[25]	PMC1_IO[27]
PMC1_PAIR14	PMC1_IO[26]	PMC1_IO[28]
PMC1_PAIR15	PMC1_IO[29]	PMC1_IO[31]
PMC1_PAIR16	PMC1_IO[30]	PMC1_IO[32]
PMC1_PAIR17	PMC1_IO[33]	PMC1_IO[35]
PMC1_PAIR18	PMC1_IO[34]	PMC1_IO[36]
PMC1_PAIR19	PMC1_IO[37]	PMC1_IO[39]
PMC1_PAIR20	PMC1_IO[38]	PMC1_IO[40]
PMC1_PAIR21	PMC1_IO[41]	PMC1_IO[43]
PMC1_PAIR22	PMC1_IO[42]	PMC1_IO[44]
PMC1_PAIR23	PMC1_IO[45]	PMC1_IO[47]
PMC1_PAIR24	PMC1_IO[46]	PMC1_IO[48]
PMC1_PAIR25	PMC1_IO[49]	PMC1_IO[51]
PMC1_PAIR26	PMC1_IO[50]	PMC1_IO[52]
PMC1_PAIR27	PMC1_IO[53]	PMC1_IO[55]
PMC1_PAIR28	PMC1_IO[54]	PMC1_IO[56]
PMC1_PAIR29	PMC1_IO[57]	PMC1_IO[59]
PMC1_PAIR30	PMC1_IO[58]	PMC1_IO[60]
PMC1_PAIR31	PMC1_IO[61]	PMC1_IO[63]
PMC1_PAIR32	PMC1_IO[62]	PMC1_IO[64]

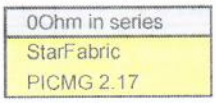
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4.5 PMC #2-P4 to CompactPCI J3

In addition to the standard PCI(-X) bus, the PMC #2 site includes a connection between its P4 connector and the CompactPCI J3 connector. This connection follows the PICMG 2.17 Standard (StarFabric Specification).

TABLE 4-3. PICMG 2.17 Routing (StarFabric)

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J3	19	GND				PMC2-1	PMC2-2
J3	18	GND			GND		
J3	17	GND			GND		
J3	16	GND			GND		
J3	15	GND			GND		
J3	14	GND	PMC2-4	PMC2-3	PMC2-8	PMC2-7	PMC2-12
J3	13	GND	PMC2-6	PMC2-5	PMC2-10	PMC2-9	PMC2-14
J3	12	GND	PMC2-11	PMC2-16	PMC2-15	PMC2-20	PMC2-19
J3	11	GND	PMC2-13	PMC2-18	PMC2-17	PMC2-22	PMC2-21
J3	10	GND	PMC2-24	PMC2-23	PMC2-26	PMC2-25	PMC2-36
J3	9	GND	PMC2-30	PMC2-28	GND	PMC2-40	PMC2-38
J3	8	GND	PMC2-34	PMC2-32	GND	PMC2-44	PMC2-42
J3	7	GND	PMC2-33	PMC2-31	GND	PMC2-43	PMC2-41
J3	6	GND	PMC2-29	PMC2-27	GND	PMC2-39	PMC2-37
J3	5	GND	PMC2-50	PMC2-48	GND	PMC2-60	PMC2-58
J3	4	GND	PMC2-54	PMC2-52	GND	PMC2-64	PMC2-62
J3	3	GND	PMC2-53	PMC2-51	GND	PMC2-63	PMC2-61
J3	2	GND	PMC2-49	PMC2-47	GND	PMC2-59	PMC2-57
J3	1	GND	PMC2-35	PMC2-46	PMC2-45	PMC2-56	PMC2-55



The StarFrabric signal pairs have a differential impedance of 100ohms. The nets do not have any termination on the C5000.

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TABLE 4-4. PICMG 2.17 Differential Pairs (StarFabric)

Name Of Matched Pair	Nets	
LINK1_TX3	PMC2_IO[38]	PMC2_IO[40]
LINK1_TX2	PMC2_IO[44]	PMC2_IO[42]
LINK1_TX1	PMC2_IO[43]	PMC2_IO[41]
LINK1_TX0	PMC2_IO[39]	PMC2_IO[37]
LINK1_RX3	PMC2_IO[30]	PMC2_IO[28]
LINK1_RX2	PMC2_IO[34]	PMC2_IO[32]
LINK1_RX1	PMC2_IO[33]	PMC2_IO[31]
LINK1_RX0	PMC2_IO[29]	PMC2_IO[27]
LINK0_TX3	PMC2_IO[60]	PMC2_IO[58]
LINK0_TX2	PMC2_IO[64]	PMC2_IO[62]
LINK0_TX1	PMC2_IO[63]	PMC2_IO[61]
LINK0_TX0	PMC2_IO[59]	PMC2_IO[57]
LINK0_RX3	PMC2_IO[50]	PMC2_IO[48]
LINK0_RX2	PMC2_IO[54]	PMC2_IO[52]
LINK0_RX1	PMC2_IO[53]	PMC2_IO[51]
LINK0_RX0	PMC2_IO[49]	PMC2_IO[47]

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Compact PCI Interface

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5.1 Introduction

A PLX PCI6540 PCI-X to PCI-X bridge connects the Tertiary segment with the CompactPCI interface. This Quaternary PCI Segment segment is called the CompactPCI Segment . The CompactPCI Interface supports 3.3V and 5V signaling operation, therefore the board is not keyed.

The clock speed is computed by a CPLD using the PCIXCAP and M66EN signals. This bridge is used in Universal mode and senses the type of CompactPCI slot (system or peripheral) and configures itself as Transparent or Non-Transparent.

In system slot the board operates as a host, and the bridge operates in Transparent mode (clock generation and arbitration). In the peripheral slot, the bridge is configured in Non-Transparent mode. This is performed automatically.

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5.2 PCI(-X) Mode and Speed Configuration

The CompactPCI Segment is capable of operating in either conventional PCI mode or in PCI-X mode, at any of the defined frequency ranges. In Transparent mode the board acts as the central resource for the CompactPCI Segment, it controls the mode and frequency determination process. It senses the maximum frequency at which the segment is capable of operating at initialization.

Due to differences between standard PCI-X and CompactPCI-X bus speed and bus type detection scheme, a PLD detects the mode through SW3 signals and determines the corresponding frequency/mode. When finished, the PLD places the secondary side of the bridge in the correct mode and the primary reset input of the bridge is deasserted.

In Universal Transparent Mode the bridge senses the state on its secondary bus, selects the mode and asserts the appropriate signals for the PCI-X initialization pattern on the secondary bus.

TABLE 5-1. PCI(X) Mode setting

PCIXCAP	M66EN	Comment
0	0	PCI 33MHz
0	1 (3.3V)	PCI 66MHz
1 (3.3V)	0	PCI-X 66MHz*
1 (3.3V)	1 (3.3V)	PCI-X 100MHz *
5.0V	1 (3.3V)	PCI-X 133MHz*

*There is no PICMG standard defining support for PCI-X in Compact PCI systems, these are recommended settings only.

TABLE 5-2. PCI(-X) Mode detection

PCIXCAP	M66EN	Comment
< 1.04V	< 1.04V	PCI 33MHz
< 1.04V	> 1.57V	PCI 66MHz
1.57V and 4V	< 1.04V	PCI-X 66MHz
1.57V and 4V	> 1.57V	PCI-X 100MHz
> 4V	> 1.57V	PCI-X 133MHz

Note – PCI-X speeds and available slots on a Compact PCI backplane is limited. See "C5000 Capabilities relating to PICMG Specifications" on page 55 for more detailed information.

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PCI(-X) Clock Initialization

The PCI(-X)-to-PCI(-X) bridge uses different clock inputs when it is in System Slot (Universal Transparent Mode) or when it is in Peripheral Slot (Universal Non-Transparent Mode). Since the secondary clocks of the bridge are not recommended for PCI-X use, a high quality clock buffer is used.

IDSEL Assignment

The PCI signal IDSEL is used to provide unique access to each logical slot for configuration purposes. By connecting one of the address lines AD31 through AD25 to each board's IDSEL pin (J1:B9), a unique address for each board is provided during configuration cycles. IDSEL on the C5000 is valid only in Non-Transparent mode.

Geographical Addressing

The C5000 supports geographical addressing for unique slot identification. The physical slot address is encoded on the backplane by grounding and leaving unconnected different combination of pins GA[4:0] at each connector.

REQ# and GNT# Assignment

In system slot configuration the C5000 supports the full complement of REQ# and GNT# signals.

Push Button Reset (PRST#)

PRST# is used to reset the System Slot board, which in turn resets the rest of the system using the PCI RST# signal. PRST# is an active low true TTL signal generated by a switch closure or an open-collector driver.

System Slot Identification (SYSEN#)

This pin is grounded on the CompactPCI backplane segment at the System Slot. This pin is not connected on the backplane for the remaining slots. The C5000 senses this signal and disable all System Slot functions, such as clock generation and arbitration when it is not installed in a System Slot.

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Miscellaneous Functions

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6.1 JTAG Chain

Chain Topology

The JTAG Chain is divided into three segments:

- Processor
- CPLDs
- Other JTAG devices

Each segment is used for a specific set of similar devices, and can be accessed separately from the remaining parts of the JTAG chain. This allows tools that only support certain devices to be used by only accessing the segment with supported devices.

For more information please contact VMETRO.

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6.2 Reset Network

The board reset network is centralized around the reset PLD. Output reset signals are routed first to the reset PLD before being propagated to the other board components.

The primary sources of reset are the power-up reset controller and reset button. Other sources are various software resets from the processor, PCI-X to PCI-X bridges and PMC modules etc.

The following devices are considered as possible reset sources:

- 2 PPMC sites
- 3 PCI6540 PCIX-to-PCIX bridges
- AMCC 440GX PowerPC processor
- Power cycle (cold boot)
- On-board reset button (warm boot)
- Reset via RJ-45 connector
- Reset from RTM board

Any kind of reset (or power up) is forwarded to the CPLD which ensures that all the components are reset correctly (without any reset loop).

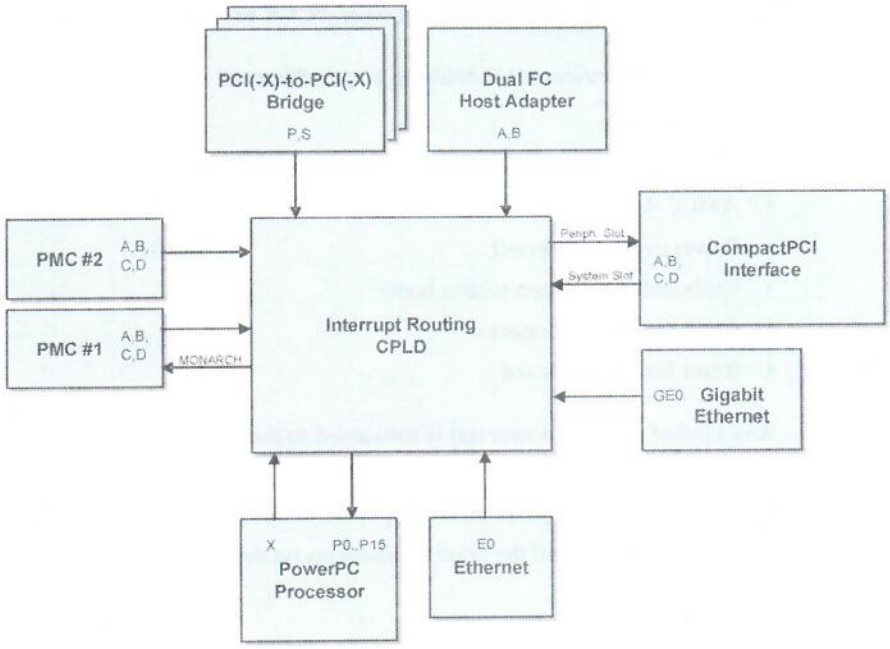
- The CPLD is always the first component to receive the initial reset signal.
- The CPLD resets all the other components on the board

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6.3 Interrupt Routing

In order to support a flexible interrupt routing mechanism, all interrupt source and destination signals are routed to a PLD which provides the actual routing between sources and destinations:

FIGURE 6-1
Interrupt Routing



The following devices are considered as possible interrupt sources:

- 2 PPMC sites (4 interrupt lines A,B,C and D)
- Intel LXT9785 Fast Ethernet controller (1 interrupt line E0)
- Marvel 88E1111 Gigabit Ethrenet Controller (2 interrupt lines GE0 and GE1)
- AMCC 440GX PowerPC processor (1 interrupt line X)
- 3 PCI6540 PCIX-to-PCIX bridges (2 interrupt lines P and S)
- ISP2312 PCIX-to-Dual FC Host Adapter (2 interrupt lines A and B)
- CompactPCI Interface (4 interrupt lines A, B, C, D); only when board configured as System Slot Board.

The following devices are considered as possible interrupt destinations:

- PPMC#1 site (4 interrupt lines A,B,C and D)
- AMCC 440GX PowerPC processor (16 interrupt lines P0 to P15)
- CompactPCI Interface (4 interrupt lines A, B, C, D); only when board configured as System Slot Board.

The following routing tables show the current interrupt mapping:

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Interrupt routing for PPMC#1

Destination	Source			
	PPMC2 A,B,C,D	CPCI A,B,C,D	PPC X	FC Controller A,B
A	A,C			A
B		A,C		B
C	B,D		X	
D		B,D		

Note – Interrupt signals routed to PMC #1 when PMC #1 available and configured as MONARCH

Interrupt Routing for CompactPCI Interface

Destination	Source		
	PPMC1 A,B,C,D	PPMC2 A,B,C,D	PPC X
A	A,C		
B		A,C	
C	B,D		X
D		B,D	

Note – Interrupt signals routed to CompactPCI interface only when board configured as peripheral device.

Temperature Sensors

There are several temperature sensors located on the board. One is close to the bottom of the board, one close to the top of the board and two located in the middle of the board.

The PowerPC processor communicates with the sensors via its second I2C bus. The type of component used is Maxim MAX1731. Contact VMETRO for more information.

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6.4 Power Supplies

The main sources of power are 3.3V, 5V and ±12V supplied by the CompactPCI backplane. The 3.3V and 5V power source is used to generate the required component voltages, ±12V is routed directly to the PMC sites.

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APPENDIXES

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A C5000 Capabilities relating to PICMG Specifications

Terminology in the PICMG specifications can be confusing as different standards may use different terms for the same thing. All underlined words/phrases in this document refer to the terminology used in the document referenced in the heading of that particular section.

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A-1 PICMG 2.0 - CompactPCI Specification

C5000 as a Peripheral Board (i.e. used in a Peripheral Slot)

C5000 is primarily designed to be used in a Peripheral Slot in a CompactPCI system running 33MHz or 66MHz, 32- or 64-bit PCI in the backplane.

	HW	SW	Comments
PCI Backplane interface			The P2P interfacing to the back plane is a non-transparent bridge. so that the board appears as an intelligent peripheral card. Memory space and BAR settings are configurable from the BSP.
PCI Auto-configuration			C5000 has a PCI Auto-configurator for the local C5000 PCI segments.
Hot swap	No*	No	*) See separate section on PICMG 2.1

C5000 as a System Slot Board (i.e. used in a in System Slot)

System slot functionality is designed into the C5000 board with small systems in mind. The typical target application for this is a data recorder system consisting of one (or more) C5000 board(s) and one (or more) Compact PCI ADC boards, with the backplane bus being used for initialization, setup and synchronization. Such configurations do not require a separate System slot board.

	HW	SW	Comments
System slot automatic detection	Yes	No	Software re configuration may be required when switching between use as System Slot. and Peripheral Board.
Arbiter	Yes	-	Up to 8 slot back planes
Clock generation	Yes	-	Up to 8 slot back planes. Auto detection of frequency (33MHz/ 66MHz) is supported.
Hot swap	No	No	
PCI Backplane interface			The P2P interfacing to the back plane is configured as a transparent bridge. No address translation provided by the bridge.
PCI Auto-configuration			An auto-configurator for the local C5000 PCI segments is provided.Contact VMETRO for details on configuring the backplane segment.
System enumeration (ENUM#)	No	No	The term "enumeration" is often used for functions like the initial set-up of the PCI address map. In PICMG 2.0 this term is only used related to Hot Swap capabilities. This is not supported by C5000.

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Other General Issues

PCI-X:

- There is no PICMG standard defining support for PCI-X in Compact PCI systems. There is the incomplete ECR (PICMG 2.0 Revision 3.0 ECR 001, R0.6a, 10/17/01) discussing how this could be done.
- C5000 supports PCI-X on all local PCI segments.
- Use of PCI-X across the backplane is not encouraged, but the bridge used to interface to the backplane supports PCI-X. The hardware is designed to allow PCI-X operation at 66, 100, and 133 MHz, in accordance with the above mentioned ECR. But since the ECR is not conclusive, any use of PCI-X across the backplane will require engineering to be involved to discuss design details and verification.

Mailbox interrupts: Mailbox interrupts are supported.

PICMG 2.1 - Hot Swap Specification

Hot Swap is not currently supported.

PICMG 2.16 - Packet Switching Backplane Specification

The C5000 provides dual GbE links through the CompactPCI Backplane connectors. These links can be used to connect either through a PICMG 2.16 backplane, or an RTM (C5000-RTM-xxx). Using one excludes the use of the other.

- Auto detect presence of a PICMG 2.16 backplane
- Auto detect 10/100/1000 Base-T operation

Node Board: C5000 supports both Link Port 'a' and Link Port 'b'. (Dual Link Port Node).

Fabric Board: The C5000 cannot operate as a Fabric Board.

PICMG 2.17 - StarFabric Specification

Hardware: C5000S-models have hardware support for PICMG 2.17 if a StarFabric PMC is used in PMC position 2. Two StarFabric links are routed from this PMC to J3 according to PICMG 2.17. This enables the use of C5000S in PICMG2.17 backplanes. In other backplanes, the RTM (C5000-RTM-xx) can be used to bring the StarFabric ports out on cables.

Basic Node Board:

- A Basic Node Board routes two StarFabric links to J3
- With PMC position 2 populated with a StarFabric PMC (like the CWCEC's SPMC-233) the C5000 can operate as a Basic Node Board.

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Multi-Segment Node Board:

- A Multi-Segment Node Board contains a StarFabric switch device, and routes four StarFabric links to J3
- The C5000 cannot operate as a Multi-Segment Node Board.

Fabric-Native Node Board:

- A Fabric-Native Node Board contains a StarFabric switch device, and routes two StarFabric links to J3 and another two links to J4
- The C5000 cannot operate as a Fabric-Native Node Board.

Fabric Board:

- A Fabric Board contains multiple StarFabric switches, and routes StarFabric links to J1, J2, J3, J4, J5.
- The C5000 cannot operate as a Fabric Board.

Software:

Contact VMETRO for further information.

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PLD Registers

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B-1 Miscellaneous PLD Registers

The PLD registers can be accessed by the processor in following address range:

TABLE B-1. PLD Registers

Offset (h)	Size (1 Byte)	Type	Register Name
0x00	1 Byte	Read	PPC Boot
0x01	1 Byte	Write	System Reset
0x02	1 Byte	Read	PCI Status
0x03	1 Byte	Read	PCI Clk
0x04	1 Byte	Read	PCIX Status
0x05	1 Byte	Read	Geographical Address
0x06	1 Byte	Read	Shelf Geographical Address
0x07	1 Byte	Read	System Controller Status
0x08	1 Byte	Read	Transparent Mode
0x09	1 Byte	Read	CompactPCI Misc
0x0A	Higher Nibble	Read	Interrupt PPC
0x0A	Lower Nibble	Read	Interrupt Ethernet (EMAC 0 or 1)
0x0B	Higher Nibble	Read	Interrupt P2P #1 Primary side
0x0B	Lower Nibble	Read	Interrupt P2P #2 Primary side
0x0C	Higher Nibble	Read	Interrupt P2P #3 Primary side
0x0C	Lower Nibble	Read	Interrupt P2P #1 Secondary side
0x0D	Higher Nibble	Read	Interrupt P2P #2 Secondary side
0x0D	Lower Nibble	Read	Interrupt P2P #3 Secondary side
0x0E	Higher Nibble	Read	Interrupt Fibre Channel #1
0x0E	Lower Nibble	Read	Interrupt Fibre Channel #2
0x0F	Higher Nibble	Read	Interrupt PMC #1 INTA
0x0F	Lower Nibble	Read	Interrupt PMC #1 INTB
0x10	Higher Nibble	Read	Interrupt PMC #1 INTC
0x10	Lower Nibble	Read	Interrupt PMC #1 INTD
0x11	Higher Nibble	Read	Interrupt PMC #2 INTA
0x11	Lower Nibble	Read	Interrupt PMC #2 INTB

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TABLE B-1. PLD Registers

0x12	Higher Nibble	Read	Interrupt PMC #2 INTC
0x12	Lower Nibble	Read	Interrupt PMC #2 INTD
0x13	Higher Nibble	Read	Interrupt ComapactPCI A
0x13	Lower Nibble	Read	Interrupt ComapactPCI B
0x14	Higher Nibble	Read	Interrupt ComapactPCI C
0x14	Lower Nibble	Read	Interrupt ComapactPCI D
0x15	Higher Nibble	Read	Interrupt GbE #0 (EMAC2)
0x15	Lower Nibble	Read	Interrupt GbE #1 (EMAC3)
0x16	Higher Nibble	Read	Test Register
0x16	Lower Nibble	Read	Test Register

PPC_BOOT

Address= 0x00
Register name = PPC_BOOT
Type = Read (R)

TABLE B-2. PPC_BOOT Register

Bit	Type	Register Bit Name	Comments
7	R	ECO_SPROM_WE#	ECO SPROM device 0: enabled 1: write-protected
6	R	PPC_ECC	PowerPC ECC Memory Access 0: ECC Memory used 1. ECC Memory not used
5	R	PPC_BOOT	PowerPC Boot Parameters 0: PCI Boot SROM 1: Flash Boot SPROM
4	R	FC_FWE#	QLOGIC ISP2312 FLASH device 0: enabled 1: write-protected
3	R	PPC_FVPEN#	PowerPC FLASH device 0: enabled 1: write-protected
2	R	PPC_FMWE#	PowerPC FLASH device (Monitor part) 0: enabled 1: write-protected
1	R	PPC_SWE#	PowerPC MFS SPROM device 0: enabled 1: write-protected
0	R	PPC_BSWE#	PowerPC Boot SPROM devices 0: enabled 1: write-protected

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System Reset

Address = 0x01
Register Name = System Reset
Type = Write (W)

TABLE B-3. System Reset Register

Bit	Type	Register Bit Name	Comments
0	W	System Reset	System Reset 1 (Peripheral Board): resets entire board 1 (System Controller): resets entire board and CompactPCI rack

PCI Status

Address: 0x02
Register Name: PCI Status
Type: Read (R)

TABLE B-4. PCI Status Register

Bit	Type	Register Bit Name	Comments
7	R	epciPres	CompactPCI Bus Present 0 CompactPCI bus not present 1 CompactPCI bus present
6	R	pmc1Mon	PMC #1 MONARCH 0 MONARCH 1 not MONARCH
5	R	pmc1Pres	PMC #1 Present 0 no PMC module 1 PMC module present
4	R	pmcERDY	PMC Site Ready 0 all PMC sites not ready 1 all PMC sites ready
3	R		
2	R		
1	R		
0	R		

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PCI_CLK

Address= 0x03
Register name = PCI_CLK
Type = Read (R)

TABLE B-5. PCI_CLK Register

Bit	Type	Register Bit Name	Comments
7	R	cpciMclk1#	CompactPCI Bus Clock Speed Bit 1 0:CLK speed not over 66MHz 1: CLK speed over 66MHz
6	R	cpciMclk0#	CompactPCI Bus Clock Speed Bit 0 0:CLK speed 33MHz or 100MHz 1: CLK speed 66MHz or 133MHz
5	R	p2Mclk1#	PMC#2 PCI(-X) Bus Clock Speed Bit 1 0:CLK speed not over 66MHz 1: CLK speed over 66MHz
4	R	p2Mclk0#	PMC#2 PCI(-X) Bus Clock Speed Bit 0 0: CLK speed 33MHz or 100MHz 1: CLK speed 66MHz or 133MHz
3	R	p1Mclk1#	PMC#1 PCI(-X) Bus Clock Speed Bit 1 0: CLK speed not over 66MHz 1: CLK speed over 66MHz
2	R	p1Mclk0#	PMC#1 PCI(-X) Bus Clock Speed Bit 0 0: CLK speed 33MHz or 100MHz 1: CLK speed 66MHz or 133MHz
1	R	procMclk1#	Processor PCI-X Bus Clock Speed Bit 1 0: CLK speed not over 66MHz 1: CLK speed over 66MHz
0	R	procMclk0#	Processor PCI-X Clock Speed Bit 0 0: CLK speed 33MHz or 100MHz 1: CLK speed 66MHz or 133MHz

TABLE B-6. Clock speed display

MCLK1	MCLK0	Clock Speed
0	0	33 MHz
0	1	66 MHz
1	0	100 MHz
1	1	133 MHz

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PCI-X Mode

Address: 0x04
Register Name: PCIX Mode
Type: Read (R)

TABLE B-7. PCI-X Mode Register

Bit	Type	Register Bit Name	Comments
7	R	cpciPcix	CompactPCI Bus Mode 0: PCI bus mode 1: PCI-X bus mode
6	R	pmc2Pcix	PMC #2 Bus Mode 0: PCI bus mode 1: PCI-X bus mode
5	R	pmc1Pcix	PMC #1 Bus Mode 0: PCI bus mode 1: PCI-X bus mode
4	R		
3	R		
2	R		
1	R		
0	R		

Geographical Address

Address = 0x05
Register name = Geographical Address
Type = Read (R)

TABLE B-8. Geographical Address Register

Bit	Type	Register Bit Name	Comments
7	R	cpciGA4	Geographical Addressing Bit 4
6	R	cpciGA3	Geographical Addressing Bit 3
5	R	cpciGA2	Geographical Addressing Bit 2
4	R	cpciGA1	Geographical Addressing Bit 1
3	R	cpciGA0	Geographical Addressing Bit 0
2	R		
1	R		
0	R		

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Shelf Geographical Address

Address: 0x06
Register Name: Shelf Geographical Address
Type: Read (R)

TABLE B-9. Shelf Geographical Address

Bit	Type	Register Bit Name	Comments
7	R	cpciSGA4	Shelf Geographical Address Bit4
6	R	cpciSGA3	Shelf Geographical Address Bit3
5	R	cpciSGA2	Shelf Geographical Address Bit2
4	R	cpciSGA1	Shelf Geographical Address Bit1
3	R	cpciSGA0	Shelf Geographical Address Bit0
2	R		
1	R		
0	R		

System Controller Status

Address: 0x07
Register Name: System Controller Status
Type: Read (R)

TABLE B-10. System Controller Status Register

Bit	Type	Register Bit Name	Comments
7	R	sysPullup33#	System Controller Board 3.3V Pull-up 0: 3.3V pull-ups to VIO disabled 1: 3.3V pull-ups to VIO enabled
6	R	sysPullup5#	System Controller Board 5V Pull-up 0: 5V pull-ups to VIO disabled 1: 5V pull-ups to VIO enabled
5	R	sysClken#	System Controller Board Clocks 0: Clocks disabled 1: Clocks enabled
4	R	sClkoff	CompactPCI bridge Secondary Clock 0: CompactPCI clock used (Peripheral Slot) 1: On-board clock used (System Slot)
3	R	p2p3Pllen#	CompactPCI Bridge PLL 0: Secondary PLL disabled (clock speed below 50MHz) 1: Secondary PLL enabled (clock speed above 50MHz)
2	R		
1	R		
0	R		

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Transparent Mode

Address: 0x08
Register Name: Transparent Mode
Type: Read (R)

TABLE B-11. Transparent Mode Register

Bit	Type	Register Bit Name	Comments
7	R	p2p3Trans	P2P #3 CompactPCI bridge mode 0: Non-Transparent Mode 1: Transparent Mode
6	R	p2p2Trans	P2P #2 Bridge Mode 0: Non-Transparent Mode 1: Transparent Mode
5	R	p2p1Trans	P2P #1 Bridge Mode 0: Non-Transparent Mode 1: Transparent Mode
4	R		
3	R		
2	R		
1	R		
0	R		

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CompactPCI Misc Register

Address: 0x09
Register Name: CompactPCI Misc
Type: Read (R)

TABLE B-12. CompactPCI Misc Register

Bit	Type	Register Bit Name	Comments
7	R	cpciDeg#	CompactPCI Power Supply Status DEG#
6	R	cpciFal#	CompactPCI Power Supply Status FAL#
5	R	rtmDetect	RTM Board Detection 0: no RTM board 1: RTM board detected
4	R	cpciHealthy#	CompactPCI Hot Swap Healthy# 0: all Hot Swap power supplies within tolerance 1: one/more Hot Swap power supplies outside tolerance
3	R	vioTres	CompactPCI VIO Detection 0: VIO = 3.3V 1: VIO = 5V
2	R		
1	R		
0	R		

INTERRUPT Registers

TABLE B-13. Interrupt Registers

Address	Register[7-4]	Register[3-0]
0x0A	PPC	Ethernet (EMAC 0 or 1)
0x0B	P2P #1 Primary side	P2P #2 Primary side
0x0C	P2P #3 Primary side	P2P #1 Secondary side
0x0D	P2P #2 Secondary side	P2P #3 Secondary side
0x0E	Fibre Channel #1	Fibre Channel #2
0x0F	PMC #1 A	PMC #1 B
0x10	PMC #1 C	PMC #1 D
0x11	PMC #2 A	PMC #2 B
0x12	PMC #2 C	PMC #2 D
0x13	CompactPCI A	CompactPCI B
0x14	CompactPCI C	CompactPCI D
0x15	GbE #0 (EMAC2)	GbE #1 (EMAC3)
0x16	Test Register	Test Register

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Connector Pinouts

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C-1 CompactPCI J1 Connector Pinout

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J1	25	GND	CPCI_VCC	CPCI_VDD	ENUM#	REQ64#	CPCI_VCC
J1	24	GND	ACK64#	AD[0]	V(I/O)	CPCI_VCC	AD[1]
J1	23	GND	AD[2]	5V	AD[3]	AD[4]	3.3V
J1	22	GND	AD[5]	AD[6]	CPCI_VDD	GND	AD[7]
J1	21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	3.3V
J1	20	GND	AD[10]	AD[11]	V(I/O)	GND	AD[12]
J1	19	GND	AD[13]	GND	AD[14]	AD[15]	CPCI_VDD
J1	18	GND	C/BE[1]#	PAR	CPCI_VDD	GND	SERR#
J1	17	GND	PERR#	GND	IPMB_SDA	IPMB_SCL	CPCI_VDD
J1	16	GND	LOCK#	STOP#	V(I/O)	PCIXCAP	DEVSEL#
J1	15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	CPCI_VDD
J1	14	Key Area					
J1	13						
J1	12						
J1	11	GND	C/BE[2]#	GND	AD[16]	AD[17]	AD[18]
J1	10	GND	AD[19]	AD[20]	CPCI_VDD	GND	AD[21]
J1	9	GND	AD[22]	GND	AD[23]	IDSEL	C/BE[3]#
J1	8	GND	AD[24]	AD[25]	V(I/O)	GND	AD[26]
J1	7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]
J1	6	GND	AD[31]	CLK0	CPCI_VDD	PCI_PRESENT#	REQ0#
J1	5	GND	GNT0#	GND	RST#	BRSVP1B5	BRSVP1A5
J1	4	GND	INTS	INTP	V(I/O)	HEALTHY#	IPMB_PWR
J1	3	GND	INTD#	CPCI_VCC	INTC#	INTB#	INTA#
J1	2	GND	TDI	TDO	TMS	CPCI_VCC	TCK
J1	1	GND	CPCI_VCC	+12V	TRST#	-12V	CPCI_VCC

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C-2 CompactPCI J2 Connector Pinout

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J2	22	GND	GA0	GA1	GA2	GA3	GA4
J2	21	GND				GND	CLK6
J2	20	GND		GND		GND	CLK5
J2	19	GND				GND	GND
J2	18	GND		GND			
J2	17	GND	GNT6#	REQ6#	PRST#	GND	
J2	16	GND		GND	DEG#		
J2	15	GND	GNT5#	REQ5#	FAL#	GND	
J2	14	GND	AD[32]	GND	AD[33]	AD[34]	AD[35]
J2	13	GND	AD[36]	AD[37]	V(I/O)	GND	AD[38]
J2	12	GND	AD[39]	GND	AD[40]	AD[41]	AD[42]
J2	11	GND	AD[43]	AD[44]	V(I/O)	GND	AD[45]
J2	10	GND	AD[46]	GND	AD[47]	AD[48]	AD[49]
J2	9	GND	AD[50]	AD[51]	V(I/O)	GND	AD[52]
J2	8	GND	AD[53]	GND	AD[54]	AD[55]	AD[56]
J2	7	GND	AD[57]	AD[58]	V(I/O)	GND	AD[59]
J2	6	GND	AD[60]	GND	AD[61]	AD[62]	AD[63]
J2	5	GND	PAR64	C/BE[4]#	V(I/O)	64EN	C/BE[5]#
J2	4	GND	C/BE[6]#	GND	C/BE[7]#		V(I/O)
J2	3	GND	GNT4#	REQ4#	GNT3#	GND	CLK4
J2	2	GND	REQ3#	GNT2#	SYSEN#	CLK3	CLK2
J2	1	GND	REQ2#	GNT1#	REQ1#	GND	CLK1

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C-3 CompactPCI J3 Connector Pinout

TABLE C-1. Pinout for StarFabric C5000 boards

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A	
J3	19	GND	SGA[0]	SGA[1]	SGA[2]	SGA[3]	SGA[4]	Shelf Addressing
J3	18	GND	LPA_DN[2]	LPA_DP[2]	GND	LPA_DN[0]	LPA_DP[0]	2 x GbE PICMG 2.16
J3	17	GND	LPA_DN[3]	LPA_DP[3]	GND	LPA_DN[1]	LPA_DP[1]	
J3	16	GND	LPB_DN[2]	LPB_DP[2]	GND	LPB_DN[0]	LPB_DP[0]	
J3	15	GND	LPB_DN[3]	LPB_DP[3]	GND	LPB_DN[1]	LPB_DP[1]	
J3	14	GND	GND	GND	GND	GND	GND	Isolation Row
J3	13	GND	PMC2-6	PMC2-5	PMC2-10	PMC2-9	PMC2-14	
J3	12	GND	PMC2-11	PMC2-16	PMC2-15	PMC2-20	PMC2-19	
J3	11	GND	PMC2-13	PMC2-18	PMC2-17	PMC2-22	PMC2-21	
J3	10	GND	GND	GND	GND	GND	GND	Isolation Row
J3	9	GND	PMC2-30	PMC2-28	GND	PMC2-40	PMC2-38	
J3	8	GND	PMC2-34	PMC2-32	GND	PMC2-44	PMC2-42	
J3	7	GND	PMC2-33	PMC2-31	GND	PMC2-43	PMC2-41	StarFabric PICMG 2.17
J3	6	GND	PMC2-29	PMC2-27	GND	PMC2-39	PMC2-37	
J3	5	GND	PMC2-50	PMC2-48	GND	PMC2-60	PMC2-58	
J3	4	GND	PMC2-54	PMC2-52	GND	PMC2-64	PMC2-62	
J3	3	GND	PMC2-53	PMC2-51	GND	PMC2-63	PMC2-61	
J3	2	GND	PMC2-49	PMC2-47	GND	PMC2-59	PMC2-57	
J3	1	GND	GND	GND	GND	GND	GND	Isolation Row

Note – On C5000 StarFabric boards all PMC signals marked with 0ohm in between are left open at the PMC #2 site. At the CompactPCI backplane site these signals are grounded (Isolation Row), except from J3-A19 and J3-B19.
In a StarFabric backplane, row 19 is used for Shelf Geographical Addressing.

TABLE C-2. Pinout for Non-StarFabric C5000 boards

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A	
J3	19	GND				PMC2-1	PMC2-2	0Ohm in series
J3	18	GND	LPA_DN[2]	LPA_DP[2]	GND	LPA_DN[0]	LPA_DP[0]	2 x GbE PICMG 2.16
J3	17	GND	LPA_DN[3]	LPA_DP[3]	GND	LPA_DN[1]	LPA_DP[1]	
J3	16	GND	LPB_DN[2]	LPB_DP[2]	GND	LPB_DN[0]	LPB_DP[0]	
J3	15	GND	LPB_DN[3]	LPB_DP[3]	GND	LPB_DN[1]	LPB_DP[1]	
J3	14	GND	PMC2-4	PMC2-3	PMC2-8	PMC2-7	PMC2-12	0Ohm in series
J3	13	GND	PMC2-6	PMC2-5	PMC2-10	PMC2-9	PMC2-14	
J3	12	GND	PMC2-11	PMC2-16	PMC2-15	PMC2-20	PMC2-19	
J3	11	GND	PMC2-13	PMC2-18	PMC2-17	PMC2-22	PMC2-21	
J3	10	GND	PMC2-24	PMC2-23	PMC2-26	PMC2-25	PMC2-36	0Ohm in series
J3	9	GND	PMC2-30	PMC2-28	GND	PMC2-40	PMC2-38	
J3	8	GND	PMC2-34	PMC2-32	GND	PMC2-44	PMC2-42	
J3	7	GND	PMC2-33	PMC2-31	GND	PMC2-43	PMC2-41	
J3	6	GND	PMC2-29	PMC2-27	GND	PMC2-39	PMC2-37	
J3	5	GND	PMC2-50	PMC2-48	GND	PMC2-60	PMC2-58	
J3	4	GND	PMC2-54	PMC2-52	GND	PMC2-64	PMC2-62	
J3	3	GND	PMC2-53	PMC2-51	GND	PMC2-63	PMC2-61	
J3	2	GND	PMC2-49	PMC2-47	GND	PMC2-59	PMC2-57	
J3	1	GND	PMC2-35	PMC2-46	PMC2-45	PMC2-56	PMC2-55	0Ohm in series

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C-4 CompactPCI J5 Connector Pinout

Connector	Position	Row F	Row E	Row D	Row C	Row B	Row A
J5	22	GND	PMC1-1	PMC1-2	PMC1-3	PMC1-4	PMC1-5
J5	21	GND	PMC1-6	PMC1-7	PMC1-8	PMC1-9	PMC1-10
J5	20	GND	PMC1-11	PMC1-12	PMC1-13	PMC1-14	PMC1-15
J5	19	GND	PMC1-16	PMC1-17	PMC1-18	PMC1-19	PMC1-20
J5	18	GND	PMC1-21	PMC1-22	PMC1-23	PMC1-24	PMC1-25
J5	17	GND	PMC1-26	PMC1-27	PMC1-28	PMC1-29	PMC1-30
J5	16	GND	PMC1-31	PMC1-32	PMC1-33	PMC1-34	PMC1-35
J5	15	GND	PMC1-36	PMC1-37	PMC1-38	PMC1-39	PMC1-40
J5	14	GND	PMC1-41	PMC1-42	PMC1-43	PMC1-44	PMC1-45
J5	13	GND	PMC1-46	PMC1-47	PMC1-48	PMC1-49	PMC1-50
J5	12	GND	PMC1-51	PMC1-52	PMC1-53	PMC1-54	PMC1-55
J5	11	GND	PMC1-56	PMC1-57	PMC1-58	PMC1-59	PMC1-60
J5	10	GND	PMC1-61	PMC1-62	PMC1-63	PMC1-64	VDD
J5	9	GND	PHY_LED[0]	PHY_LED[1]	VDD	PHY_LED[2]	PHY_LED[3]
J5	8	GND	SCLK_P[0]	SCLK_N[0]	VCC	PPC_SCL2	PPC_SDA2
J5	7	GND	SCLK_P[1]	SCLK_N[1]	VDD	VCC	
J5	6	GND	PHY_LED[4]	PHY_LED[5]	CPCI_VDD	PHY_LED[6]	PHY_LED[7]
J5	5	GND	RS_R	RS_R#	RJ45_RST#	RTM_DETECT	+12V
J5	4	GND	RS_T	RS_T#	E_TPOP	E_TPON	E_TPIP
J5	3	GND	E_LED[1]	E_LED[2]	E_LED[3]	-12V	E_TPIN
J5	2	GND	SOUT_N[0]	SOUT_P[0]	GND	SIN_N[0]	SIN_P[0]
J5	1	GND	SOUT_N[1]	SOUT_P[1]	GND	SIN_N[1]	SIN_P[1]

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PMC Connector Pinout

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D-1 General Description

"NC" means Not Connected.

"PU" and "PD" mean that the connector pin is connected to +5V via a pull up resistor or to ground (GND) via a pull down resistor respectively.

Pins that are PU, PD or NC for compliance with otherwise unsupported PCI signals have the PCI signal name appended in parenthesis.

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D-2 PMC Connector Pinout - Jn1 for both PMC slots on all Models

Jn1 64 Bit PCI

TABLE D-1. Pinout for PMC connector Jn1 (both slots/all models)

Pin#	Signal Name	Pin#	Signal Name
1	PD (TCK)	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	NC (PCI-RSVD)
11	GND	12	NC (PCI-RSVD)
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V (I/O)	20	AD[31]
21	AD[28]	22	AD[27]
23	AD[25]	24	GND
25	GND	26	C/BE[3]#
27	AD[22]	28	AD[21]
29	AD[19]	30	+5V
31	V (I/O)	32	AD[17]
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	PU (SDONE#)	42	PU (SBO#)
43	PAR	44	GND
45	V (I/O)	46	AD[15]
47	AD[12]	48	AD[11]
49	AD[09]	50	+5V
51	GND	52	C/BE[0]#
53	AD[06]	54	AD[05]
55	AD[04]	56	GND
57	V (I/O)	58	AD[03]
59	AD[02]	60	AD[01]
61	AD[00]	62	+5V
63	GND	64	REQ64#

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D-3 PMC Connector Pinout - Jn2 for both PMC slots on all Models

Jn2 64 Bit PCI

TABLE D-2. Pinout for PMC connector Jn2 (both slots/all models)

Pin#	Signal Name	Pin#	Signal Name
1	+12V	2	PD (TRST#)
3	PD (TMS)	4	NC (TDO)
5	PD (TDI)	6	GND
7	GND	8	NC (PCI-RSVD)
9	NC (PCI-RSVD)	10	NC (PCI-RSVD)
11	PU (BUSMODE2#)	12	+3.3V
13	RST#	14	PD (BUSMODE3#)
15	3.3V	16	PD (BUSMODE4#)
17	NC (PCI-RSVD)	18	GND
19	AD[30]	20	AD[29]
21	GND	22	AD[26]
23	AD[24]	24	+3.3V
25	IDSEL	26	AD[23]
27	+3.3V	28	AD[20]
29	AD[18]	30	GND
31	AD[16]	32	C/BE[2]#
33	GND	34	IDSELB
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE[1]#	44	GND
45	AD[14]	46	AD[13]
47	M66EN	48	AD[10]
49	AD[08]	50	+3.3V
51	AD[07]	52	REQB#
53	+3.3V	54	GNTB#
55	NC (PMC-RSVD)	56	GND
57	NC (PMC-RSVD)	58	EREADY
59	GND	60	RESETOUT#
61	ACK64#	62	+3.3V
63	GND	64	MONARCH#/PU

Note – MONARCH is connected for PMC#1 only (pull-up for PMC#2).

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D-4 PMC Connector Pinout - Jn3 for both PMC Slots on all Models

Jn3 64 Bit PCI

TABLE D-3. **Pinout for PMC connector Jn3 (both slots/all models)**

Pin#	Signal Name	Pin#	Signal Name
1	NC (PCI-RSVD)	2	GND
3	GND	4	C/BE[7]#
5	C/BE[6]#	6	C/BE[5]#
7	C/BE[4]#	8	GND
9	V (I/O)	10	PAR64
11	AD[63]	12	AD[62]
13	AD[61]	14	GND
15	GND	16	AD[60]
17	AD[59]	18	AD[58]
19	AD[57]	20	GND
21	V (I/O)	22	AD[56]
23	AD[55]	24	AD[54]
25	AD[53]	26	GND
27	GND	28	AD[52]
29	AD[51]	30	AD[50]
31	AD[49]	32	GND
33	GND	34	AD[48]
35	AD[47]	36	AD[46]
37	AD[45]	38	GND
39	V (I/O)	40	AD[44]
41	AD[43]	42	AD[42]
43	AD[41]	44	GND
45	GND	46	AD[40]
47	AD[39]	48	AD[38]
49	AD[37]	50	GND
51	GND	52	AD[36]
53	AD[35]	54	AD[34]
55	AD[33]	56	GND
57	V (I/O)	58	AD[32]
59	NC (PCI-RSVD)	60	NC (PCI-RSVD)
61	NC (PCI-RSVD)	62	GND
63	GND	64	NC (PCI-RSVD)

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MBTF Values

The Mean Time Between Failures (MBTF) values given here are calculated estimations representing the inherent reliability of the c5210 series SBCs.

The prediction is done according to the Inherent Model in PRISM v1.5 (System reliability assessment tool). PRISM contains experience data and methods for predicting component reliability.

Values are calculated for different environments but this does not mean that operation in this environment is supported. These environments are:

GB (Ground Benign): Locations with controlled temperature and humidity.

GF (Ground Fixed): Locations with moderately controlled environment.

NS (Naval Sheltered): Includes sheltered or below deck conditions on surface ship and equipment installed in submarines.

AIC (Airborne Inhabited Cargo): Typical conditions in cargo compartments, which can be occupied by aircrew.

ARW (Airborne Rotary Winged): Equipment installed on helicopters.

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TABLE E-1. MTBF Values (Hours)

GB (25°C)	GF (35°C)	NS (40°C)	AIC (50°C)	ARW (50°C)	ARW (75°C)

For MBTF values of other models, please contact VMETRO.

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Ordering Information

Models

	AMCC 440GX PowerPC Processor	133 MHz PCI-X PMC Positions	High Speed Streaming Memory	RJ45 10/100 Ethernet	Optical 2Gb/s Fibre Channel	RJ45 Gigabit Ethernet	Optical Gigabit Ethernet
C5210-EFF	1	2	1024MiB	1	2	-	-

In addition:

-4 option: RS-422 instead of RS-232 for the second serial line

C5210v-wXYZ where:

C is for Compact PCI MIDAS
5 represents this generation of Midas product
2 is for the two PMC positions
1 is for the number of PPCs ('0'=pure carrier, '1'=intelligent)
0 = 667MHz processor, 1 = 800MHz processor

v: S for Star Fabric option

w: E for Fast Ethernet (default)

xy: F for Fibre Channel port installed (up to two ports), 0 Fibre Channel not installed

z: 4 for RS422 instead of RS-232 on second serial line.

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Technical Support

In order for us to provide fast technical support, please provide the following information:

- Any modifications made to the default BSP.
- Any changes to the default versions of the flash files, such as mmon.ini and vxbsp.ini.
- Detailed description of all symptoms observed, including serial port output and analyzer trace files if applicable
- Information about 3rd party drivers and HW that is used.

North and South America

Telephone Support	(281) 584-0728
Fax	(281) 584-9034
Website	http://www.vmetro.com/support

Europe and the rest of the world

Telephone Support	+47 23 17 28 00
Fax	+47 23 17 28 01
Website	http://www.vmetro.com/support

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References

The Fibre Channel Industry Association (FCIA)
http://www.fibrechannel.org

American National Standards Institute
http://www.ansi.org

PCI-SIG (PCI Special Interest Group)
http://www.pcisig.com

PICMG (PCI Industrial Computer Manufacturers Group)
http://www.picmg.org/

Component Manufacturers

Vendor	Component	Available documentation
AMCC http://www.amcc.com/	440GX Processor	Processor Developers Manual Application Notes and more
PLX Technology http://www.plxtech.com	PCI 6540 PCI-X to PCI-X Bridge	Data sheet and more

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