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# DPI02

## FPDP/FPDP II Digital Parallel I/O PMC Module



VMETRO

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# DPIO2

## FPDP/FPDP II Digital Parallel I/O PMC Module

Features:

**Host Interface**
- 64-bit 33(66)MHz PCI Bus
- Advanced Linked List DMA
- DMA transfer triggered by FIFO level
- End of transfer capability, optional jump to next DMA descriptor
- All byte swap operations: Byte, Word and Double Word

**FIFO**
- 128 or 512 KBytes deep
- Data transferred by on-board DMA or Remote PCI Master
- PCI interrupt on FIFO levels

**Bi-directional design**
- Input/output mode selection under software control

**Front-end processing**
- Packing options, 1x32, 2x16 or 3x10-bits as standard. Others on request.
- Advanced synchronization control features
- Sample Skip & Store counters

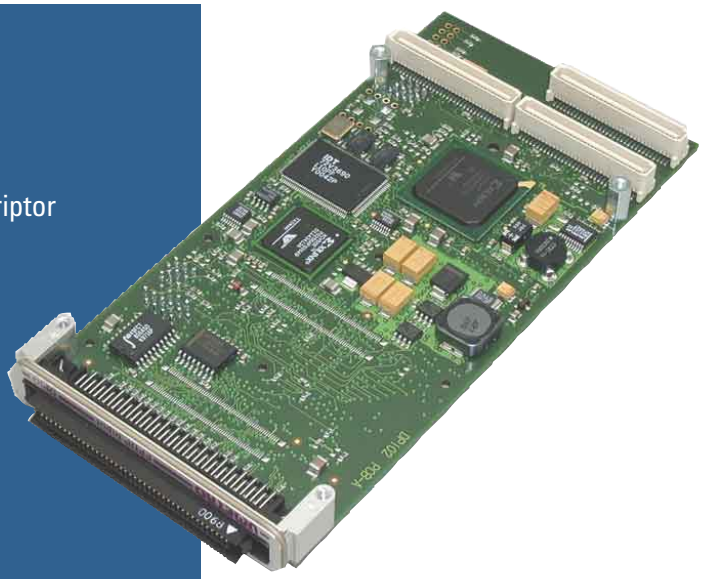
**Clocking options**
- Both input and output modules can use internal or external clock under software control
- Programmable clock generator from 500KHz to 50MHz

**Personality modules**
- LVDS & PECL versions available
- No Personality Module needed for standard TTL FPDP signaling

**FPDP interface**
- FPDP/FPDP II compatible 32-bits parallel data I/O
- FPDP II up to 400MB/s, standard FPDP up to 160MB/s
- Supports unframed, single or repeating, fixed or dynamic size framed data
- PCI Interrupt on Suspend assertion
- SUSPEND asserted by software control or FIFO high watermark
- LED indicators for SUSPEND, STROB, NRDY, DVALID and SYNC

**Software Drivers**
- VxWorks™
- Windows-2000™/NT™
- MC/OS™

**Miscellaneous**
- Rugged and extended temperature versions available



### INTRODUCTION

DPIO2 is the second generation high speed digital parallel input output PMC module from VMETRO. The new DPIO2 architecture handles the transfer speed requirements imposed by the PCI interface and the FPDP II's improved bandwidth. The advanced capabilities of the linked list DMA controller combined with the I/O handling features of the front-end FPGA will handle most data frame formats used in the data acquisition and signal processing environments. The speed is achieved by using a clock rate of 50 MHz sampling data on both edges. The module also supports the original FPDP and the basic card comes with the standard FPDP TTL signaling. Separate models also support other signal standards such as LVDS and PECL.

In large volume deliveries, the generous capabilities of the on-board FPGAs have potential for custom programming for special handling of data formats such as timestamp insertion and specific framing.

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## Benefits:

- Bi-directional design allows input or output mode under software control
- Flexible set of DMA modes and Synchronization methods to suit almost any parallel digital I/O application
- Usage spans from simple contiguous or short framed A/D input to fixed or variable length advanced framing input such as digital video
- Packing capability of narrow samples conserves PCI bandwidth
- Powerful architecture ready for advanced custom applications

## Applications:

- Radar and sonar
- High-speed data acquisition
- Digital receivers
- Spectrum and transient analysis
- Test equipment

The DPIO2 is a PCI Mezzanine Card (PMC) designed for high-speed data acquisition and generation. It combines a Digital Parallel Input or Output on one end, and a 64-bit PCI bus master/slave interface with an advanced DMA controller on the other end, with a large FIFO in between.

The PCI Interface chip provides a 64-bit PCI bus master/slave interface with a linked list DMA engine. The parallel interface is available through the front panel connector. The logical interface is based on the FPDP protocol. The electrical interface can be TTL (FPDP compliant), RS-422/485, PECL or LVDS, depending on what version of the DPIO2 is used. The DPIO2 can be delivered with two FIFO sizes, either 32 or 128 Kwords. Different packing options are available: 1x32-bit, 2x16-bit or 3x10-bit can be selected, while 4x8-bit or 8x4-bit is available on request. That means that the front panel port can use less than 32-bits, but the data cycles on PCI will always will have the optimal width (32-bit or 64-bit). When using the DMA engine, both single and linked-list DMA is supported. For linked-list DMA, 64K of descriptors are set up in the onboard SSRAM (Synchronous Static RAM), eliminating PCI contention that would occur if the descriptors were stored in host memory.

The DPIO2 is the second generation FPDP PMC (PCI Mezzanine Card) from VMETRO, now also supporting FPDP II in addition to original FPDP features. FPDP II is the new de-facto standard for high-speed parallel I/O. It is designed for digital data acquisition or generation at data rates up to 100 Msamples/sec or 400 MBytes/sec. Typically, the module is used to transfer huge amounts of raw sensor data between A/D or D/A converters and processors or memory/storage systems. The rich set of features makes DPIO2 suitable for advanced parallel I/O such as digital video and variable length framed data.

The DPIO2 is available with drivers for VxWorks, MC/OS and Windows 2000/NT. Driver source code is available for the purpose of porting it to other platforms.

## FPDP AND FPDP II COMPATIBLE

The VITA Standards Organization (VSO) adopted FPDP, and this resulted in the ANSI/VITA 17-1997 Front Panel Data Port standard.

The continuing demand for higher speed data acquisition, processing and storage systems required an increase in throughput of FPDP. Consequently, a second generation FPDP, called FPDP II was proposed.

The -FB version of the DPIO2 is fully compatible with the original FPDP (Front Panel Data Port) and the new FPDP II, both of which define 32-bit synchronous input/output parallel interfaces. FPDP is specified to operate at clock rates up to 40MHz, while FPDP II is specified to operate up to 50 MHz with clocking on both edges.

The double-edged clock in FPDP II doubles the bandwidth with no “real” increase in cable bandwidth. FPDP II builds on top of the strengths of FPDP and more than doubles the FPDP data-rate from 160 to 400 MBytes/sec. FPDP II is backwards compatible with FPDP, hence reducing the necessary engineering effort for upgrading an application, whilst keeping existing systems compatible with new solutions.

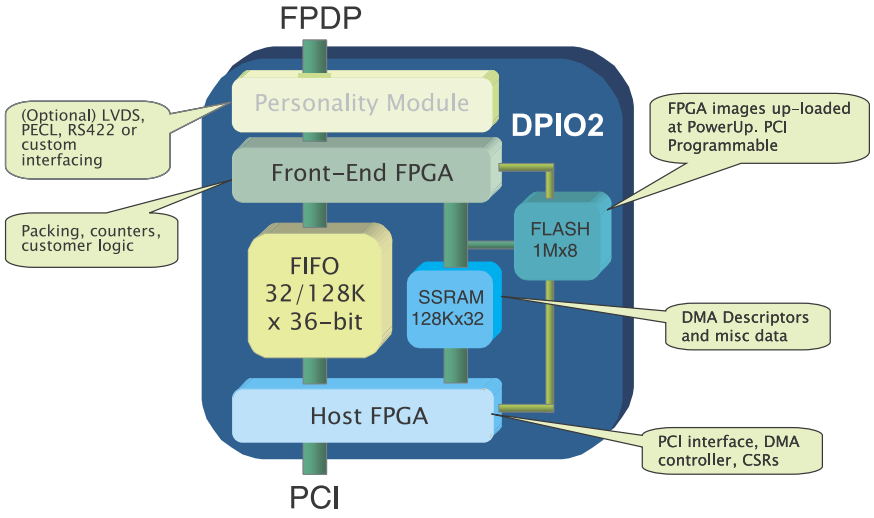



*Fig: DPIO2 - Functional Block Diagram*


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## ALTERNATIVE SIGNAL INTERFACES - LVDS, RS-422/485 and PECL

The DPIO2 PMC module is implemented with a very flexible I/O stage which can be factory configured in a number of different ways. In order to accommodate electrical interfaces other than the standard TTL such as differential signaling, there is a front-end "personality module" which holds the input buffers or line drivers that fit the application. The other DPIO2 models, -L (LVDS), -D (RS-422/485) and -E (PECL) implement the same logical interface as FPDP, but use different signaling voltages and thresholds according to these standards. This allows for longer cable lengths and better noise suppression. Even custom personality modules can be made containing application specific signal buffering.

## PACKING / UNPACKING CONSERVES PCI BANDWIDTH

In the front-end FPGA just behind the optional personality module, there is a packing/unpacking stage. This allows smaller data I/O widths to be packed into the 32-bit FIFO word size, thereby significantly reducing the load on the PCI bus. The standard packing options provided are 3x10 bit, 2x16 bit or unpacked from a 32-bit word. Other packing options are available on request.

## 32 or 128 KWord FIFO

The DPIO2 is equipped with a large 512KByte data FIFO or an optional lower cost 128KByte option. A status register, accessible via PCI includes status flags to indicate Empty, Almost Empty, Less than Half Full, More Than Half Full, Almost Full and Full. Certain FIFO status can also be set up to generate interrupts and to trigger the start of DMA transfers (Demand Mode).

## LINKED-LIST DMA CONTROLLER

The Host FPGA in the DPIO2 includes a flexible DMA-controller with linked-list capability. This can be used to transfer data to/from different memory locations in the PCI address map. This can be local memory on the base board, or remote memory on VMEbus or RACEway/ RACE++ if the DPIO2 is installed on a suitable PMC carrier such as VMETRO's PowerMIDAS.

The DMA descriptors are stored in a 1 Mbyte SSRAM available on the local bus of the DPIO2. The descriptors are initialized from the host CPU via PCI bus. The SSRAM can also be used as a general purpose RAM memory available from any PCI bus master. DMA can be initiated by register access from a processor via PCI bus, a direct hardware signal from the FIFO status outputs (Demand Mode), or Wait-for-SYNC (FPDP).

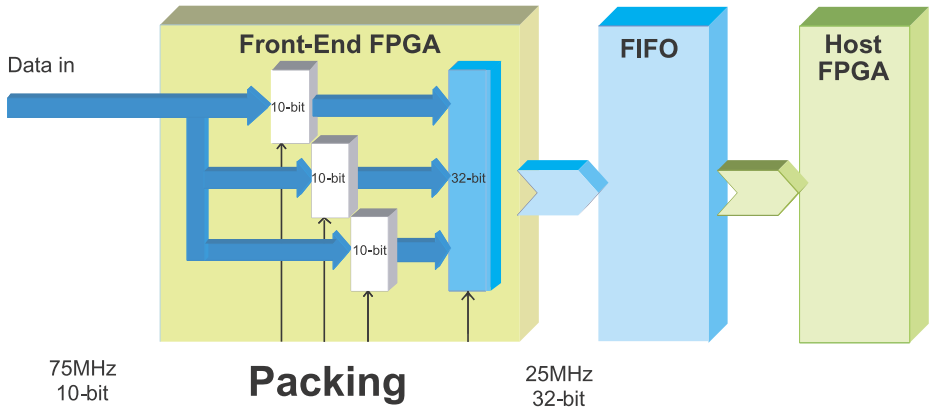



*Fig: DPIO2 data packing (example shows 3x10-bits)*

## SYNCHRONIZATION ON INPUT

The signals SYNC, PIO1, PIO2 or RES1 can be configured to generate an End-Of-Transfer (EOT) event. The EOT event can be set up to automatically abort the current DMA transfer and optionally jump to the next DMA descriptor in the chain. This function is especially useful in handling variable length frames delimited by a synchronizing signal.

## SYNCHRONIZATION ON OUTPUT

In output mode the SYNC signal can be generated at particular points in the data stream in order to provide various types of data frame synchronization. The available modes are:

- Assert SYNC prior to first sample of frame
- Assert SYNC together with last sample of frame
- Assert SYNC together with first sample of frame
- Assert SYNC during entire frame
- Assert SYNC every nth sample

## DPIO2 PERFORMANCE

The DPIO2 has a measured maximum sustained PCI performance of 255.6 MBytes/sec using the on- board DMA engine to move data from DPIO2 to PCI. This represents a 96% utilization of the available bandwidth of the 64-bit 33 MHz PCI bus. The DPIO2 is also being developed for the 66MHz PCI bus (-FB3/-LB3 versions). This will provide performance in excess of 500 Mbytes/sec, fully capable of transferring the full FPDP II bandwidth of 400 Mbytes/sec to/from the host PCI memory space.

## DEMAND MODE DMA

To ensure efficient utilization of the PCI bus when the DPIO2 acts as a BUS MASTER, it can be set to trigger DMA at Half Full FIFO level. This mode is called Demand Mode, in which all the data in the FIFO is sent in efficient size bursts to the PCI bus. This is very important if many PMC devices share the same PCI segment such as in applications where many data streams are merged.


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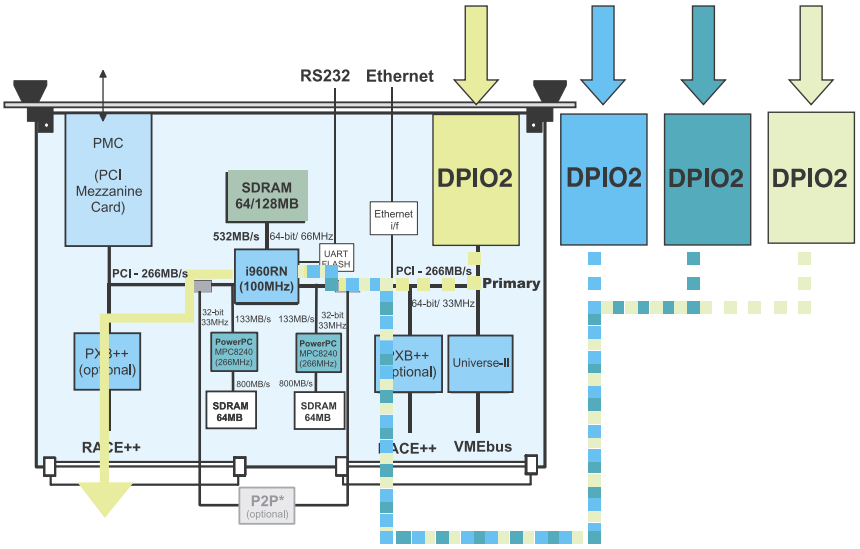



*Fig: Merging data streams, several DPIO2s bursting data onto one PCI segment (using the PowerMIDAS-3520 with 5 PMC positions.)*

## BYTE SWAPPING

The Host FPGA may perform byte swapping of data presented to PCI, avoiding software intervention to unscramble data if transferred to a big endian system. All types of swapping can be performed, byte, word and double word, and any combinations of them.

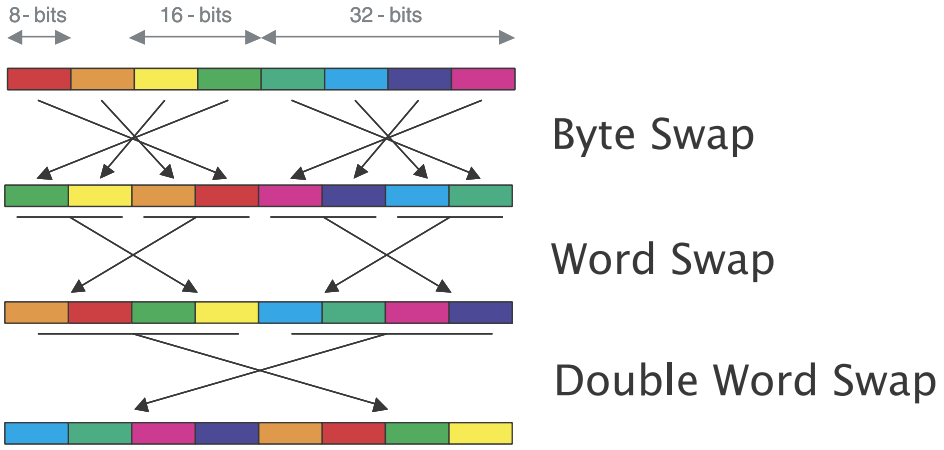



*Fig: Any combination of 8-bit, 16-bit and 32-bit swapping can be performed*

## INTERRUPT TO PCI

For maximum flexibility and throughput, the module can be programmed to generate four types of interrupts to PCI. These are:

- End of DMA Transfer (single DMA or end of chain completed)
- FIFO state: Not Empty, Empty, Almost Empty, Half Full, Almost Full, Full and Overflow
- User Input Signal asserted: PIO1, PIO2, SYNC, SUSPEND
- PCI Bus error

## CLOCKING MODES

All clocking modes are supported, both clock master and clock slave, both in input and output modes. As a clock master the DPIO2 has a software programmable clock rate from 500 KHz to 50 MHz.

## PROGRAMMABLE I/O BITS

The DPIO2 offers two programmable I/O bits (PIO1 and PIO2) through the front panel connector. These can be programmed to be either input or output, independently of whether the DPIO2 is programmed for Input or Output. The PIO1 and PIO2 bits can be read/written via PCI, and if set as input, they can generate a PCI interrupt.

## DPIO2 SOFTWARE SUPPORT

There are drivers available for the DPIO2 for VxWorks (PowerPC and i960), Mercury MC/OS and Windows 2000/NT. For customers who want to modify the driver or port the driver to another hardware platform or other operating system, VMETRO also offers the driver source code (Source Kit).

## DPIO2 DMA Modes - Default Mode

The default DMA mode is also the most used. The controller will idle wait for data in FIFO and perform DMA cycles onto the PCI bus whenever there is data. This gives low latency on data arriving to memory. When the datarate is low, the efficiency on the PCI bus is not optimal because data is sent in single cycles or small bursts only. This will not represent any problems if the DPIO2 has an exclusive PCI segment on the carrier board.

If there are more PMCs on the same PCI segment, there are mechanisms to improve efficiency. These are called “latency counters” and are used to ensure that PCI bus-mastering devices share the PCI bus fairly. “Fairly” in this case means that devices will not use more of the available PCI bus bandwidth than allows other devices to get work done. When many devices want to put data on the PCI bus, the arbiter makes sure they wait for each other. Then queues will start to build in the FIFOs in each device. This will cause each device to perform larger bursts when they gain the bus and thus automatically start working in a more efficient way on the PCI bus. The latency counter in each device should be set to a fairly high number so that the arbiter does not break up the traffic too often as this will lower utilization of the


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bus. Also the sum of all latency counters in one segment needs to be low enough so that in the worst case, no single device need to buffer up more than it can hold. If there are only DPIO2 devices in the segment, this is not a problem as the FIFOs are very large. By default, the latency counter in the DPIO2 is set to the maximum by the driver.

## DPIO2 DMA Modes - Demand Mode

In demand mode DMA, the controller will not start the DMA until the FIFO is more than half full. The FIFO will be emptied onto the PCI bus, and the controller will sit and wait until the FIFO is half-full again. This means that as much as 64KBytes or 256 KBytes (depending on the DPIO2 model) will be bursted at the time, utilizing the PCI bus to its maximum. This is very well suited to long and fast transfers and where several DPIO2s are connected to the same PCI segment and data latency is of less importance.

## DPIO2 DMA Modes - Linked List

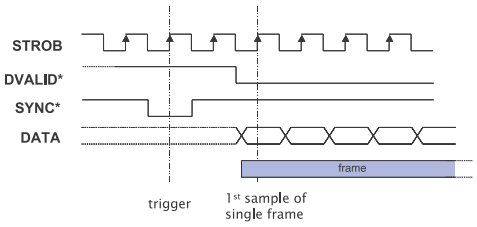
In linked list DMA many DMA descriptors are pre-allocated into the SSRAM of the DPIO. They are linked together in a chain and will be executed in the order they are organized. The DMA controller will jump to the next descriptor whenever the current one is full (DMA count satisfied) or an End-Of-Transfer (EOT) occurs. EOT can be programmed to be any of the input signals: SYNC, PIO1/2 or RES1. The linked list of descriptors can be looped, where the last descriptor is linked back to the first, and can be set up once and run forever. This is very useful for repetitive transfers that can be sent to the same set of PCI addresses every time.

Linked list DMA is especially useful for formatting data directly into memory, handling synchronization efficiently and frames of variable length. For fixed sized frames, descriptor(s) can be set up with the size of the frames (or a multiple of frames). The DMA controller jumps to the next descriptor upon full DMA containing one or more full frames. Interrupts can be generated at each DMA completion. For variable sized frames, an external signal is necessary to delimit each frame. This signal must be connected to one of the signals that can be set as EOT (typically SYNC asserted at last data using DMA-On-SYNC). Descriptors can be set up for maximum expected frame size and enable interrupt for EOT. The Interrupt Service Routine (ISR) will have to read the DMA count and associate it to the stored frame i.e. by storing it in a header. This way the application will be in sync and will know how much of each stored frame is valid.

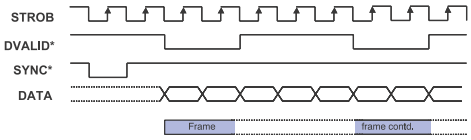
## Managing FPDP Data Flow Using FPDP SYNC Signal

Listed below are descriptions for the various ways to utilize the FPDP SYNC signal together with the advanced DPIO2 features to handle data input synchronization challenges:

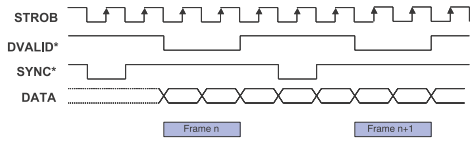
**Wait-for-SYNC:** In this mode the DPIO2 ignores all data before first SYNC, and is used for large (or endless) batches of data initiated by a starting trigger. This trigger signal is connected to the FPDP SYNC pin. Typically the data has a known and fixed format from the beginning of the transfer.




*Sync without DVALID, simple trigger for start of single frame*

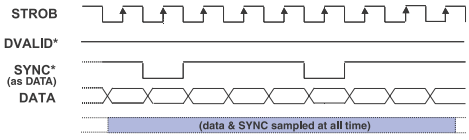



*Validating data with DVALID*



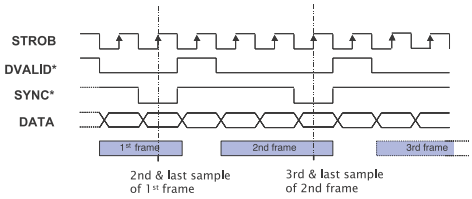

*Sync without DVALID, repeating frame*

**SYNC-as-Data:** DPIO2 allows the configuration of the FPDP SYNC signal to be placed at the LSB (Least Significant Bit) of the data. The LSB data bit often has little useful information as it is normally below the noise-level of typical A/D systems. Data and SYNC are sampled every clock. This mode is especially useful for recording when the timing on data and SYNC is to be regenerated on playback. Timing is preserved provided that the data is clocked out at the same rate during playback.




*Data and SYNC sampled at all time*

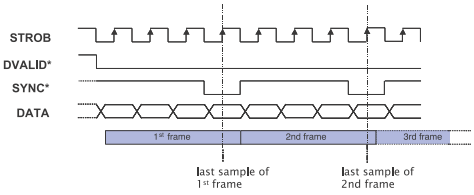
**Interrupt-on-SYNC:** Using this DPIO2 interrupt mode allows the driver to be woken up at the end of each frame. This maintains synchronization by CPU intervention between each frame when there is sufficient processing time between each. Variable length data frame can be handled this way by the Interrupt Service Routine reading the data count register. To make sure data has been transferred to memory before reading the data count register, the normal procedure is to set SYNC as EOT and enable interrupt on DMA end-of-transfer, then read the data count register in the Interrupt Service Routine.




*Sync with DVALID, Dynamic size repeating frame*

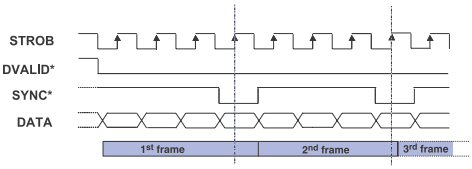
**DMA-on-SYNC:** When frames are short and/or there is no time or need for CPU intervention between each frame, full "hardware synchronization" on data can be achieved. Each frame can be directed to separate DMA descriptors in a chain. The DMA chain can be looped and run forever, combined with interrupt and jump to next descriptor on EOT, it can be used to distribute data to many parts of memory or to several different processors continuously with no additional change in the DPIO2 set-up.


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*Sync with DVALID, Fixed size repeating frame*

**DMA-Data-Counter:** (Considered feature) This mode will work like DMA-on-SYNC for each frame, but the data count register is also DMAed to separate descriptors. The linked list DMA descriptors will have to point alternately to data buffers and the corresponding data length fields (in the buffer header, etc.) This way, full "hardware synchronization" can be achieved even for small sized variable length frames.

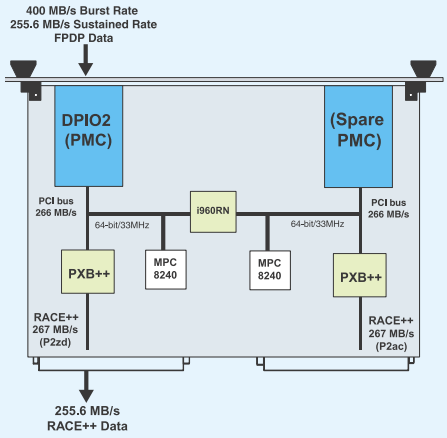



**Front-End-FPGA:** For advanced applications, the front-end FPGA can be re-programmed by the factory for custom functions regarding synchronization of input data. This can be for handling of incoming data, control signals and insertion of timestamps, tags etc. Please contact factory for any custom requirements (volume purchase required).

# Application examples

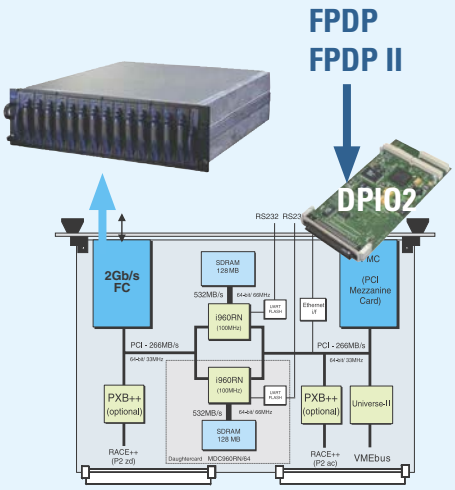
## Parallel Data to RACE++

A DPIO2 combined with a VMETRO PowerMIDAS carrier board sustains 255.6 MBytes/sec throughput to RACE++. The burst rate at FPDP II is 400 MBytes/sec.



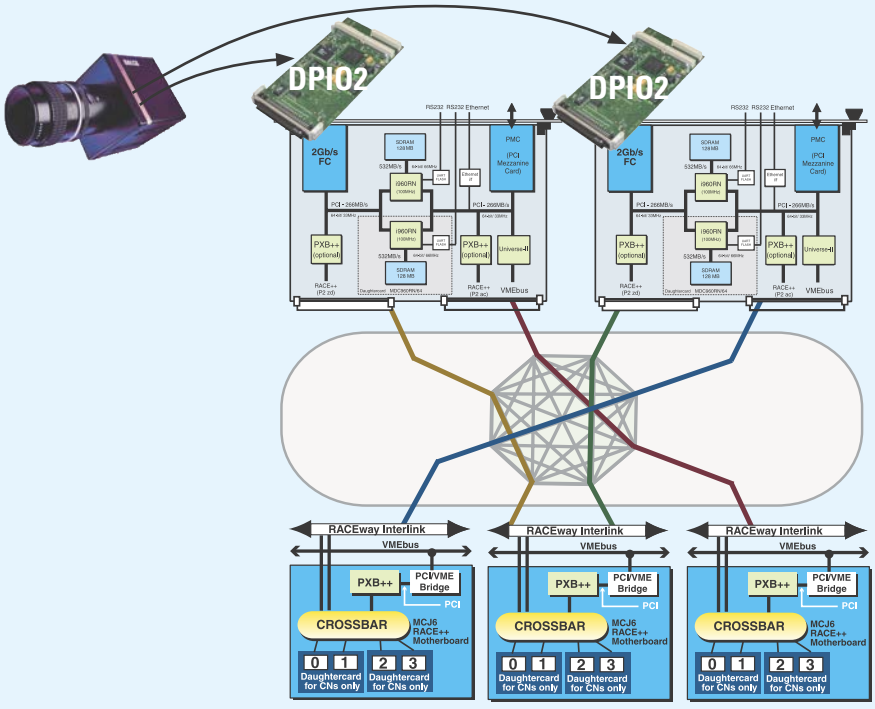

## Data Recorder

A DPIO2 used to bring FPDP data from an A/D converter into a data recorder, where high-speed data is stored in real-time on multiple disks, controlled by a PowerMIDAS board with 2 Gbit/sec Fibre Channel PMC modules.




## Digital Video Input

Two DPIO2s mounted on separate VMETRO PowerMIDAS carriers to provide enough buffer space and bandwidth for High Resolution Digital Video input from a camera used for advanced industrial visual inspection systems. The image is processed in a multi CPU array interconnected by RACE++, which also connects the camera I/O from the PowerMIDAS carriers.




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## Specifications:

**Max. Input data rate:** 400 Mbytes/Sec

**Max. PCI transfer rate:**

255.6 MBytes/sec @ 33 MHz PCI (-FBU/-LBU versions)

510 Mbytes/sec @ 66MHz PCI (-FB3/-LB3 versions)

**FIFO size:** 32Kx32 bits or 128Kx32 bits

**Local SSRAM:** 1 MByte

**Power supply voltage:** 5V

**Signal levels:**
DPIO2-FBU/LBU: Both 5V and 3.3V
DPIO2-FB3/LB3: 3.3V

**Power consumption:**

DPIO2-FBU: 3.3 W active (2.3 W idle)
DPIO2-LBU: 4.0 W active (2.8 W idle)

**Physical dimensions:** 149 x 74 mm

**Weight:**

DPIO2-FBU: 77 g
DPIO2-LBU: 89 g

**MTBF:**

DPIO2-FBU: 247655 (GB), 53257 (AIC), ambient 25 °C

## Ordering Information:

**DPIO2-FBU/32K**
64-bit 33MHz PCI, FPDP, 32Kx32 bits FIFO, Universal sign. Voltage

**DPIO2-FBU/128K**
64-bit 33MHz PCI, FPDP, 128Kx32 bits FIFO, Universal sign. Voltage

**DPIO2-FB3/128K**
64-bit 66MHz PCI, FPDP, 128Kx32 bits FIFO, 3.3V sign. voltage (contact factory)

**DPIO2-LBU/32K**
64-bit 33MHz PCI, LVDS, 32Kx32 bits FIFO, Universal sign. Voltage

**DPIO2-LBU/128K**
64-bit 33MHz PCI, LVDS, 128Kx32 bits FIFO, Universal sign. Voltage

**DPIO2-LB3/128K**
64-bit 66MHz PCI, LVDS, 128Kx32 bits FIFO, 3.3V sign. voltage (contact factory)

Contact factory for other signal interface standards such as RS-422/485 and PECL.

**VMETRO, Inc.**
**1880 Dairy Ashford, #400**
**Houston, TX 77077, USA**
**Tel.: (281) 584-0728**
**Fax: (281) 584-9034**

**VMETRO asa**
**Brynsveien 5**
**0667 Oslo, Norway**
**Tel.: +47 22 10 60 90**
**Fax: +47 22 10 62 02**

**E-mail: info@vmetro.com**
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