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MM-6170F

PMC/PCI
MEMORY MODULE

Users Guide
For P/N 96460

October 1999

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MM-6170F

256Mb PMC/PCI

Flash Memory Module

Revision A

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SECTION I GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation procedures of the **MM-6170F PMC/PCI** bus **FLASH** Memory Module.

1.2 GENERAL DESCRIPTION

The **MM-6170F FLASH Memory** is compatible with the **PCI** bus 2.1 specification. The module is a 32 bit wide **PCI** bus target, capable of operating with a 33 MHZ PCI bus clock. It is capable of being configured to map to the 32 bit address space of the host computer.

For higher performance operation, the **MM-6170F FLASH Memory** is capable of **Burst Mode Transfer** capability. The **MM-6170F** is capable of performing DMA operations (bursts of 44 Mbytes/second, from FLASH to host) as a direct PCI master without CPU intervention.

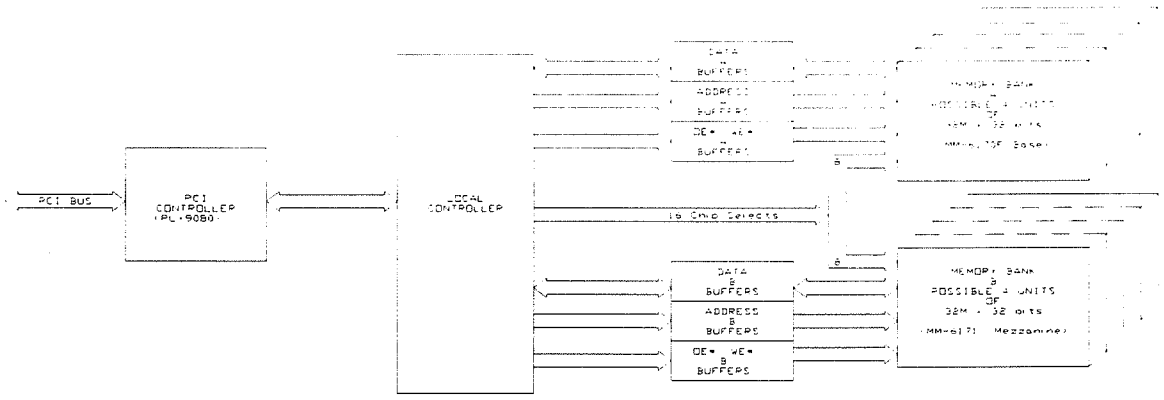


Figure 1.2 MM-6170F Block Diagram

The **MM-6170F** follows the **CMC** specification IEEE P1386 Draft 2.0 and **PMC** Specification IEEE P1386.1 Draft. If the **MM-6170F** does not recognize the bus protocol from the host CPU on BUSMODE lines, the **MM-6170F** will hold itself in reset and will not show on the PCI bus during initial polling.

The **MM-6170F FLASH Memory** modules are available in several options depending on the capacity required. **Table 1.1** lists the optional part numbers for ordering purposes, the total memory capacity provided by each version.

Table 1.1 Memory Capacity Options

Option	Capacity
MM-6170F/64M	64M Bytes
MM-6170FT/64M	64M Bytes
MM-6170F/128M	128M Bytes
MM-6170FT/128M	128M Bytes
MM-6170F/256M	256M Bytes

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1.2.2 OPERATIONAL FEATURES

The **MM-6170F Memory** module contains four base address registers, which are used to configure the address ranges of the various address blocks of the **MM-6170F**. These base address registers are located in the configuration space for the **MM-6170F**. The first base and second address register, BAR0 and BAR1 are used to used by PCI controller for its internal registers. The BAR0 will contain the start memory address of the internal registers and BAR1 will contain the start I/O address of the internal registers. The third Base address register 2 is used to establish the memory address range. The address range will start on the memory size boundary. For example, a 128M byte memory will start on a 128 M byte boundary. Base address register BAR3 is not used.

Due to the limitations of the host CPU, the CPU may not be able to address all the MM-6170F memory with a single setting. The rest of the memory range can be reached (windowed) by programming an offset register.

The **MM-6170F FLASH Memory** array can be addressed as 8 bit bytes, 16 bit words, or as 32 bit double words, using conventional Read/Write, or burst transfers. Three byte accesses are also supported.

1.3 GENERAL SPECIFICATIONS

Table 1.2
General Specifications
MM-6170F High Speed FLASH Memory Module

Characteristics	Specifications
Capacity	64M, 128M, 256M Mbytes
Address	32 bits multiplexed with data on the PCI bus
Data In/Data Out	8/16/24/32 bits bi-directional controlled by byte enable signals C/BE[3..0]#
Modes of Operation	Read, Write, Burst Read, Burst Write, DMA Burst Read, DMA Burst Write
Module Selection: PCI bus	One memory block selected on memory size boundaries within the 4 Gbyte address space, for example 128Mbytes is on 128Mbyte boundary
Program One Address Sector Erase	Typically about 7 µsec (Byte, Word or Dword) Typically about 1 sec, Maximum 8 sec
Input Interface:	PCI compliant
Output Interface:	PCI compliant
Operating Temperature	Standard Version: 0 to 60 degrees C FT Version: -35 to +75 degrees C
Storage Temperature	Standard Version: -40 to +85 degrees C FT Version: -55 to +85 degrees C
Relative Humidity	95% without condensation
Power Requirements: +5V (fully populated)	Standby Operate 0.5A 1.2A

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Table 1.3
Timing Specifications for the MM-6170F FLASH Memory Module
Assuming a PCI Clock Frequency of 33 MHZ

Cycle Type	Latency in Clock Cycles	Clock Cycles/Transfer
Write	6	3
Read	6	3

Note: In programming and erasing, the FLASH Busy signal will add cycle time to the numbers listed above

1.4 MEMORY ARRAY ORGANIZATION

The memory array is partitioned into sixteen 4M x 32 bit banks. Physically, 8 banks are located on the **PMC** mezzanine card (**MM-6170F**) with the additional 8 banks if needed located on the smaller daughter board (**MM-6171**).

The memory devices used are 32Megabit (4M x 8-Bit) CMOS 5.0 Volt-only, Uniform Sector Flash Memory featuring 64 uniform sectors of 64Kbytes per device. Data can be erased on a per-sector bassis or any combination of sectors including full chip erase. Data can be written in bytes, words or double-words. The devices are rated to provide a minimum of one million write/erase cycles and to retain data for 20 yeas at 125°C.

Determining which bits constitute what byte may be somewhat confusing. This can be cleared up by seeing the same data in the various formats used in most systems (IE: Byte, Word, and Doubleword). If the contents of the first 8 locations in memory are 01h 23h 45h 67h 89h 0ABh 0CDh 0EFh they would be seen in various formats as shown below.

Table 1.4 Memory Array Organization (Example)

BYTE Format		**WORD Format**		**DOUBLEWORD Format**	
Location	*Data*	*Location*	*Data*	*Location*	*Data*
00000000	01	00000000	2301	00000000	67452301
00000001	23	00000002	6745	00000004	EFCDAB89
00000002	45	00000004	AB89		
00000003	67	00000006	EFCD		
00000004	89				
00000005	AB				
00000006	CD				
00000007	EF				

1.5 MECHANICAL DETAILS

The **MM-6170FT** provides up to 128M Bytes of memory. One half of this memory is on the top of the board and the second half on the bottom of the board.

The **MM-6170F** provides up to 256M Bytes of memory. One quarter of this memory is on the top of the board and the second quarter on the bottom of the board. The top and the bottom of the card are shown in Figure 1.5.1. and 1.5.2. For the additional 128M Bytes of memory a daughter board (**MM-6171**) is plugged into the **MM-6170F**. The board/set plugs into standard **PMC** J1 and J2. The **PMC** connectors pin signal assignments are shown in Table 1.5.1 and 1.5.2.

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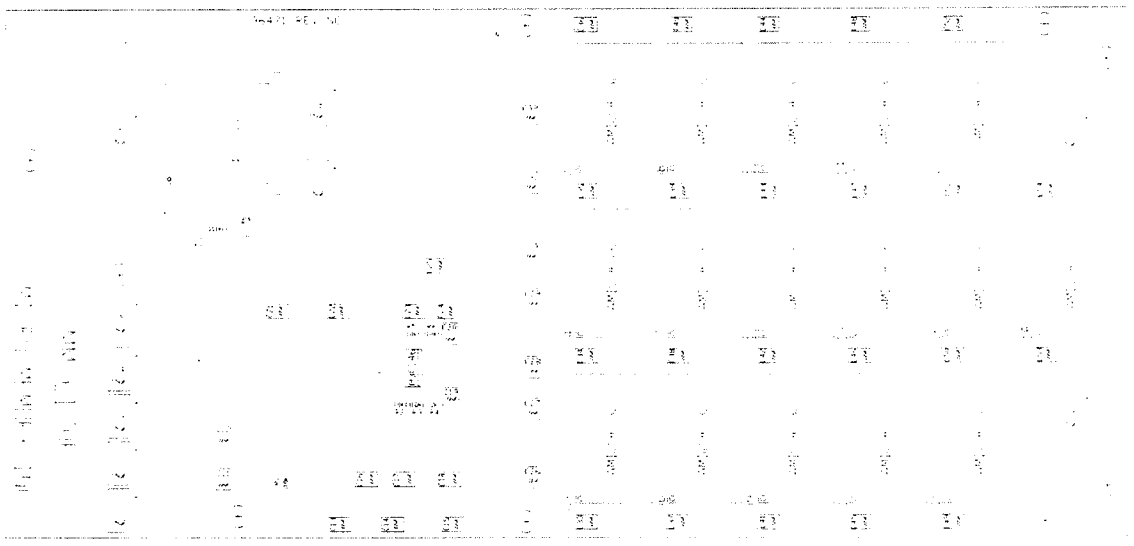


Figure 1.5.1 MM-6170F Component Layout Top View

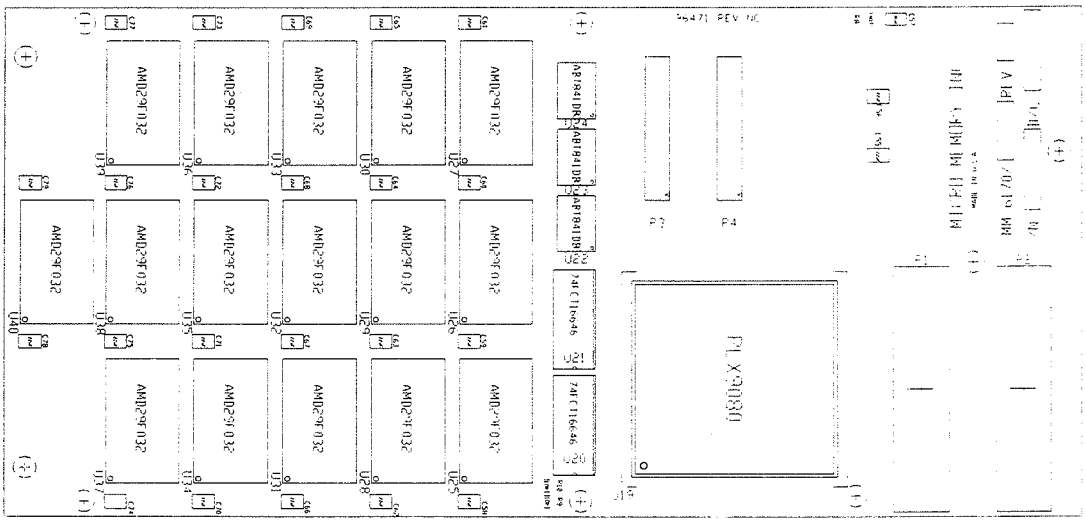


Figure 1.5.2 MM-6170F Component Layout Bottom View

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TABLE 1.5.1 PMC J1 Connector Pin Assignments

PIN	SIGNAL NAME	SIGNAL NAME	PIN
1	TCK	-12V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD*	10
11	Ground	PCI-RSVD*	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19	+5V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	+5V(I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	+5V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	+5V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64

TABLE 1.5.2 PMC J2 Connector Pin Assignments

PIN	SIGNAL NAME	SIGNAL NAME	PIN
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD*	8
9	PCI-RSVD*	PCI-RSVD*	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	PCI-RSVD*	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34
35	TRDY#	+3.3V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD	52
53	+3.3V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK64#	+3.3V	62
63	Ground	PMC-RSVD	64

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SECTION II INSTALLATION

2.1 INTRODUCTION

This section details a step by step procedure to interface the **MM-6170F Memory** to **the PMC/PCI** bus.

2.2 UNPACKING INSTRUCTIONS

Unpack module from shipping carton. If carton is damaged upon receipt, request that the carrier's agent be present during unpacking and inspection of the equipment. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment. For repairs or replacement of a board damaged during shipment, contact **MICRO MEMORY, Inc.** to obtain a Return Authorization number and further instructions.

2.3 HARDWARE PREPARATION

The memory module should be inspected prior to system installation.

2.3.1 Handling Procedure

The **MM-6170F High Speed Memory** uses CMOS components that are susceptible to damage if exposed to static electrical charges. To avoid damage of these components during handling, testing or operation, the following procedure should be used.

A. Device leads should contact conductive material to avoid building of any static charge, except during testing or operation.

B. Soldering iron tips, metal fixtures, tools, and handling facilities used in preparing the module for operation should be grounded.

C. Devices should never be removed or inserted while power is applied to the module because voltage transients may permanently damage the devices and/or module.

D. The memory module should never be plugged in or out of the motherboard while power is applied.

E. External signals should not be applied to device inputs while power is removed.

F. Any memory module removed from the system should be transferred to either non-conductive foam or an anti-static plastic bag for storage or shipment.

2.4 OPERATING ENVIRONMENT

2.4.1 AIRFLOW AND COOLING

An adequate airflow is required to maintain the operating temperature within specifications of the memory module. Failure to adhere to these requirements may result in poor long term reliability.

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2.5 Placing MM-6170F on the Host Board

Locate the **PCI** Mezzanine Card (**PMC**) slot cutout in the host card front panel. The **MM-6170F** front panel will go into this cutout. Face the host board with the component side up and **PMC** cutout in front. Look beyond the **PMC** cutout and locate the 64 pin **PMC** connectors. These are located to the rear of the host board inline with the host **PMC** cutout. There can be as many as five **PCI** mezzanine connectors per host **PMC** cutout. If there is more than 2 **PMC** connectors, the connectors the **MM-6170F** will plug in will be on the left located closest to host **PMC** cutout.

Locate the voltage keying pin. This pin should be located behind at the extreme right of the left connector closest to the host **PMC** cutout. This pin indicates the card is 5VDC. **If the pin is located in front at the extreme right of the left connector closest. STOP!** The host is +3.3VDC and because the **MM-6170F** utilizes 5 volt FLASH devices, it can't be used on a +3.3VDC host.

Position the **MM-6170F** with its front panel front and **PMC** connectors down. Bring the **MM-6170F** over the host **PMC** connectors with its front panel just beyond the host **PMC** cutout. Lift the **MM-6170F PMC** connector end up and position the **MM-6170F** in the host **PMC** cutout. Line up the host **PMC and MM-6170F** connectors and the +5VDC keying pin, then press the **MM-6170F** down over the host **PMC** connectors.

2.6 BASE ADDRESS REGISTER SETTINGS

The **MM-6170F FLASH Memory** contains one base address register which must be configured prior to accessing the memory. This is BAR2. This base address register is 32 bits wide, and may be accessed through **PCI** configuration space at offset 18h of the **MM-6170F's** configuration space header. Base register 0 BAR0 is set up to request 256 bytes of memory space and Base register 1 is set up to request 256 bytes of I/O space for the internal **PCI** controller registers.. Both registers are software read to determine the **MM-6170F** address size. Then BAR1 is written with the internal register I/O starting address, BAR1 is written with the internal register memory starting address, BAR2 is written with the memory starting address.

2.6.1 Base Address Register Configuration

Memory block selection for the **MM-6170F** memory resides on boundaries which is located on memory size boundaries. The size of each memory block may be determined by writing all one's to the corresponding base address register. The base address register is then read back. Those bits which are zeros represent the address of the memory block. The values are shown in **Table 2.5.1**. Those bits which are ones may be rewritten with the starting address of the memory block.

Table 2.6.1 BAR 2 Read Response to an All-Ones Write

Response	Size in Bytes
FC000000	64M bytes
F8000000	128M bytes
F0000000	256M bytes

2.6.2 MVME1604-001 Base Address Register Configuration Example

The PPCBUG firmware automatically locates the **MM-6170F** memory. The **MM-6170F** base register may be read and the PPCBUG can be used to manually relocate the starting address of the **MM-6170F** memory. An example of this process for a 128Mbyte memory block using Motorola MVME1604-001 with PPCBUG firmware 1.9 is shown below in figure 2.6.2. The Motorola MVME1604-001 PCI configuration space starts at 80810000. The BAR2 address is 80810018. This example shows the memory block being located in the 128Mbyte block starting at F0000000h. The keyboard entered values are in **BOLD**.

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Figure 2.6.1 Base Address Register Selection for 128Mbyte Memory Block Starting at F0000000h

```
PPC1-BUG> md 80810018:1
        80810018        00000030                ...0
PPC1-BUG> mm 80810018
        80810018        00000030?       ffffffff
** WARNING: NO MATCH **
        80810018        000000F8?       00000030=
        80810018        00000030?       .
```

The on-board MPC105 PCI Bridge/Memory Controller takes the upper two bits to decode the PCI memory space and does byte swapping from little endian to big endian on data received from PCI bus. The BAR2 processor address first two bits are used to decode the PCI configuration memory space giving a address of 00810018 on the PCI bus. The BAR1 30000000 data is converted to big endian and received as 00000030 at the processor.

The card's processor memory address is F0000000. The Controller decodes the PCI memory by using the upper two to give the PCI bus address of 30000000. The data from the processor to the memory card is converted from little endian to big endian by the controller. For example the data 78563412 at the processor arrives as 12345678 at the memory card.

When FFFFFFFF is written to the base register, the base register returns the memory size and type request. The value 000000F8 read from location 80810018 indicates the card is requesting 128M of memory space. The other values were shown in Table 2.5.1.

2.7 Enabling MM-6170F Memory

The **MM-6170F** Memory must be enabled by setting bit 1 of the PCI configuration command register to 1. See 3.1.3 for full register description.

2.7.1 MVME1604-001 Example

The PPCBUG revision 1.9 automatically enables the **MM-6170F** memory. The PCI configuration register is located at 80810004. This register can be read using the following keyboard sequence shown in Figure 2.7.1. The keyboard entered values are in **BOLD**. The value at the PCI bus is 0007. 0007 is converted to 0700 by the MPC105 PCI Bridge/Memory Controller.

Bit 0 set indicates I/O access is enabled. Bit 1 set indicates memory access enable. Bit 2 set indicates bus master enable.

Figure 2.7.1 MVME1604-001 MM-6170F PCI configuration read

```
PPC1-BUG> md 80810004:1 ;h
0700
PPC1-BUG>
```


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SECTION III PROGRAMMING INFORMATION

3.1 PCI Configuration Space Header

The **PCI Configuration Space Header** provides a **PCI bus** accessible set of locations determines the configuration of the **MM-6170F** memory module, and set the address of its memory block.

Table 3.1 PCI Configuration Space Header

BASE +	D31 D24	D23 D16	D15 D8	D7 D0
00H	DEVICE ID		VENDOR ID	
04H	STATUS		COMMAND	
08H	CLASS CODE (050000h)			REV ID
0CH	BIST (NOT USED)	HEADER TYPE (00h)	LATENCY TIMER	CACHE LINE SIZE
10H	BASE ADDRESS REGISTER 0 (internal registers, memory addressing)			
14H	BASE ADDRESS REGISTER 1 (internal registers, I/O addressing)			
18H	BASE ADDRESS REGISTER 2 (memory addressing)			
1CH	BASE ADDRESS REGISTER 3 (NOT USED)			
20H	BASE ADDRESS REGISTER 4 (NOT SUPPORTED)			
24H	BASE ADDRESS REGISTER 5 (NOT SUPPORTED)			
28H	CARDBUS CIS POINTER (NOT SUPPORTED)			
2CH	SUBSYSTEM ID (6140h)		SUBSYSTEM VENDOR ID (1332h)	
30H	LOCAL EXPANSION ROM BASE ADDRESS REGISTER (NOT USED)			
34H	RESERVED (0'S)			
38H	RESERVED (0'S)			
3CH	MAX LATENCY	MIN GRANT TIME	INTERRUPT PIN (01h)	INTERRUPT LINE

3.1.1 Vendor I.D. Word

The first 16 bit word (Config Header + 00h) provides a vendor I.D. word. The **MM-6170F** is set up to read the value of the Subsystem Vendor ID register.

3.1.2 Device I.D. Word

The next word (config Header + 02h) provides a device I.D. word. The **MM-6170F** is set up to read the value of the Subsystem ID register.

3.1.3 PCI Configuration Command Register

The next word (config Header + 04h) is the command register. Bits 15 through 10 of this register are reserved and are 0s. The functions of the other bits are tabulated below.

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Table 3.1.3 PCI Configuration Command Register

Bit	Function
9	Fast back to back cycles- A value of 1 indicates fast back-to-back transfers can occur.
8	SERR# enabled- enables SERR# to be asserted if a parity error is detected on the PCI bus during an address phase. Zeroed at RESET#.
7	Wait Cycle Enable- always 0.
6	PERR# enabled - enables PERR# to be asserted if a PCI bus parity error is detected during a data phase.
5	Palette Snoop Enable- always 0.
4	Memory Write and Invalidate Enable- Set to 1 to enable memory Write and Invalidate cycles
3	Special Cycle Enable- always 0. This module does not respond to special cycles.
2	Bus Master Enable- Set to 1 to make the board a PCI bus master. Zeroed at RESET#.
1	Memory Space Enable- This must be set to a 1 to enable access to the memory of either of the blocks. Cleared to 0 at RESET#.
0	I/O Space Enable- This must be set to a 1 to enable I/O access to the PCI controller internal registers. Cleared to 0 at RESET#.

3.1.4 PCI Configuration Status Register

The next word (config Header + 06h), is the PCI Status Register. Bits 6 through 0 are always 0. Bits 15 through 11 and 8 are cleared at RESET#, and may also be cleared by writing a 1 to them. The functions of the bits in this register are tabulated below.

Table 3.1.4 PCI Configuration Status Register

Bit	Function
15	Detected Parity Error- **MM-6170F** asserted PERR#
14	Signaled System Error- **MM-6170F** asserted SERR#
13	Master Abort- the **MM-6170F** generated a Master Abort.
12	Received Target Abort- the **MM-6170F** received a Target Abort..
11	Signaled Target Abort- the **MM-6170F** aborted a transaction.
10:9	Device select speed- these bits are set to 01 indicating a medium decode
8	Master Data Parity Error Detected. Set when the board is a master, sees a PERR# and the Parity Error Response bit in the command register is set.
7	Fast Back-to-Back Capable- Always a 1.
6:0	Reserved- always zeroes

3.1.5 Revision I.D. Register

The revision I.D. register indicates the numerical value of the **MM-6170F** board revision. 0 corresponds to Rev-NC. This is a single byte at offset 8h from the base of the config header.

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3.1.6 Class Code Register

The Class Code Register consists of three bytes, starting at offset 09h from the base of the config header.

3.1.6.1 Base Class Register

The Base Class Register identifies the type of PCI device this is. Since the **MM-6170F** is memory controller, its base class is 05h. This byte is at offset 0Bh from the base of the config header.

3.1.6.2 Sub Class Register

The Sub Class Register has a value of 01h, which identifies the **MM-6170F** as FLASH. This byte is at offset 0Ah from the base of the config header.

3.1.6.3 Programming I/F Register

The Programming Interface Register has a value of 00h. It is at offset 09h from the base of the config header.

3.1.7 Cache Line Size Register

System cache line size in units of 32-bit words. The cache line size register has a reset value of 00h, This byte is located at offset 0Ch from the base of the config header.

3.1.8 Latency Timer Register

The units of PCI clock cycles that the board as a bus master can burst data on the PCI bus. The reset value is 0. This byte is located at offset 0Dh from the base of the config header.

3.1.9 Header Type Register

The Header Type Register is a byte with value 00h at offset 0Eh from the base of the config header. Bit 7 being a zero indicates that this is a single function device.

3.1.10 BIST Register

The **MM-6170F** is not using Built In Self Test, and consequently the value of this byte register is 00h. This register is at offset 0Fh from the base of the config header.

3.1.11 Base Address Registers 0:3

The first base address register, BAR0 and BAR1 are set up to be used by PCI controller for its internal registers. Base address register 2 is used to set the memory address range. Base address register 3 is not used. Bits 3:0 of the base address registers have special meanings as tabulated below.

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Table 3.1.11 Base Address Registers 0:3

Bit	Function
31:4	These bits set the memory block base address. Writing 1s to these bits will cause those bits which are don't cares to be zeroed. The bits which may be programmed will be 1s. The bits which are 1s may then be written with the address of the region of the memory block. See section 2.6 above. BAR0 and BAR1 bits 4 through 7 are hardcoded to 0
3	Prefetchable. This bit signifies that this region of memory can be cached. If I/O space bit 3 is included in the base address. BAR0 and BAR1 bit 3 is hardcoded to 0
2:1	These two bits are 00, indicating that the base addresses for the associated block of memory may be located anywhere within the 32 bit (4 Gbyte) memory space. BAR0 and BAR1 bits are hardcoded to 0.
0	A value of 0 indicates this register maps into memory space. A value of 1 indicates this register maps into I/O space. BAR0 bit 0 is hardcoded to 0, BAR1 bit0is hardcoded to 1. BAR2 and BAR3 value after reset is 0.

3.1.12 PCI Cardbus CIS Pointer Register

This base address register provides Cardbus Information Structure Pointer for PCMCIA. It is not currently implemented. The location of this 32 bit register is at offset 28h from the base of the configuration header.

3.1.13 PCI Subsystem Vendor ID Register

This 16 bit base register contains the unique add-in board Vendor ID of 1332h. It is located at offset 2Ch from the base of the configuration. header

3.1.14 PCI Subsystem ID Register

This 16 bit base register contains the unique add-in board Device ID of 6170h. It is located at offset 2Eh from the base of the configuration. Header.

3.1.15 Expansion ROM Base Address Register

This base address register sets the base address of an expansion ROM on the **MM-6170F**. It is not currently implemented. The location of this 32 bit register is at offset 30h from the base of the configuration header.

3.1.16 Interrupt Line Register

This byte wide register is used to indicate which input of the system interrupt controller to which the interrupt line of the devices is connected. For example if the interrupt is routed to IRQ1 then the contents of this register will be 01h. The location of this 8 bit register is at offset 3Ch from the base of the configuration header. The reset value is 00h.

3.1.17 Interrupt Pin Register

This byte wide register indicates which interrupt pin the device uses. The board PCI controller is connected to INTA# and the value of this register is 1. It is at offset 3Dh from the base of the configuration header and has a reset value of 01h.

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3.1.18 Minimum Grant Register

This byte wide register is only used by bus masters. It specifies how long a burst period the device needs. It is at offset 3Eh from the base of the configuration header, and has a reset value of 00h.

3.1.19 Maximum Latency Register

This byte wide register is only used by bus masters. It indicates how often the device must gain access to the PCI bus. It is at offset 3Fh from the base of the configuration header, and has a reset value of 00h.

3.2 BUSMODE Signals

The BUSMODE signals are use to detect the PMC and to determine the logical protocol the PMC card is capable of handing. BUSMODE 2# through 4# are used by the host to poll the card, to determine if the card is present and to determine which logical protocols the card can handle. See table 4. BUSMODE #1 is used by the card to indicate a yes or no to the processor inquiry. A yes is indicated by a low logic level.

3.2.1 MM-6170F BUSMODE signals

The host BUSMODE inputs are shown in Table 4.1

Table 4.1 PMC BUSMODE inputs

BUSMODE4#	BUSMODE3#	BUSMODE2#	Mode	MM-6170F response	BUSMODE1#
L	L	L	Card Present	Yes	L
L	L	H	Uses PCI protocol	Yes	L
L	H	L	Uses SBus protocol	No	H
L	H	L	Reserved	No	H
H	X	X	Reserved or no host	No	H

3.2.2 MVME1604-001 Example

When the MVME1604-001 outputs BUSMODE4# as logic low, BUSMODE3# as logic low and BUSMODE2# as logic high indicating PCI protocol inquiry, the **MM-6170F** sets the BUSMODE1# to logic low. The MVME1604-001 reads BUSMODE1# as bit 4 of the Board Configuration Register located at processor address 80000802. The Board Configuration Register bit 4 is logic low when the **MM-6170F** is present and logic high when the **MM-6170F** is not installed in PMC slot.

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