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MM6260AD

Dynamic Memory Board for the VMEbus
Hardware Reference Manual

MICRO MEMORY INC.
9540 VASSAR AVE,
CHATSWORTH, CA 91311

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CONVENTIONS

This manual uses the following notional conventions.

NOTE A Note focuses attention on supplementary of unique information and should be read before any action is taken

* or / Used after a signal names (for example DS0* or DS0/) to indicate that the signal is active low and a signal without an asterisk or slash indicates that the signal is active high.

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation procedures of the **MM6260AD High Speed VMEbus Dynamic Random Access Memory Module.**

1.2 GENERAL DESCRIPTION

The MM6260AD High Speed Memory is compatible with the **VMEbus** C.1 specification. Inherent to the module are **VMEbus** options D32, D16 & D8 (32, 16 & 8 bit data path width), and A32, A24 (32, 24 bit address path width). The module also generates and stores a parity bit for each byte memory location on write cycles and checks this bit for each byte location read on read cycles. If a parity error is detected on a read access, the module sets a Control Status Register (CSR) bit, and may be programmed to assert the bus error signal.

For Extremely High Performance operation, the **MM6260AD High Speed Memory** is equipped with a **High Speed BLOCK Mode Transfer** capability. This allows the use of **High Performance Block Mode Controllers** to transfer up to 256 bytes on the **VMEbus**, using standard VME block transfer address modifiers; or to transfer up to 256 Kbytes ($40000) using special (user definable) address modifiers.

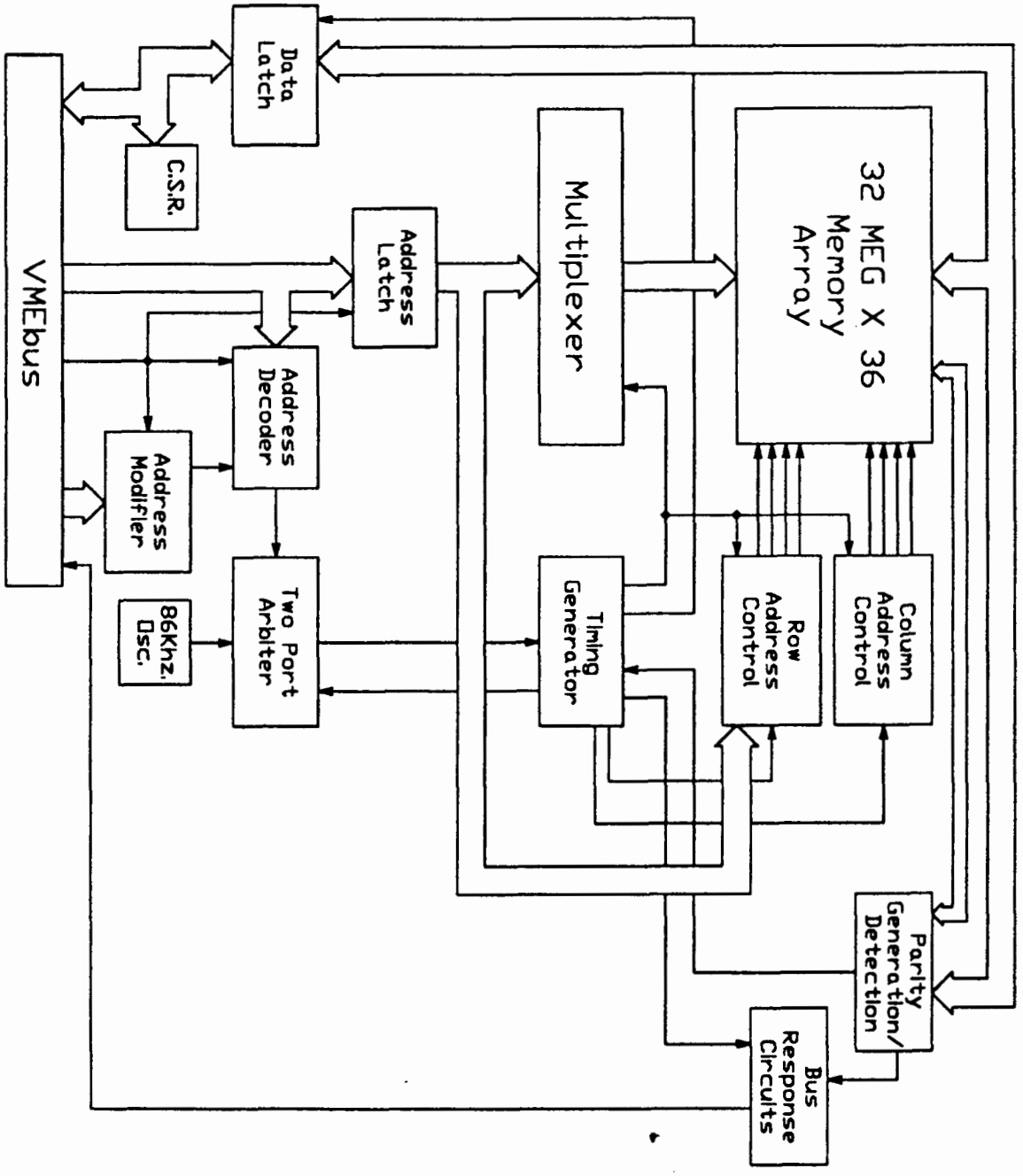
While the **MM6260AD High Speed Memory** was designed as a 32 bit wide (data path) memory board, and complies with **VMEbus** Specifications (**Revision C.1**) it can be addressed as 8 bit bytes, 16 bit words, 16 bit or 24 bit unaligned transfers or 32 bit longwords. The MM6260AD Memory can be configured for 16M, 32M, 64M and 128M bytes capacity by populating it with industry standard 16 Megabits CMOS DRAMS. The MM6260AD comes with the requested memory soldered to the board.

The **MM6260AD High Speed Memory** modules are available in several options depending on the capacity required. Table 1.1 lists the optional part numbers for ordering purposes and the total memory capacity provided by each version.

Table 1.1 summarizes the options with respect to storage capacity, available to **MM6260AD High Speed Memory** user.

Table 1.1 Memory Capacity Options

Option	Capacity
MM6260AD/16M	16.0M Bytes
MM6260AD/32M	32.0M Bytes
MM6260AD/64M	64.0M Bytes
MM6260AD/128M	128.0M Bytes



Functional Block Diagram Figure 1.1

1.2.2 OPERATIONAL FEATURES

The **MM6260AD High Speed Memory** module contains its own address register and data buffers for total compatibility with the **VMEbus Specification (Rev. C.1).**

Module selection for the **MM6260AD** resides on any 1 Mbyte (100000 hex) boundary (A24/A32). The starting and ending addresses of the **MM6260AD** may be set on any 1 Mbyte boundary within the 4 gigabytes of physical address space, for A32 address modifiers, and on any 1 Mbyte boundary within the 16 megabytes of A24 address space. The A24 ending address is separately selectable so that a portion of the **MM6260AD** may be mapped into the A24 space, for boards that are required to respond to both A24 and A32 address modifiers on the **VMEbus.**

The **MM6260AD High Speed Memory** array can be addressed as 8 bit bytes, 16 bit words, or as 32 bit longwords, using conventional Read/Write, Read/Modify/Write (RMW), or HIGH Performance **BLOCK Transfers (BLT).** Unaligned read or write transfers are also supported.

The **MM6260AD** features RAM Cache, which provides for improved access and cycle times for accesses in the same 4 Kbyte block of memory as the previous access. Memory cycle and Read/Write access times are shown in table 1.3.

The **MM6260AD High Speed Memory** responds to various Address Modifier Codes. These include $09, $0A, $0B, $0D, $0E, $0F and $17 for A32 accesses; $29 and $2D for CSR accesses; $39, $3A, $3B, $3D, $3E, $3F and $10 for A24 accesses. The codes are decoded by U1 (a socketed IFL). Note that the codes $17 and $10 are special (user defined) address modifiers for long block transfers. Various combinations are available to the user (see Section II, jumpers).

The user may select to create his/her own Address Modifier code<s>, in this event the Address Modifier evaluation IFL (U1) can be replaced to accommodate the systems' requirements (see Section II, jumpers).

A Control Status Register (CSR) is available to allow various dynamic options to be utilized by the software programmer. Included in the CSR is a bit to enable the **MM6260AD High Speed Memory** to respond to parity error by asserting BERR* instead of DTACK*. Another bit allows wrong parity to be written to the array, to test the parity circuitry. A third bit may be read or written to give the parity error status since the last write to this bit or the last bus reset. A jumper option allows write wrong parity to be disabled always, and BERR* to be returned on a parity error always. This eliminates the need for the software to manage the CSR. The CSR is an A16 Slave and has separate address selection jumpers, and may be addressed on any 2 byte boundary in the VMEbus I/O address space. Valid data is only driven on the odd byte of this two byte location. (See Section III for programming details.)

1.3 GENERAL SPECIFICATIONS

Table 1.3.1 MM6260AD High Speed Ram Memory Module General Specifications

Characteristics	Specifications
Capacity	16M,32M,64M, or 128M bytes
Address	32 bits A32/A24/BLT/UAT VMEbus
Data In/Data Out	8/16/24/32 bits bi-directional with three-state output D08/D16/D32
Modes of Operation	Read, Write Read/Modify/Write (RMW), Block Transfers (BLT), Un-aligned (UAT)
Address Modifiers	6 bits, jumper selectable, or user programmable IFL
Error Detection	Even Parity, one parity bit generated/checked for each byte.
Module Selection VMEbus	Memory selected on 1 Megabyte ($100000) boundary within the 4G byte address space, for A32 address modifiers; and any within the 16M byte address space for A24 address modifiers.
Control Status Register Selection	CSR Selected on any 2 byte boundary in the VMEbus 'A16' I/O Address space.
Inputs	TTL-compatible
Outputs	48ma. Three-state,
Operating Temperature	0 to 60 degrees C
Storage Temperature	-40 to +85 degrees C
Relative Humidity	95% without condensation
Power Requirements +5V (64 Mbytes):	Standby Operate 2.5A 3.3A

Table 1.3.2 Timing Specifications for the MM6260AD Dynamic Ram Memory Module

Cycle Type	Cycle Time	Access Time
Write (RAM Cache hit)	110 nsec.	70 nsec.
Write(RAM Cache miss)	250 nsec.	210 nsec.
Write(Block Transfer)	90 nsec.	60 nsec.
Write(First Cycle of Block Transfer)	170 nsec.	130 nsec.
Read (RAM Cache hit)	150 nsec.	120 nsec.
Read (RAM Cache miss)	290 nsec.	250 nsec.
Read(Block Transfer)	110 nsec.	80 nsec.
Read (First Cycle of Block Transfer)	210 nsec.	180 nsec.

Table 1.3.3 P1 Connector VMEbus Pin Assignments

PAGE NUMBER	ROWa SIGNAL MNEMONIC	ROWb SIGNAL MNEMONIC	ROWc SIGNAL MNEMONIC
1	D00	** BBSY*	D08
2	D01	** BCLR*	D09
3	D02	** ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	** SYSCLK	BG3IN*	** SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	** SERCLK(1)	A17
22	IACKOUT*	** SERDAT*(1)	A16
23	AM4	GND	A15
24	A07	** IRQ7*	A14
25	A06	** IRQ6*	A13
26	A05	** IRQ5*	A12
27	A04	** IRQ4*	A11
28	A03	** IRQ3*	A10
29	A02	** IRQ2*	A09
30	A01	** IRQ1*	A08
31	** -12v	** +5vSTDBY	** +12v
32	+5v	+5v	+5v

** - No Connection on MM6260AD High Speed Memory

Table 1.3.4 P2 Connector VMEbus Pin Assignments

PAGE NUMBER	ROWa SIGNAL MNEMONIC	ROWb SIGNAL MNEMONIC	ROWc SIGNAL MNEMONIC
1	N/C	+5v	N/C
2	N/C	GND	N/C
3	N/C	** RESERVED	N/C
4	N/C	A24	N/C
5	N/C	A25	N/C
6	N/C	A26	N/C
7	N/C	A27	N/C
8	N/C	A28	N/C
9	N/C	A29	N/C
10	N/C	A30	N/C
11	N/C	A31	N/C
12	N/C	GND	N/C
13	N/C	+5v	N/C
14	N/C	D16	N/C
15	N/C	D17	N/C
16	N/C	D18	N/C
17	N/C	D19	N/C
18	N/C	D20	N/C
19	N/C	D21	N/C
20	N/C	D22	N/C
21	N/C	D23	N/C
22	N/C	GND	N/C
23	N/C	D24	N/C
24	N/C	D25	N/C
25	N/C	D26	N/C
26	N/C	D27	N/C
27	N/C	D28	N/C
28	N/C	D29	N/C
29	N/C	D30	N/C
30	N/C	D31	N/C
31	N/C	GND	N/C
32	N/C	+5v	N/C

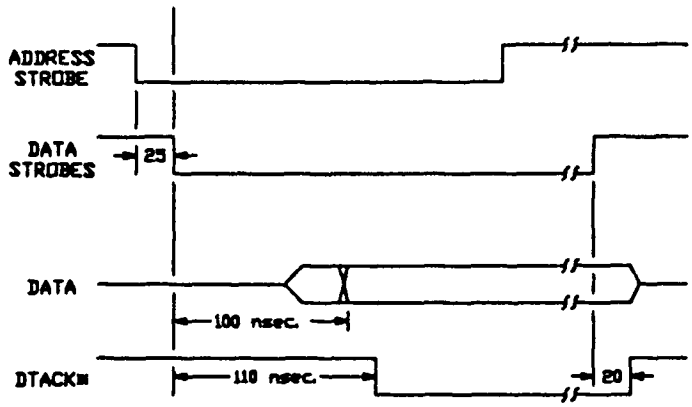
** - No Connection on MM6260AD VMEbus Memory

1.4 INTERFACE TIMING

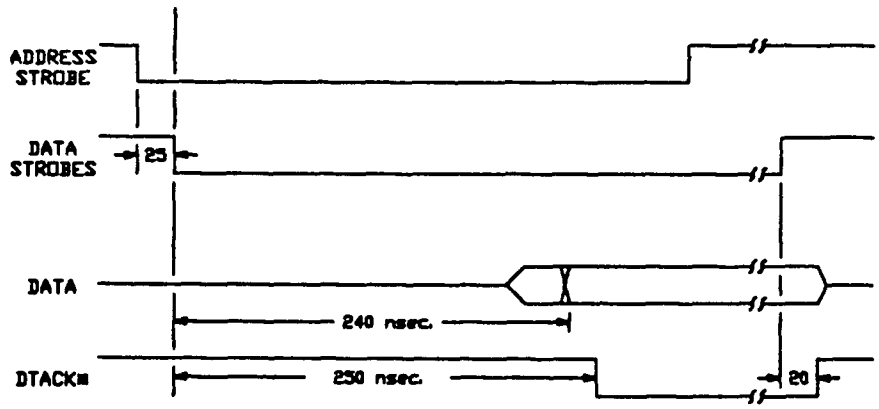
The VMEbus Interface Timing Diagrams (Figures 1.2-1.3), illustrates the timing relationships on the Data Transfer bus, for Write, and Read Cycles. Access delay time is measured from the leading edge of the Data strobes.

The refresh cycle timing is the same as read cycles. Refresh cycles are repeated once every 10usec. The cycle interval timing is generated by a free running oscillator (U39) providing a refresh transparent to memory access cycles.

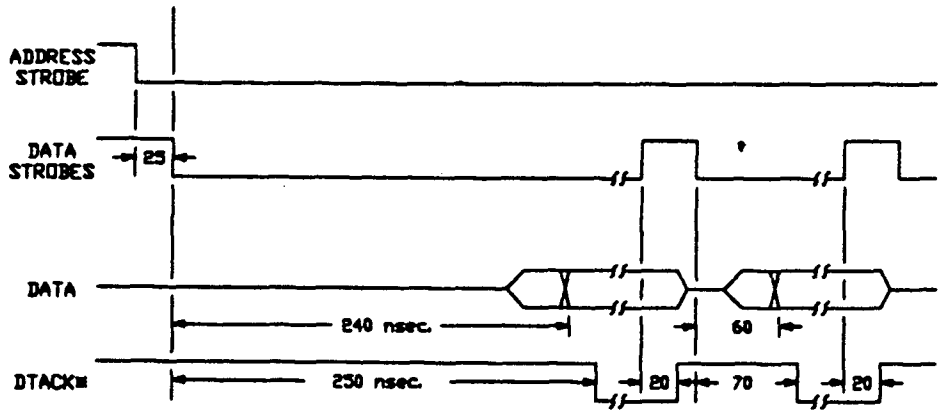
CACHE-HIT READ CYCLE



CACHE-MISS READ CYCLE

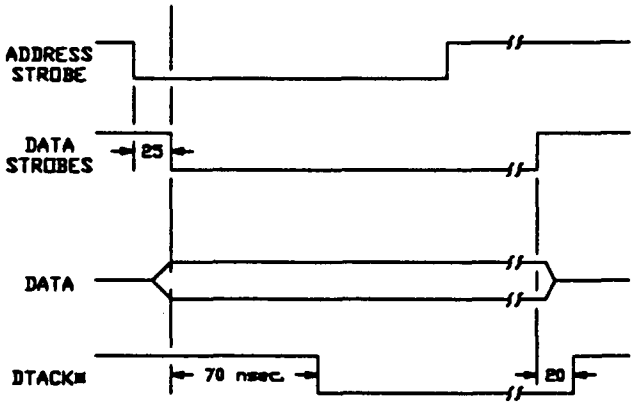


BLOCK MODE READ CYCLES

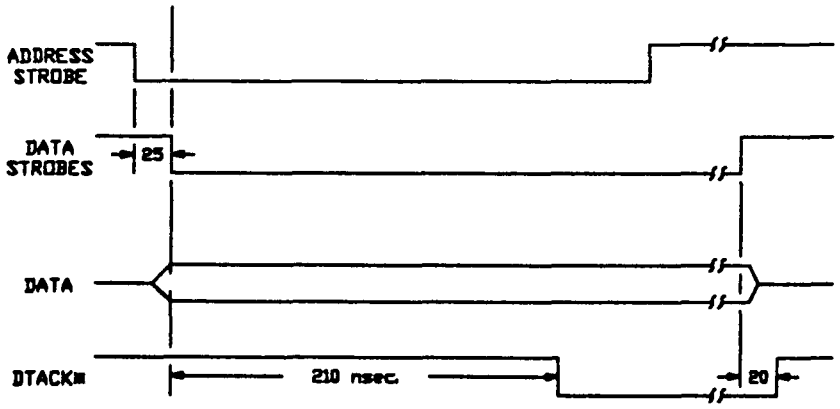


VMEbus Read Timing Diagram Figure 1.2

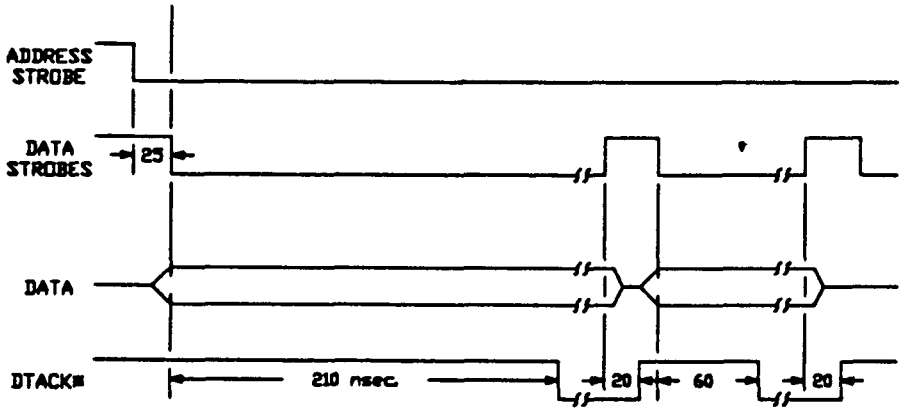
CACHE-HIT WRITE CYCLE



CACHE-MISS WRITE CYCLE



BLOCK MODE WRITE CYCLES



VMEbus Write Timing Diagram Figure 1.3

1.5 MEMORY ARRAY ORGANIZATION

The memory array is partitioned into eight 4M x 36 bit segments. The minimum memory configuration would be 4M x 36 bits, including the four parity bits DRAM in segment zero. This would translate to 16 Megabytes minimum configuration for the **MM6260AD Memory.**

Although the **MM6260AD Memory** is partitioned as four blocks of 36 bits each (32 plus 4 parity), the system will only see 32 bits of data during memory references, since the parity bits are generated or checked transparent to the user. The 32 bits of data are divided into 4 bytes (8 bits each). Memory reads and writes may be 8, 16, 24 or 32 bits wide.

Determining which bits constitute what byte may be somewhat confusing. This can be cleared up by seeing the same data in the various formats used in most systems (IE: Byte, Word, and Longword). If the contents of the first 8 locations in memory are $01 $23 $45 $67 $89 $AB $CD $EF they would be seen in various formats as shown below.

Memory Array Organization Figure 1.4

BYTE Format		WORD Format		LONGWORD Format	
Location	Data	Location	Data	Location	Data
$00000000	$01	$00000000	$0123	$00000000	$01234567
$00000001	$23	$00000002	$4567	$00000004	$89ABCDEF
$00000002	$45	$00000004	$89AB		
$00000003	$67	$00000006	$CDEF		
$00000004	$89				
$00000005	$AB				
$00000006	$CD				
$00000007	$EF				

BIT Organizations

LONGWORD

```
3                 1 1                 0 3                 1 1                 0
1.................6 5.................0 1.................6 5.................0
```

WORD

```
1                 0 1                 0 1                 0 1                 0
5.................0 5.................0 5.................0 5.................0
```

BYTE

```
0       00        0 0       00        0 0       00        0 0       00        0
7.......07........0 7.......07........0 7.......07........0 7.......07........0
```

```
0000000100100011 0100010101100111 1000100110101011 1100110111101111
 $0   $1   $2   $3  $4   $5   $6   $7  $8   $9   $A  $B   $C  $D  $E   $F
```

SECTION II

INSTALLATION

2.1 INTRODUCTION

This section details a step by step procedure to interface the **MM6260AD Memory** to the **VMEbus.**

2.2 UNPACKING INSTRUCTIONS

Unpack module from shipping carton. If carton is damaged upon receipt, request that the carrier's agent be present during unpacking and inspection of the equipment. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment. For repairs or replacement of a board damaged during shipment, contact **MICRO MEMORY, Inc.** to obtain a Return Authorization number and further instructions.

2.3 HARDWARE PREPARATION

The memory module should be inspected and prepared for jumper placement prior to system installation. The following sections describe the proper jumper options necessary for system operation (see Section 2.5, for jumper options).

2.3.1 Handling Procedure

The **MM6260AD High Speed Memory** uses CMOS components that are susceptible to damage if exposed to static electrical charges. To avoid damage of these components during handling, testing or operation, the following procedure should be used.

A. Device leads should contact conductive material to avoid building of any static charge, except during testing or operation.

B. Soldering iron tips, metal fixtures, tools, and handling facilities used in preparing the module for operation should be grounded.

C. Devices should never be removed or inserted while power is applied to the module because voltage transients may permanently damage the devices and/or module.

D. The memory module should never be plugged in or out of the cardcage while power is applied.

E. External signals should not be applied to device inputs while power is removed.

F. Any memory module removed from the system should be transferred to either non-conductive foam or an anti-static plastic bag for storage or shipment.

2.4 OPERATING ENVIRONMENT

The **MM6260AD High Speed Memory** is an extremely High Density memory product. It Contains 64 bits of high current (48ma.) data bus drivers, numerous high speed components. The environment into which the **MM6260AD Memory** is placed, must be carefully considered.

2.4.1 AIRFLOW AND COOLING

Due to the extremely high component density of the **MM6260AD Memory**, an adequate airflow is required to maintain the operating temperature within specifications of the memory module. Failure to adhere to these requirements may result in poor long term reliability.

2.4.2 POWER REQUIREMENTS

The power requirements of **MM6260AD High Speed Memory** are such, that the module should never be operated while powered only by the P1 connector. Hence power should be applied to the appropriate pins (See Tables 1.3.3 & 1.3.4) of both the P1 and the P2 connector prior to operation of the **MM6260AD Memory**.

2.5 JUMPER OPTIONS

There are several jumper options attainable on the **MM6260AD Memory** module, depending on the user application. All of the available options are selected by installing or removing mini-jumpers on wire-wrap pins on 0.100 inch centers. (see Figure 2.6)

2.5.1 Address Modifier Evaluation/Selection (Factory, Extended A32 enabled and Standard A24 disabled)

The **MM6260AD High Speed Memory** evaluates the Address Modifiers from the VMEbus to determine if they are to be responded to. The MM6260AD Memory may be configured by jumpers to respond to EXTENDED A32 address modifier codes (where all 32 bits are decoded for module selection) or to STANDARD A24 address modifier codes (where only the lower 24 address bits are decoded for module selection), or to both sets of address modifier codes. When jumper E3 is removed, the module will respond to A32 address modifier codes, and when jumper E4 is removed, the module will respond to A24 address modifier codes. The Address Modifier equations and descriptions are listed in Appendix A. The user may select to replace the Address Modifier selection IFL (U1), to allow for some other combination or the creation of a special (user defined) code or codes.

2.5.2 Memory Device Size Selection (Factory installed)

The **MM6260AD High Speed Memory** is designed to accommodate different memory array sizes of 4M DRAMs. Jumpers are installed on E6 through E21 to select the memory array size. See Table 2.5.2

Table 2.5.2 Memory Array Size Jumper Placement

Total MBytes	Jumper 1	Jumper 2	Jumper 3	Jumper 4
16M	E13-E20	E11-E18	E9-E16	E7-E14
32M	E19-E20	E11-E18	E9-E16	E7-E14
64M	E19-E20	E10-E11	E9-E16	E7-E14
128M	E19-E20	E10-E11	E15-E16	E7-E14

2.5.3 Parity Error LED Latch on Error (Factory, LED Latch disabled)

The MM6260AD High Speed Memory has a parity error indicator LED, which will be turned on by a parity error during a read access. If jumper E5 is installed, it will remain on until a bus reset, or reset by writing a 0 to the CSR, bit 7, if the CSR is enabled. (see section 2.5.4, below) If jumper E5 is removed, the LED will be turned off by the next write access or next read access without a parity error. See Section 2.6.4 for CSR selection and Section 3.1 for CSR bit descriptions.

2.5.4 CSR Enable (Factory, CSR Disabled)

If jumper E1 is removed, the CSR is enabled. A bus reset causes all bits in the CSR to be reset. Writing a 1 to bit 0 of the CSR causes a BERR* to be generated for any read cycle where a parity error is detected. Writing a 1 to bit 1 causes the wrong parity to be written with the bytes written during any memory write cycles which follow. This allows testing of the parity circuitry. Bits 2 through 6 may be written and read back, but have no effect on the MM6260AD Memory Board. Bit 7 is set whenever a parity error is detected during a read cycle, regardless of the condition of bit 0. Writing a 0 to bit 7 resets it, and if the CSR is enabled, also resets the parity error LED. If jumper E1 is installed: BERR* is always returned for read accesses where a parity error is detected; write wrong parity is inhibited; and the parity error LED may only be reset by a bus reset.

NOTE: See Section 2.6.4 for CSR selection, and Section 3.1 for CSR bit arrangement.

2.5.5 Rescinding DTACK (Factory, DTACK Resistor Pull-up)

When jumper is place between terminals 2 and 3 of E2, the MM6260AD will actively drive DTACK* high before releasing it high at the end of a cycle. If jumper is place between 1 and 2 of E2, the backplane termination resistor must pull DTACK* high. Letting MM6260AD drive DTACK* high will shorten the time for DTACK* to return high and improves system performance.

2.6 ADDRESS SWITCH SETTINGS

The **MM6260AD High Speed Memory** contains seven (7) major switches that must be configured prior to installation before proper operation can be obtained. (See Figure 2.7 for switch locations) These are SW1 through SW7. A closed switch position represents a 0, and an open switch position represents a 1.

2.6.1 VMEbus Module Selection

Module selection for the **MM6260AD Memory** resides on 1024K ($100000) byte boundaries. Selection of the VMEbus lower limit and upper limit on a particular 1024 Kilobyte ($100000) boundary within the selected bank is accomplished by closing or opening the appropriate switch positions in switches 1 through 5.

2.6.1.1 Address Selection for A32 Accesses

For A32 address modifiers, the starting address is set by the twelve bits of switches 1 and 2. Position 8 of switch 1 is the most significant bit, and corresponds to A31; position 1 of switch 2 is the least significant bit, and corresponds to A20. The ending address is set by the twelve bits of switches 3 and 4; position 8 of switch 3 is the most significant bit and corresponds to A31; position 1 of switch 4 is the most significant bit, and corresponds to A20. On all switch positions, an open corresponds to a 1, while a closed position corresponds to a 0.

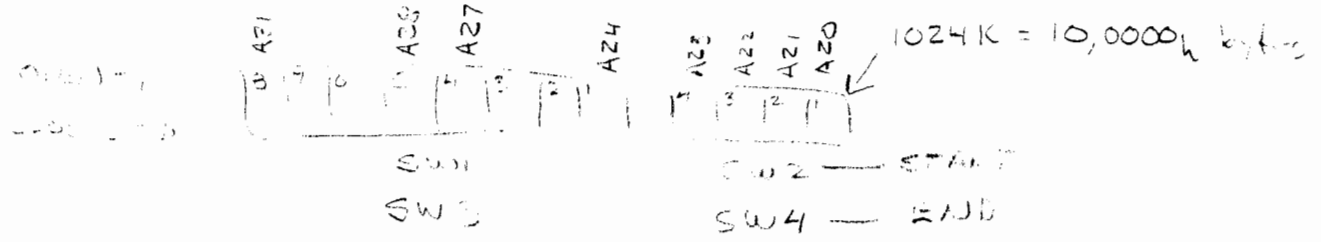
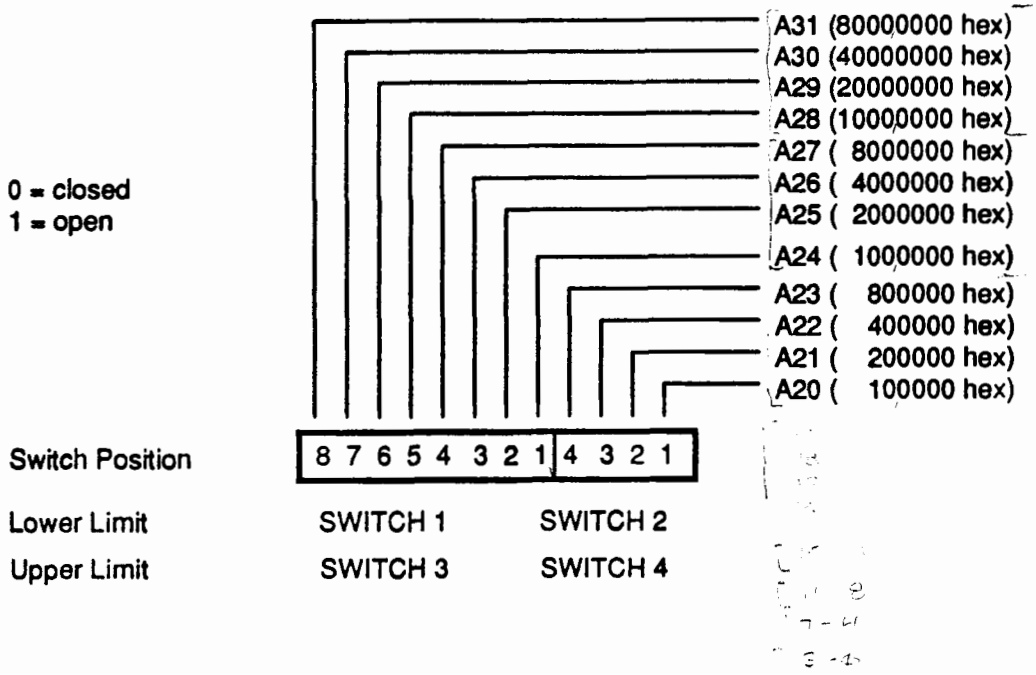


Figure 2.1 Upper & Lower Address selection for A32 Address Modifiers

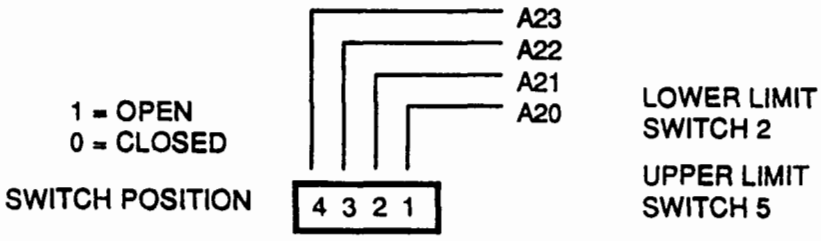


The above address switch arrangement can be thought of as three hex digits for the starting address, with the most significant digit being switch 1, positions 8-5; the next most significant digit being switch 1, positions 4-1; and the least significant digit being switch 2, positions 4-1. The three hex digits for the ending address are: the most significant digit is switch 3, positions 8-5; the next most significant digit is witch 3, positions 4-1; and the least significant digit is switch 4, positions 4-1.

2.6.1.2 Address Selection for A24 Accesses

For A24 address modifiers, the starting address is set by the same four bits of switch 2 which form the lower four bits of the A32 starting address. Position 4 is the most significant bit, and corresponds to A23; position 1 is the least significant bit, and corresponds to A20. In order to accommodate some processors which have n-board memory in the upper portion of the A24 address space, the ending address for A24 accesses is set by a separate switch from the A32 ending address. Switch 5 sets the A24 ending address. Position 4 is the most significant bit, and corresponds to A23. Position 1 is the least significant bit, and corresponds to A20.

Figure 2.2 Upper & Lower Address selection for A24 Address Modifiers



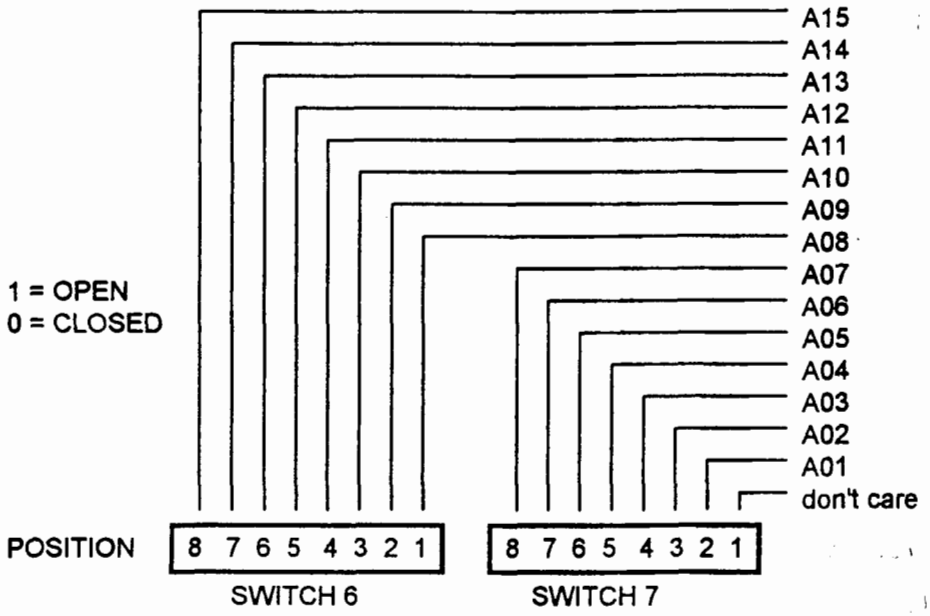
This may be thought of as a single hex digit for the starting address, which is switch 2, positions 4-1; and a single hex digit for the ending address, which is switch 5, positions 4-1.

The fact that the ending address for A24 accesses is separate from the ending address for A32 accesses allows A24 and A32 bus masters to access a common portion of memory of the MM6260AD memory. For example, if an A24 disk controller, and an A32 processor were accessing an MM6260AD, where the starting address was $00800000; the A24 ending address was $FFFFFF; and the A32 ending address was $01800000, then both masters could access the first eight Mbytes of the memory, but only the processor could access the last eight Mbytes of the memory.

2.6.2 Control/Status Register Address Selection

Selection of the CSR address may be on any 2 byte boundary, (i.e.: $0000, $0002, ..., $FFFE), within the VMEbus I/O space, by closing or opening the appropriate positions on switches 6 and 7. Switch 6, position 8 corresponds to A15, and position 1 corresponds to A08. Switch 7, position 8 corresponds to A07, and position 2 to A01. This arrangement could be viewed as four hex digits.

Figure 2.3 Control/Status Register Address selection



2.6.3 Example Addressing

To address the **MM6260AD High Speed Memory**, the user must determine first where the **MM6260AD Memory** is to be located. In this example I have chosen from 00100000 to **$010FFFFF** for the **VMEbus** A32 accesses and from **$100000** to **$EFFFFF** for the **VMEbus** A24 accesses. And an address of $0404 (VMEbus I/O space) for the CSR.

Figure 2.4 Example of VMEbus address selection:

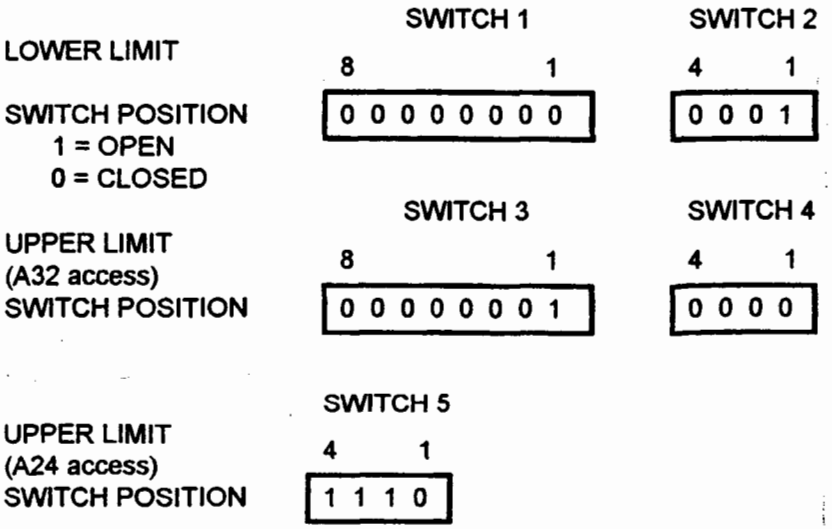
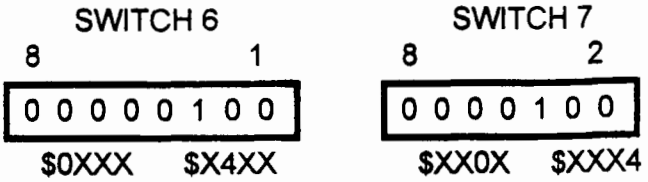


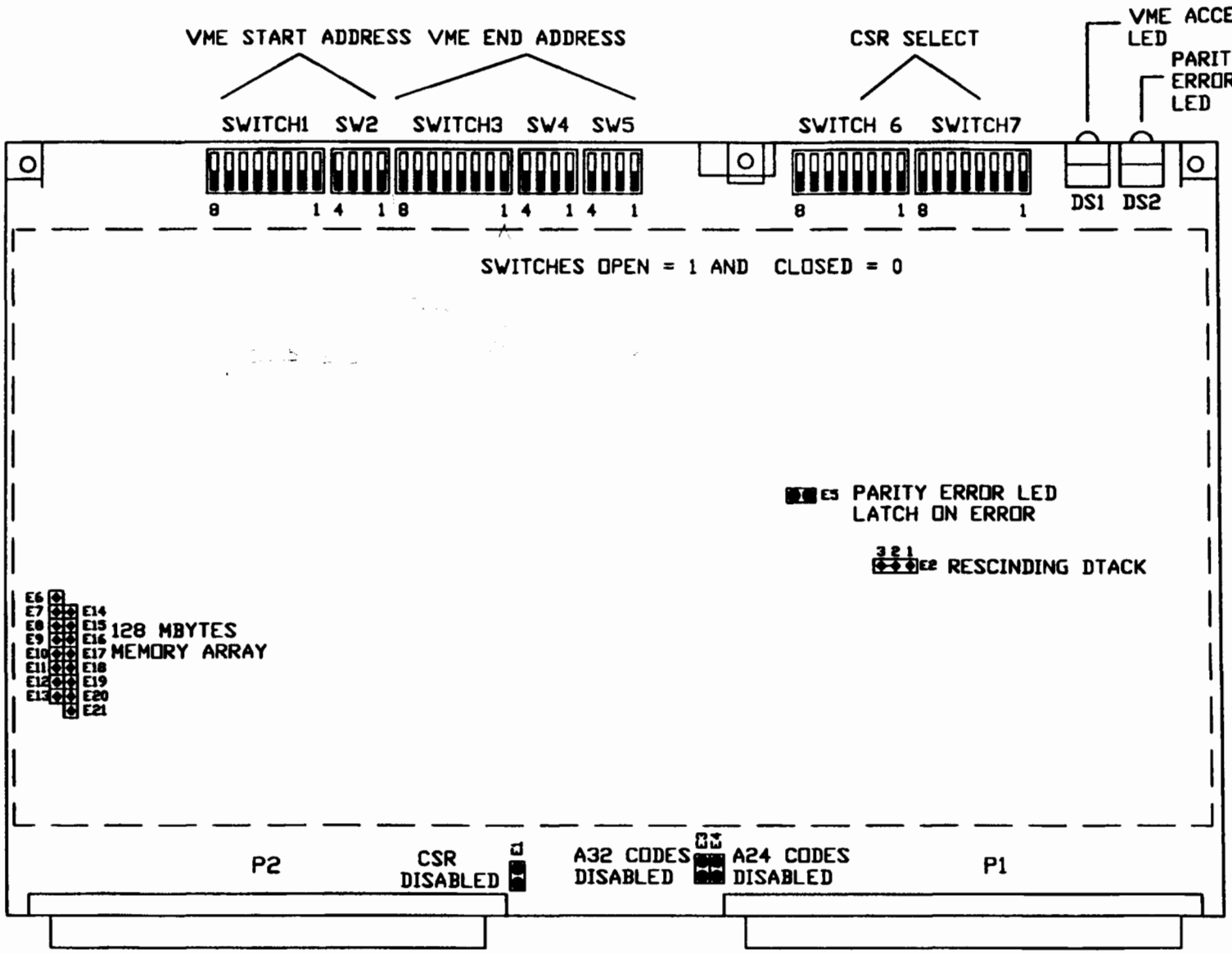
Figure 2.5 Example of CSR addressing



Then the CSR would be selected at ($0404).

2.7 Installation in the system

After selecting the memory for the proper address locations by setting the appropriate switches (see Section 2.6), installing/removing the user defined option jumpers (see Section 2.5), and after following the guidelines set forth in Section 2.3; remove power, install the **MM6260AD High Speed Memory** into the system, reapply power to the system.



Jumper and Indicator Locations Figure 2.6

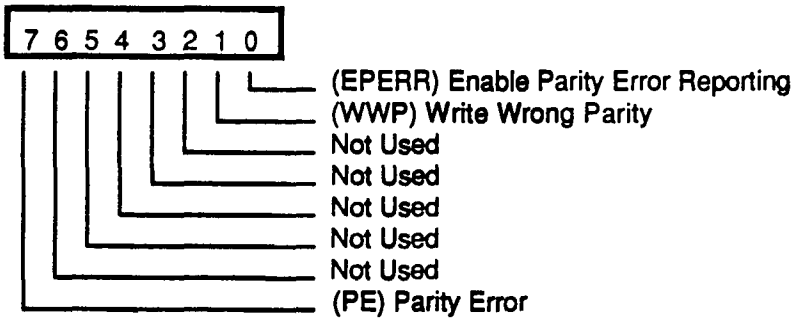
SECTION III

PROGRAMMING INFORMATION

3.1 Control Status Register

The Control Status Register (CSR) provides a VMEbus accessible resister to control and determines the status of the **MM6260AD High Speed Memory**. In the following sections, the CSR bits are defined and their use is explained.

Figure 3.1 CSR. Bit Definitions



Note: The even byte, if read, will return all 1's.

3.1.1 Parity Error Detection

The **MM6260AD High Speed Memory** generates even parity for each byte written during a write access; and checks even parity for each byte read during a read access. If a parity error is detected during a read access, the CSR PE bit will be set. It will be reset by a system bus reset, and may also be reset by writing a 0 to bit 7 of the CSR. If bit 0 is set, (EPERR), and a parity error is detected during a VMEbus read access, the BERR* lead is asserted instead of the DTACK* lead. EPERR will be reset by a system bus reset, and may also be reset by writing a 0 to bit 0 of the CSR.

3.1.2 Write Wrong Parity

When bit 1 of the CSR is set, the parity circuitry may be tested by causing the wrong parity bits to be generated, and written for all locations written while this bit is set.

3.2 Initialization of Memory

Since the memory will power up with random data, each byte location should be written to initialize its associated parity bit, before it is read, or before EPERR in the CSR is set to enable *BERR to be asserted for parity errors on read accesses.

SECTION IV

WARRANTY/SERVICE INFORMATION

4.0 WARRANTY/SERVICE INFORMATION

The MM6260AD family of memory boards have a Lifetime warranty. If it should become necessary to have the board repaired, it is imperative to first call Micro Memory Inc. to get a Return Material Authorization Number (RMA #).

Before shipping, remove all user modifications. Protect the equipment from damage in transit:

1.) Boards should be placed in anti-static bags, and padded shipping bags or boxes.

2.) Allow room in the box for protective padding, e.g., Flow Pack, foam, etc.

3.) Write the Return Authorization number on the outside of the box, and label it "FRAGILE"

4.) Damage sustained due to the lack of compliance in safe return packaging could result in extra repair charges.

5.) Forward the product and all correspondence to:

Micro Memory Inc.
Customer Service Dept.
9540 Vassar Ave.
Chatsworth, Ca.
91311-4141

RMA #_____

APPENDIX A

```
TITLE       MM6260AD VME Address Decode Summer
PATTERN       46150-- U1
REVISION      V1.1
AUTHOR       Roger Peebles
COMPANY       Micro Memory Inc.
DATE        October 10, 1995

DEVICE GAL16V8

OPERATORS * + % /

ES    '46150'

PINS

AM5         1; ADDRESS MODIFIERS- MSB
AM4         2;
AM3         3;
AM2         4;
AM1         5;
AM0         6;
/IACK       7; VME INTERRUPT ACKNOWLEDGE- ACTIVE LOW
SYSRESET      8; VME SYSTEM RESET
BAS         9; BUFFERED ADDRESS STROBE- ACTIVE HIGH

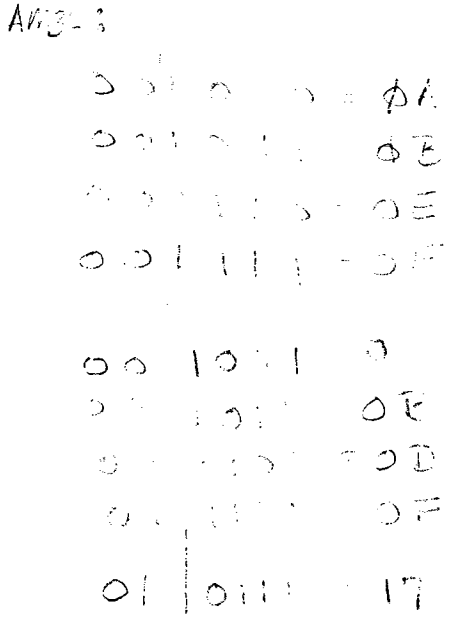
LAM24        14; LATCHED ADDRESS MODIFIER 24
SPBLK        15; SPECIAL BLOCK MODE
VMEBLK         16; VME BLOCK MODES
AM16        17; CSR IN A16 SPACE ADDRESS MODIFIERS
AM24        18; AM24 ADDRESS MODIFIERS
AM32        19; AM32 ADDRESS MODIFIERS

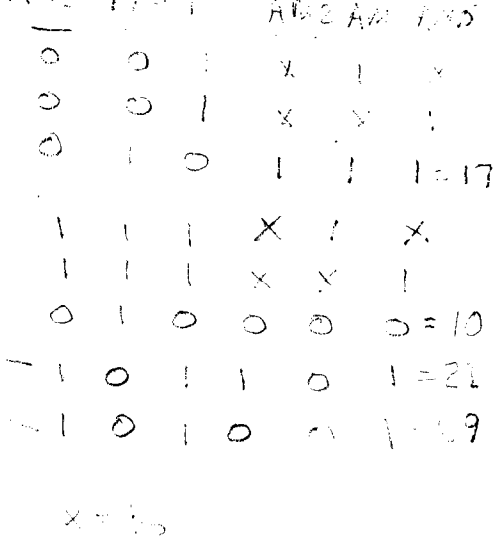

EQUATIONS

AM32 = /AM5 * /AM4 * AM3 * AM1 * /IACK * /SYSRESET
   + /AM5 * /AM4 * AM3 * AM0 * /IACK * /SYSRESET
   + /AM5 * AM4 * /AM3 * AM2 * AM1 * AM0 * /IACK * /SYSRESET
   ;

AM24 = AM5 * AM4 * AM3 * AM1 * /IACK * /SYSRESET
   + AM5 * AM4 * AM3 * AM0 * /IACK * /SYSRESET
   + /AM5 * AM4 * /AM3 * /AM2 * /AM1 * /AM0 * /IACK * /SYSRESET
   ;

AM16 = AM5 * /AM4 * AM3 * AM2 * /AM1 * AM0 * /IACK * /SYSRESET
   + AM5 * /AM4 * AM3 * /AM2 * /AM1 * AM0 * /IACK * /SYSRESET
   ;
```





```
VMEBLK = /AM5 * /AM4 * AM3 * AM1 * AM0 * /IACK * /SYSRESET
    + AM5 * AM4 * AM3 * AM1 * AM0 * /IACK * /SYSRESET
    :

SPBLK = /AM5 * AM4 * /AM3 * AM2 * AM1 * AM0 * /IACK * /SYSRESET
    + /AM5 * AM4 * /AM3 * /AM2 * /AM1 * /AM0 * /IACK * /SYSRESET
    ;

LAM24 = AM5 * AM4 * AM3 * AM1 * /IACK * /SYSRESET * /BAS
    + AM5 * AM4 * AM3 * AM0 * /IACK * /SYSRESET * /BAS
    + /AM5 * AM4 * /AM3 * /AM2 * /AM1 * /AM0 * /IACK * /SYSRESET * /BAS
    + AM5 * AM4 * AM3 * AM1 * /IACK * /SYSRESET * LAM24
    + AM5 * AM4 * AM3 * AM0 * /IACK * /SYSRESET * LAM24
    + /AM5 * AM4 * /AM3 * /AM2 * /AM1 * /AM0 * /IACK * /SYSRESET * LAM24
    + LAM24 * BAS;
```

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