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# MM-6795

## USERs Guide

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# Micro Memory inc.

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# CONVENTIONS

This manual uses the following notational conventions.

NOTE A Note focuses attention on supplementary or unique information and should be read before any action is taken

* or / Used after a signal names (for example DS0* or DS0/) to indicate that the signal is active low and a signal without an asterisk or slash indicates that the signal is active high.

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# SECTION I

# GENERAL INFORMATION

## 1.1 INTRODUCTION

This manual describes the elements of operation and installation procedures of the **MM6795 Flash/Static Memory Module** Random Access Memory Modules.

## 1.2 GENERAL DESCRIPTION

### 1.2.1 Configuration

The **MM6795** is compatible with **VMEbus** specifications (D). Inherent to the module are **VMEbus** options D64/D32/D16/D08(EO) (64/32/16/8 bit data path widths) and A32/A24 (32/24 bit address path widths).

The memory array is addressable as 8 bit bytes, 16 bit words, 32 bit longwords or 64 bit octal word. The **MM6795** can be configured for 8M, 16M, 32M, 64M, 128M and 256M bytes capacity by populating it with 128K, 512K, 1M x 8 industry standard CMOS Static RAMs or Flash devices.

The **MM6795** base memory module is available in several options depending on the capacity required. Table 1.1 lists the optional part numbers for ordering purposes, the total memory capacity provided by each version.

Table 1.1 summarizes the options with respect to storage capacity, available to **MM6795** user.

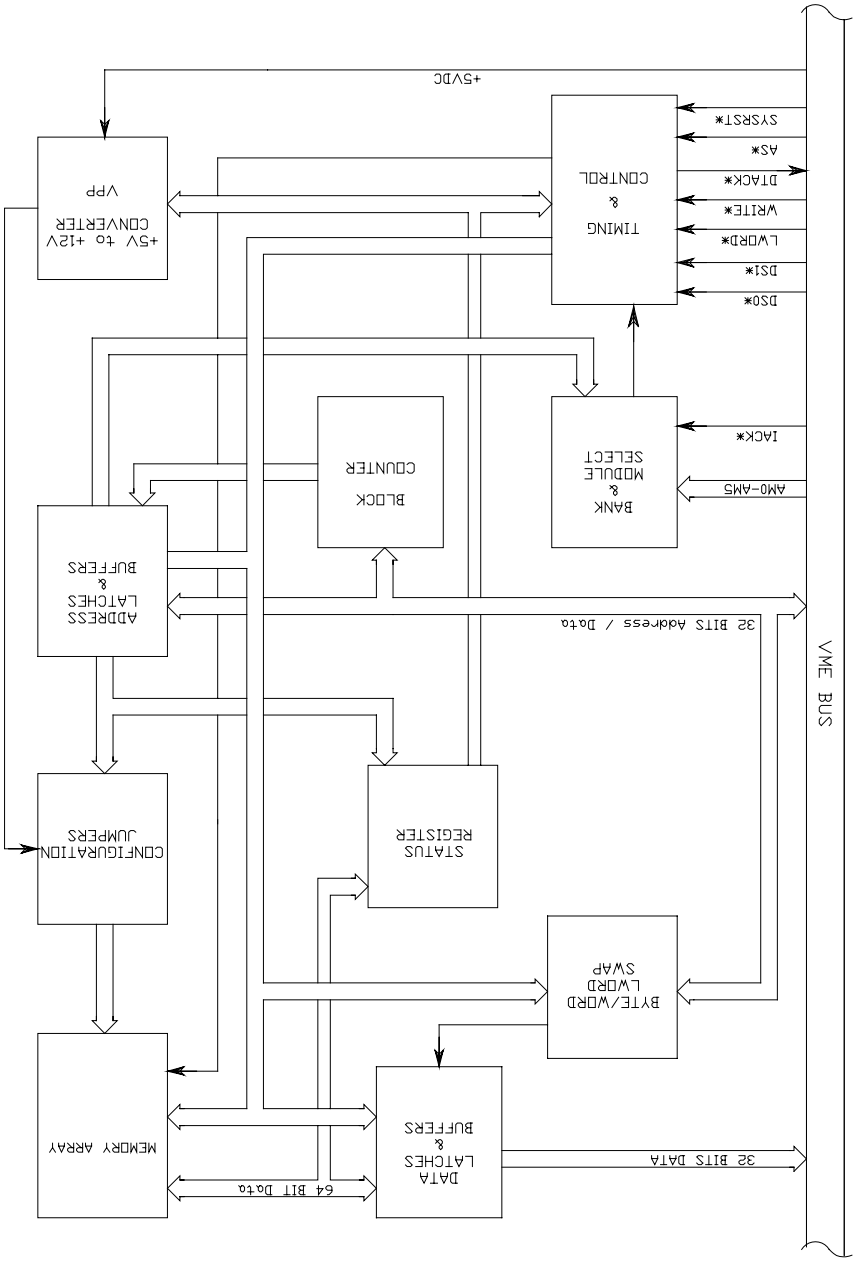
Table 1.1 Memory Capacity Options

CMOS

| OPTION | CAPACITY |
|---|---|
| MM6795C/128M | 128M Bytes |
| MM6795C/64M | 64M Bytes |
| MM6795C/32M | 32M Bytes |
| MM6795C/16M | 16M Bytes |
| MM6795C/8M | 8M Bytes |

FLASH

| OPTION | CAPACITY |
|---|---|
| MM6795F/256M | 256M Bytes |
| MM6795F/128M | 128M Bytes |
| MM6795F/64M | 64M Bytes |
| MM6795F/32M | 32M Bytes |




FUNCTIONAL BLOCK DIAGRAM FIGURE 1.1

### 1.2.2 OPERATIONAL FEATURES

The **MM6795** memory module contains its own address register and data buffers for total compatibility with the **VMEbus**.

Module bank selection for the **MM6795** resides on any 1M (100000 hex) byte boundaries (A24/A32). A module bank may be addressed anywhere within the 4G bytes of physical address space of the **VMEbus** (A32). The **MM6795**'s memory array is addressable as 8 bit bytes (D08(OE)),16 bit words (D16), 32 bit longwords (D32) or 64 bit (D64), using conventional read/write transfers, or HIGH Performance BLOCK Transfers (BLT).

The **MM6795** is configured to respond to various Address Modifier Codes (See Table 1.2). As shipped from the the factory the **MM6795** responds to A32 addresses (using addresses A24-A31), or A24 addresses (ignoring addresses A24-A31). A32 ONLY addresses may be selected (See section 2.5.2). Other combinations are available, (Contact the factory).

TABLE 1.2 Address Modifier Codes

| Hex Code | Address Modifier 5 | 4 | 3 | 2 | 1 | 0 | Function |
|---|---|---|---|---|---|---|---|
| 08 | L | L | H | L | L | L | Extended Non-Privileged 64 Block Transfer (32 Addr) |
| 09 | L | L | H | L | L | H | Extended Non-Privileged Data Access (32 Addr) |
| 0A | L | L | H | L | H | L | Extended Non-Privileged Program Access (32 Addr) |
| 0B | L | L | H | L | H | H | Extended Non-Privileged Block Transfer (32 Addr) |
| 0C | L | L | H | H | L | L | Extended Non-Privileged 64 Block Transfer (32 Addr) |
| 0D | L | L | H | H | L | H | Extended Supervisory Data Access (32 Addr) |
| 0E | L | L | H | H | H | L | Extended Supervisory Program Access (32 Addr) |
| 0F | L | L | H | H | H | H | Extended Supervisory Block Transfer (32 Addr) |
| 38 | H | H | H | L | L | L | 64 bit Non-Priviledged Block Transfer (24 Addr) |
| 39 | H | H | H | L | L | H | Standard Non-Privileged Data Access (24 Addr) |
| 3A | H | H | H | L | H | L | Standard Non-Privileged Program Access (24 Addr) |
| 3B | H | H | H | L | H | H | Standard Non-Privileged Block transfer (24 Addr) |
| 3C | H | H | H | H | L | L | 64-bit Supervisory Block Transfer (24 Addr) |
| 3D | H | H | H | H | L | H | Standard Supervisory Data Access (24 Addr) |
| 3E | H | H | H | H | H | L | Standard Supervisory Program Access (24 Addr) |
| 3F | H | H | H | H | H | H | Standard Supervisory Block Transfer (24 Addr) |

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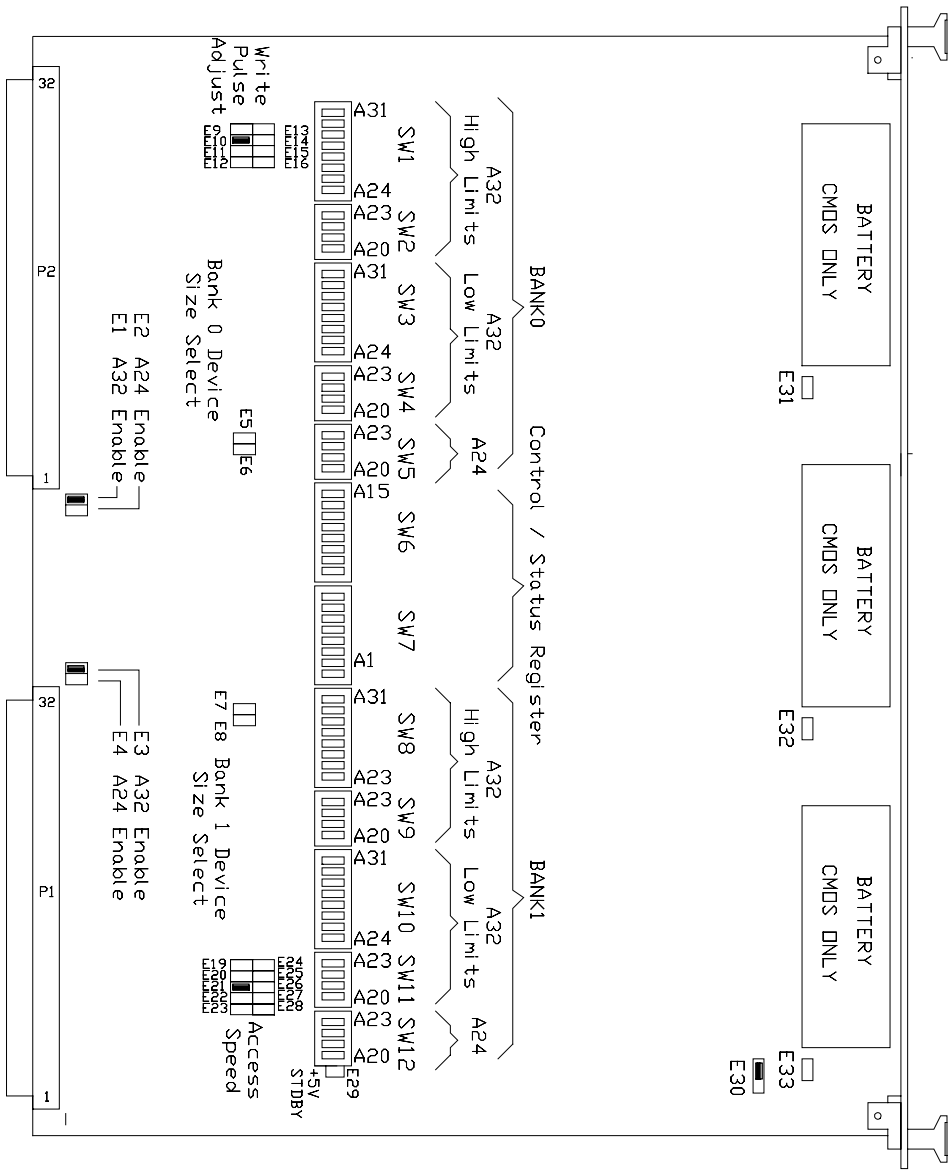



FIGURE 1.2 JUMPER & SWITCH LOCATIONS

## 1.3 GENERAL SPECIFICATIONS

Table 1.3 lists the general specifications for the **MM6795** Static Memory Module

| Characteristics | Specifications |
|---|---|
| Capacity | CMOS NVRAM: 16, 32,64,128 Mbytes<br>˝<br>Flash Memory: 32, 64, 128, 256 Mbytes |
| Address | 32-bits plus a 6-bit meory address modifier |
| Data In/Data Out | 8,16,32,64 bits (UAT) and block transfer (BLT) of 256 bytes<br>VME and 2 Kbytes for VME64(MBLT) |
| Modes of Operation | Read, write, read-modify-write |
| Module Selection | 1 Mbytes boundaries, switch-selectable |
| Interface:<br>˝<br>Inputs<br>˝<br>Outputs | VME/VME64 Rev D<br>˝<br>TTL-compatible |
| Battery Types:<br>˝<br><br>˝<br>NICAD - Rechargeable (3 batteries)<br>˝<br>or<br>˝<br>Lithium - Non-chargeable (3 batteries) | Each battery type has a voltage monitor and LEDs to indicate battery status. Three redundant batteries<br>AA type 100ma/hr each<br>(300mah Total)<br>AA Type 1.5A/hr each<br>(4.5Ah Total) |
| Data Retention:<br>CMOS (Fully populated) | <br>3 years - Lithium Non-chargeable<br>4 weeks - NICAD chargeable |
| Vpp Supply (+12.0vdc) | Rated at 250ma<br>˝<br>(Programmable ENABLE) |
| Operating Temperature | 0 to 70°Celsius |
| Storage Temperature | -40 to +85°Celsius |
| Relative Humidity | Up to 95% without condensation |
| Power Requirements:<br>˝<br>+5V (Fully - Populated) | Standby Operate<br>1.6A 1.8A |

Table 1.4 VME P1 Connector Pin Assignments
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| PIN | ROW A<br>˝<br>SIGNAL | ROW B<br>˝<br>SIGNAL | ROW C<br>˝<br>SIGNAL |
|---|---|---|---|
| 1 | D00 | ** BBSY* | D08 |
| 2 | D01 | ** BCLR* | D09 |
| 3 | D02 | ** ACFAIL* | D10 |
| 4 | D03 | BGOIN* | D11 |
| 5 | D04 | ** BGOOUT* | D12 |
| 6 | D05 | ** BG1IN* | D13 |
| 7 | D06 | ** BG1OUT* | D14 |
| 8 | D07 | ** BG2IN* | D15 |
| 9 | GROUND | ** BG2OUT* | GROUND |
| 10 | ** SYSCLK | ** BG3IN* | SYSFAIL |
| 11 | GROUND | ** BG3OUT* | BERR* |
| 12 | DS1* | ** BR0* | SYSRESET* |
| 13 | DS0* | ** BR1* | LWORD* |
| 14 | WRITE* | ** BR2* | AM5 |
| 15 | GROUND | ** BR3* | A23 |
| 16 | DTACK* | AM0 | A22 |
| 17 | GROUND | AM1 | A21 |
| 18 | AS* | AM2 | A20 |
| 19 | GROUND | AM3 | A19 |
| 20 | IACK* | GROUND | A18 |
| 21 | ** IACKIN* | ** SERCLK | A17 |
| 22 | ** IACKOUT* | ** SERDAT | A16 |

| | | | |
|---|---|---|---|
| 23 | AM4 | GROUND | A15 |
| 24 | A07 | ** IRQ7* | A14 |
| 25 | A06 | ** IRQ6* | A13 |
| 26 | A05 | ** IRQ5* | A12 |
| 27 | A04 | ** IRQ4* | A11 |
| 28 | A03 | ** IRQ3* | A10 |
| 29 | A02 | ** IRQ2* | A09 |
| 30 | A01 | ** IRQ1* | A08 |
| 31 | ** -12V | ** +5V STDBY | ** +12V |
| 32 | +5V | +5V | +5V |

˝

NOTE: ** No connection on **MM6795** High Speed Memory

Table 1.5 VME P2 Connecter Pin Assignments

| PIN | ROW A SIGNAL | ROW B SIGNAL | ROW C SIGNAL |
|---|---|---|---|
| 1 | User I/O | +5 Volts | User I/O |
| 2 | User I/O | GND | User I/O |
| 3 | User I/O | RESERVED | User I/O |
| 4 | User I/O | A24 | User I/O |
| 5 | User I/O | A25 | User I/O |
| 6 | User I/O | A26 | User I/O |
| 7 | User I/O | A27 | User I/O |
| 8 | User I/O | A28 | User I/O |
| 9 | User I/O | A29 | User I/O |
| 10 | User I/O | A30 | User I/O |
| 11 | User I/O | A31 | User I/O |
| 12 | User I/O | GND | User I/O |
| 13 | User I/O | +5 Volts | User I/O |
| 14 | User I/O | D16 | User I/O |
| 15 | User I/O | D17 | User I/O |
| 16 | User I/O | D18 | User I/O |
| 17 | User I/O | D19 | User I/O |
| 18 | User I/O | D20 | User I/O |
| 19 | User I/O | D21 | User I/O |
| 20 | User I/O | D22 | User I/O |
| 21 | User I/O | D23 | User I/O |
| 22 | User I/O | GND | User I/O |
| 23 | User I/O | D24 | User I/O |
| 24 | User I/O | D25 | User I/O |

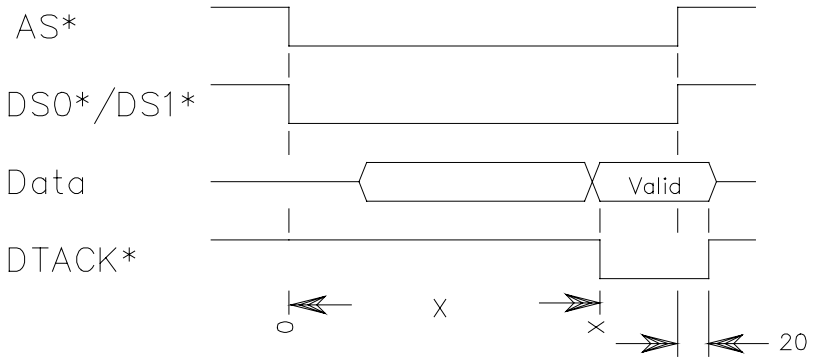
| | | | |
|---|---|---|---|
| 25 | User I/O | D26 | User I/O |
| 26 | User I/O | D27 | User I/O |
| 27 | User I/O | D28 | User I/O |
| 28 | User I/O | D29 | User I/O |
| 29 | User I/O | D30 | User I/O |
| 30 | User I/O | D31 | User I/O |
| 31 | User I/O | GND | User I/O |
| 32 | User I/O | +5 Volts | User I/O |

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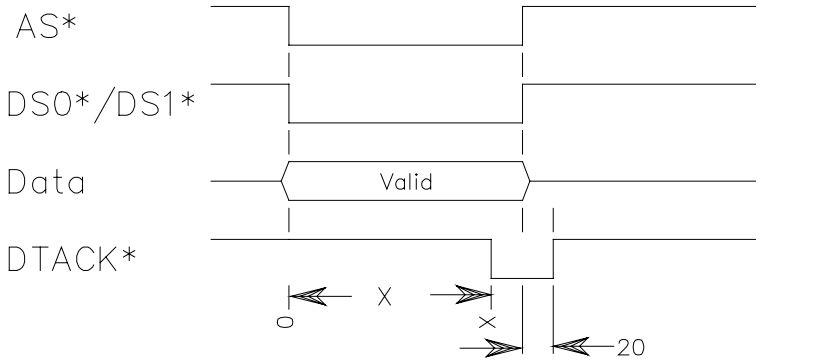
## 1.4 INTERFACE TIMING

The Interface Timing Diagram illustrates the timing relationships on the Data Transfer bus,for Read and Write Cycles. Access delay time is measured from the leading edge of the Data strobes at the **VMEbus**. (See Figure 1.3).




WHERE X = ACCESS SPEED SELECTION (See Section 2.5.1)

Read Cycle




WHERE X = ACCESS SPEED SELECTION (See Section 2.5.1)

Write Cycle

FIGURE 1.3 INTERFACE TIMING DIAGRAM

## 1.5 MEMORY ARRAY ORGANIZATION

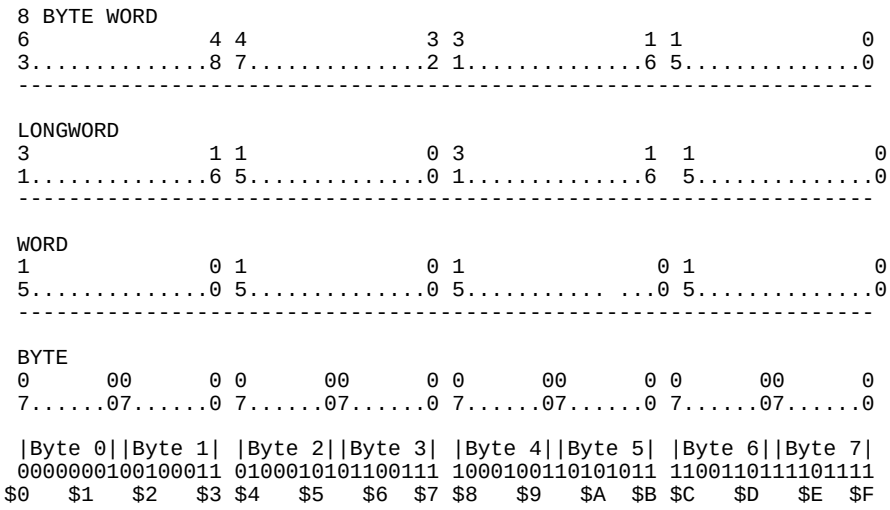
The memory array is partitioned into two (2) 64 bit wide segments. The minimum memory configuration would be 1M x 64. This would translate to a minimum configuration of 8Megabytes for the **MM6795** Static Memory Module. The 64 bits of data are divided into 8 bytes (8 bits each). While the memory reads and writes may be 8, 16, 32 or 64 bits wide, the memory is organized as 64 bit wide locations with logic controlling which byte<s> the user is reading or writing.

If the contents of the first 8 locations in memory are $01 $23 $45 $67 $89 $AB $CD $EF, determining which bits constitute what byte may be somewhat confusing. This can be cleared up by seeing the same data in the various formats used in most systems (IE: Byte, Word, Longword and 8 Byte Word).

BYTE Format WORD Format LONGWORD Format 8 BYTE WORD Format

| Location | Data | Location | Data | Location | Data | Location | Data |
|---|---|---|---|---|---|---|---|
| $00000000 | $01 | $00000000 | $0123 | $00000000 | $01234567 | $00000000 | $0123456789ABCDEF |
| $00000001 | $23 | $00000002 | $4567 | $00000004 | $89ABCDEF | | |
| $00000002 | $45 | $00000004 | $89AB | | | | |
| $00000003 | $67 | $00000006 | $CDEF | | | | |
| $00000004 | $89 | | | | | | |
| $00000005 | $AB | | | | | | |
| $00000006 | $CD | | | | | | |
| $00000007 | $EF | | | | | | |

BIT Organizations



# SECTION II

# INSTALLATION

## 2.1 INTRODUCTION

This section details the step by step procedure to interface the **MM6795 Flash/Static Memory Module** with the **VMEbus**.

## 2.2 UNPACKING INSTRUCTIONS

Unpack module(s) from shipping carton. If carton is damaged upon receipt, request that the carrier's agent be present during unpacking and inspection of the equipment. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment. For repairs or replacement of a board damaged during shipment, contact **Micro Memory Inc.** to obtain a Return Authorization number and further instructions.

## 2.3 HARDWARE PREPARATION

The **MM6795** memory module should be inspected and prepared for jumper placement and switch settings prior to system installation. The following sections describe the proper jumper options and switch settings necessary for system operation. Figure 1.2 illustrates jumper and switch locations and should be referenced as necessary.

2.3.1 Handling Procedure

The **MM6795** uses MOS components that are susceptible to damage if exposed to static electrical charges. To avoid damage of these components during handling, testing or operation, the following procedure should be used.

A. Device leads should contact conductive material to avoid building of any static charge, except during testing or operation.

B. Soldering iron tips, metal fixtures, tools, and handling facilities used in preparing the module for operation should be grounded.

C. Devices should never be removed or inserted while power is applied to the module because voltage transients may permanently damage the devices and/or module.

D. The memory module should never be plugged in or out of the cardcage while power is applied.

E. External signals should not be applied to device inputs while power is removed.

F. Any memory module removed from the system should be transferred to either non-conductive foam or an anti- static plastic bag for storage or shipment.

## 2.4 OPERATING AIRFLOW AND COOLING

An adequate airflow is required to maintain the operating temperature within specifications of the memory module.

## 2.5 JUMPER & SWITCH OPTIONS

There are several jumper options attainable on the **MM6795 Flash/Static Memory Module** depending on the application. Most of the available options are selected by installing or removing mini-jumpers on wire-wrap pins at 0.100 inch centers. (See Figure 1.2 for jumper locations)

### 2.5.1 ACCESS SPEED SELECTION (Factory Installed Option)

The **MM6795 Flash/Static Memory Module** may be configured for one (1) of ten (10) speed devices. Jumpers **E19 through E28** controls the speed at which the **MM6795 Flash/Static Memory Module** responds. Install only one jumper in the correct location to select the required speed. (See table below).

Table 2.1 Access Speed Jumper Selection

| JUMPER | SELECTED ACCESS SPEED |
|---|---|
| E28 | 15ns |
| E27 | 30ns |
| E26 | 45ns |
| E25 | 60ns |
| E24 | 75ns |
| E23 | 90ns |
| E22 | 105ns |
| E21 | 120ns |
| E20 | 135ns |
| E19 | 150ns |

| | |
|---|---|
| E28 | 15ns |
| E26 | 45ns |
| E24 | 75ns |
| E22 | 105ns |
| E20 | 135ns |

2.5.2 WRITE Pulse Timing (Factory Installed Option)

The **MM6795 Flash/Static Memory Module** may be configured for one (1) of ten (10) speed devices. **Jumpers E18 through E9** controls the speed of the **WE*** pin. Install only one jumper in the correct location to select the required speed. (See table below).

Table 2.2 Write Pulse Timing Jumper Selection

| JUMPER | WRITE PULSE TIMING |
|---|---|
| E18 | 10ns |
| E17 | 20ns |
| E16 | 30ns |
| E15 | 40ns |
| E14 | 50ns |
| E13 | 60ns |
| E12 | 70ns |
| E11 | 80ns |
| E10 | 90ns |
| E9 | 100ns |

| | |
|---|---|
| E18 | 10ns |
| E16 | 30ns |
| E14 | 50ns |
| E12 | 70ns |
| E10 | 90ns |

″

2.5.3 ADDRESS MODIFIER SELECTION (Bank 0 E1 = A32 and E2 = A24)

″

(Bank 1 E3 = A32 and E4 = A24)

″

″

As shipped from the factory, the **MM6795 Flash/Static Memory Module** may be selected using either A24 or A32 Address Modifiers. However removing E2 and/or E4 will disable A24 requests and will ignore addresses A24 through A31. E1 and/or E3 enables (installed) or disables (removed) A32 requests.

2.5.4 Control / Status Register (CSR) Definition

The Control/Status Register (CSR) on the **MM6795 Flash/Static Memory Module** is a 16 bit (WORD) read/write register, located at the EVEN address (ie: 0000, 0002, ...) of the selected I/O location.

2.5.4.1 Bit 4 - Vpp the Programing Voltage (+12V)

The **MM6795 Flash/Static Memory Module** contains of a DC to DC converter to generate the +12VDC (Vpp) for Flash programming voltage requirement. The Vpp supply is controlled by writing a 1 (ON) or 0 (OFF default) to bit 4 of the CSR location.

2.5.4.3 Battery Status

The on-board redundant batteries (CMOS Versions ONLY) may be checked by reading Bits 2 through . Bit 2 will be set to a '1' if battery 3 voltage drops below the 'Factory Set ' limits. Bit 1 will be set to a '1' if the battery 2 voltage drops below the 'Factory Set' limits. Bit 0 will be set to a '1' if the battery 1 voltage drops below the 'Factory Set' limits. LED 1 through 3 will turn on when battery 1 through 3 drop below the 'Factory Set' limits respectively.

Table 2.3 Control/Status Register Bit Definitions

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| WRITE | x | x | x | x | x | x | x | x | | x | x | x | V | x | x | x | x |
| READ | x | x | x | x | x | x | x | x | | D | x | x | V | R | B3 | B2 | B1 |

″

Where:

″

B1 = Battery #1 Status (1 = Bat. FAIL) (Read ONLY)
B2 = Battery #2 Status (1 = Bat. FAIL) (Read ONLY)
B3 = Battery #3 Status (1 = Bat. FAIL) (Read ONLY)
V = +12.0vdc (1 = Supply On / 0 = Supply Off) (Read/Write)
R = Ready/Status = Sample of RDY/BSY* of the device that supports that pin
D = DC fail
x = Indeterminate / Don't Care

For example, if reading the CSR register returns 0000 0000 0000 0111 it means all three batteries are below factory set limits.

## 2.6 Module Address Selection

The **MM6795 Flash/Static Memory Module** may be addressed, starting at any 1 Mbyte boundary in the VME bus A32 (4GBytes) and/or A24 (16MBytes) physical address space. There are two separate banks on the MM6795. The bank selection is accomplished by setting the **Low Limit** (starting or FIRST location) Address and the **High Limit** (ending or LAST location) address. The bank selection tables included Table 2.3.1 through Table 2.3.3 (High Limits) and Table 2.4.1 through Table 2.4.3 (Low Limits).

The two High Limit switches are divided into three groups of 4 bits each. Each table shows the settings of one of the three group of 4 bits with the other two groups represented by letters. The Letters x,y,z represent the hex values of A31to A28, A27 to A24 and A23 to A20 address bits respectively.

For example to set the bank 0 address upper limit of $123FFFFF (hex). go to Table 2.1.1 find $1yzFFFFF for the first digit. Set SW1 positions 8, 7, 6 to closed and position 5 to OPEN.. Next in Table 2.1.2 find $x2zFFFFF for the second digit. Set SW1 positions 4,3,1 to closed and position 2 to OPEN. Finally in Table 2.1.3 find $xy3FFFFF for the third digit. Set SW2 positions 4 and 3 to closed and positions 2 and 1 to OPEN. The final switch settings are shown in Figure 2.2.

The Lower Limit switches are set as described above. For example to set Bank 1 Lower Limit to $0230000. Find $0yz00000 for the first digit. Set SW9 all positions to closed. Next find $x2z00000 for the second digit. Set SW9 positions 4,3,1 to closed and position 2 to OPEN. Finally find $xy300000 for the third digit. Set SW11 positions 4,3 to closed and 2,1 to OPEN. The final switch settings are shown in Figure 2.3.

The switches in the above paragraph were marked OPEN on one side. If the switch manufacturer has mark their switches either ON or OFF. Substitute ON for OPEN and OFF for closed.

Note that the High Limit for A24 accesses is set separately from that for A32, by switch 5 for bank 0, and switch 12 for bank 1.

SW5 SW12

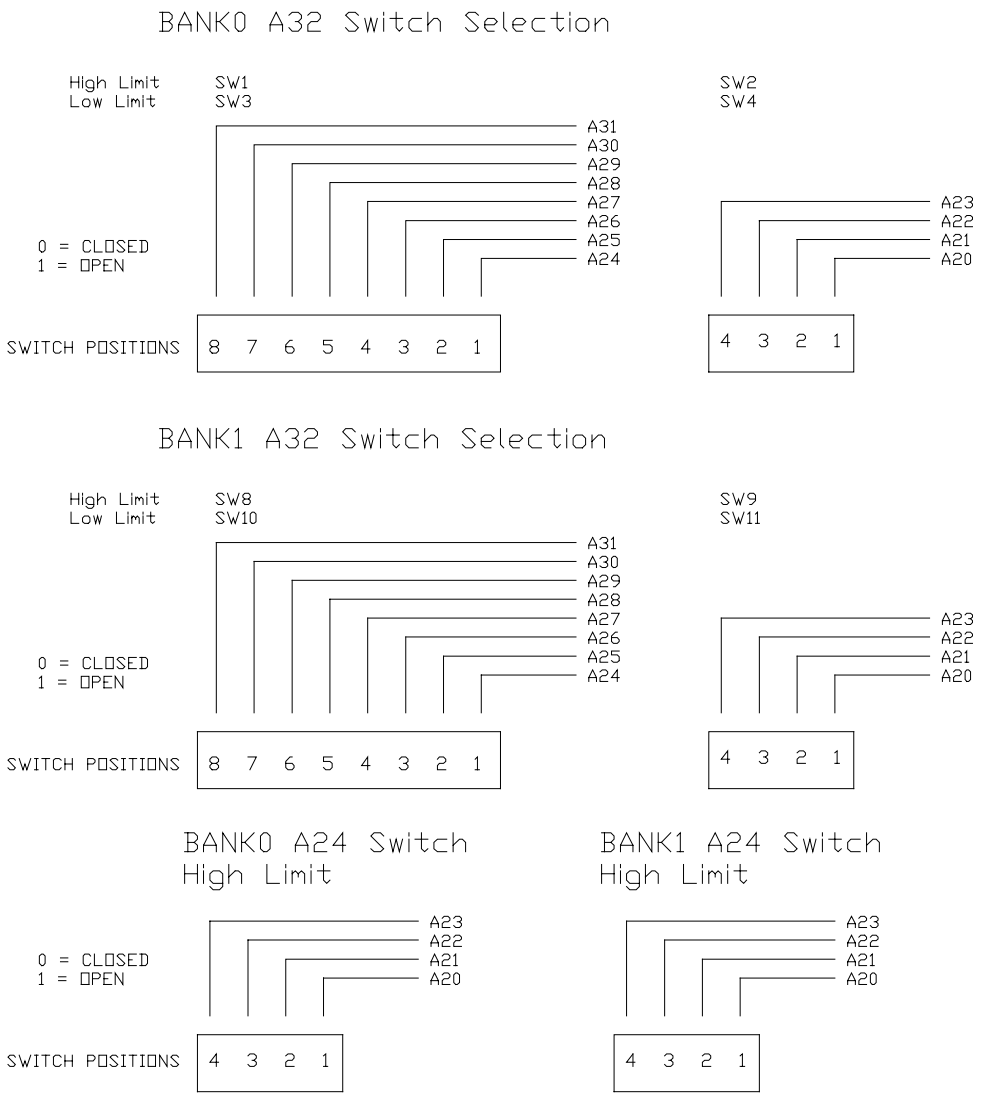



Figure 2.1 Module Address Switch Settings

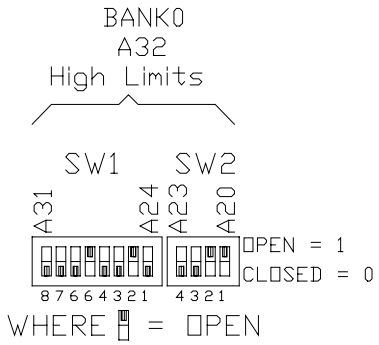



Figure 2.2 Bank 0 Upper Limit $123FFFFF Switch Settings

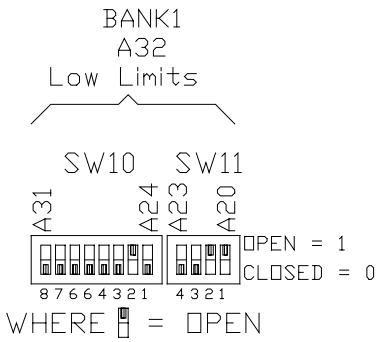



Figure 2.3 Bank 1 Upper Limit $02300000 Switch Settings

Table 2.3.1 through 2.4.3 BANK ADDRESS SELECTION

All Switches 1 = Open
0 = Close

Table 2.3.1 A31-A28 Upper Limit Address Selection

| High Limit | (A31 - A28) |
|---|---|
| SWITCH POSITION | BANK 0 SW1 ... BANK 1 SW8<br>8.7.6.5 |
| $0yzFFFFF | 0 0 0 0 |
| $1yzFFFFF | 0 0 0 1 |
| $2yzFFFFF | 0 0 1 0 |
| $3yzFFFFF | 0 0 1 1 |
| $4yzFFFFF | 0 1 0 0 |
| $5yzFFFFF | 0 1 0 1 |
| $6yzFFFFF | 0 1 1 0 |
| $7yzFFFFF | 0 1 1 1 |
| $8yzFFFFF | 1 0 0 0 |
| $9yzFFFFF | 1 0 0 1 |
| $AyzFFFFF | 1 0 1 0 |
| $ByzFFFFF | 1 0 1 1 |
| $CyzFFFFF | 1 1 0 0 |
| $DyzFFFFF | 1 1 0 1 |
| $EyzFFFFF | 1 1 1 0 |
| $FyzFFFFF | 1 1 1 1 |

Table 2.3.2 A27-A24 Upper Limit Address Selection

| High Limit | (A27 - A24) |
|---|---|
| SWITCH POSITION | BANK 0 SW1 ... BANK 1 SW8<br>4 3 2 1 |
| $x0zFFFFF | 0 0 0 0 |
| $x1zFFFFF | 0 0 0 1 |
| $x2zFFFFF | 0 0 1 0 |
| $x3zFFFFF | 0 0 1 1 |
| $x4zFFFFF | 0 1 0 0 |
| $x5zFFFFF | 0 1 0 1 |
| $x6zFFFFF | 0 1 1 0 |
| $x7zFFFFF | 0 1 1 1 |
| $x8zFFFFF | 1 0 0 0 |
| $x9zFFFFF | 1 0 0 1 |
| $xAzFFFFF | 1 0 1 0 |
| $xBzFFFFF | 1 0 1 1 |
| $xCzFFFFF | 1 1 0 0 |
| $xDzFFFFF | 1 1 0 1 |
| $xEzFFFFF | 1 1 1 0 |
| $xFzFFFFF | 1 1 1 1 |

˝

Table 2.3.3 Upper Limit A23 -A20 Address Selection

| High Limit | (A23 - A20) |
|---|---|
| SWITCH<br>″<br>″<br>POSITION | BANK 0 SW2<br>″<br>BANK 1 SW9<br>″<br>4 3 2 1 |
| $xy0FFFFF | 0 0 0 0 |
| $xy1FFFFF | 0 0 0 1 |
| $xy2FFFFF | 0 0 1 0 |
| $xy3FFFFF | 0 0 1 1 |
| $xy4FFFFF | 0 1 0 0 |
| $xy5FFFFF | 0 1 0 1 |
| $xy6FFFFF | 0 1 1 0 |
| $xy7FFFFF | 0 1 1 1 |
| $xy8FFFFF | 1 0 0 0 |
| $xy9FFFFF | 1 0 0 1 |
| $xyAFFFFF | 1 0 1 0 |
| $xyBFFFFF | 1 0 1 1 |
| $xyCFFFFF | 1 1 0 0 |
| $xyDFFFFF | 1 1 0 1 |
| $xyEFFFFF | 1 1 1 0 |
| $xyFFFFFF | 1 1 1 1 |

″

″

Table 2.4.1 Lower Limit A31-A28 Address Selection

″

| Low Limit | (A31 - A28) |
|---|---|
| SWITCH<br>″<br>POSITION | BANK 0 SW3<br>BANK 1 SW10<br>8 7 6 5 |
| $0yz00000 | 0 0 0 0 |
| $1yz00000 | 0 0 0 1 |
| $2yz00000 | 0 0 1 0 |
| $3yz00000 | 0 0 1 1 |
| $4yz00000 | 0 1 0 0 |
| $5yz00000 | 0 1 0 1 |
| $6yz00000 | 0 1 1 0 |
| $7yz00000 | 0 1 1 1 |
| $8yz00000 | 1 0 0 0 |
| $9yz00000 | 1 0 0 1 |
| $Ayz0000 | 1 0 1 0 |
| $Byz00000 | 1 0 1 1 |
| $Cyz00000 | 1 1 0 0 |
| $Dyz00000 | 1 1 0 1 |
| $Eyz00000 | 1 1 1 0 |
| $Fyz00000 | 1 1 1 1 |

″

Table 2.4.2 Lower Limit A27 -A24 Address Selection

| Low Limit | (A27 - A24) |
|---|---|
| SWITCH<br>˝<br>POSITION<br>˝ | BANK 0 SW3<br>˝<br>BANK 1 SW10<br>˝<br>4 3 2 1 |
| $x0z00000 | 0 0 0 0 |
| $x1z00000 | 0 0 0 1 |
| $x2z00000 | 0 0 1 0 |
| $x3z00000 | 0 0 1 1 |
| $x4z00000 | 0 1 0 0 |
| $x5z00000 | 0 1 0 1 |
| $x6z00000 | 0 1 1 0 |
| $x7z00000 | 0 1 1 1 |
| $x8z00000 | 1 0 0 0 |
| $x9z00000 | 1 0 0 1 |
| $xAz00000 | 1 0 1 0 |
| $xBz00000 | 1 0 1 1 |
| $xCz00000 | 1 1 0 0 |
| $xDz00000 | 1 1 0 1 |
| $xEz00000 | 1 1 1 0 |
| $xFz00000 | 1 1 1 1 |

˝

˝

˝

Table 2.4.3 Lower Limit A23-A20 Address Selection

| Low Limit | (A23 - A20) |
|---|---|
| SWITCH<br>˝<br>˝<br>POSITION | BANK 0 SW4<br>˝<br>BANK 1 SW11<br>˝<br>4.3.2.1 |
| $xy000000 | 0 0 0 0 |
| $xy100000 | 0 0 0 1 |
| $xy200000 | 0 0 1 0 |
| $xy300000 | 0 0 1 1 |
| $xy400000 | 0 1 0 0 |
| $xy500000 | 0 1 0 1 |
| $xy600000 | 0 1 1 0 |
| $xy700000 | 0 1 1 1 |
| $xy800000 | 1 0 0 0 |
| $xy900000 | 1 0 0 1 |
| $xyA00000 | 1 0 1 0 |
| $xyB00000 | 1 0 1 1 |
| $xyC00000 | 1 1 0 0 |
| $xyD00000 | 1 1 0 1 |
| $xyE00000 | 1 1 1 0 |
| $xyF00000 | 1 1 1 1 |

## 2.7 Control/Status Register Address Selection

The **MM6795 Memory Module** contains a board Status Register which may be located on any EVEN (WORD) boundary (ie: 0000, 0002, ...) located in **VMEbus** A16 (I/O) space. (See Section 2.5.4)

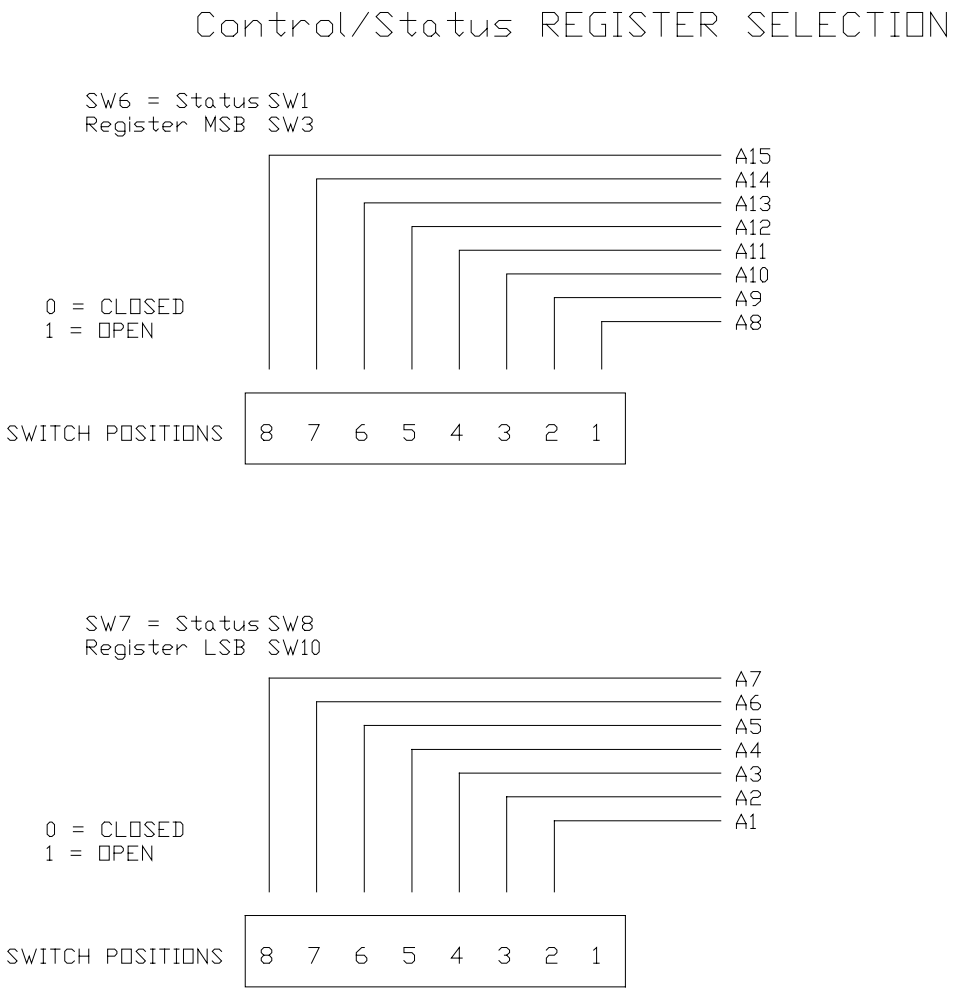



Figure 2.2 Control/Status Register Switch Settings

# SECTION III

## 3.1 WARRANTY / SERVICE INFORMATION

The **MM6795** family of memory boards have a one year warranty. If it should become necessary to have the board repaired, it is imperative to first call **Micro Memory Inc**. to obtain a Return Material Authorization Number (RMA #).

Before calling Micro Memory you should have the following information available:

1. Model and Serial Number of the product
2. Company name
3. Your shipping address
4. Telephone number and contact name

Before shipping, remove all user modifications. Protect the product from transit:

1. Product should be placed in an anti-static bag, and padded shipping box.

2. Write the R.M.A. number on the outside of the box, and label it **FRAGILE**.

3. Damage sustained due to the lack of compliance in return packaging could result in extra repair charges.

4. Forward the product and all correspondence to:

**Micro Memory Inc.**
Customer Service Dept.
9540 Vassar Ave.
Chatsworth, Ca.
91311-4141

RMA #_____

**NOTE:** Before returning your board for service or repair, be sure to remove your custom-modifications or devices and to reinstall the defaults.

Do not send your custom-modifications or devices in with the board. They are not required for board repair and their return is not guaranteed.

# Appendix A

**U1 Address Modifier Logic Equations**

```
module     u1
TITLE      'U1 - PN46xxx (MM6795 VMEbus AM Control)'

" REVISION  NC
" AUTHOR    Michael Hasenfratz - Created: September 19, 1995 [09:32am]
" COMPANY   Micro Memory Inc. Chatsworth, Ca.
" DATE      October 3, 1995 [03:10pm]

"       This device controls the VMEbus Address Modifier/Selection

am5      PIN   1; "Address Modifier 5
am4      PIN   2; "Address Modifier 4
am3      PIN   3; "Address Modifier 3
am2      PIN   4; "Address Modifier 2
am1      PIN   5; "Address Modifier 1
am0      PIN   6; "Address Modifier 0

!iack    PIN   7; "Interrupt ACKnowlage
bsysrst  PIN   8; "VME 'SYSRST*' (inverted)

blk      PIN  14; "BLOCK MODE REQUESTED
d64      PIN  15; "VME D64 (MBLT) AM
!am16    PIN  16; "VME I/O (A16) AM
!am24    PIN  17; "VME A24 AM
!am32    PIN  18; "VME A32 AM

EQUATIONS

am32     = !am5 & !am4 &  am3 & !am2 & !am1 &  am0 & !bsysrst & !iack " 0x09
       # !am5 & !am4 &  am3 & !am2 &  am1 & !am0 & !bsysrst & !iack " 0x0a
       # !am5 & !am4 &  am3 & !am2 &  am1 &  am0 & !bsysrst & !iack " 0x0b
       # !am5 & !am4 &  am3 &  am2 & !am1 &  am0 & !bsysrst & !iack " 0x0d
       # !am5 & !am4 &  am3 &  am2 &  am1 & !am0 & !bsysrst & !iack " 0x0e
       # !am5 & !am4 &  am3 &  am2 &  am1 &  am0 & !bsysrst & !iack " 0x0f
       # !am5 & !am4 &  am3 & !am2 & !am1 & !am0 & !bsysrst & !iack " 0x08
       # !am5 & !am4 &  am3 &  am2 & !am1 & !am0 & !bsysrst & !iack " 0x0c
       ;

am24     =  am5 &  am4 &  am3 & !am2 & !am1 &  am0 & !bsysrst & !iack " 0x39
       #  am5 &  am4 &  am3 & !am2 &  am1 & !am0 & !bsysrst & !iack " 0x3a
       #  am5 &  am4 &  am3 & !am2 &  am1 &  am0 & !bsysrst & !iack " 0x3b
       #  am5 &  am4 &  am3 &  am2 & !am1 &  am0 & !bsysrst & !iack " 0x3d
       #  am5 &  am4 &  am3 &  am2 &  am1 & !am0 & !bsysrst & !iack " 0x3e
       #  am5 &  am4 &  am3 &  am2 &  am1 &  am0 & !bsysrst & !iack " 0x3f
       #  am5 &  am4 &  am3 & !am2 & !am1 & !am0 & !bsysrst & !iack " 0x38
       #  am5 &  am4 &  am3 &  am2 & !am1 & !am0 & !bsysrst & !iack " 0x3c
       ;

am16     =  am5 & !am4 &  am3 & !am2 & !am1 &  am0 & !bsysrst & !iack " 0x29
       #  am5 & !am4 &  am3 &  am2 & !am1 &  am0 & !bsysrst & !iack " 0x2d
```

```
      ;

blk     = !am5 & !am4 &  am3 & !am2 &  am1 &  am0 & !bsysrst & !iack " 0x0b
      # !am5 & !am4 &  am3 &  am2 &  am1 &  am0 & !bsysrst & !iack " 0x0f
      # !am5 & !am4 &  am3 & !am2 & !am1 & !am0 & !bsysrst & !iack " 0x08
      # !am5 & !am4 &  am3 &  am2 & !am1 & !am0 & !bsysrst & !iack " 0x0c
      #  am5 &  am4 &  am3 & !am2 &  am1 &  am0 & !bsysrst & !iack " 0x3b
      #  am5 &  am4 &  am3 &  am2 &  am1 &  am0 & !bsysrst & !iack " 0x3f
      #  am5 &  am4 &  am3 & !am2 & !am1 & !am0 & !bsysrst & !iack " 0x38
      #  am5 &  am4 &  am3 &  am2 & !am1 & !am0 & !bsysrst & !iack " 0x3c
      ;

d64     = !am5 & !am4 &  am3 & !am2 & !am1 & !am0 & !bsysrst & !iack " 0x08
      # !am5 & !am4 &  am3 &  am2 & !am1 & !am0 & !bsysrst & !iack " 0x0c
      #  am5 &  am4 &  am3 & !am2 & !am1 & !am0 & !bsysrst & !iack " 0x38
      #  am5 &  am4 &  am3 &  am2 & !am1 & !am0 & !bsysrst & !iack " 0x3c
      ;

END
```

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