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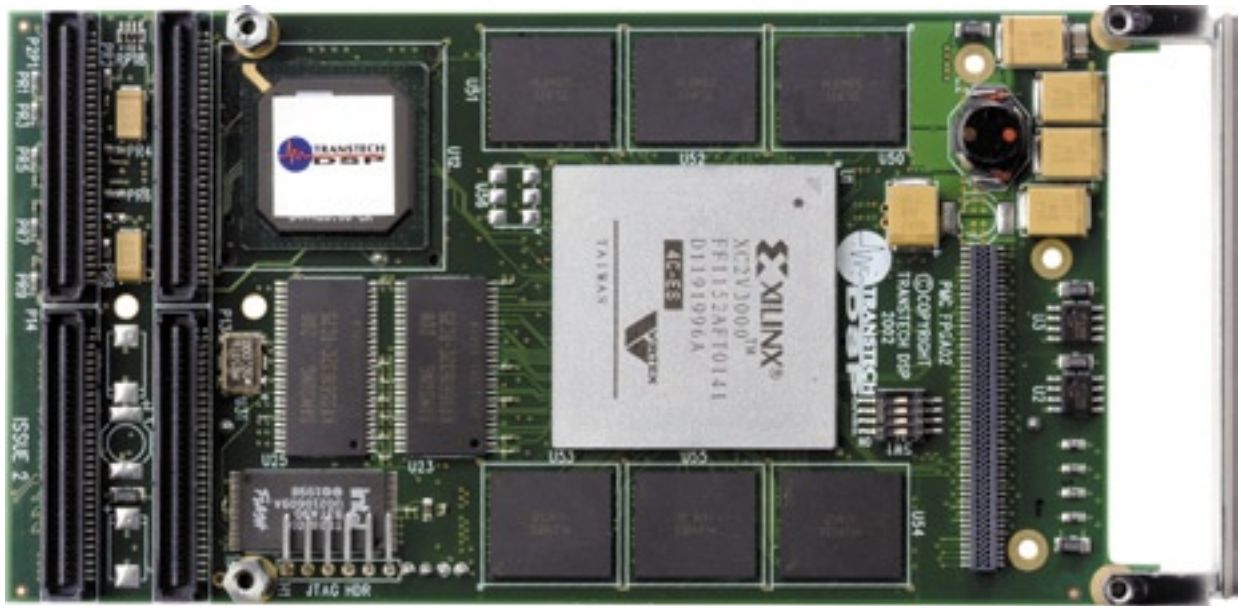
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Find the *Curtiss-Wright / VMETRO / Transtech DSP PMC-FPGA02* at our website: *Click HERE*

PMC-FPGA02

Xilinx Virtex-II FPGA PMC



Features

Xilinx Virtex-II™ FPGA (XC2V3000-XC2V8000)

Header module to provide level translation and external connector

Choice of front panel or user I/O routing

FPDP and channel-link build variants

64-bit/66MHz master/slave PCI interface

128Mbytes SDRAM

6x banks 1Mbytes QDR SRAM

4Mbyte Flash Memory

The PMC-FPGA02 is an FPGA based digital I/O PMC module intended for compute intensive applications. The PMC is fitted with a latest generation Xilinx Virtex-II FPGA and multiple banks of QDR SRAM for increase space for storing local data and maximizing performance.

The PMC-FPGA02 also supports high-speed digital I/O through either the PMC front panel or the user I/O connector for VME or CompactPCI back-panel I/O.

TRANSTECH™ DSP

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Overview

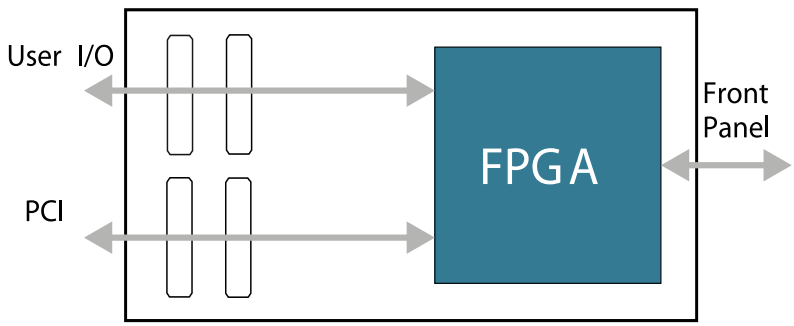
The PMC-FPGA02 is a 64-bit/ 66MHz PMC format high-speed processing module with direct wide-bandwith digital I/O using a Xilinx Virtex-II FPGA. I/O is customizable through a front panel adapter. 128Mbytes of SDRAM and 6Mbytes of QDR (quad data rate) SRAM is provided for local buffering, temporary data storage etc.

Xilinx Virtex-II FPGA

A choice of Xilinx Virtex-II FPGAs are available for the PMC-FPGA02 ranging from XC2V3000 to XC2V8000. A Xilinx XC2V3000 ('-4' speed grade) FPGA is offered as standard.

Digital I/O

The FPGA incorporates direct data ports that can be used for digital I/O schemes such as FPDP, digital camera interfaces, serial ports, custom interfaces and LVDS. Since the FPGA is used to control the bus protocol and timings, the I/O adapter becomes simple, low cost and easy to develop with the minimum of engineering design. Transtech provides module options for FPDP and LVDS. For digital I/O, 69 signals from the FPGA are routed to a header near the front panel. Another 64 FPGA signals are routed to the PMC's user I/O connector. PMC hosts, such as VME boards, can make use of these signals directly with backplane I/O. The FPGA IO signals to the front panel and to the user I/O are separate FPGA data ports and have separate power supplies to allow a choice of operation.

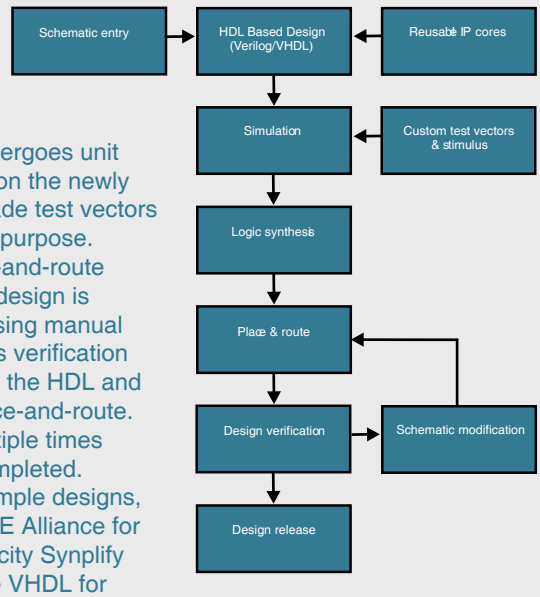


Flexible data I/O options

FPGA Design Flow

Designers typically start with HDL-based design and/or a schematic entry. Reusable IP cores are often selected and added into the design. Following that, the design undergoes unit testing - individual simulation on the newly developed modules. Hand-made test vectors are usually developed for this purpose.

Logic synthesis and place-and-route activities then follow, and the design is programmed for verification using manual test vectors. The results of this verification stage lead to a modification of the HDL and schematic and a return to place-and-route. This cycle can take place multiple times before the design is finally completed. In creating reference and example designs, Transtech have used Xilinx ISE Alliance for placement and routing, Synplicity Synplify for synthesis and Aldec Active VHDL for verification of the designs.



QDR Memory

The PMC-FPGA02 includes six QDR SRAMs of 1Mbyte each. QDR memory has the ability to perform read and write operations simultaneously [see QDR SRAM box]. There are separate read and write busses, both of which clock data on both the rising and falling edge of the clock signal. If QDR memory is clocked at 100MHz, then an aggregate read/write bandwith of 400Mbytes/s is achievable.

PCI Interface

The PMC-FPGA02 features a high-speed (64-bit/66MHz) Initiator/target PCI interface and includes full FPGA to PCI interrupts and DMA. The PCI core interface includes 6 FIFOs, 4 DMA engines, mailbox registers and complex interrupt support. It is fully compliant with the PCI specification revision 2.2. Example VHDL code is provided to allow the developer accelerated access to the built-in resources of the PMC module.

Software Support

FPGA

The Xilinx Virtex-II FPGA is based on SRAM technology and therefore must be reconfigured on each power cycle of the board. Code for the FPGA can be loaded in two ways: from an external host or from the local ash memory.

To allow the FPGA to be configured by a host, Transtech supplies loader utilities for VxWorks and Windows hosts (contact Transtech for the availability of other hosts including linux). This enables developers to use their standard tools [see sidebar on "FPGA design ow"] then to transfer the application to the PMC-FPGA02 easily and quickly. Multiple test points are accessible to logic probes, assisting the user in debugging their FPGA based application.

Once the application has been finalised, it can be programmed into

ash so that on a system power-up, the FPGA is automatically configured without the need of the host. A host based ash programming utility is provided to facilitate this step.

Host Tools

Software development is supported using the most common compilers for the operating system platform. This is Microsoft Visual C++ for Microsoft platforms and the GNU compiler for VxWorks, Linux, Solaris, LynxOS etc. The BSP library provides integration support for using the PMC-FPGA02 from within a host application. It is a C++ library supporting general hardware access and the implementation of high-speed DMA routines. Full source code for the libraries is included with the release. Example programs using these library routines are included to perform such tasks as setting up various DMAs to and from the board, including 'continuous mode' DMAs, using the QDR SRAM and how the board handles interrupts.

The host services provided by the libraries usually require the support of an operating system dependent device driver. Drivers for Windows NT4/2000 and VxWorks operating systems are currently supported.

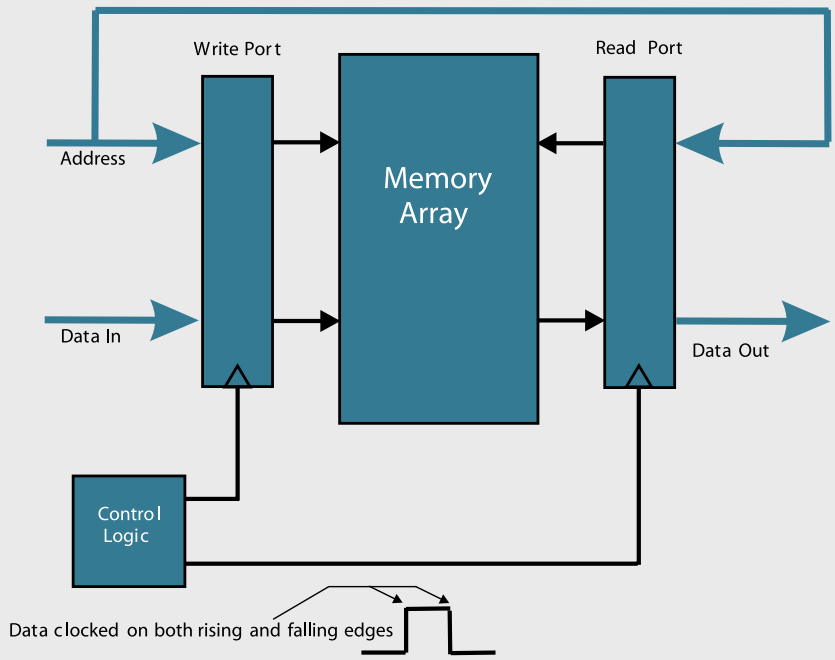
Host utilities are provided to give the user a graphical user interface with a complete view of the board hardware (registers, memory etc.). Other utilities allow for system evaluation and functional testing, as well as configuring the FPGA from the host and loading the ash.

Programming the FPGA

The configuration file for the FPGA can be loaded directly from the host computer's file system across the PCI bus interface using the loader utility or as part of a host application.

The configuration file can be loaded into the ash using the host based programming utility. If the auto-configuration switch is set, the FPGA will load from the ash on power up.

QDR SRAM



Quad Data Rate SRAM has separate, simultaneously operating inputs and outputs. Each data bus operates on two words of data per clock cycle, so that four bus-widths of data are operated on per clock cycle: i.e. 2 reads and 2 writes per clock cycle. 2-word burst QDR SRAM (the type used on the PMC-FPGA02) can indefinitely sustain both a 2-word READ and a 2-word WRITE each clock cycle.

This extremely fast memory can be used in the same manner as standard SRAM or like a FIFO. It is ideal for storing intermediate data created by algorithms running on the FPGA

FPGA Toolset Utilities

bview provides a complete display of the installed PMC-FPGA02 hardware. It is able to show all Xilinx registers, all interface registers as well as Flash and SDRAM memory. It is suitable for detailed debugging and system examination.

bviewd is a remote monitor for non-Microsoft platforms such as Windriver's VxWorks.

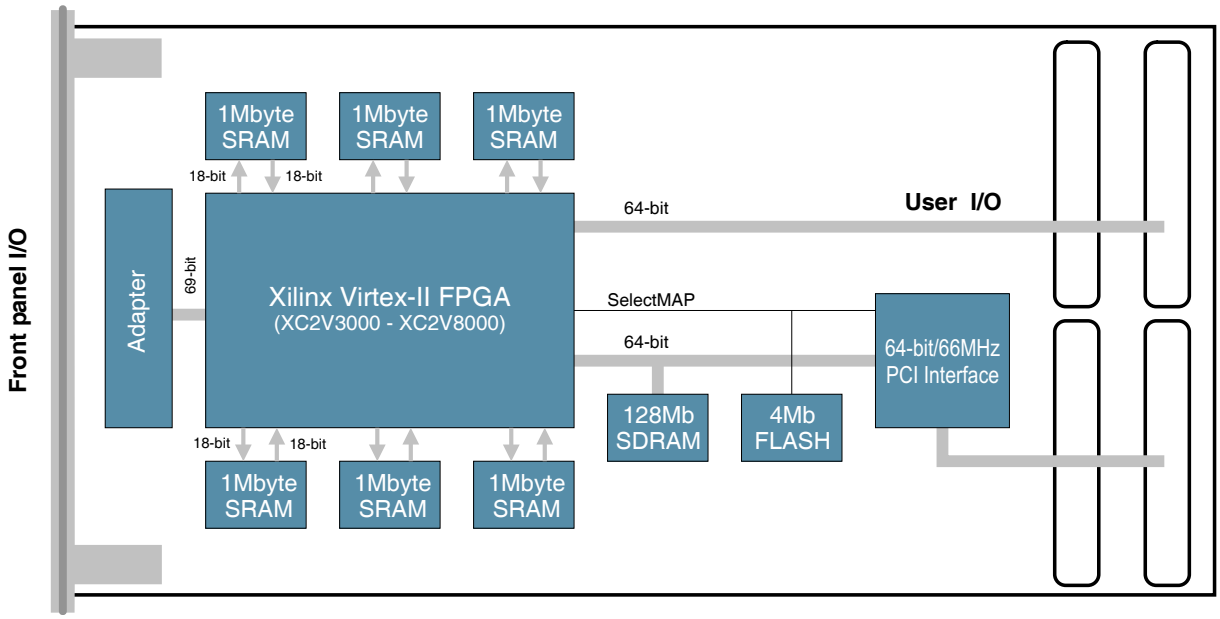
pfcfg allows data files to be copied into the FLASH memory of any Transtech PMC-FPGA product. Up to 15 separate files to be loaded into FLASH, the data of which can be retreived by name from a host program or by address from the FPGA.

pfprobe is a general purpose system status evaluation tool. Normally, it probes the system bus for all Transtech PMC-FPGA boards. For each card found, it is able to:

- Display board information.
- Perform a complete functional test of the board.
- Assess the PCI data transfer bandwidth of the board.

pfreset Software reset a PMC-FPGA board

Block Diagram



Technical Specification

FPGA

Device	Xilinx Virtex XC2V3000 to XC2V8000 (speed grade '-4' default, but can take '5' and '-6' parts)
Package	FF1152

Memory

SDRAM	128Mbytes
SRAM	6x 1Mbytes (QDR)
FLASH	4Mbytes FPGA boot/configuration Programmable via PMC/PCI interface

PCI

Device	QL5064
Compliance	32/64-bit PCI 2.2 33/66MHz 3.3/5V tolerant Master/slave/DMA
Enhancements	DMA, interrupt support
Bandwidth	>500Mbytes/sec

Input/Output

Front Panel	header behind front panel (69-bit data plus power)
User I/O	64-bit data

I/O Adaptor Modules

FPDP	50-way IDC header Transmit Master and Receive Master
Channel Link	40-way Honda connector 2x ports
LVDS	68-way SCSI-III style connector up to 28 I/O pairs outputs

Environmental

Standard	TBA
Rugged	TBA
Conduction Cooled	TBA

Software Support

Toolschain	Synopsis Synplicity and Xilinx Foundation
Utilities	Flash and FPGA programming (VxWorks and Windows NT/2000)
Example code	FPDP, DMA, interrupt handling

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