ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

**Artisan Technology Group**
(217) 352-9330 | sales@artisantg.com | artisantg.com

**Full-service, independent repair center**
with experienced engineers and technicians on staff.

**We buy your excess, underutilized, and idle equipment**
along with credit for buybacks and trade-ins.

**Custom engineering**
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

**Expert team | Trust guarantee | 100% satisfaction**

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Curtiss-Wright / VMETRO / Transtech DSP VPF1* at our website: *Click HERE*







Data Sheet

# VPF1

## Dual PowerPC/Xilinx® Virtex®-II Pro Processing Engine



### Applications

- RADAR
- SONAR
- Electronic warfare / Signal Intelligence (SIGINT)/ Surveillance
- Real-time imaging / Inspection / Machine vision
- Medical imaging

### Features

- FPGA and PowerPC™ based processing
- Dual Xilinx Virtex-II Pro XC2VP70 FPGAs
- Dual 744x PowerPC processors
- 8x Serial I/O links operating up to 3.125Gbps
- 6U VXS/VITA 41 form factor
- Air or conduction cooled rugged versions

### Benefits

- Balance of performance with ease of programming
- Powerful and sophisticated PowerPC processing power
- FPGA options for optimal DSP or logic-centric designs with high-bandwidth communications
- Industry standard form factors
- For use in deployed or commercial environments

### Overview

The VPF1 is a modular signal and data processing engine that couples the power of the latest generation PowerPC CPUs, large Xilinx FPGAs and high-bandwidth multi-channel serial communication fabric to create a balanced and scalable compute platform.

Architecturally, the VPF1 consists of four processor nodes; two nodes are based on the PowerPC 744x CPU and two nodes are based on the Xilinx Virtex-II Pro FPGA. All processor nodes have a fully distributed memory structure with multiple inter-node communications channels. The communications fabric interconnects boards together as well as local processor elements for a scalable solution. The board is VXS compliant and able to handle Gbps backplane communications. The VPF1 can also be provided in a- VME64x format, which is supplied without a VXS connector, as a factory build option.

### FPGA Nodes

#### *Xilinx Virtex-II Pro FPGA*

The board's FPGA nodes use Xilinx Virtex-II Pro XC2VP70 devices as standard, though other devices may be fitted: contact Curtiss-Wright for details. Each node features:

- Eight 2.0/3.125Gbps SERDES transceiver pairs
- Four banks of 2M x 18-bit QDR SRAM
- Two banks of 64Mbytes DDR SDRAM
- JTAG port

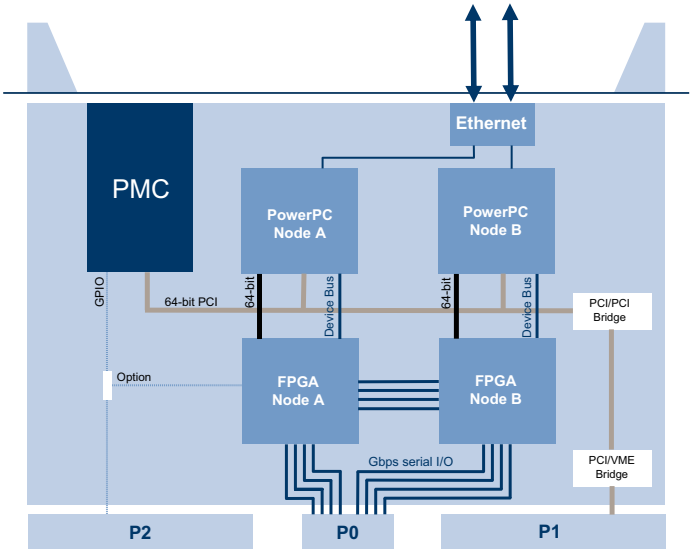
**Learn More**
**Web / sales.cwcembedded.com**
**Email / sales@curtisswright.com**

CURTISS WRIGHT Controls
Embedded Computing

Innovation In Motion.
cwcembedded.com



Figure 1: Architectural Overview




### *Gigabit Communication Channels*

The Virtex-II Pro FPGAs feature serial communications, via RocketIO™ transceivers, able to operate up to 3.125Gbps. The transceivers provide fast data links between VXS boards and between the board's local FPGAs: four RocketIO channels connect the two FPGA nodes and four channels from each FPGA are available for off-board (VXS) communications. Each RocketIO channel has separate LVDS pairs for receive and transmit signals. Groups of RocketIOs (from a single device) can be 'bonded' together to synthesize fewer, but higher bandwidth data links if required. The serial communication bit rate is determined by a very low jitter reference oscillator, and is specified at the time of ordering.

### *PCI Express®, Serial RapidIO® & Beyond*

The board's high-speed serial communications are compatible with standards and specifications based on VITA 41.x (VXS) to support switch packet interfaces. The serial channels are electrically compliant with PCI Express (PCIe), Serial RapidIO (sRIO) and other serial interfaces. Implementing these protocols requires suitable IP cores. The serial communications can also be used without protocols for stripped down, more efficient systems.

### *QDR Memory Banks*

Each FPGA node includes four banks of 2Mx 18-bit QDR SRAM with read or write bandwidths of up to 500Mbytes/s. As read and write transfers can take place concurrently, a total bandwidth of 1Gbyte/s is available per device.

The QDR SRAM memory devices are directly linked to and controlled by the FPGAs. This means that each QDR memory bank can be utilized to implement FIFO (or delay memory), linear addressable memory pool, bit-reversed addressing or circular buffer as best suits the application. Fast banks of SRAM are ideal for lookup tables, local data buffers and DSP operations such as concurrent (MAC) Multiply-Accumulate data streams.

### *SDRAM Memory Banks*

Bulk data storage for the FPGA nodes is provided through the dual 64Mbyte SDRAM banks. These can be used to store large data-sets such as image frames for medical imaging or temporal processing. Dual memory banks are also useful for decoupling I/O data streams allowing data to be processed more easily while the other bank is filling up.

### *FPGA Configuration*

The configuration file for each FPGA node is stored in the FLASH memory of the adjacent PowerPC node. Curtiss-Wright supplies tools for programming the FPGA in both development and run-time environments. JTAG connectivity can also be used for FPGA development using Xilinx's optional ChipScope™ FPGA logic analyzer. An optional battery is available so that encrypted keys can be stored for secure FPGA configurations.

### PowerPC Processor Nodes

A VPF1 includes two PowerPC 744x subsystems complete with SDRAM, FLASH, Ethernet, serial I/O ports, PCI interfaces and operating system support. Each PowerPC 744x node is available with 256Mbytes of DDR SDRAM with ECC and is coupled via a MV64360 bridge and 64Mbytes FLASH memory. The SDRAM is implemented with 72-bit data paths and clocked at 125MHz.



Figure 2: PMC User I/O to P2

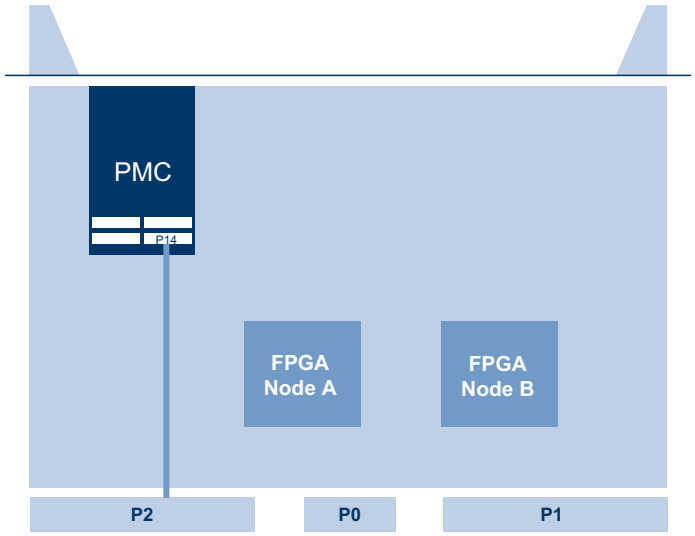



Figure 3: FPGA Parallel I/O to P2

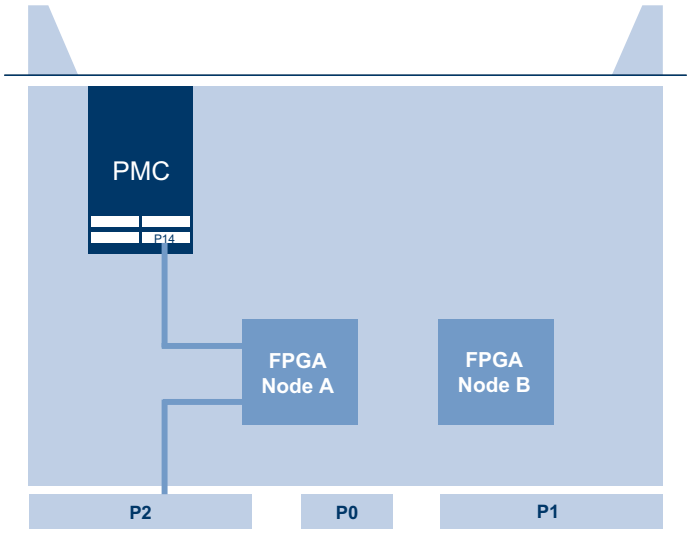
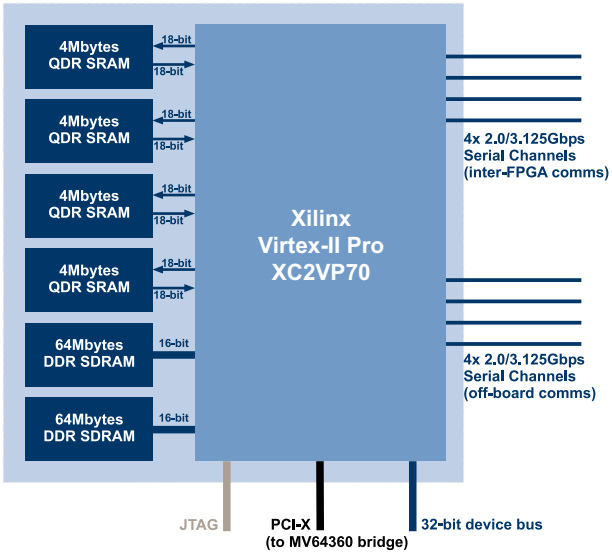



Figure 4: FPGA Processing Node




### *Ethernet*

Two off-board 100/1000Mbit auto-negotiation Ethernet interfaces are provided, one from each PowerPC processor node, connected via the front panel 1000BASE-T RJ45 connectors. An Ethernet connection between the two PowerPC nodes is also provided. Alternatively, Ethernet can be routed to the VME P2 connector.

### *RS422 (EIA-422) & RS232 (EIA-232) Interfaces*

One RS422 interface with RTS/CTS handshaking and one RS232 port are provided per PowerPC node. These ports are routed to the VME P2 connector. Both ports are available for user applications and either can be used for a serial console as required by VxWorks for boot configuration.

### *Watchdog Timer, Temperature Sensors & Power Monitors*

A hardware watchdog timer is provided and can be used to cause the board to reset and/or activate an interrupt if the watchdog is not serviced within a pre-defined period due to application failure. Accessible via the PowerPC processor, the board includes sensors to monitor the temperature of the board and monitor the local supply voltages.

### *JTAG Interface*

The board features multiple, independent JTAG chains via Firecron JTS01/JTS06 controllers, accessible via both on-board JTAG headers and the VME P2 connector. These connections also provide connectivity for the COP (PowerPC) and ChipScope/Agilent trace ports (FPGA) ports. The separate JTAG chains permit the board to undergo dynamic diagnostic during normal application run-time.



Figure 5: A fully connected VXS card system including a switch card which defines the data link routing

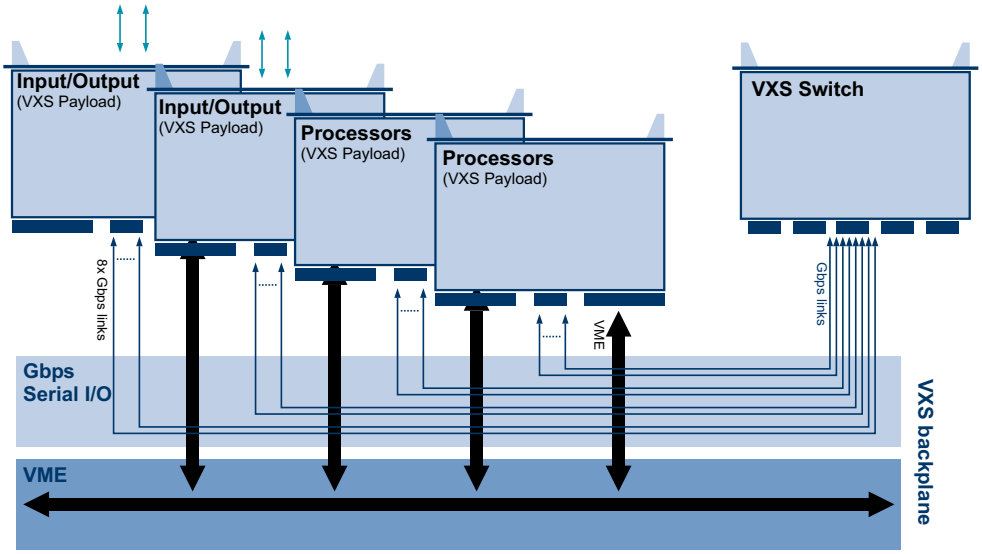
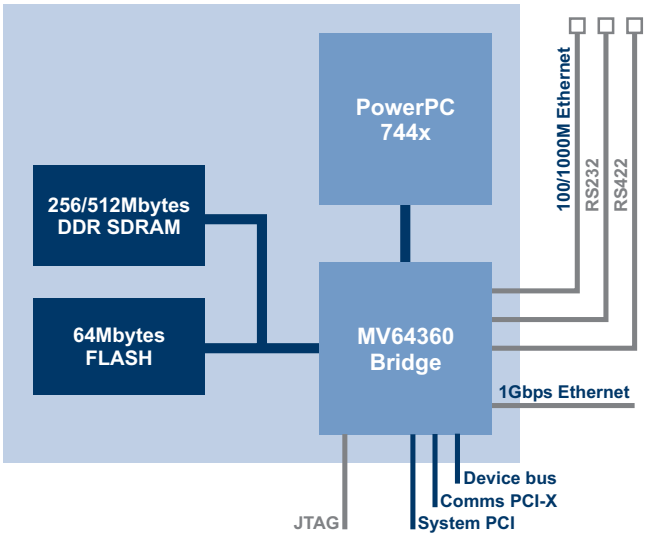



Figure 6: PowerPC Processor Node




## Input/Output

### *PMC Site & FPGA Parallel I/O*

The usual I/O data stream will be via the high-speed Gbps serial interfaces. However, the board also provides a 64-bit/66MHz PMC for local I/O such as analog I/O or frame grabbers. The PMC site has a PMC user I/O connector routed to the VME P2 connector (build option) for backplane communications.

As an alternative to PMC based backplane I/O, the VPF1 can use PMC user I/O (P14) to FPGA plus FPGA to VME P2 (rows a & c) I/O routing, which is useful for implementing custom interfaces such as LVDS. Whether these pins are PMC user I/O to VME P2 or direct FPGA connections is defined through a range of build options.

### *VXS & High-Speed Serial Communications*

Each board has eight, off-board, multi-Gbps transceivers, each of which can be used to establish a point-to-point data link. These links can be wired to create a wide range of topologies to best suit the application, such as pipelines of arrays, to smoothly scale the system.

In order to achieve the Gigabit speed data links, the board uses a MultiGig (RT2) type connector with balanced differential signal routing and ground planes. This connector (as outlined in the VITA 41/VXS specification) is not compatible with the standard VME P0 connector. VXS backplanes are based on the VME64x bus backplane with an alternative P0 connector designed to support Gbps differential serial communications.



Figure 7: P2 Breakout Module




The VITA 41/VXS specification defines a standard P0 pin-out for the payload cards that is fabric independent. Sub-VXS specifications define support for serial interconnects such as Aurora, PCIe, sRIO, etc. In addition to the payload cards, the VITA 41/VXS specification provides for switch cards to control the routing of data links. For VXS backplanes that support this feature, a special switch slot is set aside in the backplane.

### *Software & HDL Support*

The VPF1 lends itself to different applications and markets. These demands require that the board is available with different layers of software support. For system critical applications, Built-In-Test (BIT) provides a power up and run-time system diagnostic. To make application development easier, I/O board drivers and optimized libraries are available. The operating systems supported are VxWorks and Linux.

### *TransComm™*

TransComm is an optional communications toolbox for use with the VPF1 and other PowerPC and FPGA based products and is supplied as a set of software & firmware components and utilities.

This includes a communications harness for PowerPC to PowerPC, FPGA to FPGA and FPGA to PowerPC communications for high-performance, low latency communications anywhere around the TransComm network - even across bridges. This simplifies the ability to build and scale systems and allows developers to focus on their code development and not worry about the infrastructure. TransComm also allows developers to integrate their own IP within the fabric through the use of simple but well defined interfaces.

### *Power-On Self Test (POST)*

The board architecture includes two PowerPC CPU nodes each with a host bridge incorporating the system memory and FLASH memory controllers, Ethernet controller and bus interfaces. The correct operation of this hardware is critical to the functioning of an operating system (OS) on the board, so each board performs certain POST functions to check that this hardware is in a sound state to facilitate booting an operating system. Checks include:

*Memory* - checks that the expected amount of memory is available and that all control/address/data lines between the memory controller and memory are intact. Interrupts - confirms that the interrupt connection between the host bridge and the CPU functions correctly.

*Ethernet* - checks the connectivity between the Ethernet Media Access Controller (MAC) in the host bridge device, and the Ethernet Physical Layer Device (PHY).

POST tests run automatically at power on and output reports to the console serial port. Upon passing all the tests, the operating system will be booted. In the unlikely event that one or more tests fail, the system will halt. This behavior may be overridden to force operating system boot regardless of test status.

### *BIT*

Comprehensive testing of the remainder of the system can be carried out using run-time BIT functions, which run in the OS environment of the board. The BIT system consists of two components: an API and a test specification language. The API allows a BIT script to be run on the hardware. The test specification language provides a precise description of one or more BIT tests for the script.

The specification language contains a series of BIT blocks (see BIT table). Each block may be run either sequentially or in parallel. In a sequential block, each BIT test is run in the order listed. All tests in a parallel block are started at the same time and rely on the OS thread scheduler to allocate time on the processor.



## Table 1: BIT Specifications

| Test | Description |
|---|---|
| DDR Byte Write | Confirms that byte writes to the DDR memory attached to the FPGA are functional |
| DDR Refresh | Confirms that the DDR memory attached to the FPGA is being properly refreshed |
| DDR/QDR Data Generator/ Checker | Confirms that the data checkers and generators in the FPGA memory interface correctly generate & check their defined test data patterns |
| DDR/QDR DMA | Confirms that the FPGA can reliably transfer test data to and from an attached memory device |
| DDR/QDR Independence | Confirms individual memory devices may be accessed without interfering with each other |
| DDR/QDR Size | Confirms that the expected amount of memory is connected to the FPGA and available for use |
| Error Reporter | Generates errors to validate the error reporting system |
| FLASH | Confirms that the flash can be read |
| FRAM | Confirms that a defined region of FRAM memory is writable and readable |
| JTAG Controller | Confirms that the controller is accessible from the host |
| Marvell Integrity Monitor | Hooks all the Marvell integrity interrupts (e.g. bus parity errors) and redirects them into the BIT test report |
| Network Error Monitor | Monitors for transmit and receive errors on a specified Ethernet interface |
| Network Load | Connects a client to a specified server, and sends a specified count of packets of given size |
| Network Load Server | Starts a server on a specified interface, waits (with time-out) for a client connection and sinks any data received |
| PCI Bus Master Abort | Confirms that the bridge chip receives a master abort for invalid PCI cycles |
| PCI-X DMA Checker | Confirms that the data checkers and generators in the FPGA's PCI-X interface correctly generate and check their defined test data patterns |
| PCI-X DMA Input/ Output | Confirms that the bridge can reliably transfer test data between the FPGA & PowerPC SDRAM over the PCI-X bus |
| Xilinx Register | Confirms that the FPGA generates the correct 'bus ready' signal on the register bus |
| Xilinx Register Bus Parity | Confirms that the bridge chip receives correct parity on the FPGA device bus |

| Test | Description |
|---|---|
| POST Results | Evaluate the results of POST tests run before the OS booted |
| Power Dissipation | Defines the level of power dissipated by the test HDL's power block |
| QDR DCM Sweep | Sweep the QDR Digital Clock Manager over its full phase shift range |
| QDR Parity | Confirms that parity error detection for the QDR memory is operational |
| Real Time Clock | Confirms that the RTC is incrementing |
| RocketIO Data Checker | Confirms that the data checkers and generators in the FPGA RocketIO interface correctly, generate & check their defined test data patterns |
| RocketIO Data Transfer | Confirms that the FPGA can reliably send data through a specified RocketIO link |
| Simple Worker | Provides a variable CPU load, so that the BIT control system can be validated |
| Synchronous QDR | Confirms that the FPGA can simultaneously transfer test data reliably to/from all QDR memory devices |
| System Clock | Confirms that all system clocks are running at the correct frequency |
| System Voltage | Confirms that the boards power supply rails are within range |
| Temperature Alarm | Confirms that the temperature sensors correctly detect defined alarm conditions |
| Temperature Monitor | Periodically prints out board temperatures |
| Voltage Monitor | Periodically prints out board voltages |
| Watchdog Alarm | Confirms that the watchdog can be enabled and serviced |
| Xilinx Configuration | Confirms that the FPGA can be unconfigured and that the test HDL can then be configured into the device |
| Xilinx Integrity Monitor | Hooks all the Xilinx integrity interrupts (e.g. QDR parity errors) and redirects them into the BIT test report |
| Xilinx Interrupt | Confirms that the FPGA is able to generate interrupts to the bridge chip |
| Xilinx Register | Confirms that the FPGA generates the correct 'bus ready' signal on the register bus |
| Xilinx Register Bus Parity | Confirms that the bridge chip receives correct parity on the FPGA device bus |



### *BSP Software*

To support development, Curtiss-Wright supplies a comprehensive system of BSP software. The major components include user libraries, kernel libraries and utilities.

### *User Libraries*

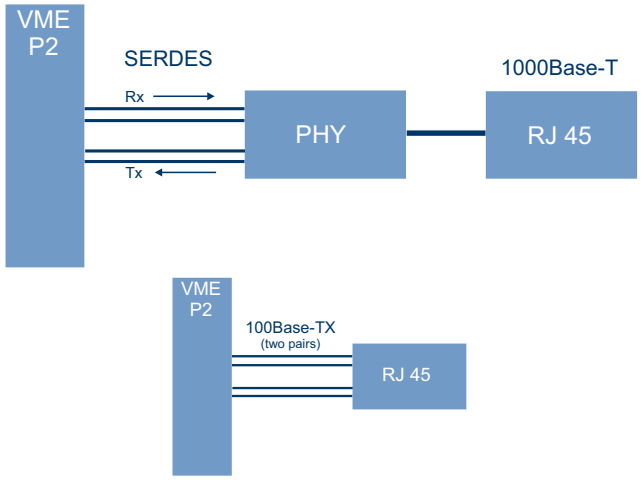
The user libraries are designed to support general hardware access and high-speed DMA transfers. These C++ libraries are source compatible across all supported operating systems. The services provided by the API fall into these broad categories:

- Accessing Remote Nodes
- Allocating DMA Buffers
- Board Initialization
- Bridge Chip SRAM
- Built In Test
- Configuring the FPGA
- DMA Driven I/O
- FLASH Memory
- FRAM Memory
- Hardware Semaphores
- Interrupt Handling
- Persistent Environment Variables
- User Reserved Memory
- Voltage and Temperature Sensors
- Watchdog Timer

### *Kernel Libraries*

The kernel level library includes low level routines required by the VxWorks/Linux kernel in order to run on the VPF1 plus a suite of device drivers which enable the kernel and user applications to exploit all available board hardware. The driver suite is divided into two parts: standard (WindRiver/Linux and Marvell) device drivers and Curtiss-Wright board specific drivers. The low level access to operating system functionality means these library functions are not portable between supported operating systems. Most Curtiss-Wright library routines return an error code. Macros are provided to manipulate these error codes, aiding in application debugging.

Figure 8: P2 Breakout Module




### *Utilities*

### *Board Viewer Tool: BView*

Provides snapshot access to all of the registers (including user defined FPGA registers) and most of the memory on VPF1. BView is a client/server program, with a graphical user interface (GUI) running on a Windows 2000/XP machine and a monitor daemon running on the VPF1 card.

### *Xilinx Configuration Utility*

Configures the FPGA either from a host file or from data already stored in the node's FLASH memory.

### *Card Environment Access Utility*

Provides access to the system and user environment variables stored in a node's FLASH memory. System environment variables describe a card's build properties (e.g. clock speeds, amount of memory fitted, etc.), while user environment variables can be used for any application purpose.

### *FLASH Viewing & Programming Utility*

Allows the user to reserve regions of FLASH to be programmed with application data, including bootable kernels, FPGA configuration data and BIT scripts.

The BSP includes a number of example programs showing how to use the APIs for numerous essential tasks such as



setting up DMAs, handling interrupts, running BIT, setting up a watchdog, etc. It is Curtiss-Wright policy to release source code for libraries and utilities wherever possible.

## Hardware Development Logic Support

In a number of instances, the services provided by the BSP are dependent on the functionality of the Hardware Development Logic (HDL) configured into the FPGA. In order to ensure compatibility between user defined HDL and the BSP, Curtiss-Wright supplies a number of standardized HDL interface components and recommend that a set of "standard" registers are implemented in the FPGA by users. A "features" register defines which elements are actually implemented. The HDL library components include:

### *Functional interface components*

- DDR SDRAM interfaces
- Device bus interface
- ICS8442 programming interface
- PCI-X interface
- QDR SRAM interface

### *Simulation model components*

- DDR SDRAM simulation model
- MV64360 bridge simulation model
- QDR SRAM simulation model

### *Other library files*

- Component definitions for all library components
- Constants and types definitions
- ModelSim Macro file for library compilation
- ModelSim project file
- Text file revision history of the library files section
- Utilities used by the MV64360 simulation

## VPF1 P2 Breakout Module

The majority of the board's input/output is available via the backplane. System I/O is routed to the VME P2 connector while the high-speed serial I/O is routed to a VXS P0 connector. To access the VME P2 based system I/O, an optional Curtiss-Wright breakout module is available. For conduction-cooled variants, the application backplane can incorporate these signals directly for a more robust configuration.

### *RS232 (EIA-232)*

PowerPC processors A and B each have access to RS232 serial port I/O through the breakout module. The connectors are male (plug) right angle 9-way 'D' subminiature.

### *RS422 (EIA-422)*

A single header breaks out RS422 from both PowerPC processors. The signal pairs are connected to MAX3074EE (or equivalent) buffers on the board and terminated with 100Ω resistors. The signals are DC coupled.

### *Ethernet*

The Ethernet connection from each PowerPC node can be routed to VME P2 rather than the front panel. Each Ethernet link may be individually configured as either SERDES or raw 100Base-TX signaling as a build option, so the P2 breakout module needs to be ordered to match the VPF1 build.

### *Mechanical Outline*

The P2 breakout module is designed to fit a standard VME rear card guide and complies with IEEE 1101.11-1998 specification for rear plug-in units.

### *SERDES to Copper*

When the board is built with SERDES connections to P2 (the default build), the breakout module can be used to convert these signals to Gigabit Ethernet (1000Base-T), using the module's own PHY devices (Marvell 88E1011S), which will auto-negotiate only for Gigabit operation. The RJ45 connectors include the necessary magnetics.

### *100Base-TX*

When the board is built with raw 100Base-Tx Ethernet to P2, the breakout module can be used to route the signals to an RJ45 connector, which includes the necessary magnetics. The PHY on the main board is the source of the 100Base-TX signals and it will auto-negotiate, but will not support Gigabit Ethernet.



### *JTAG*

Two connectors on the breakout module provide access to JTAG boundary scan signals. P3 provides JTAG access to the module's PHY devices. P7 provides access to VPF1 JTAG signals routed to VME P2. Both connectors are 14-way 0.1" pitch shrouded headers.

### VPF1 Debug Module

The VPF1 connects all debug signals to a single connector (J15) near the front panel. A debug breakout module is available for customers to access these signals. There are 2 COP port connectors on the debug module: one for each PowerPC. Xilinx FPGA JTAG ports are provided to allow JTAG configuration and ChipScope debugging of the FPGAs.

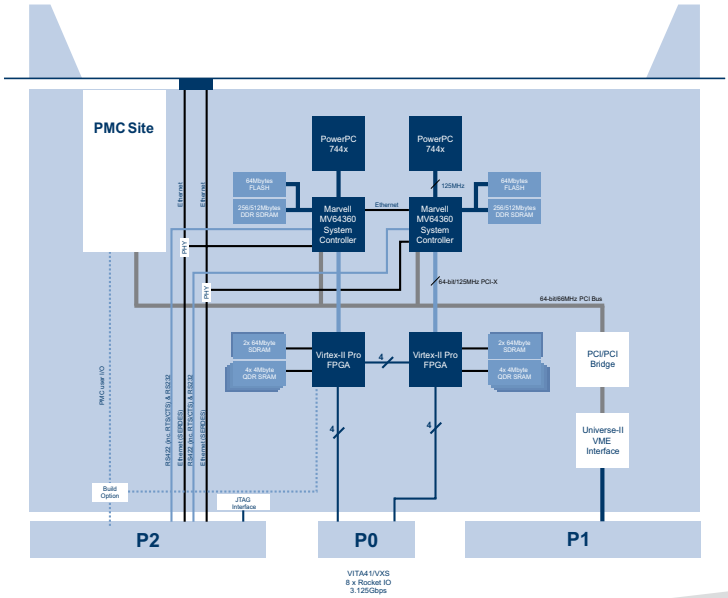
Table 2: Specifications

| | |
|---|---|
| **PowerPC Nodes** | |
| Number | 2 |
| Processor (per node) | PowerPC 7447 1000MHz[1] |
| Bridge (per node) | Marvell MV64360 |
| SDRAM (per node) | 256 or 512Mbytes (future) |
| FLASH (per node) | 64Mbytes |
| Ethernet (per node) | 100/1000 Base-T |
| Serial I/O (per node) | 1x RS-422; 1x RS-232 |
| **FPGA Nodes** | |
| Number | 2 |
| FPGA | XC2VP70 |
| RocketIO | Up to 3.125Gbps (-6 speed grade FPGA) |
| QDR SRAM | 4 banks of 2 or 4Mbytes; 18-bit data paths |
| DDR SDRAM | 128Mbytes (2 banks of 64Mbytes) with ECC |
| **Inter-Node Communications** | |
| FPGA to FPGA | 4x 2.0/3.125Gbps |
| PowerPC to FPGA | 64-bit/125MHz link |
| Other | Shared 64-bit/66MHz PCI (backbone) |

| | |
|---|---|
| **Off-board Communications** | |
| High-Speed Serial | 8x 2.0/3.125Gbps (4 per FPGA node)<br>MultiGig RT2 (VITA 41 style) Connector |
| VME | VME64 (Universe II Bridge) |
| Serial I/O (per node) | 1x RS232, 1x RS422 (with RTS/CTS) |
| Other | Direct FPGA (VME P2) connections (build option) |
| **Debug** | |
| JTAG | Multiple JTAG/COP chains - J15 or VME P2 |
| **PMC** | |
| Sites | 1 |
| User I/O Routing | VME P2 or FPGA node A |
| **Software Support** | |
| Operating Systems (PowerPC) | VxWorks, Linux |
| Diagnostics | POST, BIT |
| Libraries | User, Kernel |
| HDL Code | Interface & Simulation components |

Notes
1. Please consult Curtiss-Wright for 7447A (1,000MHz) and 7448 (1,250MHz) device availability.

Figure 9: VPF1 Block Diagram




### *Ruggedized Versions*

Curtiss-Wright offers ruggedized versions of the VPF1 that are characterized for extended temperature range, shock, vibration, altitude and humidity. These boards are equipped with extra and/or special hardware to improve tolerance against shock and vibration.



Table 3:
Environmental Specifications

| | | Air-cooled | | Conduction-cooled |
|---|---|---|---|---|
| | | Level 1 | Level 2 | Level 4 |
| Part number extension | | - blank - | - blank - | - blank - |
| Temperature | Operational[1] (at sea level) | 0°C to +50°C | -10°C to +65°C | -40°C to +75°C |
| | Non-operational | -40°C to +85°C | -40°C to +85°C | -55°C to +85°C |
| Vibration | Operational (Sinus) | - | - | 10G peak 15-2000Hz |
| | Operational (Random) | - | 0.02 $g^2$/Hz (20-2000Hz) | 0.04 $g^2$/Hz (15-2000Hz) |
| Shock | Operational | - | 30 g peak 11ms half sine | 40 g peak 11ms half sine |
| Humidity | Operational non-condensing | 0-95% non-condensing | 0-95% non-condensing | 0-100% non-condensing |
| Altitude | Operational | 10,000ft | 20,000ft | 70,000ft |
| Conformal Coat | | No | Yes | Yes |

Notes
1. The maximum operating temperature is heavily dependant on the power dissipation of the FPGA devices. Applications with high levels of FPGA utilization may not operate to the maximum ambient temperatures stated.

## Warranty

This product has a one year warranty.

## Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

The information in this document is subject to change without notice and should not be construed as a commitment by Curtiss-Wright Controls Inc., Embedded Computing (CWCEC) group. While reasonable precautions have been taken, CWCEC assumes no responsibility for any errors that may appear in this document. All products shown or mentioned are trademarks or registered trademarks of their respective owners.

© Copyright 2008, Curtiss-Wright Controls, Inc.,
All Rights Reserved. MKT-DS-VPF1-111008v1

**Artisan Technology Group** is an independent supplier of quality pre-owned equipment

## Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

## We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

## Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP