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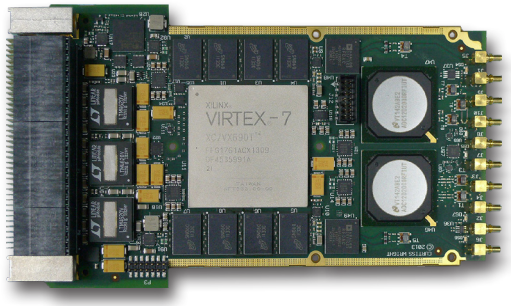
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Find the *Curtiss-Wright VPX3-530* at our website: ***Click HERE***

VPX3-530

High Speed Transceiver with Xilinx® Virtex®-7 FPGA

CURTISSWRIGHTDS.COM



Key Features

- Dual 4 Gsps 12-bit or Quad 2 Gsps 12-bit analog inputs
- Dual 5.6 Gsps 14-bit DAC update rate (maximum 2.8 Gsps data rate)
- Multi-board, multi-channel synchronization
- Xilinx user programmable Virtex-7 VX690T FPGA
- Up to 8 Gbytes DDR3L SDRAM (64-bit data paths)
- 3U OpenVPX compliant
- Onboard power and temperature measurement
- VxWorks and Linux host support
- Air- and Conduction-cooled variants

Applications

- Radar
- SIGINT/ELINT
- Electronic Warfare (EW)

Overview

The VPX3-530 combines multiple channel high-speed ADCs and DACs with a latest generation user programmable Xilinx® Virtex®-7 FPGA in a range of rugged build formats for demanding applications such as SIGINT, radar and Software Defined Radio (SDR).

Analog Input/Output

Up to four analog inputs are supported by the VPX3-530. These analog inputs can be configured as dual 4 Gsps/12-bit using native interleaving of the ADC devices or four 2 Gsps/12-bit channels. Each analog input is AC coupled via baluns for maximum ADC performance.

Complementing the analog inputs are two 5.6 Gsps 14-bit DACs. Each DAC has a maximum data rate of 2.8 Gsps. Outputs above 2.8 Gsps are achieved through data interpolation modes.

Sample rates above 2 Gsps use interleaved ADC modes. For optimal ADC input performance, the VPX3-530 is available in options for up to 2 Gsps ADC or 2 to 4 Gsps configurations. See graphs (Figures 3-6) for performance characteristics for the analog input and outputs.

All analog I/O connectivity is provided through the front panel via rugged SSMC connectors.

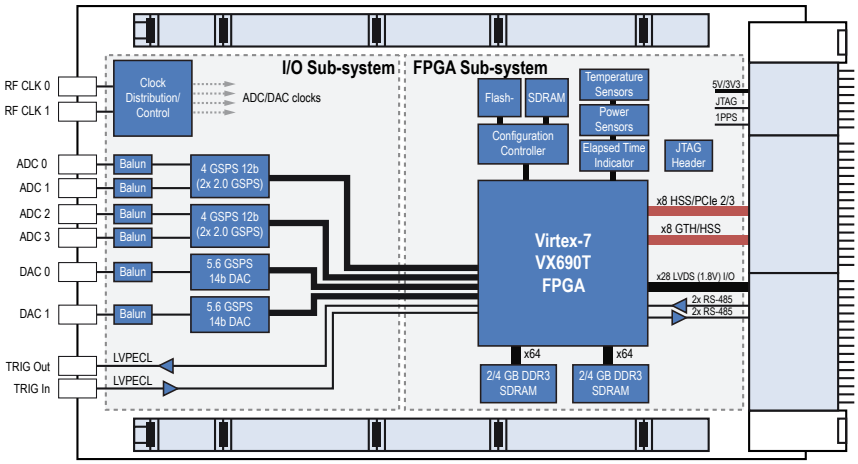


Figure 1: VPX3-530 block diagram

TABLE 1	Analog Input/Output	
	INPUT (see note)	OUTPUT
Number of channels	› 2 (4 Gsps) or › 4 (2 Gsps) › No ADCs fitted (build option)	2 or no DACs fitted (build option)
Sampling frequency	Up to 4 Gsps per channel	› Up to 5.6 Gsps update rate › Up to 2.8 Gsps direct RF synthesis
Full scale Input	Up to 4 dBm adjustable	
Full scale Output		-3 dBm (contact factory for other input ranges)
Analog bandwidth	› Non-DES mode 3dB: 5 MHz to 1500 MHz › Non-DES mode 6dB: <5 MHz to 2100 MHz	
SFDR (typ)	62 dBc @ 498 MHz, 2 Gsps	-65 dBc @ 350 MHz, 2600 Msps
SNR (typ)	54 dBc @ 498 MHz, 2 Gsps	
ENOB (typ)	8.6 bits @ 498 MHz, 2 Gsps	
Sample clock	› Min: 200 MHz › Max: 2000 MHz	› Min: 1400 MHz › Max: 2800 MHz
Input impedance	50 Ohm, AC coupled	
Input connector	Front panel SSMC	
Full power B/W		Baseband 3 dB: 14 MHz to 1550 MHz

Notes: contact factory for alternative sample rates and performance

Specifications Summary

FPGA

- Device: Xilinx Virtex-7 VX690T (speed grade 2), contact factory for alternative FPGA sizes
- Configuration: over PCI Express® (PCIe) interface
  - 1 Gbit flash (FPGA boot/configuration including recovery image)
  - 512 Mbit SDRAM (FPGA volatile configuration)
  - JTAG/ChipScope™ Pro port

Clock Input

- Clock Input sources:
  - Mode 1: RF Clock 0 to all ADC and DACs (RF Clock 1 not used)
  - Mode 2: RF Clock 0 to ADCs, RF Clock 1 to DACs
- Clock Input: 50 Ohm, AC coupled LVPECL
- Trigger Input/Output: Single-ended, 50 Ohm, LVPECL buffered to FPGA
- Clock Input connector: Front panel SSMC

VPX

- OpenVPX profiles
  - MOD3-PAY-1D-16.2.6-2
  - MOD3-PER-1F-16.3.2-2
- VPX P0
  - 5V: 19.8A (max)
  - 3V3_Aux: 0.8A (max)
  - 3V3: not required
  - VBAT: 3V (nom)
  - 12V: not required
  - 1PPS
  - REF_CLK
  - JTAG
- VPX P1
  - 8 x HSS (user defined up to 10.1 Gbps per lane, PCIe 1 or PCIe 2 (contact factory for PCIe Gen 3)
  - 8 x HSS (user defined up to 10.1 Gbps per lane)
- VPX P2
  - 2 x RS-422/485 inputs (FPGA controlled)
  - 2 x RS-422/485 outputs (FPGA controlled)
  - 28 x 1.8V LVDS (FPGA controlled)
- Board pitch
  - Conduction-cooled: 0.85”
  - Air-cooled: 1”

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Memory

- Type: DDR3L SDRAM
- Capacity
  - Total: 4 or 8 Gbytes
  - 2 x 256 M x 64-bit or 2 x 512 M x 64-bit
- Bandwidth: >9.6 GBps (read or write) per bank

Software/HDL

- Support/Utilities
  - FusionXF™ Development Kit
  - FPGA/flash programming, diagnostics
- Host drivers: VxWorks® or Linux® (Fedora™), contact factory for Windows® support
- HDL example: Memory interfaces, PCIe, data DMA, data acquisition, data playback

Miscellaneous

- LED: 2, user controlled via FPGA
- Elapsed Time Indicator (ETI): 0.25 second resolution, maximum accumulated time 34 years
- Power: Card input voltage and current measurement facility
- Weight (typ)
  - Air-cooled: 524g
  - Conduction-cooled: 603g

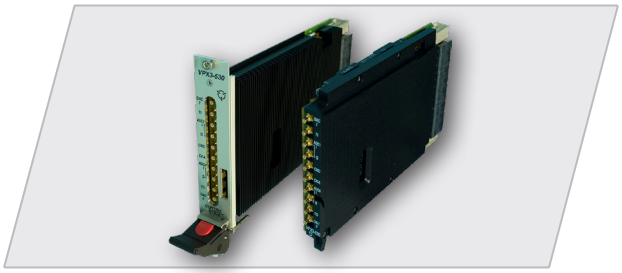


Figure 2: Air and conduction-cooled VPX3-530 variants

Quad Analog Input (non-DES mode)

The VPX3-530 is available with variants supporting up to four analog input channels and implemented using two dual channel ADCs. These ADCs are configured in a mode referred to as “non-DES”. DES is “Dual Edge Sampling” and relates to a mode which interleaves ADCs using alternate edge of the input sample clock. For “non-DES” mode, single-edge input sample clocking is used. Although all analog inputs are independent, the ADCs use a common sample clock.

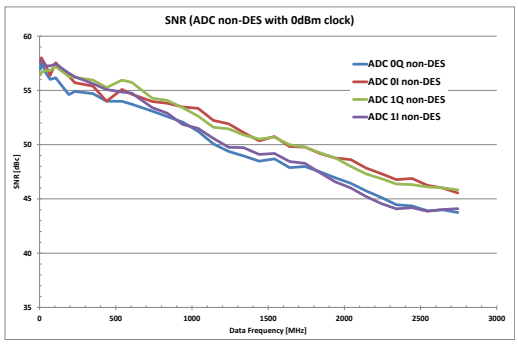


Figure 3: ADC SNR (typ) (non-DES mode)

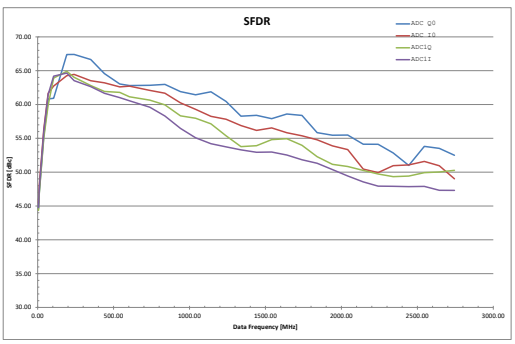


Figure 4: ADC SFDR (typ) (non-DES mode)

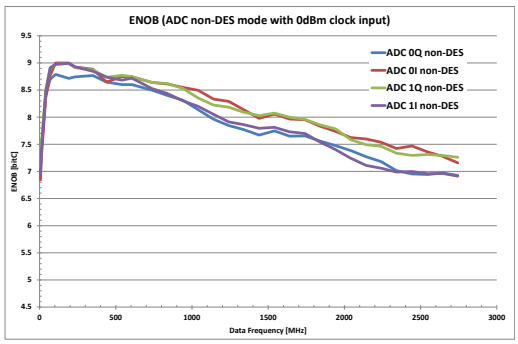


Figure 5: ADC ENOB (typ) (non-DES mode)

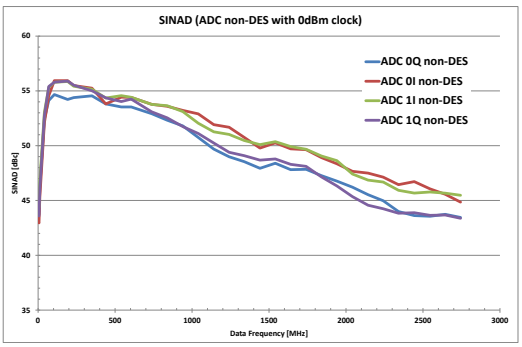


Figure 6: ADC SINAD (typ) (non-DES mode)

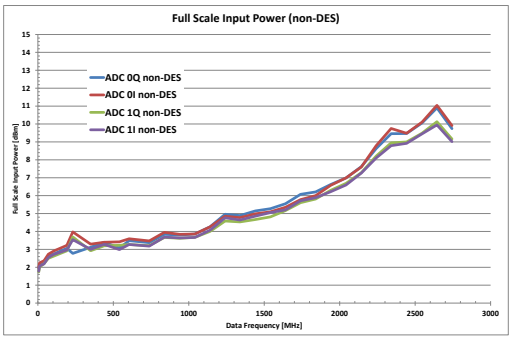


Figure 7: Full scale input power (typ)

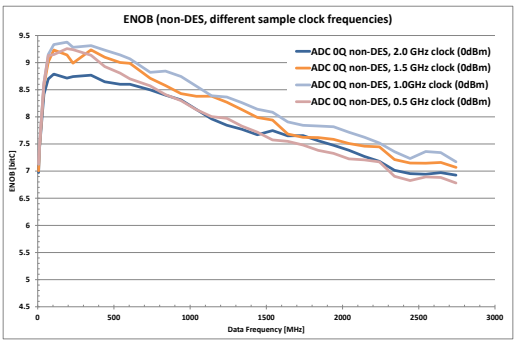


Figure 8: ADC ENOB (typ) vs sample frequency (non-DES mode)

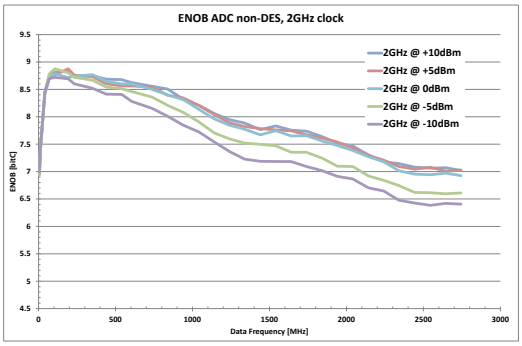


Figure 9: ADC (non-DES) ENOB (typ) vs input clock power

Dual Analog Input (DES mode)

The VPX3-530 can also be provided as dual input analog front end to support up to 4 Gsps per channel. This is achieved using ADC interleaving via its physical I and Q inputs. These modes are referred to as DES modes. The ADC support a number of these modes including analog coupling into one ADC input, which is then split to the other on-chip ADC or coupling the same analog input into both channels as the card input level. Please consult Texas Instruments technical documentation for a detailed discussion on the modes and their relative advantages.

The data below outlines typical measured performance data for DESQ (similar to DESI), in which only a single input per interleaved ADCs is required and DESIQ where the input is driven from two analog inputs (this is usually achieved using an external splitter).

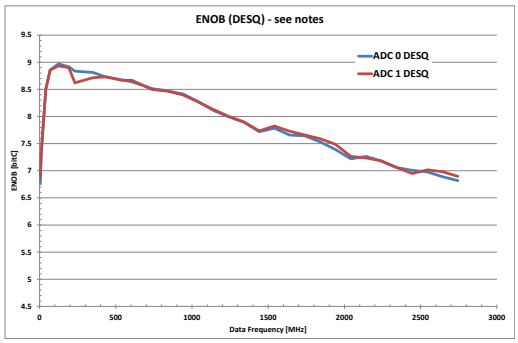


Figure 10: ADC ENOB (typ) (DESQ mode)

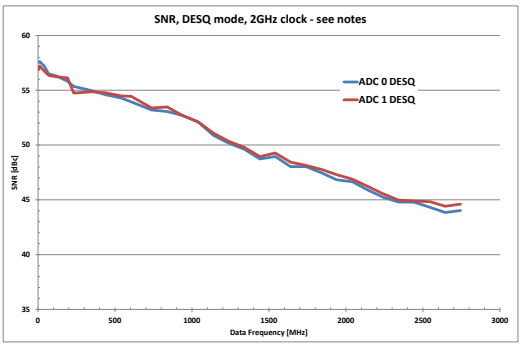


Figure 11: ADC SNR (typ) (DESQ mode)

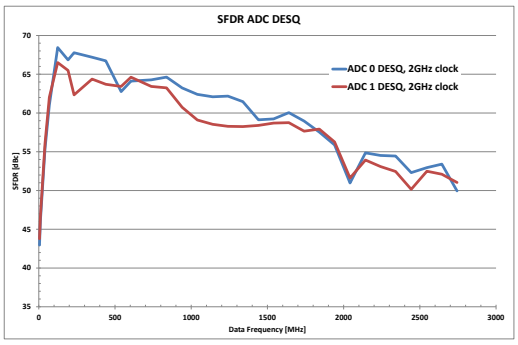


Figure 12: ADC SFDR (typ) (DESQ mode)

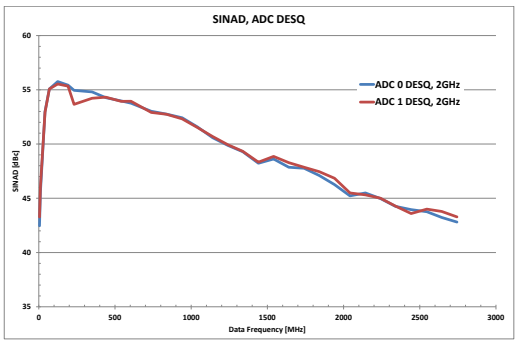


Figure 13: ADC SINAD (typ) (DESQ mode)

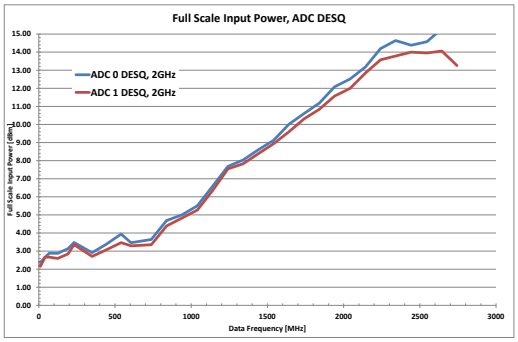


Figure 14: ADC full scale input power (typ) (DESQ mode)

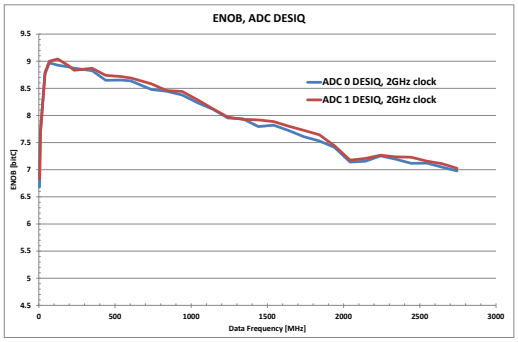


Figure 15: ADC ENOB (typ) (DESIQ mode)

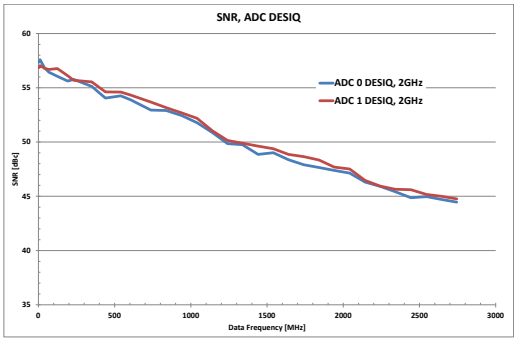


Figure 16: ADC SNR (typ) (DESIQ mode)

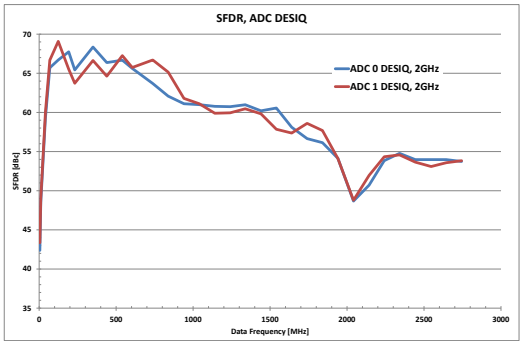


Figure 17: ADC SFDR (typ) (DESIQ mode)

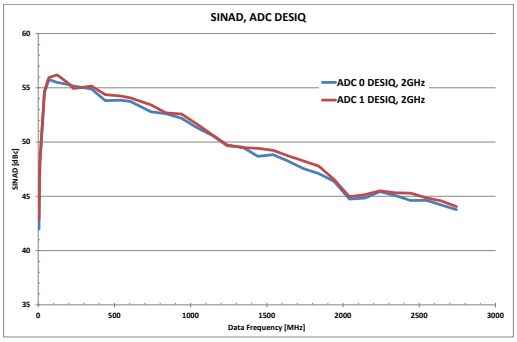


Figure 18: ADC SINAD (typ) (DESIQ mode)

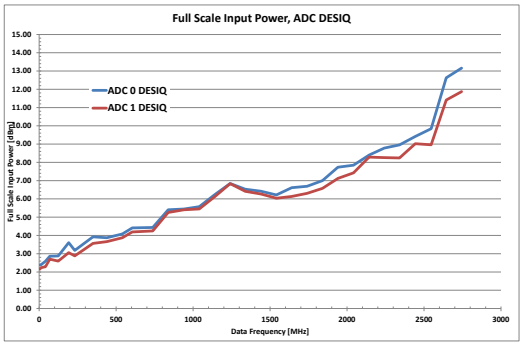


Figure 19: ADC full scale input power (typ) (DESIQ mode)

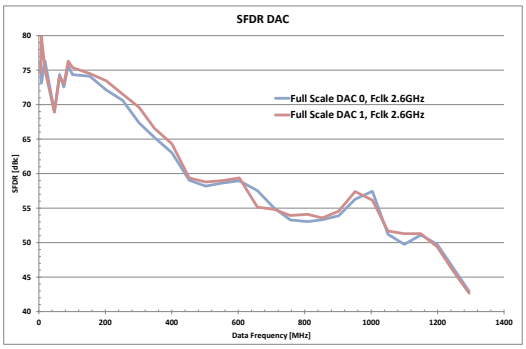


Figure 20: DAC SFDR (typ)

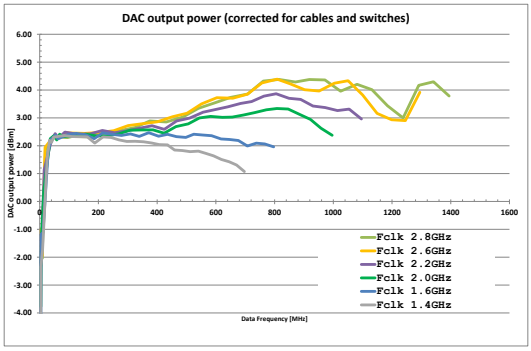


Figure 21: DAC output power (typ)

Notes: The performance characteristics for all DES modes require adjustments at the board level for phase, delay and gain to ensure board ADCs on each dual converter are working in a proper interleaved way. Using the ADCs without adjustment will work, but the performance may typically be affected in the range of 5-10dB. Please consult Texas Instruments' documentation on the part for a full understanding.

Sample Clocks, Triggers and Synchronization

The VPX3-530 provides the choice of two RF sample clock sources through the front panel. Supported modes allow synchronous ADC and DAC data sampling or independent sample clock for the ADCs and DACs. This allows coherent input and output sampling or the ability to operate the ADCs and DACs separately.

The ADC12D2000RF ADCs support multiple modes, but can be separated into interleaved and non-interleaved modes for the two ADCs in each device. In the non-interleaved mode, each ADC is synchronously clocked off the same sample clock edge. For the interleaved mode, Dual Edge Sampling (DES) is used in which one ADC is clocked off rising edge of the sample clock and the other ADC is clocked off the falling edge of the sample clock. The standard build configurations of the VPX3-530 use two dual ADC devices. Since the ADC devices can operate up to 2 Gsps per channel in non-interleaved mode or up to 4 Gsps in DES interleaved mode, the maximum sample clock input frequency is 2 GHz.

The VPX3-530's AD9129 DACs support two general modes: direct baseband update and mixed mode. The direct mode allows data updates of up to 2.8 Gsps with a corresponding output rate and using up to a 2.8 GHz sample clock. Mix mode allows a doubling of DAC output rates of up to 5.6 Gsps though interpolation of the input data and sample clock. It should be noted the minimum DAC sample clock is 1.4 GHz.

Since the clocking modes supported by the ADC and DAC devices, there is a use case where using clocks above 2 GHz would require the ADCs to operate in DES mode, while the DAC operate in single edge clock up to 2.8 GHz i.e. the ADCs will sample at twice the rate that the DAC updates. If this is an issue, the DAC could be programmed to operate in mix mode, thereby ensure common input and out update rates. See diagram below for an overview of the input clock structure.

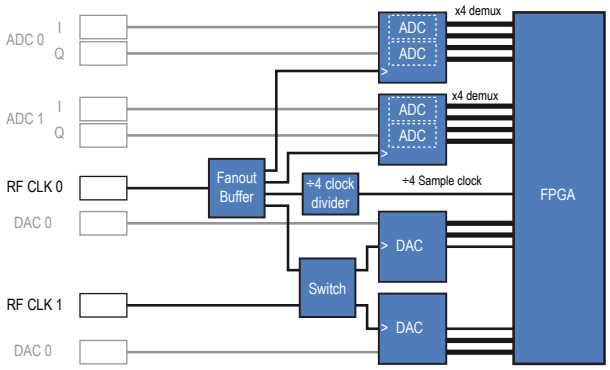


Figure 22: Overview of RF sample clock inputs

The VPX3-530 does not use a local sample clock, but instead an external source for maximum performance.

Trigger inputs and outputs are provided through front panel connectors, though with suitable HDL, backplane based triggers are also possible.

Both 'Trigger In' and 'Trigger Out' are single-ended LVPECL buffered signals connected to the host FPGA. These signals are also used as part of the mechanism to synchronize the ADCs on multiple VPX3-530 cards; effectively the function of these signals is changed to a sync mode when this is required.

Additional signals are unbuffered 1.8V LVDS or RS-485 via the VPX P2 connector. These are available for the user application. A 1PPS signal input is also provided through the VPX P0 connector (user HDL required to implement).

Xilinx Virtex-7 FPGA

The VPX3-530 is built around a user programmable Xilinx Virtex-7 VX690T FPGA resource (speed grade 2). Virtex-7 is a member of Xilinx's 28 nm 7-Series family. The FPGA is supported by high speed DDR3L memory resources directly connected the FPGA.

The FPGA configuration images can be stored in either the flash memory or DDR SDRAM configuration memory and can be updated by the host CPU using the PCIe interface. The DDR SDRAM resource allows configurations to be downloaded from the host and bypass the non-volatile flash. Since SDRAM based configuration is volatile, it is an attractive mode for security sensitive applications and allows the VPX3-530 to be more easily declassified should the need arise.

The FPGA can be reconfigured from any one of a number of images indexed in the flash including a write protected recovery configuration. FPGA configuration from either flash or DDR SDRAM can also take advantage of AES encryption.

Multiple Memory Banks

The VPX3-530 supports two banks of 256 M x 64-bit or 512 M x 64-bit DDR3L SDRAM, each directly connected to the FPGA. As each memory bank is independently connected to the FPGA, there is great flexibility in how they may be used. Each memory bank supports read or write bandwidths of around 9.6 GBps.

Power and Temperature Measurement

The VPX3-530 includes built in power (including current and temperature) measurement capabilities. For rugged applications using high power components like FPGAs, this provides critical feedback on the health of the card and whether recalibration might be recommended.

Elapsed Time Indicator

The VPX3-530 incorporates an Elapsed Time Indicator (ETI). This provides the ability to determine the total accumulated time (up to 34 years) the card has been under power and to support system maintenance plans.

JTAG

A standard 2 mm JTAG header is provided on the VPX3-530. This allows a standard Xilinx JTAG pod to be used for debug.

VPX Connectivity

The VPX3-530 supports OpenVPX profiles for PCIe Gen 1 and 2. Contact factory for PCIe Gen 3 support.

PCIe is supported through direct connectivity to the Xilinx Virtex-7 FPGA which enables up to x8 lane width over the VPX P1 connector. In addition, a second bank of x8 HSS links, again directly connected to the FPGA is provided over the VPX P1 connector. This bank of x8 HSS links is fully user programmable with each link able to operate over 10 Gbps. This is ideal for efficient inter-FPGA communications or to implement I/O ports such as Serial FPDP (sFPDP) or 10/40 GbE. Note: the use of sFPDP or Ethernet protocols requires additional HDL. The x8 PCIe port can also be user defined as the backplane links are directly connected to the FPGA without the use of bridges.

PX P2 connectivity is reserved for the "parallel" I/O ports from the FPGA and configured as differential I/O pairs. Two of the input I/O pairs is buffered using RS-485/422 compliant devices to the FPGA, two further FPGA driven RS-485/422 pairs are outputs to the backplane. The remaining 28 differential VPX P2 I/O are connected directly to the FPGA and can be defined as either inputs or outputs as the application requires.

The VPX3-530 requires +5V and 3V3_Aux power supplies thereby allowing greater system flexibility. +12V and 3V3 power inputs are not required.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF Development Kit includes software, HDL and utilities complete with examples for using the VPX3-530. FusionXF includes a C programming language API, driver framework and sophisticated DMA support. One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively.

Software utilities are provided for configuring the FPGA. These include flash programming and configuring the FPGA from one of many indexed images in flash.

FusionXF supports VxWorks and Linux Fedora operating systems. Additional operating systems, such as Windows, or other distributions of Linux can be considered on request.

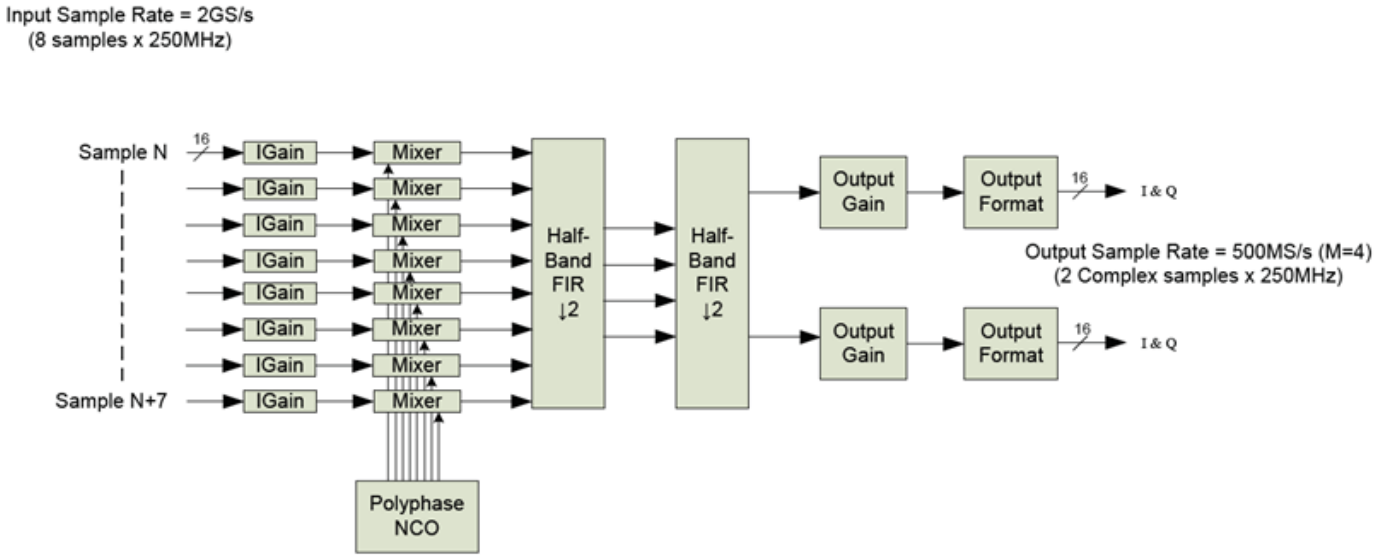


Figure 23: Architectural example of DDC suitable for VPX3-530 data rates

Embedded DDC Options

A reference design is included which provides simple decimators to down sample the multi-GBps of data that can be generated by the VPX3-530. Curtiss-Wright can provide DDC IP either as a drop replacement for the decimator in the reference design or as IP which can be integrated into an HDL application. High DDC usually require some level of customization to deal with the trade-offs associated with maximizing FPGA resource and throughput. For this reason, Curtiss-Wright has developed DDC IP designed for semi-custom modification up to ultra-wideband functionality for use on products like the VPX3-530. An example architecture of a DDC suitable for the VPX3-530 data rates is shown above in Figure 23. Contact Curtiss-Wright for more information on high bandwidth DDCs.

Quick Start Kits and Systems

The VPX3-530 can be purchased in a number of ways ranging from boards only to kits to systems ready for developers to load their own applications on to.

Quick Start Kits (QSKs) provide a lab chassis, VPX3-530 hardware, a suitable SBC, an optional sample clock generator and software tools. This formula allows customers to purchase a kit of parts without having to wonder whether key elements are missing and therefore convenient.

Additional integrated or rugged solutions can also be provided. These systems provide bespoke system to be provide pre-integrated to you system requirements

Contact Curtiss-Wright for more information on QSKs or configured sub-systems.

Rugged Build Options

A range of environmental requirements are addressed by the VPX3-530 including commercial, air-cooled rugged and conduction-cooled. Contact Curtiss-Wright for details.

VPX3-530 VPX Pinout

TABLE 2 VPX3-530 VPX Pinout

PIN		G	F	E	D	C	B	A
VPX P0	1	NC	NC	NC	NC	NC	NC	NC
	2	NC	NC	NC	NC	NC	NC	NC
	3	5V	5V	5V	NC	5V	5V	5V
	4	IPMBB_SCL	IPMBB_SDA	GND	NC	GND	SYSRST	NVMRO
	5	GAP	GA4	GND	3V3_AUX	GND	IPMBA_SCL	IPMBA_SDA
	6	GA3	GA2	GND	NC	GND	GA1	GA0
	7	JTAG_TCK	GND	JTAG_TDO	JTAG_TDI	GND	JTAG_TMS	JTAG_TRST
	8	GND	REF_CLK_N	REF_CLK_P	GND	1PPS_N	1PPS_P	GND
VPX P1	1	P1_SE1 MBSC_SYNC	GND	PCIE_TX0_N	PCIE_TX0_P	GND	PCIE_RX0_N	PCIE_RX0_P
	2	GND	PCIE_TX1_N	PCIE_TX1_P	GND	PCIE_RX1_N	PCIE_RX1_P	GND
	3	V_BAT	GND	PCIE_TX2_N	PCIE_TX2_P	GND	PCIE_RX2_N	PCIE_RX2_P
	4	GND	PCIE_TX3_N	PCIE_TX3_P	GND	PCIE_RX3_N	PCIE_RX3_P	GND
	5	SYSCON_L	GND	PCIE_TX4_N	PCIE_TX4_P	GND	PCIE_RX4_N	PCIE_RX4_P
	6	GND	PCIE_TX5_N	PCIE_TX5_P	GND	PCIE_RX5_N	PCIE_RX5_P	GND
	7	P1_SE3	GND	PCIE_TX6_N	PCIE_TX6_P	GND	PCIE_RX6_N	PCIE_RX6_P
	8	GND	PCIE_TX7_N	PCIE_TX7_P	GND	PCIE_RX7_N	PCIE_RX7_P	GND
	9	P1_SE4	GND	HSS_TX0_N	HSS_TX0_P	GND	HSS_RX0_N	HSS_RX0_P
	10	GND	HSS_TX1_N	HSS_TX1_P	GND	HSS_RX1_N	HSS_RX1_P	GND
	11	P1_SE5	GND	HSS_TX2_N	HSS_TX2_P	GND	HSS_RX2_N	HSS_RX2_P
	12	GND	HSS_TX3_N	HSS_TX3_P	GND	HSS_RX3_N	HSS_RX3_P	GND
	13	P1_SE6	GND	HSS_TX4_N	HSS_TX4_P	GND	HSS_RX4_N	HSS_RX4_P
	14	GND	HSS_TX5_N	HSS_TX5_P	GND	HSS_RX5_N	HSS_RX5_P	GND
	15	P1_SE7	GND	HSS_TX6_N	HSS_TX6_P	GND	HSS_RX6_N	HSS_RX6_P
	16	GND	HSS_TX7_N	HSS_TX7_P	GND	HSS_RX7_N	HSS_RX7_P	GND
VPX P2	1	P2_SE0	GND	LVDS_1_N	LVDS_1_P	GND	LVDS_0_N	LVDS_0_P
	2	GND	LVDS_3_N	LVDS_3_P	GND	LVDS_2_N	LVDS_2_P	GND
	3	P2_SE1	GND	LVDS_5_N[1]	LVDS_5_P[1]	GND	VDS_4_N	LVDS_4_P
	4	GND	LVDS_7_N	LVDS_7_P	GND	LVDS_6_N	LVDS_6_P	GND
	5	P2_SE2	GND	LVDS_9_N	LVDS_9_P	GND	LVDS_8_N	LVDS_8_P
	6	GND	LVDS_11_N	LVDS_11_P	GND	LVDS_10_N	LVDS_10_P	GND
	7	P2_SE3	GND	LVDS_13_N	LVDS_13_P	GND	LVDS_12_N	LVDS_12_P
	8	GND	LVDS_15_N	LVDS_15_P	GND	LVDS_14_N	LVDS_14_P	GND
	9	P2_SE4	GND	LVDS_17_N	LVDS_17_P	GND	LVDS_16_N	LVDS_16_P
	10	GND	LVDS_19_N	LVDS_19_P	GND	LVDS_18_N	LVDS_18_P	GND
	11	P2_SE5	GND	LVDS_21_N	LVDS_21_P	GND	LVDS_20_N	LVDS_20_P
	12	GND	LVDS_23_N[2]	LVDS_23_P[2]	GND	VDS_22_N[1]	LVDS_22_P[1]	GND
	13	P2_SE6	GND	LVDS_25_N[2]	LVDS_25_P[2]	GND	LVDS_24_N[2]	LVDS_24_P[2]
	14	GND	LVDS_27_N	LVDS_27_P	GND	LVDS_26_N[1]	LVDS_26_P[1]	GND
	15	P2_SE7	GND	RS485_IN0_N	RS485_in0_P	GND	RS485_OUT0_N	RS485_OUT0_P
	16	GND	RS485_IN1_N	RS485_IN1_P	GND	RS485_out1_N	RS485_OUT1_P	GND

Notes:

1. Multi-Region Clock Capable (MRCC)
2. Single-Region Clock Capable (SRCC)

Configuration Examples

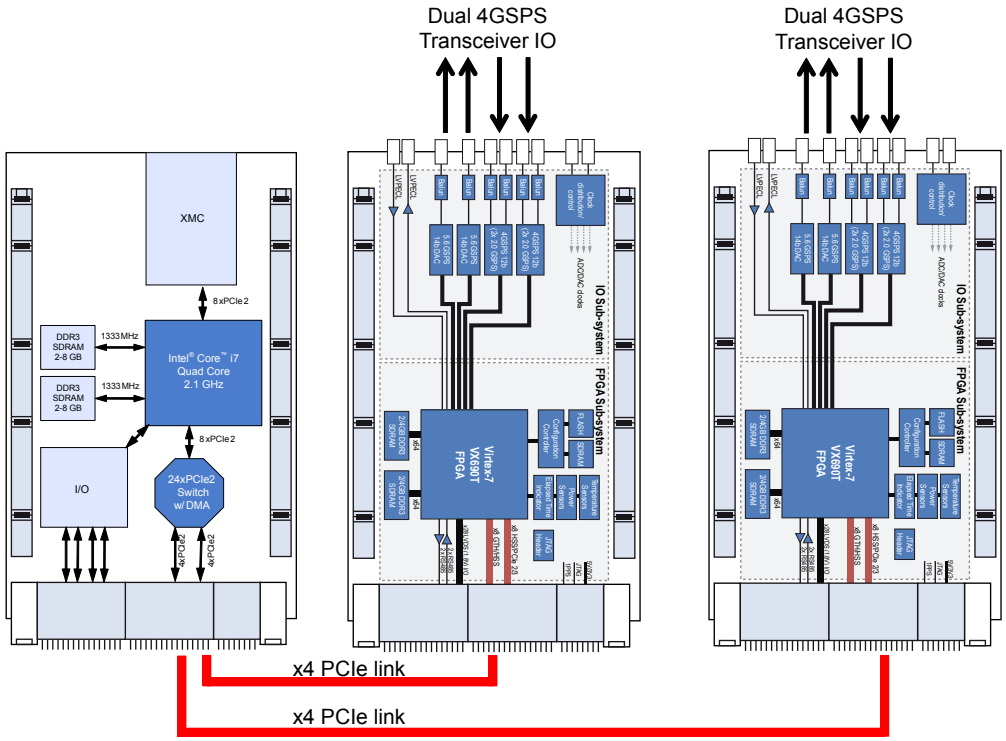


Figure 24: Quad transceiver example

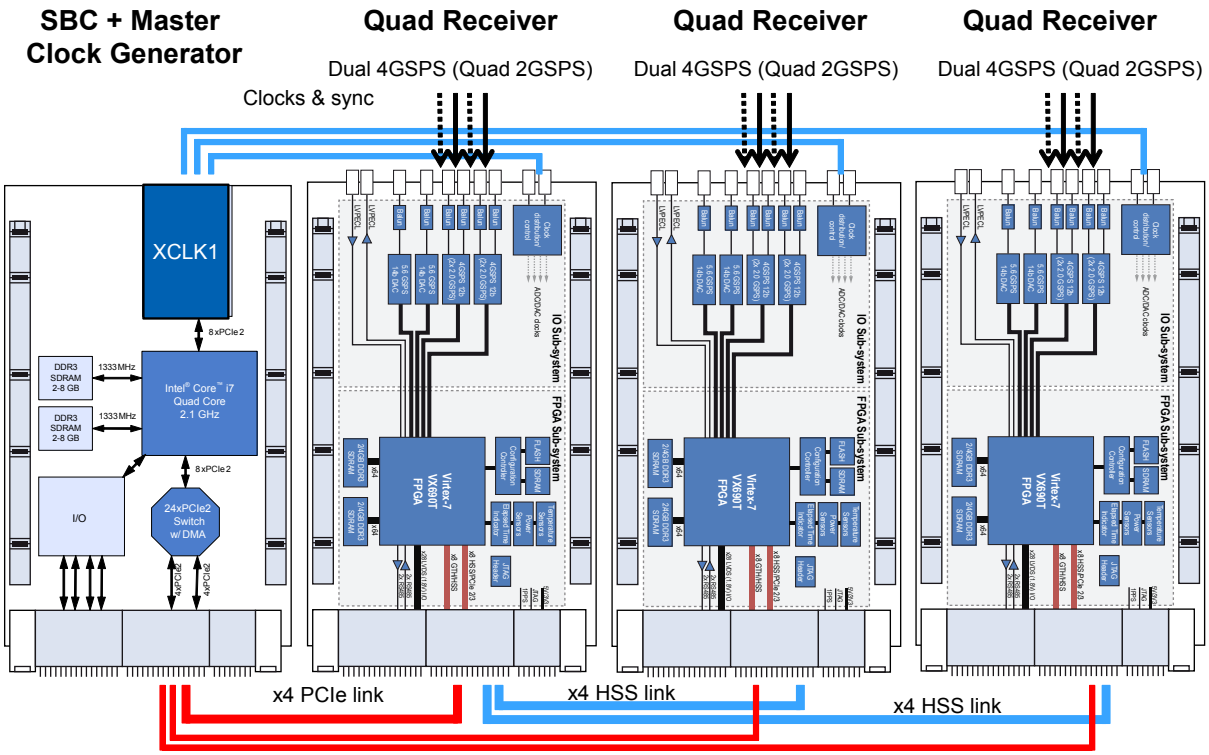


Figure 25: SIGINT/Direction finding example

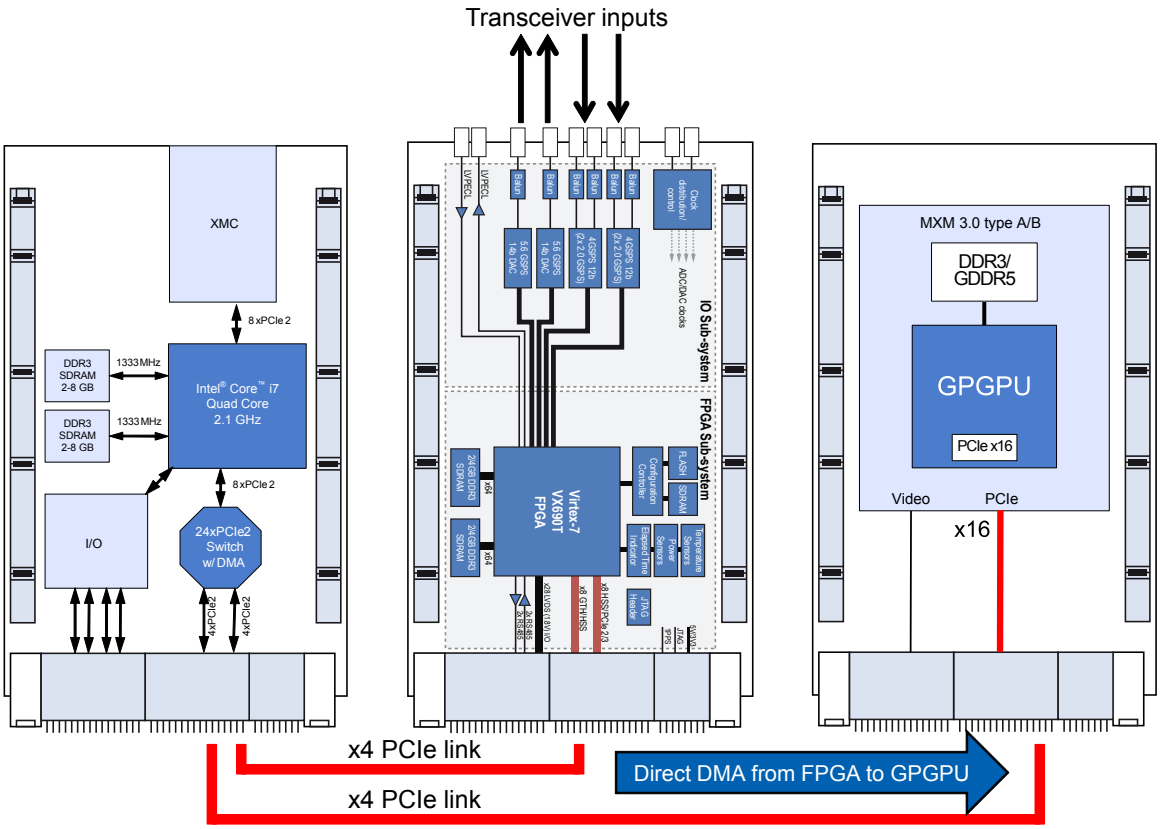


Figure 26: Integration with a GPGPU with direct DMA support (via PCIe Bridge)

Ordering Information

TABLE 3 Analog Input/Output

PART NUMBER	CHANNELS		RUGGEDIZATION	COMMENT
	INPUT	OUTPUT		
VPX3-530-A061240	4x 2 GSPS	2x 5.6 GSPS (2.8 GSPS update rate)	AC L0	2 GSPS mode
VPX3-530-A161240	4x 2 GSPS	2x 5.6 GSPS (2.8 GSPS update rate)	AC L100	2 GSPS mode
VPX3-530-C261240	4x 2 GSPS	2x 5.6 GSPS (2.8 GSPS update rate)	CC L200	2 GSPS mode
VPX3-530-A062240	2x 4 GSPS	2x 5.6 GSPS (2.8 GSPS update rate)	AC L0	4 GSPS mode
VPX3-530-A162240	2x 4 GSPS	2x 5.6 GSPS (2.8 GSPS update rate)	AC L100	4 GSPS mode
VPX3-530-C262240	2x 4 GSPS	2x 5.6 GSPS (2.8 GSPS update rate)	CC L200	4 GSPS mode
VPX3-530-XFL	-	-	-	FusionXF tools for a Linux based host (inc. example designs)
VPX3-530-XFV	-	-	-	FusionXF tools for a VxWorks based host (inc. example designs)

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