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Find the *Curtiss-Wright VPX3-534* at our website: ***Click HERE***

VPX3-534

Quad 3 Gsps Transceiver with Xilinx® UltraScale™ FPGA

CURTISSWRIGHTDS.COM



Key Features

- Quad 3 Gsps 12-bit ADC inputs (or dual 6 Gsps 12-bit)
- Dual 6 Gsps 12-bit DAC outputs
- Xilinx user programmable Kintex UltraScale FPGA
- Embedded Zynq UltraScale+ MPSoC including quad ARM core CPU
- 3U OpenVPX compliant
- Onboard power and temperature measurement
- VxWorks and Linux support
- Conduction-cooled build

Applications

- Radar
- SIGINT/ELINT
- Electronic Warfare
- Software Defined Radio

Overview

The VPX3-534 combines multiple channel high-speed Analog to Digital Converters (ADC) and Digital to Analog Converters (DAC), a user programmable Xilinx® Kintex® UltraScale™ FPGA and Xilinx® Zynq™ UltraScale+ MPSoC® in a range of rugged build formats for demanding applications such as radar, Signal Intelligence (SIGINT), Electronic Warfare (EW), and Software Defined Radio (SDR).

Analog I/O and Synchronization

The VPX3-534 supports up to four 3 Gsps 12b analog inputs with a mode for interleaving ADCs to achieve a dual 6 Gsps 12b inputs. Each analog input is AC coupled via baluns to support full 6 GHz bandwidth.

Complementing the analog inputs, two 12-bit DAC outputs operate at 6 Gsps non-interpolated outputs.

The VPX3-534 is architected for synchronous operation, and to support multiple modes. In its most basic mode, a common Radio Frequency (RF) sample clock can be used to drive all ADCs and DACs. Synchronization IP provided with the HDK/SDK package ensures both ADCs and DACs are aligned for phase coherent operation. This allows for proper support of I&Q based inputs from tuner front ends and synchronous modes required by applications such as EW.

In addition to onboard ADC and DACs synchronization, the VPX3-534 provides multi-board synchronization (note: first generation IP will not support multi-board synchronization) to support radar beamforming and SIGINT or direction finding applications. Multi-board synchronization requires a Curtiss-Wright Defense Solutions multi-channel clock generator that performs both low jitter sample RF sample clock distribution and a stoppable mode that allows digital data paths to be aligned in the background for full synchronous operation.

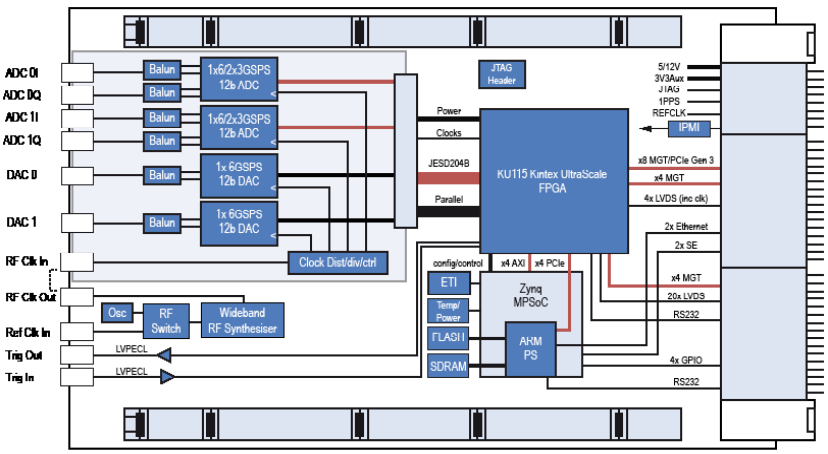


Figure 1: VPX3-534 block diagram

Xilinx Kintex UltraScale FPGA

The VPX3-534 is built around a user programmable Xilinx Kintex UltraScale KU115 FPGA resource (speed grade 2). A Xilinx Virtex UltraScale+ VU9 option will be available via VPX3-535 derivative, with VITA 48.8 Air-Flow Through (AFT) for high power cooling. See Table 1 below for a comparison of the onboard resources. VPX3-535 also provides extended flash support and dual banks of DDR4 SDRAM directly attached to the Virtex UltraScale+ FPGA.

The FPGA configuration images can be either stored in the flash memory, SDRAM or controlled by the Zynq MPSoC processor. Configurations can be downloaded from a remote host across PCIe or network due to the DDR SDRAM resource. This bypasses non-volatile flash, and since SDRAM based configuration is volatile, it is an attractive mode for security sensitive applications and allows the VPX3-534 to be more easily declassified should the need arise.

The FPGA can be reconfigured from any one of a number of images indexed in the flash including a write protected recovery configuration. FPGA configuration from either flash or DDR SDRAM (contact factory) can also take advantage of the encryption modes supported by these FPGAs.

Xilinx Zynq UltraScale+ MPSoC

The VPX3-534 has an embedded Zynq ZU4 MPSoC that fulfills a number of optional functions including processing, system I/O and security.

The Zynq UltraScale+ MPSoC includes a quad Cortex®-A53 ARM® application processor core and a dual Cortex-R5 real-time processing engine. This allows the VPX3-534 to be a self-contained I/O, FPGA and user programmable CPUs in a single product occupying a single 3U VPX slot. Alternatively, external host CPUs can be used to drive multiple VPX3- 534 cards as a centralized processing engine (contact factory for information on which SBCs are supported).

Programmable Sample Clock Generator

To simplify the use of the VPX3-534, an onboard programmable clock is provided. The reference for this clock generator is either from an external master reference or a local high quality clock. The clock source is user selectable. Alternatively, a separate external master RF sample clock can be fed to the VPX3-534.

VPX Connectivity

The VPX3-534 supports OpenVPX profiles for PCIe Generation 1, 2 and 3.

PCIe is supported through direct connectivity to the Xilinx Virtex FPGA.

Additional backplane connectivity is provided for high-speed serial ports for efficient inter-FPGA data links, direct I/O, and to drive fiber-optic data links, serial FPDP or Ethernet.

The Zynq processor sub-system has its own dedicated backplane I/O for RS-485 console, Ethernet and digital I/O.

Software/HDL Support

Curtiss-Wright's VPX3-534 SmartXF™ Development Kit includes software, HDL and utilities complete with examples for using the card. The tools include a C programming language API, driver framework and sophisticated DMA support. One of the core elements of the development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively.

Software utilities are provided for configuring the FPGA. These include flash programming and configuring the FPGA from one of many indexed images in flash.

SmartXF supports VxWorks® (contact factory for Linux availability and revision) operating systems.

TABLE 1 Selected resource comparison between FPGA sizes

Logic Cells	693K	1,451K	1,724K	2,518K
Flip Flops	864K	1,327K	1,576K	2,364K
LUTs	432K	663K	788K	1,182K
DSP Slices	3,600	5,520	4,560	6,840
BRAM	52.9 Mb	75.9 Mb	50.6 Mb	75.9 Mb
URAM	0	0	180 Mb	270 Mb

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Specifications Summary

Analog input

- Number of channels: 4 (3 Gsps per channel)
- Full scale input: TBC
- Analog bandwidth: 6 GHz
- SFDR: TBC @ 1 GHz, 6 Gsps
- Input impedance: 50 Ohm, AC-coupled
- Input connector: SMPM
- Device: Texas Instruments ADC12DJ3200

Analog output

- Number of channels: 2 @ 6 Gsps or 4 @ 3 Gsps
- Full scale output: TBC
- Analog bandwidth: 6 GHz (TBC)
- SFDR: TBC @ 2.205 GHz, 6 Gsps
- Output impedance: 50 Ohm, AC-coupled
- Output connector: SMPM
- Device: E2V EV12DS460A

User Programmable Virtex FPGA

- Device: Xilinx Kintex UltraScale KU115 (speed grade 2), contact factory for alternative FPGA sizes
- Configuration
  - QSPI flash (FPGA boot/configuration including recovery image)
  - Zynq UltraScale+ MPSoC
  - JTAG/ChipScope™ Pro port

Zynq MPSoC

- Device: Xilinx Zynq UltraScale+ ZU3
- Memory: 1 x 32b bank DDR4 SDRAM
- Connectivity: RS-232, dual Ethernet

Clock

- Clock input sources:
  - External RF reference
  - External 10 to 100 MHz reference clock to programmable clock generator
  - Onboard 10 MHz reference clock to programmable clock generator
- Clock input: 50 Ohm, AC coupled LVPECL
- Trigger input/output: Single-ended, 50 Ohm, LVPECL buffered to FPGA
- Clock input connector: Front panel SMPM

VPX

- OpenVPX™ profiles
  - SLT3-PAY-2F1F2U-14.2.1Y
- VPX P0
  - 5V and 12V primary supplies: TBD A (max)
  - 3V3_Aux: 0.8A (max)
  - 3V3: not required
  - 1PPS
  - REF_CLK
  - JTAG
- VPX P1
  - 8 x PCI Express® (PCIe) 2/3
  - 4 x HSS full duplex (user defined)
  - 3 x LVDS
  - 1 x Ref clock
  - 2 x Ethernet (Zynq MPSoC)
- VPX P2
  - 2 x RS-422/485 inputs (FPGA controlled)
  - 2 x RS-422/485 outputs (FPGA controlled)
  - 20 x 1.8V LVDS (FPGA controlled)
  - 2 x Ethernet (Zynq MPSoC)
  - 4 x HSS full duplex (user defined up to TBC Gbps per lane)
  - 4 x GPIO (MPSoC)
  - 2 x RS232 (1x MPSoC, 1x PL)
- Board pitch
  - Conduction-cooled: 1”

Software/HDL

- Support/Utilities
  - VPX3-534 tools Development Kit
  - FPGA/flash programming, diagnostics
- Host drivers: VxWorks® (contact factory for Fedora™ Linux® availability)
- HDL example: Memory interfaces, PCIe, data DMA, data acquisition, data playback

Miscellaneous

- Elapsed Time Indicator (ETI): 0.25 second resolution, maximum accumulated time 34 years
- Power: Card input voltage and current measurement facility

TABLE 2 VPX3-534 VPX Backplane Pinout

	PIN	G	F	E	D	C	B	A
VPX P0	1	12V[3]	12V[3]	12V[3]	NC	3.3V[3]	3.3V[3]	3.3V[3]
	2	12V[3]	12V[3]	12V[3]	NC	3.3V[3]	3.3V[3]	3.3V[3]
	3	5V	5V	5V	NC	5V	5V	5V
	4	IPMBB_SCL	IPMBB_SDA	GND	-12V_AUX[3]	GND	SYSRST_L	NVMRO
	5	GAP_L	GA4_L	GND	3V3_AUX	GND	IPMBA_SCL	IPMBA_SDA
	6	GA3_L	GA2_L	GND	+12V_AUX[3]	GND	GA1_L	GA0_L
	7	JTAG_TCK	GND	JTAG_TDO	JTAG_TDI	GND	JTAG_TMS	JTAG_TRST_L
	8	GND	REF_CLK_N	REF_CLK_P	GND	1PPS_N	1PPS_P	GND
VPX P1	1	GDiscrete (MBSC_SYNC_L)	GND	PCIE_TX0_N	PCIE_TX0_P	GND	PCIE_RX0_N	PCIE_RX0_P
	2	GND	PCIE_TX1_N	PCIE_TX1_P	GND	PCIE_RX1_N	PCIE_RX1_P	GND
	3	V_BAT	GND	PCIE_TX2_N	PCIE_TX2_P	GND	PCIE_RX2_N	PCIE_RX2_P
	4	GND	PCIE_TX3_N	PCIE_TX3_P	GND	PCIE_RX3_N	PCIE_RX3_P	GND
	5	SYSCON_L	GND	PCIE_TX4_N	PCIE_TX4_P	GND	PCIE_RX4_N	PCIE_RX4_P
	6	GND	PCIE_TX5_N	PCIE_TX5_P	GND	PCIE_RX5_N	PCIE_RX5_P	GND
	7	JTAG_SEL0	GND	PCIE_TX6_N	PCIE_TX6_P	GND	PCIE_RX6_N	PCIE_RX6_P
	8	GND	PCIE_TX7_N	PCIE_TX7_P	GND	PCIE_RX7_N	PCIE_RX7_P	GND
	9	JTAG_SEL1	GND	HSS_TX0_N	HSS_TX0_P	GND	HSS_RX0_N	HSS_RX0_P
	10	GND	HSS_TX1_N	HSS_TX1_P	GND	HSS_RX1_N	HSS_RX1_P	GND
	11	ALT_BOOT_L	GND	HSS_TX2_N	HSS_TX2_P	GND	HSS_RX2_N	HSS_RX2_P
	12	GND	HSS_TX3_N	HSS_TX3_P	GND	HSS_RX3_N	HSS_RX3_P	GND
	13	WR_EN_L	GND	LVDS_1_N	LVDS_1_P	GND	REF_CLK_N	REF_CLK_P
	14	GND	LVDS_3_N	LVDS_3_P	GND	LVDS_2_N	LVDS_2_P	GND
	15	MaskableReset_L	GND	CP_GE1_T-	CP_GE1_T+	GND	CP_GE1_R-	CP_GE1_R+
	16	GND	CP_GE0_T-	CP_GE0_T+	GND	CP_GE0_R-	CP_GE0_R+	GND
VPX P2	1	PSRS232_TX0	GND	HSS_TX4_N	HSS_TX4_P	GND	HSS_RX4_N	HSS_RX4_P
	2	GND	HSS_TX5_N	HSS_TX5_P	GND	HSS_RX5_N	HSS_RX5_P	GND
	3	PSRS232_RX0	GND	HSS_TX6_N	HSS_TX6_P	GND	HSS_RX6_N	HSS_RX6_P
	4	GND	HSS_TX7_N	HSS_TX7_P	GND	HSS_RX7_N	HSS_RX7_P	GND
	5	PLRS232_TX1	GND	DIO _5_N	DIO _5_P	GND	DIO _4_N	DIO_4_P
	6	GND	DIO _7_N	DIO _7_P	GND	DIO _6_N	DIO _6_P	GND
	7	PLRS232_RX1	GND	DIO _9_N	DIO _9_P	GND	DIO _8_N	DIO _8_P
	8	GND	DIO _11_N	DIO _11_P	GND	DIO _10_N	DIO _10_P	GND
	9	MPSoC_SE0	GND	DIO _13_N	DIO _13_P	GND	DIO _12_N	DIO _12_P
	10	GND	DIO _15_N	DIO _15_P	GND	DIO _14_N	DIO _14_P	GND
	11	MPSoC_SE1	GND	DIO _17_N	DIO _17_P	GND	DIO_16_N	DIO _16_P
	12	GND	DIO _19_N	DIO _19_P	GND	DIO _18_N	DIO _18_P	GND
	13	MPSoC_SE2	GND	DIO _21_N	DIO _21_P	GND	DIO _20_N	DIO _20_P
	14	GND	DIO _23_N	DIO _23_P	GND	DIO _22_N	DIO _22_P	GND
	15	MPSoC_SE3	GND	RS485_IN0_N	RS485_IN0_P	GND	RS485_OUT0_N	RS485_OUT0_P
	16	GND	RS485_IN1_N	RS485_IN1_P	GND	RS485_OUT1_N	RS485_OUT1_P	GND

Ordering Information

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