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Find the *Curtiss-Wright VPX3-127-A01A210* at our website: *Click HERE*







Data Sheet

VPX3-127

Single Board Computer



Features

- Single or Dual-core Freescale Power Architecture™ MPC8640 processor up to 1.25 GHz
  - 2x e600 processor cores
  - Each core has 64 KB L1 cache
  - Each core has 1 MB L2 cache with ECC
  - 16 GFLOPs @ 1.0 GHz (dual-core)
- MPC8640 additional features
  - 2x DDR2 memory controllers with ECC
  - 2x Gigabit Ethernet (GbE) controllers
  - Serial I/O controller
  - 2x I2C channels
  - 2x PCI Express® (PCIe) interfaces
  - 1x Serial RapidIO® (SRIO) interface
- Two independent 64-bit DDR2 SDRAM controllers integrated into the MPC8640
- Up to 2 GB of DDR2 SDRAM with ECC to correct single-bit errors and detect double-bit errors
- Up to 1 GB of resident NAND Flash
- 256 MB of contiguous direct-mapped Flash memory
  - Hardware Flash write protection jumper
- Permanent Alternate Boot Site (PABS) provides back-up boot capability
- 512 KB Ferroelectric Random Access Memory (FRAM)
- Two x4 fabric ports on the VPX P1 connector mapped as per VITA 46.9 that can be configured as:
  - Two x4 PCIe ports, one port non-transparent capable
  - One x8 PCIe port (not transparent)
  - One x4 PCIe port + one x4 SRIO port
- One PMC/XMC (VITA 42.3) site on independent PCI and PCIe buses
  - Provides either a 133 MHz PCI-X capable interface or 8-lane PCIe interface
  - For PN4 - 64 signals from the PN4 are routed to the backplane as 32 differential pairs following VITA 46.9 pinout, 64S pattern
  - For XMC PN6 - follows the VITA 46.9 X20D2 4S pin-out which provides 20 differential pairs and 24 single-ended signals
- Conduction-cooling of PMC/XMC sites optimized with secondary thermal interfaces and mid plane thermal shunt
- Two GbE interfaces on P1 connector mapped per VITA 46.9
  - Configuration option to supports 2x 1000Bx GbE interfaces
- Up to four asynchronous RS-232 serial ports
- Two synchronous capable RS-422 serial full duplex channels with DMA and HDLC support
  - Each serial signal is software-configurable as differential discrete I/O, with interrupt capability on inputs. Provides up to four differential I/O inputs and four differential I/O outputs
- Up to eight LVTTL discretes, each is software configurable as input or output, with interrupt capability as input
- Up to two USB 2.0 ports
- Four general-purpose 32-bit user timers per core provided by Core Functions FPGA

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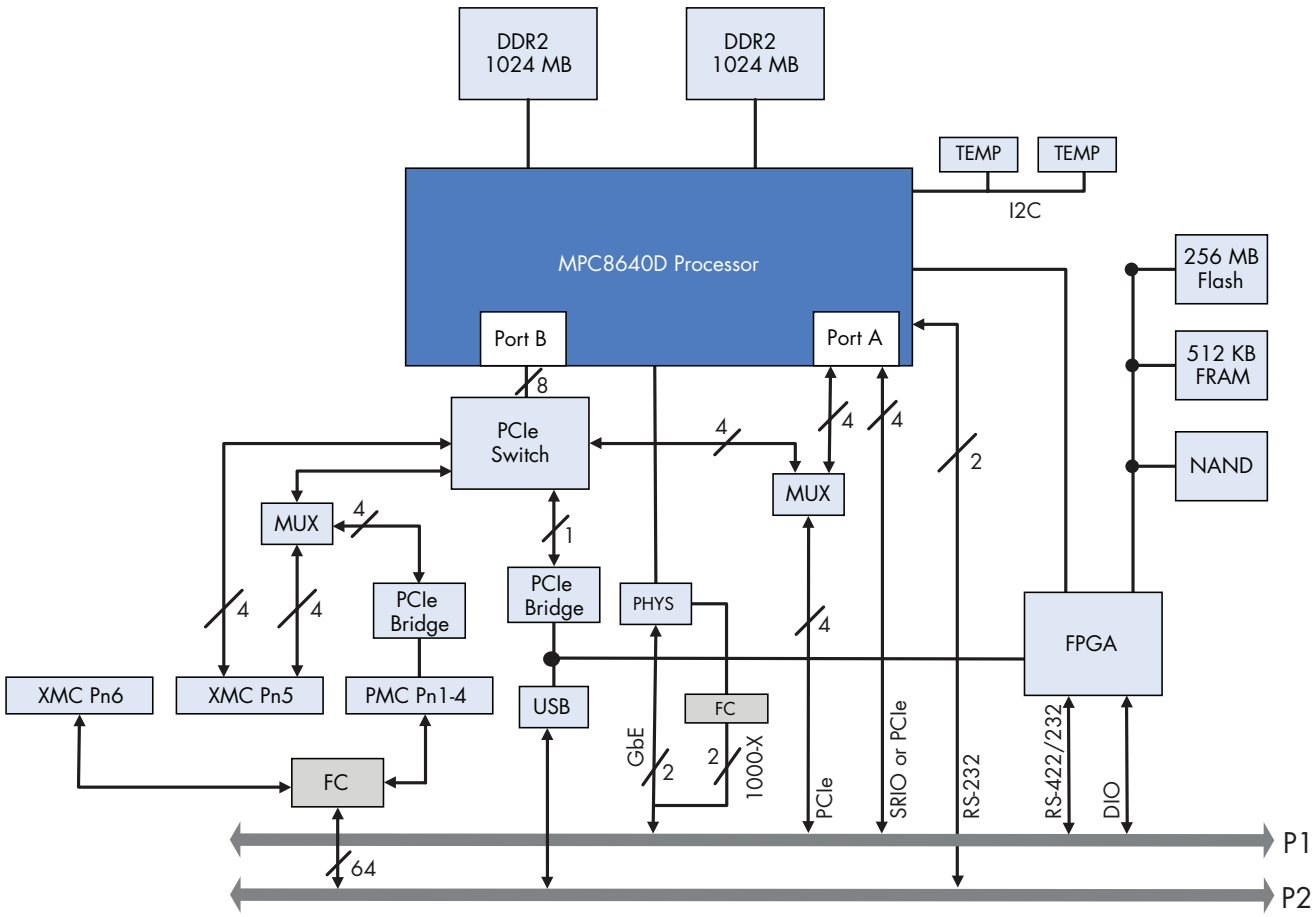
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- General purpose DMA controllers provided by the MPC8640
- Two avionics-style watchdog timers with external watchdog event indicator discrete
- Two on-board temperature sensors, with alarm interrupts, plus processor temperature sensors
- Status LED
- +5V operation
- Power management features
- CSA firmware providing a comprehensive suite of system debug, exerciser, and update functions, BIT, and non-volatile memory sanitization function
- Circuit card assembly is done to class 3 standards of IPC-A-610C, Acceptability of Electronic Assemblies
- Standard conformal coating is acrylic
- PWB meets UL 94 V-0 flammability rating
- Available in a range of ruggedization levels
  - Air-cooled level 0 and 100, conduction-cooled level 200 per VITA 46.0 (.8" pitch)
  - Conduction-cooled per VITA 48.2, Type 1 card (.85" pitch with top and bottom covers, compatible with 1.0" pitch usage) upon customer request
- Available software packages
  - VxWorks® 6.5+ BSP and Driver Suite supporting Workbench 2.x IDE
  - VxWorks 6.5+ MIL-STD-1553 Driver
  - Continuum Vector AltiVec™-optimized signal processing library
  - Wind River® Linux®
  - INTEGRITY® available from Green Hills®

Figure 1: VPX3-127 Block Diagram



Note:
FC- Factory Configuration

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Introduction

Curtiss-Wright Controls Embedded Computing's VPX3-127 combines the performance and the advanced I/O capabilities of MPC8640 low power processor with an extensive I/O complement to provide a highly capable processing platform for a wide range of embedded military/ aerospace applications. Designed for space constrained applications, the VPX3-127 represents the latest step in the evolution of rugged high performance, highly integrated small form factor single board computers (SBCs).

Available in a full range of environmental build grades the VPX3-127 is targeted to the challenging task of high density computing packing the greatest functionality into the smallest standard form factor, with the lowest power possible while retaining as much flexibility as possible. The VPX3-127 meets this challenge by offering impressive complement of I/O capability to satisfy the most demanding application needs, be it in tactical aircraft, armored vehicles or rugged naval systems.

The VPX3-127 is designed to occupy a standard 0.8" slot and may be used for upgrading existing CompactPCI (cPCI) systems in the same footprint.

VPX Module Format

The Versatile Performance Switching (VPX) module format, governed by the VITA 46 specification and the associated VITA 48 Ruggedized Enhanced Design Implementation (REDI) was established to address the fundamental requirement to provide open-architecture modules that incorporate the high-speed serial interconnect technology that is becoming pervasive in high performance computing. The VPX standard was developed by the leading providers of military commercial-off-the-shelf (COTS) modules to address the major issue of high-speed serial interconnect, as well as incorporating numerous improvements learned after years of integrating VME and cPCI modules. The VPX standard, in short provides:

- 3U and 6U Eurocard form factors preserve chassis mechanical designs
- Support four up to x4 serial interfaces as the primary fabric
- Support up to 128 differential pairs in 6U format for modern high-speed interfaces such as DVI, SATA, SFPDP, SAS and custom sensor interfaces
- Support of VME for interoperability with legacy equipment
- Support of higher power modules and improved cooling
- Improved logistics with two-level maintenance and keying

The VPX module format provides many benefits to integrators of high performance multi-processor systems for radar, electro-optical and signal intelligence applications. In particular SRIO is suited to high-bandwidth communications between processors in a VPX system, while PCIe functions as a fast connection between processors and the new generation of XMC modules which can easily be placed on VPX format carrier cards.

Overview

The VPX3-127 is one of a family of modules from Curtiss-Wright to employ the new open-architecture VITA 46 standard. VITA 46, also known as "VPX" was collaboratively developed by COTS industry leaders which included prime military integrators to marry high-speed serial interconnect such as SRIO and PCIe. It is well suited to the military/aerospace which can take advantage of and utilize this form factor and feature set in their demanding applications. The VPX3-127 provides SBC functionality to the Curtiss-Wright VPX family that includes quad-processor DSP, FPGA accelerator and XMC/PMC carrier modules.

The VPX3-127 is based on the MPC8640 processor. Available in single-core and dual-core versions with AltiVec and up to 2 GB of high-bandwidth DDR2 SDRAM, the VPX3-127 provides high performance processing, the massive 4 GB/s bandwidth of VPX and a long list of features and I/O interfaces to satisfy the most demanding requirements of embedded computing.

Available in a full range of environmental build grades the VPX3-127 is targeted to the challenging data- and digital signal-processing needs of tactical aircraft, armored vehicles and harsh environment naval systems.

The VPX3-127 will occupy a standard 0.8" slot and may be used for upgrading existing cPCI systems in the same footprint. The VPX3-127 is also available in the VITA 48 (VPX REDI) format with covers to support two level maintenance LRM requirements.

Dual-core Freescale Power Architecture MPC8640 Processor

The processing function of the VPX3-127 is provided by the MPC8640. The MPC8640 provides in a single package one or two e600 cores, dual DDR2 memory controllers with ECC, a SRIO interface, two PCIe interfaces, GbE controllers and serial I/O controllers.

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The e600 core and AltiVec units of the MPC8640 processor are based on the proven internals of the MPC7448 processor, offering a large 1 MB internal L2 cache. Existing C, assembly and AltiVec assembly code will run on the MPC8640 without change.

The MPC8640 processor integrates controller functions that previously required the use of an external bridge. In addition to the benefit of reduced size and higher reliability, the integrated dual memory controllers of the MPC8640 provide a much higher level of performance and reduced latency.

Dual Data Rate (DDR2) SDRAM

The MPC8640 provides two independent DDR2 memory controllers supporting DDR2 SDRAM which the VPX3-127 uses to provide up to 2 GB DDR2 SDRAM. The design supports the next generation of 2-Gbit SDRAM devices, which provides a growth path to for up to 2 GB of SDRAM. The DDR2 interface operates at a rate up to 500 MHz resulting in a peak bandwidth of 4 GB/s per memory bank, 8 GB/s total.

To preserve data integrity, the VPX3-127 takes advantage of the MPC8640 memory controller's ECC circuitry to correct single-bit errors and detect double-bit errors. The SDRAM is accessible from the processor as well as the Ethernet and PCIe interfaces. Subject to the configuration of BSP settings controlling the memory management of the MPC8640 processor, the memory can be accessed from other boards via the off-board PCIe links or local XMC/PMC devices.

Flash Memory

The VPX3-127 is configured with 256 MB of NOR Flash Memory. The Flash will retain data for 20 years at +85C°. Note: these figures assume the sector the data is in has less than 1,000 erase cycles. The data retention drops as erase cycle count increases. After 10,000 cycles, data retention is for 10 years. After 100,000 cycles, data corruption will likely be noticeable in one year. Read performance of the Flash array is optimized in order to minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical.

For absolute security against inadvertent Flash programming or corruption, a hardware jumper is provided to disable writing to Flash. The CSA Firmware on the VPX3-127 provides Flash programming functions with support for downloading Flash images over Ethernet. See the separate CSA firmware data sheet for details.

Permanent Alternate Boot Site (PABS)

The VPX3-127 is equipped with 64 MB of Permanent Alternate Boot Site (PABS) NOR Flash. PABS provides a backup boot capability in the event that the firmware in the main Flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main Flash without removing the card from the system in which it is installed. An on-board jumper is provided to cause the card to boot from PABS, thus allowing a user to reinstall the standard firmware load. The PABS feature guarantees that a card will never need to be removed from a system to perform Flash updates.

FRAM

A Ramtron FM22L16 Ferroelectric Random Access Memory (FRAM) provides fast, non-volatile storage of mission state data that must not be lost when power is removed. FRAM reads and writes like standard SRAM and as with all FRAM devices, writes occur at bus speed and are immediately non-volatile. The FRAM memory is non-volatile due to its unique ferroelectric memory process which means that data is retained after power is removed. It provides data retention for over 10 years. Fast write timing and high write endurance make FRAM superior to other types of memory. The FM22L16 includes a low voltage monitor that blocks access to the memory array when VDD drops below a critical threshold. The memory is protected against an inadvertent access and data corruption under this condition. The device also features software-controlled write protection.

Non-volatile Memory Security

The VPX3-127, as well as other Curtiss-Wright Continuum Architecture products, provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices such as Flash, FRAM and FPGA PROM may be individually write-protected by a hardware jumper. The jumpers may be visually inspected to conform to security procedures.

The CSA Firmware of the VPX3-127 provides a non-volatile memory scrub function to perform a secure erase per NISPOM requirements.

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The VPX3-127 I/O System

The VPX3-127 features a large number of I/O interfaces including EIA-232, EIA-422 serial, USB, Ethernet, TTL and differential discrete I/O. The details of the I/O interfaces are described in the following paragraphs.

Table 1: VPX3-127 Standard Product I/O

	Standard Product I/O Options		
	Mode 0	Mode 1	Mode 2
x4 fabric	2 PCIe or 1 PCIe +1 SRIO	2 PCIe or 1 PCIe +1 SRIO	2 PCIe or 1 PCIe +1 SRIO
EIA-232	2	2	2
EIA-422	2 Sync	2 Async	2 Async
Gigabit Ethernet	2GbE	2GbE	2GbE
USB	1	2	2
DIO	4	8	8
PMC I/O	32 diff. pairs (P64S)	32 diff. pairs	-
XMC IO (PN6)	-	-	20 diff pairs, 24 single-ended (X12D+X8D+X24S)
Diff. I/O Max (shared)	4 In 4 Out	2 In 2 Out	2 In 2 Out
XMC (PN5)	x8 PCIe	x8 PCIe	x8 PCIe

Two Gigabit Ethernet Interfaces

The VPX3-127 provides two 10/100/1000Base-T Ethernet interfaces in I/O mode 0 and 1, both implemented within the MPC8640. Both ports are routed to the P1 backplane connector and follow the pinout as defined by VITA 46.9. The Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9 KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence. Dependent on the configuration option ordered, these ports can be operated as 1000Bx SERDES. They are still routed to P1.

Fabric Ports

The VPX3-127 provides two x4 PCIe ports to the backplane on all I/O modes, both implemented within the MPC8640. Both ports are routed to the P1 backplane connector and follow the pinout as defined by VITA 46.4. These interfaces can be used to interconnect VPX3-127's together or to expand PMC/XMC capability using the VPX3-215 3U ExpressReach Carrier. One of the two fabric ports can also be configured to run as a x4 SRIO fabric port.

The VPX3-127 I/O System

The VPX3-127 features a large number of I/O interfaces including EIA-232, EIA-422 serial, USB, Ethernet, TTL and differential discrete I/O. The details of the I/O interfaces are described in the following paragraphs.

Two EIA-232 Serial Ports

All VPX3-127 configurations provide two EIA-232 serial channels. The EIA-232 serial ports (Channels 0, 1) support asynchronous communications with one transmit and one receive signal. The two ports are connected to the P2 connector single-ended signals. One serial port supports the use of the DCD signal to automatically detect the connection of a data terminal and can be used to control the boot-up sequence of the card if desired. Both ports utilize the MPC8640 DUARTs. The Baud rate of all two ports can be set independently from 300 to 115200.

Two EIA-232/422 Serial Ports

The VPX3-127 is available in configurations with two synchronous capable serial ports. (Channel numbers 2-3). These additional serial ports are implemented with a 85230 Serial Communication Controller (SCC) core in the Core Functions FPGA. Both of the serial ports support asynchronous communication with baud rates of 300 to 115200 in EIA-232 or 422 modes. The serial ports also support synchronous HDLC/SDLC communications at up to 2.0 MB/s in EIA-422 mode. In synchronous mode, a full range of data encoding schemes are supported. (NRZ, NRZI Mark, NRZI Space, FM0, FM1, Manchester, and Differential Manchester) Dependent of the I/O mode ordered, the synchronous ports support separate transmit and receive clock signals and can use internal or external clocking, or clock encoded schemes. The serial ports support software selection of either EIA-232 (async only) or EIA-442 (sync or async) signal levels. See the Differential Discrete I/O section below for information on how the VPX3-127 provides the capability to control each of the EIA-422 drivers and receivers as differential-mode discrete signals for use as serial control signals or general purpose I/O. See Table 2 for configurations that include the optional 232/422 serial channels.

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LVTTL Discrete Digital I/O Option

The VPX3-127 optionally provides up to 8-bits of LVTTL compatible discrete digital I/O. Each bit is individually programmable to be an input or output. Each I/O bit is capable of generating an interrupt upon a change of state, programmable to detect either edge. Each bit has a 10K pull-up resistor to 5V. The output drive current is 24 mA. No protection is provided on DIO.

Differential Discrete Digital I/O

The VPX3-127 provides the capability to control each of the EIA-422 drivers and receivers as differential-mode discrete signals via registers in the Core Functions FPGA. This allows flexibility in how the drivers and receivers are used. The choice of whether the drivers and receivers are attached to serial ports or used as discrete differential I/O is software selectable on a per-serial channel basis. When configured as discrete differential I/O, the drivers and receivers can be used as serial-line control signals (RTS, CD, etc.) in conjunction with another serial channel, or used as general-purpose differential mode control signals unrelated to serial I/O requirements. Differential discrete inputs can generate an interrupt upon a change of state, with programmable edge direction. Note that if the serial channel physical levels are set to EIA-232, then discrete digital I/O at EIA-232 levels is obtained.

Two USB 2.0 Ports

The VPX3-127 incorporates a Phillips ISP1562 USB Controller to provide up to two USB 2.0 ports dependent on the I/O mode. Each port can handle high-speed (480 MB/s), full-speed (12 MB/s), and low-speed (1.5 MB/s) operation. When operating at low- speed or full-speed, each port is managed by independent OHCI-compliant controllers internal to the device. One EHCI compliant controller manages any ports operating in high-speed mode.

One USB port is accessible on the P1 connector and the other is accessible on the P2 connector. Each port provides a +5V output to power external USB devices such as keyboards.

Extensive Timing Resources

The VPX3-127 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in the table below.

Avionics Watchdog Timers

The VPX3-127 provides a watchdog timer for each of the two processor cores. Each watchdog timer is a pre-settable down-counter with a resolution of 1µsec. Time-out periods from 1msec to 32 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts. A watchdog event indicator discrete signal is output to the backplane.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to

Table 2: VPX3-127 Available Timing Resources

Timer	Implementation	Type	Size	Tick Rate/Period	Maximum Duration
PowerPC Time Base Register	1 per CPU	Free Running Counter	64	125MHz/8nsec	4,676 yrs
PowerPC Decrementer	1 per CPU	Presettable, Readable Downcounter	32-bit	125MHz/8nsec	34.35 sec
General Purpose #0-3	MPC8640	Presettable, Readable Downcounter with autoread and stop options	31-bit	62.5MHz/16nsec	34.36 sec
Watchdog Timers (per CPU)	Core Functions FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	25-bit	1MHz/1usec	33.55 sec
System Timers #0-5	Core Functions FPGA	Presettable, readable downcounter with interrupt on terminal count	32-bit	50MHz/20nsec	85.9 sec

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operate in “Avionics” mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event.

General Purpose DMA Controllers

The MPC8640 provides a minimum of four DMA channels that are available for general purpose use. The DMA subsystem can be used for transferring blocks of data between the SDRAM, Flash memory, device bus peripherals, Gigabit and the PCI bus. The DMA controllers support direct and descriptor-driven chained operation. The DMA controllers can support source and destination striding. The DMA controllers also feature a bandwidth management feature to allow the user to control the distribution of bandwidth between the four DMA channels.

XMC/PMC Site

The VPX3-127 is equipped with one mezzanine site, capable of supporting IEEE 1386 PMC or VITA 42.3 XMC modules. The PMC site interfaces to other system elements via 64-pins of back panel I/O, mapped as 32 differential pairs as per VITA 46.9 to P2 (P64S). The PMC sites allows the use of single width PMC modules. The XMC site variant option supports the VITA46.9 X20D24S X12D+X8D+X24S pin-out of 20 differential pairs and 24 single-ended.

The PMC site is served by its own dedicated 64-bit, 133 MHz-capable PCI-X bus providing a peak bandwidth to memory of 800 MB/sec. High-performance PMC modules such as networking modules or graphics modules can operate at 133 MHz. This XMC site variant supports a x8 lane PCIe connection to the MPC8640 thru a PCIe bridge.

The VPX3-127 conforms fully to the IEEE 1386/1386.1 requirement for a component keep-out area at the front of the PMC site for connectors or high components. The PMC site uses 3.3V signaling and is 5V tolerant. No PMC keying is provided. The VIO voltage to PMC site 1 is selectable via push on jumpers.

PMC Power Routing

The PMC site is provided with 5V, 3.3V,+ 12V, and - 12V power from the VITA 46 backplane.

Conduction-cooled PMC Modules

To support the industry drive to open standards on conduction-cooled cards, the PMC site mechanical interfaces follow the VITA 20- 2001 (R2005) conduction-cooled PCI Mezzanine Card standard. To optimize the thermal transfer from PMC modules to the basecard the standard VPX3-127 thermal frame incorporates both the Primary and Secondary thermal interfaces as defined by VITA 20-2001.

The combination of the secondary thermal interfaces, the mid-plane thermal shunt, and Curtiss-Wright TherMax™ thermal frame design provides optimum cooling for conduction-cooled PMC modules, allowing for higher power PMCs and/or increased long-term reliability through lower component temperatures.

Status Indicators and Controls

The VPX3-127 SBC provides run/fail status by asserting a backplane signal and illuminating a red front panel LED in the event the diagnostics detect a card failure. There are also two software controlled green LEDs that the application can use to indicate status of each CPU core independently.

COP Emulator Interfaces

The VPX3-127 provides access to the MPC8640 COP interface. Consult the Hardware User’s Manual for more information if you need to use a COP emulator with the VPX3-127.

Temperature Sensors

The VPX3-127 provides temperature sensors to measure board and processor temperatures. There is a sensor at each edge of the card, one sensor in close proximity to the processor and one sensor to directly measure the die temperature of the MPC8640 using its thermal diode feature. The sensors can be read by software, and they may be configured to generate an interrupt in case of an over temperature condition.

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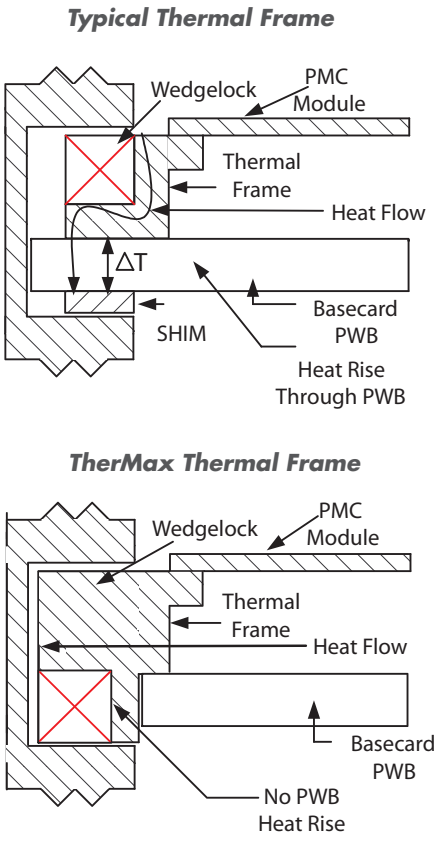


TherMax-style Thermal Frame

A TherMax thermal frame provides an unbroken metallic path from the PMC sites and shunted components to the back- side cooling surface of the card therefore minimizing the temperature rise to these devices. In comparison, a typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB, which has a high thermal resistance compared to aluminum.

Figure 2: TherMax diagram

A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame

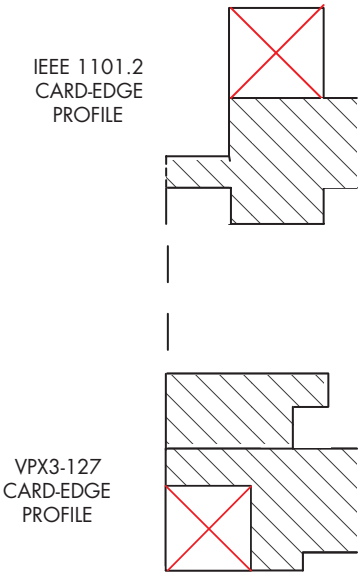


Full-width Thermal Interface to Back-side Slot Wall

To minimize the temperature rise from the mating slot wall of conduction-cooled enclosures to the back-side thermal interface region of the VPX3-127, the VPX3-127 thermal frame maximizes the thermal interface area by extending the frame to the full width of the card, as illustrated in Figure 3. This deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis, has the benefit of lower card operating temperatures and increased long term reliability. During test and integration activities where it may be desirable to install a conduction-cooled VPX3-127 into an air-cooled card-cage, this can normally be accomplished simply by removing the card guides.

Figure 3: Card-edge Profile Deviates from IEEE 1101.2

VPX3-127 *Card-edge Profile is Optimized to Provide a Full-width Thermal Interface to the Back-side Slot Wall*



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Software Support

Continuum Software Architecture (CSA)

The VPX3-127 is supported by a suite of firmware, RTOS board support packages (BSP), communication libraries and signal processing libraries. The Continuum Software Architecture is Curtiss-Wright's suite of firmware and BSP APIs that is common to SBC (VME, cPCI and VPX) and multi-processor boards. Developers of mixed systems will find a common set of features and software interfaces for all future processing products from Curtiss-Wright. The Continuum Software Architecture is comprised of:

Continuum Firmware Monitor

The monitor provides a command line interface over serial port or Ethernet to allow a user to perform a variety of system integration activities with the card. The monitor provides debug and display commands, diagnostic results display and exerciser controls, non-volatile memory programming and declassification and programming of parameters used to control boot-up and diagnostics.

Continuum Built-in-Test (BIT) - a library of diagnostic routines to support Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) designed to provide 95% fault coverage.

Operating System Software

The VPX3-127 is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported or planned for the VPX3-127.

- VxWorks 6.x from Curtiss-Wright (Part number DSW-127-0006-CD).
- Wind River 3.0 Linux BSP from Curtiss-Wright (Part number DSW-127-6100-GPP). The Linux BSP does not support the same level of BIT as does the VxWorks BSPs.

Continuum Vector Library

VPX3-127 derives its floating-point performance from the pair of AltiVec vector/SIMD (single instruction stream, multiple data streams) multimedia extension vector engine technology which is a short vector parallel architecture that extends the Power Architecture instruction set and accelerates the performance of various software applications. The vector instruction set architecture (ISA) is based on separate vector/SIMD-style execution units that have high data parallelism, allowing operation on multiple data elements in a single instruction.

The Continuum Vector Library provides over 200 functions optimized for the AltiVec unit, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for the Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector data sheet for detailed information.

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Rear Transition Module

To gain access to the backplane I/O signals of the VPX3-127, a rear transition module, the RTM3-127-000 is provided. This provides access to the I/O as defined in mode 0 and mode 1 I/O options.

Table 3: Specifications

Power Requirements (estimated - Note 1)		
5V	• Dual-core will range between 32.7W to 38W (6.54A to 7.6A) for 5V • Single-core will range between 22.5W and 27W (4.5A to 5.4A) for 5V	
3.3V	Only used by PMC/XMC	
+3.3V_AUX	Only used to pull-up backplane system signals	
12V	Not used	
+/-12V_AUX	Only used by PMC/XMC	
Dimensions and Weight (Notes 2-5)		
Option	**Dimensions**	**Weight (grams)**
Air-cooled	per VITA46/1101.1	395
Conduction-cooled	per VITA 46/IEEE 1101.2	410
Conduction-cooled LRM	per VITA 48.1	545
RTM3-127	per VITA 46	135
Cooling Air Requirements (Note 6)		
Configuration	Dual-core 1.0GHz	
Temperature Range	-40°C to 71°C	
Air-Flow	15 CFM	

Notes:
1. Values above are estimated typical maximums.
2. The air-cooled format is designed to fit chassis with 0.8" slot pitch, but is shipped with 1" faceplates.
3. Air-cooled cards available in temperature ranges 0 and 1.*
4. Refer to Ruggedization Guidelines data sheet for more information.
5. Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The air-flow specifications are for worst case (highest power) conditions, without any PMC/XMCs installed. Curtiss-Wright can supply additional recommendations for specific power/temperature/altitude scenarios and pressure drop characteristics of the VPX3-127 support the design and testing of cooling subsystems

Table 4: OpenVPX Mapping

Supported OpenVPX/VITA 65 Profiles	127 Variant
MOD3-PAY-2F2U-16.2.3-2	VPX3-127-xxxBxxx
MOD3-PAY-1F1F2U-16.2.4-1	VPX3-127-xxxBxxx
MOD3-PAY-1F1F2U-16.2.4-3	VPX3-127-xxxBxxx
MOD3-PAY-2F2T-16.2.5-2	VPX3-127-xxxAxxx
MOD3-PER-2F-16.3.1-2	VPX3-127-xxxxxxx
MOD3-PER-1F-16.3.2-1	VPX3-127-xxxxxxx

Ruggedization Levels

Air-cooled cards are available in levels 0, 100.

Conduction-cooled cards are available in levels 100 and 200. Note that level 200 is a standard product option, where level 100 is via customer specific request.

Please see the Curtiss-Wright ruggedization guidelines fact sheet for more information.

Ordering Information

VPX3-127 - C T F B N M P

- Pin out Options:
  - Mode 0: Minimal DIO
  - Mode 1: Maximum DIO
  - Mode 2: XMC Support
  - 3:9: Reserved
- Memory:
  - 0: 512 MB DDR2, 256 MB Flash, 1 GB NAND Flash
  - 1: 1024 MB DDR2, 256 MB Flash, 1 GB NAND Flash
  - 2: 2048 MB DDR2, 256 MB Flash, 1 GB NAND Flash
  - 3:8: Reserved
- Number of Cores:
  - 0: Single-core @ 1.25 GHz
  - 1: Reserved
  - 2: Dual-core @ 1.0 GHz
  - 3:9: Reserved
  - 9: Custom
- Backplane I/F:
  - A: 2 x4 fabric ports PCIe/SRIO + 2 GbE
  - B: 2 x4 fabric ports PCIe/SRIO + 2 1000-x
  - Z: Custom configuration
- Mechanical Format:
  - 1: 0.8" pitch
  - 3: 0.85" pitch, 2-level maintenance support (covers)
- Temperature Range:
  - 0: 0° to 50° C
  - 1: -40° to 71° C
  - 2: -40° to 85° C
- Cooling Method:
  - A: Air-cooling
  - C: Conduction-cooling

Notes:
1. Not all combinations of an orderable variant are available as standard product.
2. Please consult your location sales office for further help in selecting the appropriate variant.

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Figure 4: VPX3-127 Conduction-cooled



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support

Email: support1@cwcembedded.com

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