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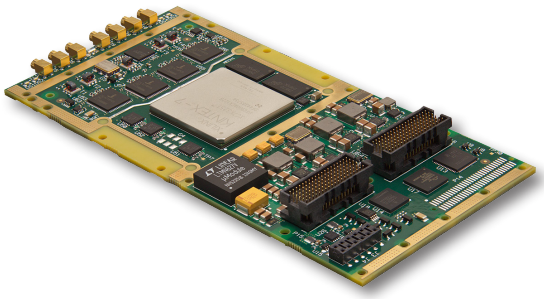
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Find the *Curtiss-Wright XF07-518* at our website: ***Click HERE***

XF07-518

4x 500 MSPS 14-bit Analog I/O XMC Xilinx® Kintex™ XC7K325T FPGA

CURTISSWRIGHTDS.COM



Key Features

- Quad channel 500 MSPS 14-bit analog inputs
- Xilinx user programmable Kintex-7 XC7K325T FPGA
- 2 x banks of 16b x 128M DDR3 SDRAM (total 512 Mbytes)
- XMC format
- VxWorks and Linux host support
- Air- and conduction-cooled variants

Applications

- Radar
- SIGINT/ELINT
- Electronic Warfare (EW)

Overview

The XF07-518 is a high speed quad channel 500 MSPS analog input XMC format mezzanine card, with a user programmable FPGA for combining data acquisition and user algorithms. The combination of direct high-speed analog I/O and next generation FPGA processing makes the XF07-518 ideal for demanding applications including radar, imaging and test equipment within commercial and defense market spaces.

The XF07-518 is a member of Curtiss-Wright's XF07 XMC family of products based on the Xilinx® Kintex®-7 XC7K325T FPGA.

Analog Input

The XF07-518 provides four synchronously sampled analog input channels connected through front panel (or bulkhead for conduction-cooled) connectors. Each analog input is AC coupled to an Intersil™ ISLA214P50 ADC and is able to sample at up to 500 MSPS.

An onboard user programmable sample clock generator is provided for a complete integrated acquisition solution. Alternatively, the sample clock can be derived from either a 10 MHz or direct RF external clock source. The choice of clock source is controlled by the Kintex-7 FPGA. An external clock is recommended for the highest performance solution.

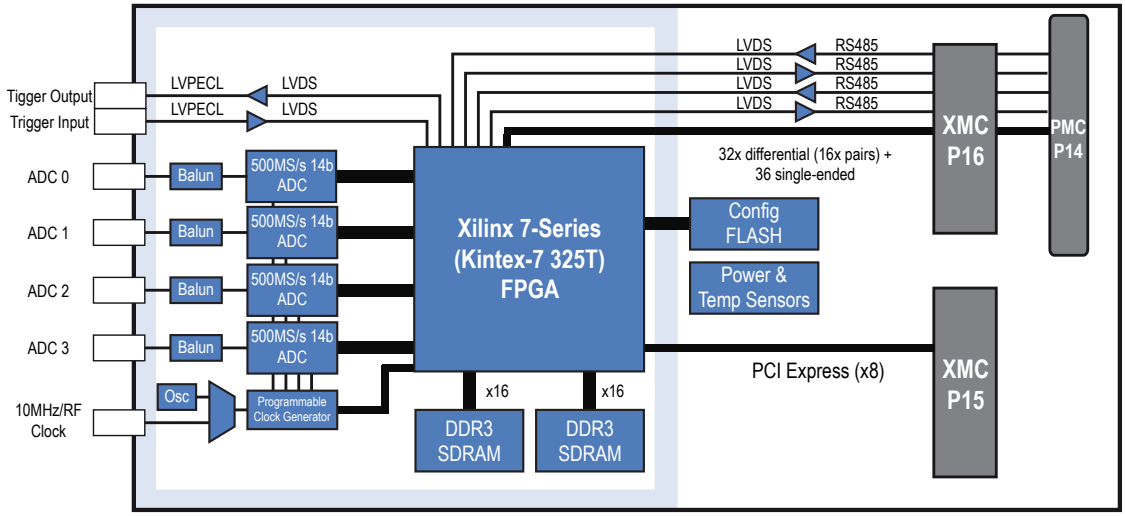


Figure 1: XF07-518 block diagram

Specifications

FPGA

- Device: Xilinx Kintex-7 K325T (speed grade 2)
- Configuration: Over PCI Express® (PCIe) interface
  - 1 Gbit Flash (FPGA boot/configuration including recovery image)
  - JTAG/ChipScope™ Pro port

FPGA resources

- Slices: 50,950
- Logic cells: 326,080
- CLB flip-flops: 407,600
- Total block RAM (Kbits): 16,020
- DSP48E1 slices: 840

Analog input (preliminary)

- Number of channels: 4, single-ended, front panel MMCX
- Sampling frequency: Up to 500 MSPS
- Full scale input: 11.5 dBm @ 105 MHz
- ADC devices: Intersil ISLA214P50
- SFDR (typ): 89 dBc @ 105 MHz
- SNR (typ): 72 dBFS @ 105 MHz
- ENOB (typ): 11.6 bits @ 105 MHz
- Input Impedance: 50 Ω, AC coupled

Clock and trigger inputs

- Clock input connector: Front panel MMCX
- Clock input: 50 Ω, AC coupled LVPECL
- Clock input frequency: 10 MHz (reference) or 80-250 MHz (RF)
- Internal clock: Programmable (derived from 10 MHz external source or internal): Si571 VCXO
- Trigger input/output: Single-ended, 50 Ω, LVPECL buffered to host FPGA

Rear I/O (build option)

- PMC/XMC digital I/O
  - 20 x differential pairs + 38 x single-ended (XMC)
  - 32 x differential pairs (PMC)
  - Note:
    - PMC and XMC digital I/O are mutually exclusive build options
    - 1 x signal is input TTL and 4 x RS-485 buffered (2 x input pairs and 2 x output pairs)
- Connector: XMC P16 or PMC P14 (build options)

Memory

- Type: DDR3 SDRAM
- Capacity:
  - Total: 512 MB
  - Arranged as two banks, each 128M x 16-bit
- Bandwidth: >2 Gbytes/sec

XMC interface

- Compliance: VITA 42.0
- XMC P15: x4/x8 PCIe

Software/HDL

- Support/Utilities
  - FusionXF development kit
  - FPGA/flash programming, diagnostics
- Host drivers
  - VxWorks
  - Linux (Fedora)
- HDL examples: Memory interfaces, PCIe, data DMA
- Acquisition: Digital receiver ADC application mode

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Xilinx Kintex-7 FPGA

The XF07-518 features a user programmable Xilinx Kintex-7 XC7K325T FPGA resource (speed grade 2, industrial temperature range). Although a Kintex-7 FPGA is a mid-range Xilinx 7-Series FPGA, it is a powerful resource compared to Virtex®-5 or even Virtex®-6 previous generation devices. See Specifications on page 2 for a summary of the onchip resource for a Kintex-7 XC7K325T device.

The FPGA configuration images can be stored in the flash memory which can be updated and controlled by the host CPU using the PCIe interface. The FPGA can be reconfigured from images indexed in the flash including a write protected recovery configuration. FPGA configuration from flash can also take advantage of AES encryption.

Multiple Memory Banks

The XF07-518 supports two banks of 128Mx16-bit DDR3 SDRAM, each directly connected to the FPGA. As each memory bank is independently connected to the FPGA, there is great flexibility in how they may be used. Each memory bank supports read or write bandwidths of >2 Gbytes/sec.

Triggers, Synchronization and Digital I/O

'Trigger In' and 'Trigger Out' signals are routed to the front panel. The functionality of these signals is dependent on the HDL code and therefore may be retargetted. Both 'Trigger In' and 'Trigger Out' are single-ended LVPECL buffered signals connected to the host FPGA. It is possible to synchronize the ADCs on multiple XF07-518s using the 'Trigger In' & 'Trigger Out' signals with appropriate HDL code; effectively the function of these signals is changed to a sync mode when this is required.

Up to 64 digital I/O signals are provided through the PMC P14 connector and directly controlled by the Kintex-7 FPGA for general purpose I/O. The majority of signals are 3.3V differential signals, but RS-485 and TTL compliant I/O is also provided. These are available for the user application and can be used for user defined functions as secondary triggers, PPS inputs or any other function. As an alternative build option to PMC P14 I/O, up to 78 digital I/O signals are provided to an XMC P16 connector. I/O to PMC P14 and XMC P16 is mutually exclusive.

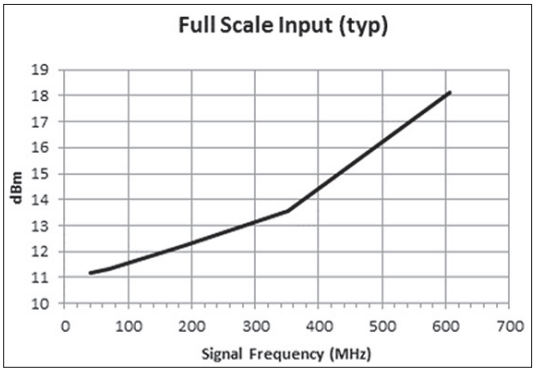


Figure 2: Full Scale Input with Sample Rate

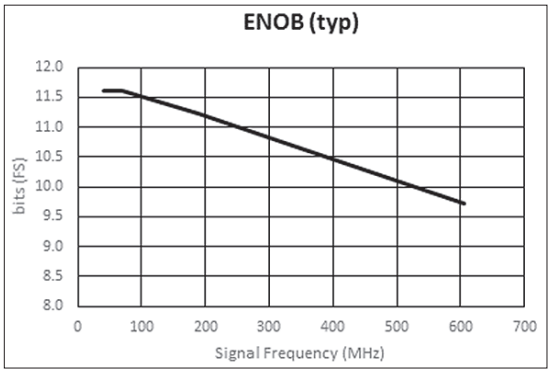


Figure 3: ENOB with Sample Rate

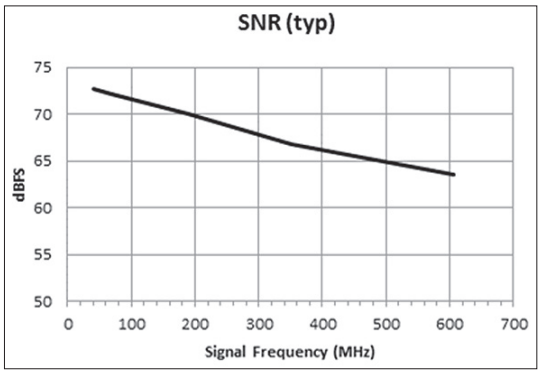


Figure 4: SNR with Sample Rate

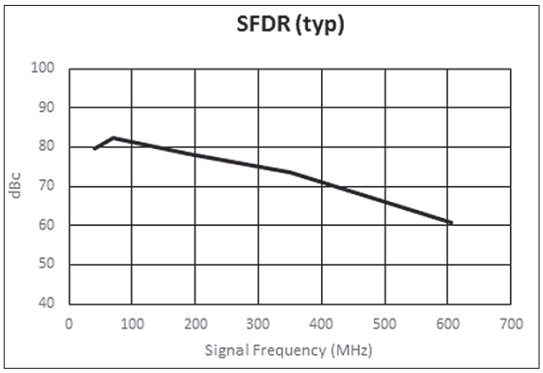


Figure 5: SFDR with Sample Rate

PCIe and Multi-GB/s I/O

The XF07-518 supports a x4/x8 PCIe Gen2 channel through the primary XMC P15 connector using the FPGA's built-in PCIe end-point block. Alternatively, the XMC P15 can be used to provide user defined protocol support over the data links, such as Aurora™ for higher bandwidth and lower latency operation. However, this mode would require customer HDL development for new modes.

FusionXF™ Software/HDL Support

Curtiss-Wright's FusionXF Development Kit includes software, HDL and utilities complete with examples for using the XF07-518. FusionXF includes a C programming language API, driver framework and sophisticated DMA support. One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively. FusionXF allows user applications to be associated with standard drivers, thereby speeding up application development.

Software utilities are provided for configuring the FPGA. These include flash programming and configuring the FPGA from one of multiple indexed images in stored in flash.

FusionXF supports VxWorks® and Fedora™ Linux® operating systems. Additional operating systems such as Windows or other distributions can be considered on request.

Rugged Build Options

A range of environmental requirements are addressed by the XF07-518 including commercial, air-cooled rugged and conduction-cooled.

TABLE 1 PMC P14 connector digital I/O pinouts

PIN	SIGNAL	SIGNAL	PIN
1	USER_LVDS_13_N (1)	USER_SE34	2
3	USER_LVDS_13_P (1)	TTL_IN	4
5	RS485OUT0_N	RS485IN0_N	6
7	RS485OUT0_P	RS485IN0_P	8
9	USER_SE32	USER_SE35	10
11	USER_SE30	USER_SE33	12
13	USER_SE28	USER_LVDS_2_N	14
15	USER_SE26	USER_LVDS_2_P	16
17	USER_SE25	USER_LVDS_4_N (1)	18
19	USER_SE27	USER_LVDS_4_P (1)	20
21	USER_SE24	USER_LVDS_3_N (1)	22
23	USER_SE22	USER_LVDS_3_P (1)	24
25	RS485OUT1_N	RS485IN1_N	26
27	RS485OUT1_P	RS485IN1_P	28
29	USER_SE20	USER_SE23	30
31	USER_SE18	USER_SE21	32
33	USER_SE19	USER_LVDS_18_N	34
35	USER_SE17	USER_LVDS_18_P	36
37	USER_SE16	USER_LVDS_17_N (1)	38
39	USER_SE14	USER_LVDS_17_P (1)	40
41	USER_SE11	USER_LVDS_20_N	42
43	USER_SE9	USER_LVDS_20_P	44
45	USER_LVDS_7_N (1)	USER_SE12	46
47	USER_LVDS_7_P (1)	USER_SE10	48
49	USER_SE7	USER_LVDS_8_N	50
51	USER_SE5	USER_LVDS_8_P	52
53	USER_LVDS_9_N	USER_SE8	54
55	USER_LVDS_9_P	USER_SE6	56
57	USER_SE1	USER_LVDS_10_N	58
59	USER_SE3	USER_LVDS_10_P	60
61	USER_LVDS_11_N	USER_LVDS_12_N (1)	62
63	USER_LVDS_11_P	USER_LVDS_12_P (1)	64

NOTE: (1) Clock capable pairs

TABLE 2 XMC P16 connector digital I/O pinouts

P16 USER DEFINED I/O						
PIN	A	B	C	D	E	F
1	USER_LVDS_13_P (1)	USER_LVDS_13_N (1)	USER_SE37	USER_LVDS_14_P	USER_LVDS_14_N	USER_SE38
2	GND	GND	USER_SE35	GND	GND	TTL_IN
3	RS485OUT0_P	RS485OUT0_N	USER_SE33	RS485IN0_P	RS485IN0_N	USER_SE34
4	GND	GND	USER_SE31	GND	GND	USER_SE32
5	USER_LVDS_1_P	USER_LVDS_1_N	USER_SE29	USER_LVDS_2_P	USER_LVDS_2_N	USER_SE30
6	GND	GND	USER_SE27	GND	GND	USER_SE28
7	USER_LVDS_3_P (1)	USER_LVDS_3_N (1)	USER_SE25	USER_LVDS_4_P (1)	USER_LVDS_4_N (1)	USER_SE26
8	GND	GND	USER_SE23	GND	GND	USER_SE24
9	RS485OUT1_P	RS485OUT1_N	USER_SE21	RS485IN1_P	RS485IN1_N	USER_SE22
10	GND	GND	USER_SE19	GND	GND	USER_SE20
11	USER_LVDS_17_P (1)	USER_LVDS_17_N (1)	USER_SE17	USER_LVDS_18_P	USER_LVDS_18_N	USER_SE18
12	GND	GND	USER_SE15	GND	GND	USER_SE16
13	USER_LVDS_19_P	USER_LVDS_19_N	USER_SE13	USER_LVDS_20_P	USER_LVDS_20_N	USER_SE14
14	GND	GND	USER_SE11	GND	GND	USER_SE12
15	USER_LVDS_7_P (1)	USER_LVDS_7_N (1)	USER_SE9	USER_LVDS_8_P	USER_LVDS_8_N	USER_SE10
16	GND	GND	USER_SE7	GND	GND	USER_SE8
17	USER_LVDS_9_P	USER_LVDS_9_N	USER_SE5	USER_LVDS_10_P	USER_LVDS_10_N	USER_SE6
18	GND	GND	USER_SE3	GND	GND	USER_SE4
19	USER_LVDS_11_P	USER_LVDS_11_N	USER_SE1	USER_LVDS_12_P (1)	USER_LVDS_12_N (1)	USER_SE2

NOTE: (1) Clock capable pairs

XF07-518 Digital Down Converter

Features

- 16-bit input
- NCO with 32-bit tuning word, 105 dB SFDR
- 18-bit coefficients
- Four independent programmable coefficient sets
- Up to 2560 filter taps
- Complex or real outputs
- Decimation of 4, 8, 16, 32, 64 or 128 (complex)
- Decimation of 2, 4, 8, 16, 32 or 64 (real)
- Output formatting to 16-bits or 24-bits
- Output spectrum can be inverted or shifted by Fo/2

Overview

The DDC option for the XF07-518 is a wideband Digital Down Converter (DDC) providing similar functionality to the GC1012B from Texas Instruments. XF07-518 are available with or without embedded DDC IP examples in configuration FLASH memory. For these variants of the XF07-518, customers can use the card without needing to develop FPGA IP. For users that wish to integrate this IP into their application, a separate DRK (DDC Resource Kit) is available. Contact Curtiss-Wright for ordering information.

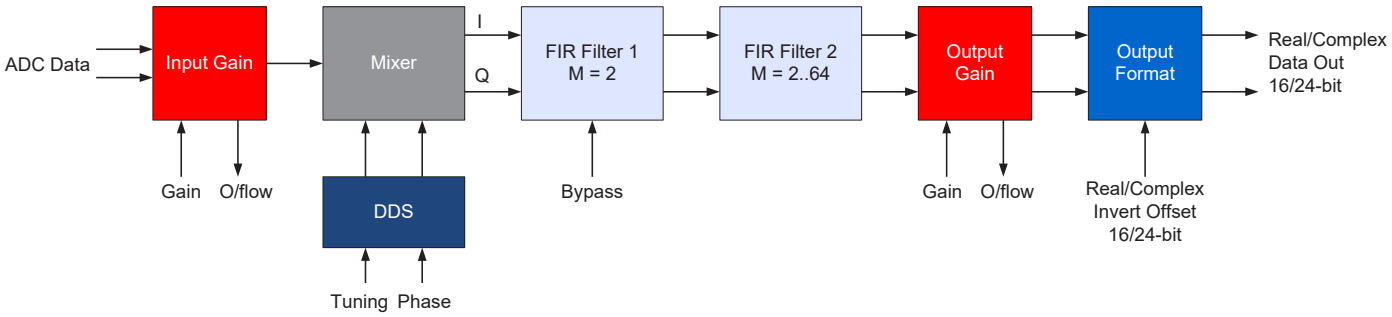


Figure 6: DDC block diagram

Input Gain

Permits scaling of the input signal by up to 48 dB with a granularity of 0.03 dB, the gain is specified by an 8-bit input with an 8-bit fractional part. The Input Gain Block has an overflow output, in the event of an overflow the output from this block saturates to the maximum positive or negative value as appropriate.

NCO

The NCO has a 32-bit accumulator and provides a 105 dB SFDR using phase dithering and interpolation. The NCO also supports a 14-bit phase offset.

Mixer

The Mixer takes a real input from the Input Gain Block and multiplies it with the Cos and –Sin inputs from the NCO to produce a complex output which is passed to the Decimating FIR filter.

Decimating FIR Filter

Decimates and filters the output of the Mixer. Consists of a fixed decimate by 2 half band filter followed by a programmable FIR filter supporting decimation rates of 2, 4, 8, 16, 32 and 64. Giving an overall decimation in the range of 4 to 128. All four sets of filter coefficients are programmable; two sets are preprogrammed with coefficients supporting passbands of 80% and 90% of the output bandwidth.

TABLE 3	Characteristics of the supplied filters	
FILTER PASSBAND* (of Fo/2)	PASSBAND RIPPLE	STOPBAND
80%	< 0.08 dB	> 93 dB
90%	< 0.5 dB	> 74 dB

*Note: Passband is defined as the point at which the filter attenuation exceeds the specified ripple.

TABLE 4 Number of taps for each of the decimation rates

DECIMATION RATE	FILTER TAPS
2	80
4	160
8	320
16	640
32	1280
64	2560

Output Gain

The amplitude of the output from the filter can be modified by 90 dB with a granularity of 0.03 dB. The Output Gain Block saturates in the event of overflow and indicates that an overflow has occurred on a status output.

Output Formatter

The output from the DDC can be real or complex, rounded to 24 or 16-bits, with the output spectrum inverted or offset by Fo/2.

TABLE 5 Resource usage

RESOURCE TYPE	RESOURCE USED	% OF KINTEX-7 K325T
DSP48E1	64	7
Slices	6200	2
BlockRAM	13	2

Note: The resource utilization is approximate and provided for guidance as it may change slightly as improvements are made to the design.

Ordering Information

TABLE 6 Board ordering information

PRODUCT NUMBER	ANALOG INPUTS	DIGITAL I/O	RUGGEDIZATION	COMMENT
XF07-518-A004040	4 x 500 MSPS x14b	PMC P14: 32 x DIFF	Air-cooled, Level 0	
XF07-518-A004060	4 x 500 MSPS x14b	XMC P16: 30 x DIFF + 38 x SE	Air-cooled, Level 0	
XF07-518-A104040	4 x 500 MSPS x14b	PMC P14: 32 x DIFF	Air-cooled, Level 100	
XF07-518-A104060	4 x 500 MSPS x14b	XMC P16: 30 x DIFF + 38 x SE	Air-cooled, Level 100	
XF07-518-C204040	4 x 500 MSPS x14b	PMC P14: 32 x DIFF	Conduction-cooled, Level 200	Requires host front panel IO
XF07-518-C204060	4 x 500 MSPS x14b	XMC P16: 30 x DIFF + 38 x SE	Conduction-cooled, Level 200	Requires host front panel IO
XF07-518-A004042	4 x 500 MSPS x14b	PMC P14: 32 x DIFF	Air-cooled, Level 0	Embedded DDC
XF07-518-A004062	4 x 500 MSPS x14b	XMC P16: 30 x DIFF + 38 x SE	Air-cooled, Level 0	Embedded DDC
XF07-518-A104042	4 x 500 MSPS x14b	PMC P14: 32 x DIFF	Air-cooled, Level 100	Embedded DDC
XF07-518-A104062	4 x 500 MSPS x14b	XMC P16: 30 x DIFF + 38 x SE	Air-cooled, Level 100	Embedded DDC
XF07-518-C204042	4 x 500 MSPS x14b	PMC P14: 32 x DIFF	Conduction-cooled, Level 200	Embedded DDC. Requires host front panel IO
XF07-518-C204062	4 x 500 MSPS x14b	XMC P16: 30 x DIFF + 38 x SE	Conduction-cooled, Level 200	Embedded DDC. Requires host front panel IO

TABLE 7 Software, HDL and Support

PRODUCT NUMBER	COMMENT
XF07-516-XFV	FusionXF for VxWorks
XF07-516-XFL	FusionXF for Linux (Intel CPU host)
XF07-516-DRK	DDC Resource Kit (DRK). HDL library for allowing DDC IP to be integrated in user programmable HDL environment (contact factory for availability)
JTAG-ZF5	JTAG adaptor module for use with Xilinx JTAG pod

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