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Data Sheet

XMC-FPGA05D

Adaptable I/O PMC/XMC with User Programmable Xilinx® Virtex®-5 FPGA



Applications

- Analog, Digital and Video data I/O
- Signal Processing
- Data Encryption

Features

- High density, FPGA controlled parallel I/O
- Range of front panel I/O personality modules (including ADC, DAC, LVDS, RS-485/422 and Camera Link)
- User programmable Xilinx® Virtex®-5 FPGA (SX95T)
- Two banks of 9MBs QDR2 SRAM memory
- Two banks of 128MB DDR2 SDRAM memory
- PMC/XMC form-factor
- VxWorks®, Linux® and Windows® host support
- Air- and Conduction-cooled variants

Benefits

- High bandwidth I/O
- Flexible and customizable I/O
- For use in deployed or commercial environments
- Industry standard form factor

Overview

The XMC-FPGA05D is a high density I/O platform, controlled by a Virtex-5 FPGA, and supported by a range of front panel I/O modules including analog I/O, RS-485/422, LVDS and Camera Link. The card can also accommodate application specific I/O schemes when used with a custom designed front panel I/O module. Non-front panel I/O is also supported through PMC P14 and XMC P15/16 I/O. The XMC-FPGA05D is a versatile FPGA processing and I/O platform for a wide range of applications including imaging, direct sensor interfacing and system control.

Xilinx Virtex-5 FPGA

The XMC-FPGA05D is centered around a user programmable Xilinx Virtex-5 SX95T FPGA resource (speed grade 2).

The FPGA configuration images can be stored in the FLASH memory and can be updated and controlled by the host using the PCI/PCI-X or PCI Express® (PCIe) interfaces. The FPGA can be reconfigured from any number of files indexed in the FLASH. Alternatively, a 'FLASH bypass' mode can be invoked which uses SRAM to temporarily store the FPGA configuration data; thus when power is removed, no trace of the configuration is left on the board – useful for secure applications. A bit stream stored in SRAM has the added benefit from faster downloads.

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Front Panel I/O

There are 138 signals connected directly from the FPGA to a 180-way Samtec connector near the front panel. These lines are routed so that they may be used as single-ended signals or differential pairs. The FPGA I/O signals are banked, with four banks being used at the front panel connector. Each bank is independently configurable to 2.5V or 3.3V signaling.

Table 1: Front panel I/O Modules supported by the XMC-FPGA05D

Module	Function	Notes
LVDS-MOD3	32 LVDS pairs	68-way SCSI-3 style front panel connector
LVDS-MOD4	64 LVDS pairs	152-way high-density front panel connector
LVDS-MOD5	2x 26 LVDS pairs	Two 80-way front panel connectors
ADC-MOD2	Dual 125MSPS, 14-bit ADC	AC coupled, front panel MMCX connector
DAC-MOD2	Dual 210MSPS, 14-bit DAC	AC coupled, front panel MMCX connector
RS485-MOD2	33x RS-485/422/422B channels	VHDCI - SCSI-5 style front panel connector
CAML-MOD3	Camera Link	Supports Base, Medium and Full mode

Multiple Memory Banks

The XMC-FPGA05D supports two banks of 64Mx16-bit (128MB) DDR2 SDRAM, each directly connected to the FPGA. In support of DSP functions, two banks of 4Mx18-bit (9MB) QDR2-SRAM also connect directly to the FPGA using independent interfaces. As each memory bank is independently connected to the FPGA, there is great flexibility in how they may be used. The XMC-FPGA05D will also support larger memory devices as they become available.

PCI/PCI-X, PCI Express & Multi-GB/s I/O

The XMC-FPGA05D routes two x8 Virtex-5 FPGA RocketIO™ HSS ports to the XMC P15 and P16 connectors allowing the board to be used with a choice of protocols and connectivity. The XMC-FPGA05D supports a x8/x4 PCIe channel through the primary XMC P15 connector using the Virtex-5 FPGA's built-in PCIe end-point block. Alternatively, the XMC P15 and P16 connectors can be used to provide user defined protocol support over the data links, such as Aurora™ for higher bandwidth, lower latency operation. The XMC-FPGA05D includes a PCI/PCI-X interface to the PMC connectors, supporting up to 64-bit, 133MHz PCI-X operation. An on-board switch is used to determine whether the board powers up using the PCI-X or PCIe interface.

PMC P14 Digital I/O

The XMC-FPGA05D is equipped with 64-bit non-front panel digital I/O that can be used as high-speed differential or single-ended I/O including LVDS. The 64-bit digital I/O is provided through the PMC P14 connector and it is directly connected to, and controlled by, the FPGA. These lines are routed to support both 50 Ohm single-ended or 100 Ohm differential operation so that they may be configured as 32 LVDS pairs, 20 LVDS pairs plus 24 single-ended lines or 64 single-ended lines.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities complete with examples for using the XMC-FPGA05D. FusionXF includes a C programming language API, driver framework and sophisticated DMA support. One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively.

Reference software/HDL illustrates how to interface to on-board devices such as PCI-X, PCIe, DDR2 SDRAM and XMC interfaces. Front panel I/O modules usually include their own examples.

Software utilities are provided for configuring the FPGA by the host over either the PCI-X or PCIe interfaces. These include FLASH programming and configuring the FPGA from one of many indexed images in FLASH. The FPGA may also be configured by SRAM using the 'FLASH bypass' mode or ChipScope™ Pro/JTAG interface. Host operating systems supported by the FusionXF suite include Windows, VxWorks and Linux.





Rugged Build Options

A range of environmental requirements are addressed by the XMC-FPGA05D including commercial, air-cooled rugged and conduction-cooled. For conduction-cooled applications, the host board must be able to incorporate any front panel I/O connections. Depending on the application, a suitable heatsink will be required as the FPGA is capable of dissipating high power for demanding applications.

Table 2: PMC P14 connector digital I/O pinouts

P14 User Defined IO			
Pin	Signal	Signal	Pin
1	USER_LVDS_N_0	USER_LVDS_N_1	2
3	USER_LVDS_P_0	USER_LVDS_P_1	4
5	USER_LVDS_N_2	USER_LVDS_N_3	6
7	USER_LVDS_P_2	USER_LVDS_P_3	8
9	USER_LVDS_N_4	USER_LVDS_N_5	10
11	USER_LVDS_P_4	USER_LVDS_P_5	12
13	USER_LVDS_N_6	USER_LVDS_N_7	14
15	USER_LVDS_P_6	USER_LVDS_P_7	16
17	USER_LVDS_N_8	USER_LVDS_N_9	18
19	USER_LVDS_P_8	USER_LVDS_P_9	20
21	USER_LVDS_N_10	USER_LVDS_N_11	22
23	USER_LVDS_P_10	USER_LVDS_P_11	24
25	USER_LVDS_N_12	USER_LVDS_N_13	26
27	USER_LVDS_P_12	USER_LVDS_P_13	28
29	USER_LVDS_N_14	USER_LVDS_N_15	30
31	USER_LVDS_P_14	USER_LVDS_P_15	32
33	USER_LVDS_N_16	USER_LVDS_N_17	34
35	USER_LVDS_P_16	USER_LVDS_P_17	36
37	USER_LVDS_N_18	USER_LVDS_N_19	38
39	USER_LVDS_P_18	USER_LVDS_P_19	40
41	USER_LVDS_N_20	USER_LVDS_N_21	42
43	USER_LVDS_P_20	USER_LVDS_P_21	44
45	USER_LVDS_N_22	USER_LVDS_N_23	46
47	USER_LVDS_P_22	USER_LVDS_P_23	48
49	USER_LVDS_N_24	USER_LVDS_N_25	50
51	USER_LVDS_P_24	USER_LVDS_P_25	52
53	USER_LVDS_N_26	USER_LVDS_N_27	54
55	USER_LVDS_P_26	USER_LVDS_P_27	56
57	USER_LVDS_N_28	USER_LVDS_N_29	58
59	USER_LVDS_P_28	USER_LVDS_P_29	60
61	USER_LVDS_N_30	USER_LVDS_N_31	62
63	USER_LVDS_P_30	USER_LVDS_P_31	64

Build Options

A number of build options are available for the XMC-FPGA05D including:

- Type of FPGA
- I/O module fitted
- PMC only (no XMC connectors)
- XMC (P15 or P15/P16 fitted)
- Memory
- Ruggedization level

Table 3: Primary XMC P15 connector pin definition

Primary XMC P15 Connector Pin Definition						
	A	B	C	D	E	F
1	TX00+	TX00-	3.3V	TX01+	TX01-	VPWR
2	GND	GND	TRST#	GND	GND	MRST1#
3	TX02+	TX02-	3.3V	TX03+	TX03-	VPWR
4	GND	GND	TCK	GND	GND	NC[2]
5	TX04+	TX04-	3.3V	TX05+	TX05-	VPWR
6	GND	GND	TMS	GND	GND	NC[4]
7	TX06+	TX06-	3.3V	TX07+	TX07-	VPWR
8	GND	GND	TDI	GND	GND	NC[4]
9	NC	NC	NC	NC	NC	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	RX00+	RX00-	MBIST#	RX01+	RX01-	VPWR
12	GND	GND	GA1	GND	GND	GND[1]
13	RX02+	RX02-	3.3V_AUX	RX03+	RX03-	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	RX04+	RX04-	NC	RX05+	RX05-	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	RX06+	RX06-	NC	RX07+	RX07-	NC
18	GND	GND	NC	GND	GND	NC
19	NC	NC	NC[3]	NC	NC	NC

Notes:
1. This is the MPRESENT# signal to the carrier card.
2. The module does not implement the MRSTO# signal.
3. The module does not implement the WAKE# signal.
4. The module is not connected to the +-12V rails from the carrier.





Table 4: Secondary XMC P16 connector pin definition

P16 Connector I/O						
	A	B	C	D	E	F
1	TX08+	TX08-	NC	TX09+	TX09-	NC
2	GND	GND	NC	GND	GND	NC
3	TX10+	TX10-	NC	TX11+	TX11-	NC
4	GND	GND	NC	GND	GND	NC
5	TX12+	TX12-	NC	TX13+	TX13-	NC
6	GND	GND	NC	GND	GND	NC
7	TX14+	TX14-	NC	TX15+	TX15-	NC
8	GND	GND	NC	GND	GND	NC
9	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
11	RX08+	RX08-	NC	RX09+	RX09-	NC
12	GND	GND	NC	GND	GND	NC
13	RX10+	RX10-	NC	RX11+	RX11-	NC
14	GND	GND	NC	GND	GND	NC
15	RX12+	RX12-	NC	RX13+	RX13-	NC
16	GND	GND	NC	GND	GND	NC
17	RX14+	RX14-	NC	RX15+	RX15-	NC
18	GND	GND	NC	GND	GND	NC
19	NC	NC	NC	NC	NC	NC

Figure 1: XMC-FPGA05D

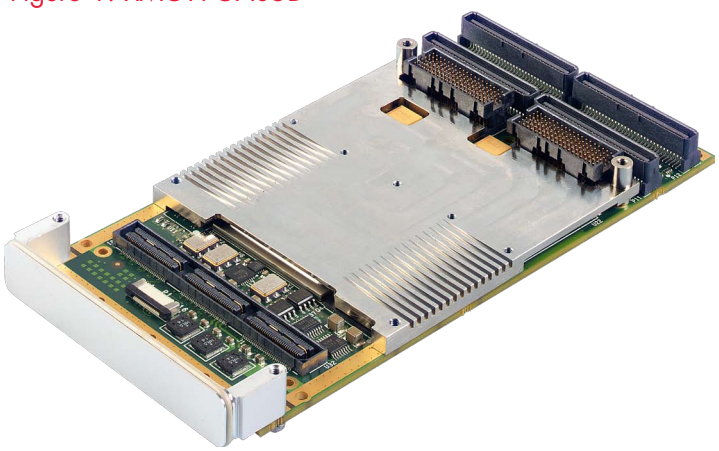


Table 5: Specifications

FPGA	
Device	Xilinx Virtex-5 SX95T Speed grade 2
Configuration	Over PCI, PCI-X or PCIe interface - 1Gbit FLASH (FPGA boot/configuration including rescue image) - FLASH bypass - images stored in SRAM - JTAG/ChipScope pro port
SRAM Memory	
Type	QDR2 SDRAM
Capacity	Total: 18MB Arranged as two banks, each 9M x 18-bit
SDRAM Memory	
Type	DDR2 SDRAM
Capacity	Total: 256MB Arranged as two banks, each 128M x 16-bit
Front Panel I/O	
Connector	180 way Samtec QSH-090-01-L-D-A
Supports	Front panel I/O modules for analog or digital I/O
PCI and PCI-X Interface	
PCI Compliance	32/64-bit PCI 33/66MHz, 32/64-bit PCI-X 66/100/133MHz Master/slave/DMA, Interrupt support 3.3V VIO only
PMC P14 User I/O	64-bit I/O arranged as 32 differential pairs connected directly to the FPGA
XMC Interface	
Compliance	VITA 42.0
XMC P15	8x RocketIO GTP @ up to 3.75GB/s or x4/x8 PCIe release 1.1
XMC P16	8x RocketIO GTP @ up to 3.75GB/s
Software/HDL	
Host Drivers	Windows XP, VxWorks, Linux
Support/Utilities	FusionXF development kit FPGA/FLASH programming, diagnostics
HDL examples	Memory interfaces, PCI-X, PCIe, data DMA
Miscellaneous	
Weight	TBA
Power	TBA
MTBF	TBA





Table 6:
Environmental Specifications

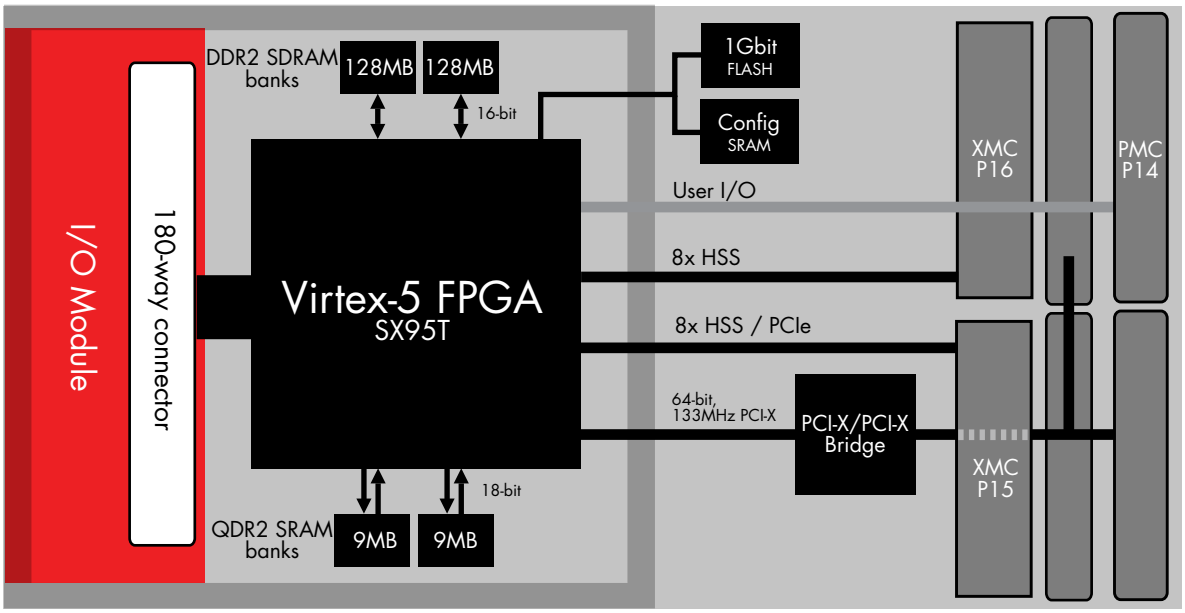
		Commercial	Rugged	
			Air-cooled	Conduction-cooled
			Level 100[1]	Level 100[1]
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow)[2]	-40°C to +70°C (20 CFM air flow)[2]	-40°C to +70°C (Card Edge Temp)[3]
	Non-Operational	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C
Vibration	Operational (Random)	-	0.04g2/Hz	0.1g2/Hz
Shock	Operational	-	30g peak, 11ms half sine	40g peak, 11ms half sine
Humidity	Operational	5-95% non-condensing	Up to 95%	Up to 95%
Altitude[4]	Operational	-	-1,500 to 60,000ft	-1,500 to 60,000ft
Conformal Coating[5]		No	Yes	Yes

Notes
1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate should be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. http://humiseal.com for details)

*While the XMC-FPGA05D is designed to meet these environmental requirements, formal qualification testing has not been performed to these levels. Please contact your local sales representative to discuss your program specific requirements.



Figure 2: XMC-FPGA05D Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

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Email: sales@cwcembedded.com

For technical support, please visit:

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