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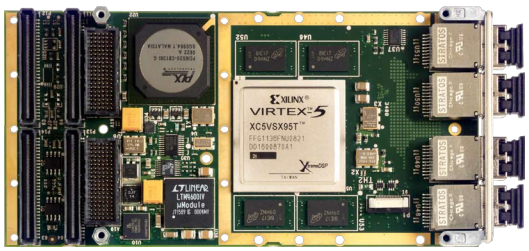




Data Sheet

XMC-FPGA05F

Programmable Xilinx® Virtex®-5 FPGA PMC/XMC with Quad Fiber-optics



Applications

- Remote Sensor Interface
- Data Recorders
- Distributed Processing Interconnect
- Protocol Converter
- Data Encryption

Features

- Up to four fiber-optic transceivers
- User programmable Xilinx® Virtex®-5 FPGA (SX95T)
- Four banks of DDR SDRAM memory
- PMC/XMC form factor (HSS links or PCI Express®)
- VxWorks®, Linux® and Windows® host support
- Commercial and rugged build options

Benefits

- Fiber-optic I/O and high performance processing in a single product
- High bandwidth I/O
- For use in deployed or commercial environments
- Industry standard form factor

Overview

Incorporating quad fiber-optic transceivers with a user programmable Xilinx Virtex-5 FPGA, the XMC-FPGA05F XMC/PMC module combines data processing and I/O in a single module. The FPGA is closely coupled to all interfaces to minimize data bottlenecks.

The XMC-FPGA05F can be used for a wide range of tasks including remote sensor I/O, data recording and linking systems in real-time. The FPGA can be used to implement custom protocols, data encryption or a network processor.

Xilinx Virtex-5 FPGA

The XMC-FPGA05F is designed to be a user programmable FPGA resource and is fitted with a Xilinx Virtex-5 SX95T FPGA (contact Curtiss-Wright for availability of other FPGA variants) which is optimized for a high ratio of DSP blocks to standard logic blocks to support high performance signal processing.

The FPGA configuration can be updated and controlled by the host across the PCI/PCI-X or PCI Express (PCIe) interfaces using the FLASH memory to store images. The host issues commands over the PCI/PCIe interface to cause FPGA reconfiguration from any of the stored images. A 'FLASH bypass' mode can be invoked which uses temporary storage in SRAM, instead of FLASH, to provide the FPGA configuration. A bit stream stored in SRAM benefits from faster downloads while bypassing non-volatile storage - useful for secure applications.

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Fiber-optic I/O

Up to four full duplex 'low-rider' Stratos Optical Technologies fiber-optic transceivers can be fitted to the XMC-FPGA05F for front panel connections. The transceivers can be supplied in frequencies ranging from 1.0625 to over 3GB/s with single and multi-mode options. Each transceiver is driven directly by an FPGA RocketIO™ high-speed serial (HSS) link and gives the developer full control over the fiber-optic data protocol. The flexibility of the XMC-FPGA05F even allows different protocols on different channels, such as Serial FPDP (sFPDP) and Aurora™, to be used at the same time (note there are some restrictions on concurrently using several different transceiver frequencies). The XMC-FPGA05F has a choice of on-board clock sources and, together with flexible multipliers within the Virtex-5 FPGA, allows most major signaling frequencies to be achieved in the standard product. There are also provisions for fitting a custom oscillator as a build option if it is required.

Table 1: Example signalling frequencies supported by the XMC-FPGA05F clock sources

Speed	Protocol	Clock Source
3.125GB/s	Serial RapidIO type 3, XAUI, Aurora	125MHz
2.5GB/s	Serial RapidIO type 2, Aurora, sFPDP	125MHz
2.125GB/s	2x Fibre Channel, Aurora, sFPDP	106.25MHz
1.25GB/s	1x Gigabit Ethernet, Aurora	125MHz
1.0625GB/s	1x Fibre Channel, Aurora, sFPDP	106.25MHz

Multiple Memory Banks

The XMC-FPGA05F features four banks of DDR2 SDRAM connected to and controlled by the FPGA. The memory banks are available to the developer to use for any purpose. Each memory bank can, for example, be associated with each of the four fiber-optic data streams as large independent data buffers dedicated to each channel, used for look-up tables or DSP processing. Each of the SDRAM banks has a capacity of 128MB (higher capacity options may be available in the future) and provides a 16-bit data path.

PCI/PCI-X, PCI Express & Multi-GB/s I/O

The XMC-FPGA05F includes a PCI/PCI-X interface, supporting up to 133MHz operation, and a PCIe interface. Depending on the interface being used, the board provides at least four DMA controllers.

The PCIe interface uses the Virtex-5 FPGA's RocketIO HSS transceivers and an embedded end-point controller, which is a hard IP block within the Virtex-5 FPGA. The built-in PCIe end-point block supports x4 or x8 lane communications, but can be bypassed to support other protocols like Aurora, sFPDP or Serial RapidIO® (SRIO). Protocols like Aurora provide low latency communications at high-speed and can be used as either x1, x4 or x8 wide data paths.

Digital I/O

Although the XMC-FPGA05F is intended for high-speed serial I/O and FPGA processing applications, it is also equipped with 64-bit digital I/O that can be used as high-speed differential or single-ended I/O including LVDS. The 64-bit digital I/O is provided through either the board's PMC P14 or XMC P16 connectors connected directly to the FPGA. The choice of P14 or P16 connector I/O is defined through a build option. See the PMC P14 and XMC P16 table for details on the connector pinouts.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities complete with examples for using the XMC-FPGA05F. FusionXF is a common environment used across Curtiss-Wright's Virtex-5 FPGA-based family of products. FusionXF includes a C-API, driver framework and sophisticated DMA support. One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA easily and effectively.

Example software/HDL illustrates how to interface to on-board devices such as fiber-optics, PCI, PCIe, DDR2 SDRAM and XMC interfaces.

Software utilities are provided for configuring the FPGA. These include FLASH programming and commands to configure the FPGA from a given image in FLASH. The





FPGA may also be configured via a 'FLASH bypass' mode or ChipScope™ Pro/JTAG interface. Host operating systems supported by the FusionXF suite includes Windows, VxWorks and Linux.

Rugged Build Options

A range of environmental requirements are addressed by the XMC-FPGA05F including commercial, air-cooled rugged and conduction-cooled. For conduction-cooled applications, the host board must be able to incorporate front panel I/O connections. Depending on the application, a suitable heatsink may be required as the FPGA is capable of dissipating high power for demanding applications.

Build Options

A number of build options are available for the XMC-FPGA05F including:

- Type of FPGA
- Number of transceivers
- Type of transceivers
- PMC only (no XMC connectors)
- XMC (P15 or P15 and P16 fitted)
- Memory
- Custom clock speed
- Ruggedization level

Table 2: PMC P14 connector digital I/O pinouts

P14 user defined IO			
Pin	Signal	Signal	Pin
1	USER_LVDS_N_0	USER_LVDS_N_1	2
3	USER_LVDS_P_0	USER_LVDS_P_1	4
5	USER_LVDS_N_2	USER_LVDS_N_3	6
7	USER_LVDS_P_2	USER_LVDS_P_3	8
9	USER_LVDS_N_4	USER_LVDS_N_5	10
11	USER_LVDS_P_4	USER_LVDS_P_5	12
13	USER_LVDS_N_6	USER_LVDS_N_7	14
15	USER_LVDS_P_6	USER_LVDS_P_7	16
17	USER_LVDS_N_8	USER_LVDS_N_9	18
19	USER_LVDS_P_8	USER_LVDS_P_9	20
21	USER_LVDS_N_10	USER_LVDS_N_11	22
23	USER_LVDS_P_10	USER_LVDS_P_11	24
25	USER_LVDS_N_12	USER_LVDS_N_13	26
27	USER_LVDS_P_12	USER_LVDS_P_13	28
29	USER_LVDS_N_14	USER_LVDS_N_15	30
31	USER_LVDS_P_14	USER_LVDS_P_15	32
33	USER_LVDS_N_16	USER_LVDS_N_17	34
35	USER_LVDS_P_16	USER_LVDS_P_17	36
37	USER_LVDS_N_18	USER_LVDS_N_19	38
39	USER_LVDS_P_18	USER_LVDS_P_19	40
41	USER_LVDS_N_20	USER_LVDS_N_21	42
43	USER_LVDS_P_20	USER_LVDS_P_21	44
45	USER_LVDS_N_22	USER_LVDS_N_23	46
47	USER_LVDS_P_22	USER_LVDS_P_23	48
49	USER_LVDS_N_24	USER_LVDS_N_25	50
51	USER_LVDS_P_24	USER_LVDS_P_25	52
53	USER_LVDS_N_26	USER_LVDS_N_27	54
55	USER_LVDS_P_26	USER_LVDS_P_27	56
57	USER_LVDS_N_28	USER_LVDS_N_29	58
59	USER_LVDS_P_28	USER_LVDS_P_29	60
61	USER_LVDS_N_30	USER_LVDS_N_31	62
63	USER_LVDS_P_30	USER_LVDS_P_31	64

Table 3: XMC P16 connector digital I/O pinouts

P16 user defined I/O						
	A	B	C	D	E	F
1	USER_LVDS_P_12	USER_LVDS_N_12	NC	USER_LVDS_P_13	USER_LVDS_N_13	NC
2	GND	GND	NC	GND	GND	NC
3	USER_LVDS_P_14	USER_LVDS_N_14	NC	USER_LVDS_P_15	USER_LVDS_N_15	NC
4	GND	GND	NC	GND	GND	NC
5	USER_LVDS_P_0	USER_LVDS_N_0	NC	USER_LVDS_P_1	USER_LVDS_N_1	NC
6	GND	GND	NC	GND	GND	NC
7	USER_LVDS_P_2	USER_LVDS_N_2	NC	USER_LVDS_P_3	USER_LVDS_N_3	NC
8	GND	GND	USER_LVDS_N_21	GND	GND	USER_LVDS_N_20
9	USER_LVDS_P_4	USER_LVDS_N_4	USER_LVDS_P_21	USER_LVDS_P_5	USER_LVDS_N_5	USER_LVDS_P_20
10	GND	GND	USER_LVDS_N_23	GND	GND	USER_LVDS_N_22
11	USER_LVDS_P_16	USER_LVDS_N_16	USER_LVDS_P_23	USER_LVDS_P_17	USER_LVDS_N_17	USER_LVDS_P_22
12	GND	GND	USER_LVDS_N_25	GND	GND	USER_LVDS_N_24
13	USER_LVDS_P_18	USER_LVDS_N_18	USER_LVDS_P_25	USER_LVDS_P_19	USER_LVDS_N_19	USER_LVDS_P_24
14	GND	GND	USER_LVDS_N_27	GND	GND	USER_LVDS_N_26
15	USER_LVDS_P_6	USER_LVDS_N_6	USER_LVDS_P_27	USER_LVDS_P_7	USER_LVDS_N_7	USER_LVDS_P_26
16	GND	GND	USER_LVDS_N_29	GND	GND	USER_LVDS_N_28
17	USER_LVDS_P_8	USER_LVDS_N_8	USER_LVDS_P_29	USER_LVDS_P_9	USER_LVDS_N_9	USER_LVDS_P_28
18	GND	GND	USER_LVDS_N_31	GND	GND	USER_LVDS_N_30
19	USER_LVDS_P_10	USER_LVDS_N_10	USER_LVDS_P_31	USER_LVDS_P_11	USER_LVDS_N_11	USER_LVDS_P_30



Serial FPDP

Serial Front Panel Data Port (sFPDP) is an open standard (ANSI/VITA 17.1-2003) with broad appeal in the industry to users of remote subsystems and sensors.

Data is transferred over a 2.5Gbit/s link using a simple point to point protocol which is both low overhead and deterministic: resulting in sustained data throughputs of 247MB/s.

The XMC-FPGA05F XMC/PMC module can be supplied preconfigured to support four independent channels of sFPDP data through the front panel fiber optic transceivers.

The sFPDP link_core includes the PLL, the MGT and registers for control and configuration. To ensure smooth dataflow, each incoming channel is buffered using an independent 128MB DDR2 SDRAM block as a FIFO. For transmitted data, 64KB BlockRAM FIFOs are used. Data movement between the host card and the XMC-FPGA05F is via DMA through PCI-X or PCI Express.

The HDL for the application may also be supplied as a sFPDP IP core allowing developers to modify functionality or add data processing as part of the application within the FPGA on the XMC-FPGA05F.

In either case, the application HDL presents a capability list which is fully compliant with the FusionXF SDK allowing developers to use the standard software development tools supplied with the board for development purposes. As part of the package, the preconfigured board and the IP core is supplied with example software source code to provide an easy jump off point to customized software. The IP core is supplied with VHDL source code and testbench for HDL development.

Figure 1: Simplified sFPDP Core Dataflow Block Diagram

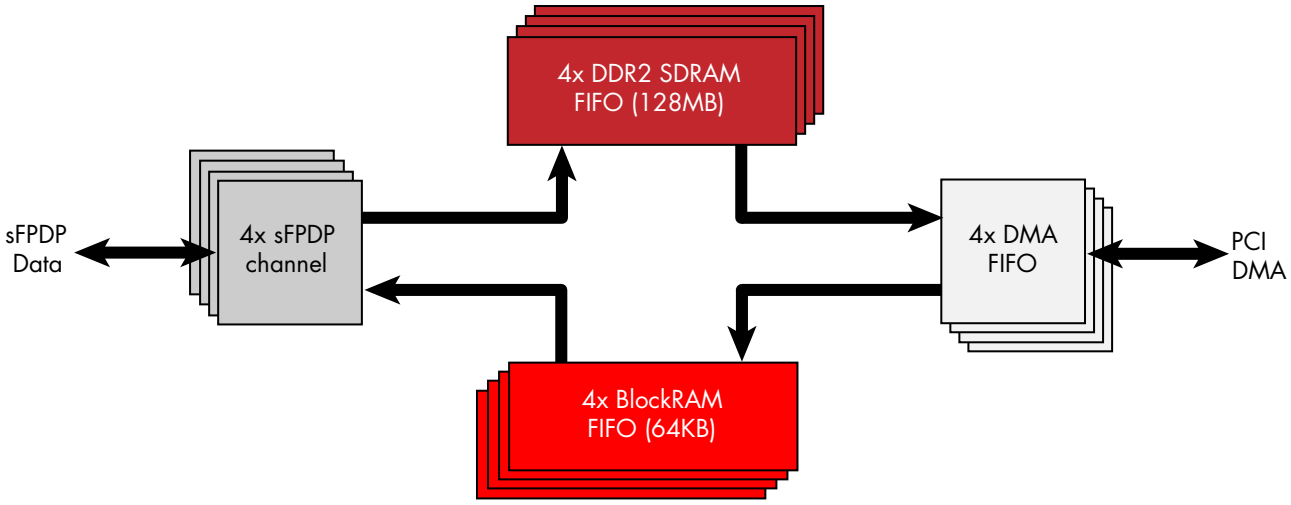






Table 4: Specifications

FPGA	
Device	Xilinx Virtex-5 SX95T Speed grade 2
Configuration	Over PCI, PCI-X or PCIe interface - 1Gbit FLASH (FPGA boot/configuration including rescue image) - FLASH bypass - images stored in SRAM - JTAG/ChipScope pro port
Memory	
Type	DDR2 SDRAM
Capacity	Total: 512MB Arranged as four banks, each 64M x 16-bit
Fiber-optic Interface	
Number of Transceivers	2 or 4 full duplex transceivers connected to FPGA RocketIO HSS
Connector	LC (contact Curtiss-Wright for alternatives) single-mode and multi-mode
Transceivers	2.5 and 3.125GB/s 850nm, multi-mode Contact Curtiss-Wright for alternative speeds and single-mode
PCI and PCI-X Interface	
PCI Compliance	PCI 33/66MHz, PCI-X 66/100/133MHz Master/slave/DMA, Interrupt support 3.3V VIO only
PMC P14 User I/O	64-bit I/O arranged as 32 differential pairs connected directly to the FPGA (note this is a mutually exclusive build option with XMC P16 I/O)

XMC Interface	
Compliance	VITA 42.0
XMC P15	8x RocketIO GTP @ up to 3.75GB/s (LXT/SXT) or x4/x8 PCIe release 1.1
XMC P16	64-bit I/O compliant with VITA 46.9 X20d24s connected directly to the FPGA (note this is a mutually exclusive build option with XMC P16 I/O)
Software/HDL	
Host Drivers	Windows XP, VxWorks, Linux
Support/Utilities	FusionXF development kit FPGA/FLASH programming, diagnostics
HDL examples	Fiber-optic I/O (RocketIO), memory interfaces, PCI-X, PCIe, data DMA
Miscellaneous	
Weight	TBA
Power	TBA
MTBF	TBA

Table 5: Environmental Specifications

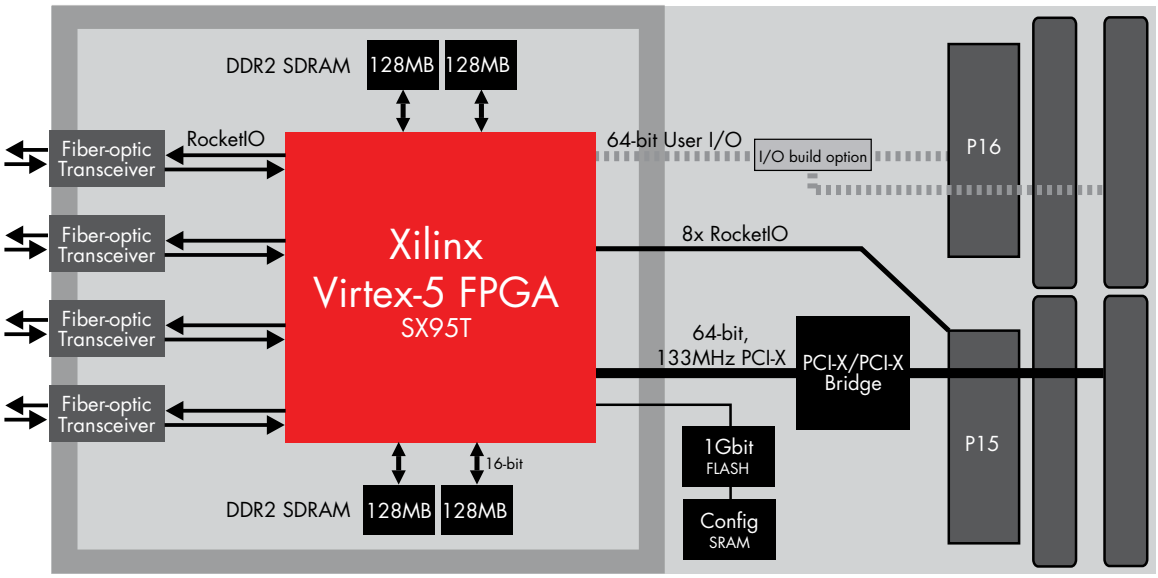
		Commercial	Rugged	
			Air-cooled	Conduction-cooled
			Level 100[1]	Level 100[1]
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow)[2]	-40°C to +70°C (20 CFM air flow)[2]	-40°C to +70°C (Card Edge Temp)[3]
	Non-Operational	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C
Vibration	Operational (Random)	-	0.04g2/Hz	0.1g2/Hz
Shock	Operational	-	30g peak, 11ms half sine	40g peak, 11ms half sine
Humidity	Operational	5-95% non-condensing	Up to 95%	Up to 95%
Altitude[4]	Operational	-	-1,500 to 60,000ft	-1,500 to 60,000ft
Conformal Coating[5]		No	Yes	Yes

Notes
1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate should be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. http://humiseal.com for details)_

*While the XMC-FPGA05F is designed to meet these environmental requirements, formal qualification testing has not been performed to these levels. Please contact your local sales representative to discuss your program specific requirements.



Figure 2: XMC-FPGA05F Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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