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PRODUCT DATASHEET



PMC-440 ProWare FPGA Module & ProWare Design Kit

FPGA I/O Interfacing and DSP Pre-Processing PMC Module and Design Kit



Features

Xilinx Virtex-II Pro™ Platform FPGA (XC2VP20 or XC2VP40)

- 64-bit, 66MHz PCI interface (tracking provision for PCI-X)
- Four RocketIO™ transceivers to front-panel connector offering up to 1.6 GB/sec aggregate peak throughput
- Four RocketIO transceivers to Pn4 connector offering up to 1 GB/sec aggregate peak throughput
- 48 LVDS/LVTTL to Pn4 connector
- 30 LVDS/LVTTL I/O to front-panel connector
- 256 Mbytes of 32-bit DDR266 SDRAM
- Temperature sensor
- Current sensor
- Indicator LEDs
- Support for ChipScope Pro and JTAG processor debug interfaces
- ProWare Design Kit (PDK) offers a library of IP modules, simulation testbench files, an example design, VxWorks driver, documentation, JTAG cable, and a loopback cable
- Range of air- and conduction-cooled versions available

Overview

The PMC-440 ProWare PMC module provides systems integrators with a powerful, easy-to-use means to capture EO/IR and radar inputs, interface to legacy system elements, and perform sensor data pre-processing. The ProWare module offers flexibility with its choice of I/O options that include LVDS, LVTTL, and RocketIO. Ease-of-use is provided via a comprehensive ProWare Design Kit (PDK) that includes a library of IP modules, simulation testbench files, a reference design, and full documentation.

For sensor data preprocessing, the ProWare module with VP40 FPGA offers the power of up to 192 18x18 multipliers for a theoretical maximum of over 20 billion operations per second to apply to DSP operations such as FFTs and digital filters. The PMC-440 ProWare PMC is an ideal front-end interface/processing module for products such as CWCEC's VME SBCs such as the 181x and Rhino/Raptor series, CompactPCI SBCs such as the 122 and G4C, and the CHAMP-AV, CHAMP-FX, and Manta series of multi-computing products.

PMC-440 FPGA Capability

The PMC-440 ProWare module comes with either a Xilinx XC2VP20 or VP40 Virtex II Pro FPGA that offers the following features:

- High-performance "-6" speed grade, example performance attributes include:
  - > max clock frequency of 420 MHz (using DCM outputs)
  - > 16-bit adder up to 334 MHz
  - > 18-bit x 18-bit multiplier up to 147 MHz
  - > max device pad-to-pad input setup time/hold time of .26/.29 nsec
- I/O connectivity:
  - > 48 LVDS/LVTTL I/Os to Pn4 connector
  - > 30 LVDS/LVTTL I/O to front panel (air-cooled modules only)
  - > 4 RocketIO transceivers to Pn4 connector, configured for 625 Mbits/sec or 1.25 Gbits/sec operation
  - > 4 RocketIO transceivers to front panel, configured for 1.0 or 2.0 Gbits/sec operation (air-cooled modules only)
- Extensive logic resources (see Table 1 - next page)

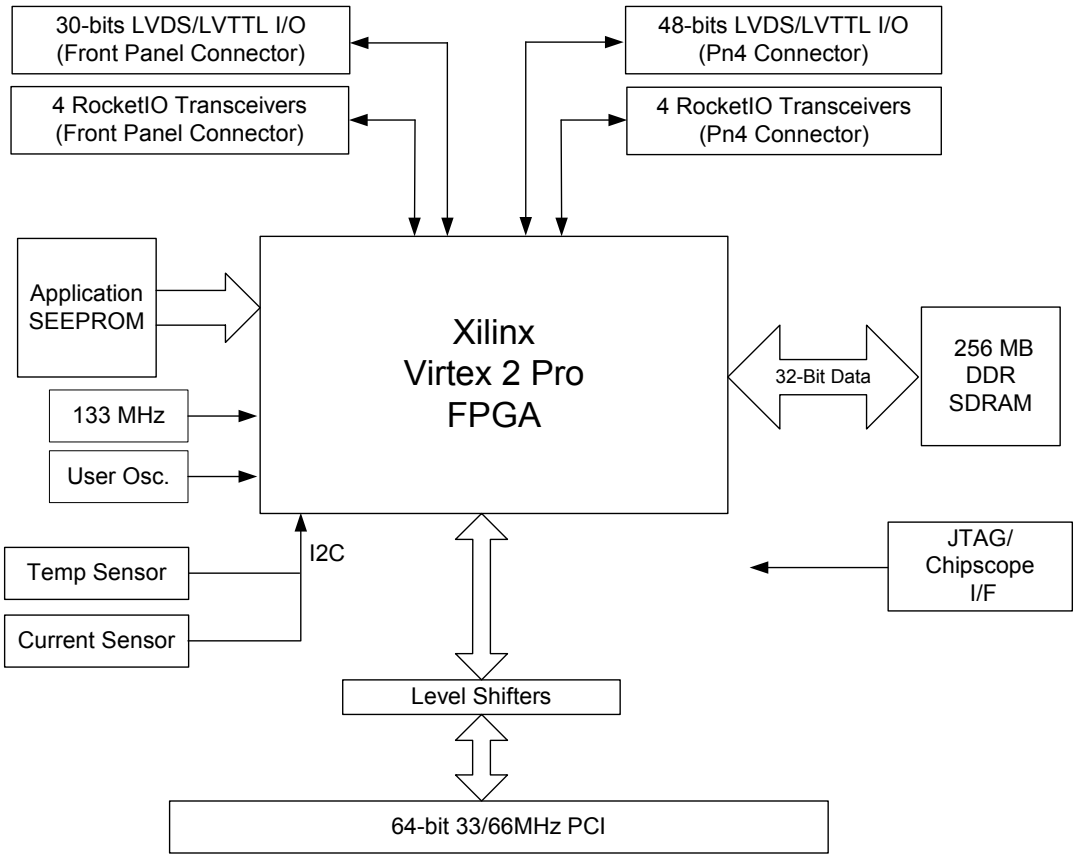
Table 1: PMC-440 ProWare Logic Resources

Device	Logic Slices	Total Block RAM(Kbits, (Blocks))	18 x 18 Multipliers	Digital Clock Management Blocks	Supported RocketIO Transceivers
XC2VP20	9,280	1,585, (88)	88	8	8
XC2VP40	19,392	3,456, (192)	192	8	8

The 440 includes a Parallel EEPROM for FPGA configuration. The configuration FPGA is initially programmed with a CWCEC default image that provides an example design. The PMC-440 parallel configuration EEPROM is user-programmable through the onboard JTAG header. Cable CBL-440-JTAG-000 provides users with a means to interface from the 440's onboard JTAG header and a standard Xilinx Parallel Cable IV.

Note that the ProWare module does not provide support for the use of the embedded PPC405processor inside the FPGA.

Figure 1: PMC-440 ProWare Hardware Block Diagram





PMC-440 Memory

The 440 provides 256 MB of 32-bit DDR SDRAM running on a 133 MHz SDRAM bus.

PMC-440 PMC Interface

- 64-bit PCI
- tracking for PCI-X (note that available IP is 33/66 MHz PCI-capable)
- PCI interface is 5V-tolerant (level shifters used)
- conduction-cooled module conforms to VITA 20-2005 including left and right secondary thermal interfaces and additional 5 mounting holes for rear stiffening bar

Discrete Digital I/O

The PMC-440 supports 48 bits of general purpose discrete digital I/O to the rear panel through the Pn4 connector, and a separate 30 bits to the front panel. The physical levels of the discrete digital I/O are configurable by the FPGA load for 3.3V and 2.5V LVTTL, and 2.5V LVDS operation. The PMC-440 routes all digital I/O lines as differential pairs to support LVDS configurations.

All front-panel I/Os are from FPGA bank 0, two I/Os can be clocks. From the rear panel, 22 I/Os are from FPGA bank 4, 26 I/Os are from bank 5. A total of four rear-panel I/Os can be clocks.

The PMC-440 provides user-selectable jumpers to select the FPGA Vcco voltage. One set of jumpers selects between 3.3V and 2.5V for all the 48 rear-panel I/O signals, a second set selects between 3.3V and 2.5V for all the 30 front-panel I/O signals.

RocketIO

The PMC-440 supports Xilinx' RocketIO technology, which provides a high performance low latency serial interconnection method for sensor-to-board or board-to-board data communications. Each RocketIO port of the 440 is configured as a bi-directional, 4-bit link with 4 differential transmit pairs and 4 differential receive pairs per port. The 440 provides two RocketIO ports - one through the Pn4 connector and the other through a dedicated Infiniband-style front panel connector.

The Pn4 RocketIO port is driven from a dedicated 62.5MHz LVPECL reference clock, allowing for operation at either 625 Mbits/sec or 1.25 Gbits/sec. At 1.25 Gbits/sec the nominal peak data rate is 500 MB/sec in each direction.

The front panel RocketIO port is driven from a dedicated 100MHz LVPECL reference clock, allowing for operation at either 1 Gbits/sec or 2 Gbits/sec. At 2 Gbits/sec the nominal peak data rate is 800 MB/sec in each direction.

PMC-440 Utility Features

- a 133 MHz clock is provided as standard for FPGA logic
- a spare site is provided for an application-specific clock (requires factory installation)
- PCI-readable temperature sensor on I2C bus
- PCI-readable current sensor on I2C bus
- header for JTAG/ChipScope Pro connection
- one red and three green LEDs
- only input voltage required is 5V

PMC-440 Temperature Sensor

The 440 provides one Maxim 6634 temperature sensor located in an approximately central location on the component side of the board. Through an I2C controller integrated into the FPGA, host card software can read the temperature sensor at any time. The temperature sensor is accurate to +/-2.5C from -40C to 125C. The temperature alert output is connected to the FPGA.

PMC-440 Current Sensors

The 440 provides current sensors for the 1.5V (FPGA core voltage), 2.5, and 3.3V rails. The current sensing circuitry for each rail consists of an 8-milliohm sense resistor input into a TI INA138 current shunt monitor that in turn is input into a TI ADS1112 16-bit A/D converter. The ADS1112 interfaces to the FPGA via the I2C bus.

PMC-440 Clock Oscillators

The PMC-440 includes the following clock oscillators:

- a 133.33MHz general system clock
- dedicated 100 MHz clock for the front panel RocketIO ports, supporting speeds of 1.0 and 2.0Gbits/sec
- dedicated 62.5 MHz clock for the rear panel RocketIO ports, supporting speeds of 625 MHz and 1.25 Gbits/sec
- a spare site for a factory-installable application-specific oscillator



PMC-440 Front Panel

Air-cooled 440 modules provide the following front panel provisions:

- Infiniband-style receptacle connector for RocketIO, FCI part number 10009629102010 or equivalent incorporating EMI gasket and threaded standoffs
- 31-pin connector for discrete digital I/O, Glenair part number MWDM2L31SCBRP110 or equivalent

All modules are provided with 4 user programmable general purpose LEDs mounted on the front edge of the PWB on the solder side - one red and three green.

Mechanical Format

The PMC-440 is a single width PMC module. Air-cooled modules are designed in accordance with the IEEE 1386 and 1386.1 specifications.

Conduction-cooled modules are designed in accordance with ANSI/VITA 20-2005, Conduction-Cooled PCI Mezzanine Standard. The cooling surfaces provided are the Primary Thermal Interface Region and the side 1 Secondary Thermal Interface Regions.

ProWare Design Kit

A ProWare Design Kit (PDK) is available for the PMC-440 ProWare module consisting of the following elements:

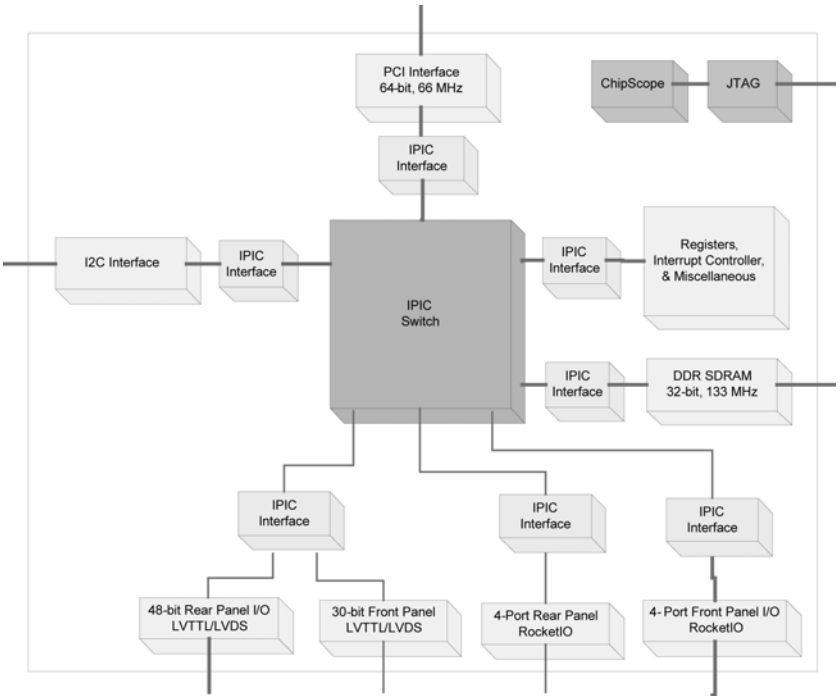
- IP library with the following functional elements:
  - > 32/64-bit, 66 MHz PCI initiator/target interface with integral DMA controller
  - > 32-bit DDR SDRAM controller
  - > discrete digital I/O module
  - > board register module with configuration identification and LED control bits
  - > I2C interface for connecting to temperature and current sensors
  - > interrupt controller logic
  - > RocketIO
  - > IPIC switch
- associated project, pinout files, and constraint files
- common IPIC interface for all PDK functional elements
- associated simulation files including MacroCad PCI testbench
- example design incorporating all the elements of the IP library into an example design that is preloaded unto the module when delivered
- VHDL implementation language for use with Xilinx EDK (Embedded Development Kit) design flow
- VxWorks driver
- documentation
- front-panel loop-back cable
- adapter cable to interface PMC-440 JTAG header to Xilinx Parallel Cable IV

IPIC-Based Architecture

Designing with the CWCEC ProWare Design Kit is greatly simplified by the use of an IPIC-based architecture. IPIC (IP InterConnect) is a Xilinx-defined standard inter-module interface standard. IPIC defines all the requisite elements for exchanging data in a parallel fashion between two digital blocks - two unidirectional 64-bit data busses, 32-bit address bus, and signals for read/write control signals, arbitration, and bursting.

All the IP modules provided with the ProWare Design Kit have IPIC interfaces (refer to Figure 2).

Figure 2: ProWare Design Kit IP Modules



IPIC Switch

For most customer designs, the IPIC switch can provide the core interconnection scheme for the overall FPGA logic. By incorporating an IPIC interface into the customer design, the custom logic can simply "plug into" the CWCEC-provided IPIC switch and achieve immediate connectivity to CWCEC IP such as the PCI and SDRAM cores, and to any other user logic or third party logic that also has an IPIC interface.

The IPIC switch provides separate IPIC initiator and IPIC target interfaces. The number of IPIC interfaces is configurable, up to a maximum of 8 initiator and 8 target interfaces.

Simulation Models

The ProWare Design Kit provides the following simulation models:

- PCI (from MacroCad)
- SDRAM
- RocketIO

Supported FPGA Development Environment

The CHAMP-FX is designed to work seamlessly with the Xilinx tool suite. The development environment is optimized for the Xilinx EDK (Embedded Development Kit) design flow, with VHDL as the implementation language. The following system is recommended for an optimal development environment:

- Xilinx EDK 6.3 (provided by Xilinx)
- Xilinx ISE 6.3 (provided by Xilinx)

Other related tools below are not required, but may prove to be helpful:

- ChipScope Pro 6.3 (provided by Xilinx)
- ModelSim 5.8 (VHDL - provided by Mentor Graphics)
- Synplify Pro 7.5 (provided by Synplicity)
- MATLAB (provided by The Mathworks)/ System Generator for DSP(provided by Xilinx)

VxWorks Driver Suite

The VxWorks driver is delivered in source format. The major elements of the driver are:

- driver for PCI DMA controller supporting chaining and interrupts for DMA done and error conditions
- driver for RocketIO including DMA controller supporting chaining and interrupts for DMA done and error conditions
- driver for I2C controller
- function library for configuring and reading/writing discrete digital I/O registers
- function library for writing to LED control registers
- demo program showing use of the various Driver Suite APIs



ProWare Design Kit Contents, Licensing, and Support Provisions

The ProWare Design Kit physically consists of:

- one CD-ROM for the FPGA IP and associated documentation
- one CD-ROM for the software driver and associated documentation
- front panel loop-back cable
- adapter cable to interface PMC-440 JTAG header to Xilinx Parallel Cable IV

The ProWare Design Kit is sold separately from the PMC-440 ProWare modules and is licensed on a per-program, per-site basis. Purchase of the PMC-440 is mandatory for users of the PMC-440.

Included with the ProWare Design Kit is 8 hours of technical support, applicable to any effort related to the use of the PMC-440 card and/or ProWare Design Kit. It is recommended that customers purchase additional consulting services via part number SVC-TECH-FPGA-L which provides for 80-hours of additional support time.

The ProWare Design Kit part number is DSW-440-000-CD

Specifications

Ruggedization Levels

(Refer to Ruggedization Guidelines datasheet for more details)

Air-Cooled Module	0 and 100
Conduction-Cooled Module	200

Power Requirements

	Maximum	Typical
+5V	tbd	tbd
+/- 12V, 3.3V	Not used	Not used

Dimensions and Weight

	Size	Weight
Air-Cooled Module	per IEEE 1386	<300g
Conduction-Cooled Module	per ANSI/VITA 20-2005 incorporates VITA 20 Primary Thermal Interface Region and side 1 Secondary Thermal Interface Regions	<300g



Contact Information

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Email: sales@cwcembedded.com

For technical support, please visit:

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