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SPMC/DPMC-211

CANBUS, UTILITY BUS, AND DISCRETE DIGITAL I/O MODULE

USER'S MANUAL

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PREFACE

PURPOSE

This manual provides an overview of the features and functions of the PMC-211 CANbus, Utility Bus, and Discrete Digital I/O Module. The manual also provides details of the connector interfaces as well as the programming interface. Basic instructions for installing the PMC-211 onto a basecard (such as the SVME/DMV-179 Single Board Computer) are also provided.

AUDIENCE

This document is intended for readers with a technical understanding of hardware engineering fundamentals, as well as an understanding of the VMEbus, PCI, CANbus and Utility Bus architectures.

SCOPE

This manual contains the following chapters:

Chapter 1 - Functional Description. Describes the features and functions of the PMC-211.

Chapter 2 - Connector Pin Assignments. Provides detailed information describing the Pn1, Pn2 and Pn4 connectors of the PMC-211, while also providing typical VME P0 and P2 interface pinouts when a PMC-211 is present.

Chapter 3 - Programming Interface. Describes the memory map and the local control and status register of the PMC-211.

Chapter 4 - Installation Instructions. Summarizes how to install the PMC-211 on a basecard and make connections to the interfaces it provides.

RELATED DOCUMENTS

Foundation Firmware v8.0 User's Manual, Dy 4 Systems document #808006.

Refer to the latest version of *The V350EPC, V360EPC Local Bus to PCI Bridge User's Manual* from V^3 Semiconductor for a detailed description of the V360EPC component's features and operation.

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CONVENTIONS USED IN THIS MANUAL

This document and the accompanying documents in the documentation package use various icon conventions and abbreviations to make the documents clearer and easier to read. These conventions cover typography for such elements as sample software code and keystrokes, signal meanings, and graphical elements for important information such as warnings or cautions.

Typographic Conventions

Table 1 lists the typographical conventions used in documents contained in this documentation package.

TABLE 1: Typographical Conventions

Item	Convention	Example
Keystrokes	Keys are listed as they appear on most keyboards, surrounded by < > marks. Combinations of key-strokes appear within a single set of < > brackets.	Type < Ctrl-Alt-C > to return to the previous menu. Type < Esc > to exit.
File Names	File names are set in italics.	Open the file named *es.h*.
Directory Names	Directory names show the full directory path. The last directory in the path does not have a trailing slash following it.	Go to the *c:\windows\temp\backup* directory.
Monitor Displays	Prompts and other text appearing on monitors is set in bold monospace type.	`% mpp MC68040gnu >`
Firmware Code	Firmware code, and any information you need to type in response to a prompt, is set in monospace type.	`% make -f Makefile.MC68040gnu`

Signal Conventions

Table 2 lists symbols that can follow a signal name. For example, the asterisk (#) is used with a PCI signal name, such as IRDY#.

TABLE 2: Signal Conventions

Symbol	Description
[no symbol]	The signal is active HIGH.
# or -	The signal is active LOW.

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Abbreviations

Table 3 lists the abbreviations used to describe the size of a memory device or a range of addresses.

TABLE 3: Abbreviations

Abbreviation	Convention
1 Kbyte	1,024 bytes
1 Mbyte	1,024 Kbytes
1 Gbyte	1,024 Mbytes

Memory Addresses

Unless otherwise stated, all memory addresses are shown in hexadecimal notation.

Icons

The following icons are used throughout this document:



Cross Reference

Cross references to other documents are used when a subject being discussed is addressed in depth by another, more authoritative document. Cross references are also used for document chapters and sections.



Warning

The warning icon indicates procedures in the manual that, if not carried out, or if carried out incorrectly, could cause physical injury, electrical damage to equipment, or a non-recoverable corruption of data. Warnings include instructions for preventing such damage. Please observe warning icons and read the accompanying text completely before carrying out the procedure.



Caution

The caution icon indicates non-catastrophic incidents, complex practices, or procedures which, if not observed, could result in damage to the hardware. Cautions include specific instructions for avoiding or minimizing these incidents.



Note

The note icon highlights exceptions and special information.



Tip

Tips provide extra information on the subject matter. This could include hints about how to use your current DY 4 card to its maximum potential.

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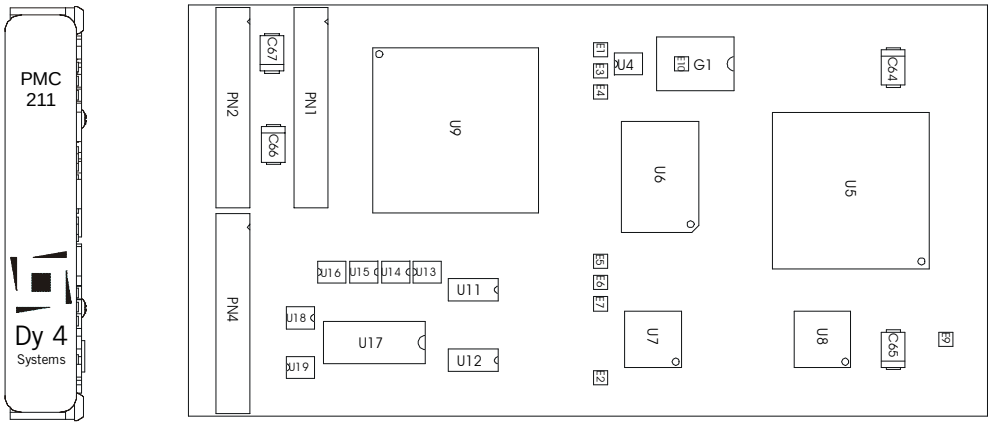
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1 FUNCTIONAL DESCRIPTION

INTRODUCING THE PMC-211

The PMC-211 primarily serves as a bridge between the PCI Bus and the Controller Area Network (CAN). It also serves as a bridge between the PCI Bus and the Utility Bus. The PMC-211's PCI interface complies with the *PCI Local Bus Specification*, Revision 2.1. It is beyond the scope of this manual to completely describe the PCI bus. This chapter provides a summary description of PCI bus operations; in particular, how the PMC-211 implements the PCI bus.

FIGURE 1.1: PMC-211 Front and Component Side Views



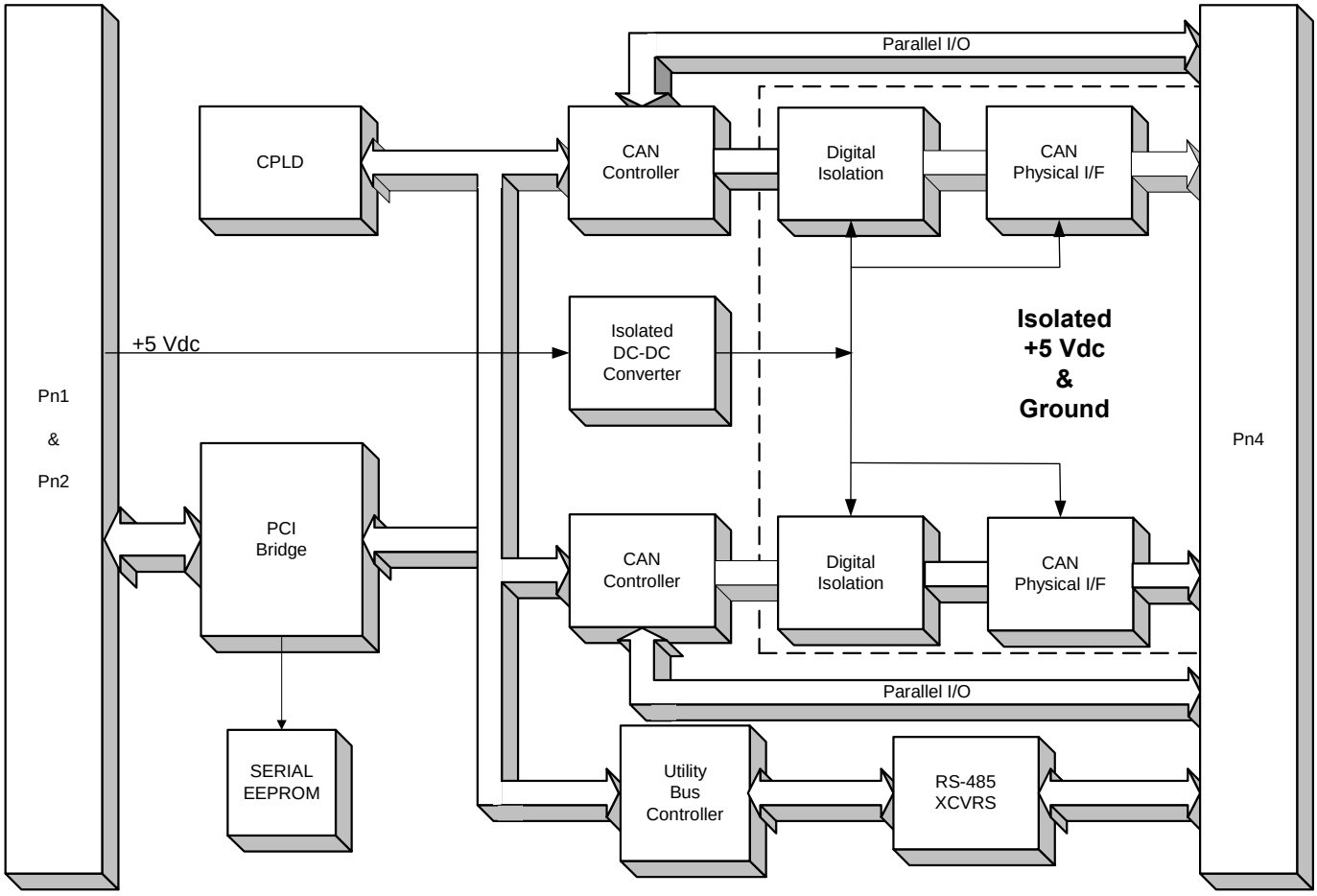
Note

Throughout this manual the term, "PMC", represents both SPMC and DPMC products unless otherwise noted.

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Figure 1.2 shows a functional block diagram of the PMC-211.

FIGURE 1.2: PMC-211 Functional Block Diagram



The PMC-211 includes a Vetronix MIC-3 bus controller, compliant with the standard Army Vetronix architecture. Note that the MIC is also referred to by its older name, UBIC (Utility Bus Interface Chip). The two terms are used interchangeably throughout this manual, but UBIC is used where backwards compatibility is important.

PMC-211 FEATURES LIST

The major features of the PMC-211 include:

- initiator-target PCI interface, with DMA capability
- Two Controller Area Network (CAN) interfaces based on the Intel 82527 stand-alone CAN controller
- CAN Physical Layer is fully compatible with ISO 11898-24V standard
- CAN transceiver can support high speed (up to 1 MBaud)
- 16 parallel I/O, implemented in the CAN controllers
- CAN interface outputs are galvanically isolated
- network configuration allows selection of CAN transfer rates of 250 Kbit/sec, 500 Kbit/sec, and 1 Mbit/sec on each channel independently

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- network control allows explicit control of bus state (OFF, ON)
- Utility Bus Controller
- option to depopulate Vetronix MIC-3 Controller
- capable of operation up to the level 200 limits specified in Table 1.3.
- Card Level Diagnostic capabilities are implemented within the FF/W on the host base-card.

POWER REQUIREMENTS

The PMC-211 maximum and typical 5 Volt power requirements are listed in Table 1.1.

TABLE 1.1: PMC-211 Board Current Requirements

Voltage	Maximum Current (mA)	Typical Current (mA)
+3.3V	Not Used	Not Used
+5V ± 0.25V	760	420
+12V ± 0.6V	Not Used	Not Used
-12V ± 0.6V	Not Used	Not Used

VOLTAGE REQUIREMENTS

The PMC-211 requires a steady state input voltage of 5.0 ± 0.25 volts DC.

PHYSICAL CHARACTERISTICS

The PMC-211 board has the following physical characteristics:

Weight Limits

The mass of the PMC-211 board shall not exceed the values specified in Table 1.2.

TABLE 1.2: Maximum CCA Mass

Card Type	Weight (grams)
DPMC	150
SPMC	200

Dimensions

The dimensions of the PMC-211 adheres to the dimensions defined in IEEE 1386 Draft 2.0, IEEE 1386.1 Draft 2.0 and VITA 20-199x CCPMC, Draft 1.6 January 20, 1998.

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PCI MEZZANINE CARD OVERVIEW

PMCs (PCI Mezzanine Cards) are modules which can be fitted to several of Dy 4's latest generation single board computers. Both air-cooled and conduction-cooled versions are available. The DPMC conduction-cooled models incorporate an embedded copper core thermal plane which provides structural rigidity and an excellent thermal path to the VMEbus basecard. The integrated assembly of the basecard and PMC module meets the same demanding environmental specifications as all other Dy 4 conduction-cooled products.

The PMC specification defines the electrical and mechanical elements of the PMC design to ensure that modules like the PMC-211 can be used on future single board computer products. This allows the systems integrator to upgrade through technology insertion to higher performance hardware while preserving the software invested in the PMC module.

ENVIRONMENTAL CHARACTERISTICS

Table 1.3 shows the complete range of environmental specification limits used to categorize the ruggedization levels of Dy 4 products. The PMC-211 is available in ruggedization levels 0 and 200.

TABLE 1.3: Environmental Specification Limits and Ruggedization Levels

Card Type	Operating Temperature	Storage Temperature	Operating Humidity	Storage Humidity	Sine Vibration (note 1)	Random Vibration (note 4)	Mechanical Shock (note 5)
Air-Cooled Level 0	0°C to 50°C inlet 4 cfm air flow (note 6)	-40°C to 85°C	0 to 95% non-condensing	0 to 95% non-condensing	N/A	N/A	N/A
Air-Cooled Level 100	-40°C to 71°C inlet 4 cfm air flow (note 6)	-55°C to 85°C	0 to 100% non-condensing	0 to 100% non-condensing	10 g peak 15-2000 Hz (note 2)	0.04 g^2/Hz 15-2000 Hz	30 g peak half sine pulse 11 ms duration
Conduction-Cooled Level 100	-40°C to 71°C card edge temperature	-55°C to 85°C	0 to 100% non-condensing	0 to 100% non-condensing	10 g 15-2000 Hz (note 3)	0.01 g^2/Hz 15-2000 Hz	40 g peak half sine pulse 11 ms duration
Conduction-Cooled Level 200	-55°C to 85°C card edge temperature	-62°C to 125°C	0 to 100% non-condensing	0 to 100% condensing	10 g 15-2000 Hz (note 3)	0.1 g^2/Hz 15-2000 Hz	40 g peak half sine pulse 11 ms duration

Notes

1. All levels based on a sweep duration of ten minutes per axis, each of three mutually perpendicular axis.
2. Displacement limited to 0.10 inches displacement amplitude from 15 to 44 Hz.
3. Displacement limited to 0.436 inches displacement amplitude from 15 to 21 Hz.
4. 60 minutes per axis each of three mutually perpendicular axes.
5. Three hits per direction per axis (total of 18 hits).
6. At sea level.

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PMC-211 PCI INTERFACE OVERVIEW

PCI BRIDGE

The PCI interface is implemented using the V^3 Semiconductor V360EPC Enhanced PCI Bridge Controller. The features of the V360EPC include:

- 32-bit, 33 MHz PCI interface, compliant with Revision 2.1 of the PCI Local Bus Specification, supporting operation as both Target and Initiator
- 32-bit Local Bus, with non-multiplexed address and data
- burst access support on both the PCI Bus and the Local Bus
- two DMA channels, with chaining
- dynamic, address-based Local Bus sizing
- flexible interrupt handling
- power on configuration via serial EEPROM.



Cross Reference

Refer to the latest version of *The V350EPC, V360EPC Local Bus to PCI Bridge User's Manual* from V^3 Semiconductor for a detailed description of V360EPC features and operation.

DATA TRANSFER APERTURES

The V360EPC uses programmable data transfer apertures to map between the Local Bus and the PCI Bus. An aperture is defined by the following characteristics:

- base address on the Local Bus
- base address on the PCI Bus
- size of address
- a number of other operational parameters involved in interfacing the two buses (for example, if byte lane swapping is performed or if the aperture appears in PCI Memory space or I/O space).

The V360EPC supports two apertures for PCI-to-Local transfers and two apertures for Local-to-PCI transfers.



Note

DMA transfers bypass these aperture definitions. Therefore, since there is no other Local Bus master on the PMC-211, the Local-to-PCI apertures are unused.

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LOCAL BUS SIZING

The V360EPC is able to treat the Local Bus as 8 bits wide, 16 bits wide or 32 bits wide when interfacing with peripherals. For example, if a 32-bit PCI read of an 8-bit local peripheral occurs, the V360EPC can be configured to automatically perform four 8-bit reads on the Local Bus and assemble a 32-bit read response.

Local Bus size is defined on an address basis. The Local Bus address space is broken up into sixteen 256 MByte regions, each of which can have a distinct bus size. Data bus sizes for the PMC-211 are defined in Table 1.4.

TABLE 1.4: PMC-211 Local Bus Sizes

Bus Size (bits)	Device
8	CAN Controllers
32	MIC
32	Local Control & Status Registers

The assignment of these devices to regions is described in the memory map section on page 3-1.

FIFOS AND TRANSFER POSTING

To buffer the PCI Bus and the Local Bus from each other, the V360EPC includes FIFOs through which data is transferred. This allows write accesses to be pipelined since the V360EPC will assert the PCI Target Ready signal as soon as data is written into a FIFO. Successive writes can continue in this fashion until the FIFO is full.

Acknowledgement of the data transfer before the data is actually written to its target device is called Write Posting. The V360EPC can also support Read Posting by issuing a Target Retry to a PCI request. This causes the Initiator to give up the PCI bus and try the request again later when the actual data is being fetched at the Target. The V360EPC will issue the initial retry immediately without waiting for the maximum PCI latency. If a second retry is required the V360EPC will wait until the maximum PCI latency of 16 clock cycles is reached before issuing the Target Retry.



Note

All read accesses from the PMC-211 require longer than the maximum allowable PCI latency of 16 clock cycles to complete if Read Posting is not used.

Read accesses posted to the 8-bit aperture will cause the V360EPC to perform a 32-bit local bus access regardless of the size of the posted PCI access. The desired data will be available on the expected PCI byte lane(s), but the local bus access may take up to 4 times longer than expected.

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PCI INTERRUPTS

The V360EPC has versatile PCI interrupt handling capabilities. There are four interrupt pins, any of which can drive a PCI interrupt signal or act as an interrupt input. Input to output routing is programmable inside the V360EPC. On the PMC-211, the UBIC and CAN interrupts are connected to the INTB#, INTC# and INTD# pins on the V360EPC, and INTA# is used for output to the PCI Bus. Interrupts can also be issued for DMA completion.

BRIDGE CONFIGURATION

The operation of the V360EPC is managed by a set of control and status registers located in PCI Configuration Space, as required by the PCI Local Bus Specification. These registers are initialized from the PMC-211 serial EEPROM when the card is brought out of reset and can then be modified by PCI Bus accesses.

A number of these control registers need to be modified during normal operation of the PMC-211. Some of these registers include:

- **Card Level Reset:** Asserting and negating PMC-211 card-level reset is accomplished by clearing and setting the RST_OUT field in the SYSTEM register. (Note that the CAN requires that card-level reset remain asserted for a minimum of **2** milliseconds after power up.)
- **PCI Base Address Registers (PCI_BASE0, PCI_BASE1):** These registers define the PCI base addresses of the PCI-to-Local data transfer apertures. These will generally be modified during PCI system configuration.
- **FIFO Configuration Registers (FIFO_PRIORITY, FIFO_CFG):** These registers, specific to the V360EPC, control how the internal FIFOs are filled and emptied. Optimal settings for these registers may vary from application to application.
- **DMA Registers:** The DMA Registers must be modified to initiate DMA transfers.



Caution

There are some control register fields, however, which should never be modified on the PMC-211. These include settings which are vital to normal operation. Some of these settings include:

- **Local Bus Size:** The Local Bus width for each region is specified in the LB_SIZE register. These must be defined correctly for the 8-bit and 32-bit regions on the PMC-211. *This register will be initialized correctly from the serial EEPROM and should never be changed thereafter*.
- **Local Bus Byte Ordering:** The ENDIAN field in the Local Bus Configuration Register (LB_CFG) controls byte ordering on the local bus, as well as the connectivity of 8-bit peripherals. *This register will be initialized correctly from the serial EEPROM and should never be changed thereafter*.
- **Interrupt Configuration:** The PCI Interrupt Configuration Register (PCI_INT_CFG) controls internal interrupt handling, and must be set to match the PMC-211 pin usage. Also, the INT_PIN field in the PCI Bus Parameter Register (PCI_BPARAM) must be set to correctly define the interrupt output pin.
- **Byte Swapping:** In order for the MIC registers to appear correctly to a processor, the byte lanes must be swapped. This requires that the SWAP field in the PCI_MAPx register corresponding to the MIC's aperture be programmed for "8-bit swap".
- **PCI Command Register:** This register defines what the PMC-211 can and cannot do on the PCI bus. The master bit [2] must be set to enable the V360EPC to become an initiator on the PCI bus. Bits 1-0 control which target cycles the V360EPC will accept. Both of these bits must be set for the PMC-211 to respond to PCI memory and PCI I/O accesses.

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You can bypass the V^3 PCI bridge configuration via the serial EEPROM. Shunt pin 34 on the PMC-211's Pn4 connector to ground. Refer to document ANSI/VITA 35-2000 for pin assignments for the PMC P4 connector to VME P0 and P2 connectors.

DATA TRANSFER APERTURE USAGE

The usage of data transfer apertures is a system design issue. However, the card-level design can form the basis of some guidelines as follows:

The 8-bit region and the 32-bit region should each be assigned to a separate aperture. This will restrict byte swapping to the 32-bit devices. Also, this will allow efficient use of PCI address space, since a huge aperture would be required to encompass both regions.

The data transfer apertures are inside the V360EPC, and may be modified by changing the base and map registers for each aperture. The PCI base address may be easily moved around inside PCI Memory or I/O space as the system design requires. The PCI Map registers cannot be as easily changed, as this register controls the PCI to local bus address decoding for each aperture. The local bus address decoding is performed inside the CPLD and cannot be changed. If the MAP_ADR bits are improperly modified, the PMC-211 will not function properly.

The PCI Map register also controls the byte swapping for each aperture. The 32-bit aperture requires byte swapping to match byte ordering on Dy 4 SBCs. This function may be disabled if the byte swapping is performed by software.

PCI to local bus aperture 1 is an 8-bit aperture intended to be mapped into PCI I/O space, and requires 512 bytes of address space. The aperture may be moved to PCI memory space, and if the Map register contents are not changed will occupy 16 MBytes of address space.

The apertures can be programmed to appear in either PCI I/O Space or Memory Space.

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INTERRUPTS

The PMC-211 asserts an interrupt on the PCI INTA# line to the basecard. The source can be the MIC or either CAN controller. On the PMC-211 design, the INTA# line is connected from the V360EPC to the PCI bus, and is the only possible interrupt output from the board. The UBIC and CAN interrupts are connected to INTB#, INTC#, and INTD# and so must always be configured as inputs if these devices are populated. When any of the input interrupt sources are asserted, INTA# will be asserted and remain asserted until all the input interrupts have been cleared.

The CAN Interrupts are auto-vectored only. The UBIC interrupts may be configured to be vectored or auto-vectored by setting a bit in the LCSR. Clearing the interrupt is different for each peripheral device. To clear the UBIC interrupt, the basecard must cause an external IACK cycle to occur. This is done by reading the UBIC IACK memory location defined in the PMC-211 address map. If the UBIC is configured in vector mode, the interrupt vector will be read during this access, otherwise the data read will be meaningless. A CAN interrupt can be cleared by reading registers within each CAN device.



Note

The PMC-211 does not support PCI IACK cycles. The IACK cycle for a vectored UBIC Interrupt must be manually generated by reading the register location.

The V360EPC interrupt inputs are assigned as follows:

- UBIC interrupt connects to INTB#
- CAN1 interrupt connects to INTC#
- CAN2 interrupt connects to INTD#



Cross Reference

Refer to Chapter 3 of this manual for further information on programming interrupts.

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ADDRESS/DATA BUS

Data is taken and made available as per Table 1.5. A 32-bit read or write to these devices will cause four consecutive accesses on the PMC-211 local bus. A 16-bit read or write to these devices will cause two consecutive accesses on the PMC-211 local bus.

TABLE 1.5: PMC-211 Supported Accesses

Function	32-Bit	16-Bit	8-Bit
MIC Write	✓		
MIC Read	✓		
CAN Write	✓	✓	✓
CAN Read	✓	✓	✓
LCSR Write	✓		
LCSR Read	✓		

SYSTEM RESET

The PCI signal RST# from the basecard is used as the master reset for the PMC-211. A low logic level signal on this line resets all control logic on the card. If a message is being transmitted at the time of the assertion of reset, the transmission will be aborted. Messages being received at the time of a reset will be lost. This is true for both CAN and UBIC messages. After the PCI RST# is removed, the V360EPC will be reinitialized by the serial EEPROM or to its default state if the serial EEPROM is disabled. The local bus reset bit will be asserted, holding the rest of the PMC-211 in reset until it is cleared by the basecard.

CPLD RESET

The CPLD is reset by the LRST output line from the V360EPC. The CPLD will continue to output the 16 MHz local bus clock while reset is asserted.

CLOCK GENERATION

The PMC-211 will operate on the PCI interface at clock rates up to 33 MHz. The 33 MHz clock is generated on the basecard.

A separate 16 MHz local clock is used by the CAN Controllers and the UBIC. The 16 MHz clock is generated by the CPLD from the 32 MHz oscillator module on the PMC-211.

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INITIALIZATION

After the signal PCI RST# is deasserted, the V360EPC needs to be re-initialized before the resources on the PMC-211 are available to the basecard. This may be done one of two ways:

- **Serial EEPROM**: The first 128 bytes of the V360EPC register space will be downloaded from the Serial EEPROM if it is detected when PCI RST# is deasserted. The V360EPC will detect the EEPROM if the SDA line (serial data) is high after reset. This line is normally pulled up so the default condition is for the V360EPC to receive its configuration from the Serial EEPROM.
- **Software Initialization**: The V360EPC configuration registers may be modified by the basecard immediately after PCI RST# is deasserted through the PCI I/O configuration address space. Accesses to these address locations cause the IDSEL line to be asserted to the V360EPC, indicating that the PCI cycle is an initialization access.



Note

The serial EEPROM defines the requirements of the PMC-211 to the host system. This enables the host system to properly allocate PCI memory for the PMC-211 during the PCI scan phase of its boot process. During the serial EEPROM load operation the V360EPC will issue retries on the PCI bus to any PCI device trying to access it.

If software initialization is the desired method, the serial EEPROM data line must be pulled to ground, at the P2 (or P0) connector. If this is not done the data will be automatically downloaded before the software configuration can occur, and certain patterns of random data can cause the PMC-211 and the basecard to lock up. If the serial EEPROM is disabled, the V360EPC will boot up in its default state. In this condition the PCI to Local apertures will not be set up, but the configuration registers will all be accessible by PCI configuration cycles.



Note

If the serial EEPROM option is used and the data becomes corrupted, the PMC-211 may cause the basecard to lockup during initialization. To correct this, the serial EEPROM must be disabled to allow the V360EPC to reach its default state. Then the card can be initialized with software, and the EEPROM data can be reprogrammed.

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CONTROLLER AREA NETWORK (CAN) INTERFACE



Cross Reference

The PMC-211 provides two CAN interfaces based on the Intel 82527 CAN Controller. The PMC-211 supports CAN Specification 2.0 Part A and Part B (Standard 11 bit identifier and Extended 29 bit identifier Data Frames) as implemented in the Intel 82527. Refer to the *82527 Serial Communications Controller Architectural Overview* (located on Intel's developers' website) for a detailed description of the CAN Controller's features.

CAN PHYSICAL INTERFACE

The PMC-211 supports the CAN-High-Speed physical interface as specified in ISO 11898. Galvanic isolation from the CAN-Controller is supported. CAN termination resistors and shield termination are not provided.

CAN CLOCK GENERATION

The PMC-211 provides a 16 MHz clock to the CAN Controller. This clock is generated from a CPLD by dividing a 32 MHz clock signal. The 32 MHz clock is driven by an oscillator module located on the PMC-211.

CAN ACCESS

Since the CAN interface is operating in a synchronous mode, access timing is important. On the PMC-211, the CAN interface operates at 16 MHz, so there are certain internal clocking requirements. The SCLK and MCLK frequencies must both be set to 8 MHz. If this is not done, the read and write cycle times will be incorrect since they are specified in terms of MCLK, and data errors will probably occur.

Certain registers (including the inside Port registers and the message control registers) inside the CAN may not be modified by an external processor without setting the software initialization bit in the control register. This bit must be set before these registers can be modified.

The PMC-211 CAN interface uses the PCA82C251 for its physical layer. This means that the CAN controller will send and receive its data using TTL levels. The 82527 is capable of a differential interface, but is not configured this way. The Bus Configuration register must be set up to ignore the RX1 input and to disable the TX1 output.



Cross Reference

For more information on the CAN register map see Table 3.5 on page 3-4.

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CAN BIT TIMING

The 82527 CAN Controller is capable of CAN transfer rates of 250K, 500K, and 1 Mbit/s. However, this setup is dependent upon two different settings: the SCLK frequency and the internal bit timing. The SCLK frequency must be set to 8 MHz, and this determines the sampling rate for the incoming bit stream. This is the fastest setting so it has the highest resolution, but the sampling times still must be set according to the frequency of the incoming data. This is controlled by the bit timing registers and is discussed in the *82527 Serial Communications Controller Architectural Overview*, located on Intel's developers' website.

MIC-3 BUS CONTROLLER

The PMC-211 includes a Vetronix MIC-3 bus controller, compliant with the standard Army Vetronix architecture. The MIC (MEPCAM Interface Chip) on the PMC-211 provides a dual-redundant MEPCAM (Multiplexed Electrical Power/Data Control And Management) bus interface. This device provides a complete interface to the MEPCAM bus which uses EIA-485 as its electrical specification. This bus supports a 1.33 Mbps standard data rate (up to 2 Mbps max.), Manchester signal encoding, and open command/response protocol. The message format supported is 3-bit sync, 32-bit data, with 1-bit parity. Sixty four modules are addressable per bus, with 32 devices addressable per module, yielding up to 2048 analog and/or discrete devices per controller module.

MIC ACCESS

MIC-3 registers are 32 bits wide and only 32-bit aligned accesses should be used. Although byte and word accesses are not supported, the PMC-211 will respond normally. Read accesses will return the default data-bus state (0xFFFFFFFF) and write accesses will be non-destructive.

Several MIC-3 registers are read-only or write-only. The MIC will not respond to read attempts to write-only registers or write attempts to read-only registers. In this case the PMC-211 will respond normally, but the attempted access will have had no effect.



Cross Reference

For information on the MIC-3 register map, refer to MIC Register Set on page 3-7.

MIC ADDRESS SELECTION

Five MIC address lines are routed to the SBC's P2 connector for programming the MIC Module ID. Refer to the *Getting Started* manual for your particular CCA to determine the exact P2 pins the UBIC address lines are presented on.

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MIC RECEIVER GATING

The PMC-211 incorporates MIC receiver gating circuits which allow received data to be masked from the MIC. This is useful for fault detection algorithms which require that the two redundant channels be completely isolated.

For example, consider the following scenario, where we must test the MIC's Channel A receiver:

The MIC sends a message to a remote terminal using Channel A, with Channel B disabled. When the remote terminal sends its echo response to the MIC, it uses both Channels A and B, as required under MEPCAM bus protocol. While the MIC did not use Channel B to send the original message to the remote terminal, it receives the echo on both A and B channels.

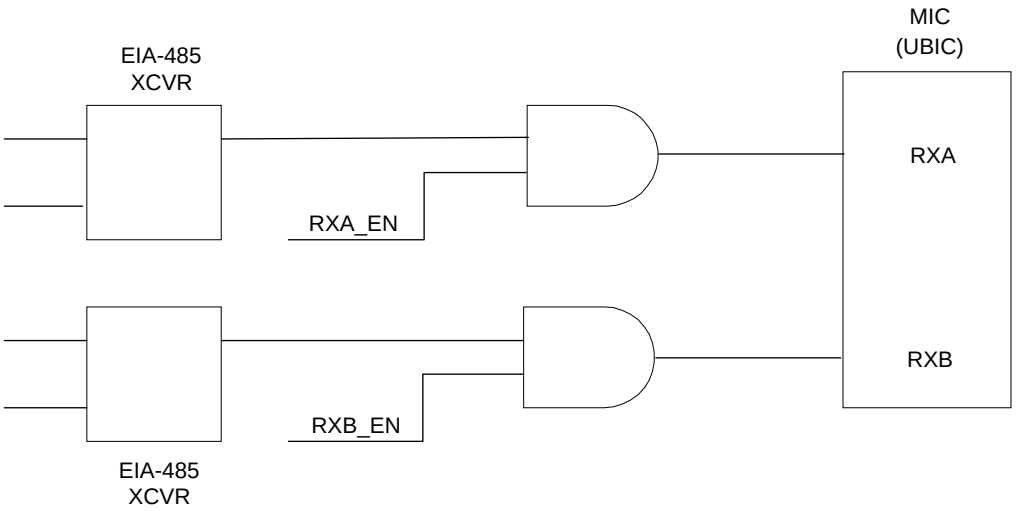
There is no provision in the MIC chip to inform its host that data was correctly received on only one of the channels. Control software cannot directly determine if the MIC's Channel A receiver was defective, since Channel B successfully receives the echo. By disabling the Channel B receiver, the control software can test Channel A's receiver circuitry.



Cross Reference

Figure 1.3 shows the MIC receiver gating circuitry. MIC receiver gating control bits are described in the Local Control/Status Register section on page 3-6.

FIGURE 1.3: MIC Receiver Gating



MIC RESET

The MIC is reset when the PMC-211 local reset signal is asserted, or alternatively, it may be reset under software control.

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MIC INTERRUPTS

The MIC device supports both vectored and auto-vectored interrupts, and the PMC-211 provides circuitry to handle both modes of operation. The AVSEL bit in the LCSR selects the interrupt mode of the MIC, and the read-only UBIC_IACK memory location will cause an interrupt acknowledge cycle when accessed.

In vectored mode, the MIC interrupt vector is placed on the data bus during the interrupt acknowledge cycle and the MIC interrupt is negated.

In auto-vectored mode, the MIC does not respond with an interrupt vector. Since the MIC does not negate interrupt requests until it receives an interrupt acknowledge cycle, the basecard must access the UBIC_IACK memory location to synthesize an interrupt acknowledge cycle to the MIC.

Most MEPCAM commands sent by the MIC result in the addressed remote terminal echoing a response to the command. When the MIC receives the echoed response, it automatically generates an interrupt to the basecard's processor.

In many cases, it is not necessary to process the MIC interrupts, however, the MIC device does not provide a mechanism to disable its interrupt requests. To allow the basecard to eliminate the overhead associated with processing these undesired interrupts, the PMC-211 provides a software-controlled MIC interrupt masking mechanism. With MIC interrupts masked, the masking circuitry intercepts MIC interrupts and prevents unwanted interrupts from reaching the basecard.

Since the MIC does not negate interrupt requests until it receives an interrupt acknowledge cycle, the masking circuitry also synthesizes interrupt acknowledge cycles for the intercepted MIC interrupts. The masking circuitry will assert the AVSEL bit, placing the MIC in auto-vectored mode. This prevents an unwanted interrupt vector from being placed on the data bus by the MIC during masked interrupt acknowledge cycles.

MIC interrupt masking is controlled by the UBIC_MASK bit of the Local Control and Status Register. This bit may be set or cleared dynamically. If the UBIC_MASK bit is changed while an acknowledge cycle is in progress, the internal version of the bit will not change until the cycle is complete. When the PMC-211 is synthesizing an interrupt acknowledge cycle, any incoming cycles to the MIC are held off until the interrupt acknowledge cycle is complete.



Cross Reference

Refer to page 3-6 for additional information on the Local Control and Status Register.

GENERAL PURPOSE I/O

The PMC-211 supports 16 bits of General Purpose TTL I/O, configurable on a per-bit basis as inputs or outputs. Each CAN Controller controls 8 of the TTL I/O bits. The direction and value of each bit is set under software control by registers contained in each CAN Controller. CAN Controller 1 (U8) controls DIO signals IO [7:0], while Can Controller 2 (U7) controls DIO signals [15:8].

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LOCAL CONTROL/STATUS REGISTER



Cross Reference

The PMC-211 provides a local status register that is contained within the CPLD. Refer to Chapter 3 for information on bit definition.

LOCAL READ/WRITE

The V360EPC drives the local Read/Write line high for local bus write accesses, and low for read accesses. This is opposite to the sense of the PMC-211 peripherals. The local read/write line is inverted in the CPLD and then driven to the CAN and UBIC devices.

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2 CONNECTOR PIN ASSIGNMENTS

INTRODUCTION

This chapter lists the pin-outs for the following connectors:

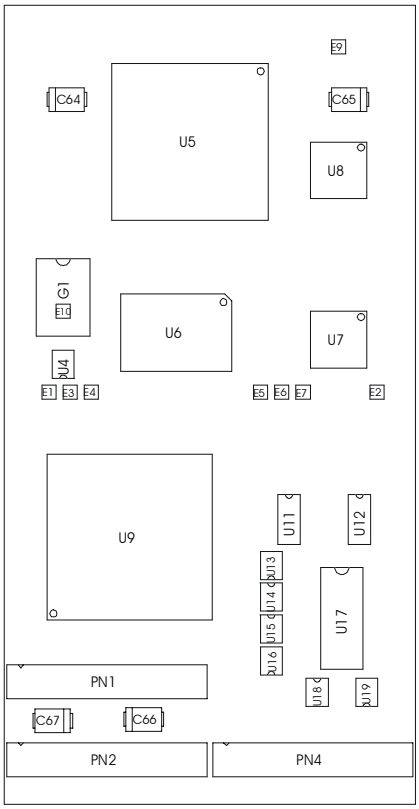
- Pn1 and Pn2 connectors
- Pn4 connector
- typical VME P2 and P0 connectors.

The PMC-211 uses three 64 way connectors for electrical connection to the basecard conforming to IEEE P1386.1/Draft 2.0 April 4th 1995. Connectors Pn1 and Pn2 are used for the 32-bit PCI Interface. Pn4 is used for routing PMC I/O to the VME backplane via the basecard P0 or P2 connector.

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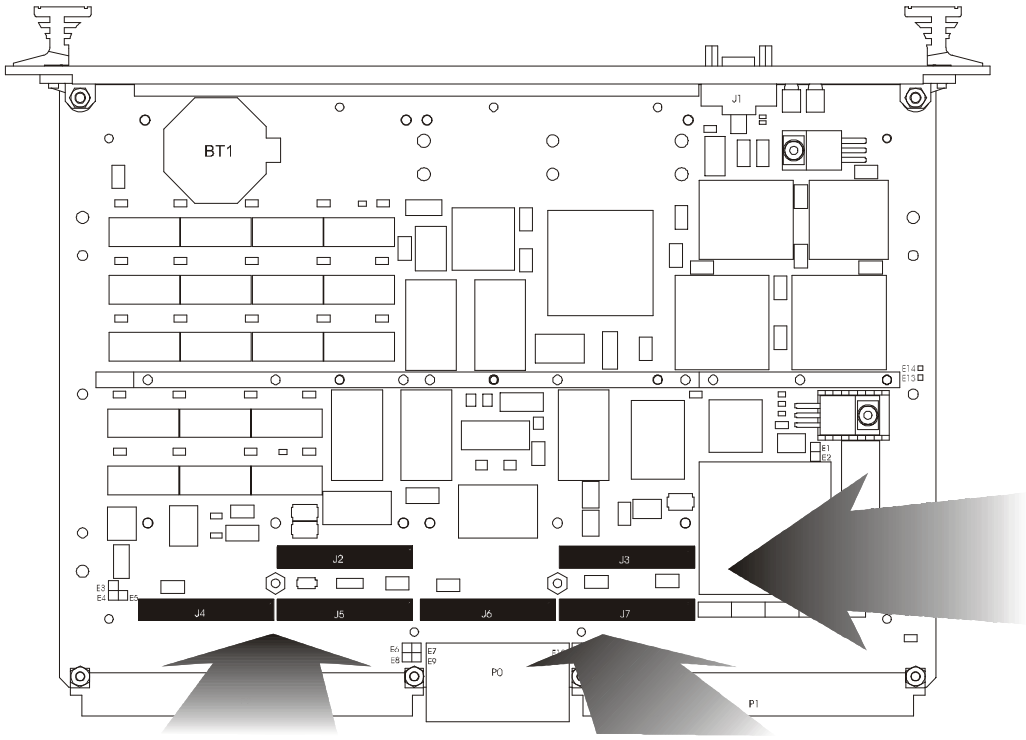
Figure 2.1 illustrates PMC connector orientation on Side 1 of the PMC-211. Figure 2.2 on page 2-3 illustrates where the PMC-211 connects to the basecard.

FIGURE 2.1: Connector Orientation on PMC, Side 1



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FIGURE 2.2: Connector Orientation on Basecard



CONNECTOR PIN ASSIGNMENTS

The pin-out details for the Pn1 and Pn2 connectors appear in Tables 2.2 to 2.7.

TABLE 2.1: Signal Type Definitions

Signal Type	Definition
IN	Input is a standard input only signal
OUT	Output is a standard active driver
I/O	Input - Output
PWR	Power Connection
NC	No Connect
General Purpose TTL	DC characteristics: Vil 0.3*Vcc max, Vih 0.7*Vcc min. Vol 0.45Volts, @ Iol = 1.6 mA Voh Vcc - 0.8V, @ Ioh = -200 µA Note: No protection exists for DIO on the card. Signal reference must be the same as digital ground on the PMC-211. At reset these pins are tristate and pulled up to 5 Volts until the configuration register in the CAN configuration registers are written to. Please see the data sheet for the 82527 for more information.

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TABLE 2.2: Pin-out for Connector Pn1

Pn1 32 Bit PCI			
Pin #	**Signal Name**	**Signal Name**	**Pin #**
1	TCK	-12V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD*	10
11	Ground	PCI-RSVD*	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19	V (I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64

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TABLE 2.3: Pn1 Connector Description (Odd Pin Numbers)

Pin No.	Signal	Dir	Description	Electrical Characteristics
1	TCK	IN	JTAG Clock	
3	Ground	PWR	Ground	
5	INTB#	NC	Interrupt B	
7	BUSMODE1#	OUT	Asserted to indicate card present and capable of PCI protocol	
9	INTD#	NC	Interrupt D	
11	Ground	PWR	Ground	
13	CLK	IN	PCI System Clock	PCI Specification 2.1
15	Ground	PWR	Ground	
17	REQ#	I/O	Request	
19	V (I/O)	NC		
21	AD[28]	I/O	Address/Data Line 28	PCI Specification 2.1
23	AD[25]	I/O	Address/Data Line 25	PCI Specification 2.1
25	Ground	PWR	Ground	
27	AD[22]	I/O	Address/Data Line 22	PCI Specification 2.1
29	AD[19]	I/O	Address/Data Line 19	PCI Specification 2.1
31	V(I/O)	NC		PCI Specification 2.1
33	FRAME#	I/O	Asserted by Master to indicate beginning and duration of access, negated when transaction is in final data phase	PCI Specification 2.1
35	Ground	PWR	Ground	
37	DEVSEL#	I/O	Asserted by Target to indicate it is the device being addressed.	PCI Specification 2.1
39	Ground	PWR	Ground	
41	SDONE#	NC	Snoop Done	
43	PAR	I/O	Parity signal across AD31:0 and C/BE3:0. Parity is even	PCI Specification 2.1
45	V(I/O)	NC		
47	AD[12]	I/O	Address/Data Line 12	PCI Specification 2.1
49	AD[09]	I/O	Address/Data Line 09	PCI Specification 2.1
51	Ground	PWR	Ground	
53	AD[06]	I/O	Address/Data Line 06	PCI Specification 2.1
55	AD[04]	I/O	Address/Data Line 04	PCI Specification 2.1
57	V(I/O)	PWR		
59	AD[02]	I/O	Address/Data Line 02	PCI Specification 2.1
61	AD[00]	I/O	Address/Data Line 00	PCI Specification 2.1
63	Ground	PWR	Ground	

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TABLE 2.4: Pn1 Connector Description (Even Pin Numbers)

Pin No.	Signal	Dir	Description	Electrical Characteristics
2	-12V	NC		
4	INTA#	OUT	Interrupt A	PCI Specification 2.1
6	INTC#	NC	Interrupt C	PCI Specification 2.1
8	+5V	PWR		PCI Specification 2.1
10	PCI-RSVD*	NC	PCI Reserved	
12	PCI-RSVD*	NC	PCI Reserved	
14	Ground	PWR	Ground	
16	GNT#	IN	Grant	
18	+5V	PWR		PCI Specification 2.1
20	AD[31]	I/O	Address/Data Line 31	PCI Specification 2.1
22	AD[27]	I/O	Address/Data Line 27	PCI Specification 2.1
24	Ground	PWR	Ground	
26	C/BE[3]#	I/O	Bus Command and Byte Lane Enable 3	PCI Specification 2.1
28	AD[21]	I/O	Address/Data Line 21	PCI Specification 2.1
30	+5V	PWR		PCI Specification 2.1
32	AD[17]	I/O	Address/Data Line 17	PCI Specification 2.1
34	Ground	PWR	Ground	
36	IRDY#	I/O	Initiator Ready	PCI Specification 2.1
38	+5V	PWR		PCI Specification 2.1
40	LOCK#	NC	Lock	
42	SBO#	NC	Snoop Backoff	
44	Ground	PWR	Ground	
46	AD[15]	I/O	Address/Data Line 15	PCI Specification 2.1
48	AD[11]	I/O	Address/Data Line 11	PCI Specification 2.1
50	+5V	PWR		PCI Specification 2.1
52	C/BE[0]#	I/O	Bus Command and Byte Lane Enable 0	PCI Specification 2.1
54	AD[05]	I/O	Address/Data Line 05	PCI Specification 2.1
56	Ground	PWR	Ground	
58	AD[03]	I/O	Address/Data Line 03	PCI Specification 2.1
60	AD[01]	I/O	Address/Data Line 01	PCI Specification 2.1
62	+5V	PWR		
64	REQ64#	NC	Request 64-bit transfer	

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TABLE 2.5: Pin-out for Connector Pn2

Pn2 32 Bit PCI			
Pin #	**Signal Name**	**Signal Name**	**Pin #**
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD*	8
9	PCI-RSVD*	PCI-RSVD*	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	PCI-RSVD*	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34
35	TRDY#	+3.3V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD	52
53	+3.3V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK64#	+3.3V	62
63	Ground	PMC-RSVD	64

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TABLE 2.6: Pn2 Connector Description (Odd Pin Numbers)

Pin No.	Signal	Dir	Description	Electrical Characteristics
1	+12V	NC	Unused by PMC-211	
3	TMS	NC	TDO	
5	TDI		Connected to TD0 for a loopback.	
7	Ground	PWR	Ground	
9	PCI-RSVD*	NC	PCI Reserved	
11	BUSMODE2#	IN		
13	RST#	IN	Reset	PCI Specification 2.1
15	3.3V	NC	Unused by PMC-211	
17	PCI-RSVD*	NC	PCI Reserved	
19	AD[30]	I/O	Address/Data Line 30	PCI Specification 2.1
21	Ground	PWR	Ground	
23	AD[24]	I/O	Address/Data Line 24	PCI Specification 2.1
25	IDSEL	IN	Initialization Device Select	PCI Specification 2.1
27	+3.3V	PWR	Unused by PMC-211	
29	AD[18]	I/O	Address/Data Line 18	PCI Specification 2.1
31	AD[16]	I/O	Address/Data Line 16	PCI Specification 2.1
33	Ground	PWR	Ground	
35	TRDY#	I/O	Target Ready	
37	Ground	PWR	Ground	
39	PERR#	I/O	Parity Error	PCI Specification 2.1
41	+3.3V	NC	Unused by PMC-211	
43	C/BE[1]#	I/O	Bus Command and Byte Lane Enable 1	PCI Specification 2.1
45	AD[14]	I/O	Address/Data Line 14	PCI Specification 2.1
47	Ground	PWR	Ground	
49	AD[08]	I/O	Address/Data Line 08	PCI Specification 2.1
51	AD[07]	I/O	Address/Data Line 07	PCI Specification 2.1
53	+3.3V	NC	Unused by PMC-211	
55	PMC-RSVD	NC	PMC Reserved	
57	PMC-RSVD	NC	PMC Reserved	
59	Ground	PWR	Ground	
61	ACK64#	NC	Acknowledge 64-bit transfer	
63	Ground	PWR	Ground	

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TABLE 2.7: Pn2 Connector Description (Even Pin Numbers)

Pin No.	Signal	Dir	Description	Electrical Characteristics
2	TRST#	NC		
4	TDO		Connected to TDI for a loop-back	
6	Ground	PWR	Ground	
8	PCI-RSVD*	NC	PCI Reserved	
10	PCI-RSVD*	NC	PCI Reserved	
12	+3.3V	NC	Unused by PMC-211	
14	BUSMODE3#	IN		
16	BUSMODE4#	IN	Driven by basecard to query card presence and protocol supported.	
18	Ground	PWR	Ground	
20	AD[29]	I/O	Address/Data Line 29	PCI Specification 2.1
22	AD[26]	I/O	Address/Data Line 26	PCI Specification 2.1
24	+3.3V	NC	Unused by PMC-211	
26	AD[23]	I/O	Address/Data Line 23	PCI Specification 2.1
28	AD[20]	I/O	Address/Data Line 20	PCI Specification 2.1
30	Ground	PWR	Ground	
32	C/BE[2]#	I/O	Bus Command and Byte Lane Enable 2	
34	PMC-RSVD	NC	PMC Reserved	
36	+3.3V	NC	Unused by PMC-211	
38	STOP#	I/O	Stop	
40	Ground	PWR	Ground	
42	SERR#	I/O	System Error	
44	Ground	PWR	Ground	
46	AD[13]	I/O	Address/Data Line 13	PCI Specification 2.1
48	AD[10]	I/O	Address/Data Line 10	PCI Specification 2.1
50	+3.3V	NC	Unused by PMC-211	
52	PMC-RSVD	NC	PMC Reserved	
54	PMC-RSVD	NC	PMC Reserved	
56	Ground	PWR	Ground	
58	PMC-RSVD	NC	PMC Reserved	
60	PMC-RSVD	NC	PMC Reserved	
62	+3.3V	NC	Unused by PMC-211	
64	PMC-RSVD	NC	Reserved	

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PN4 CONNECTOR PIN ASSIGNMENTS

The pin-out details for the Pn4 connector are shown in Table 2.8. Signals shown in bold use pins corresponding to the MAX-657.

TABLE 2.8: Pin-out for Connector Pn4

Pin#	Signal Name	Signal Name	Pin#
1	N/A	N/A	2
3	IO8	IO9	4
5	IO10	IO11	6
7	N/A	N/A	8
9	N/A	N/A	10
11	IO12	IO13	12
13	IO14	IO15	14
15	N/A	N/A	16
17	CAN2_H	N/A	18
19	CAN2_L	N/A	20
21	CAN1_H	N/A	22
23	CAN1_L	JTAG_TDO	24
25	JTAG_TDI	JTAG_TCLK	26
27	JTAG_TMS	N/A	28
29	N/A	**UBICA+**	30
31	**IO0**	**UBICA-**	32
33	GND	EEPROM_DATA	34
35	**IO1**	**UBICB+**	36
37	**IO2**	**UBICB-**	38
39	**IO3**	**UBIC_MID5**	40
41	UBIC_MID4	UBIC_MID3	42
43	UBIC_MID2	UBIC_MID1	44
45	IO4	IO5	46
47	IO6	N/A	48
49	N/A	IO7	50
51	N/A	N/A	52
53	N/A	N/A	54
55	N/A	N/A	56
57	N/A	N/A	58
59	N/A	N/A	60
61	N/A	N/A	62
63	N/A	N/A	64

Signals shown in bold use pins corresponding to the MAX-657.

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TABLE 2.9: Pn4 Connector Description (Odd Pin Numbers)

Pin No.	Signal	Dir	Description	Electrical Characteristics
1	N/A			
3	IO8	I/O	General Purpose TTL I/O Bit 8	
5	IO10	I/O	General Purpose TTL I/O Bit 10	
7	N/A			
9	N/A			
11	IO12	I/O	General Purpose TTL I/O Bit 12	
13	IO14	I/O	General Purpose TTL I/O Bit 14	
15	N/A			
17	CAN2_H	I/O	CANbus Channel 2 Transceiver High Output	ISO11898 CAN Spec.
19	CAN2_L	I/O	CANbus Channel 2 Transceiver Low Output	ISO11898 CAN Spec.
21	CAN1_H	I/O	CANbus Channel 1 Transceiver High Output	ISO11898 CAN Spec.
23	CAN1_L	I/O	CANbus Channel 1 Transceiver Low Output	ISO11898 CAN Spec.
25	JTAG_TDI	IN	JTAG Data In for CPLD In Circuit Programming	
27	JTAG_TMS	IN	JTAG Mode Set, for CPLD In Circuit Programming	
29	N/A	N/A	N/A	
31	**IO0**	I/O	General Purpose TTL I/O Bit 0	
33	GND			
35	**IO1**	I/O	General Purpose TTL I/O Bit 1	
37	**IO2**	I/O	General Purpose TTL I/O Bit 2	
39	**IO3**	I/O	General Purpose TTL I/O Bit 3	
41	UBIC_MID4	IN	UBIC Module ID Configuration Input, Bit 4	
43	UBIC_MID2	IN	UBIC Module ID Configuration Input, Bit 2	
45	IO4	I/O	General Purpose TTL I/O Bit 4	
47	IO6	I/O	General Purpose TTL I/O Bit 6	
49	N/A			
51	N/A			
53	N/A			
55	N/A			
57	N/A			
59	N/A			
61	N/A			
63	N/A			

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TABLE 2.10: Pn4 Connector Description (Even Pin Numbers)

Pin#	Signal Name	Dir	Description
2	N/A		
4	IO9	I/O	General Purpose TTL I/O Bit 9
6	IO11	I/O	General Purpose TTL I/O Bit 11
8	N/A		
10	N/A		
12	IO13	I/O	General Purpose TTL I/O Bit 13
14	IO15	I/O	General Purpose TTL I/O Bit 15
16	N/A		
18	N/A		
20	N/A		
22	N/A		
24	JTAG_TDO	OUT	JTAG Data Out for CPLD In Circuit Programming
26	JTAG_TCLK	IN	JTAG Clock for CPLD In Circuit Programming
28	N/A	N/A	N/A
30	**UBICA+**	I/O	UBIC Channel A Transceiver High Output.
32	**UBICA-**	I/O	UBIC CHannel A Transceiver Low Output
34	EEPROM_DATA	IN	Serial EEPROM data line must be pulled to GND to disable the EEPROM boot option.
36	**UBICB+**	I/O	UBIC Channel B Transceiver High Output
38	**UBICB-**	I/O	UBIC Channel B Transceiver Low Output.
40	**UBIC_MID5**	IN	UBIC Module ID Configuration Input, Bit 5
42	UBIC_MID3	IN	UBIC Module ID Configuration Input, Bit 3
44	UBIC_MID1	IN	UBIC Module ID Configuration Input, Bit 1
46	IO5	I/O	General Purpose TTL I/O Bit 5
48	N/A		
50	IO7	I/O	General Purpose TTL I/O Bit 7
52	N/A		
54	N/A		
56	N/A		
58	N/A		
60	N/A		
62	N/A		
64	N/A		

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TYPICAL VME P2 CONNECTOR PIN ASSIGNMENTS

The pin-out details for a typical VME P2 connector (as specified for single-PMC-slot basecards in Draft Standard Common Mezzanine Card Family: CMC) is as shown in Table 2.11. The row B pin-out is fixed by the VME IEEE 1014-1987 Specification. Note that some host basecards may not be compliant with this standard.

TABLE 2.11: Pin-out for VME P2 Connector

Pin #	Row A Signals	Row B Signals	Row C Signals
	PMC I/O		PMC I/O
1	Unused	+5V	Unused
2	IO9	GND	IO8
3	IO11	RESERVED	IO10
4	Unused	A24	Unused
5	Unused	A25	Unused
6	IO13	A26	IO12
7	IO15	A27	IO14
8	Unused	A28	Unused
9	Unused	A29	CAN2_H
10	Unused	A30	CAN2_L
11	Unused	A31	CAN1_H
12	JTAG_TDO	GND	CAN1_L
13	JTAG_TCLK	+5V	JTAG_TDI
14	Unused	D16	JTAG_TMS
15	**UBICA+**	D17	Unused
16	**UBICA-**	D18	**IO0**
17	EEPROM_DATA	D19	GND
18	**UBICB+**	D20	**IO1**
19	**UBICB-**	D21	**IO2**
20	**UBIC_MID5**	D22	**IO3**
21	UBIC_MID3	D23	UBIC_MID4
22	UBIC_MID1	GND	UBIC_MID2
23	IO5	D24	IO4
24	Unused	D25	106
25	IO7	D26	Unused
26	Unused	D27	Unused
27	Unused	D28	Unused
28	Unused	D29	Unused
29	Unused	D30	Unused
30	Unused	D31	Unused
31	Unused	GND	Unused
32	Unused	+5V	Unused

UBIC signal pin-out matches that supported by MAX-657. Row B pin-out is fixed by the VME specification.

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TYPICAL VME P0 CONNECTOR PIN ASSIGNMENTS

The pin-out details for a VME64x 95 pin P0 connector will be as shown in Table 2.11.

TABLE 2.12: Pin-out for VME P0 Connector

Pin #	A	B	C	D	E
1	Unused	Unused	Unused	Unused	Unused
2	Unused	Unused	Unused	Unused	Unused
3	Unused	Unused	Unused	Unused	Unused
4	IO10	IO9	IO8	Unused	Unused
5	Unused	Unused	Unused	Unused	IO11
6	Unused	IO15	IO14	IO13	IO12
7	Unused	CAN2_L	Unused	CAN2_H	Unused
8	JTAG_TDI	JTAG_TDO	CAN1_L	Unused	CAN1_H
9	Unused	Unused	Unused	Unused	Unused
10	Unused	Unused	Unused	Unused	Unused
11	Unused	Unused	Unused	Unused	Unused
12	UBICA+	Unused	Unused	JTAG_TMS	JTAG_TCLK
13	IO1	EEPROM_DATA	GND	UBICA-	IO0
14	UBIC_MID5	IO3	UBICB-	IO2	UBICB+
15	IO4	UBIC_MID1	UBIC_MID2	UBIC_MID3	UBIC_MID4
16	IO7	Unused	Unused	IO6	IO5
17	Unused	Unused	Unused	Unused	Unused
18	Unused	Unused	Unused	Unused	Unused
19	Unused	Unused	Unused	Unused	Unused

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3 PROGRAMMING INTERFACE

INTRODUCTION

This chapter covers the following topics:

- memory map
- PMC-211 control and status register.

PROGRAMMING INTERFACE

ACCESS ABBREVIATIONS

Abbreviations used in this section are listed in Table 3.1.

TABLE 3.1: Access Abbreviations

Abbreviation	Meaning
R/W	Read/Write access
RO	Read Only writing has no effect
WO	Write Only reading produces meaningless data
N/A	Not Applicable when used for reset conditions, the reset is undefined
X	Don t care state field is ignored and not used

MEMORY MAP

The PMC-211 local bus shall have an address map as shown in Table 3.2.

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TABLE 3.2: PMC-211 Local Bus Address Map

Local Address	Access	Range
1000 01FF 1000 0100	CAN Controller 2	256 bytes[1]
1000 00FF 1000 0000	CAN Controller 1	256 bytes[1]
0FFF FFFF 0100 0000	unused	240M
00FF FFFF 00E0 0000	UBIC Interrupt Register	2M[2]
00DF FFFF 00C0 0000	Local Control and Status Register	2M[2]
00BF FFFF 0080 0000	UBIC	4M[3]

1. The CAN Controllers occupy 512 bytes, aliased together throughout their address space.
2. Each register occupies 1 word (4 bytes) aliased throughout its address space.
3. The UBIC occupies 32 words (4 bytes each) aliased throughout its address space.

The PCI address map of the PMC-211 is determined by configuration of the V360EPC internal registers. This would normally be done as part of PCI system configuration. Table 3.3 shows a typical address map, with all of the 32 bit PMC-211 devices mapped into PCI memory space, and the 8 bit devices mapped into PCI I/O Space.

The PCI address map of the PMC-211 is determined by configuration of the V360EPC PCI-to-Local-Bus Apertures, as programmed in internal registers.



Note

The PCI base address can be modified by programming V360EPC registers. The following sections describe the registers available within the address spaces shown in Table 3.5.

TABLE 3.3: Default PCI Memory and I/O Map

I/O or Memory Space	PCI Address Offset	Size	Name
I/O	0x0000 00FF 0x0000 0000	256 Bytes	Configuration Registers
I/O	0x0000 01FF 0X0000 0100	256 Bytes	Can 1
I/O	0x0000 02FF 0x0000 0200	256 Bytes	Can 2
Memory	0x00FF FFFF 0x00E0 0000	2 MBytes	UBIC Interrupt Register
Memory	0x00DF FFFF 0x00C0 0000	2 MBytes	Local Control and Status Register
Memory	0x00BF FFFF 0x0080 0000	4 MBytes	UBIC

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V360EPC CONFIGURATION SPACE

Table 3.4 defines the configuration registers in the V360EPC and their accessibility. The offset in the table is the location of each register with respect to the PMC-211 base configuration address. Refer to your basecard's *Hardware User's Manual* for the configuration address space.

TABLE 3.4: V360EPC Configuration Space Register (PMC Base Address + Offset)

Register	o your b configuration addres

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TABLE 3.4: V360EPC Configuration Space Register (Continued)(PMC Base Address + Offset)

Register				Offset
DM_LOCAL_ADDR0				84 H
DMA_CSR0	DMA_LENGTH0			88 H
DMA_CTLB_ADR0				8C H
DMA_PCI_ADDR1				90 H
DMA_LOCAL_ADDR1				94 H
DMA_CSR1	DMA_LENGTH1			98 H
DMA_CTLB_ADR1				9C H
Reserved				A0 - BC H
MAIL_DATA3	MAIL_DATA2	MAIL_DATA1	MAIL_DATA0	C0 H
MAIL_DATA7	MAIL_DATA6	MAIL_DATA5	MAIL_DATA4	C4 H
MAIL_DATA11	MAIL_DATA10	MAIL_DATA9	MAIL_DATA8	C8 H
MAIL_DATA15	MAIL_DATA14	MAIL_DATA13	MAIL_DATA12	CC H
PCI_MAIL_IERD		PCI_MAIL_IEWR		D0 H
LB_MAIL_IERD		LB_MAIL_IEWR		D4 H
MAIL_RD_STAT		MAIL_WR_STAT		D8 H
QBA_MAP				DC H
Reserved			DMA_DELAY	E0 H

82527 CAN CONTROLLER REGISTER DEFINITIONS

Table 3.5 defines the registers within the Intel 82527 CAN Controller and their accessibility.

TABLE 3.5: Intel 82527 CAN Controller Reg. Definitions (PMC Base Addr + CAN Offset + Addr Offset)

BASE+ Address Offset	Register Description	Access Rights
00H	Control Register	R/W
01H	Status Register	R/W
02H	CPU Interface Register	R/W
03H	Reserved	
04-05H	High Speed Read	RO
06-07H	Global Mask - Standard	R/W
08-0BH	Global Mask - Extended	R/W
0C-0FH	Message 15 Mask	R/W
10-1EH	Message 1	R/W
1FH	CLKOUT Register	R/W
20-2EH	Message 2	R/W

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TABLE 3.5: Intel 82527 CAN Controller Reg. Definitions (PMC Base Addr + CAN Offset + Addr Offset)

2FH	Bus Configuration Register	R/W
30-3EH	Message3	R/W
3FH	Bit Timing Register 0	R/W
40-4EH	Message 4	R/W
4FH	Bit Timing Register 1	R/W
50-5EH	Message 5	R/W
5FH	Interrupt Register	RO
60-6EH	Message 6	R/W
6FH	Reserved	
70H-7EH	Message 7	R/W
7FH	Reserved	
80-8EH	Message 8	R/W
8FH	Reserved	
90-9EH	Message 9	R/W
9FH	P1CONF	R/W
A0-AEH	Message 10	R/W
AFH	P2CONF	R/W
B0-BEH	Message 11	R/W
BFH	P1IN	R/W
C0-CEH	Message 12	R/W
CFH	P2IN	R/W
D0-DEH	Message 13	R/W
DFH	P1OUT	R/W
E0-EEH	Message 14	R/W
EFH	P2OUT	R/W
F0-FEH	Message 15	R/W
FFH	Serial Reset Address	WO

UBIC REGISTER DEFINITIONS

Table 3.6 defines the registers within the UBIC and their accessibility.

TABLE 3.6: UBIC Register Definitions (PMC Base Addr + UBIC Offset + Addr Offset)

BASE+ Address Offset	Register Description	Access Rights
00	Bus Time-out Constant	WO
08	No Command Time-out Constant	WO
10	No Response Time-out Constant	WO
18	Interrupt Acknowledge Time-out Constant	WO
20	Set-up register	WO

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TABLE 3.6: UBIC Register Definitions (PMC Base Addr + UBIC Offset + Addr Offset) (Continued)

28	Status Register	RO
30	Base Vector Number	WO
30	Physical Address Register	WO
38	Transmit Buffer	WO
40	Receive Buffer	RO

LOCAL CONTROL/STATUS REGISTER

Table 3.7 shows the bits that are provided in the Local Control/Status Register.

TABLE 3.7: Local Status Register Bit Definitions

31	30	29	28	27	26	25	24
SW[3]	SW[2]	SW[1]	SW[0]	RXB_EN	RXA_EN	UBIC_AVSEL	UBIC_MASK

Bit No.	Bit Name	Access	@Reset	Description
31	SW[3]	RO	X	CCA Configuration for Standard Product PMC-211. 0 (active low) = original PMC-211 (see document number 808280 for relevant information) 1 (active high) = new PMC-211
30	SW[2]	RO	X	CCA Configuration for Standard Product PMC-211. Reserved for future use, normally set to 0
29	SW[1]	RO	X	CCA Configuration for Standard Product PMC-211. If SW[3] = 1, then: 0 = no UBIC installed 1 = with UBIC installed Otherwise, 0 (as in the original PMC-211)
28	SW[0]	RO	X	CCA Configuration for Standard Product PMC-211. If SW[3] = 1, then: 0 = air-cooled version 1 = conduction cooled version
27	RXB_EN	R/W	1	UBIC Receiver Channel B Enable 0 = RXB held low at UBIC pin 1 = RXB follows transceiver signal
26	RXA_EN	R/W	1	UBIC Receiver Channel A Enable 0 = RXA held low at UBIC pin 1 = RXA follows transceiver signal
25	UBIC_AVSEL	R/W	1	UBIC Interrupt Vector Mode 0 = Vectored mode 1 = Auto-vectored mode
24	UBIC_MASK	R/W	0	UBIC Interrupt Mask Bit 0 = UBIC Interrupts Enabled 1 = UBIC Interrupts Masked
23:0	Reserved	RO	FFFFFF	Reserved for future use.

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UBIC IACK REGISTER

A read access to this register causes an Interrupt Acknowledge cycle to be generated to the UBIC. When the UBIC is in vectored interrupt mode, this read access also returns the UBIC Interrupt vector as shown in Table 3.8.

TABLE 3.8: UBIC Interrupt Register Bit Definitions

7	6	5	4	3	2	1	0
VBIT.7	VBIT.6	VBIT.5	VBIT.4	VBIT.3	VBIT.2	VBIT.1	VBIT.0

Bit No.	Bit Name	Access	@Reset	Description
31:8	Reserved	RO	NA	Reserved for future use.
7:0	Vector	RO	NA	UBIC Interrupt Vector

MIC REGISTER SET

The MEPCAM Interface Chip (MIC) register set is described in Table 3.10. Most registers are right justified in a 32-bit field, and occupy the least significant bits. The Physical Address/Base Vector Number Register is divided into bit fields, as shown in Table 3.9.

The PMC-211 only supports 32-bit accesses to the MIC registers. Incorrectly sized accesses will appear to terminate normally, but no action will have been taken (reads will return invalid data, writes will be non-destructive). Accesses which violate access rights will terminate in the same fashion.



Cross Reference

For detailed register descriptions, consult Vetronix Research Corporation's *MIC-3 Design Notes (July 1991)*.



Note

The MIC device is also known as the *UBIC* (Utility Bus Interface Chip).

TABLE 3.9: Physical Address/Base Vector Register Layout

31: 14	13: 8	7: 0
Not Used	Physical Address	Base Vector Number

TABLE 3.10: MIC Register Set

Address Offset	Description	Size	Access Rights
00_H	Bus Time-out Constant	16 Bits	WO
08_H	No Command Time-out Constant	16 Bits	WO
10_H	No Response Time-out Constant	10 Bits	WO

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TABLE 3.10: MIC Register Set

18_H	Interrupt Acknowledge Time-out Constant	10 Bits	WO
20_H	Setup Register	16 Bits	WO
28_H	Status Register	23 Bits	RO
30_H	Physical Address Register/Base Vector Number	14 Bits	WO
38_H	Transmit Buffer	32 Bits	WO
40_H	Receive Buffer	32 Bits	RO

VARIANT CONFIGURATION OPTIONS

The PMC-211 incorporates the Variant Configuration options as defined in Table 3.7. The variant configuration information is made available by accessing a register within the FPGA. Configuration resistors assign a different bit code for each PMC-211 variant. The PMC-211 PCI Bridge IC (V360EPC) provides PCI Subsystem ID and PCI Subsystem Vendor Configuration Registers.

All of the possible variants and CCA configuration are captured in the Control/Status Register found in the CPLD, at PMC base address + offset 0x00c0.0000.

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SAMPLE MEMORY MAP

Figure 3.1 provides an example of the resulting display when using the GPM "map" command to view the hardware map for the basecard and its installed PMC devices.

FIGURE 3.1: Sample Memory Map

```
SVME/DMV-179, PowerPC 750 General Purpose Monitor, Version 8.0
(c) DY 4 Systems Inc.

Type ? for help



48000000* map

                  Hardware map for the SVME/DMV-179

                  Base Addr.     Size      LM Addr.
                  ----------  ----------  ----------
              A24:  0x00480000  0x00080000  0x00000000
              A32:  0x48000000  0x07FFF000  0x00000000
                  ----------  ----------  ----------
       CFI1-4Mx16:  0xFF000000  0x01000000
       CFI1-4Mx16:  0xFE000000  0x01000000
             DRAM:  0x00000000  0x08000000
           NOVRAM:  0xF4008000  0x00008000
                  ----------  ----------  ----------
                  ----------  ----------  ----------

             Vendor Device HDR    Config        Memory Space Allocation
 Device name   ID     ID   TYPE Base Addr   BAR  PCI Base     Size       Type
 ----------- ------ ------ ---- ----------  --- ---------- ---------- -------
 GT-64130    0x11AB 0x6320 0x00 0x80000000   0  0x00000000 0x08000000 Memory
                                             4  0xF0000000 0x00001000 Memory
 Universe    0x10E3 0x0000 0x00 0x80003000   0  0xD0001000 0x00001000 Memory
                                             1  0xE0001000 0x00001000 I/O
 SYM53C885SC 0x1000 0x000D 0x80 0x80004000   0  0xE0000100 0x00000100 I/O
                                             1  0xD0000100 0x00000100 Memory
                                             2  0xD0002000 0x00001000 Memory
 SYM53C885ET 0x1000 0x0701 0x80 0x80004100   0  0xE0000000 0x00000100 I/O
                                             1  0xD0000000 0x00000100 Memory
 Unknown     0xD4D4 0x010F 0x00 0x80005000   0  0xE0002200 0x00000100 I/O
                                             1  0xE0002000 0x00000200 I/O
                                             2  0xD1000000 0x01000000 Memory

48000000*
```


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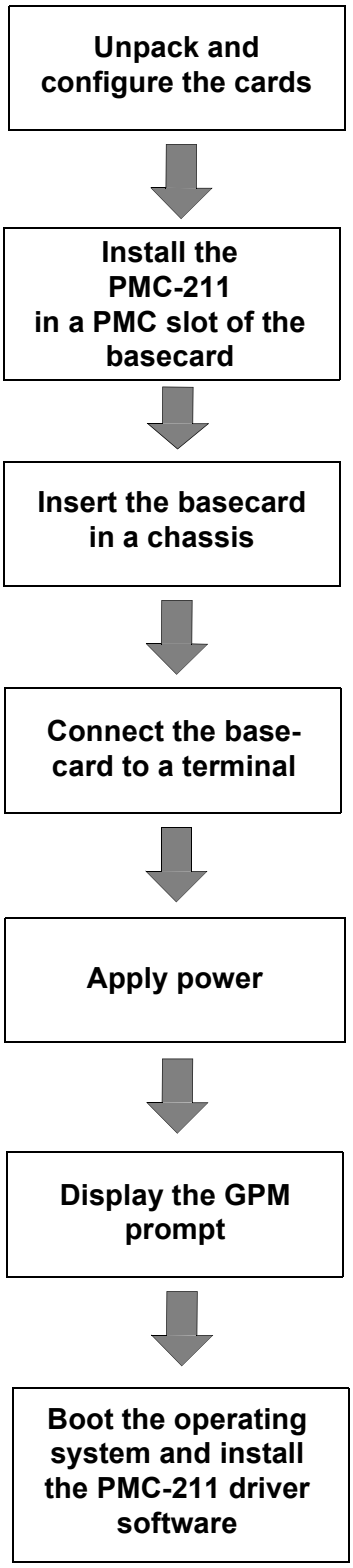
4 INSTALLATION INSTRUCTIONS

INTRODUCTION

This chapter explains how to install the PMC-211 on a Dy 4 PowerPC Single Board Computer (SBC) and verify that it is operating correctly.

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INSTALLATION PROCEDURE SUMMARY



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INSTALLATION PROCEDURE - DY 4 POWERPC BASECARD

BEFORE YOU BEGIN



Warning

This card uses components that are sensitive to electrostatic discharges. It must be kept in its conductive package until just before the installation begins. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card; static discharge can damage integrated circuits.

Turn the power off before inserting or removing cards from the VME chassis. Failure to do so could damage the card circuitry or cause personal injury.

UNPACK AND CONFIGURE THE CARDS

Before installing the card into a chassis, ensure that you complete the pre-installation tasks described in Chapter 2 of the *Getting Started Manual* for the basecard.



Cross Reference

See Tables 2.11 and 2.12 to obtain the P2/P0 interface pin out configuration.

INSTALL THE PMC-211 ON THE BASECARD

If you received your PMC-211 as a stand-alone product, install it in a PMC slot of your basecard using the Dy 4 mounting kit (901354-036 for SVME products and 901354-119 for DMV products).

When the PMC-211 is mounted in slot 1 (at the centre of the basecard), its I/O signals are available on the backplane P0 connector. When the PMC-211 is mounted in slot 2 (near the P2 connector), its I/O signals are available on the backplane P2 connector.

CHOOSING A VME SLOT LOCATION

Select Slot 1, the left-most slot in the VME chassis, if you want the basecard to be the System Controller (SYSCON). If you intend to use another card as the SYSCON, select the left-most unoccupied slot. All VME cards should be installed in adjacent slots; leaving empty slots may cause problems with interrupts and Bus Grant signals.

INSERT THE BASECARD IN THE CHASSIS

Ensure that the chassis power is turned off before inserting the card.

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An SVME basecard is equipped with a faceplate compliant with IEEE 1101.10. The large ejectors on this faceplate facilitate insertion of the basecard into the 160-contact, 5-row connectors for P1 and P2.

If the faceplate is not compatible with your chassis, you can purchase an alternate faceplate from Dy 4. Use the basecard generic drawing to determine how to mount the faceplate on the card.

With SVME basecards with the alternate faceplate and with DMV cards, proper mating of these connectors with the VME backplane requires a significant amount of insertion force. Use extra care when aligning and inserting your basecard into your chassis, to ensure that a secure mechanical and electrical connection is made between the card and the backplane mating connectors.

Insert the basecard in the selected slot in the chassis.

CONNECT THE BASECARD TO A TERMINAL

Connect the basecard to a terminal via either the front panel connector (SVME version only) or the P2/P0 connector (both SVME and DMV versions). Use the following settings for your terminal emulation software: 9600 baud, 8 data bits, no parity, 1 stop bit.

Using the Basecard Front Panel Connector

An SVME basecard has a single connector on the front panel that provides access to two EIA-232 serial channels (1 and 2). Some basecards also provide an Ethernet 10BaseT or 100BaseTX interface, plus a COP/JTAG interface for debugging purposes. The front panel cable routes the different interfaces to separate connectors.

For more information on the front panel cable, consult Chapter 3 of the Getting Started Manual for your basecard.

Using the Basecard P0 or P2 Connector

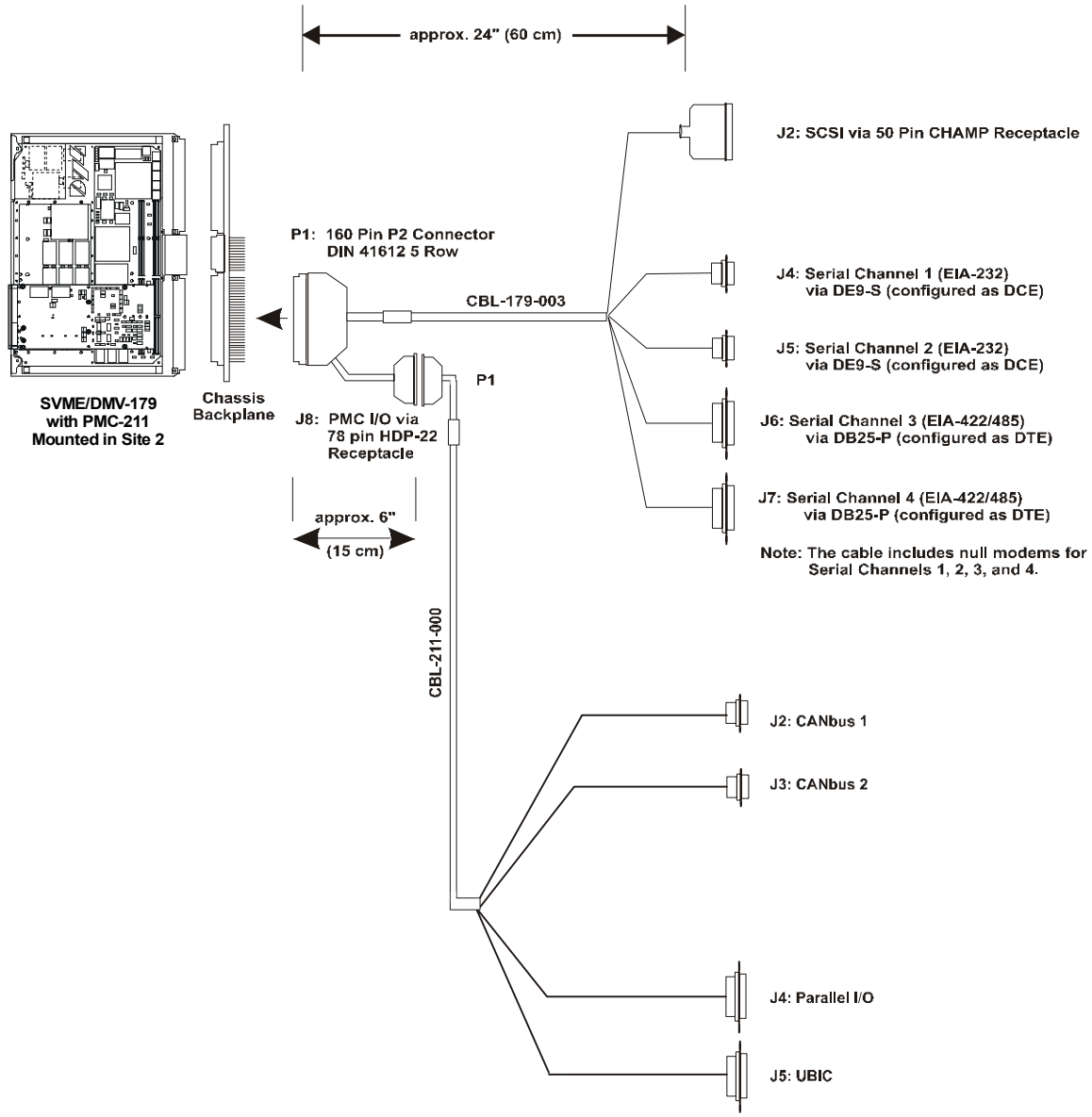
Consult Chapter 3 of the Getting Started Manual for your basecard for information about the P0 and P2 cables available for your basecard. Serial channel 1 is normally accessible on these cables.

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CONNECTING TO THE PMC-211 INTERFACES

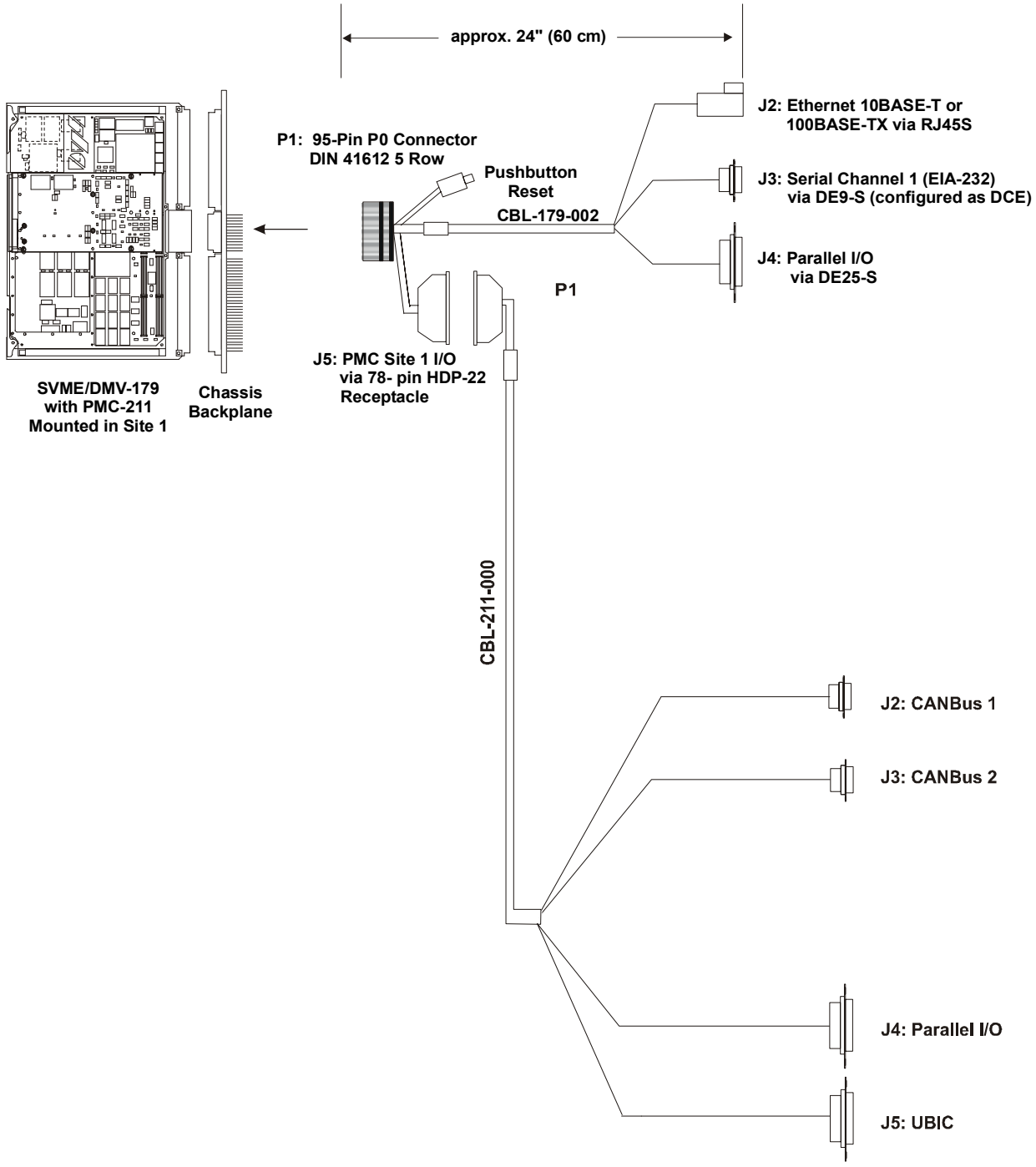
Cable number CBL-211-000 connects to a basecard P0 or P2 cable and provides access to the SPMC/DPMC-211 signals. This is illustrated in Figures 4.1 and 4.2.

FIGURE 4.1: Using the CBL-211-000 Cable with a Basecard P2 Cable



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FIGURE 4.2: Using the CBL-211-000 Cable with a Basecard P0 Cable



The mapping of CANbus 1 signals on the 9 contact D SUB plug connector (CBL-211-000 J2) is shown in Table 4.1.

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TABLE 4.1: CBL-211-000 J2 (CANbus 1) Signal Mapping

J2 Pin	Signal Name
J2-2	CAN1_L
J2-3	CAN1_H
J2-7	GND

The mapping of CANbus 2 signals on the 9 contact D SUB plug connector (CBL-211-000 J3) is shown in Table 4.2.

TABLE 4.2: CBL-211-000 J3 (CANbus 2) Signal Mapping

J3 Pin	Signal Name
J3-2	CAN2_L
J3-3	CAN2_H
J3-7	GND

The mapping of parallel I/O signals on the 25 pin D SUB receptacle (CBL-211-000 J4) is shown in Table 4.3.

TABLE 4.3: CBL-211-000 J4 (Parallel I/O) Signal Mapping

J4 Pin	Signal Name
J4-1	I/O0
J4-3	I/O1
J4-5	I/O2
J4-7	I/O3
J4-9	I/O4
J4-11	I/O5
J4-13	I/O6
J4-14	I/O7
J4-16	I/O8
J4-18	I/O9
J4-20	I/O10
J4-22	I/O11
J4-2, 6, 10, 17, 21	GND

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The mapping of UBIC signals on the 25 pin D SUB receptacle (CBL-211-000 J5) is shown in Table 4.4.

TABLE 4.4: CBL-211-000 J5 (UBIC) Signal Mapping

J5 Pin	Signal Name
J5-2	UBICA+
J5-4	UBICA-
J5-6	UBICB+
J5-8	UBICB-
J5-10	UBIC_MID5
J5-12	UBIC_MID3
J5-14	UBIC_MID1
J5-16	UBIC_MID4
J5-18	UBIC_MID2
J5-20	GND

APPLY POWER

Power up the chassis.

Immediately after the chassis is powered on, the red FAIL LED and green STATUS LED come on.

Once the basecard passes its initial diagnostics, the Card Level Diagnostics (CLD) routines turn the red FAIL LED off. If the CLD routines detect a failure, the red FAIL LED stays on. In either case, the green STATUS LED stays on.



Cross Reference

For additional information on the power-up sequence, refer to Chapter 3 of the *Getting Started Manual* for your basecard.



Cross Reference

If the red FAIL LED on the basecard stays on after power-up, then the CLD suite found one or more problems. Refer to “Troubleshooting” on page 4-9 for information about locating the problem.

DISPLAY THE GPM PROMPT

Press any key on the terminal keyboard to display the GPM prompt. The initial screen message shows the card’s VME base address, which should be 4000 0000 if the card is installed in Slot 1.

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Cross Reference

For information on the General Purpose Monitor (GPM), refer to Chapter 6 of the FFW User's Manual (808006).

BOOT THE OPERATING SYSTEM

Once the hardware is correctly configured and installed in the chassis, the next step is to boot the operating system.

VxWorks and the Dy 4 BSP

If you are using VxWorks, install the Board Support Package software (BSP). See the section "BSP Installation Procedure", in Chapter 1 of your BSP Software User's Manual. The BSP Software User's Manual is provided on the BSP CD-ROM. It is also installed in the Tornado tree when the BSP is installed.



Tip

There is also a BSP installation demo on the Technical Documentation CD-ROM.

INSTALL THE PMC-211 SOFTWARE

Follow the instructions in the PMC-211 Software User's Manual to install the PMC-211 software drivers.

TROUBLESHOOTING

Ensure that the basecard is properly seated in the chassis backplane mating connectors.

The PMC-211 does not require 3.3 V power. However, if a second PMC module is installed on the basecard, it can cause problems if it requires 3.3 V power and does not receive it. The SVME/DMV-178, SVME/DMV-179, and SVME/DMV-181 do not supply 3.3 V power to PMC modules. 3.3 V power is routed from the backplane, through the basecard, to the PMC module. Make sure that the backplane is properly wired to provide 3.3 V power.

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