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Data Sheet

SVME/DMV-183

Single/Dual Freescale™ Power Architecture™ MPC7447A/7448 Single Board Computer



Features

- Single or dual Freescale™ Power Architecture™ MPC7447A/7448 processors (AltiVec™ Technology-enhanced), each with:
  - 64 KB L1 cache
  - 512 KB/1 MB internal L2 cache
  - ECC option on MPC7448 internal L2 cache
  - AltiVec-enabled e600 core (previously referred to as G4 core)
  - 9.6 GFLOPS peak processing power at 1.2 GHz
- High-performance Discovery III system controller
  - Dedicated CPU-to-SDRAM path reduces memory read latency
- 512 MB or 2 GB of DDR SDRAM with ECC
- 128 MB to 512 MB of contiguous direct-mapped flash
  - Hardware flash write protection jumper
- PABS provides backup boot capability
- 128 KB AutoStore NVSRAM with hardware write protection
- Three Ethernet interfaces:
  - 1x 10/100Base-T to front panel
  - 1x GbE to P0 connector
  - 1x to P2 either 10/100Base-T or GbE depending on pin-out mode
- 2x 64-bit PMCs on independent PCI buses
  - 1x 100 MHz PCI-X, 1x 66 MHz PCI-X
  - Optimized cooling of conduction-cooled PMCs
  - Controlled impedance routing of Pn4 I/O for digital video, StarFabric, Fibre Channel and other high-speed interfaces
- 2x asynchronous RS-232 serial ports
- Up to 4 HDLC/SDLC-capable synch/asynch RS-232/422/485 serial channels with DMA support
- Up to 14 TTL discretes software-configurable as input or output, with interrupt capability as inputs
- Up to 16 RS-422/485 differential discretes, with interrupt capability on inputs
- Up to two MIL-STD-1553 channels
- Option for either 8-bit or 16-bit SCSI interface
- Option for two SATA 1.0 interfaces
- 2x USB 2.0 ports
- 4x general-purpose 32-bit user timers
- 4x general-purpose PCI/SDRAM DMA controllers
- 6x 32-bit OS timers, 3x per processor
- 2x avionics-style watchdog timers, one per processor
- Real-time Clock
- 4x on-board temperature sensors
- Tundra® Universe II VME64 master/slave interface with VME DMA
- Support for VME64x geographic addressing
- Basecard uses +5 V-only, backplane 3.3 V, 5 V, and +/-12 V are routed to the PMC sites
- Occupies single .8″ slot in all configurations
- Optimized conduction cooling with TherMax thermal frame and direct processor shunts

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- Debug monitor with system exerciser functions
  - Power-up BIT PBIT
  - Embedded Non-volatile Memory Programmer
  - Support for warm boot/cold boot determination
  - Declassification function to erase all non-volatile memories
- VxWorks®/Tornado™ integration:
  - Tornado 2.2.x and Workbench® 2.0
  - Full suite of drivers for hardware features
  - Run-time BIT libraries for Initiated and Continuous BIT
- INTEGRITY® BSP
- SSSL AltiVec-optimized DSP library
- LynxOS® BSP
- Available in a range of ruggedization levels, both air- and conduction-cooled

Overview

Using single or dual Motorola® MPC7447A/ 7448 processors with AltiVec™ technology and up to 2 GB of state-of-the-art DDR SDRAM, the SVME/DMV-183 represents the latest advancement in functionality and performance for rugged single board computers (SBCs). With two 64-bit PMC sites, one supporting 100 MHz PCI-X, and an innovative complement of I/O capability such as GbE, up to six serial ports, up to two MIL-STD-1553 channels, SCSI, SATA, and two USB 2.0 ports, the SVME/DMV-183 satisfies the most demanding requirements of embedded computing applications. Available in a full range of environmental build grades the SVME/DMV-183 is targeted to the challenging data- and digital signal-processing needs of tactical aircraft, armored vehicles and harsh environment naval systems.

For retrofit and technology insertion applications, the SVME/DMV-183 offers a superset of the I/O features of earlier generations of Curtiss-Wright Controls Embedded Computing 17x and 18x Freescale™ Power Architecture™ SBCs and optional pin-out modes for backplane compatibility as well. As a member of Curtiss-Wright's continuously evolving stream of SBCs including the SVME/DMV-178, SVME/DMV-179, SVME/DMV-181, and SVME/DMV-182, the SVME/DMV-183 supports the life-cycle model of successive technology insertions throughout a platform's lifetime.

Powerful Core Architecture

Figure 1 illustrates the core processing architecture of the SVME/DMV-183. Two powerful MPC7447A/7448 processors connect via the MPX bus to the advanced GT-64460 Discovery III system controller. The Discovery III system controller bridges the MPX bus of the two processors to the DDR SDRAM bus, two 64-bit PCI busses, and a high-performance device bus on which the flash EPROM and non-PCI peripherals are found. The powerful crossbar fabric internal to the Discovery III device allows for concurrent data transfers to take place on the various busses of the SVME/DMV-183. Examples of data transfers that can occur concurrently on the SVME/DMV-183 include:

- Processor accesses to flash concurrent with PCI-SDRAM transfers on either PCI bus
- Processor accesses to one PCI bus concurrent with PCI-SDRAM transfers on the other PCI bus
- Processor accesses to on-chip peripherals (Ethernet and serial ports) concurrent with PCI-SDRAM transfers on either PCI bus

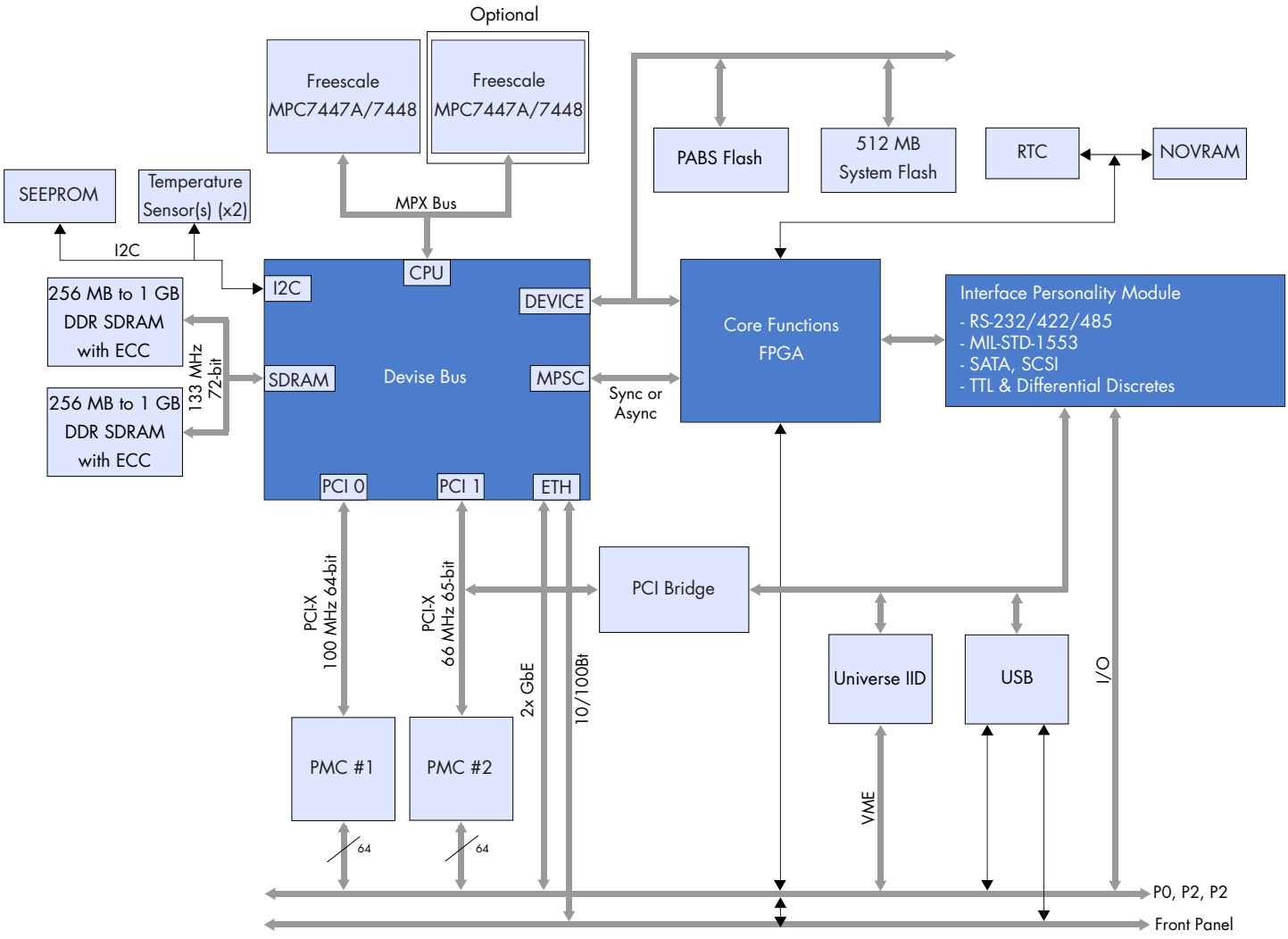
The SVME/DMV-183 provides hardware-enforced cache coherency with respect to accesses to SDRAM from PCI and bus mastering peripherals, freeing driver software developers from the complexity of managing cache coherency in software. For applications requiring the highest-possible PCI-SDRAM performance, hardware-enforced cache coherency can be disabled.

The Core Functions FPGA is a Spartan-3 1000 device that implements a number of important SVME/DMV-183 features including asynchronous serial ports, interrupt control, system timers, watchdog timers, TTL discrete I/O and differential discrete I/O control registers. In addition, the Core Functions FPGA bridges the Discovery device bus to the flash array and to a peripheral bus that interfaces to the Real-Time Clock (RTC) and NVSRAM. To increase the serviceability of the SVME/DMV-183 over the long life-cycles of the military/aerospace programs for which it is designed, the Core Functions FPGA is In-System Programmable (ISP) and can be reprogrammed in the field.

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Figure 1: SVME/DMV-183 Core Processing Architecture



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PCI Bus 1 is a 64-bit, 100 MHz-capable PCI-X bus that is dedicated to PMC Site 1. Offering a peak PCI transfer rate of 800 MB/s, PMC Site 1 has the necessary bandwidth to support high-performance PMC modules such as Fibre Channel NICs, graphics controllers, fabric interfaces, and custom high-speed devices. PCI bus 2 is a 64-bit, 66MHz-capable PCI-X bus serving PMC site 2 and a PCI to PCI bridge which connects to the low-speed PCI peripherals.

Discovery III Controller Delivers Full Potential of PowerPC MPX Bus

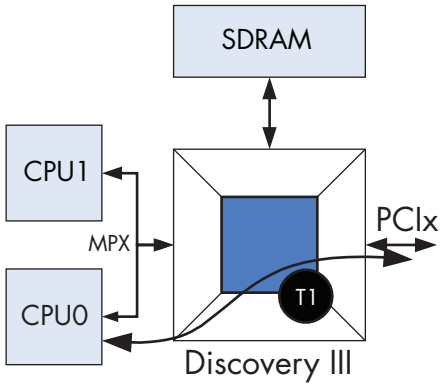
The SVME/DMV-183's Discovery III system controller provides optimum support for the Power Architecture's advanced MPX bus interface in a dual processor configuration, providing the following performance features:

- Split transactions, illustrated in Figure 2, allows faster accesses such as to DDR SDRAM to complete in advance of an access to a slower device such as flash or a PCI peripheral that was initiated first
- Data intervention, explained further below, allows a cached copy of data found in the cache of one processor to be transferred directly to the second processor
- Address streaming; no dead cycles between consecutive address tenures driven by the same device
- Data streaming, no dead cycles between consecutive data phases driven by the same device
- A direct path between the MPX bus and system memory, which significantly reduces memory-read latency compared to the earlier Discovery II device

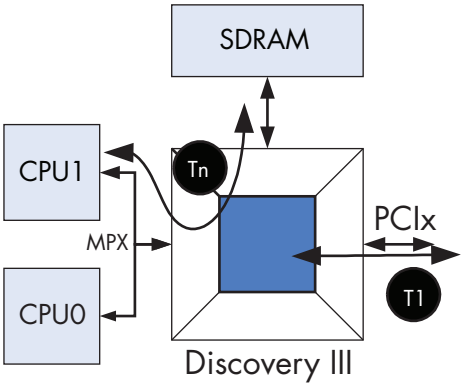
Support for the split transaction feature of the MPX bus allows the Discovery III system controller to provide data from high-speed targets such as SDRAM between the address and data phases of a transaction targeting a lower-speed peripheral.

Figure 2: Split Transaction Feature Support

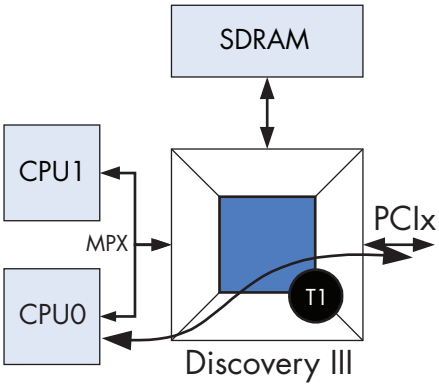
CPU0 initiates transaction T1 to a slower target such as a PCI peripheral.



While transaction T1 is in process on the PCI bus, one or more transactions, Tn, to a faster target such as SDRAM can take place from either CPU.



When data from the PCI peripheral is available, it is driven unto the MPX bus.



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Data Intervention with the Discovery III

If a processor using the MPX bus protocol performs a read of data that exists modified in another processor's cache, the modified data can be directly forwarded to the requesting processor. Systems based on the 60x bus, in comparison, would require that the cached data be pushed back to memory, the requesting cycle retried, and the data finally obtained from memory. Data Intervention allows the latency for data that exists in another processor's cache to be reduced from 20 clock cycles or more to as low as 5 or 6 cycles. See Figure 3.

Flexible I/O with Interface Personality Modules (IPMs)

Figure 4 illustrates the SVME/DMV-183's feature-rich I/O subsystem. I/O features integral to the SVME/DMV-183 basecard include VME, two RS-232 ports, three Ethernets, two USB 2.0 ports, card fail status out, card reset input, and ALT-BOOT input.

Figure 3: Data Intervention

When a processor sees a cache-line read operation on the MPX bus (1) for data which is in its cache in a modified state, it will intervene and provide the data directly to the requesting processor. (2). This is known as Data Intervention.

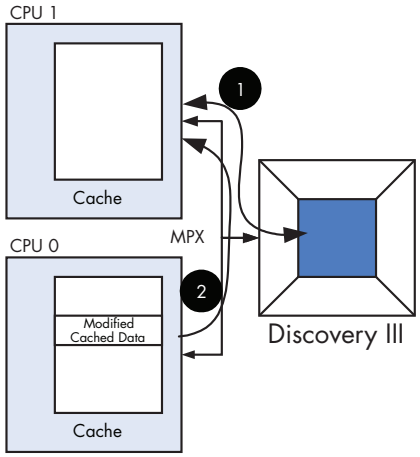
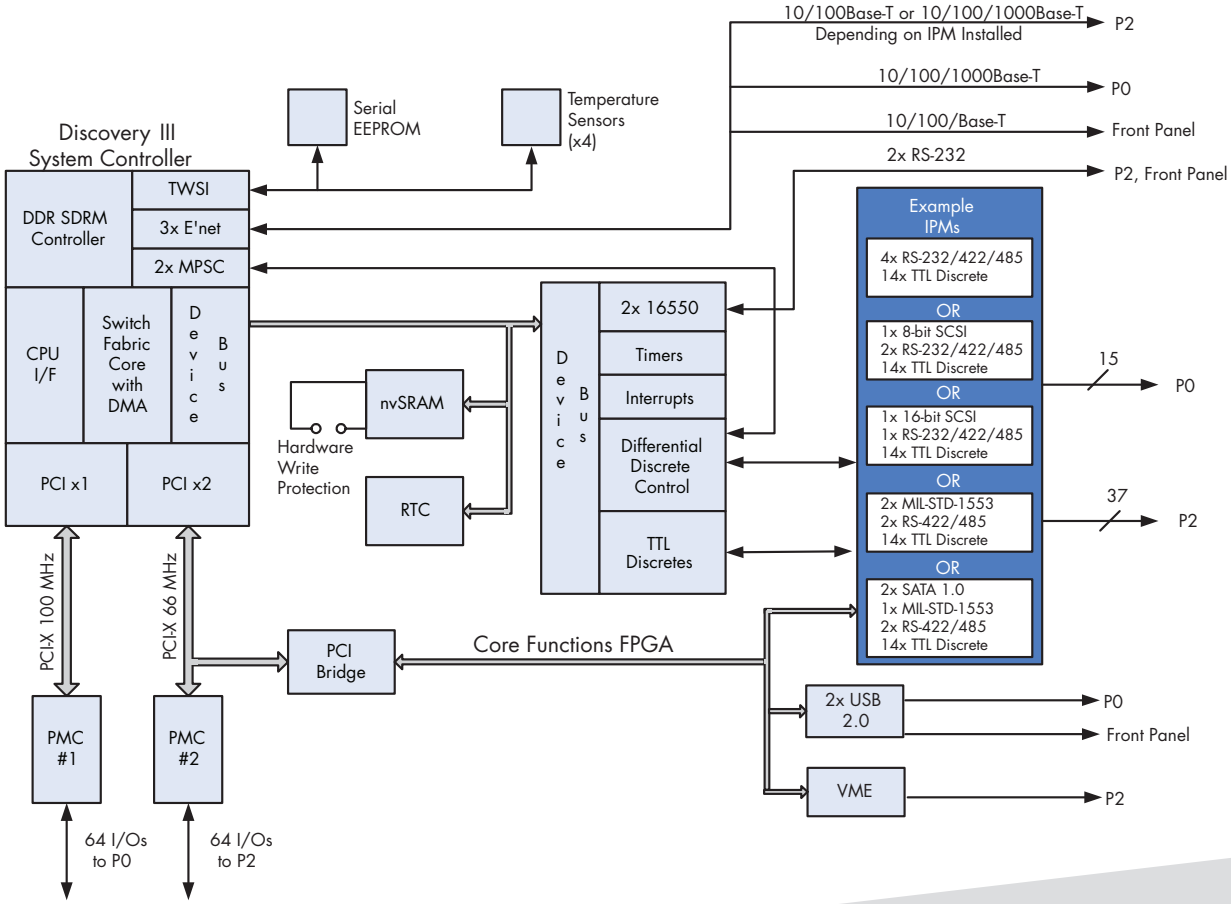


Figure 4: 183 I/O Subsystem



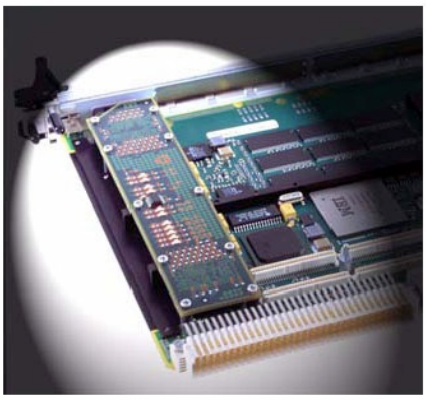
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SVME/DMV-183 I/O Subsystem Architecture

I/O can be expanded by the addition of IPMs that work in conjunction with the Core Functions FPGA. The IPM is a connectorized subassembly that can either simply provide physical-level transceivers for controller devices implemented in the Core Functions FPGA or can host PCI peripherals such as a SCSI interface device. The combination of the large FPGA on the SVME/DMV-183 basecard and the IPM for physical level tailoring provides the SVME/DMV-183 with a flexible means to incorporate product improvements and custom requirements.

Figure 5: Interface Personality Module (IPM) Adds Flexibility



Designed for Harsh Environments

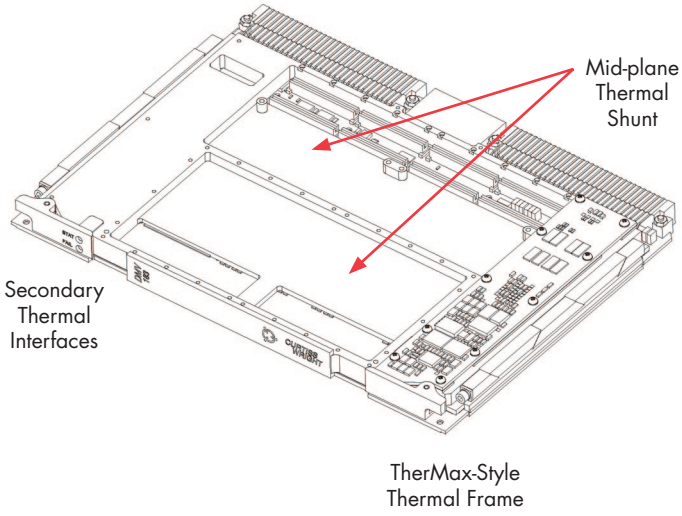
To cost-effectively address a diverse range of military/aerospace applications, the SVME/DMV-183 is available in a range of ruggedization levels, both air- and conduction-cooled. All versions are functionally identical, with air-cooled versions (SVME) available in Curtiss-Wright ruggedization levels 0 and 100, and conduction-cooled versions (DMV) in levels 100 and 200. Air-cooled level 200 is available on a special order basis. Curtiss-Wright's standard ruggedization guidelines define the environmental tolerance of each ruggedization level (see the Curtiss-Wright Ruggedization Guidelines factsheet for more information).

Enhanced Thermal Management for Conduction-Cooled Applications

For those demanding application environments that require conduction-cooling, the SVME/DMV-183 uses a combination of thermal management layers within the Printed Wiring Board (PWB) and an aluminum thermal frame that provides a cooling path for the PMC sites and for high-power components such as the processors, caches, and bridge device. The SVME/DMV-183 thermal frame employs a number of innovative design techniques to keep the temperature rise of the electronic components to a minimum, thus increasing the long-term reliability of the product:

- Direct processor thermal shunts
- Provision of both primary and secondary thermal interfaces on PMC sites
- Mid-plane thermal shunts for PMC sites
- TherMax design approach
- Full-width thermal interface to back-side slot wall

Figure 6: Representative Thermal Frame



Mid-plane Thermal Shunts for PMCs

To optimize the conduction-cooling of high-performance, high-power PMC modules such as graphics or networking PMCs, the SVME/DMV-183 thermal frame incorporates mid-plane thermal shunts for the PMC sites. High-power PMCs can include a mating cooling surface on the PMC module to contact the mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC modules can significantly lower the heat rise from the SVME/DMV-183 card edge to the PMC components. The midplane thermal shunt does not impinge on the VITA 20- allowed component height.

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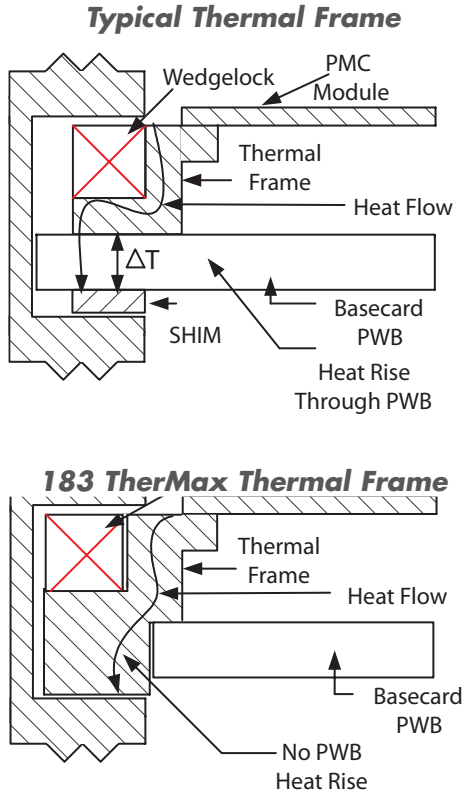


TherMax-style Thermal Frame

A TherMax thermal frame provides an unbroken metallic path from the PMC sites and shunted components to the back-side cooling surface of the card, therefore minimizing the temperature rise to these devices. In comparison, a typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB which has a high thermal resistance compared to aluminum.

Figure 7: TherMax diagram

A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame

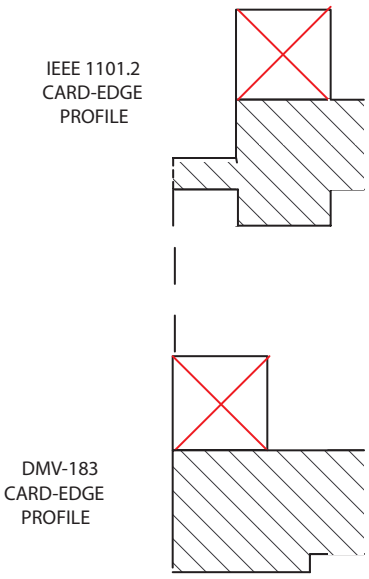


Full-width Thermal Interface to Back-side Slot Wall

To minimize the temperature rise from the mating slot wall of conduction-cooled enclosures to the back-side thermal interface region of the SVME/DMV-183, the SVME/DMV-183 thermal frame maximizes the thermal interface area by extending the frame to the full width of the card, as illustrated in Figure 9. This deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis, has the benefit of lower card operating temperatures and increased long term reliability. During test and integration activities where it may be desirable to install a conduction-cooled SVME/DMV-183 into an air-cooled card-cage, this can normally be accomplished simply by removing the card guides.

Figure 8: Card-edge Profile Deviates from IEEE 1101.2

DMV-183 Card-edge Profile is Optimized to Provide a Full-width Thermal Interface to the Back-side Slot Wall



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Advanced MPC7447A/7448 Processors

The SVME/DMV-183 is equipped with two high-performance MPC7447A/7448 processors, advanced fourth generation members of Motorola's broad family of Power Architecture family of 32/64-bit RISC microprocessors. Developed for a wide range of embedded computing applications, the MPC7447A/7448 provides industry-leading performance per watt. The SVME/DMV-183's processors run at speeds of up to 1.2 GHz on-chip.

The MPC7447A/7448 processor incorporates Freescale's powerful AltiVec Technology, which enhances the architecture through the addition of a 128-bit vector execution unit. The vector unit provides for highly parallel operations, allowing for the simultaneous execution of up to 16 integer operations or eight floating point operations per clock cycle. For two processors each operating at 1.2 GHz, this translates to a peak theoretical computational rate of 19.2 GFLOPS.

Table 1: Split Transaction Feature Support

Processor	MPC7447A @ 1.0 GHz	MPC7448 @ 1.2GHz
Dhrystone 2.1 MIPS	2,710 (1)	3,252 (2)

1. Freescale Power Architecture MPC7447A factsheet, MPC7447AFS Rev a
2. Extrapolated from MPC7447A data

Multiprocessor Support Features

The SVME/DMV-183 provides a number of important features to allow the applications software running on the two processors to communicate efficiently and to share the hardware resources of the board. These consist of the following:

- SMP-style shared memory, providing each processor with a uniform view of the board memory map, including flash and SDRAM
- Doorbell interrupt registers
- Semaphore registers
- Powerful interrupt mapping logic SDRAM for semaphore operations, creating additional contention for that critical resource

Doorbell Interrupt Registers

Implemented within the Discovery III system controller, the SVME/DMV-183 has a doorbell interrupt register for each processor. The doorbell interrupt registers allow for processor-to-processor interrupts, PCI-to-processor interrupts, or for a processor to interrupt itself.

Semaphore Registers

Implemented within the Discovery III system controller, the SVME/DMV-183 has a total of eight high-speed hardware semaphore registers that can be used as locks for resources being shared between the two processors and/or a PCI device. Having dedicated hardware semaphores can avoid having the processor access SDRAM for semaphore operations, creating additional contention for that critical resource.

Powerful Interrupt Mapping Logic

Through a combination of the Discovery III system controller and logic implemented in the Core Functions FPGA, the SVME/DMV-183 allows the hardware to adapt to the needs of the software by providing a means to route all interrupts sources (PMCs, VME, PCI, peripherals, etc.) to either or both processors. This feature speeds interrupt response time by routing the interrupt directly to the intended processor.

Up to 2 GB of Dual Data Rate (DDR) SDRAM

Current main memory options for the SVME/DMV-183 include 512 MB or 1 GB of high-performance DDR SDRAM. Future component availability will allow for up to 2 GB of SDRAM. To preserve data integrity, the SDRAM is provided with ECC circuitry that detects and corrects all single-bit data errors, detects all double bit errors, and detects all three and four bit errors within the same nibble. With ECC enabled, the instantaneous peak data transfer rate to the DDR SDRAM is 2.0 GB/s. The DDR SDRAM is accessible from the processor and from both PCI busses. Via the Universe II™ PCI-to-VME interface, the DDR SDRAM is also accessible from the VMEbus.

Up to 512 MB of Flash Memory

Current options for the SVME/DMV-183 include 128 MB or 256 MB of flash memory. Future component availability will allow for up to 512 MB of flash. The SVME/DMV-183 flash is contiguous, directly-accessible, high-speed flash memory using AMD S29GL512 devices. The flash devices are specified for a minimum of 100,000 program-erase cycles and a data retention time of 20 years at 125 °C.

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Read performance of the flash array is optimized in order to minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical, and execution directly from flash without first cross loading to SDRAM is advantageous.

Optimizations include:

- 32-bit wide flash array
- 100 MHz device bus operation
- Support for burst reads at 30 nsec.

For absolute security against inadvertent flash programming or corruption, a hardware jumper is provided to disable the Write Enable line to the flash devices. Cards are configured for shipment with flash reprogramming enabled in hardware.

Flash memory is reprogrammable on-board using Curtiss-Wright's NVM Programmer utility embedded into the standard Foundation Firmware.

Protected Access Boot Site (PABS)

PABS provides a backup boot capability in the event that the foundation firmware in the main Flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main flash without removing the card from the system in which it is installed. When a P0 backplane pin is asserted the SVME/DMV-183 will boot from PABS, and run a reduced version of Curtiss-Wright's standard Foundation Firmware that will allow users to reinstall the standard firmware load.

256 KB High-speed SRAM

Incorporated into the Discovery III system controller, the SVME/DMV-183 provides 256 KB of high-speed SRAM directly on the processors' MPX bus. While useful as a general-purpose high-performance memory area that off-loads traffic to SDRAM, the high-speed SRAM is particularly beneficial for holding descriptors for Discovery III peripheral devices, allowing DMA units to simultaneous access data from SDRAM while descriptors are accessed from the SRAM.

128 KB of AutoStore NVSRAM

A Simtek 14CA8N 45 nsec. AutoStore NVSRAM provides fast, non-volatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes the AutoStore NVSRAM just like standard SRAM, with no special programming algorithm required. Upon detecting a power loss on the +5 V rail, an AutoStore cycle is performed and all 128 KB are automatically transferred from the on-chip SRAM to the on-chip EEPROM using energy stored in an on-board capacitor. At the next power-up a recall cycle is performed to transfer the EEPROM contents back to the SRAM, where the application code can now utilize the stored data to continue normal operation. The number of recall cycles is unlimited: the maximum number of store cycles is 1,000,000 and the data retention period is 100 years.

For security against inadvertent writes to NVSRAM, a hardware jumper is provided to disable the Write Enable line to the device. Cards are configured for shipment with NVSRAM reprogramming enabled in hardware.

Serial EEPROM

The SVME/DMV-183 provides 512 bytes of Serial EEPROM for storing configuration data used by card initialization firmware.

Three Ethernet Interfaces

The SVME/DMV-183 is equipped with three Ethernet interfaces, all implemented within the Discovery III system controller device. ENETFP is 10/100Base-T capable and routed to both the front panel. ENETP0 is GbE-capable and is routed to the P0 connector. ENETP2 is connected to the P2 connector and is either 10/100- or GbE-capable depending on the particular I/O mode - see Table 3.

The Discovery III Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9 KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence.

Optional 8/16-bit SCSI-2 Interface

The SVME/DMV-183 optionally provides a single-ended, 8-bit or 16-bit Ultra SCSI (SCSI-2) interface, based on the LSI Logic 53C875 SCSI controller. The 53C875 is a highly autonomous device and transfers data to and from PCI via an internal SCSI DMA controller and an associated DMA FIFO, minimizing the loading of the main processors by SCSI traffic. As a PCI master the 53C875 is capable of zero wait-state data bursts at 132 MB/s, conserving both PCI bus and main memory bandwidth.

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In 16-bit mode the device supports peak transfer rates of 40 MB/s synchronous and 14 MB/s asynchronous. In 8-bit mode peak transfer rates on the SCSI bus are 20 MB/s in synchronous mode and 7 MB/s asynchronous.

See Table 3, I/O Options, for information on I/O options that include SCSI.

Option for Two SATA 1.0 Interfaces

The SVME/DMV-183 optionally provides two SATA 1.0 (1.5 GB/s) interfaces based on the Silicon Image 3124 device. Each interface incorporates several performance-enhancing features such as:

- Independent DMA channel with 2 K FIFO
- Independent command fetch, scatter/gather, and command execution

See Table 3, I/O Options, for information on I/O options that include SATA.

Two RS-232 Serial Ports

Serial channels 1 and 2 are RS-232 serial ports implemented with a 16550-based controller built into the Core Functions FPGA. A base clock of 36.864 MHz allows for all standard asynchronous baud rates from 50 baud to 11 5.2 Kbaud. The baud rate of each port can be set independently. The DSR signal on serial channel 1 is used as a cable detect signal to force the card to boot into the General Purpose Monitor.

On air-cooled cards the two RS-232 channels are accessible on the front panel in addition to being available on the rear-panel on both air- and conduction-cooled cards.

Option for Up to Four RS-232/422/485 Serial Ports

Up to a total of four asynchronous- and synchronous-capable RS-232/422/485 ports are available on the SVME/DMV-183.

Serial channels 3 and 4 are implemented with the Discovery III's Multi-Protocol Serial Controllers (MPSC). These powerful serial controllers handle standard asynchronous and synchronous HDLC/SDLC. In synchronous mode a full range of data encoding schemes are supported (NRZ, NRZI Mark, NRZI Space, FM0, FM1, Manchester, and Differential Manchester). Based on an input clock of 133 MHz, all standard asynchronous baud rates up to 11 5.2 Kbaud are provided as well as synchronous bit rates up to 5 Mbits/s for NRZ clock mode, 2.5 Mbits/s for clock-encoded modes (FM0, FM1,etc.). The Discovery III MPSC ports are equipped with dedicated DMA controllers to off-load the processors from handling serial data traffic to and from the controllers.

The choice of physical level (RS-232 or RS-422/485) for the MPSC serial channels is software selectable on a per-channel basis via a control register within the Core Functions FPGA.

Serial channels 5 and 6 are implemented with a 85230-based core integrated into an FPGA on the Serial IPM. Asynchronous communication at baud rates from 1200 to 11 5.2 Kbaud, and synchronous HDLC/SDLC data rates up to 2.0 Mb/s are provided. To support high data rate applications without excessive loading of the processors, dedicated serial DMA controllers are provided. The choice of physical level (RS-232 or RS-422/485) for the 85230-based serial channels is software selectable on a per-channel basis via.

See Differential Discrete I/O below for information on how the SVME/DMV-183 provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals for use as serial control signals or general purpose I/O.

See Table 3, I/O Options, for information on which serial I/O channels are available for the different I/O options.

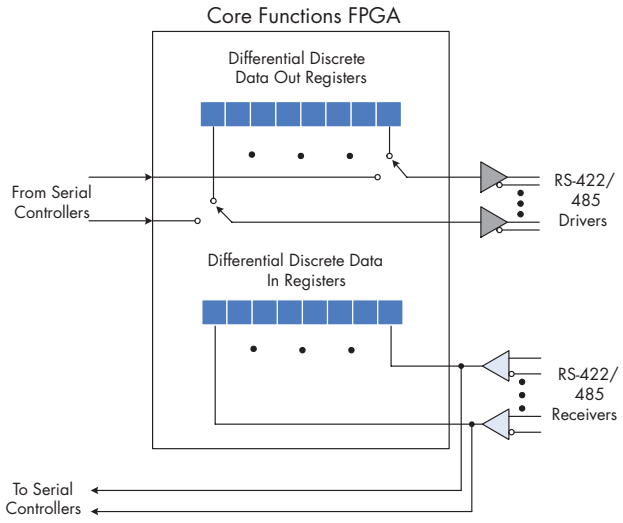
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Up to 16-bits of Differential Discrete Digital I/O

The SVME/DMV-183 provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals via registers in the Core Functions FPGA. This allows flexibility in how the drivers and receivers are used. The choice of whether the drivers and receivers are attached to serial ports or used as discrete differential I/O is software selectable on a per-serial channel basis. When configured as discrete differential I/O, the drivers and receivers can be used as serial-line control signals (RTS, CD, etc.) in conjunction with another serial channel, or used as general-purpose differential mode control signals unrelated to serial I/ O requirements. Differential discrete inputs can generate an interrupt upon a change of state, with programmable edge direction. Note that if the serial channel physical levels are set to RS-232, then discrete digital I/O at RS-232 levels is obtained.

Figure 9: Discrete Differential I/O Option for Discrete Control of RS-422/485 Drivers and Receivers



Two USB 2.0 Ports

The SVME/DMV-183 incorporates an NEC uPD720100 which provides two USB 2.0-capable ports in a 32-bit, 33 MHz PCI 2.2-compatible device. Each port can handle high-speed (480 MB/s), full-speed (12 MB/s), and low-speed (1.5 MB/s) operation. When operating at low- speed or full-speed, each port is managed by independent OHCI-compliant controllers internal to the device. One EHCI-compliant controller manages any ports operating in high-speed mode. One USB port is accessible on the front panel connector only, the other is accessible on the P0 connector only. Each port provides a fused +5 V output to power low-power USB devices such as keyboards.

14-bits of LVTTL

The SVME/DMV-183 optionally provides 14-bits of LVTTL-compatible discrete digital I/O. Each bit is individually programmable to be an input or output. In addition, each bit is capable of generating an interrupt upon a change of state, with the edge direction (high-to-low, low-to-high) also being programmable. Each bit has a 10K pull-up resistor to 5 V. Output drive current is
24 mA.

Real-time Clock (RTC)

A Maxim/Dallas Semiconductor DS1501 RTC chip provides the RTC function. It contains registers for century, year, month, day, hours, minutes, and seconds. The RTC is capable of generating alarm interrupts.

The RTC draws its power from the standard +5 V input during normal operation. In the event of loss of +5 V power, the RTC will automatically switch over to draw current from the +5 V STDBY line.

Extensive Timing Resources

The SVME/DMV-183 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in Table 2.

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Avionics Watchdog Timers

The SVME/DMV-183 provides two watchdog timers, one for each processor. Each watchdog timer is a presettable downcounter with a resolution of 1 usec. Time periods from 1 usec to 16 seconds can be programmed. Initialization software can select whether a watchdog exception event causes an interrupt or a card reset. Once enabled to cause a reset, the watchdog cannot be disabled. A watchdog time- out log bit tells start-up code whether the last card reset was due to a watchdog exception. The SVME/DMV-183 provides a software-selectable option to configure a discrete digital output to act as an External Watchdog Time-out Indicator, one for each watchdog timer.

The watchdog timer can be used in two ways. Used as a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. (i.e., writing to the watchdog register either too soon or too late causes an exception event.)

Four General Purpose DMA Controllers

Four DMA controllers provided by the Discovery III bridge chip are available for general purpose use. The four general purpose DMA controllers can be used for transferring blocks of data between the SDRAM, flash memory, device bus peripherals, and the PCI busses without loading down the Power Architecture CPU. The General Purpose DMA controllers are capable of sustaining burst transfers using the full 64-bit width of the PCI bus. Advanced features include DMA chaining and the ability to schedule DMA transfers via a general-purpose timer.

For transferring large blocks of data over the VMEbus, it is recommended that the DMA controllers internal to the Universe II device be used rather than the two general purpose DMA controllers. This is because the Universe II DMA controllers are capable of supporting maximum-size MBLT block sizes on the VMEbus.

Table 2: SVME/DMV 183 Timing Resources

Timer Facility	Implementation	Type	Size	Tick Rate/ Period	Maximum Duration
PowerPC Time Base Register	One per CPU	Free running counter	64-bit	33.33MHz/30.0 nsec.	17,549 years
PowerPC Decrementer	One per CPU	Presettable, readable downcounter	32-bit	33.33MHz/30.0 nsec.	128.8 sec.
General Purpose #0-3	Discovery III	Presettable, readable downcounter with autoreload or stop options	32-bit	133.33MHz/7.5 nsec.	32.2 sec.
RTC Alarm Interrupt	RTC	Alarm interrupt	-	Specific day, hour, minute, and second	-
Watchdog Timers (one per CPU)	Core Functions FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	24-bit	1MHz/1 usec.	16.77 sec.
System Timers #1-6	Core Functions FPGA	Presettable, readable, downcounters with interrupt on terminal count	32-bit	50MHz/20 nsec.	85.9 sec.

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Option for Up to Two MIL-STD-1553 Channels

The SVME/DMV-183 provides up to two MIL-STD-1553 channels implemented with DDC 65864 PCI micro-ACE TE devices offering the following key features:

- Support for MIL-STD-1553A, MIL-STD-1553B Notice 2, and STANAG 3838 protocols
- BC, RT, MT modes independently selectable for each channel
- Choice of transformer-coupled (standard) or direct-coupled outputs (on a special order basis)
- MIL-STD-1760 amplitude compliant
- 64 K words of RAM per channel, with parity
- PCI interface is 33 MHz, 32-bit and supports burst writes with a FIFO for up to one complete MIL-STD-1553 message
- Transmit Inhibit input for each channel
- Bus Controller features:
  - Highly autonomous bus controller with built-in message sequence control engine for multi-frame message scheduling, branching, and asynchronous message insertion
  - Programmable inter-message gap size
  - Single frame or auto-repeat modes
  - Automatic retries
  - Time-tag can be transmitted with Synchronize with Data mode code
  - External Trigger input for each channel
- Remote Terminal features
  - Programmable illegalization of RT commands
  - Busy bit programmable on a sub-address basis
  - 16-bit time-tag option with options of 2, 4, 8, 16, 32, or 64 µsec/LSB based on internal clock
  - External time-tag clock input
  - Time-tag can be set via Synchronize With Data mode code
  - External Subsystem Flag input
- Monitoring Terminal features
  - Selective message monitor mode, use for selecting monitoring based on RT address, Transmit/Receive bit, and Sub-address
  - Simultaneous RT and monitor modes

The RT address for each channel can be set by software. Also, for each channel a backplane configuration input is provided that can independently select an option whereby the RT address can be set by using a subset of the TTL discrete digital I/O lines.

To meet the MIL-STD-1760 First Response requirement of an RT response within 150 msec, one of the MIL-STD-1553 channels initializes as an RT with the Busy status word bit set. This requires that the MIL-STD-1553 channel be configured to set the RT address in hardware.

Curtiss-Wright's driver software for the SVME/DMV-183's MIL-STD-1553 channels provides a flexible, easy to use, and robust applications programming interface (API). The driver supports BC, RT, and MT modes of operation, and offers a high degree of compatibility to the proven software driver provided for Curtiss-Wright's popular PMC-601 MIL-STD-1553 module. Source code is provided for user reference.

The MIL-STD-1553 driver for the SVME/DMV-183 is sold separately from the hardware and the SVME/DMV-183 Board Support Packages. See separate datasheet for details.

Figure 10: Interface Personality Module with MIL-STD-1553



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VME Interface

The 64-bit PCI architecture of the SVME/DMV-183 combined with the Universe II's 64-bit PCI interface and extensive decoupling FIFOs allow for high-speed, bandwidth efficient data transfers between the VMEbus and on-board memory and PCI targets. VME data can be transferred at the full sustained rate of 50+ MB/s supported by the Universe II while only consuming only a fraction of the local PCI bus bandwidth of 264 MB/s. Other key features of the SVME/DMV-183's VME interface include:

- Full system controller capability including the Dy4/Tundra Auto-ID option
- Programmable DMA controller with linked list support
- Wide range of VMEbus address and data transfer modes
- A32/A24/A16 master and slave (not A64 or A40)
- D64/D32/D16/D08 master and slave (no MD32)
- MBLT, BLT, ADOH, RMW, LOCK, and location monitors
- Four mailbox registers and four location monitors for inter-board communications and synchronization
- Nine programmable PCI-to-VME windows and eight programmable VME-to-PCI windows
- Extensive support for BIT

The SVME/DMV-183 also provides support for five geographical addressing bits as defined by the ANSI/VITA 1.1-1997 (VME64 extensions) specification.

PMC Sites

The functionality of the SVME/DMV-183 SBC can be substantially expanded via its two PCI Mezzanine Card (PMC) sites. The two PMC sites interface to other system elements via 64-pins of back panel I/O per site. The placement of the PMC sites is such that a single, double width PMC module can also be fitted.

PMC site 1 (closer to top of card) is served by its own dedicated 64-bit, 100 MHz-capable PCI-X bus providing a peak bandwidth to memory of 800 MB/s. High-performance PMC modules such as networking modules or graphics modules can operate at 100 MHz independent of the speed at which the PMC module in PMC site 2 operates. PMC site 2 (closer to bottom of card) is served by a 64-bit, 66 MHz PCI-X bus providing a peak bandwidth to memory of 533 MB/s.

I/O routing is done in accordance with ANSI/VITA 35-2000 specification, such that PMC site 1's I/O is routed to the P0 connector, while that of PMC site #2 is routed to A and C rows of the P2 connector. Front panel I/O is supported as a standard feature on air-cooled cards and, on a special order basis, for conduction-cooled cards.

The SVME/DMV-183 conforms fully to the IEEE 1386/1386.1 requirement for a component keep-out area at the front of the PMC site for connectors or high components.

Each PMC site uses 3.3 V signaling, is 5 V tolerant, and is keyed as a universal PMC site (no keys are installed). The Vio voltage to each PMC is selectable via push-on jumpers.

Routing for High-speed PMC I/O Signals

The SVME/DMV-183's routing for PMC I/O signals to the rear-panel connectors is carefully implemented to support high-bandwidth signals. PMC site #1, which routes to the P0 connector in accordance with ANSI/VITA 35-2000, has the following routing provisions:

- 27 differential pairs with a nominal impedance of 50 ohms
- Pair-to-pair skew is controlled within various pair groupings as required to support multiple TMDS and LVDS digital video channels as implemented on Curtiss-Wright's PMC-70x graphics modules
- Select pairs constrain in-pair skew to 0.012" (nominal) to support two Fibre Channel interfaces as implemented on Curtiss-Wright's PMC-643 Fibre Channel module

PMC site #2, which routes to the A & C rows of P2, has the following routing provisions:

- All 64 signals are routed as differential pairs with a nominal impedance of 50 ohms capable of supporting four full Star-Fabric links as implemented on Curtiss-Wright's StarLink PMC module
- Pair-to-pair skew is controlled within various pair groupings as required to support multiple TMDS and LVDS digital video channels as implemented on Curtiss-Wright's PMC-70x graphics modules
- Select pairs constrain in-pair skew to 0.012" (nominal) to support two Fibre Channel interfaces as implemented on Curtiss-Wright's PMC-643 Fibre Channel module

Contact your Curtiss-Wright representative for further information on the routing provisions for high-speed PMC I/O.

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PMC Power Routing

The PMC sites are provided with 3.3 V, +12 V, and -12 V power from the VMEbus backplane. No 3.3 V power is provided to the PMC sites by the regulators on the SVME/DMV-183 basecard itself.

Support for Processor PMCs

The SVME/DMV-183 is capable of hosting Processor PMCs in non-Monarch mode as described in the VITA 32-2003 draft standard (the Monarch# signal is left floating). The SVME/DMV-183 does not support the optional second PCI agent, the optional EREADY signal, or the optional RESETOUT# signal.

Conduction-cooled PMC Modules

To support the industry drive to open standards on conduction-cooled cards, the PMC site mechanical interfaces follow the VITA 20- 2001 (R2005) conduction-cooled PCI Mezzanine card standard. To optimize the thermal transfer from PMC modules to the basecard the standard SVME/DMV-183 thermal frame incorporates both the primary and secondary thermal interfaces as defined by VITA 20-2001.

The combination of the secondary thermal interfaces, the mid-plane thermal shunt, and Curtiss-Wright's TherMax™ thermal frame design provides optimum cooling for conduction-cooled PMC modules, allowing for higher power PMCs and/or increased long-term reliability through lower component temperatures.

Status Indicators and Controls

The SVME/DMV-183 SBC provides run/fail status by asserting a backplane signal and illuminating a red front panel LED in the event the diagnostics detect a card failure. There is also a software controlled green LED that the application can use to indicate status.

A card reset signal is available on the backplane connectors and on the front panel connector on air-cooled cards. The front panel and P0 break-out cables for the SVME/DMV-183 include a push button switch that interfaces to this signal to allow the card to be reset without doing a full system reset.

COP, JTAG Test and Debug Interfaces

For software debug purposes the Control and Observation Port (COP) of the MPC7447A/7448 processors are accessible via a permanently installed test connector. The test connector is accessible on all build grades of the SVME/DMV-183 including conduction-cooled. A wire link option allows one processor or the other to be accessed via the COP interface. An interface cable is available to provide a standard 2x8 .1" pitch header for JTAG emulators.

To support acceptance testing the SVME/DMV-183 provides a JTAG scan chain accessible on a permanently-installed test connector. The JTAG test chain coverage includes the processors, Discovery III system controller, VMEbus interface chip, Core Functions FPGA, and PCI-to-PCI bridge. PMC modules are automatically added to the JTAG chain when present.

Temperature Sensors

The SVME/DMV-183 provides four Maxim 6634 temperature sensors located at the approximate corners of the board. Software can read the temperature sensors at any time through their I2C interface connected via the Discovery III system controller, or receive an independent interrupt for each sensor when a software programmable over- or under-temperature condition occurs. The temperature sensors are accurate to +/-2.5 °C from -40 °C to +125 °C.

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I/O Options

See Table 3 for a definition of the various I/O modes available for the SVME/DMV-183.

Table 3: SVME/DMV-183 I/O Options

Mode	Front Panel (air-cooled only)	P0 Connector	P2 Connector
#0	Upper 9-pin connector: ◆ Serial 1, RS-232 ◆ Serial 2, RS-232 ◆ Card reset input Lower 9-pin connector: ◆ ENETFP ◆ USB 1	◆ PMC Site #1 I/O ◆ ENETP0 (GbE) ◆ USB 2 ◆ Carfail status out ◆ Card reset input ◆ ALT_BOOT input ◆ (No TTL discrete I/O)	◆ PMC Site #2 I/O (rows A & C) ◆ ENETP2 (10/100) ◆ Serial 1, RS-232 ◆ Serial 2, RS-232
#1	Same	◆ PMC Site #1 I/O ◆ ENETP0 (GbE) ◆ 14 TTL discrete I/O ◆ USB 2 ◆ Carfail status out ◆ Card reset input ◆ ALT_BOOT input	◆ PMC Site #2 I/O (rows A & C) ◆ ENETP2 (10/100) ◆ 8-bit SCSI ◆ Serial 1, RS-232 ◆ Serial 2, RS-232 ◆ Serial 3, RS-232/422/485 ◆ Serial 4, RS-232/422/485
#4	Same	Same as Mode #1	◆ PMC Site #2 I/O (rows A & C) ◆ ENETP2 (10/100) ◆ 16-bit SCSI ◆ Serial 1, RS-232 ◆ Serial 2, RS-232 ◆ Serial 3, RS-232/422/485
#6	Same	Same as Mode #1	◆ PMC Site #2 I/O (rows A & C) ◆ ENETP2 (10/100) ◆ Serial 1, RS-232 ◆ Serial 2, RS-232 ◆ Serial 3, RS-232/422/485 ◆ Serial 4, RS-232/422/485 ◆ Serial 5, RS-232/422/485 ◆ Serial 6, RS-232/422/485
#8	Same	Same as Mode #1	◆ Same as Mode #9 but only MIL-STD-1553 #1
#9	Same	Same as Mode #1	◆ PMC Site #2 I/O (rows A & C) ◆ ENETP2 (GbE) ◆ Serial 1, RS-232 ◆ Serial 2, RS-232 ◆ Serial 3, RS-232/422/485 ◆ Serial 4, RS-232/422/485 ◆ MIL-STD-1553 #1 ◆ MIL-STD-1553 #2
#10	Same	Same as Mode #1	◆ Same as Mode #9 but only no MIL-STD-1553
#11	Same	Same as Mode #1	◆ PMC Aite #2 I/O (rows A & C) ◆ ENETP2 (GbE) ◆ Serial 1, RS-232 ◆ Serial 2, RS-232 ◆ Serial 3, RS-232/422/485 ◆ Serial 4, RS-232/422/485 ◆ MIL-STD-1553 #1 ◆ SATA #1 ◆ SATA #2
#12	Same	Same as Mode #1	◆ Same as Mode #11 but without MIL-STD-1553

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Software Support

Foundation Firmware and BIT

The SVME/DMV-183 SBC is equipped with a comprehensive on-board firmware package called Foundation Firmware that includes:

- General Purpose Monitor (GPM) - provides monitoring, diagnostic, and board exerciser functions to facilitate system startup and integration activities
- Built-in-Test (BIT) - a library of Card Level Diagnostic (CLD) routines is provided to support Power-up BIT (PBIT), Initiated BIT (IBIT) and Continuous BIT (CBIT)
- Non-Volatile Memory Programmer (NVMP) - provides for in-circuit and closed chassis reprogramming of flash memory over serial port or Ethernet (see Non-Volatile Memory Programmer data sheet for more information)
- Warm boot/cold boot determination
- Declassification function to erase all non-volatile memories Curtiss-Wright's BIT firmware is designed to provide 95% fault coverage for testable functionality and supports tests in Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) modes. PBIT consists of a reduced set of tests that provide confidence that the hardware is operating correctly while minimizing power-up time.

The IBIT capability allows users to initiate testing with a more comprehensive suite of tests to provide more robust testing in an offline mode. CBIT allows applications to test hardware components in the background while the mission software operates as a higher priority task. The selection of tests for PBIT, IBIT, and CBIT is user configurable.

Operating System Software

The SVME/DMV-183 is supported by the following real-time operating systems:

- VxWorks (Tornado) from Wind River Systems (see separate VxWorks BSP and Driver Suite datasheet for details)
- INTEGRITY from Green Hills Software (see separate datasheet for details)
- Linux 2.6 BSP from Curtiss-Wright (see separate datasheet for details)
- LynxOS BSP

Contact your Curtiss-Wright representative for updates on support for other operating systems.

Continuum Vector Library

Curtiss-Wright's Continuum Vector DSP library allows customers to fully exploit the performance potential of the SVME/DMV-183's AltiVec-equipped 74xx processors. Continuum Vector provides a comprehensive set of AltiVec optimized C-callable functions written primarily in assembly language, yielding a significant performance advantage over equivalent functions written only in a high-level language. This object-format library integrates easily with standard software development tools and supports real and complex array, vector, and scalar signal processing functions.

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Cable Set

See Table 4, SVME/DMV-183 cable set for details on the various I/O cables available with the SVME/DMV-183.

Table 4: SVME/DMV-183 Cable Set

Cable Number	Connects To	Description
CBL-182-FPL-000	Front panel in all pin-out modes	Two-part front panel cable set for SVME-182/183. One cable provides two 9-pin D connectors for RS-232 ports and a push-button switch for card reset; second cable provides standard RJ-45 10/100Base-T Ethernet jack and one USB type A receptacle.
CBL-182-P0-000	P0 in all pin-out modes	P0 break-out cable for 182/183 in all pin-out modes. Provides RJ-45 Jack for 10/100/1000Base-T Ethernet interface, 25-pin female D connector for TTL discretes, USB type A receptable for USB port 2, and PMC I/O on 78-way connector. Also includes reset switch.
CBL-183-P2-000	P2 in pin-out Mode #0 (no IPM)	P2 break-out cable for 182/183 in pin-out Mode 0. Provides separate branches and connectors for two 9-pin D connectors for RS-232 ports, RJ45 jack for Ethernet, and 18x-standard 78-way connector for PMC I/O.
CBL-SBC-P2-000	P2 in pin-out Mode #1	P2 break-out cable for 179/181/182/183 in pin-out Mode 1 with separate branches and connectors for 8-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 ports 3 and 4, and PMC I/O on 78-way connector. (Note - no Ethernet branch.)
CBL-SBC-P2-002	P2 in pin-out Mode #4	P2 break-out cable for 179/181/182/183 in pin-out mode 4 with separate branches and connectors for 16-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 port 3, and PMC I/O on 78-way connector. (Note - no Ethernet branch.)
CBL-183-P2-006	P2 in pin-out Mode #6	P2 breakout connector for 181/182/183 in pin-out mode 6. Provides two 9-pin D connectors for RS-232 ports, four 25-pin D connectors for RS-422/485 ports, RJ45 jack for Ethernet, and 18x-standard 78-way connector for PMC I/O.
CBL-183-P2-009	P2 in pin-out Mode #8 and #9	P2 break-out for 182/183 in Mode 8 (single MIL-STD-1553) and Mode 9 (dual MIL-STD-1553). Provides separate branches and connectors for the transformer-coupled MIL-STD-1553 signals, MIL-STD-1553 configuration inputs, two RS-232 ports, two RS-232/422/485 ports, RJ-45 jack for Ethernet, and PMC I/O on 18x-standard 78-way connector. Connectors for MIL-STD-1553 signals are 3-lug Twinax bulkhead jack connectors, Trompeter part number BJ79-47.
CBL-182-P2-010	P2 in pin-out Mode #10	P2 break-out for 182/183 in Mode 10. Provides separate branches and connectors for two RS-232 ports, two RS-232/422/485 ports, GbE, and PMC I/O on 78-way connector.
CBL-183-P2-011	P2 in pin-out Mode #11	P2 break-out cable for 183 in Mode 11. Provides separate branches and connectors for one MIL-STD-1553 channel, MIL-STD-1553 configuration inputs, two RS-232 ports, two RS-232/422/485 ports, GbE, 2 SATA ports, and PMC I/O on 78-way connector. Connectors for 'MIL-STD-1553 signals are 3-lug Twinax bulkhead jack connectors, Trompeter part number BJ79-47.
CBL-183-P2-012	P2 in pin-out Mode #12	P2 break-out cable for 183 in Mode 12. Provides separate branches and connectors for two RS-232 ports, two RS-232/422/485 ports, GbE, 2 SATA ports, and PMC I/O on 78-way connector.
CBL-183-P2-236	P2 in pin-out Mode #6 and with StarLink PMC	P2 breakout cable for 182/183 in pin-out Mode 6 with PMC-230/233 StarLink module. Separate branches and connectors for 2 EIA-232 ports, 4 EIA-422/485 ports, one 10/100MB/s Ethernet branch terminating in an RJ-45 bulkhead-mount plug, and 8 branches with StarFabric connections (4 x Tx, 4 x Rx) terminating in RJ-45 bulkhead-mount plugs. All branches a minimum length of 18".
CBL-183-P2-2310	P2 in pin-out Mode #10 and with StarLink PMC	P2 breakout cable for 182/183 in pin-out Mode 10 with PMC-230/233 StarLink module. Separate branches and connectors for 2 EIA-232 ports, 2 EIA-422/485 ports, 1GbE branch terminating in an RJ-45 bulkhead-mount jacks, and 8 branches with StarFabric connections (4 x Tx, 4 x Rx) terminating in RJ-45 bulkhead-mount jacks. All branches a minimum length of 18".
CBL-183-JTAG	183 test connector	Connects to 183 test connector and provides standard 2x8.1î pitch header for JTAG/COP emulators

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Product Documentation

Documentation Delivery on DVD-ROM

A standard DVD-ROM (DPK-TechDoc-DVD) is included with every SVME/DMV-183. Providing many ease of use features, the DVD-ROM serves as a complete Technical Documentation library for the SVME/DMV-183. Along with the user documentation, a complete library of Product Release Notes is also included.

Pinout Configurator Utilities

The pin-out configurator is a Microsoft® Windows® application that allows users to generate accurate backplane connector pinout tables based upon the customer's specific SVME/DMV-183 configuration. Using a visual point and click interface, users select which PMC module is installed in the PMC site on their basecard, then click a button to generate the precise pinout information, which can then be viewed on-screen, printed, or exported into a common application such as MS-Word.

Convenient Web Links

The interface of the DVD-ROM provides convenient point-and-click access to additional corporate information, contacts and resources, such as Technet, Sales and Support contacts. (Please consult the Technet web site (http://technet.cwcembedded.com) periodically to view or download new or updated releases of user documentation that may become available between DVD-ROM releases.)

Power Inputs and Power Consumption

The SVME/DMV-183 basecard uses only +5 V and optionally +5 V STDBY for the real-time clock. Onboard regulators provide all necessary internal voltages. Backplane +5 V, ±12 V, and 3.3 V is routed to the PMC sites.

Power Consumption

See Table 5 for power consumption figures for the SVME/DMV-183 basecard. Power consumption increases as operating temperature rises. Table 5 figures are for the highest rated operating temperature while executing a test application generating CPU processing loads and data traffic representative of a typical customer application. See Table 6 for power consumption figures for the Interface Personality Modules available with the SVME/DMV-183.

Table 5: SVME/DMV-183 Power Consumption

Ruggedization Level	Reference Configuration	Typical Power (W)
L0	SVME-183-0000 (1x MPMC7447A @ 1.0 GHz)	21.5
Level 100 Air-cooled	SVME-183-1000	24
Level 100 Conduction-cooled	DMV-183-1000	23
Level 200 Conduction-cooled	DMV-183-2000	24
L0	SVME-183-0100 (1x MPMC7448 @ 1.2 GHz)	25
Level 100 Air-cooled	SVME-183-1100	27.5
Level 100 Conduction-cooled	DMV-183-1100	26.5
Level 200 Conduction-cooled	DMV-183-2100	27.5
L0	SVME-183-0600 (2x MPMC7447A @ 1.0 GHz)	31
Level 100 Air-cooled	SVME-183-1600	33.5
Level 100 Conduction-cooled	DMV-183-1600	32.5
Level 200 Conduction-cooled	DMV-183-2600	33.5
L0	SVME-183-0700 (2x MPMC7448 @ 1.2 GHz)	38
Level 100 Air-cooled	SVME-183-1700	40.5
Level 100 Conduction-cooled	DMV-183-1700	39.5
Level 200 Conduction-cooled	DMV-183-2700	40.5

Notes
1. Typical power is measured power while running stress test software that exercises CPU and board functions including AltiVec. The actual power consumption observed will vary by application.
2. For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption figures. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption figures.

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Table 6: SVME/DMV-183 Interface Personality Module Power Consumption

Ruggedization Level	Reference Configuration	Typical Power (W)
All	Mode 1 IPM	2
All	Mode 4 IPM	2
All	Mode 6 IPM	2
All	Mode 8 IPM	3
All	Mode 9 IPM with both MIL-STD-1553 channels at 50% Tx time	5
All	Mode 9 IPM with both MIL-STD-1553 channels at 25% Tx time	3
All	Mode 10 IPM	1
All	Mode 11 IPM with MIL-STD-1553 channel at 50% Tx Time	4
All	Mode 11 IPM with MIL-STD-1553 channel at 25% Tx Time	3
All	Mode 12 IPM	2

Note: For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption figures. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption figures.

Mechanical Format

Conduction-cooled modules conform to the dimensions defined in IEEE 1101.2-1992, Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards (see page 7 for more details on frame limitations).

Air-cooled modules conform to the dimensions defined in ANSI/VITA 1-1994, American National Standard for VME64. Front panel hardware on air-cooled modules includes: injector/ extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 11 01.10).

For air-cooled applications where the enclosure is not compatible with the IEEE 11 01.10-style front panels, original-style non-injector equipped front panel kits can be purchased separately and fitted to the card by the customer.

Table 7: SVME/DMV-183 Specifications

Power Requirements	Maximum	Typical (Amps)
+5 V (+5.0%, -2.5%)	See Tables 5 and 6	See Tables 5 and 6
+12 V	0 A	Not used by the basecard, only routed to the PMC sites.
-12 V	0 A	Not used by the basecard, only routed to the PMC sites.
3.3 V	0 A	Not used by the basecard, only routed to the PMC sites.
+5 V STDBY with 5 V present	5 uA max	3 uA typical
+5 V STDBY without 5 V present	5 uA max	3 uA typical

Table 8: SVME/DMV-183 Dimensions & Weight

Dimensions & Weight	Dimensions	Weight (grams)
SVME card	per ANSI/VITA 1-1994	<500 (<1.21 lbs.)
DMV card	per IEEE 1101.2**	<800 (<1.77 lbs)
IPM	-	39 (max)

** Except for the card-edge profile as shown in Figure 8

Ruggedization Levels

SVME card

Available in Levels 0, 100
(Required airflow is 10 cfm at sea level)

DMV card

Available in Levels 100 and 200

- Standard conformal coating is acrylic
- PWB meets UL 94 V-0 flammability rating
- Circuit card assembly is done to class 3 standards of IPC-A-610C, Acceptability of Electronic Assemblies

Unless otherwise noted environmental tolerance is as defined in Curtiss-Wright's Ruggedization Guidelines factsheet.

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Part Numbers

Check with a Curtiss-Wright representative for availability of specific part numbers.

Table 9: SVME/DMV-183 Standard Part Numbers

SVME/DMV - 183- xyzz

- Pin-out mode (see Table 3)
- Processing core:
  - 0: Single MPC7447A @ 1.0 GHz, 512 MB SDRAM, 128 MB Flash
  - 1: Single MPC7448 @ 1.2 GHz, 512 MB SDRAM, 128 MB Flash
  - 3: Single MPC7448 @ 1.2 GHz, 1 GB SDRAM, 256 MB Flash
  - 6: Dual MPC7447A @ 1.0 GHz, 1 GB SDRAM, 256 MB Flash
  - 7: Dual MPC7448 @ 1.2 GHz, 1 GB SDRAM, 256 MB Flash
  - 8: Custom configuration
  - 9: Dual MPC7448 @ 1.2 GHz, 2 GB SDRAM, 512 MB Flash
- Ruggedization level:
  - 0: 0 to +50°C
  - 1: -40 to +71°C
  - 2: -40 to +85°C
  - 4: Custom environment
- Model number:
  - 183
- Cooling method:
  - SVME - Air-cooling
  - DMV - Conduction-cooling

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support

Email: support1@cwcembedded.com

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