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D50 PLC
User's Manual

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Preface

Welcome to Cutler-Hammer’s D50 PLC User's Manual. This preface describes the contents of this manual and provides information on Support Services.

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About This Manual

Purpose

This manual focuses on describing the D50 Programmable Logic Controller (PLC).

What's Inside

This manual is organized in the following way:

Preface
Chapter 1: Introduction
Chapter 2: System Configuration
Chapter 3: Product Specification
Chapter 4: Installation and Wiring
Chapter 5: CPU Operation and Memory
Chapter 6: Instructions
Chapter 7: Testing and Troubleshooting
Chapter 8: Troubleshooting Noise Problems
Appendix A: D50 PLC Communication Protocol
Appendix B: Special I/O Functions
Appendix C: D50PGM10 Pocket Editor



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2. Expedite an existing order.
3. Product assistance and product price information.
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Table of Contents

Preface **I**

About This Manual ii
Purpose ii
What's Inside ii
Support Services iii

Table of Contents **v**

Chapter 1: Introduction **1**

Overview of the Manual 2
Features of the D320 PLC 2
Self Diagnostics 3
Large Program Memory 3
Integrated 700mA Power Supply 3
Battery-Free Program Backup 3
I/O Module Support 3
Peripheral Support 4
System Installation Considerations 4
Environmental Considerations 4
Preventing PLC System Malfunctions 4

Chapter 2: System Configuration **5**

D50 PLC System Components 6
D50 PLC Product List 7
D50 PLC Expansion Configurations 9

Chapter 3: Product Specification **11**

Environmental Operating Ranges 12
CPU Performance Specifications 12
Electrical Specifications 13
Power Supply Specifications 13
24VDC Input Specifications 14
115VAC Input Specifications 15
Relay Output Specifications 16
Transistor (24VDC) Output Specifications 17
SSR (115VAC) Output Specifications 18
Name and Function of Controller Components 19

Chapter 4: Installation And Wiring **21**

System Design Considerations 22
Power Supply Wiring 22
Interlock Circuit and Emergency Stop Circuit (Safety measures in system design) 22
Momentary Power Failure and Voltage Drop 23
System Installation Guidelines 23
Environmental Usage Conditions 23
Control Panel Installation 24
System Wiring and Installation Procedures 26
Installation Dimensions 26

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DIN Rail Mounting 26
Unit Installation Height 27
Expansion Cable Connection 27
Power Supply Wiring 28
Power wiring 28
Grounding 28

Chapter 5: CPU Operation And Memory **29**

Terminology 30
Overview of CPU Operation Mode 31
What Is the CPU Operation Mode? 31
Run Mode (operating) 31
Stop Mode 31
Error Mode 31
CPU Processing Procedure 32
Program Processing Procedure 32
Introduction to Registers 33
Internal/External Address Designation 33
Expression Example 35
Double Mode Address Designation 36
Absolute Address Designation 37
I/O Address Designation 38
Digital I/O Address Designation 38
Analog I/O Address Designation 38
Special Internal Addresses 39
Timer/Counter (TC0-255) 44

Chapter 6: Instructions **47**

Basic Instructions 48
Timer/Counter Instructions 49
Comparison Instructions 50
Substitution, Increment/Decrement Instructions 50
Arithmetic Instructions 51
Logic Instructions 52
Rotation Instructions 52
Word Conversion Instructions 53
Bit Conversion Instructions 54
Transfer Instructions 55
Block Processing Instructions 56
How to Read the Description of Instructions 57
Instruction 57
Ladder 57
Description 58
Example 59
Basic Instruction Details 59
STR, STN 59
AND, ANN, (ADN) 60
OR, ORN 61
OUT, SET, RST 62
NOT 63
STR DIF, STR DFN, AND DIF, AND DFN, OR DIF, OR DFN 64
ANB, ORB 65
MCS, MCR 66

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Timer/Counter Instruction Details 67
TIM, SST 67
UC, DC 69
UDC 71
Comparison Instruction Details 73
=, <>, >, >=, <=, < 73
Substitution, Increment, Decrement Instruction Details 74
LET, DLET 74
INC, DINC, INCB, DINCB 75
DEC, DDEC, DECB, DDECB 76
Arithmetic Instruction Details 77
ADD, DADD, ADDB, DADDB 77
SUB, DSUB, SUBB, DSUBB 79
MUL, DMUL, MULB, DMULB 80
DIV, DDIV, DIVB, DDIVB 81
ADC, DADC, ADCB, DADCB 82
SBC, DSBC, SBCB, DSBCB 84
ABS, DABS, NEG, DNEG, NOT, DNOT 86
Logic Instruction Details 87
AND, DAND 87
OR, DOR 88
XOR, DXOR 89
XNR, DXNR 90
Rotation Instruction Details 91
RLC, DRLC 91
RRC, DRRC 92
ROL, DROL 93
ROR, DROR 95
SHL, DSHL 96
SHR, DSHR 98
Word Conversion Instruction Details 99
BCD, DBCD, BIN, DBIN 99
XCHG, DXCHG 100
SEG 101
ENCO, DECO 102
DIS, UNI 104
Bit Conversion Instruction Details 106
BSET, BRST, BNOT, BTST 106
SUM 108
SC, RC, CC 109
Transfer Instruction Details 110
LDR, DLDR 110
STO, DSTO 112
MOV, FMOV 114
BMOV, BFMV 116
Block Processing Instruction Details 117
FOR, DFOR, NEXT 117
JMP, LBL 119
JMPS, JMPE 120
CALL, SBR, RET 122
WAT 124
END 125

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Chapter 7: Testing And Troubleshooting **127**

Test Precautions ... 128
System Checks ... 128
Testing Procedures ... 130
Correcting Errors ... 132
System Check ... 132
Power Supply Check ... 133
Run Check ... 134
Error Check ... 135
I/O Check ... 136
Troubleshooting, Maintenance and Inspection Tables ... 138
Periodic Inspection and Preventive Maintenance ... 141

Chapter 8: Troubleshooting Noise Problems **143**

Noise Occurrence ... 144
Types of Noise ... 144
Electrical Noise Fundamental Definitions ... 144
Sources of Noise ... 145
Advised Installation Practices ... 146
Shield the PLC ... 146
Proper Cable Selection ... 146
Ground the PLC ... 146
Isolation and Filtering Techniques ... 147
Isolation ... 147
Filters ... 148
Methods of Handling Large Voltage Spikes Such as Lightning ... 149
Surge Absorber ... 149
Burying Wire ... 149
Shielding Cabling ... 150
Methods to Handle I/O Inductive Loads ... 151
Warning ... 153
Troubleshooting ... 154

Appendix A: D50 PLC Communication Protocol **155**

Communication Rules ... 156
Communication Environment ... 156
Communication Protocol ... 156
Step 1—Query (Q) ... 156
Step 2—Query Acknowledge (QA) ... 156
Step 3—Response Request (RR) ... 156
Step 4—Response (R) ... 156
Step 5—Repeated Response ... 157
Communications Delay ... 157
Example ... 157
CPU ID ... 158
Function Codes Included in the Query ... 158
Cyclic Redundancy Checking (CRC) ... 159
The Structure of the Communications Frame ... 160
Read Bits ... 161
Write Bits ... 162
Read Words ... 163
Write Words ... 164

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Read Bits and Words....165
Write Bits and Words....166
Communication Program Example....167

Appendix B: Special I/O Functions 173

Overview....174
High Speed Counter....174
Configurable Input Response Delay....174
Pulse Catch Input....174
Pulse Output....174
Special I/O Function Registers....175
High Speed Counter....176
Register Descriptions....176
Bit Registers....177
Programming Procedure....178
Configurable Input Response Delay....179
Pulse Catch Input....180
Pulse Output....181
Register Descriptions....181
Pulse Mode Programming Procedure....183
PWM Mode Programming Procedure....184

Appendix C: D50PGM10 Pocket Editor 185

Overview....186
Specifications....186
Part Descriptions....187
Instruction LED's....187
Status LED's....187
Register LED's....188
Address/Data LED Display....188
Instruction Keys....188
Function Keys....189
Operating Procedures....190
Clear Program....191
Add Instruction....192
Monitor Program....193
Edit Program....197
Error Checking....200
Monitor I/O....201
Run/Stop PLC....204
Instruction Codes....205
Basic Instructions....205
Advanced Instructions....206
Programming Examples....208
Example 1 – Basic Instructions....208
Example 2 – Timer Instructions....210
Example 3 – Counter Instructions....211
Example 4 – Comparison/Advanced Instructions....213

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Introduction

1

Welcome to the D50 PLC User's Manual. The D50 Programmable Logic Controller (PLC) is a small application industrial controller, designed to provide maximum flexibility at a minimum cost. This manual will give you a complete understanding of how to install and program the D50 PLC. It also includes complete product specifications, and a description of the various products that work with the D50 PLC.

This chapter contains:

- *An overview of this manual*
- *The features of the D50 PLC*
- *System installation considerations*

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Overview of the Manual

This manual contains the following information:

- Chapter 1 introduces the D50 PLC by describing its features and discussing installation considerations.
- Chapter 2 discusses various system configurations and products that can be used with the D50 PLC.
- Chapter 3 gives performance specifications and operating ranges of the CPU and the D50 series products.
- Chapter 4 describes installation and wiring guidelines and procedures including system design considerations, wiring the power supply, and connecting the PLC to a PC.
- Chapter 5 introduces many concepts you need to know to program the D50 PLC including terminology, how the registers are used, different types of address designations, and the CPU processing procedure.
- Chapter 6 presents detailed information on the Instruction Set that is used by the D50 PLC.
- Chapter 7 discusses testing and troubleshooting procedures.
- Chapter 8 describes electrical interference or noise and the ways you can reduce its influence.
- Appendix A gives rules and procedures for D50 PLC communication.
- Appendix B details the configuration and operation of the integrated special I/O functions of the D50 PLC, including High Speed counters, Pulse Output, and adjustable inputs.
- Appendix C describes mnemonic programming and the use of the D50 Pocket Editor.

Features of the D50 PLC

The D50 Programmable Logic Controller (PLC) is a versatile and dependable industrial controller, designed to handle a wide range of small control applications to improve productivity and reduce operating costs. This “micro” or “brick” PLC provides high-speed processing of user control programs, and comes with a complete line of expansion I/O modules, including digital and analog. These features combine to provide the right solution for a multitude of applications.

- The D50 PLC is designed for small-sized control applications that require from 1 to 56 control points, high-speed count or analog capability, and advanced functionality.
- The D50 PLC is built to simplify operation, maintenance, and repair with its modular design.
- I/O flexibility is achieved through the wide variety of available digital and analog modules, covering a broad range of voltage and current ratings.

The D50 PLC has many additional features that combine to make it the ideal choice for many control applications.

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Self Diagnostics

When placed in the Run mode, the D50 PLC performs startup self-diagnostics and error-checking on the processor, control program, and I/O system. Error status information is stored internally, providing for quick and easy troubleshooting of system and programming errors.

Large Program Memory

Sufficient program capacity is furnished for even the most demanding applications. Internal program memory handles up to 2048 separate control steps.

Integrated 700mA Power Supply

The AC-powered D50 PLC controller provides up to 700mA of 24VDC output power. This can eliminate the need for an additional power supply for standard 24VDC control power requirements.

Battery-Free Program Backup

An EEPROM is used to provide battery-free permanent program and data storage.

I/O Module Support

The D50 PLC I/O expansion module line includes complete coverage of all major standard I/O requirements. Digital inputs can be of 24 VDC or 115 VAC type, while digital outputs can be 24 VDC transistor, 115VAC SSR, or relay type. Analog support is available for voltage and current A/D and D/A.

Peripheral Support

The D50 PLC has two program loader software packages available for use on standard PCs: the DOS-based GPC5, and the Windows-based WinGPC. These packages provide advanced programming, monitoring, editing, and troubleshooting for the D50 PLC. A dedicated hand-held programmer is also available for harsh environments. Cutler-Hammer also offers a complete line of Operator Interface products and HMI software packages compatible with the D50 PLC.

Note: When this manual uses the term GPC, either GPC5 or WinGPC can be used.

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System Installation Considerations

Environmental Considerations

The D50 PLC system should **never** be installed under the following environmental conditions:

1. Ambient temperature outside the range of 0 to 55°C (32 to 131°F).
2. Direct sunlight.
3. Humidity outside the range of 20% to 90%.
4. Altitudes greater than 10,000 ft. (3,000 m).
5. Corrosive or dusty air.
6. High voltage, high magnetics, or high electromagnetic waves.
7. Locations subject to direct impact greater than 10G or vibrations greater than 1G @ 57-2000 Hz.

Preventing PLC System Malfunctions

1. Use an isolation transformer and line filter on the incoming power to the PLC when in the vicinity of equipment using or producing high current, high voltage, or large magnetic fields.
2. Separate the main PLC power line ground from all other power grounds. Always use triple-grounding.
3. Do not exceed the current and power rating of the external 24 VDC provided by the D50 power supply.
4. Avoid system faults due to programming errors by reading and fully understanding this system manual and the PLC instruction set.
5. Perform regular preventive maintenance on installed systems, checking devices and wiring for potential breakdowns and failures.

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System Configuration

2

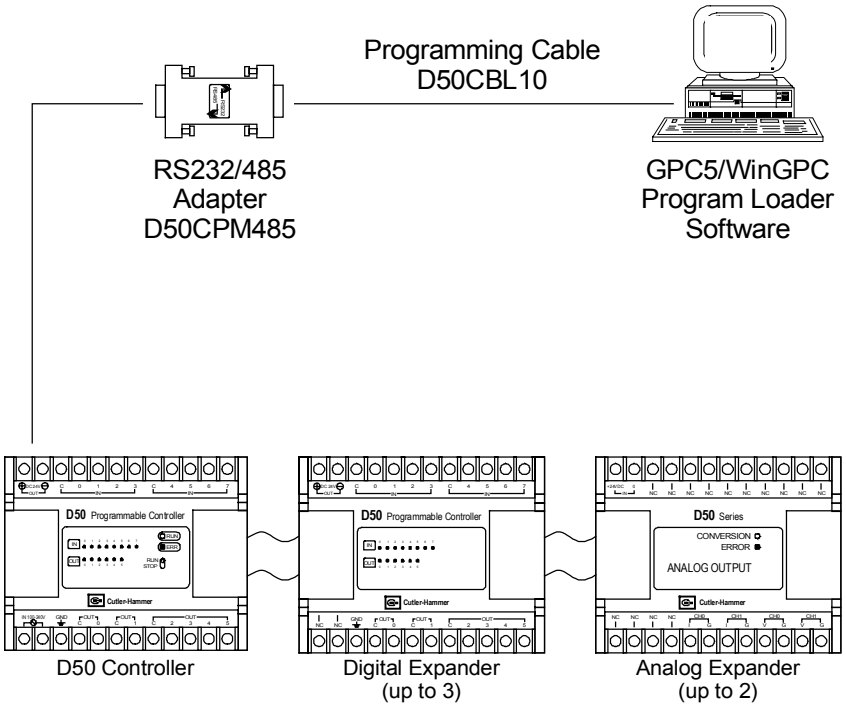
This chapter provides information on the various products that are available for the D50 PLC. It includes diagrams that show the D50 PLC system components and expansion configurations.

This chapter contains:

- *Information about the D50 PLC system components*
- *Descriptions of the line of D50 PLC products*
- *The D50 PLC expansion configurations*

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D50 PLC System Components



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D50 PLC Product List

Controllers

Name	Catalog #	Product Description	Remarks
Controller	D50CR14	115/230VAC Power, 24VDC Inputs, Relay Outputs	All controllers have 8 digital inputs and 6 digital outputs.
	D50CRA14	115/230VAC Power, 115VAC Inputs, Relay Outputs	
	D50CD14	115/230VAC Power, 24VDC Inputs, 24VDC Outputs	
	D50CAA14	115/230VAC Power, 115VAC Inputs, 115VAC Outputs	
	D50DCR14	24VDC Power, 24VDC Inputs, Relay Outputs	
	D50DCD14	24VDC Power, 24VDC Inputs, 24VDC Outputs	

Digital I/O Expansion

Name	Catalog #	Product Description	Remarks
Digital Expander	D50ER14	24VDC Inputs, Relay Outputs	All expanders have 8 digital inputs and 6 digital outputs.
	D50ERA14	115VAC Inputs, Relay Outputs	
	D50ED14	24VDC inputs, 24VDC Outputs	
	D50EAA14	115VAC inputs, 115VAC Outputs	

Analog I/O Expansion

Name	Catalog #	Product Description	Remarks
Analog Expander	D50AIM410V	0-10VDC, 0-5VDC, or 4-20mA Analog Inputs	4 Channels
	D50AOM210V	0-10VDC, 0-5VDC, or 4-20mA Analog Outputs	2 Channels

Analog/Frequency Converters

Name	Catalog #	Product Description	Remarks
A/F Converter	48160-450	Convert Analog 0-10VDC input signal to 0-10kHz Frequency input to D50 PLC	Maximum of 2 may be used per D50
F/A Converter	48160-480	Convert Pulse output from D50 PLC into a 0-10VDC or 4-20mA analog output signal	Maximum of 1 may be used per D50

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Programming Equipment

Name	Catalog #	Product Description	Remarks
Handheld Program Loader	D320PGM500	Write, edit, monitor program (mnemonic only) Memory BACK-UP function Backlit LCD screen Supports RS-232C/485 communication	Does not include cable Also supports the D300/D320 PLC's.

Name	Catalog #	Product Description	Remarks
Pocket Editor	D50PGM10	Write, edit, monitor program (mnemonic only) Supports RS485 communication	Includes cable

Name	Catalog #	Product Description	Remarks
GPC5 (DOS)	D50CCS35	Software for computer which provides programming, monitoring, uploading, downloading, online editing, error checking, PLC status monitoring, and other troubleshooting and diagnostic features.	For MS-DOS
WinGPC (Windows)	D50WINCS35		For Windows 3.1, 95, 98, NT

Note: When this manual uses the term GPC, either GPC5 or WinGPC can be used.

Programming Cables

Name	Catalog #	Product Description	Remarks
RS232C/485 Cable	D50CBL10	Handheld Program Loader (PGM500) For IBM-PC communication (GPC)	6 ft (2 m)

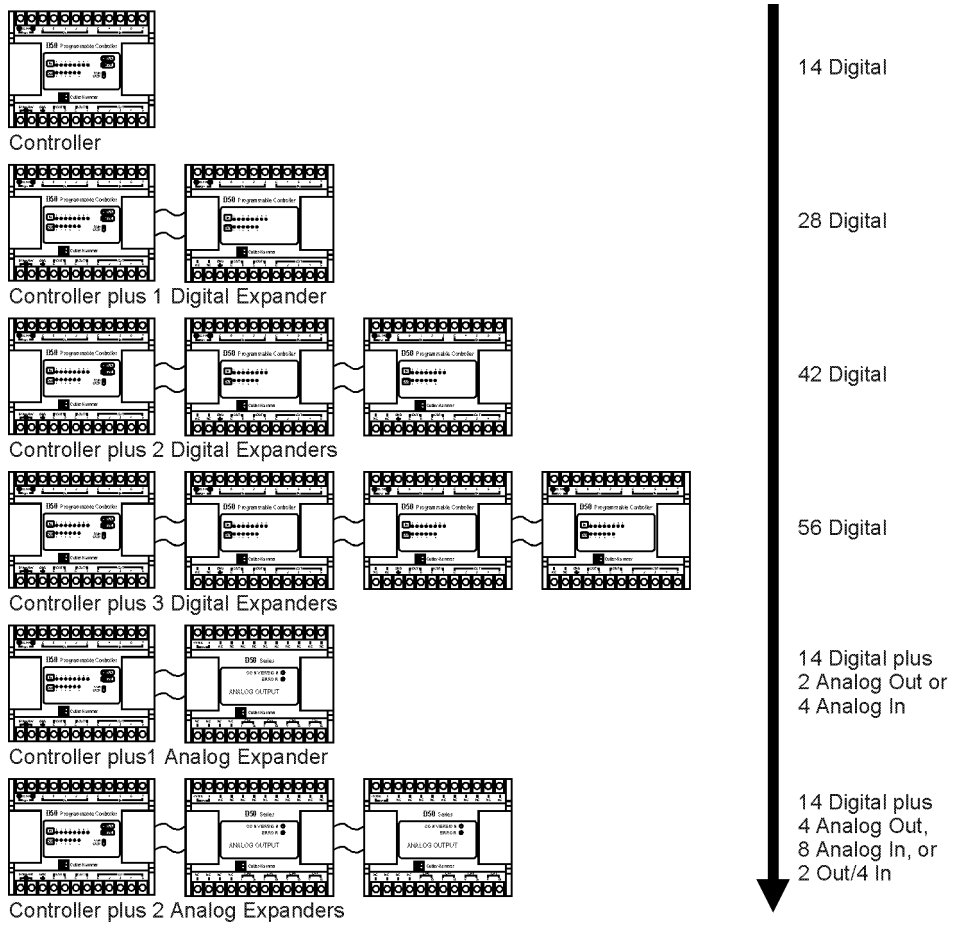
Manuals

Name	Catalog #	Product Description	Remarks
D50 Hardware Manual	D50SA122	Installation and programming manual for the D50 PLC.	Must be ordered separately
Analog Expander Manual	D50SA495	Configuration and operation manual for the D50AIM410V and D50AOM210V analog I/O.	Must be ordered separately
GPC5 Manual	D50SA464	Software Instruction manual for GPC5	
WinGPC Manual	D50SA467	Software Instruction manual for WinGPC	

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D50 PLC Expansion Configurations

- All digital I/O modules, both controller and expander, contain 14 I/O points – 8 digital inputs, and 6 digital outputs.
- Up to 3 digital expansion units can be added to the controller.
- Up to 2 analog expansion units can be added to the controller. These can be either two analog input modules, two analog output modules, or one of each.
- Any type of digital and analog expansion unit can be mixed and matched as required for the application.
- The digital and analog expansion units may be added in any order.
- A maximum of 56 digital points and 8 analog channels are available. This is achieved by using three digital expansion units, and two analog input expansion units.



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Product Specification

3

This chapter outlines the environmental conditions for D50 PLC operation and the performance specifications and component functions of the controller.

This chapter discusses:

- *The environmental operating ranges for the D50 Series products*
- *The performance specifications of the controller and expansion modules*
- *The name and function of the controller components*

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Environmental Operating Ranges

Item		Specifications
Ambient temperature	Operating temp.	0 to 55°C (32 to 131°F)
	Storage temp.	-10 to 75°C (14.0 to 167°F)
Ambient humidity	Operating	20% to 90% RH (Non-condensing)
	Storage	10% to 90% RH (Non-condensing)
Breakdown voltage		Between AC external terminal and earth, AC 1500 V for 1 min.
Insulation resistance		Min. 20Mohms, between AC external terminal and earth, 500 VDC.
Vibration resistance		16.7Hz, amplitude 3 mm, each direction of X, Y, Z for 2 hours.
Impact resistance		10G for 2 hours, X, Y, Z each direction.
Noise resistance		1500 Vp-p pulse width 50 ns, 1 μs (according to noise simulator method)
Usage condition		No corrosive gas or severe dust conditions.

Controller Performance Specifications

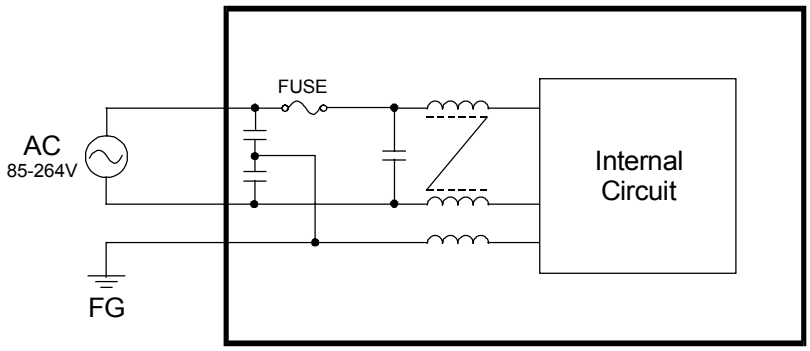
Control method		Program storage, Repeat calculation method
External I/O	Digital	Onboard 14 points; Max. 56 points
	Analog	Max. 8 Input Channels, or4 Output Channels, or 4 In/2 Out
Instruction	Basic instruction	25 types
	Application instruction	About 130 types
Process speed	Basic instruction	2 to 4 μS/step
Program capacity		2k steps (1 step = 1 word) (1k step = 1,024 steps)
Memory capacity	Local I/O (R)	R000.0 to R03.7 (32 Input); R015.0 to R18.5 (24 Output)
	Special I/O (R)	R004 to R14; R19 to R29
	Internal contact (M)	M000.0 to M31.15 (512 points, 32 words)
	Retentive internal contact (K)	K000.0 to K15.15 (256 points, 16 words)
	System flags (F)	F000.0 to F001.15 (32 points)
	Timer/Counter (TC or TIM)	256 channels (timer + counter), set point: 0 to 65,535 Timer: 0.01 second: TC000 to TC015 (16 channels) 0.1 second: TC016 to TC255 (240 channels) counter: TC000 to TC255 (256 channels)
	Data word (W)	W0000 to W255 (256 words)
	System registers (W, SR)	SR000 to SR255 (256 words)
Special functions	High-speed Counter	2 channel (24bit up/down; single phase 10kHz, dual-phase 5kHz)
	Pulse Output	1 point (20Hz to 5kHz); 24VDC Transistor output units only
	Input Delay	0 to 64msec adjustable
	Pulse Catch Input	150μsec minimum width
Comm. Port Interface		RS485 Multidrop at 9600bps

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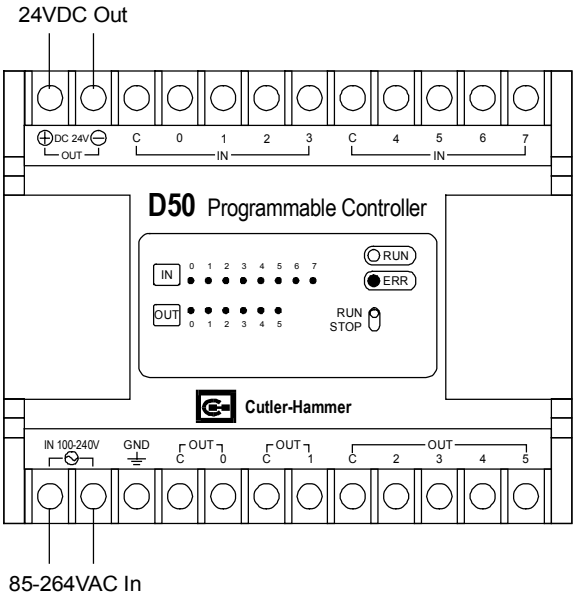
Electrical Specifications

Power Supply Specifications

Internal Circuit Diagram



Wiring Diagram



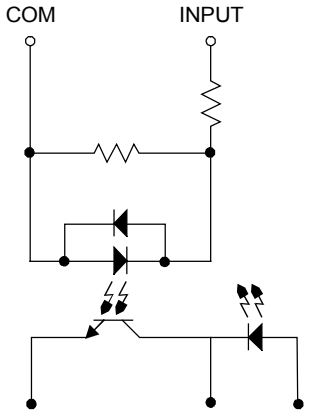
Specifications

Voltage Input	AC Models: 85-264VAC; DC Models: 20-28VDC
AC Frequency	47-63Hz
Current Consumption	Max. 0.6A
Output Power	24VDC @ 700mA max.

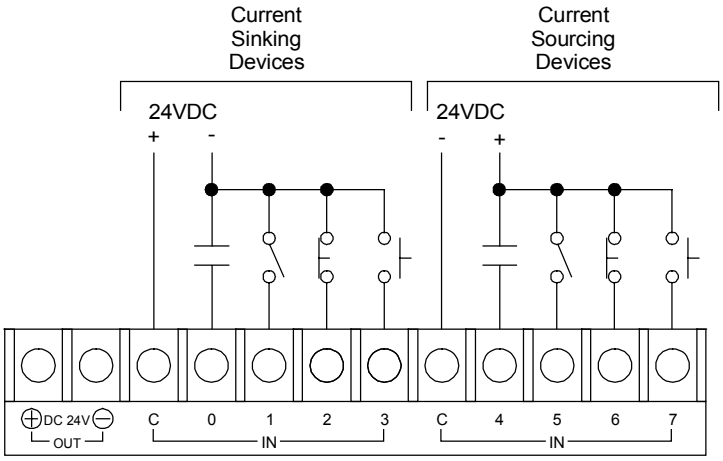
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24VDC Input Specifications

Internal Circuit Diagram



Wiring Diagram



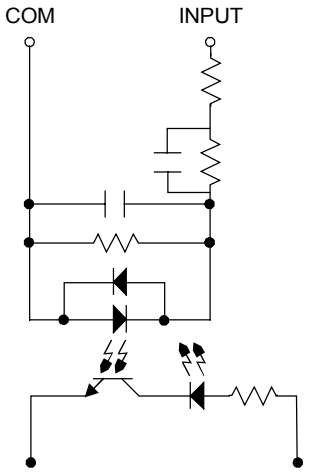
Specifications

Rated Voltage		12 to 24VDC
Operating Voltage Range		9 to 30VDC
Input Resistance		3.3 kΩ
Input Delay Time	Off → On	Less than 10ms
	On → Off	Less than 10ms
Number of Inputs		8 points
Points per Common		4 points/common
Isolation		Photocoupler

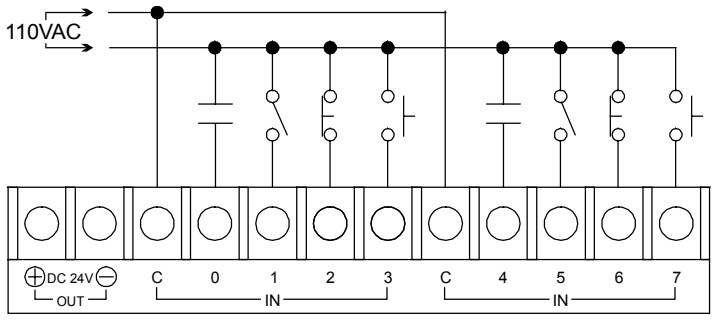
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115VAC Input Specifications

Internal Circuit Diagram



Wiring Diagram

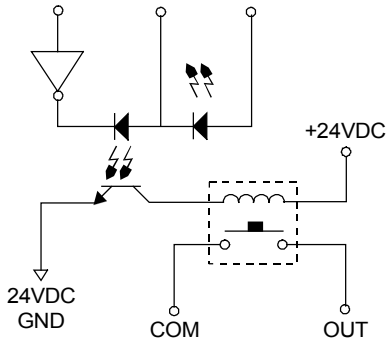


Specifications

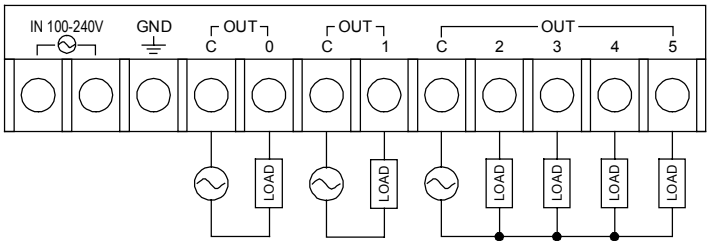
Rated Voltage		110VAC
Operating Voltage Range		85 to 132VAC
Input Current		5mA to 14mA
Operating Voltage	Min. On	85VAC
	Max. Off	30VAC
Input Delay Time	Off → On	Less than 12ms
	On → Off	Less than 12ms
Number of Inputs		8 points
Points per Common		4 points/common
Isolation		Photocoupler

Relay Output Specifications

Internal Circuit Diagram



Wiring Diagram



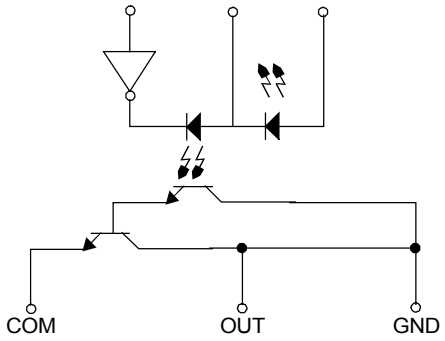
Specifications

Rated Voltage		110/220VAC; 30VDC
Operating Voltage Range		85 to 132VAC
Electrical Life		200,000 operations @ rated current
Mechanical Life		10M operations
Max. Load Current	Per Output	2A
	Per Common	4A
Min. Load Current	Per Output	30mA
Output Delay Time	Off → On	Less than 10ms
	On → Off	Less than 10ms
Number of Outputs		6 points
Points per Common		2 Isolated, 1 group of 4 points/common
Isolation		Photocoupler

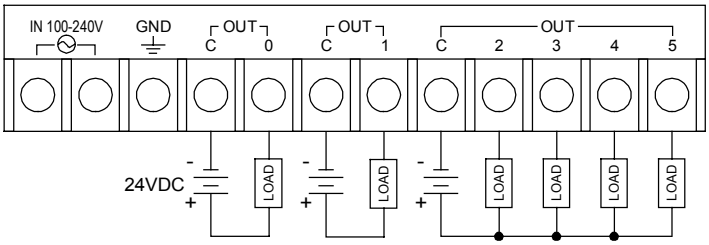
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Transistor (24VDC) Output Specifications

Internal Circuit Diagram



Wiring Diagram



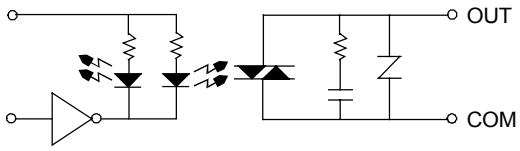
Specifications

Rated Voltage		24VDC
Operating Voltage Range		5 to 27VDC
Max. Load Current	Per Output	0.5A
	Per Common	4A
Min. Load Current	Per Output	10mA
Output Delay Time	Off → On	Less than 1ms
	On → Off	Less than 1ms
Number of Outputs		6 points
Points per Common		2 Isolated, 1 group of 4 points/common
Isolation		Photocoupler

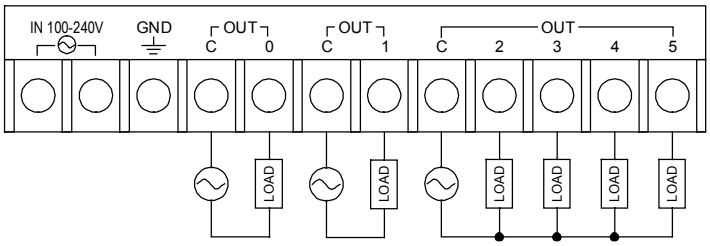
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SSR (115/230VAC) Output Specifications

Internal Circuit Diagram



Wiring Diagram

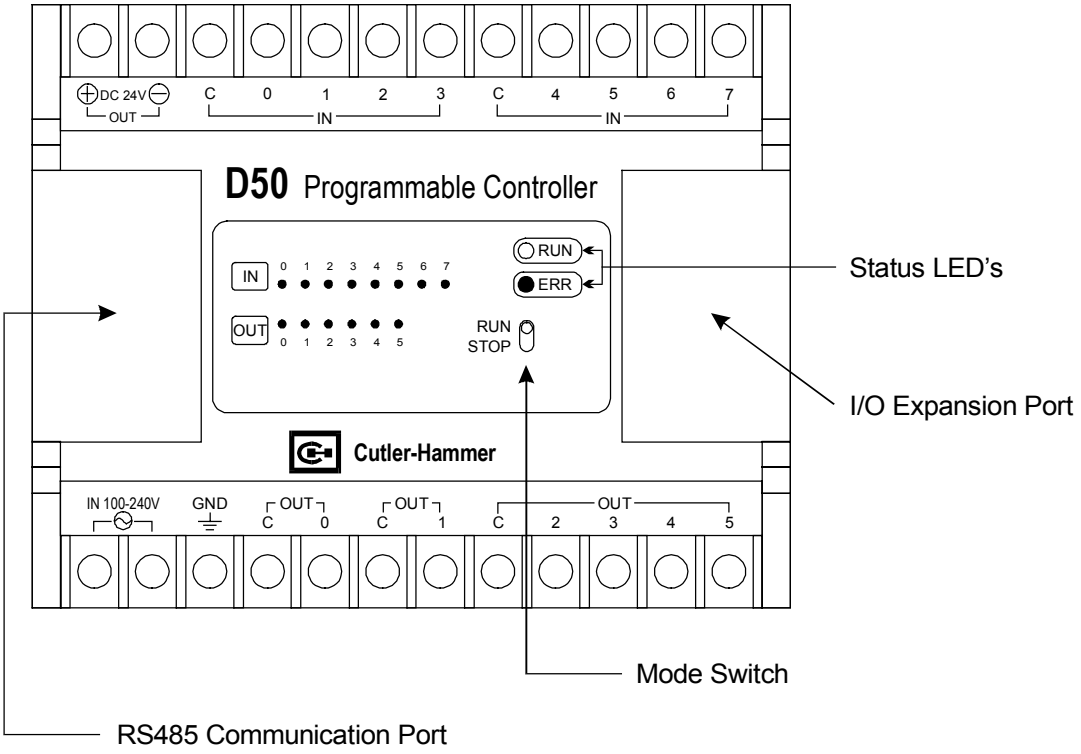


Specifications

Rated Voltage		110/220VAC
Operating Voltage Range		85 to 132VAC
Max. Load Current	Per Output	0.5A
	Per Common	3A
Min. Load Current	Per Output	50mA
Output Delay Time	Off → On	Less than 5ms
	On → Off	Less than 12ms
Number of Outputs		6 points
Points per Common		2 Isolated, 1 group of 4 points/common
Isolation		Photocoupler

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Name and Function of Controller Components



The mode switch has the following settings:

State	Function
RUN	CPU set in Run or Stop/Program Override mode.
PROG.	CPU set in Stop/Program mode.

The Status LED's provide the following information:

LED	Color	Function
RUN	Green	On when the CPU is in Run mode.
		Flashing when the CPU is in Stop/Program mode.
ERROR	Red	On when CPU has an error.

The I/O Expansion Port supplies a 10-pin connector for adding digital and/or analog expansion modules to the base controller.

The RS485 Communication Port supports an RS485 connection for programming, configuring, and monitoring the PLC. For communication with most RS232 peripherals, such as a personal computer, an RS232/485 converter must be used. When placed on an RS485 network with other D50, D300, or D320 PLC's, the ends of the network should be properly terminated with 120 Ohm resistors to prevent communication errors due to noise and reflections on the transmission line.

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Installation and Wiring

4

This chapter provides considerations and information on installing and wiring the D50 PLC. Diagrams are included to illustrate the installation procedures.

This chapter contains:

- *System design considerations*
- *System installation guidelines*
- *System wiring and installation procedures*

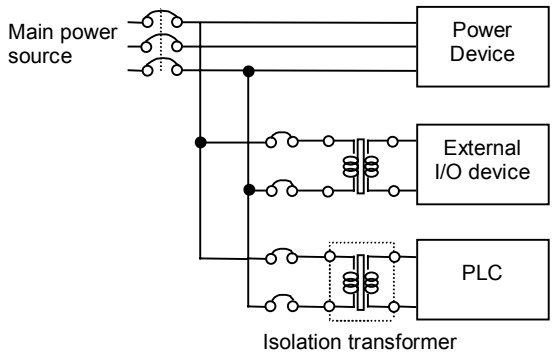
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System Design Considerations

Power Supply Wiring

Physical and Electrical Isolation of Power Supplies

When wiring the PLC, external control I/O, and large power equipment such as motors, each system should be electrically separated as shown:



Interlock Circuit and Emergency Stop Circuit (Safety measures in system design)

In any PLC application, abnormal and potentially dangerous operation can occur. These system malfunctions may result from power surges, brownouts, blackouts, shorted or opened I/O devices, or any type of system component failure. Any errors of the PLC, the external power source, and/or external devices can cause a system malfunction. The potentially dangerous effects of these errors on the whole system can be prevented with proper safety precautions. The use of properly designed safety circuits external to the PLC will protect against both equipment damage and human injury.

Interlock Circuit

An interlock circuit can control and prevent problems such as those caused by unexpected or reversed operation of a motor. Install the interlock circuit external to the PLC control wiring and circuitry.

Emergency Stop Circuit

Every industrial control application involving electrical or moving parts should be wired with an emergency stop circuit. The emergency stop circuit turns off the power immediately to all output devices in the system. The emergency stop circuit should provide independent power cutoff from the PLC system.

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Power-Up Sequence

In a properly designed control system, the default Off state of the system is the safe state, in which no machinery is operating. Before the PLC is powered-up, line power and control power are applied to the system. Once the system is powered up in the safe/default state, the PLC is powered up and begins system control. As necessary, the control system should be modified to ensure the proper delayed startup to prevent problems on power-up.

For example: 1) Run the PLC after turning on the power
2) Use an external or internal timer to delay the operation of the PLC.

Momentary Power Failure and Voltage Drop

Momentary Power Failure

The D50 PLC will ride through momentary power failures of 10 msec or less. The PLC will stop and turn off its outputs if a momentary power failure greater than 20 msec occurs. For momentary power failures between 10 msec and 20 msec, the PLC's operation depends on circumstances at that time, and is not defined. The control system should be designed specifically to ensure safe operation for these potential power-loss conditions.

Voltage Drop (Brownouts)

The PLC will stop and turn off its outputs if the PLC 's power supply voltage drops below the allowable fluctuating voltage range (see specifications for power supply units).

⚠ CAUTION: Steps should be taken to prevent damage to the PLC system through fluctuating voltages, brownouts, blackouts, shorts, ground faults, or other power supply failures. For example, you may need to apply an isolation transformer before the incoming PLC power supply and/or I/O control wiring.

System Installation Guidelines

Environmental Usage Conditions

Avoid the Following Environments:

- Ambient temperature outside the range of 0 to 55°C (32 to 131°F).
- Humidity levels outside the range of 20% to 90%.
- Abrupt temperature variations which lead to the formation of dew.
- Presence of corrosive or flammable gases.
- Presence of dense dust, salt, and iron concentrations.
- Presence of corrosive solutions such as benzene, thinner, alcohol, ammonia and caustic soda.

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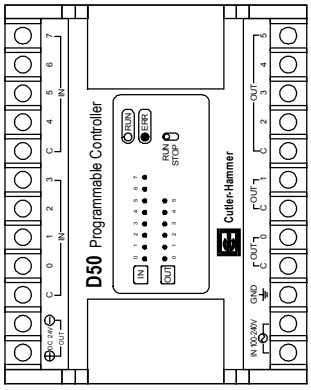
- Locations subject to direct impact greater than 10 G or vibrations greater than 1 G @ 57-2000 Hz.
- Direct sunlight.
- Presence of water, oil, and other chemicals.

Electrical Noise Considerations

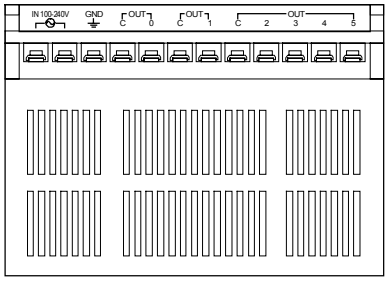
- Do not install near high-tension wires, high-voltage devices, power cables, power devices, and other devices which generate large power surges or electromagnetic fields when starting and stopping.
- Do not place near wireless communications devices with transceivers, such as walkie talkies, cellular phones, or shortwave radios.

Control Panel Installation

- Leave enough space at the top of unit from other devices or wiring ducts to allow ventilation space and easy replacement and wiring of the unit (see the following diagrams).
- Do not mount the PLC system rotated vertically, or facing up or down. This will prevent proper air cooling of the PLC CPU, which will cause abnormal overheating inside the PLC (see the following diagrams).



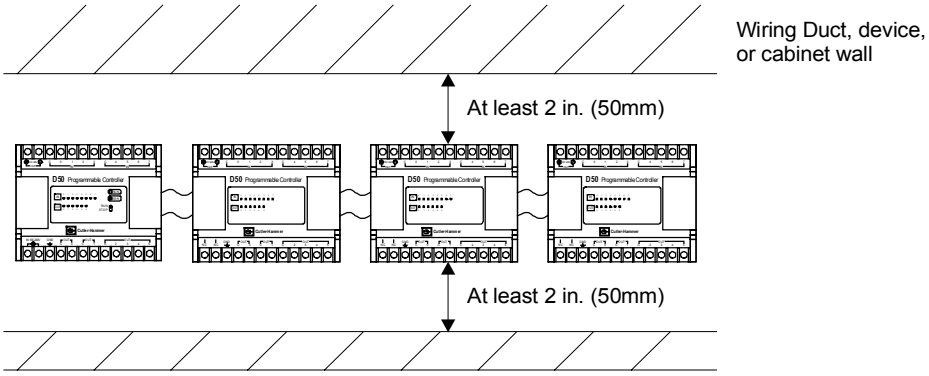
Incorrect: Vertical Mounting



Incorrect: Horizontal Mounting

- Avoid installation over heat generating equipment such as heaters, transformers, and power resistors.
- Avoid radiation noise by leaving a minimum distance of 4 inches (100 mm) from the surface of each unit to the power cable, and the noise-generating device (motor starter, solenoid, etc.).

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Leave at least 2 inches (50 mm) from the duct or other devices:

- To prevent overheating.
- For easy replacement and wiring of the unit.

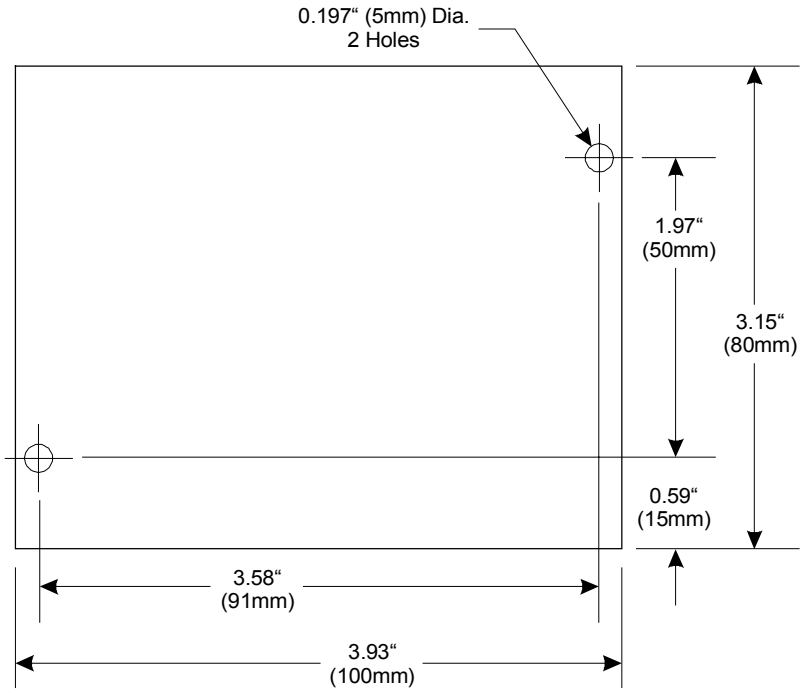
When installing the PLC in a cabinet or enclosure:

- Leave 4 inches (100 mm) or more from the front surface of unit.
- This area in front of the PLC helps to avoid the effects of emission, noise, and heat.
- The additional space also allows for easier connection to the programming port as needed.

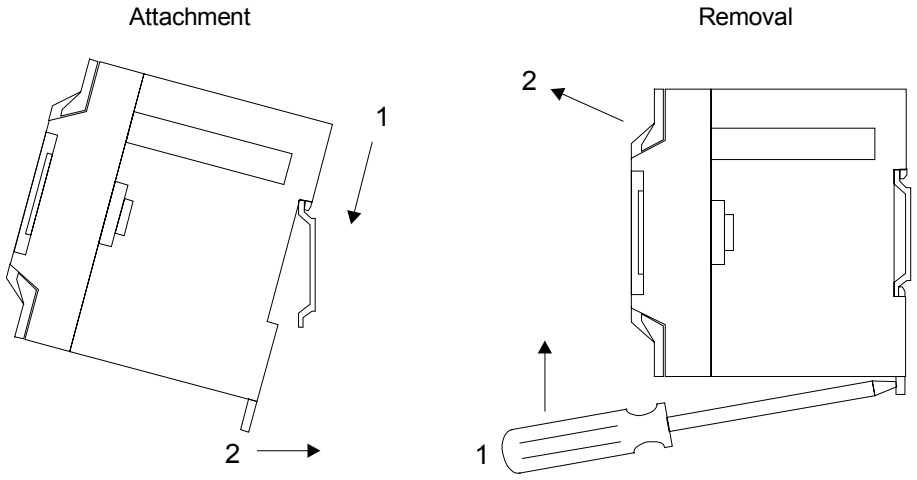
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System Wiring and Installation Procedures

Installation Dimensions

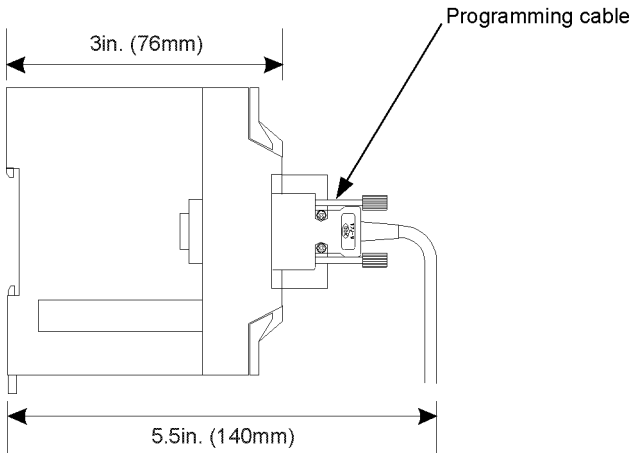


DIN Rail Mounting



Unit Installation Height

The depth of the D50 PLC is 3 inches (76 mm) when the unit is installed on DIN rail. When the communication cable is connected and the unit is installed in an enclosure, additional space is required. The minimum installation sizes are given in the following diagram.



Expansion Cable Connection

Connecting the Expansion Cable

- The expansion cable is connected between the I/O expansion ports on the controller and expander units.
- The expansion cable is keyed to prevent incorrect wiring, with Pin 1 at the top of the connector.
- The connector can be up to 12” in length for mounting the expansion unit above, below, or farther away from the controller. A 2.5” cable is included with each expansion unit. The following table lists the parts required to construct a longer cable.

Expansion Cable Components

Part	Description
AMP #746286-1	10-socket socket connectors (2)
AMP #499252-5	Strain relief connectors (2) for socket connectors above
Ribbon cable	28AWG stranded wire, 0.050 spacing 10 conductor w/ PVC insulation, 105deg. C, wire #1 color-coded

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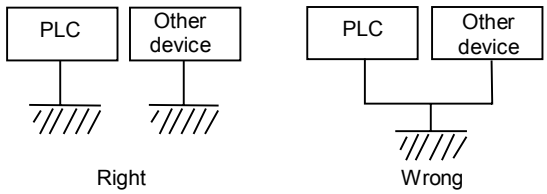
Power Supply Wiring

Power wiring

- When connecting the power cable:
  To reduce power loss in the wiring, use at least 14 AWG (2 mm) cable.
  To reduce the effect of noise, use twisted, shielded cable.
- An isolation transformer can be used to further reduce noise and to prevent failures from power problems such as ground faults.

Grounding

- In normal low-noise environments such as closed-room control cabinets, it is possible to operate the PLC without frame grounding. However, it is necessary to ground the PLC for noisy environments, and is recommended for all installations regardless of electronic noise levels.
- For the frame ground, use a cable of at least 14 AWG (2 mm) in size. The ground should be exclusive to the PLC. Sharing the ground connection with other devices can cause problems due to ground loops and current feedback.



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CPU Operation and Memory

5

This chapter provides you with information about memory addresses and the CPU operation. It includes a terminology section and an overview of registers.

This chapter discusses:

- *The terminology used in the D50 PLC manual*
- *CPU operation and processing*
- *Internal/external address designation*
- *Special function internal addresses*

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Terminology

This section introduces some terminology you should know.

1. **Address (register)**
   Address refers to the location of memory being used. It can refer to the external input/output module or internal memory. An address is categorized into 1 bit, 16 bit (word), or 32 bit (double word).
2. **Bit**
   A bit is the minimum unit required for calculation. It can be either On (1) or Off (0).
3. **Byte**
   A byte is made up of 8 bits. It can hold data values from 0 to 255. In base 16, or hexadecimal, a byte can be expressed as 0 to FF. You cannot have a value greater than 255 when using one byte.
4. **Word**
   A word is made of 16 bits. It can hold data values from 0 to 65,535. In base 16 a word can be expressed as 0 to FFFF.
5. **Double Word**
   A double word is made of 32 bits. It can hold data values from 0 to 4,294,976,295. In base 16 a double word can be expressed as 0 to FFFFFFFF. In the D50, a double word is made up of two consecutive word addresses.
6. **Scan Time**
   The CPU follows a procedure in which it 1) reads the inputs, 2) processes the ladder program, and 3) updates the outputs. It continually repeats this process. This 3-step process is called a "scan," and the time it takes to complete this process is the "scan time." In a typical PLC application, most of the scan time is used to process the program. When programming, keep in mind that the scan time will increase as you increase the number of inputs and outputs and/or the size of the program.
7. **Edge**
   An edge is defined as the point when an input changes state. For example, a rising edge occurs during the very first scan after the input has changed from Off to On. A falling edge occurs after the input has changed from On to Off.
8. **Hex (Hexadecimal)**
   A hexadecimal number is a value expressed in Base 16. Base 16 values consist of digits from 0 to F. In a byte, word, or double word, each set of 4 bits corresponds to a single hex digit. For example, the binary value 01001111 would correspond to the hex value 4F, and a decimal value of 79. A hex value is designated by the use of the symbol "$" in front of the value (i.e. $4F is the hex value 4F).
8. **BCD (Binary Coded Decimal)**
   BCD is used to express a decimal digit (0 to 9) using 4 bits. Conversion of BCD values can be done in hexadecimal calculations. For example, the BCD representation of decimal 27 would be two sets of 4 bits: 0010 0111.
9. **EEPROM**
   EEPROM is electronically erasable and programmable memory that retains its data even through loss of power. The PLC program is stored in EEPROM and will be retained when power is off.



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10. **GPC**
    Graphic Programming Console. Cutler-Hammer offers two program loader software packages for programming, monitoring, and configuring the D50 PLC. The DOS-based package is GPC5, the Windows™-based package is WinGPC. In this manual, GPC is used to refer to either of these programs.

Overview of CPU Operation Mode

What Is the CPU Operation Mode?

The CPU has an external RUN/STOP switch. The PLC performs a system check that determines the position of the switch. The switch position determines which operating mode the PLC is in. It can be in Run, Stop, or Error mode.

Run Mode (operating)

The D50 PLC reads the external input signals and executes the user program stored in RAM. The external outputs are updated every scan according to program results. When the switch is in Run Mode, the user can also use the GPC program loader software to switch between the RUN and STOP states.

Stop Mode

The user program is stopped and the external outputs are turned Off. In the Stop mode, you can correct, delete, and transfer the program.

Error Mode

The Error mode occurs when the D50 PLC finds an error after running the self-diagnostics. When an error occurs, the CPU stops program operation and turns off all external outputs. When the Error mode occurs, do one of the following:

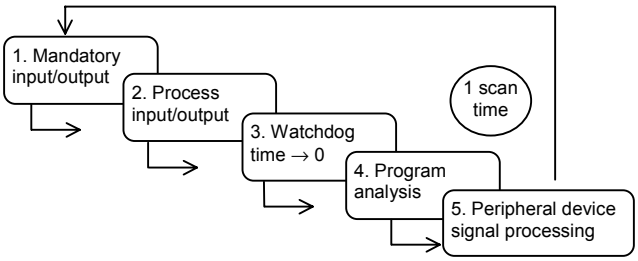
- Check the error code and take appropriate measures, then change power from Off to On.
- Switch the mode switch back to the STOP position. When the switch is returned to RUN the program and data are re-initialized (excluding the retentive data).



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CPU Processing Procedure

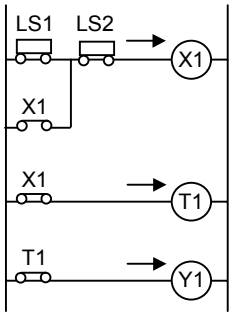
Program Processing Procedure



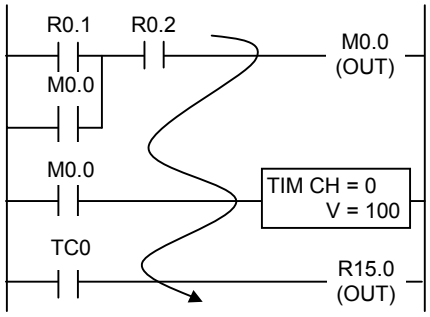
The diagram above indicates the PLC program processing procedure. The CPU regularly repeats procedure 1 through 5. This cycle is called 1 scan time.

1. **Mandatory input/output processing**
   The internal force table is applied to internal/external I/O, turning forced I/O On or Off.
2. **Input/output processing**
   Preserves the On/Off state of the external I/O and uses it as input in the next scan. (For accurate processing, input should continue for more than 1 scan time.) The processed program outputs are sent from the internal memory to the external modules.
3. **Watchdog time initialization**
   The watchdog elapsed time value is set to 0. This value is the watchdog calculation point until the next scan.
4. **Program analysis**
   Executes the program from its first step to its final step and stores the internal/external output in the working RAM.
5. **Peripheral device signal processing**
   Stores data from communications module or peripheral device in the internal memory.

The following illustration shows the difference between the relay board and PLC sequence processing. The relay carries out all sequences simultaneously while the PLC processes sequentially throughout the program.



Processing of relay sequence
(parallel process)



Processing of PLC program
(serial process)

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Introduction to Registers

The D50 PLC has a series of registers for storing data. Different registers store different types of data.

1. R (Relay) register (Can be bit, byte, or word)
   Indicates the internal memory address which is directly linked with the real-world external input/output module. The address and number of R registers are predefined for the controller and expansion module I/O.
2. M (Memory) register (Can be bit, byte, or word)
   An internal bit memory address which supports relay logic operations. Can also be used as a byte or word variable for general calculations and programs. M Registers are non-retentive—when the power of the PLC is Off or the CPU has stopped, the register value is reset to 0.
3. W (Word) register (Can be byte or word)
   Used for general calculations, data storage, and recipe values. Values are cleared after the power is turned off, or by new program download.
4. K (Keep) register (Can be bit, byte, or word)
   Same usage as M registers. The K Registers are retentive—the value is preserved when the power is turned off.
5. F (Flag) register (Can only be bit)
   These bit registers provide special application specific functions to the programmer of the PLC. They are also used as diagnostic and system control bits, providing Run/Stop control of the PLC and other system conditions.

Each type of register is used for a variety of purposes. The register used will be determined by the type of function being performed.

1. When a calculation or input value exceeds 255 ($FF), use double mode instructions which can store and calculate values up to 65,535 in the K, M, R, and W registers..
2. When a value needs to be stored even through a loss of system power, use the K area. The K area is preserved unless specifically erased. The W area is erased by program downloads or loss of power.
3. For bit operations, such as setting, resetting, shifting, or rotating use the M, K, or R registers. You cannot perform bit operations on W registers.
4. The Set Value of timers and counters is stored in a special area of the W registers, W2048 to W2303. These values can also be addressed using register type SV. The Set Values are then referenced as SV000 to SV255.
5. The Present Value of timers and counters is stored above the Set Values in the W registers, from W2304 to W2559. These values can also be addressed using the PV designation, PV000 to PV255. The Present Values for channels 0 to 16 are maintained in the Stop state. It is also retentive—the value is maintained through loss of power.

Internal/External Address Designation

- The memory address designation types are R, L, M, K, F, W, SV, PV, SR, and TC.
  - Types F and TC can only be used to designate bits.
  - Types W, SV, PV, and SR can only be used to designate words.

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- Types R, L, M, and K can be used for either bits or words.

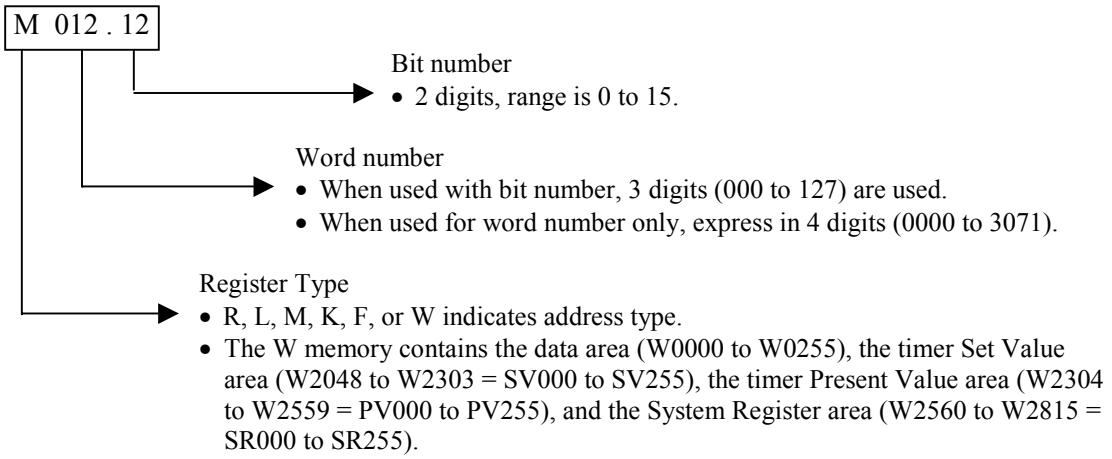
- A bit address is composed of a character (R, L, M, K, F), a three digit word address (000 to 127), a decimal point, and a bit address (0 to 15). The timer/counter contact is represented by the TC label followed by three digits. The three digits indicate the channel number of the timer/counter (TC000 to TC255).
- A word address is composed of a character (R, L, M, K, W) and a four digit number (i.e. W0000 to W0255). Special areas of word memory have alternate designations. For example, words W2560 to W2815 are also referred to as the System Registers, and can be represented as SR0000 to SR0511.
- The bit address indicates an On (1) or Off (0) state. The byte address is composed of 8 bits that holds data values of 0 to 255. The word address is composed of 16 bits that holds data values of 0 to 65,535.

D50 Memory Addresses

Type	Scope	Features
External I/O Area	R000.0 to R003.7 R015.0 to R018.5	Local I/O memory area. 56 points, 8 words
Special I/O Area	R004 to R014 R019 to R029	Configuration register for High-speec counters, Pulse Output, Input delay, and Pulse catch.
Internal Contact	M000.0 to M031.15	Internal auxiliary contact memory area. 512 points, 32 words
Retentive Contact	K000.0 to K015.15	Retentive internal auxiliary contact memory area. 256 points, 16 words
System Flag	F000.0 to F001.15	Special internal contact memory area. 32 points, 2 words
Timer/Counter	TC000 to TC255 Set Value: W2048 (SV000) to W2303 (SV255) Present Value: W2304 (PV000) to W2559 (PV255)	256 channel common use. TC is contact signal or “Done” bit. SV is Set Value, PV is Present Value. SV can hold values from 0 to 65535.
Data Word	W0000 to W0255	Word value memory area. Used for tables, data storage, and math operations. Cannot be designated with a bit.
System Register	SR000 to SR255	Special internal data area for CPU status.

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Expression Example



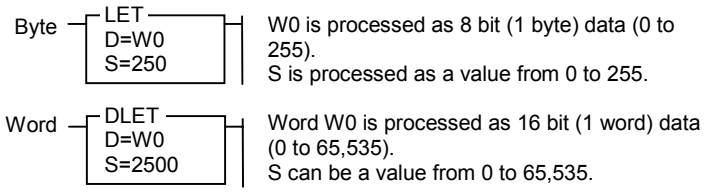
Note: The basic contact and coil instructions require a bit designation and use the 3.2 bit address format. Comparison and application instructions most often use word parameters, and are expressed using the 4 digit word address.

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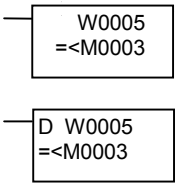
Double Mode Address Designation

- Words are composed of two bytes put together. The designation for a word is exactly the same as the designation for the byte, consisting of a one character register type and a 4 digit word address. Bytes hold 8 bits of data, words hold 16 bits of data.
- The type of instruction used determines whether the register is processed as a single byte or a word. For comparison instructions (>, <, ==, etc.), the programmer must be in "Double Mode" to enter a word comparison (refer to program loader manual for details). For application instructions, those instructions that start with a D in front of the related instruction are word instructions, and process the data as 16-bit words instead of bytes.

Example 1:



Example 2: Comparison Instruction



The example shows comparison instructions being used in the single mode of GPC. The parameters W0005 and M0003 represent only 8 bits of data. The high 8 bits are NOT used as part of the comparison.

In this example, GPC is in double mode and comparison instructions are used. The comparison is performed on 16 bits of data. All of word W0005 and M0003 will be compared.

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Absolute Address Designation

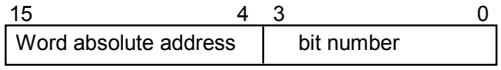
In LDR, DLDR, STO, DSTO instructions, the absolute address is used to perform indirect memory operations using pointers. The absolute address is also used by the D50 program loader port protocol for reading and writing memory areas.

	Register Address	Absolute Address	
		Dec.	Hex.
External I/O	R0000	0	0000
	R0001	1	0001
	R0002	2	0002
	:	:	:
	R0028	28	001C
	R0029	29	001D
Internal Contact	M0000	192	00C0
	M0001	193	00C1
	M0002	194	00C2
	:	:	:
	M0030	222	00DE
	M0031	223	00DF
Internal Keep Contact	K0000	320	0140
	K0001	321	0141
	K0002	322	0142
	K0003	323	0143
	:	:	:
	K0014	334	014E
	K0015	335	014F

	Register Address	Absolute Address	
		Dec.	Hex.
Data Words	W0000	512	0200
	W0001	513	0201
	W0002	514	0202
	:	:	:
	W0254	766	02FE
	W0255	767	02FF
T/C Set Value	SV000	512	0200
	SV001	2560	0A00
	:	:	:
	SV255	2815	0AFF
T/C Present Value	PV000	2816	0B00
	PV001	2817	0B01
	:	:	:
	PV255	3071	0BFF
System Registers	SR000	3072	0C00
	SR001	3073	0C01
	:	:	:
	SR254	3326	0CFE
	SR255	3327	0CFF

When accessing a bit absolute address using the program loader port communications protocol, the bit address (0 to 15) is kept separate from the word address (as shown below).

1 word display

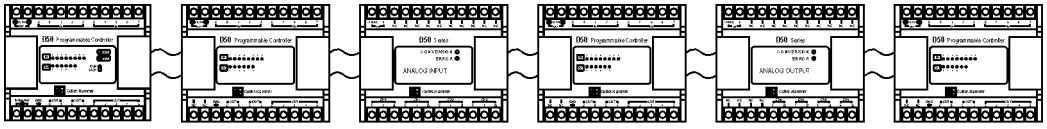


For example, the absolute bit address for K012.12 internal contact is $14CC (hex).
(word absolute address = $014C + bit number = $C = $14CC)

Refer to the appendix for a detailed explanation of the communications protocol.

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I/O Address Designation



Example I/O Addressing Configuration

Module No.	00	01	02	03	06	07
I/O Points	14	14	4 words	14	2 words	14
Word No.	R0, R15	R1, R16	W240 – W243	R2, R17	W248, W249	R3, R18
Bit No.	R0.0 – R0.7 R15.0 – R15.5	R1.0 – R1.7 R16.0 – R16.5	-	R2.0 – R2.7 R17.0 – R17.5	-	R3.0 – R3.7 R18.0 – R18.5

Digital I/O Address Designation

- The CPU assigns addresses to the digital inputs in sequential order, starting at address R0. Each module uses 8 bits of the address for the 8 inputs.
- The CPU assigns addresses to the digital outputs in sequential order, starting at address R15. Each modules uses 6 bits of the address for the 6 outputs.
- A maximum of 3 digital modules, of any mix of voltage I/O type, may be added.

Analog I/O Address Designation

- The first analog input module uses data words W240 to W243 for its four analog input channels. Each word contains the 12-bit representation of the analog input signal for the channel. The second analog input module is assigned words W244 to W247. These assignments are independent of the position of the module in the chain, or whether an analog output module is present.
- The first analog output module uses data words W248 and W249 for its two analog output channels. The 12-bit representation to be output as an analog signal on the channel must be placed in these words. The second analog input module is assigned words W250 and W251. These assignments are independent of the position of the module in the chain, or whether an analog input module is present.
- A maximum of two analog modules, input and/or output, may be added.

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Special Internal Addresses

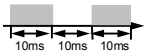
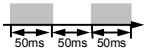
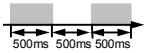
F0.0 to F0.15 (F0 word register) System/Diagnostic Functions

Address	Function	Details	Remarks
F0.0	System check	When power is applied, the system runs self-diagnostics. Should any fault exist, the error lamp is turned on. Output and operation are halted.	Normal: Off
F0.1	CPU ROM check	When power is applied, the system self-checks the ROM. Should any faults exist, the error lamp is turned on. Output and operation are halted.	Normal: Off
F0.2	CPU RAM check	When the power is applied, the system self-checks the RAM. Should any faults exist, the error lamp is turned on. Output and operation are halted.	Normal: Off
F0.3	User program memory error	If the user program memory is damaged or the program is faulty, the error lamp is turned on. Output and operation are halted.	Normal: Off
F0.4	Program check	The CPU initially runs and checks the user program's syntax. In the case of an error, the error lamp is turned on. Output and operation are halted.	Normal: Off
F0.5	Not Used		
F0.6	Module change error	On when an I/O module is removed/added/fails while the system is running. The error lamp is turned on, and output and operation are halted.	Normal: Off
F0.7	Module type error	On when module information that is stored in the CPU and module that is installed are different types. The error lamp is turned on and operation stops.	Normal: Off
F0.8	Input data control	Off when the running CPU input module's data is not updated. (Input update is turned Off.)	Normal: On
F0.9	Output data control	Off to suspend updating of the output modules while the CPU is in the run state. (Output update is turned Off.) The outputs are maintained in their last valid state prior to update being disabled.	Normal: On
F0.10	All outputs OFF	Turns all outputs off while CPU is in the run state. (Outputs are disabled.)	Normal: On
F0.11	Not Used		
F0.12	Not Used		
F0.13	Not Used		
F0.14	Program changes during run	On when error-checking the program while in run mode. If there are syntax errors, the CPU is stopped.	Normal: Off
F0.15	Run state control	On when the CPU is in the run state. Off when stopped or paused.	Normal: On



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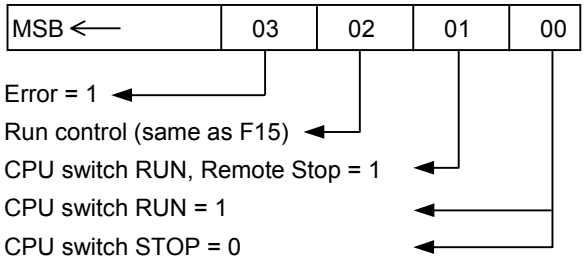
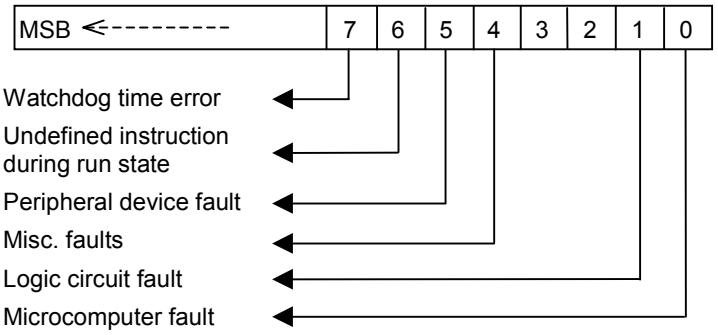
F1.0 to F1.15 (F1 word register) Special Application Functions

Address	Function	Details	Note
F1.0	First single scan	Maintain On state for first single-scan period, when the CPU changes its status from Stop to Run.	
F1.1	Scan clock	Cycle On/Off state for each scan during the program. (1Scan On, 1Scan Off)	
F1.2	0.02 sec. Clock	10 ms: On, 10 ms: Off 	
F1.3	0.1 sec. Clock	50 ms: On, 50 ms: Off 	
F1.4	1 sec. Clock	500 ms: On, 500 ms: Off 	
F1.5	Instantaneous interrupt	On when power is off for over 20 ms.	Maintained
F1.6	Execute status	On when the CPU is in the run state.	
F1.7	Keep error display	On when the K retentive data is destroyed and/or changed on power loss.	
F1.8	Carry Flag	On in the event of carry when performing math instructions (ADD, SUB, etc.)	
F1.9	Division by zero error	On when the denominator of division commands is zero.	
F1.10	Range designation error	On when the absolute address used in LDR and STO instructions exceeds the specified range.	
F1.11	Reserved	System use.	Do not use.
F1.12	Reserved	System use.	Do not use.
F1.13	Reserved	System use.	Do not use.
F1.14	Reserved	System use.	Do not use.
F1.15	Reserved	System use.	Do not use.

Note: The 16 bits in the F1 address provide the CPU's special function and self diagnosis result. They are used for status contacts only, and are not used to modify or control the PLC. Only the F1.5 instantaneous interrupt display contact should be used as an output contact by the user, to be turned off after power loss indication.

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System Registers SR0 to SR255

Address	Function	Detail
SR000	CPU address	Indicates the CPU ID number in the lower 8 bits. 0 to 223 are the valid user-defined values, 255 is the default value.
SR001	CPU status	Indicates current CPU information state. (stop/remote control mode/run mode/error) 
SR002	User watchdog	Indicates the user program watchdog time. (unit: msec)
SR003	Scan time	Indicates the scan time when executing a program. (unit: msec)
SR004	Max. scan time	Indicates maximum value of scan time when executing a program. Initialized as zero when the program mode changes from the stop state to the run state.
SR005 to SR0016	Reserved	System Use – Do not use.
SR017	System error information	Gives result of self-check by CPU. Indicates error content when F0.0 turns On. 
SR018	Location of undefined instruction	Indicates the location of the instruction (the step number) that caused an undefined instruction error during program execution.
SR019	Reserved	System use.
SR020	Multiplication	Stores high order 8 bit values upon executing 16 bit multiplication instructions.
SR021	Remainder – Low	Stores the remainder after a division instruction has been executed (low order 16 bits).
SR022	Remainder – High	Stores the remainder after a division instruction has been executed (high order 16 bits).
SR023 to SR0029	Reserved	System use.

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Address	Function	Detail
SR030	Syntax Error information	Stores syntax error information when the user program fails the system diagnostic check. Each bit in the word indicates a different error condition. See table below.
SR031	Reserved	System Use.
SR032	Error Step #	Contains step number where error occurred when bit 0 of word SR030 is turned On.
SR033	Error Step #	Contains step number where error occurred when bit 1 of word SR030 is turned On.
SR034	Error Step #	Contains step number where error occurred when bit 2 of word SR030 is turned On.
SR036	Error Step #	Contains step number where error occurred when bit 4 of word SR030 is turned On.
SR037	Error Step #	Contains step number where error occurred when bit 5 of word SR030 is turned On.
SR038	Error Step #	Contains step number where error occurred when bit 6 of word SR030 is turned On.
SR039	Error Step #	Contains step number where error occurred when bit 7 of word SR030 is turned On.
SR040	Error Step #	Contains step number where error occurred when bit 8 of word SR030 is turned On.
SR041	Error Step #	Contains step number where error occurred when bit 9 of word SR030 is turned On.
SR042	Error Step #	Contains step number where error occurred when bit 10 of word SR030 is turned On.
SR043	Error Step #	Contains step number where error occurred when bit 11 of word SR030 is turned On.
SR044	Error Step #	Contains step number where error occurred when bit 12 of word SR030 is turned On.
SR045	Error Step #	Contains step number where error occurred when bit 13 of word SR030 is turned On.
SR047	Error Step #	Contains step number where error occurred when bit 15 of word SR030 is turned On.



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Syntax Check Data (16 bits of SR30)

Indicates the result of the automatic check on user program syntax when the programmer or GPC executes a syntax check, and when operation mode is switched from the Stop state to the Run state. If the value of SR30 is not zero, F0.4 turns On. The error lamp also turns On.

There are two error correction methods:

Method 1: Find the error in the CPU online mode, then correct the program.
Method 2: Use the syntax checking function, then correct the program.

Word	Bit	Detail
SR30	0	On if the I/O number range of bit process instruction is beyond the specified range or designates an external contact/output module which is not installed.
	1	On if the channel number of the timer or the counter exceeds 255 or is duplicated.
	2	On if the bit or word number in the application program is beyond the specified range or if it designates a module which is not installed.
	3	Not used.
	4	On if an undefined instruction exists.
	5	On in the event of a user program memory error.
	6	On in the event of miscellaneous errors.
	7	On if the user program memory is destroyed.
	8	On if an external I/O register address is improperly used within the program. For example, OUT R0.1 is used in the program, and R0.1 is an input.
	9	On if the label numbers of the JMP or CALL instructions exceed 63, the corresponding instruction (LBL, SBR) does not exist, and/or the corresponding LBL/SBR instructions exist prior to JMP/CALL instructions.
	10	On if the label number of the LBL instruction exceeds 63 and/or is duplicated.
	11	On if the JMPS/JMP instructions are mistakenly combined and/or used.
	12	On if the FOR/NEXT instructions are mistakenly combined and/or used more than five times. (Loop)
	13	On if SBR/RET instructions are not combined and/or used and/or the SBR instructions overlap or exceed 63.
	14	Not used.
	15	On if no END instruction exists.

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Timer/Counter (TC0-255)

The table below gives the alternate Word address for the timer/counter Set Value and Present Value

Ch	SV	PV
0	W2048	W2304
1	W2049	W2305
2	W2050	W2306
3	W2051	W2307
4	W2052	W2308
5	W2053	W2309
6	W2054	W2310
7	W2055	W2311
8	W2056	W2312
9	W2057	W2313
10	W2058	W2314
11	W2059	W2315
12	W2060	W2316
13	W2061	W2317
14	W2062	W2318
15	W2063	W2319
16	W2064	W2320
17	W2065	W2321
18	W2066	W2322
19	W2067	W2323
20	W2068	W2324
21	W2069	W2325
22	W2070	W2326
23	W2071	W2327
24	W2072	W2328
25	W2073	W2329
26	W2074	W2330
27	W2075	W2331
28	W2076	W2332
29	W2077	W2333
30	W2078	W2334
31	W2079	W2335
32	W2080	W2336
33	W2081	W2337
34	W2082	W2338
35	W2083	W2339
36	W2084	W2340
37	W2085	W2341
38	W2086	W2342
39	W2087	W2343

Ch	SV	PV
40	W2088	W2344
41	W2089	W2345
42	W2090	W2346
43	W2091	W2347
44	W2092	W2348
45	W2093	W2349
46	W2094	W2350
47	W2095	W2351
48	W2096	W2352
49	W2097	W2353
50	W2098	W2354
51	W2099	W2355
52	W2100	W2356
53	W2101	W2357
54	W2102	W2358
55	W2103	W2359
56	W2104	W2360
57	W2105	W2361
58	W2106	W2362
59	W2107	W2363
60	W2108	W2364
61	W2109	W2365
62	W2110	W2366
63	W2111	W2367
64	W2112	W2368
65	W2113	W2369
66	W2114	W2370
67	W2115	W2371
68	W2116	W2372
69	W2117	W2373
70	W2118	W2374
71	W2119	W2375
72	W2120	W2376
73	W2121	W2377
74	W2122	W2378
75	W2123	W2379
76	W2124	W2380
77	W2125	W2381
78	W2126	W2382
79	W2127	W2383

Ch	SV	PV
80	W2128	W2384
81	W2129	W2385
82	W2130	W2386
83	W2131	W2387
84	W2132	W2388
85	W2133	W2389
86	W2134	W2390
87	W2135	W2391
88	W2136	W2392
89	W2137	W2393
90	W2138	W2394
91	W2139	W2395
92	W2140	W2396
93	W2141	W2397
94	W2142	W2398
95	W2143	W2399
96	W2144	W2400
97	W2145	W2401
98	W2146	W2402
99	W2147	W2403
100	W2148	W2404
101	W2149	W2405
102	W2150	W2406
103	W2151	W2407
104	W2152	W2408
105	W2153	W2409
106	W2154	W2410
107	W2155	W2411
108	W2156	W2412
109	W2157	W2413
110	W2158	W2414
111	W2159	W2415
112	W2160	W2416
113	W2161	W2417
114	W2162	W2418
115	W2163	W2419
116	W2164	W2420
117	W2165	W2421
118	W2166	W2422
119	W2167	W2423

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Timer/Counter Word addressing

Ch	SV	PV
120	W2168	W2424
121	W2169	W2425
122	W2170	W2426
123	W2171	W2427
124	W2172	W2428
125	W2173	W2429
126	W2174	W2430
127	W2175	W2431
128	W2176	W2432
129	W2177	W2433
130	W2178	W2434
131	W2179	W2435
132	W2180	W2436
133	W2181	W2437
134	W2182	W2438
135	W2183	W2439
136	W2184	W2440
137	W2185	W2441
138	W2186	W2442
139	W2187	W2443
140	W2188	W2444
141	W2189	W2445
142	W2190	W2446
143	W2191	W2447
144	W2192	W2448
145	W2193	W2449
146	W2194	W2450
147	W2195	W2451
148	W2196	W2452
149	W2197	W2453
150	W2198	W2454
151	W2199	W2455
152	W2200	W2456
153	W2201	W2457
154	W2202	W2458
155	W2203	W2459
156	W2204	W2460
157	W2205	W2461
158	W2206	W2462
159	W2207	W2463
160	W2208	W2464
161	W2209	W2465
162	W2210	W2466
163	W2211	W2467
164	W2212	W2468
165	W2213	W2469

Ch	SV	PV
166	W2214	W2470
167	W2215	W2471
168	W2216	W2472
169	W2217	W2473
170	W2218	W2474
171	W2219	W2475
172	W2220	W2476
173	W2221	W2477
174	W2222	W2478
175	W2223	W2479
176	W2224	W2480
177	W2225	W2481
178	W2226	W2482
179	W2227	W2483
180	W2228	W2484
181	W2229	W2485
182	W2230	W2486
183	W2231	W2487
184	W2232	W2488
185	W2233	W2489
186	W2234	W2490
187	W2235	W2491
188	W2236	W2492
189	W2237	W2493
190	W2238	W2494
191	W2239	W2495
192	W2240	W2496
193	W2241	W2497
194	W2242	W2498
195	W2243	W2499
196	W2244	W2500
197	W2245	W2501
198	W2246	W2502
199	W2247	W2503
200	W2248	W2504
201	W2249	W2505
202	W2250	W2506
203	W2251	W2507
204	W2252	W2508
205	W2253	W2509
206	W2254	W2510
207	W2255	W2511
208	W2256	W2512
209	W2257	W2513
210	W2258	W2514
211	W2259	W2515

Ch	SV	PV
212	W2260	W2516
213	W2261	W2517
214	W2262	W2518
215	W2263	W2519
216	W2264	W2520
217	W2265	W2521
218	W2266	W2522
219	W2267	W2523
220	W2268	W2524
221	W2269	W2525
222	W2270	W2526
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232	W2280	W2536
233	W2281	W2537
234	W2282	W2538
235	W2283	W2539
236	W2284	W2540
237	W2285	W2541
238	W2286	W2542
239	W2287	W2543
240	W2288	W2544
241	W2289	W2545
242	W2290	W2546
243	W2291	W2547
244	W2292	W2548
245	W2293	W2549
246	W2294	W2550
247	W2295	W2551
248	W2296	W2552
249	W2297	W2553
250	W2298	W2554
251	W2299	W2555
252	W2300	W2556
253	W2301	W2557
254	W2302	W2558
255	W2303	W2559

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Note: Channel: The inherent number of the timer and the counter.

Set Value (SV): The designated value for the timer (to turn On) and the counter (number of times On) to start operation.

Present Value (PV): Current processing value of the timer (elapsed time) and the counter (number of counts).

Note: When using GPC software, the above W registers can be represented as follows.

Ch	Set Value (SV)	Present Value (PV)
0	W2048 = SV0	W2304 = PV0
1	W2049 = SV1	W2305 = PV1
:	:	:
255	W2303 = SV255	W2559 = PV255

Where SV is Set Value and PV is Present Value.

⚠ CAUTION: Be sure you understand the programming of the timer/counter thoroughly. If you change the above registers while the program is running or program them incorrectly, errors or damage may occur.

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Instructions

6

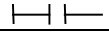
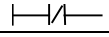
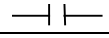
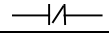
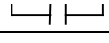
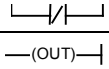
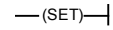
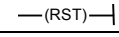
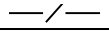
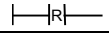
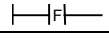
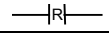
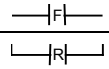
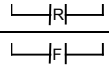
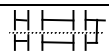
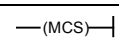
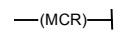
This chapter contains all of the instructions that are used with the D50 PLC. The instructions are grouped by function, and then explained in detail.

This chapter discusses:

- *The instructions that are used with the D50 PLC*
- *How to read the descriptions of the instructions*
- *Detailed information concerning the usage of the instructions*

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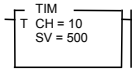
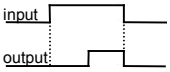
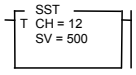
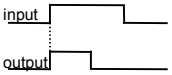
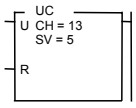
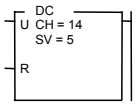
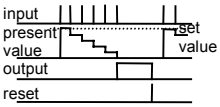
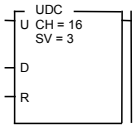
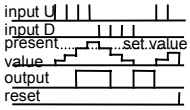
Basic Instructions

Mnemonic	Command	Ladder Symbol	Description
STR	Start		Start NO contact.
STN	Start Not		Start NC contact.
AND	And		NO contact series circuit.
ANN (ADN)	And Not		NC contact series circuit.
OR	Or		NO contact parallel circuit.
ORN	Or Not		NC contact parallel circuit.
OUT	Out		Relay output.
SET	Set		Turn On output.
RST	Reset		Turn Off output.
NOT	Not		Invert logic result.
STR DIF	Start Differential		Start rising edge contact ().
STR DFN	Start Dif. Not		Start falling edge contact ().
AND DIF	And Dif.		Rising edge series connection ().
AND DFN	And Dif. Not		Falling edge series connection ().
OR DIF	Or Dif		Rising edge parallel connection ().
OR DFN	Or Dif. Not		Falling edge parallel connection ().
ANB	And Block		Circuit block series connection.
ORB	Or Block		Circuit block parallel connection.
MCS	Master Control Set		Start batch processing block.
MCR	Master Control Reset		End batch processing block.

Note: NO = Normally Open
NC = Normally Closed

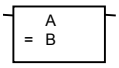
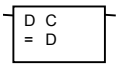
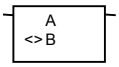
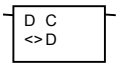
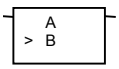
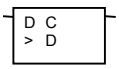
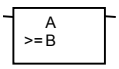
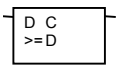
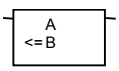
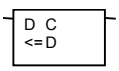
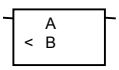
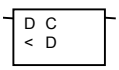
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Timer/Counter Instructions

Mnemonic	Command	Ladder Symbol	Description	Remarks
TIM	On Delay Timer		Turn on after set delay time from input on. 	Time Base: Ch 0-15: 0.01s Ch 16-255: 0.1s Setting range: SV = 0-65535 Done Contact: TC + channel no.
SST	Single Shot Timer		Turn off after set delay time from input on. 	Time Base: Ch 0-15: 0.01s Ch 16-255: 0.1s Setting range: SV = 0-65535 Done Contact: TC + channel no.
UC	Up Counter		Up counter 	Range of channel: Ch 0 to 255 (Shared with timer) Setting range: SV = 0-65535 Done Contact: TC + channel no.
DC	Down Counter		Down counter 	Range of channel: Ch 0 to 255 (Shared with timer) Setting range: SV = 0-65535 Done Contact: TC + channel no.
UDC	Up-Down Counter		Up/down counter 	Range of channel: Ch 0 to 255 (Shared with timer) Setting range: SV = 0-65535 Done Contact: TC + channel no.

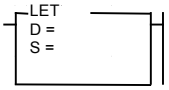
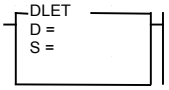
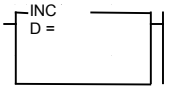
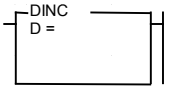
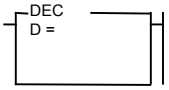
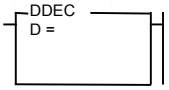
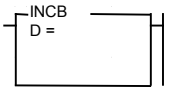
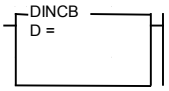
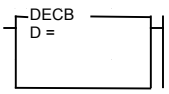
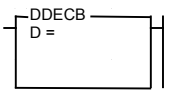
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Comparison Instructions

Mnemonic	Command	Byte	Word	Description
STR = AND = OR =	START = AND = OR =			On if A(C) value and B(D) value are the same.
STR <> AND <> OR <>	START <> AND <> OR <>			On if A(C) value and B(D) value are different. <> means the same as ≠.
STR > AND > OR >	START > AND > OR >			On if A(C) value is greater than B(D) value.
STR >= AND >= OR >=	START >= AND >= OR >=			On if A(C) value is greater than or equal to B(D) value.
STR <= AND <= OR <=	START <= AND <= OR <=			On if A(C) value is less than or equal to B(D) value.
STR < AND < OR <	START < AND < OR <			On if A(C) value is less than B(D) value.

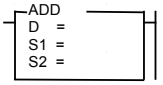
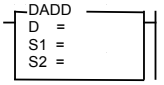
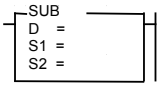
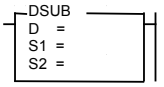
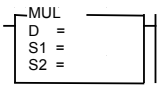
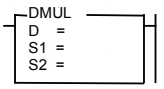
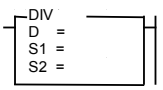
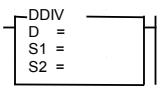
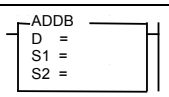
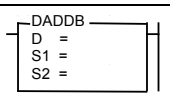
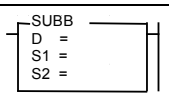
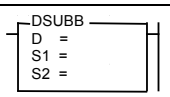
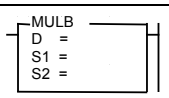
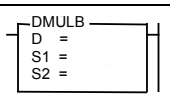
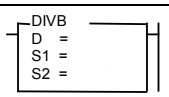
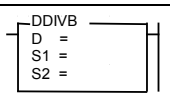
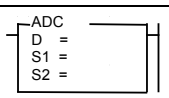
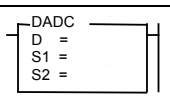
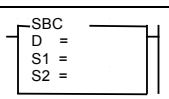
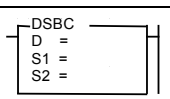
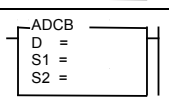
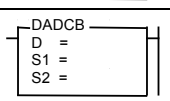
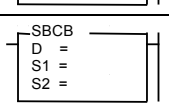
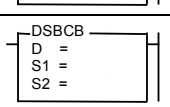
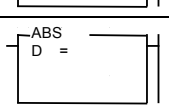
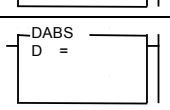
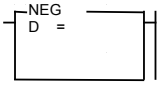
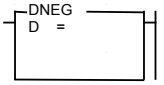
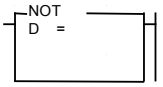
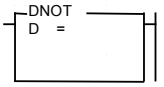
Substitution, Increment/Decrement Instructions

Note: Application instructions that operate in double mode on whole words (16-bit) are designated with a "D" in front of the single mode instruction. For example, DINC refers to double mode word decimal increment, DDEC refers to double mode word decimal decrement, etc.

Mnemonic	Command	Byte	Word	Description
LET (DLET)	Let (Substitution)			Store value of designated register S into D.
INC (DINC)	Decimal increment			D value increased by 1 whenever input is On.
DEC (DDEC)	Decimal decrement			D value decreased by 1 whenever input is On.
INCB (DINCB)	BCD increment			D value increased by 1 (BCD) whenever input is On.
DECB (DDECB)	BCD decrement			D value decreased by 1 (BCD) whenever input is On.

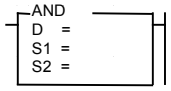
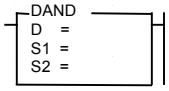
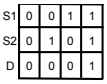
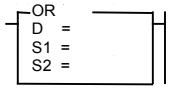
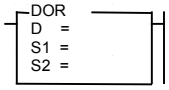
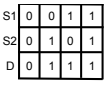
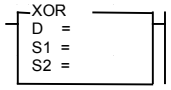
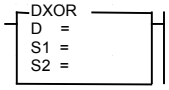
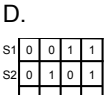
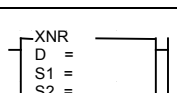
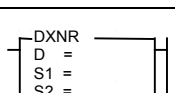
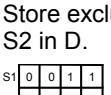
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Arithmetic Instructions

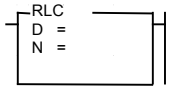
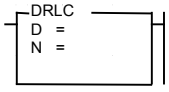
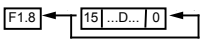
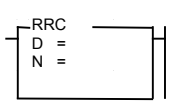
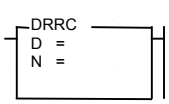
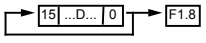
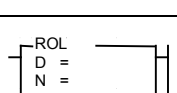
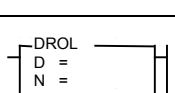
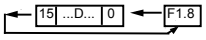
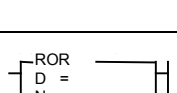
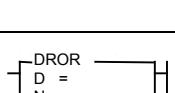
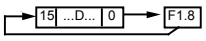
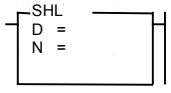
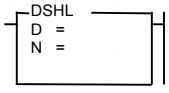
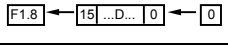
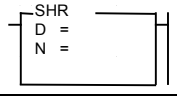
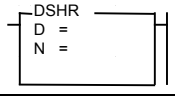
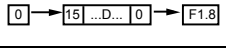
Mnemonic	Command	Byte	Word	Description
ADD (DADD)	Decimal addition			D = S1 + S2 (Decimal operation)
SUB (DSUB)	Decimal subtraction			D = S1 - S2 (Decimal operation)
MUL (DMUL)	Decimal multiplication			D = S1 × S2 (Decimal operation)
DIV (DDIV)	Decimal division			D = S1/S2 (Decimal operation)
ADDB (DADDB)	BCD addition			D = S1 + S2 (BCD operation)
SUBB (DSUBB)	BCD subtraction			D = S1 - S2 (BCD operation)
MULB (DMULB)	BCD multiplication			D = S1 × S2 (BCD operation)
DIVB (DDIVB)	BCD division			D = S1/S2 (BCD operation)
ADC (DADC)	Decimal addition w/carry			D = S1 + S2 + CY (Decimal operation, include carry)
SBC (DSBC)	Decimal subtraction w/carry			D = S1 - S2 - CY (Decimal operation, include carry)
ADCB (DADCB)	BCD addition w/carry			D = S1 + S2 + CY (BCD operation, include carry)
SBCB (DSBCB)	BCD subtraction w/carry			D = S1 - S2 - CY (BCD operation, include carry)
ABS (DABS)	Absolute value			D = |D| (Absolute value operation)
NEG (DNEG)	Negative (2's complement)			Store the 2's complement of D in D (1's complement + 1).
NOT (DNOT)	NOT (1's complement)			Store the 1's complement of D in D.

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Logic Instructions

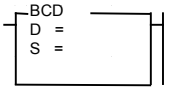
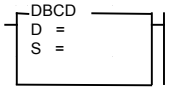
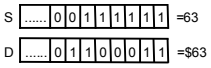
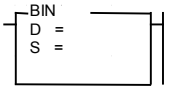
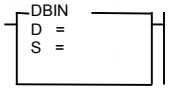
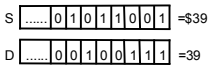
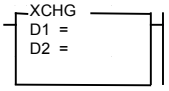
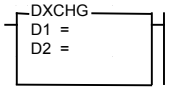
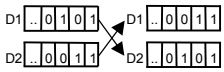
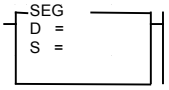
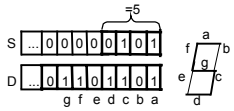
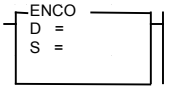
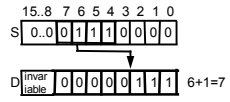
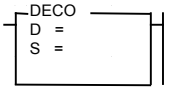
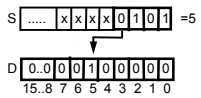
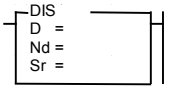
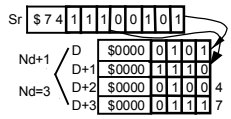
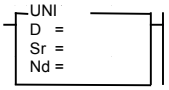
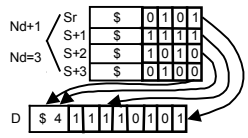
Mnemonic	Command	Byte	Word	Description
WAND (DAND)	Bitwise AND (logic multiply)			Store AND of S1 and S2 in D. 
WOR (DOR)	Bitwise OR (logic sum)			Store OR of S1 and S2 in D. 
XOR (DXOR)	Exclusive OR			Store exclusive OR of S1 and S2 in D. 
XNR (DXNR)	Exclusive OR NOT (equal circuit)			Store exclusive OR NOT of S1 and S2 in D. 

Rotation Instructions

Mnemonic	Command	Byte	Word	Description
RLC (DRLC)	Rotate left without carry			Rotate contents of designated register D to the left N times. (lower→higher) 
RRC (DRRC)	Rotate right without carry			Rotate contents of designated register D to the right N times. (higher→lower) 
ROL (DROL)	Rotate left			Rotate (shift) to the left N times. (lower→higher) (Input F1.8 value for low bit) 
ROR (DROR)	Rotate right			Rotate (shift) to the right N times. (higher→lower) (Input F1.8 value for high bit) 
SHL (DSHL)	Shift left			Shift value of designated register D to the left N times. (Input 0 for low bit) 
SHR (DSHR)	Shift right			Shift value of designated register D to the right N times. (Input 0 for high bit) 

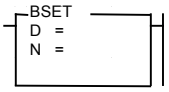
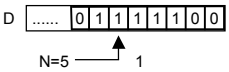
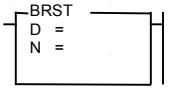
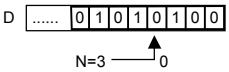
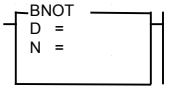
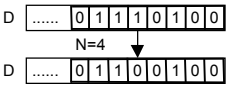
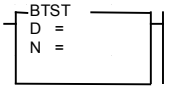
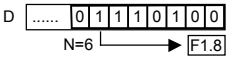
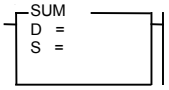
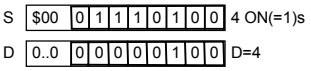
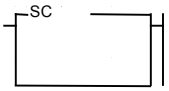
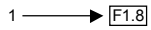
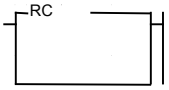
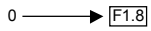
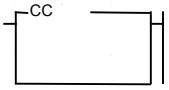
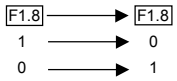
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Word Conversion Instructions

Mnemonic	Command	Byte	Word	Description
BCD (DBCD)	Binary Coded Decimal			Convert binary number of S to BCD and store in D. 
BIN (DBIN)	Binary			Convert BCD of S to binary number and store in D. 
XCHG (DXCHG)	Exchange			Exchange D1 and D2. 
SEG	Segment			Convert the low-order 4 bit value of S to 7-segment display pattern and store in D. 
ENCO	Encode			Store the location of the highest set bit in S in D. 
DECO	Decode			Convert the low-order 4 bit value of S to a power of 2 (2^S) and store in D. 
DIS	Dissemble			Separate Sr into Nd+1 units of 4 bits each, and store in the low 4 bits of words starting at D. (N = 0-3) 
UNI	Unify			Combine the low 4 bits of Nd+1 words starting at Sr, and store in D. (Nd = 0-3) 

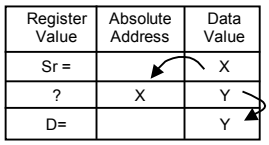
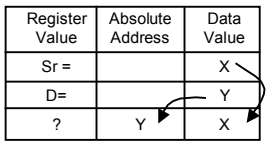
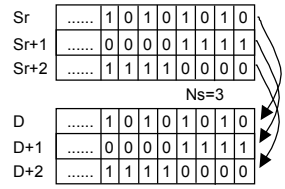
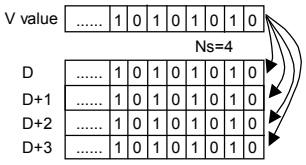
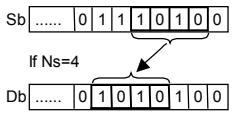
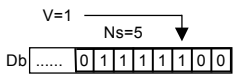
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Bit Conversion Instructions

Mnemonic	Command	Byte	Word	Description
BSET	Bit Set		———	Set Nth bit of D to 1. 
BRST	Bit Reset		———	Reset Nth bit of D to 0. 
BNOT	Bit Not		———	Reverse state of Nth bit of D. 
BTST	Bit Test		———	Set carry bit F1.8 to the state of the Nth bit of D. 
SUM	Sum		———	Store the number of bits in S that are 1 in D. 
SC	Set Carry		———	Set carry bit (F1.8) to 1. 
RC	Reset Carry		———	Reset carry bit (F1.8) to 0. 
CC	Complement Carry		———	Reverse carry bit (F1.8). 

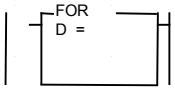
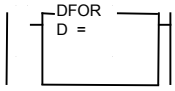
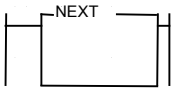
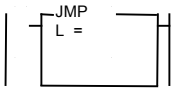
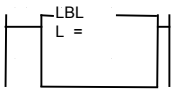
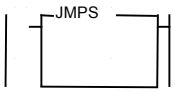
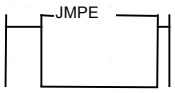
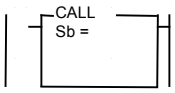
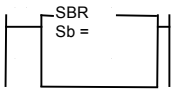
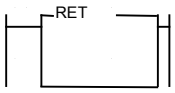
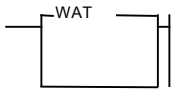
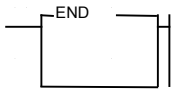
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Transfer Instructions

Mnemonic	Command	Byte	Word	Description
LDR (DLDR)	Load D←(Sr)	LDR D = Sr =	DLDR D = Sr =	Store value at absolute address Sr in D. 
STO (DSTO)	Store (D)←Sr	STO Sr = D =	DSTO Sr = D =	Store Sr in register at absolute address D. 
MOV	Move	MOV D = Sr = Ns =		Copy Ns words from Sr to D. 
FMOV	Fill Move	FMOV D = Ns = V =		Repeatedly copy the value V, Ns times to words starting at D. 
BMOV	Bit Move	BMOV Db = Sb = Ns =		Move Ns bits from bit address Sb to bit address Db. 
BFMV	Bit Fill Move	BFMV Db = Ns = V =		Repeatedly copy the bit value V, N times to bit address Db. (V = 0,1) (Ns = 0, 1,…, 15). 

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Block Processing Instructions

Mnemonic	Command	Byte	Word	Description
FOR (DFOR)	For Loop			Begin execution of instructions between FOR and corresponding NEXT. Repeat execution D times.
NEXT	Next		———	Decrease D of FOR instruction by 1. If not zero, repeat from FOR Instruction.
JMP	Jump		———	Jump to LBL instruction L. (L = 0 to 63)
LBL	Label		———	Position jumped to by JMP instruction. (L = 0 to 63)
JMPS	Jump Start		———	Jump to JMPE instruction.
JMPE	Jump End		———	Position jumped to by JMPS instruction.
CALL	Call Subroutine		———	Call subroutine Sb. (Sb = 0 to 31)
SBR	Subroutine Start		———	Start subroutine. (Sb = 0 to 31)
RET	Subroutine Return		———	End subroutine. Returns execution to instruction after CALL.
WAT	Watchdog Timer		———	Clear watchdog elapsed value.
END	END		———	End program. This instruction is automatically added by GPC.

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How to Read the Description of Instructions

Each instruction is explained in three parts: the instruction itself, its ladder diagram, and a description. This section explains how to read the instructions.

Sample Instruction

Mnemonic	Substitution Formula (Assignment expression)	Range
LET DLET	Direct substitution of number (direct output of number)	☐ Bit
		■ Byte
		■ Word

Explanation of Codes

☐ = unavailable option

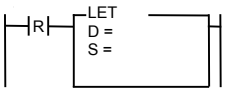
■ = available option

$xx indicates a hexadecimal number.

Explanation of Table

- Mnemonic—A byte (single mode) instruction, D designates word (double mode) instruction.
- Assignment expression—Description of the instruction.
- Range—Size of data that can be used by this instruction.

Sample Ladder



D: Destination

S: Source

Example: S = M0, and M0 is 123

D = R17, and R17 is 45

Before execution: M0 = 123, R17 = 45

After execution: M0 = 123, R17 = 123

Explanation of Ladder

The ladder diagram shows the structure of the instruction as it is displayed. Additional text typically gives an example and explains the processing structure.

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Sample Description

Range: LET: 0 to 255
DLET: 0 to 65,535

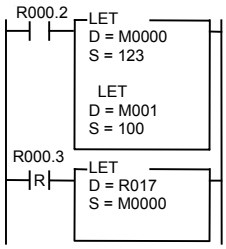
1. Either a register (R, M, K, L, or W) address or a constant number can be assigned for S.
2. When S is a register address, copy the data of the register to D.
3. When S is a constant number, copy the value to D.
4. This operation occurs on every scan for which the input condition to the instruction is true.

Explanation of Description

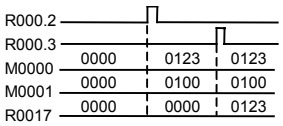
The description provides details of the instruction.

Sample Example

Program Expression



Time Chart



Explanation of Example

The example shows an application of an instruction as programmed in GPC. The time chart demonstrates how the instruction operates with respect to time and the changing input conditions for the example. The results of the operation may also be shown as part of the example.

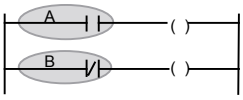
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Basic Instruction Details

Instruction

Mnemonic	Start of the Circuit	Range
STR	Start rung with NO contact	■ Bit
STN	Start rung with NC contact	☐ Byte
		☐ Word

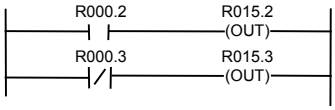
Ladder



Used for the start of a circuit.
STR: Start NO (normally open) contact
STN: Start NC (normally closed) contact (STR NOT)
A: Circuit started with NO contact→STR
B: Circuit started with NC contact→STN

Description

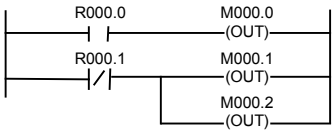
1. Every rung in the ladder program begins with either a STR or STN.
2. Every rung will contain one or more contacts.
3. Every rung will end in one or more output coils or application instructions.
4. When programming a ladder with NO and NC contacts, GPC will automatically use the proper contact instruction (STR, STN, AND, ANN, OR, ORN).



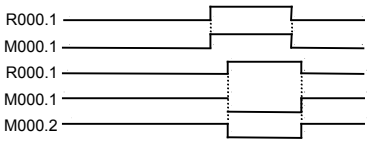
Start of circuit: R000.2, R000.3
End of circuit: R015.2, R015.3

Example

Program Expression



Time Chart



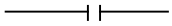
M000.0 has the same logic as R000.0
M000.1, M000.2 have the opposite logic as R000.1

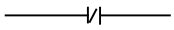
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Instruction

Mnemonic	Series Connection	Range
AND ANN (ADN)	Series connection	■ Bit ☐ Byte ☐ Word

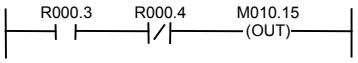
Ladder


AND: NO (normally open) contact series connection.


ANN: NC (normally closed) contact series connection.

Description

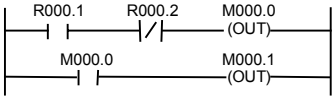
1. AND and ADN (AND NOT) indicate a series connection of each contact.
2. The number of ANDs and ADNs used within one branch (rung) is unlimited.



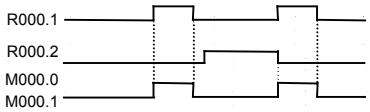
3. M010.15 is On only when contact R000.3 is On and contact R000.4 is Off. M010.15 is Off for all other cases.

Example

Program Expression



Time Chart



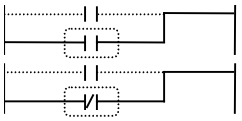
Contact M000.0 is On only when R000.1 is On and R000.2 is Off. M000.0 is Off for all other cases.

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Instruction

Mnemonic	Parallel Circuit	Range
OR ORN	Parallel connection	■ Bit ☐ Byte ☐ Word

Ladder

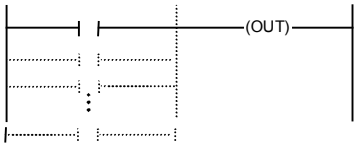


← OR: NO (normally open) contact parallel connection.

← ORN: NC (normally closed) contact parallel connection.

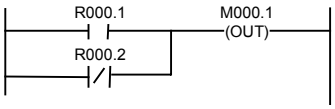
Description

1. OR and ORN (OR NOT) indicate parallel connection of each contact.
2. The number of ORs and ORNs used within a branch is unlimited.

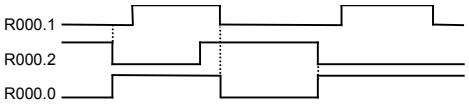


Example

Program Expression



Time Chart



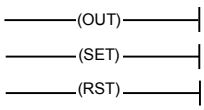
Contact M000.1 is On if contact R000.1 is On or contact R000.2 is Off.

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Instruction

Mnemonic	Output	Range
OUT	Relay output	■ Bit
SET	On output	☐ Byte
RST	Off output	☐ Word

Ladder



OUT: Relay coil turns On or Off based on the state of the input conditions.

SET: Relay coil turns On when the input conditions are true.

RST: Relay coil turns Off when the input conditions are true.

Description

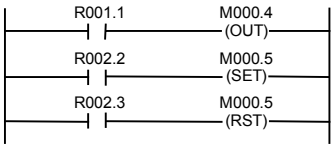
For an OUT instruction, you cannot use the same address twice.

OUT, SET, and RST instructions must be connected to the right bus and not in the middle of the circuit.

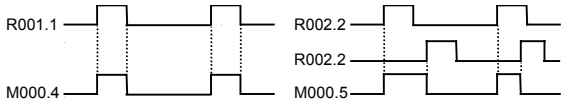
1. OUT—Use for external I/O (R), internal (M), and retentive (K) contacts. On or Off according to status of the input condition.
2. SET—Use for external I/O (R), internal (M), and retentive (K) contacts. The same address can be used more than once. When the input conditions are true, the coil is turned On and stays on unless turned off by a RST. The output is turned Off in the Stop mode.
3. RST—Use for external I/O (R), internal (M), and retentive (K) contacts. The same address can be used more than once. When the input conditions are true, the coil is turned Off and stays off unless turned on by a SET. The output is Off in the Stop mode.
4. When using retentive coils (K) in OUT, SET, or RST, the state is maintained. It will remain On or Off even after placed in the Stop mode and power is turned off.

Example

Program Expression



Time Chart



M000.4 follows contact logic for R001.1 input.

When R002.2 contact is On, M000.5 output is On.

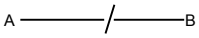
When R002.3 contact is On, M000.5 output is Off.

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Instruction

Mnemonic	Reverse	Range
NOT	Reverse the previous status of the logic.	■ Bit
		☐ Byte
		☐ Word

Ladder



Reverse the logic result of the input conditions before A at B.

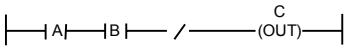
Reverse the previous On/Off state and transfer to the next input.

The results of the NOT execution:

Before	After
A (On)→	B (Off)
A (Off)→	B (On)

Description

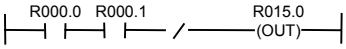
1. The instruction cannot be connected directly to the bus—it must come after a contact or set of contacts.
2. The instruction directly inverts the result of the input conditions before it. The instruction can be used for verification of the circuit or in the test stage.



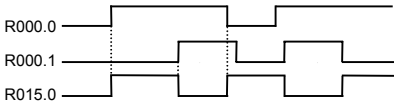
A	B	C
On	On	Off
Off	On	On
On	Off	On
Off	Off	On

Example

Program Expression



Time Chart

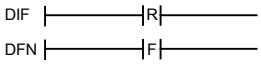


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Instruction

Mnemonic	Edge Contact	Range
STR DIF STR DFN AND DIF AND DFN OR DIF OR DFN	Contact which is On for one scan at the up or down point of contact	■ Bit ☐ Byte ☐ Word

Ladder



DIF: On at the rising edge (⊥↑) (Off→On) for one scan.

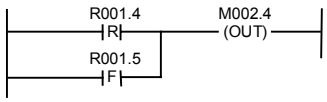
DFN: On at the falling edge (⊤↓) (On→Off) for one scan.

Description

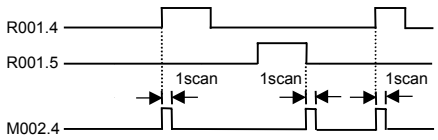
1. The DIF and DFN instructions may be used more than once in the ladder program for any of the bit addresses (R, L, M, K, F, and TC).
2. The DIF instruction is a contact which is On for the first scan after the signal has changed from Off→On. The contact is Off for all other scans, when the signal has not changed from Off or On.
3. The DFN instruction is a contact which is On for the first scan after the signal has changed from On→Off. The contact is Off for all other scans, when the signal has not changed from Off or On.
4. Both DIF and DFN can be used on the same bit address in a single scan.

Example

Program Expression



Time Chart



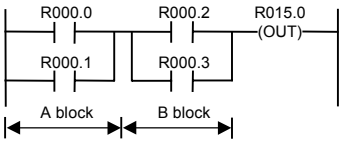
Contact M002.4 is On if contact R001.4 changes from Off→On or contact R001.5 changes from On→Off.

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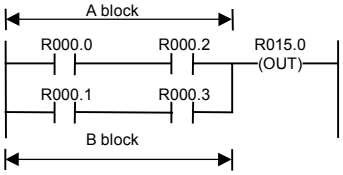
Instruction

Mnemonic	Block Circuit	Range
ANB ORB	Connect circuit by block	■ Bit ☐ Byte ☐ Word

Ladder



ANB: block in series



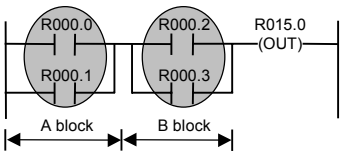
ORB: block in parallel

Description

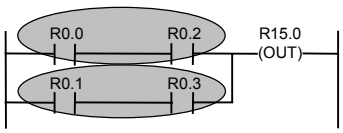
1. Block in series:
   - Series connection of more than two contacts.
   - Starts with STR or STN.
   - Ends with ANB.
2. Block in parallel:
   - Parallel connection of more than two contacts.
   - Starts with STR or STN.
   - Ends with ORB.
3. When programming in ladder, GPC will automatically add the proper ANB and ORB instructions as required by the contact connections.

Example

Program Expression (ANB)



Program Expression (ORB)

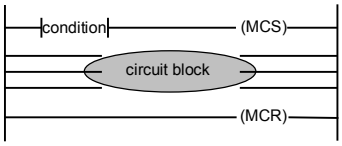


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Instruction

Mnemonic	Master Control Set (Reset)	Range
MCS MCR	Execute block circuit using the specified conditions.	☐ Bit ☐ Byte ☐ Word

Ladder

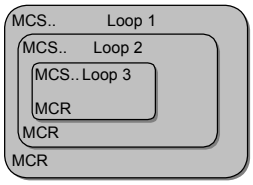


MCS: Enable processing of the following block of instructions.

MCR: End block of instructions enabled by MCS.

Description

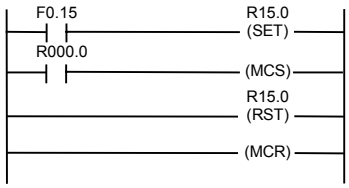
1. MCS (Master Control Set)—Marks the start of a conditional block of instructions. When the input conditions to the MCS are false, the block of instructions that follow are executed as false. Must be used with MCR.
2. MCR (Master Control Reset)—Marks the end of a conditional block of instructions. Must be used with MCS.
3. Up to seven MCS/MCR blocks can be nested.



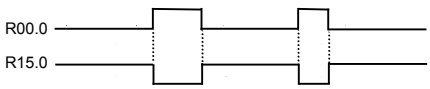
4. If you use eight or more MCS/MCR nested blocks, a syntax error will occur.

Example

Program Expression



Time Chart



The circuit block R15.0 bit is reset (0) by R000.0.

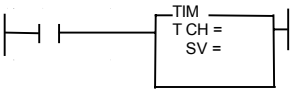
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Timer/Counter Instruction Details

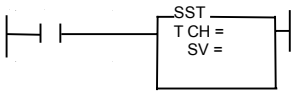
Instruction

Mnemonic	Timer	Range
TIM	On delay timer	■ Bit
SST	Single shot timer	☐ Byte
		☐ Word

Ladder



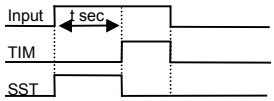
In t seconds (t = SV × time base) after the input is On, the output is On.
If the input is Off, the output is Off.
Valid channel numbers: Ch 0 through Ch 255 (256 channels)
Done contact: TC + channel number
SV set range: 0 to 65,535



For t seconds (t = SV × time base) after input is On, the output is On. At the end of t seconds, the output is Off.
If the input is Off, the output is Off.
Valid channel numbers: Ch 0 through Ch 255 (256 channels)
Done contact: TC + channel number

Description

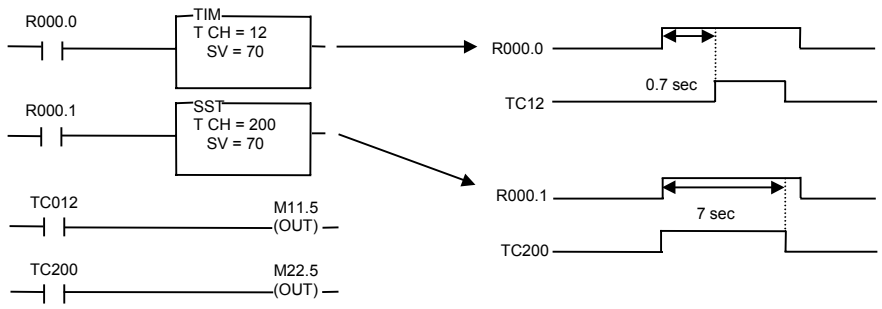
1. Ch 0 to Ch 15: Time base = 0.01 sec (10 msec)
   Ch 16 to Ch 255: Time base = 0.1 sec (100 msec)



2. The output done contact of the timer is TC + channel number.
3. The channel number can only be used once. It cannot be reused by other timer or counter instructions (UC, DC , UDC).
4. To change the Set Value or Present Value of the timer while the program is running, modify registers W2048 to W2559. In GPC, you may also reference these registers using the PV or SV designation.
5. The Present Value (PV) is reset to zero when the input is Off, in Stop mode, or when power is off.

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Example

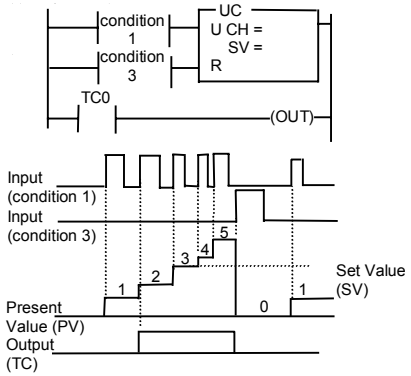


Program Expression **Time Chart**

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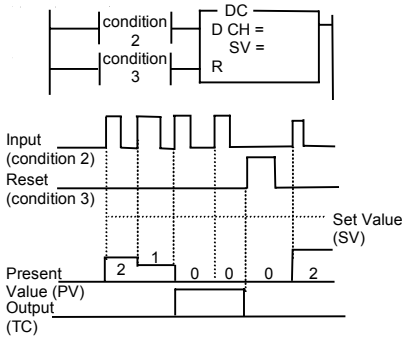
Instruction

Mnemonic	Timer (I)	Range
UC	Up counter	■ Bit
DC	Down counter	☐ Byte
		☐ Word



Example of UC with SV = 3.

- Whenever count input condition (U input) turns On, PV increases by 1. When PV and SV are the same, the output TC done contact is On. When the reset input condition (R input) is On, the output contact is Off.
- While the count input pulses On, the PV will continue to count up to a maximum of 65,535. When the reset input is On, the PV is reset to a value of 0.



Example of DC with SV = 3.

- Whenever count input condition (D input) turns On, PV decreases by 1. When PV is 0, the output TC done contact is On.
- When the reset input condition (R input) is turned On, the TC done contact is turned Off, and the PV is set to 0.

Description

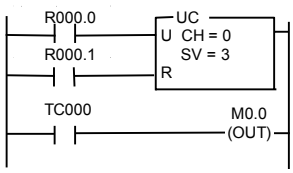
1. The timer/counter channel can only be used once. It cannot be reused by other timer or counter instructions (TIM, SST , UDC). A maximum of 256 channels (Ch 0 to Ch 255) can be used.
2. The output done contact is displayed as TC + channel no. in the counter.
3. The elapsed value (PV) of the counter is maintained in case of a power failure and for retentive purposes.
4. When SV is 0, the output contact (TC) turns On if one pulse of input occurs.
5. SV can be specified from 0 to 65,535.

⚠ CAUTION: Each input condition to the counter should be on its own line of the rung. They should not share a common contact or be connected in any way.

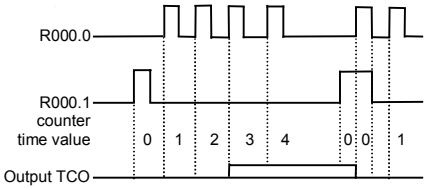
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Example

Program Expression



Time Chart

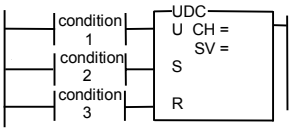


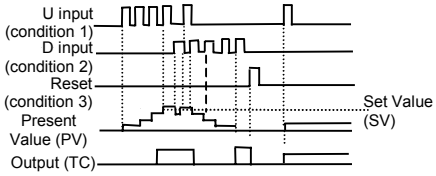
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Instruction

Mnemonic	Up/Down Counter	Range
UDC	Up/Down counter	■ Bit
		☐ Byte
		☐ Word

Ladder





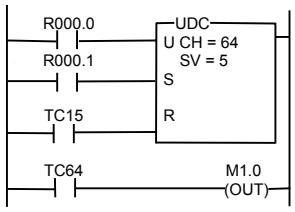
Description

1. When the up count input (U input) turns On, the Present Value (PV) increases by 1. When the down count input (D input) turns On, PV decreases by 1. When PV is greater than or equal to the Set Value (SV) or is reduced to 0, the output done contact turns On.
2. In the following cases, the output done contact changes from On to Off:
   - When the reset input is turned On.
   - When the PV is decreased below the SV by the down count pulse input.
   - When the PV increases from 0 to 1 by the up count pulse input.
3. If the reset input (R input) is On, the output is Off. In this state, the up/down counter input pulses are ignored and the Present Value stays reset to 0.
4. When the up count input pulse and the down count input pulse occur at the same time, the PV does not change.
5. When the PV is 0, if the down count pulse is input, the Present Value does not change, and the output is On. When the Present Value is 65,535, if the up-counter pulse is input, the Present Value is reset to 0.
6. When the counter Set Value is 0, if the reset input is On then the output is Off. If up or down is input while the reset input is Off, the output changes to On.
7. The timer/counter channel can only be used once. It cannot be reused by other timer or counter instructions (TIM, SST, UC, DC). The number of channels available is 256 (Ch 0 through Ch 255).
8. The SV can be set to a maximum value of 65,535.

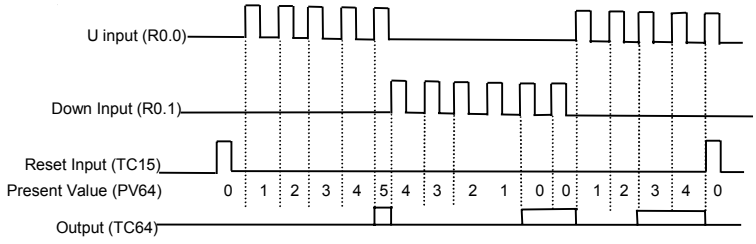
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Example

Program Expression



Time Chart



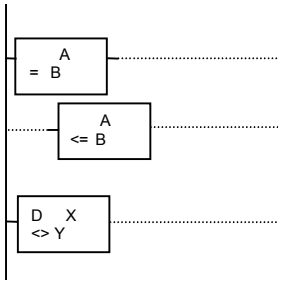
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Comparison Instruction Details

Instruction

Mnemonic	Comparing the Value	Range
=	A = B (A is equal to B)	☐ Bit
<>	A <> B (A is not equal to B)	
>	A > B (A is greater than B)	■ Byte
>=	A >= B (A is greater than or equal to B)	
<=	A <= B (A is less than or equal to B)	■ Word
<	A < B (A is less than B)	

Ladder



A or B: Constant value 0 to 65,535 or a word address (R, L, M, K, W, PV, SV, SR).

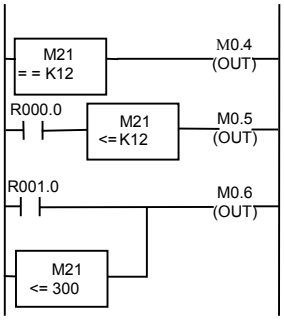
D is displayed when words are input. When using GPC5 to program, change the mode to double (Ctrl+T) and then enter the comparison command.

Description

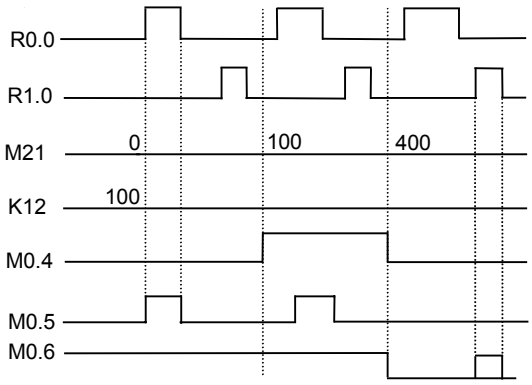
1. The comparison functions as a contact, whose On/Off state is determined by the result of the comparison of A and B. If the comparison is true, the state is On.
2. Each comparison instruction can be used with the STR, AND, and OR instructions (GPC will automatically use the correct instruction).
3. Double mode comparison instructions can process up to 16 bits of data (0 to 65,535).

Example

Program Expression



Time Chart



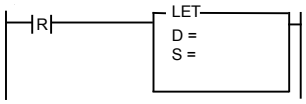
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Substitution, Increment/Decrement Instruction Details

Instruction

Mnemonic	Substitution Formula	Range
LET DLET	Direct substitution of number (direct output of number)	☐ Bit ■ Byte ■ Word

Ladder



D: Destination

S: Source

Example: S = M0, and M0 is 123
D = R17, and R17 is 45

Before execution: M0 = 123, R17 = 45

After execution: M0 = 123, R17 = 123

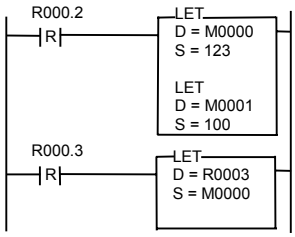
Description

Range: LET: 0 to 255
DLET: 0 to 65,535

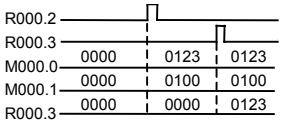
1. Either a register (R, M, K, L, or W) address or a constant number can be assigned for S.
2. When S is a register address, copy the data of the register to D.
3. When S is a constant number, copy the value to D.
4. This operation occurs on every scan for which the input condition to the instruction is true.

Example

Program Expression



Time Chart

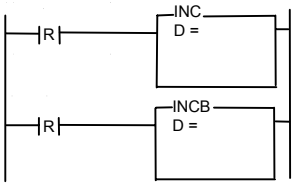


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Instruction

Mnemonic	Increment	Range
INC DINC INCB DINCB	Increment (INC, DINC) BCD increment (INCB, DINCB)	☐ Bit ■ Byte ■ Word

Ladder



D = D + 1: Decimal number increment

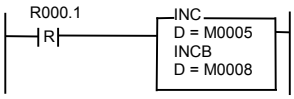
D = D + 1: BCD increment

Description

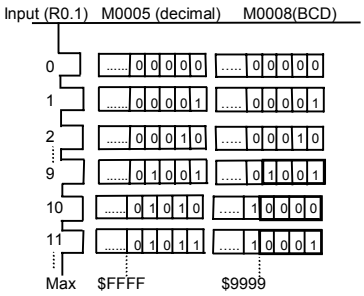
1. INC and DINC increase D in decimal by 1 when the input is On.
2. INCB and DINCB increase D in BCD (Binary Coded Decimal) by 1.
3. INC and INCB are byte instructions for processing 8 bit data.
4. DINC and DINCB are word instructions for processing 16 bit data.

Example

Program Expression



Time Chart

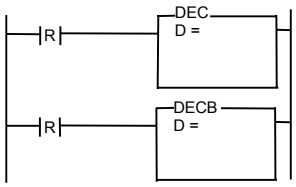


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Instruction

Mnemonic	Decrement	Range
DEC DDEC DECB DDECB	Decrement (DEC, DDEC) BCD decrement (DECB, DDECB)	☐ Bit ■ Byte ■ Word

Ladder



D = D - 1: Decimal decrement

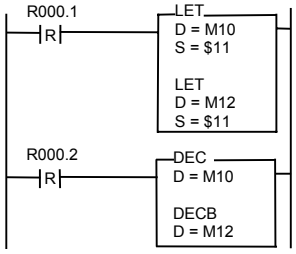
D = D - 1: BCD decrement

Description

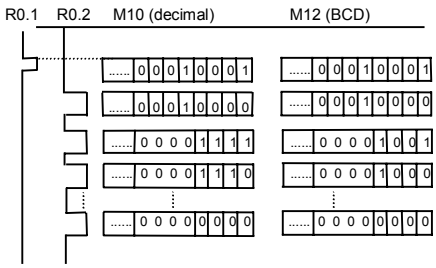
1. DEC and DDEC decrease D by 1 down to 0 when the input is On.
2. DECB and DDECB decrease D by 1 in BCD to 0 when the input is On.
3. Byte instructions (DEC, DECB) process 8 bit data, word instructions(DDEC, DDECB) process 16 bit data.

Example

Program Expression



Time Chart



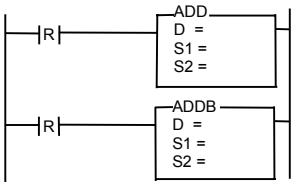
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Arithmetic Instruction Details

Instruction

Mnemonic	Addition	Range
ADD	Decimal addition (ADD, DADD)	☐ Bit
DADD	BCD addition (ADDB, DADDB)	■ Byte
ADDB		■ Word
DADDB		

Ladder



D = S1 + S2

Decimal: S1 = 21, and S2 = 22

Hexadecimal: S1 = $15 and S2 = $16

ADD Example:

Decimal: 21 + 22 = 43

ADDB Example:

BCD: $15 + $16 = $31

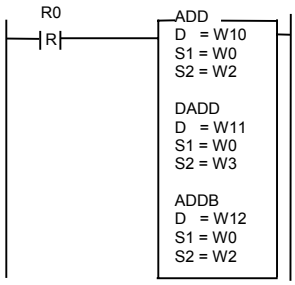
Description

1. Add the data in the S1 and S2 addresses, then store the result in the D register.
2. When using ADD and ADDB, the calculation ranges are as follows:
   - S1: 0 to 255 (0 to $FF)
   - S2: 0 to 255 (0 to $FF)
   - D: 0 to 255 (0 to $FF)
3. When using DADD and DADDB, the calculation ranges are as follows:
   - S1: 0 to 65,535 (0 to $FFFF)
   - S2: 0 to 65,535 (0 to $FFFF)
   - D: 0 to 65,535 (0 to $FFFF)
4. If the result exceeds the range of calculation, a carry occurs. The carry flag (F1.8) is changed to On.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

Initial conditions: W0 = 00017 = $0011
W1 = 00001 = $0001
W2 = 00025 = $0019
W3 = 00250 = $00FA

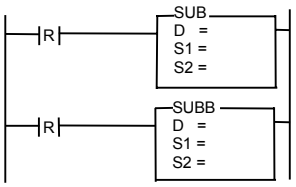
Operation results: W10 = 00042 = $002A
W11 = 00267 = $010B
W12 = 00048 = $0030

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Instruction

Mnemonic	Subtraction	Range
SUB	Decimal subtraction (SUB, DSUB)	☐ Bit
DSUB	BCD subtraction (SUBB, DSUBB)	■ Byte
SUBB		■ Word
DSUBB		

Ladder



D = S1 - S2

Decimal: S1 = 34 and S2 = 19
Hexadecimal: S1 = $22 and S2 = $13

SUB Example:
Decimal: 34 - 19 = 15

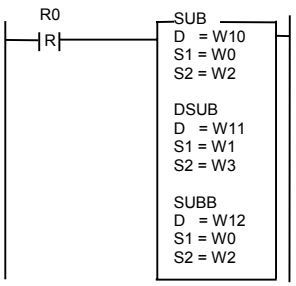
SUBB Example:
BCD: $22 - $13 = $09

Description

1. Subtract the data in S2 from S1, then store the result in the D register.
2. When using SUB and SUBB, the calculation ranges are as follows:
   - S1: 0 to 255 (0 to $FF)
   - S2: 0 to 255 (0 to $FF)
   - D: 0 to 255 (0 to $FF)
3. When using DSUB and DSUBB, the calculation ranges are as follows:
   - S1: 0 to 65,535 (0 to $FFFF)
   - S2: 0 to 65,535 (0 to $FFFF)
   - D: 0 to 65,535 (0 to $FFFF)
4. If the result exceeds the range of calculation, a carry occurs. The carry flag (F1.8) is changed to On.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = 00016 = $0010
W1 = 00520 = $0208
W2 = 00007 = $0007
W3 = 00384 = $0180

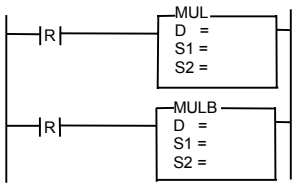
Operation results: W10 = 00009 = $0009
W11 = 00136 = $0088
W12 = 00003 = $0003

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Instruction

Mnemonic	Multiplication	Range
MUL DMUL MULB DMULB	Decimal multiplication (MUL, DMUL) BCD multiplication (MULB, DMULB)	☐ Bit ■ Byte ■ Word

Ladder



D = S1 × S2
Decimal: S1 = 3 and S2 = 7
Hexadecimal: S1 = $03 and S2 = $07

MUL Example:
Decimal: 3 × 7 = 21

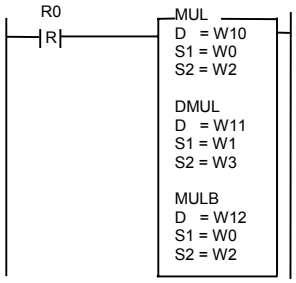
MULB Example:
BCD: $03 × $07 = $21

Description

1. Multiply the data in the S1 and S2 addresses, then store the result in the D register.
2. When using MUL and MULB, the calculation ranges are as follows:
   - S1: 0 to 255 (0 to $FF)
   - S2: 0 to 255 (0 to $FF)
   - D: 0 to 255 (0 to $FF)
3. When using DMUL and DMULB, the calculation ranges are as follows:
   - S1: 0 to 65,535 (0 to $FFFF)
   - S2: 0 to 65,535 (0 to $FFFF)
   - D: 0 to 65,535 (0 to $FFFF)
4. If the result exceeds the range of calculation, a carry occurs. The carry flag (F1.8) is changed to On. The high word of the result that exceeds the range of D is automatically stored in SR20.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = 00002 = $0002
W1 = 00030 = $001D
W2 = 00006 = $0006
W3 = 00500 = $01E4

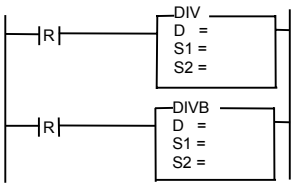
Operation results: W10 = 00012 = $000C
W11 = 15000 = $3A98
W12 = 00018 = $0012

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Instruction

Mnemonic	Division	Range
DIV	Decimal division (DIV, DDIV)	☐ Bit
DDIV	BCD division (DIVB, DDIVB)	■ Byte
DIVB		■ Word
DDIVB		

Ladder



D = S1 ÷ S2

Decimal: S1 = 18 and S2 = 3
Hexadecimal: S1 = $12 and S2 = $03

DIV Example:
Decimal: 18 ÷ 3 = 6

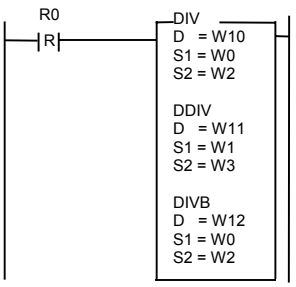
DIVB Example:
BCD: $12 ÷ $03 = $04

Description

1. Divide the data in S1 by S2, then store the result in the D register.
2. When using DIV and DIVB, the calculation ranges are as follows:
   - S1: 0 to 255 (0 to $FF)
   - S2: 0 to 255 (0 to $FF)
   - D: 0 to 255 (0 to $FF)
3. When using DDIV and DDIVB, the calculation ranges are as follows:
   - S1: 0 to 65,535 (0 to $FFFF)
   - S2: 0 to 65,535 (0 to $FFFF)
   - D: 0 to 65,535 (0 to $FFFF)
4. The quotient is stored in the D register, and the remainder in special register SR22.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = 00024 = $0018
W1 = 01024 = $0400
W2 = 00004 = $0004
W3 = 00128 = $0080

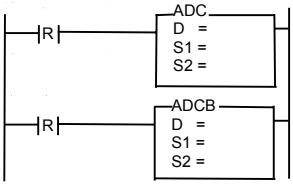
Operation results: W10 = 00006 = $0006
W11 = 00008 = $0008
W12 = 00004 = $0004

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Instruction

Command	Addition with Carry	Range
ADC DADC ADCB DADCB	Decimal addition with carry (ADC, DADC) BCD addition with carry (ADCB, DADCB)	☐ Bit ■ Byte ■ Word

Ladder



D = S1 + S2 + carry

Decimal: S1 = 21, and S2 = 22
Hexadecimal: S1 = $15 and S2 = $16
Carry Flag: F1.8 = On

ADC Example:

Decimal: 21 + 22 + 1 = 44

ADCB Example:

BCD: $15 + $16 + $1 = $32

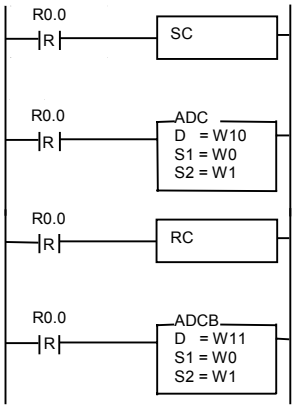
Description

1. Add the data in the S1 and S2 addresses. If the carry flag F1.8 is On, add 1, otherwise add 0. Then store the result in the D register.
2. When using ADC and ADCB, the calculation ranges are as follows:
   - S1: 0 to 255 (0 to $FF)
   - S2: 0 to 255 (0 to $FF)
   - D: 0 to 255 (0 to $FF)
3. When using DADD and DADDB, the calculation ranges are as follows:
   - S1: 0 to 65,535 (0 to $FFFF)
   - S2: 0 to 65,535 (0 to $FFFF)
   - D: 0 to 65,535 (0 to $FFFF)
4. If the result exceeds the range of calculation, a carry occurs. The carry flag (F1.8) is changed to On.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

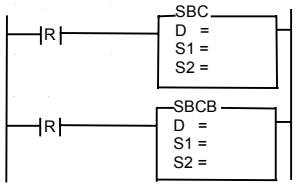
Initial conditions: W0 = 00017 = $0011
W1 = 00025 = $0019
Operation results: W10 = 00017 + 00025 +1 = 00043
W11 = $0011 + $0019 + 0 = $0030

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Instruction

Command	Subtraction with Carry	Range
SBC DSBC SBCB DSBCB	Decimal subtraction with carry (SBC, DSBC) BCD subtraction with carry (SBCB, DSBCB)	☐ Bit ■ Byte ■ Word

Ladder



D = S1 - S2 - carry

Decimal: S1 = 34 and S2 = 19
Hexadecimal: S1 = $22 and S2 = $13
Carry Flag: F1.8 = On

SBC Example:
Decimal: 34 - 19 - 1 = 14

SBCB Example:
BCD: $22 - $13 - $01 = $08

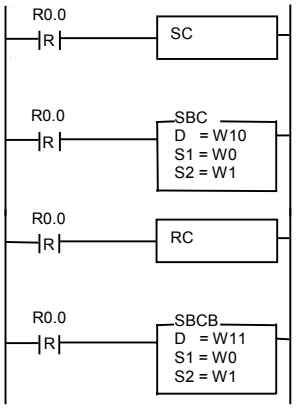
Description

1. Subtract the data in S2 from S1. If the carry flag F1.8 is On, subtract 1. Then store the result in the D register.
2. When using SBC and SBCB, the calculation ranges are as follows:
   - S1: 0 to 255 (0 to $FF)
   - S2: 0 to 255 (0 to $FF)
   - D: 0 to 255 (0 to $FF)
3. When using DSBC and DSBCB, the calculation ranges are as follows:
   - S1: 0 to 65,535 (0 to $FFFF)
   - S2: 0 to 65,535 (0 to $FFFF)
   - D: 0 to 65,535 (0 to $FFFF)
4. If the result exceeds the range of calculation, a carry occurs. The carry flag (F1.8) is changed to On.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

Initial conditions: W0 = 00016 = $0010
W1 = 00002 = $0002

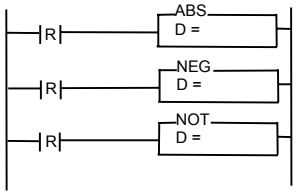
Operation results: W10 = 00016 - 00002 - 1 = 00013
W11 = $0010 - $0002 - 0 = $0008

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Instruction

Mnemonic	Absolute Value, NEG and NOT	Range
ABS	ABS: Absolute value	☐ Bit
DABS	NEG: 2's complement	■ Byte
NEG	NOT: 1's complement	■ Word
DNEG		
NOT		
DNOT		

Ladder



ABS: Take the absolute value of D, and store it in D.

NEG: Take the 2's complement and store it in D.

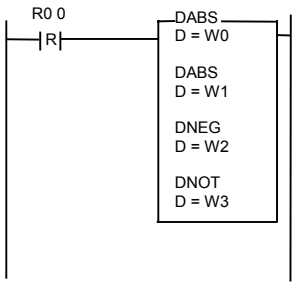
NOT: Take the 1's complement and store it in D.

Description

1. For the ABS (absolute value) instruction, if the highest bit (MSB) is 1, take the 2's complement. If the highest bit is 0, leave it as it is.
   - For example, the absolute value of $9A52 (=1001 1010 0101 0010) is $65AE (=0110 0101 1010 1110). The absolute value of $7A52 (=0111 1010 0101 0010) is $7A52.
2. The NEG (2's complement) instruction is expressed as the 1's complement + 1.
   - For example, DNEG of $7A52 (=0111 1010 0101 0010) is $85AE (=1000 0101 1010 1110)
3. The NOT (1's complement) instruction is performed by reversing each bit.
   - For example, DNOT of $7A52 (=0111 1010 0101 0010) is $85AD (=1000 0101 1010 1101)
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $9A52
W1 = $7A52
W2 = $7A52
W3 = $7A52

Operation results: W0 = $65AE
W1 = $7A52
W2 = $85AE
W3 = $85AD

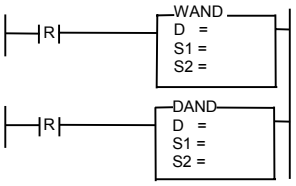
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Logic Instruction Details

Instruction

Mnemonic	Bit AND Operation	Range
WAND DAND	Bit AND operation	☐ Bit ■ Byte ■ Word

Ladder



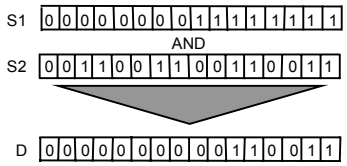
Process each bit of S1 and S2 in bit AND operation and store the result in D.

S1	S2	D
0	0	0
0	1	0
1	0	0
1	1	1

Description

1. Process the values of the S1 and S2 bits (byte/word) in bit AND operation and store the result in D.

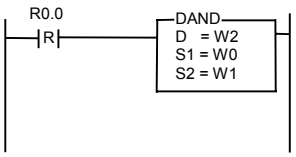
   For example: S1 = $00FF (hex)
   S2 = $3333 (hex)
   D = $0033 (hex)



2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $00FF
W1 = $3333
W2 = $XXXX

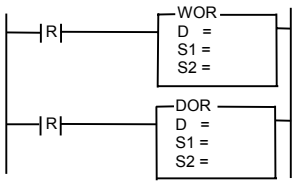
Operation results: W0 = $00FF
W1 = $3333
W2 = $0033

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Instruction

Mnemonic	Bit OR Operation	Range
WOR DOR	Bit OR operation	☐ Bit ■ Byte ■ Word

Ladder



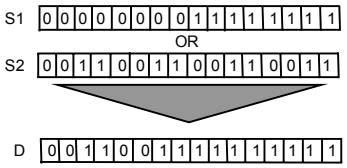
Process S1 and S2 in bit OR operation and store the result in D.

S1	S2	D
0	0	0
0	1	1
1	0	1
1	1	1

Description

1. Process S1 and S2 (byte/word) by bit OR operation and store the result in D.

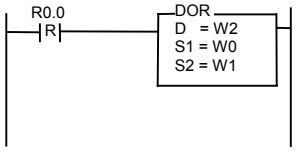
   For example: S1 = $00FF (hex)
   S2 = $3333 (hex)
   D = $33FF (hex)



2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $00FF
W1 = $3333
W2 = $XXXX

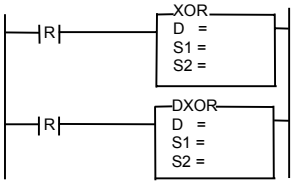
Operation results: W0 = $00FF
W1 = $3333
W2 = $33FF

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Instruction

Mnemonic	Bit Exclusive OR Operation	Range
XOR DXOR	Bit exclusive OR operation	☐ Bit ■ Byte ■ Word

Ladder



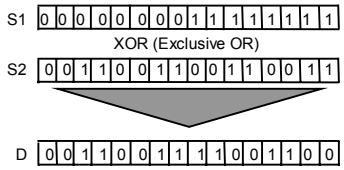
Process S1 and S2 in bit exclusive OR operation and store the result in D.

S1	S2	D
0	0	0
0	1	1
1	0	1
1	1	0

Description

1. Process S1 and S2 (byte/word) by bit exclusive OR operation and store the result in D.

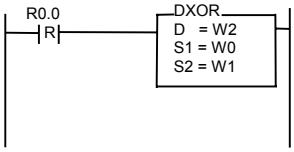
   For example: S1 = $00FF (hex)
   S2 = $3333 (hex)
   D = $33CC (hex)



2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $00FF
W1 = $3333
W2 = $XXXX

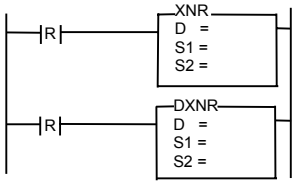
Operation results: W0 = $00FF
W1 = $3333
W2 = $33CC

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Instruction

Mnemonic	Bit Exclusive NOR Operation	Range
XNR DXNR	Bit exclusive OR NOT operation	☐ Bit ■ Byte ■ Word

Ladder



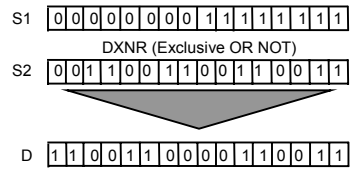
Process S1 and S2 in bit exclusive OR NOT operation and store the result in D.

S1	S2	D
0	0	1
0	1	0
1	0	0
1	1	1

Description

1. Process S1 and S2 (word/double word) by bit exclusive OR NOT operation and store the result in D.

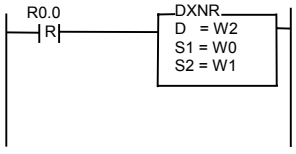
   For example: S1 = $00FF (hex)
   S2 = $3333 (hex)
   D = $CC33 (hex)



2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $00FF
W1 = $3333
W2 = $XXXX

Operation results: W0 = $00FF
W1 = $3333
W2 = $CC33

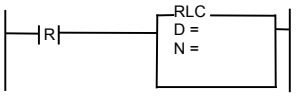
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Rotation Instruction Details

Instruction

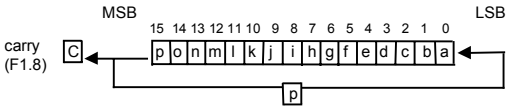
Mnemonic	Rotate to the Left Without Carry	Range
RLC DRLC	Rotate specified address to the left (low to high)	☐ Bit
		■ Byte
		■ Word

Ladder



D = Register address

N = Number of bits to rotate

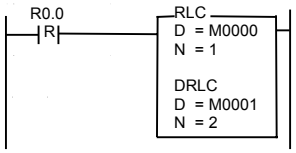


Description

1. Order:
   - Shift by N bits to the left (from low-order bit to high-order bit).
   - Fill the carry bit (F1.8) with the MSB (most significant bit).
   - Shift the MSB to the LSB (least significant bit).
2. Shift the register specified as D to the left by N bits. Each bit will move one bit position higher in the register.
3. The D register is either a byte or a word. For RLC (byte), N = 0 to 7. For DRLC (word), N = 0 to 15.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

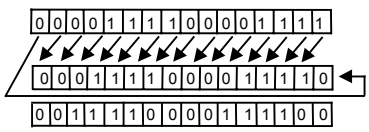
Program Expression



Operation Results

Initial condition: M0000 = $0F0F
M0001 = $0F0F

Operation results: M0000 = $0F1E
M0001 = $3C3C

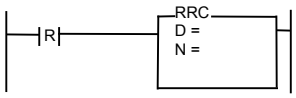


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Instruction

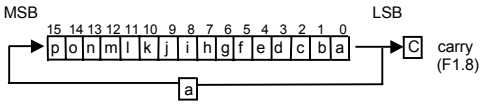
Mnemonic	Rotate to the Right Without Carry	Range
RRC DRRC	Rotate the specified address to the right (high to low)	☐ Bit ■ Byte ■ Word

Ladder



D = Register address

N = Number of bits to rotate

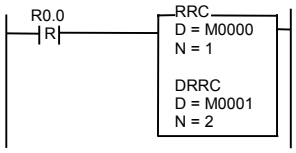


Description

1. Order:
   - Shift N bits to the right (from high-order bit to low-order bit).
   - Fill the carry bit (F1.8) with the LSB (least significant bit).
   - Shift the LSB to the MSB (most significant bit).
2. Shift the register specified as D to the right by N bits. Each bit will move one bit position lower in the register.
3. The D register is either a byte or a word. For RLC (byte), N = 0 to 7. For DRLC (word), N = 0 to 15.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

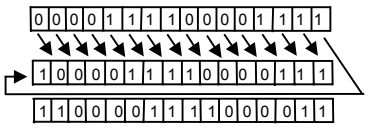
Program Expression



Operation Results

Initial condition: M0000 = $0F0F
M0001 = $0F0F

Operation results: M0000 = $0F87
M0001 = $C3C3

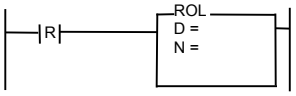


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Instruction

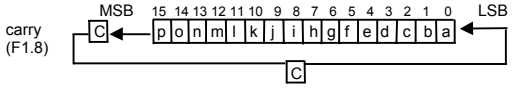
Mnemonic	Rotate to the Left	Range
ROL DROL	Rotate the specified address to the left with the carry flag	☐ Bit ■ Byte ■ Word

Ladder



D = Register address

N = Number of bits to rotate



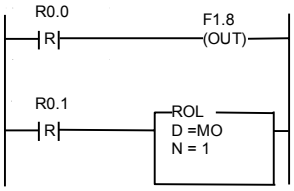
Description

1. Order:
   - Shift N bits to the left (from low-order bit to high-order bit) including the carry bit.
   - The MSB (most significant bit) moves to the carry bit (F1.8).
   - Input F1.8 (carry bit) in the LSB (least significant bit).
2. This instruction is different from the RLC instruction because it sends the MSB to the carry bit and the carry bit moves to the LSB. The input to the LSB can be changed by setting or clearing the carry bit.
3. The D register is either a byte or a word. For ROL (word), N = 0 to 7. For DROL (word), N = 0 to 15.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

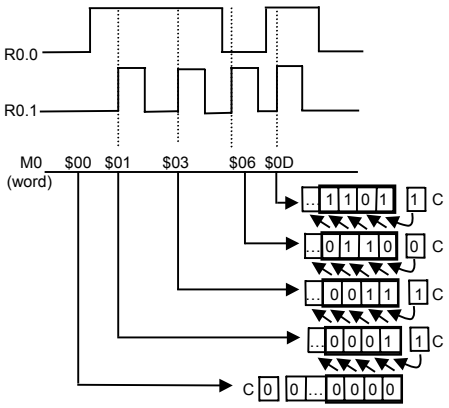
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Example

Program Expression



Operation Results



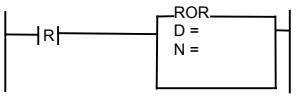
- If N = 1, the bits shift by one, and the LSB is always input from F1.8.
- If N = 2, the bits shift by two. The bits are shifted one position, and the first data input to the LSB is F1.8. The original MSB is stored in F1.8. The bits are again shifted one position, with the LSB being set by the new F1.8, and F1.8 being changed to the state of the last MSB.

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Instruction

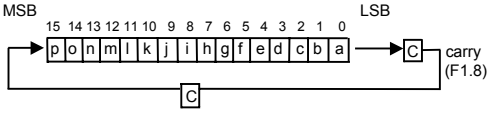
Mnemonic	Rotate to the Right	Range
ROR DROR	Rotate the specified address to the right with the carry flag	☐ Bit ■ Byte ■ Word

Ladder



D = Register address

N = Number of bits to rotate

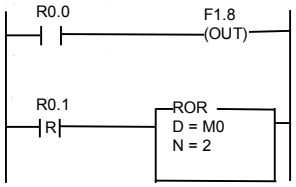


Description

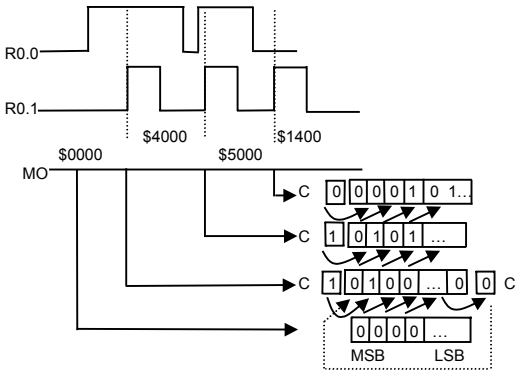
1. Order:
   - Shift N bits to the right (from high-order bit to low-order bit) including the carry bit.
   - Input the carry bit (F1.8) to the MSB (most significant bit).
   - The LSB (least significant bit) moves to the carry bit (F1.8).
2. This instruction is different from the RRC instruction because it sends the LSB to the carry bit, and the carry bit shifts to the MSB. The input to the MSB can be changed by setting or clearing the carry bit.
3. The D register is either a byte or a word. For ROR (byte), N = 0 to 7. For DROR (word), N = 0 to 15.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



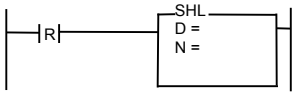
Operation Results



Instruction

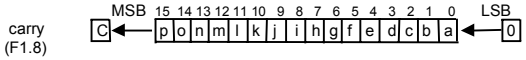
Mnemonic	Shift to Left	Range
SHL DSHL	Shift to left (high-order bit) by N bits Lowest bit becomes 0	■ Bit ☐ Byte ☐ Word

Ladder



D = Register address

N = Number of bits to rotate



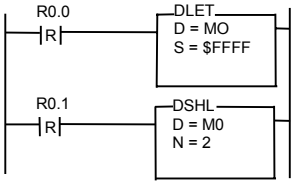
Description

1. Order:
   - Shift N bits to the left (from low-order bit to high-order bit) including the carry bit.
   - The MSB (most significant bit) moves to the carry bit (F1.8).
   - The LSB (least significant bit) becomes 0.
2. Shift the register specified as D to the left by N bits. Each bit will move one position higher in the register.
3. The D register is either a byte or a word. For SHL (byte), N = 0 to 7. For DSHL (word), N = 0 to 15.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

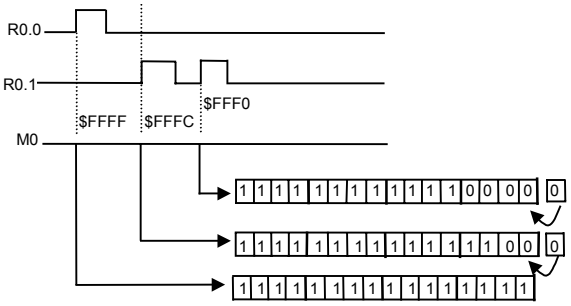
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Example

Program Expression



Operation Results



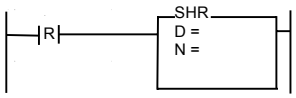
- Regardless of N, the MSB moves to the carry bit (F1.8) and the LSB always becomes 0.
- The R0.0 input is the initial condition, used to set the initial value of M0 to $FFFF.

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Instruction

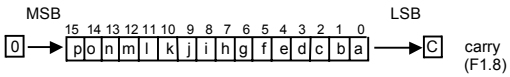
Mnemonic	Shift to Right	Range
SHR DSHR	Shift to right (low-order bit) by N bits The highest bit becomes 0	☐ Bit ■ Byte ■ Word

Ladder



D = Register address

N = Number of bits to rotate

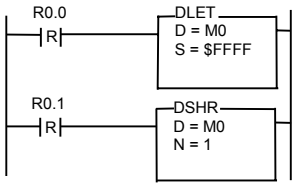


Description

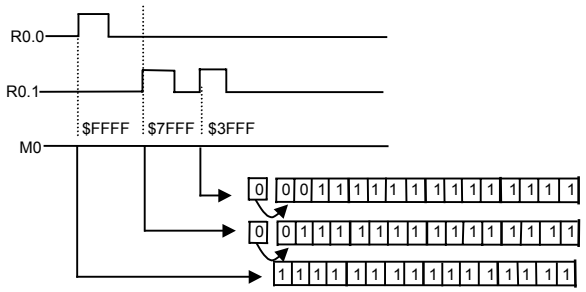
1. Order:
   - Shift N bits to the right (from high-order bit to low-order bit).
   - MSB (most significant bit) becomes 0.
   - Fill the carry bit (F1.8) with the LSB (least significant bit).
2. Shift the register specified as D to the right by N bits. Each bit will move one bit position lower in the register.
3. The D register is either a byte or a word. For SHR (byte), N = 0 to 7. For DSHR (word), N = 0 to 15.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Time Chart



- Regardless of N, the MSB moves to the carry (F1.8) and the LSB always becomes 0.
- The R0.0 input is the initial condition, used to set the initial value of M0 to $FFFF.

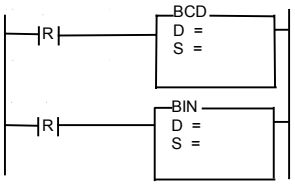
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Word Conversion Instruction Details

Instruction

Mnemonic	BCD Conversion, Binary Conversion	Range
BCD DBCD BIN DBIN	BCD: Convert binary to BCD BIN: Convert BCD to binary	☐ Bit ■ Byte ■ Word

Ladder



BCD: Convert the S value from binary into BCD and store in D.

BIN: Convert the S value from BCD into binary and store in D.

Description

1. BCD: Convert S, which is expressed in binary (byte /word), into BCD and store in D. The range is as follows:

   Byte conversion: S = 0 to $63 (hex) = 99 (decimal)
   D = 0 to $99 (hex) = 153 (decimal)

   Word conversion: S = 0 to $270F (hex) = 9999 (decimal)
   D = 0 to $9999 (hex) = 39321 (decimal)

2. BIN: Convert S, which is expressed in BCD (byte /word), into binary (binary code) and store in D. The range is as follows:

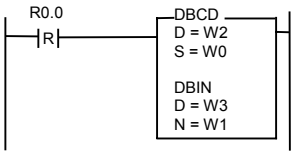
   Byte conversion: S = 0 to $99 (hex) = 153 (decimal)
   D = 0 to $63 (hex) = 99 (decimal)

   Word conversion: S = 0 to $9999 (hex) = 39321 (decimal)
   D = 0 to $270F = 9999 (decimal)

3. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $07CC = 1996 (decimal)
W1 = $1996 = 6550 (decimal)
W2 = $XXXX
W3 = $XXXX

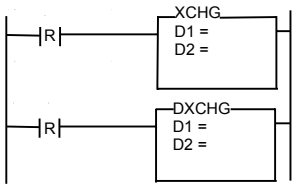
Operation results: W0 = $07CC
W1 = $1996
W2 = $1996 = 6550 (decimal)
W3 = $07CC = 1996 (decimal)

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Instruction

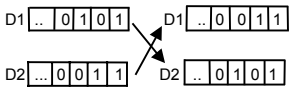
Mnemonic	Data Exchange	Range
XCHG DXCHG	Exchange registers of D1, D2 with each other	☐ Bit ■ Byte ■ Word

Ladder



Exchange registers D1 and D2 (byte /word) with each other.

D1 => D2, D2 => D1



Description

1. Exchange registers D1 and D2 with each other (byte/word). For example:

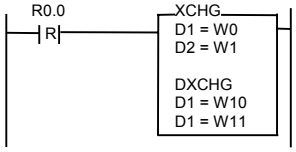
   Byte operation: D1 = $1234 (hex) D2 = $1278 (hex)
   D1 = $5678 (hex) D2 = $5634 (hex)

   Word operation: D1 = $1234 (hex) D2 = $5678 (hex)
   D1 = $5678 (hex) D2 = $1234 (hex)

2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $1234
W1 = $5678
W10 = $5678
W11 = $1234

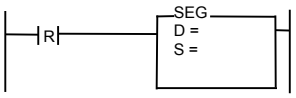
Operation results: W0 = $1278
W1 = $5634
W10 = $1234
W11 = $5678

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Instruction

Mnemonic	7-Segment Decoder	Range
SEG	Convert the low-order 4 bits of S into 7-segment display format and store in D	☐ Bit
		■ Byte
		☐ Word

Ladder

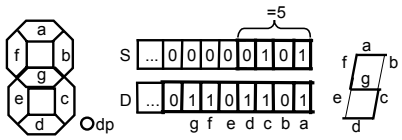


Convert the value in the low-order 4 bits of address S (0 to 15) into the proper format for display by a 7-segment display and store in D. In the converted format, if a bit is 1, the segment is illuminated (= active high output).

Description

1. Convert the value in the low-order 4 bits of address S into SEG display format, and store it in D. The high-order 8 bits of D do not change. The 8th bit of the D register, used with many 7-segment display cells as the decimal point, is not affected by this instruction.

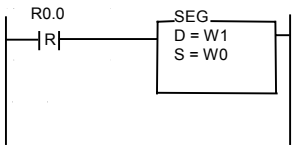
   For example: S = $XXX5 (hex)
   D = $XX6D (hex)



2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: W0 = $876**5** (hex)
W1 = $1234 (hex)

Operation results: W0 = $8765 (hex)
W1 = $12**6D** (hex)

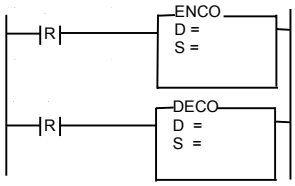
The 8th bit of W1 does not change.

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Instruction

Mnemonic	Decoder and Encoder with 8421	Range
ENCO	ENCO: 8421 encoder	☐ Bit
DECO	DECO: 8421 decoder	■ Byte
		☐ Word

Ladder

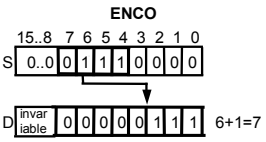


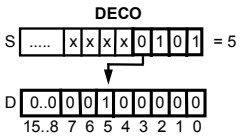
ENCO: Inspect the S register. If there is a bit in the On state, encode it (on bit n) and store it in the low-order 8 bits of D. If there are two or more bits in the S register that are in the On state, only the highest bit will be processed. The higher 8 bits of D do not change.

DECO: Interpret the lower 4 bits of the S register and store in D.

Description

1. ENCO: Set D to the value of the bit number of highest bit in S that is On (0 to 16). If there are two or more On bits in S, use the location of the highest bit. The high-order 8 bits of D do not change.
2. DECO: Set the bit location (0 to 15) in D pointed to by the value in the low 4 bits of S. All other bits in D are reset to 0.



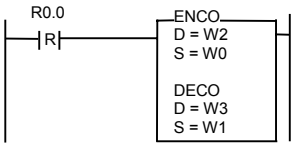


ENCO	$0000→$00	$0020→$06	$0800→$0C
	$0001→$01	$0040→$07	$1000→$0D
	$0002→$02	$0080→$08	$2000→$0E
	$0004→$03	$0100→$09	$4000→$0F
	$0008→$04	$0200→$0A	$8000→$10
	$0010→$05	$0400→$0B	
DECO	$0→$0001	$6→$0040	$C→$1000
	$1→$0002	$7→$0080	$D→$2000
	$2→$0004	$8→$0100	$E→$4000
	$3→$0008	$9→$0200	$F→$8000
	$4→$0010	$A→$0400	
	$5→$0020	$B→$0800	

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Example

Program Expression



Operation Results

Initial conditions: W0 = $**0070** (hex)
W1 = $123**5** (hex)
W2 = $5678 (hex)
W3 = $9ABC (hex)

Operation results: W0 = $0070 (hex)
W1 = $1235 (hex)
W2 = $56**07** (hex)
W3 = $**0020** (hex)

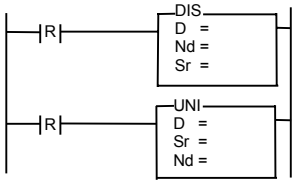
The high-order 8 bits of W2 do not change.

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Instruction

Mnemonic	Dissemble by 4 bit units/ Unify by 4 bit units	Range
DIS UNI	DIS: Dissemble by 4 bit units UNI: Unify by 4 bit units	☐ Bit ■ Byte ☐ Word

Ladder

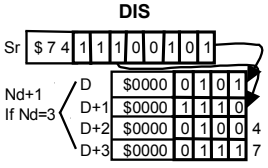


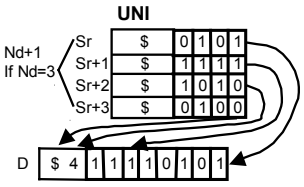
DIS: Separate Sr into Nd+1 units of 4 bits each, and store in the low 4 bits of words starting at D.

UNI: Combine the low 4 bits of Nd+1 words starting at Sr, and store in D.

Description

1. DIS: Separate the word value in register Sr into Nd+1 units of 4 bits each, and store these 4 bit units in sequence into registers starting at D. The 12 remaining high-order bits in each register become 0.
2. UNI: Combine the low-order 4 bit units from Nd+1 registers starting at Sr, and store in D.



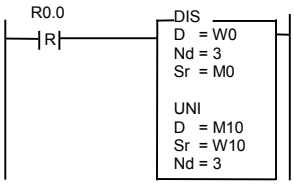


3. Nd + 1 represents the number of 4-bit segments to dissemble or unify. The range for Nd is Nd = 0 to 3.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

Initial conditions:	M0 = $**74E5** (hex)	W0 = $1111 (hex)
		W1 = $2222 (hex)
		W2 = $3333 (hex)
		W3 = $4444 (hex)
	W10 = $012**3** (hex)	M10 = $ABCD (hex)
	W11 = $456**F** (hex)	
	W12 = $789**A** (hex)	
	W13 = $765**4** (hex)	
Operation results:	M0 = $74E5 (hex)	W0 = $**0005** (hex)
		W1 = $**000E** (hex)
		W2 = $**0004** (hex)
		W3 = $**0007** (hex)
	W10 = $0123 (hex)	M10 = $**4AF3** (hex)
	W11 = $456F (hex)	
	W12 = $789A (hex)	
	W13 = $7654 (hex)	

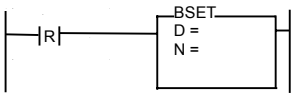
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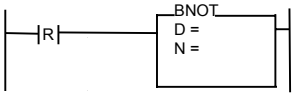
Bit Conversion Instruction Details

Instruction

Instruction	Bit Set, Reset, Reverse, Test	Range
BSET	BSET: Nth bit set	☐ Bit
BRST	BRST: Nth bit reset	☐ Byte
BNOT	BNOT: Nth bit reverse	■ Word
BTST	BTST: Nth bit test	

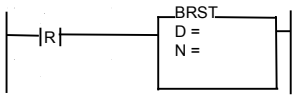
Ladder

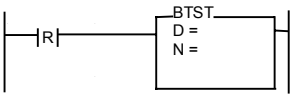




BSET: Set the Nth bit in the D register (X→1).

BNOT: Reverse the Nth bit in the D register (0→1, 1→0).



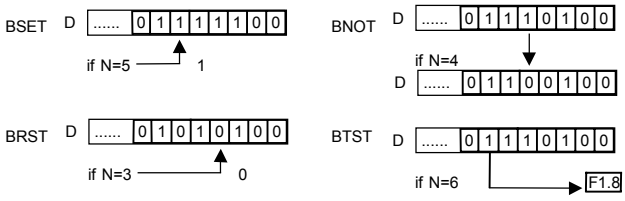


BRST: Reset the Nth bit in the D register (X→0).

BTST: Copy the Nth bit to the carry bit in the D register (X→F1.8).

Description

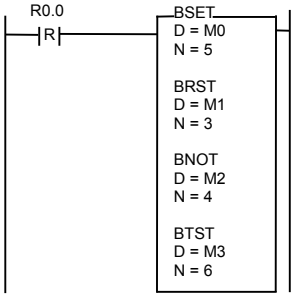
1. BSET: Set the Nth bit of register D to 1.
2. BRST: Reset the Nth bit of register D to 0.
3. BNOT: Reverse the state of the Nth bit of register D.
4. BTST: Set the carry bit F1.8 to the state of the Nth bit of register D.
5. These instructions are useful when it is necessary to perform bit-level operations on word-only memory addresses, such as W, PV, SV, and SR.



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Example

Program Expression



Operation Results

Initial conditions: M0 = 0001 0010 00**0**1 1100 (binary)
M1 = 0011 0100 0101 **1**100 (binary)
M2 = 0101 0110 011**1** 0100 (binary)
M3 = 0111 1000 0**1**11 0100 (binary)
F1.8 = **0 (Off)**

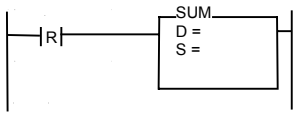
Operation results: M0 = 0001 0010 00**1**1 1100 (binary)
M1 = 0011 0100 0101 **0**100 (binary)
M2 = 0101 0110 011**0** 0100 (binary)
M3 = 0111 1000 0111 0100 (binary)
F1.8 = **1 (On)**

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Instruction

Mnemonic	Count Number of On (= 1) Bits	Range
SUM	Count On (= 1) bits in the S register	☐ Bit
		■ Byte
		☐ Word

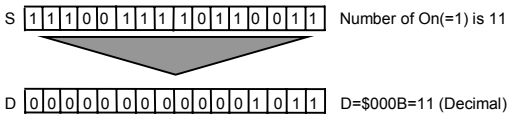
Ladder



SUM: Count the number of On (= 1) bits in the S register and store the result in the D register.

Description

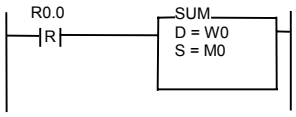
1. Count the number of On (= 1) bits in the S register and store the result in the D register.



2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

Initial conditions: M0 = 1110 0111 1011 0011 (binary)
W0 = $XXXX (hex)

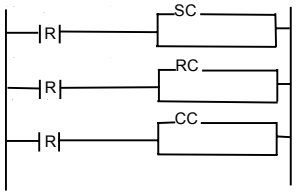
Operation results: M0 = 1110 0111 1011 0011 (binary)
W0 = $000B (hex) = 11 (decimal)

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Instruction

Mnemonic	Carry Bit (F1.8) Set, Reset, Reverse	Range
SC	SC: Set carry bit	☐ Bit
RC	RC: Reset carry bit	☐ Byte
CC	CC: Reverse carry bit	☐ Word

Ladder



SC: Carry bit set (F1.8: X→1).

RC: Carry bit reset (F1.8: X→0).

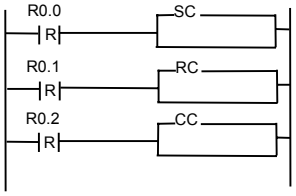
CC: Carry bit reverse (F1.8: 0→1, 1→ 0).

Description

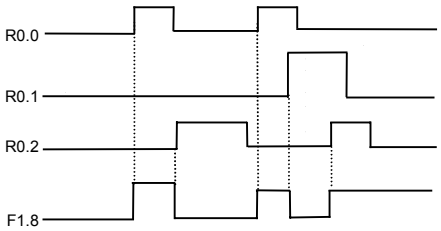
1. The carry bit (F1.8) is a special internal flag that holds the result of various types of mathematical and bit shift operations. When rotating, shifting, adding, or subtracting with a carry, the operation depends on the state of the carry flag, as well as changes the state of the carry flag. The above instructions are useful for setting the state of the carry flag as needed for these types of operations.
2. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results



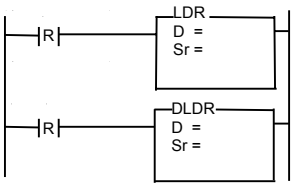
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Transfer Instruction Details

Instruction

Mnemonic	Load Absolute Address	Range
LDR DLDR	Store value at absolute address Sr in D, D←(Sr)	☐ Bit ■ Byte ■ Word

Ladder



Store the value located at the absolute address pointed to by Sr into register D.

R0 word absolute address: 0
M0 word absolute address: 192
W0 word absolute address: 512

Description

1. This instruction is useful in transferring data patterns stored sequentially in memory, to a single output register location. For example, if the register addresses W100 through W199 contained a set of 100 control patterns (P0 to P99) that needed to be transferred to theoutputs of a module (address R015), the LDR instruction can be used to load the data from the absolute addresses of W100 to W199 (absolute addresses 612 to 711) into the destination register R015.
2. In the example below, register W0 is used as the Sr (source) register, which contains the absolute address of the data patterns to be loaded. Initially, W0 contains 612, which is the absolute memory address of register W100. As W0 is incremented, it successively points to the next higher W register to load data from.
3. See Chapter 5, Absolute Address Designation, for a complete table of absolute addresses.

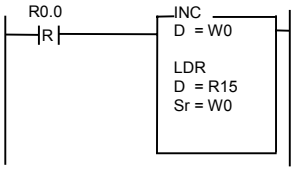
Control Pattern	Register (Absolute Address)	Register Value
P0	W100 (612)	$22
P1	W101 (613)	$10
P2	W102 (614)	$33
:	:	:
:	:	:
P98	W198 (710)	$05
P99	W199 (711)	$85

Transfer the data of W100-W199 ($22, $10, $33,..., $05, $85) registers in sequence into R015. See the following example.

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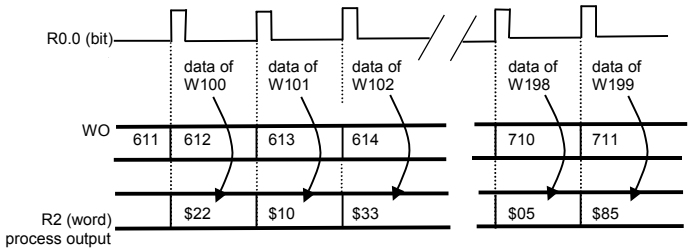
Example

Program Expression



Operation Results

Initial conditions: W0 = 611

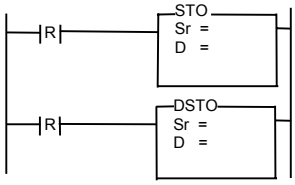


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Instruction

Mnemonic	Store Absolute Address	Range
STO DSTO	Store Sr in register at absolute address D, (D)←Sr	☐ Bit ■ Byte ■ Word

Ladder



Store the data contained in the Sr register into the register pointed to by the absolute address contained in register D.

R0 word absolute address: 0 (decimal)
M0 word absolute address: 192 (decimal)
W0 word absolute address: 512 (decimal)

Description

1. This instruction is useful in storing data patterns from a single input register to a sequential table of registers in memory. For example, if the process measurements (D0 to D99) from an input module located at address R001 needed to be stored in register addresses W100 through W199. The STO instruction can be used to load the data from the source register R001 to the absolute addresses of W100 to W199 (absolute addresses 612 to 711).
2. In the example below, register W0 is used as the D (destination) register, which contains the absolute address of the locations to store the process measurements. Initially, W0 contains 612, which is the absolute memory address of register W100. As W0 is incremented, it successively points to the next higher W register to store data.
3. See Chapter 5, Absolute Address Designation, for a complete table of absolute addresses.

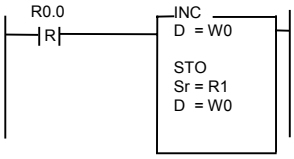
Process Measurement	Register (Absolute Address)	Register Value
D0	W100 (612)	$34
D1	W101 (613)	$25
D2	W102 (614)	$88
:	:	:
:	:	:
D98	W198 (710)	$17
D99	W199 (711)	$09

Store the process measurement data ($34, $25, $88,...,$17, $09) you get from inputs at 001 in sequence into W100-W199. See the following example.

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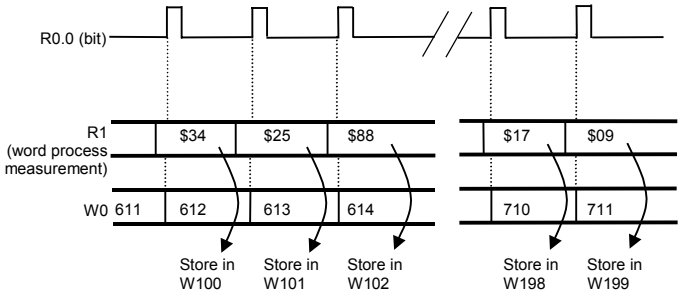
Example

Program Expression



Operation Results

Initial conditions: W0 = 611

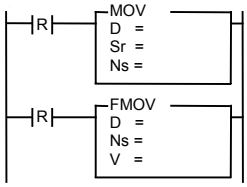


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Instruction

Mnemonic	Duplicate Word, Duplicate the Same Word	Range
MOV FMOV	MOV: Copy a block of words FMOV: Fill a block of words with the same value	☐ Bit ☐ Byte ■ Word

Ladder

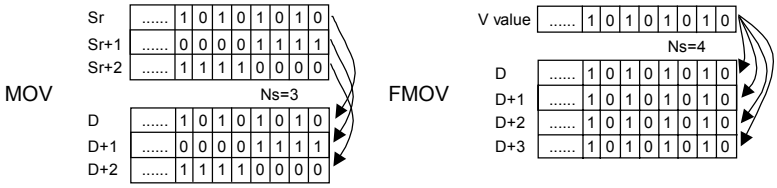


MOV: Copy Ns words from Sr to D.

FMOV: Repeatedly copy the value V, Ns times to words starting at register address D.

Description

1. MOV: Copy a total of Ns registers from registers starting at Sr word into registers starting at D. This instruction is used for mass duplication of blocks of registers.
2. FMOV: Copy the constant number V, Ns times into registers starting at D. This instruction is useful for initializing the internal and external memory of certain areas when initializing a program.

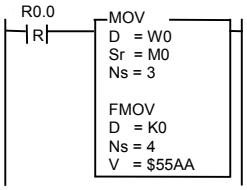


3. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

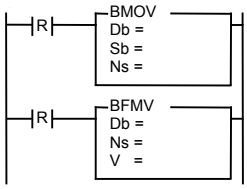
Initial conditions:	M0 = $12AA (hex)	W0 = $XXXX (hex)
	M1 = $340F (hex)	W1 = $XXXX (hex)
	M2 = $56F0 (hex)	W2 = $XXXX (hex)
	K0 = $XXXX (hex)	K2 = $XXXX (hex)
	K1 = $XXXX (hex)	K3 = $XXXX (hex)
Operation results:	M0 = $12AA (hex)	W0 = $12AA (hex)
	M1 = $340F (hex)	W1 = $340F (hex)
	M2 = $56F0 (hex)	W2 = $56F0 (hex)
	K0 = $55AA (hex)	K2 = $55AA (hex)
	K1 = $55AA (hex)	K3 = $55AA (hex)

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Instruction

Mnemonic	Copy Bit, Copy the Same Bit	Range
BMOV BFMV	BMOV: Copy a block of bits BFMV: Fill a block of bits with the same bit value	■ Bit ☐ Byte ☐ Word

Ladder

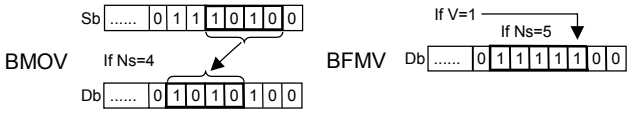


BMOV: Copy Ns bits from bit address Sb into bit address D.

BFMV: Copy the V bit (0 or 1) into bit address D, Ns times.

Description

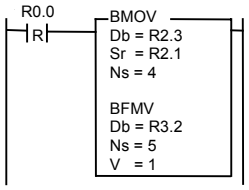
1. BMOV: Copy a block of Ns bits starting at bit address Sb to bit address D. This instruction is useful for moving large blocks of bits at one time, or for copying sections of bits within a word without copying the entire word.
2. BFMV: Fill a block of Ns bits starting at bit address D with the value of V (0 or 1). This instruction is useful for initializing a set of bits to 0 or 1 at the start of a program or process.



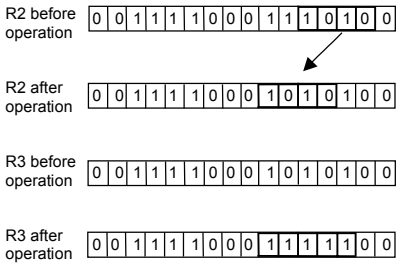
3. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results



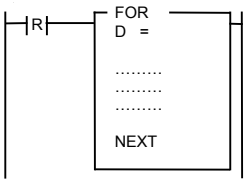
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Block Processing Instruction Details

Instruction

Mnemonic	FOR-NEXT Loop	Range
FOR	FOR (DFOR): Start loop	☐ Bit
DFOR	NEXT: End loop	■ Byte
NEXT		■ Word

Ladder



FOR: Begin execution of instructions between (D)FOR and corresponding NEXT. Repeat execution D times.

NEXT: Decrease D of FOR instruction by 1. If not zero, repeat from FOR instruction.

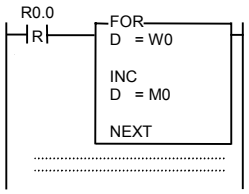
Description

1. The FOR/NEXT instructions are used to perform a block of instructions inside a ladder program repeatedly. The parameter D of the FOR instruction is a value indicating how many times the block of instructions is to be performed.
2. Branch instructions such as JMP and CALL can be made inside the FOR/NEXT loop.
3. The number of loops to execute (D value) can be changed inside of the FOR/NEXT loop. This can be used to dynamically increase or decrease the number of loops performed while processing the loops.
4. If the D register is 0 before the FOR instruction, the instructions between the FOR and NEXT instructions will NOT be executed. Instead, the program will jump directly to the instruction following the NEXT.
5. As the FOR/NEXT loop occurs within a single program scan, a large value of D will lengthen the scan time of the program considerably.
6. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

Initial condition: W0 = 10
M0 = 0

Operation results: W0 = 0
M0 = 10

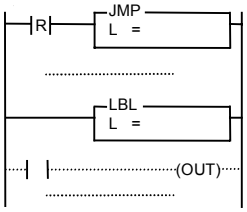
When the R0.0 contact changes from Off→On, execution of the FOR/NEXT loop occurs. At the FOR instruction, the value of W0 is evaluated. If W0 is not 0, then the instructions between the FOR and NEXT (INC D = M0) is performed. At the NEXT instruction, 1 is subtracted from the value of W0, and execution returns to the FOR instruction. This is repeated 10 times, until the value of W0 is 0. When this occurs, execution goes directly the instruction following the NEXT instruction.

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Instruction

Mnemonic	Jump by Pointer	Range
JMP LBL	JMP: Jump by pointer LBL: Specify the pointer	☐ Bit ☐ Byte ☐ Word

Ladder



JMP: Jump to the LBL instruction L (L = 0 to 31).

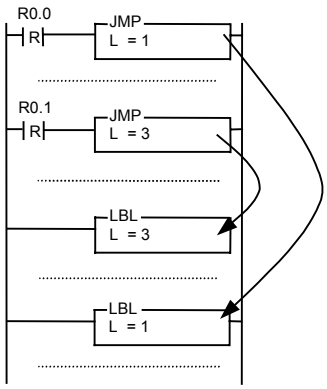
LBL: Position jumped to by the JMP instruction.

Description

1. This instruction is used to conditionally perform a set of instructions in the program. When the input condition to the JMP instruction is true, execution will jump over the following instructions, directly to the corresponding LBL label. When the input condition is false, the instructions following the JMP will be executed normally, and no jump occurs.
2. The range of L is 0 to 31, allowing 32 jumps to be used.
3. The given L label may only be used once in a program. It may not be duplicated.
4. For a given JMP with parameter L, there MUST be a corresponding LBL with the same L value. Also, the LBL instruction must come after the JMP instruction in the program. If either of these two conditions is not satisfied, an error will occur preventing execution of the program.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

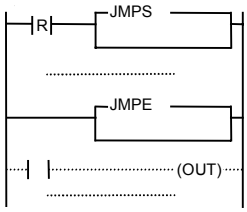
- When contact R0.0 turns On, JMP 1 occurs, and execution jumps directly to LBL 1—the instructions between the JMP and LBL are not executed.
- When contact R0.1 turns On, execution of the program jumps directly from JMP 3 to LBL 3.

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Instruction

Mnemonic	Jump	Range
JMPS	JMPS: Start jump	☐ Bit
JMPE	JMPE: End jump	☐ Byte
		☐ Word

Ladder



JMPS: Jump directly to the corresponding JMPE instruction.

JMPE: Position jumped to by JMPS instruction.

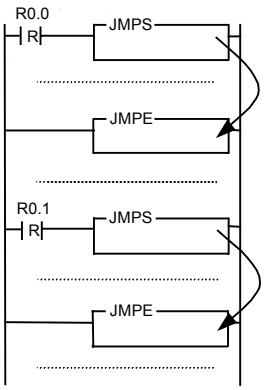
Description

1. The JMPS and JMPE instruction function identically to the JMP and LBL instructions, but do not require the use of a label. Additionally, the JMPS/JMPE pair may be used more than once in a program.
2. This instruction is used to conditionally perform a set of instructions in the program. When the input condition to the JMPS instruction is true, execution will jump over the following instructions, directly to the corresponding JMPE. When the input condition is false, the instructions following the JMPS will be executed normally, and no jump occurs.
3. For the JMPS instruction, there MUST be a corresponding JMPE. Also, the JMPE instruction must come after the JMPS instruction in the program. If either of these two conditions is not satisfied, an error will occur preventing execution of the program.
4. The JMPS/JMPE instructions may NOT be nested—after each JMPS instruction, there must be a JMPE instruction before the next JMPS instruction may be programmed.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

By executing a JMPS:

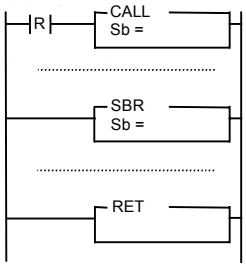
- When contact R0.0 or R0.1 turns On, execution of the program jumps directly from the associated JMPS to its corresponding JMPE.

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Instruction

Mnemonic	Call Subroutine	Range
CALL	CALL: Call subroutine	☐ Bit
SBR	SBR: Start subroutine	☐ Byte
RET	RET: End subroutine	☐ Word

Ladder



CALL: Call subroutine Sb (Sb = 0 to 31)

SBR: Start Subroutine

RET: Return from Subroutine

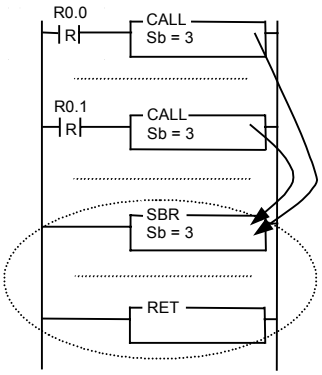
Description

1. The subroutine instructions are used when a block of instructions needs to be called more than once, or called with different values, from the main program.
2. The subroutine to be called is specified by the Sb parameter in the CALL and SBR instructions. The CALL instruction causes execution to jump to the specified SBR instruction. After executing the instructions between SBR and RET, program execution is returned to the instruction following the CALL instruction that called the subroutine.
3. The subroutine defined by the SBR and RET instructions must come after the associated CALL instruction. All subroutines must be defined and programmed at the end of the control program. A total of 64 subroutines are available (Sb = 0 to 31).
4. The same subroutine (SBR Sb) can be called by multiple CALL instructions. However, each subroutine number may only be used once by an SBR instruction.
5. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

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Example

Program Expression



Operation Results

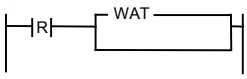
When contact R0.0 and/or R0.1 turns On, the CALL Sb = 3 instruction is executed and the instructions between SBR Sb = 3 and RET are executed. After executing this subroutine, the program returns to the next instruction after the CALL.

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Instruction

Mnemonic	Clear Watchdog Time	Range
WAT	WAT: Clear watchdog time	☐ Bit
		☐ Byte
		☐ Word

Ladder



WAT: Clears the watchdog timer while executing the program.

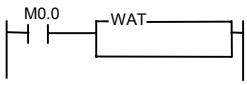
Description

1. This instruction clears the watchdog timer within the CPU module to prevent the program from stopping even if the scan time exceeds the maximum watchdog time. The default watchdog time is 3 seconds.
2. Under normal operation, the PLC executes the following process:
   - Read external inputs.
   - Process the control program.
   - Update the external outputs.

   One execution of this process is termed a scan. When the time it takes to process a single scan (the scan time) is excessively long, abnormal results may occur caused by the delay in reading inputs and updating outputs. For this reason, a watchdog time is set by the PLC which, when exceeded, indicates that an error has occurred. When this happens, the PLC stops the program to prevent abnormal operation.
3. Under certain circumstances, extremely lengthy scan times may be allowable. The WAT instruction allows the user to reset the watchdog timer to prevent the PLC from automatically going into the error condition and stop mode when the watchdog time is exceeded.
4. This operation will occur on every scan for which the input condition is true (On). To perform the operation only on a change of input condition, use the rising/falling edge contact.

Example

Program Expression



Operation Results

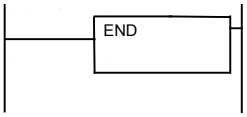
In certain applications, the user program may contain loops which cause lengthy scan times. In the example, turning on M0.0 prevents the PLC from stopping when the watchdog time (maximum of 3 sec) is exceeded. For normal PLC control applications, this instruction should not be used.

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Instruction

Mnemonic	End Control Program	Range
END	END: End control program (Inserted automatically)	☐ Bit
		☐ Byte
		☐ Word

Ladder



Description

1. This instruction indicates the end of the control program.
2. This instruction is automatically added by GPC. It is not programmed by the user.

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Testing and Troubleshooting

7

This chapter provides information on testing and troubleshooting the D50 PLC.

This chapter discusses:

- *Testing procedures for the D50 PLC*
- *How to troubleshoot the D50 PLC*

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Test Precautions

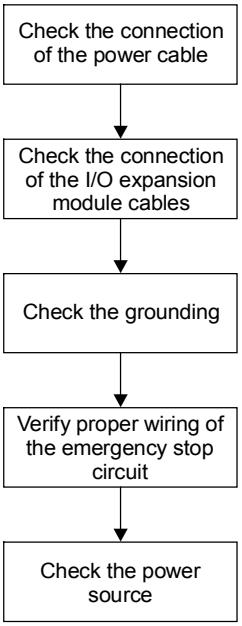
When checking the system:

⚠ CAUTION: Always turn off the power whenever you install or remove a module.

1. Check the module more than one time before exchanging the part.
2. Include a complete description of the symptoms when you return a defective module for repair.
3. When you suspect that a contact may be defective, it might only need cleaning. Clean the contact using a clean cotton cloth and alcohol. Then retest the module.
4. Do not use thinner to clean any of the parts.

System Checks

Before installing the I/O wiring of the PLC and supplying power, check the following items.



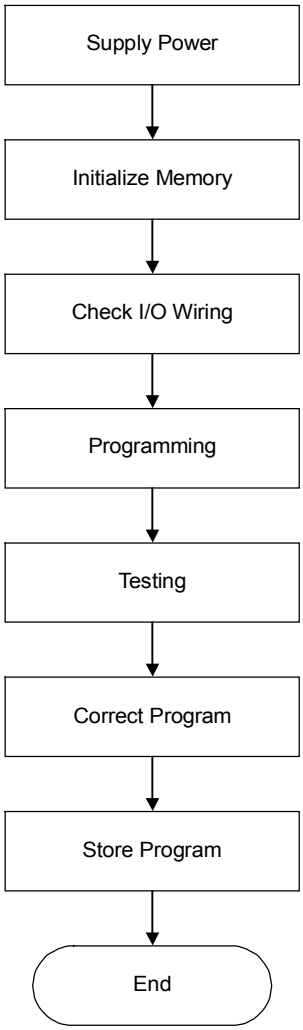
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Item	What to Check
The connection of the power cable and the I/O expansion cables.	• Check that the wiring is secure and intact. • Check that the terminal screws are tightly fastened. • Check that I/O module is firmly fixed. • Check that the power cable connection is secure. • Check that the cable size is correct.
Grounding	• Check that the grounding is triple grounded and separate from other device grounds.
Emergency stop circuit	• Check that the emergency stop circuit for problems external to the PLC is wired accurately, and will IMMEDIATELY disconnect power on demand.
Power source	• Check that the power and voltage sources are within specifications. For 110/220 VAC (85 to 264 VAC) For 24 VDC (20 to 28 VAC) • Check that the voltage to AC-type I/O is within specifications.

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Testing Procedures

When the PLC has been installed and wired, begin testing in the following order.



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Item	What to Check/Do
Power source	• Check that the input voltage to the power supply is within specification. • Check that the control voltage to the I/O is within specification. • Turn on the power source. • Check the LED display on the controller.
Initialize memory	• Initialize the PLC module using GPC. (This clears the program in the PLC.)
Check I/O wiring	• Check the LEDs of the input modules and use the monitor function of GPC after testing the input device. • Check the wiring of the output by turning the output On/Off using the monitor mode of GPC (set PLC to Run mode).
Programming	• Check the program. • Download the program into the CPU module.
Testing	• Check the Run LED for illumination by setting the mode switch of the controller to Run. • Check for the proper operation of the program.
Correct programming	• Correct any program errors. • Program is stored.
Store program	• Store the program onto a floppy disk or similar storage device and place in a secure place. • Record the PLC type, program capacity, name of installation, and date for the recorded program. • Print the program (ladder, mnemonic) and store it in a secure place.

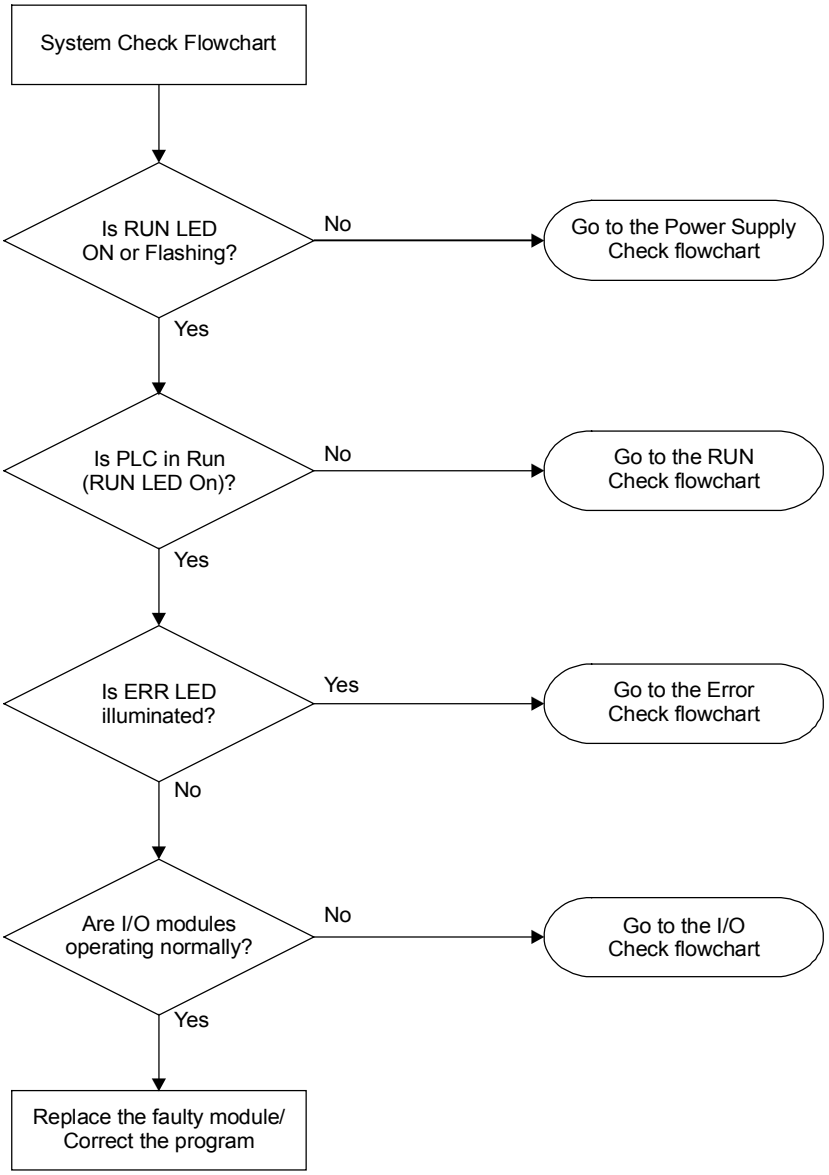


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Correcting Errors

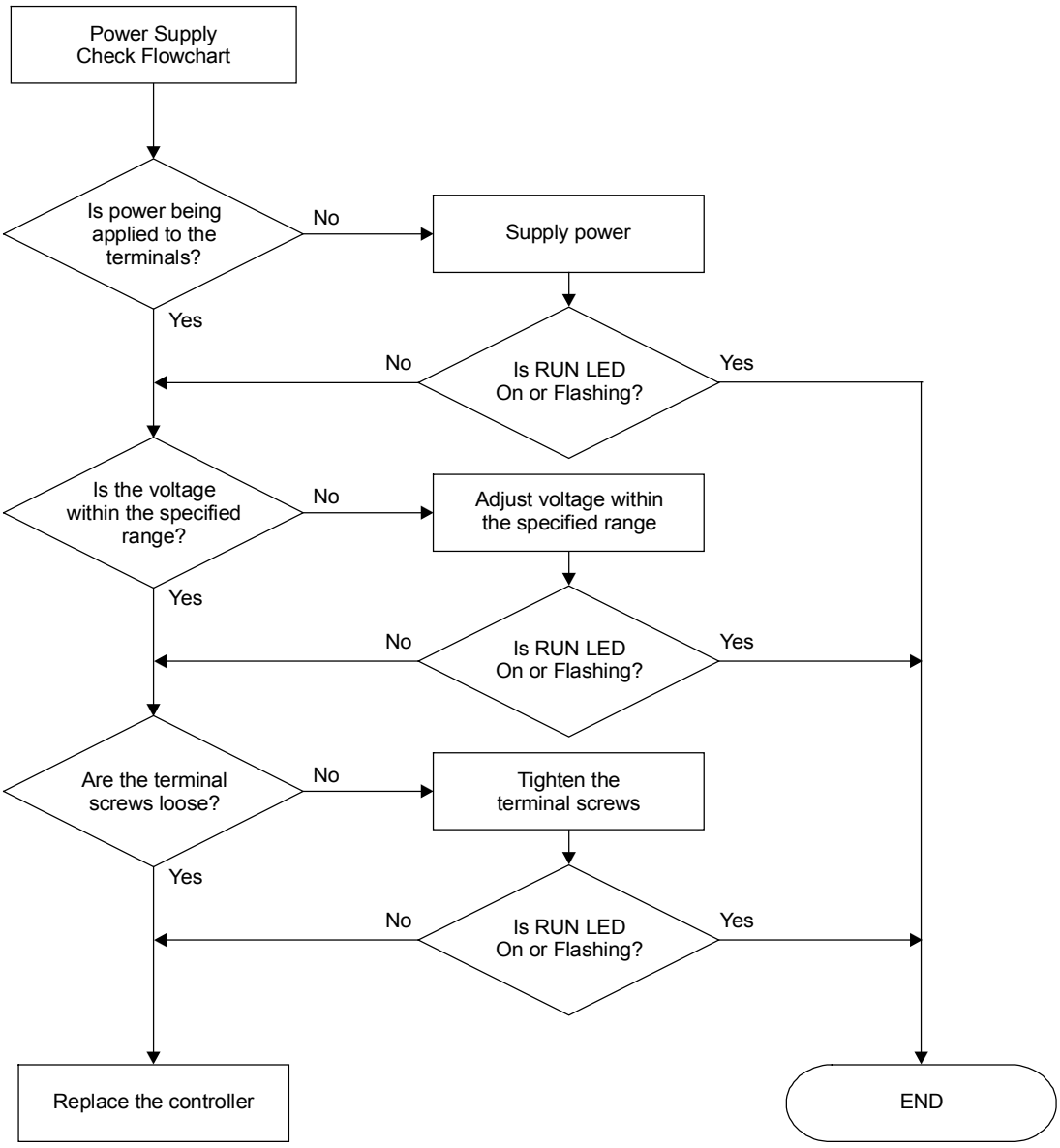
System Check

Refer to the system check flow chart when you encounter problems during startup and testing.



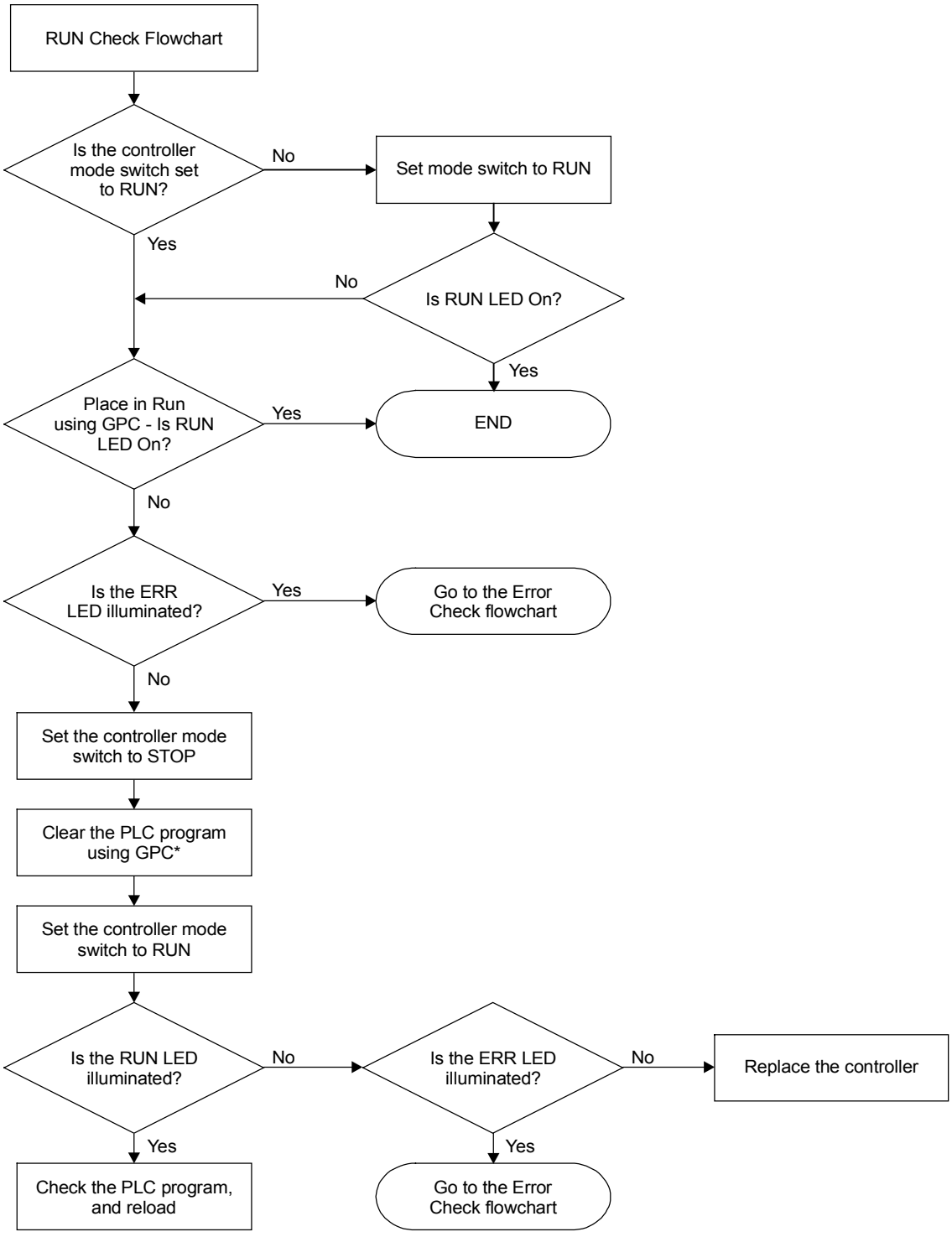
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Power Supply Check



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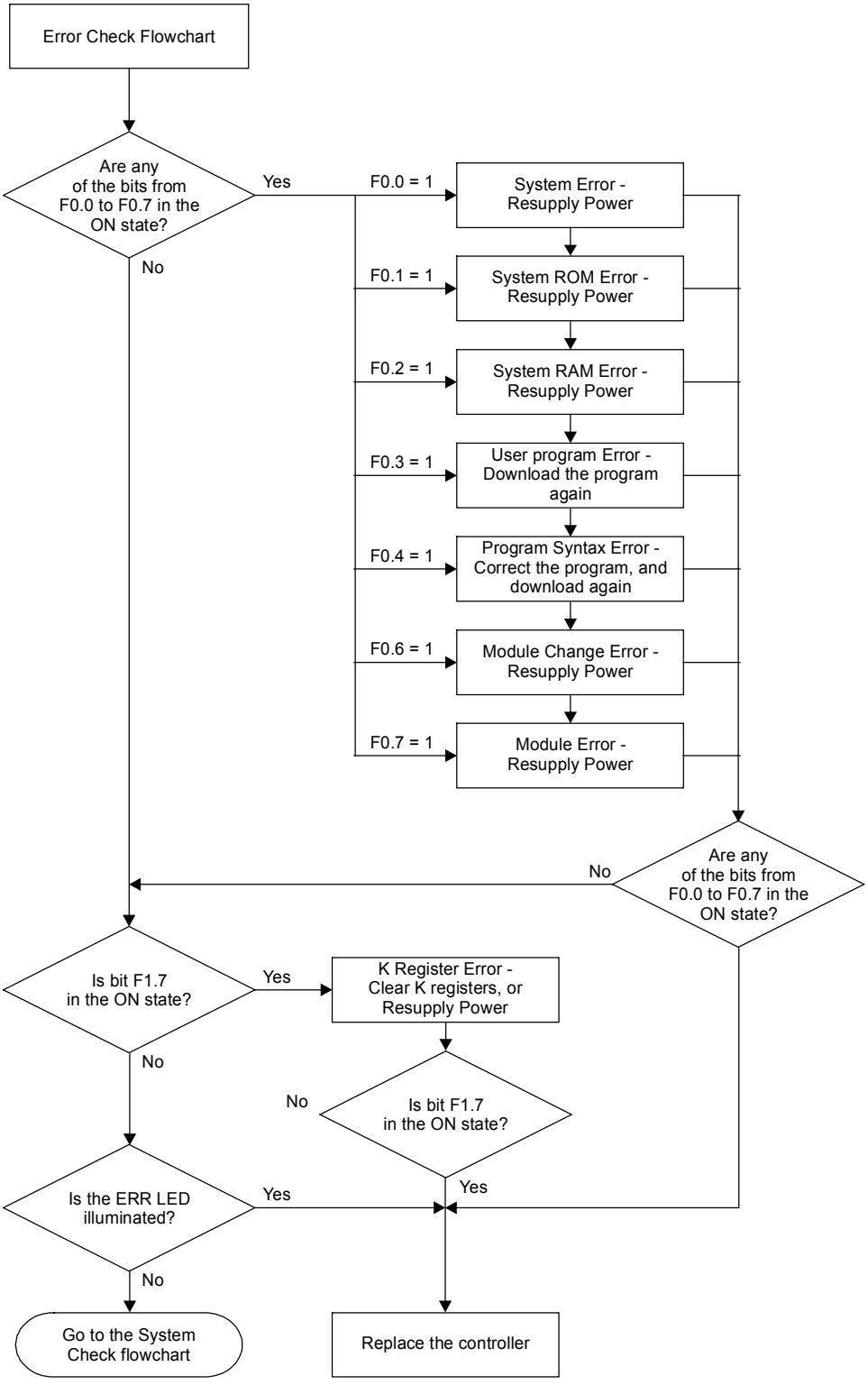
Run Check



*Be certain to save the program before clearing the PLC program so it is not lost.

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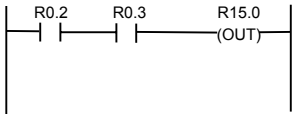
Error Check

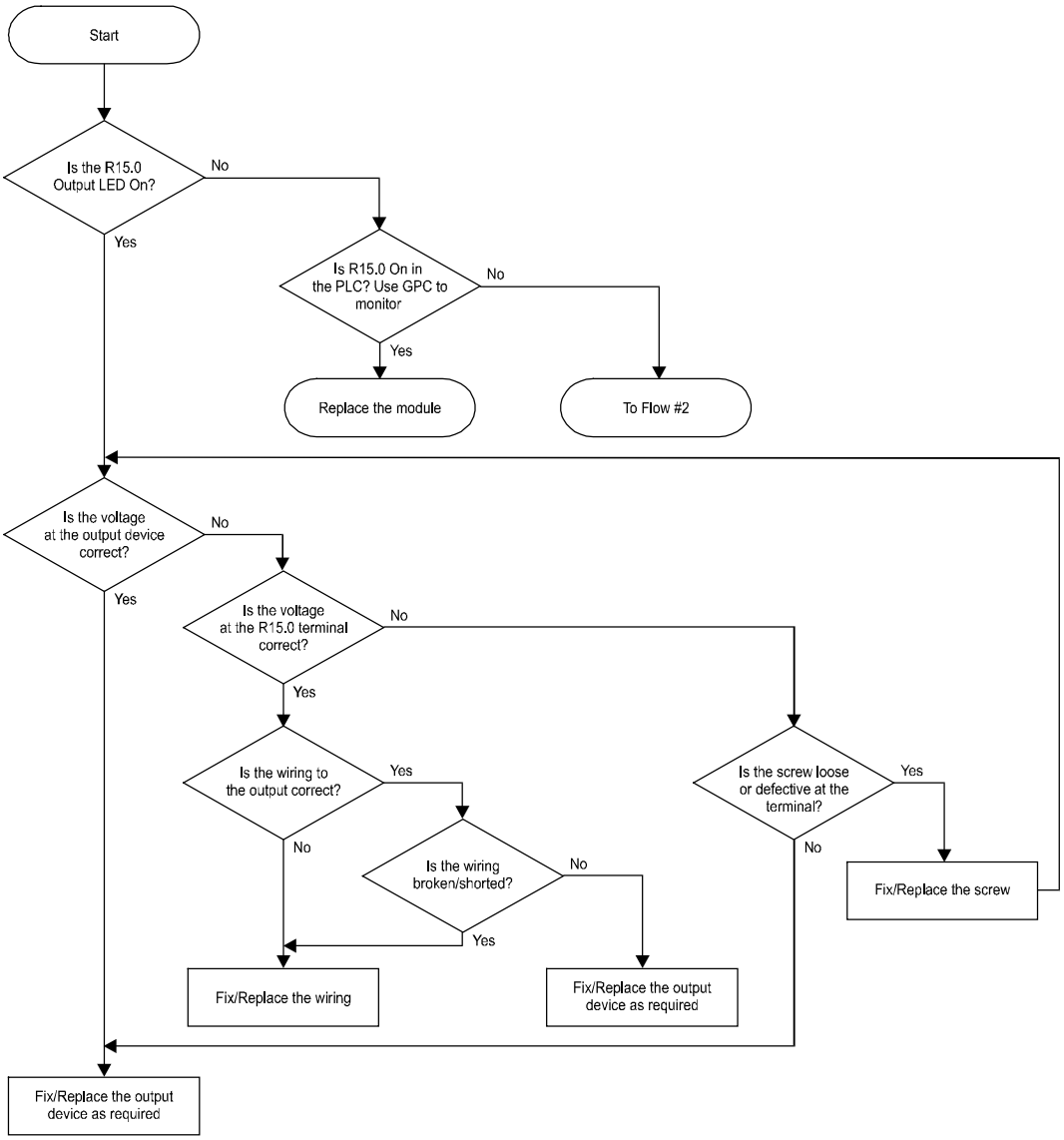


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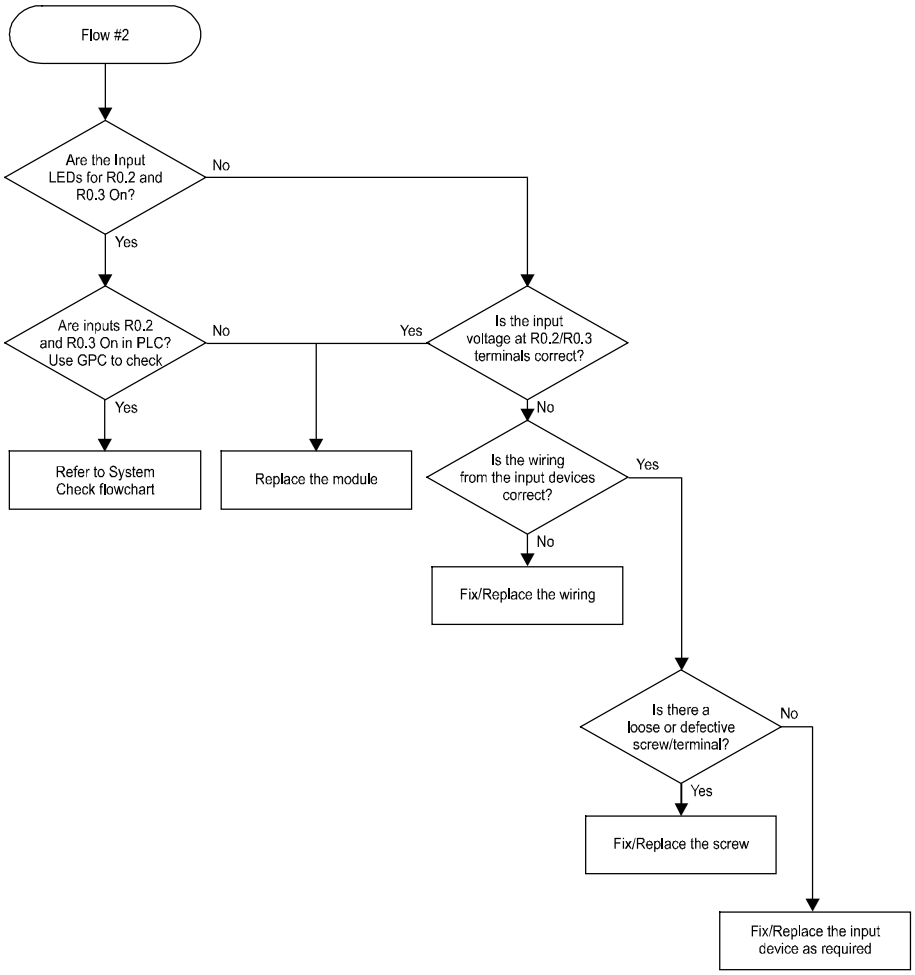
I/O Check

This page presents an example of a troubleshooting procedure to follow when errors are encountered with the external I/O. In this example, two of the inputs on the controller are used to control an output on the controller. This flow chart is based on the following circuit, and assumes that the error encountered is that the output connected to R15.0 is not turned On when it should be.





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Troubleshooting, Maintenance and Inspection Tables

The following tables list some common problems and troubleshooting procedures for the PLC system in the event of faulty operation. Additionally, a table is provided which covers the routine maintenance procedures to be followed to ensure long life of the PLC system with minimum downtime and maintenance cost.

System Operation

Symptom	Expected Cause	Troubleshooting
Run LED will not illuminate.	Program errors	Correct the program.
	Power line defect	Replace the CPU module.
Output will not turn to On state during Run.	Short or open circuit	Replace the CPU module.
I/O Modules above a certain address will not operate.	I/O bus error	Check I/O expander cable.
Not all points on an I/O module operate properly.	I/O bus error	Check I/O expander cable.

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Digital Inputs

Symptom	Expected Cause	Troubleshooting
No inputs on the module will turn On (LEDs are not illuminated).	No external input power	Supply power.
	Low external input voltage	Make sure full voltage is being supplied.
	Terminal screw is loose/ Defective contact	Tighten screw/ Reconnect the module
Inputs will not turn to On state (LEDs are illuminated).	Defective input circuit	Replace the module.
One or more inputs on an I/O module will not turn On.	Device connected to input module is defective.	Replace the input device.
	Loose input wiring	Reconnect the input wiring.
	External input time is too short.	Adjust the input device.
	Terminal screw is loose/ Defective contact	Tighten screw/ Reconnect module
One or more inputs on an I/O module will not turn Off.	Defective input circuit	Replace the module.
Input changes On/Off state erratically.	Low external input voltage	Make sure full supply voltage is being input.
	Noise error	Troubleshoot for noise.
	Terminal screw is loose/ Defective contact	Tighten screw/ Reconnect module
Input display LED will not illuminate (input is On in PLC).	LED error	Replace the module.

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Digital Outputs

Symptom	Expected Cause	Troubleshooting
No outputs on the module will turn On.	No external input power	Supply power.
	Low external input voltage	Make sure full voltage is being supplied.
	Terminal screw is loose/ Defective contact	Tighten screw/ Reconnect module
	I/O contact connection	Replace the module.
	Defective output circuit	Reconnect the module.
One or more outputs on an I/O module will not change to On or Off state.	Output circuit error	Replace the module.
Output on an I/O module will not turn Off (LED is not illuminated).	Output time too short	Correct the program.
	Defective output circuit	Replace the module.
Output on an I/O module will not turn Off (LED is illuminated).	Incorrect output load	Replace the output load.
	Loose output wiring	Reconnect the output wiring.
	Terminal screw is loose/ Defective contact	Tighten screw/ Reconnect module
	Output contact error	Replace the module of the relay.
	Defective output circuit	Replace the module.
Output on an I/O module will not turn On (LED is illuminated).	Output contact error	Replace the module of the relay.
	Leakage current to low-current load	Apply leakage current protection
Output on an I/O module will not turn On (LED is not illuminated).	Defective output circuit	Replace the module.
Output changes On/Off state erratically.	Low external input voltage	Make sure full supply voltage is being input.
	Noise error	Troubleshoot for noise.
	Terminal screw loose/ Defective contact	Tighten screw/ Reconnect module
All outputs on a module with the same common operate incorrectly or identically.	Common terminal screw loose	Tighten the screw.
	Defective contact/ Terminal connector	Reconnect the module.
	CPU module error	Replace the CPU module.
Output display LED is not on (output is On to field device).	LED error	Replace the module.

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Periodic Inspection and Preventive Maintenance

The D50 PLC Series requires regular inspection and maintenance for proper operation. The following items should be checked every six months.

Item	What to Check	Criteria	Test Equipment
Supplied Power	Does the voltage measured within the power terminal fall within the specified range?	Voltage must fall within the power module input voltage specifications.	Voltmeter
Environment	Does the temperature fall within the specified range?	0 to 55°C (32 to 131°F)	Thermometer
	Does the humidity fall within the specified range?	Humidity levels below 20% RH.	Hygrometer
	Is there any dust present?	No dust.	Visual
I/O Power	Does the control voltage supplied to the I/O modules fall within the specified limit?	Control voltage must fall within the input and output modules specifications.	Voltmeter
Module Mounting and Wiring	Are all of the modules secure?	All should be firmly secured.	Screwdriver
	Is the connection cable secure?		
	Is the external wiring screw loose?		

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Troubleshooting Noise Problems

8

This chapter outlines the various causes of noise that affect the D50 PLC system. Installation tips and troubleshooting methods for identifying noise problems are also provided.

This chapter discusses:

- *The causes of noise*
- *Installation tips for avoiding noise*
- *Methods to identify and resolve noise problems*



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Noise Occurrence

Types of Noise

- Radiation noise is transmitted in the form of a magnetic wave. The amplitude of the magnetic wave is measured in Gauss.
- Conduction noise is transmitted through a direct path such as signal wiring or ground connections as a strong, high-voltage surge. This type of noise is measured as voltage, current, or power.
- Normal mode (single ended developed) noise can come through the power and/or the signal cables. This type of noise is not equally distributed across the PLC input terminals.
- Common mode noise can come through the power and/or the signal cables. In this case the noise is close to the same amplitude thus the term common on both leads of the cable.
- Impulse noise is electrical or magnetic energy that has less than a 200 msec pulse duration.
- Surge noise is electrical energy that has a pulse duration of 200 msec to 2 sec.
- Transient noise is electrical energy that has an extremely short duration usually lasting only a few nanoseconds (1×10^{-9}).

Electrical Noise Fundamental Definitions

- Isolation means to physically separate the connection between areas. Isolation is effective for common mode noise.
- Filters are effective against conduction noise such as impulses. Filtering is used to remove normal mode noise and common mode noise that has been imprinted onto the signal or power cables. A low-pass filter passes only low frequency signals. Low-pass filters are classified as either LC (L = inductor and C = capacitor) filters or RC (R = resistor and C = capacitor) filters, according to the electrical parts that form the filter.
- Surge absorbers are devices that protect electronic equipment by clamping down extremely high voltage spikes (lightning strikes) in power cables to a safe level.
- Charge is an excess or deficiency of electrons in an object. When an object becomes charged, a magnetic field forms around the object and can radiate noise as the amplitude of the charge is varied.
- An inductive load is a device which creates a large magnetic field that opposes any change in the voltage applied across the device. Devices that act as inductive loads are relay coils, motor coils, starter coils and actuator coils.
- Stray capacitance and inductance is created during the installation of an electrical system. When excess cabling is left wound up this creates stray inductance in the form of a coil. All cabling inherently has a capacitive rating (so many picofarads per meter). Excessively long cable runs or untrimmed cable lengths or poorly specified cable types can add large levels of stray capacitance.

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Sources of Noise

There are three main sources of noise. Some of these sources generate large noise amplitudes. The occurrence time can be very short (impulse type) or continuous (power line induced). Some noise levels can damage the D50 PLC components and peripheral devices.

1. **Noise Generated by Electronic Equipment**
   All electronic devices radiate noise in the form of a magnetic field. The magnetic field is created around the printed circuit board or the wiring of electronic devices due to the flow of electrical current. The amplitude of the magnetic field changes over time due to changes in the flow of the electrical current. The magnetic field strength increases as the amount of the electrical current flow increases.

   As a device crosses the magnetic field, electrical currents will be induced. The induced current could be summed vectorially with the normal electrical currents. In some cases this could cause cancellation of electrical current flow (essentially shutting down the circuit). In other cases this could create large surge currents that cause severe damage to the circuit. In most cases the summation of the currents cause errors in readout and control values. Some sources of this kind of noise are relays, magnetic contactors, inverters, computer monitors, and motors.
2. **Noise from Power Cables**
   When various loads are connected to a single power source the current draw conditions and impedance imbalance can cause unwanted noise. The noise created by these sources can affect other devices connected to the power source, via spikes, sags, reflected high speed switching noise, and ground pulse. This is the most frequent cause of noise in a PLC's environment.
3. **Noise from Natural Causes and Work Practices**
   Lightning, welding, shared cable trays, "grandfather'd plant wiring," and static electricity can also be sources of noise.

In the first case, the noise is caused within the equipment and is called internal noise. In the second case, the noise is caused by external factors and referred to as external noise. These two types of noise may also be referred to as artificial system noise.

The noise caused by natural occurrences can not be prevented, but can be controlled. Precautions such as good grounding techniques, surge suppressors, and burying cables underground can help minimize the affect. This type of noise may be referred to as natural noise.



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Advised Installation Practices

Shield the PLC

The most common method of shielding, is to install the PLC inside a grounded steel enclosure.

Proper Cable Selection

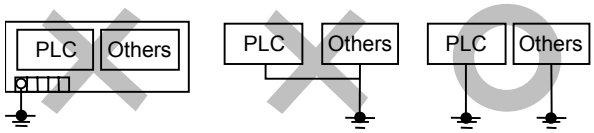
Use twisted, shielded-pair cable for the power cable and field wiring. Properly terminate the shields of all cables to a single-point high-quality ground. (See section on shielding.)

Ground the PLC

The purpose of grounding the PLC is to protect the electronic equipment from electric shock and harmful noise.

To ground the PLC, connect a 12 to 16 gauge wire from the frame ground terminal strip screw of the controller to a high quality earth ground (less then 2 Ω). Since electrical currents always take the path of least resistance, the noise currents induced by a magnetic field will flow through the PLC frame ground terminal screw to earth ground. This essentially draws the noise away from the PLC modules.

The most effective method of grounding the PLC frame is to ground the PLC independent of other equipment. Avoid grounding the PLC through a daisy chain of wire connections with other equipment. See figures below for good and bad examples:



The length of the ground cable should not exceed 65 feet (20 m). For best results, the resistance of the ground cable should be less than 2 Ω.

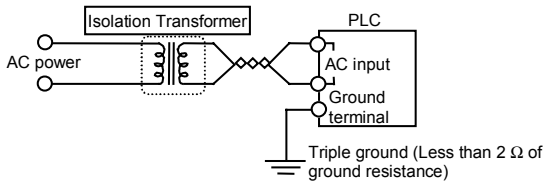
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Isolation and Filtering Techniques

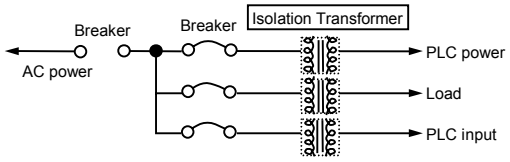
Isolation

There are several methods of isolation:

- Attach an isolation transformer between the PLC power supply and the VAC source to help remove noise that flows in the power cable. Try to attach the isolation transformer as near to the PLC power supply input terminal strip as possible.
- Some isolation transformers come with a shield that can be grounded. This shield, when properly grounded, enhances the transformers ability to remove unwanted spikes.
- Be certain to size the isolation transformer to handle the necessary power rating required by the system. A good practical rule in specifying an isolation transformer is to multiply the required load capability by 1.35 (35% additional deliverable power). This allows expansion of the PLC system at a later date without the immediate need to upgrade the isolation transformer.



- When heavy noise is expected, also use an isolation transformer on the AC control power to the I/O modules and devices. A cost-effective way of specifying the isolation transformer for this requirement would be to specify a transformer with multiple primary and secondary windings and wiring the PLC as shown below. Again, be certain to size the isolation transformer to handle the necessary power required plus a 35% surplus and additional windings to allow for future expansion of the system.



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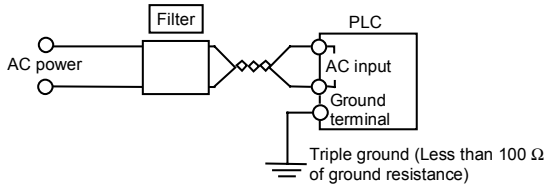
Filters

Filters should be used to suppress high frequency noise.

When using a low-pass filter specify one that is designed for power line applications. Many different types are available from simple modules to complex units.

A single device is not necessarily the most cost-effective device for all applications. In specifying the proper filter one must take into account the amplitude/power level of the noise and how often the noise is present.

When the proper device is selected it is best to place the device as close to the PLC power supply connections as possible. Below is an example of how to install a filter. The chart lists a typical midrange power line filter for reference.



For installation and application details, refer to the manufacturers manuals.

Model Name	Manufacturer	Remarks
PQI-3120N12	Superior Electric, DANA/ Warner Electric Division	Used for 120 V power
PQI-3220N12	Superior Electric, DANA/ Warner Electric Division	Used for 240 V power

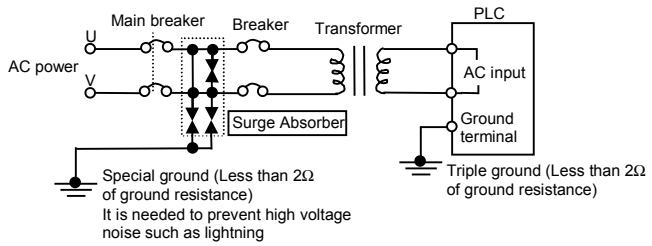
The PQI-3120N12 and PQI-3220N12 come in a NEMA 12 rated enclosure.

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Methods of Handling Large Voltage Spikes Such as Lightning

Surge Absorber

- A surge absorber reduces the electrical shock to the PLC by taking high-voltage spikes to ground. Attach a surge absorber in the power line in front of the PLC to prevent damage from lightning. The surge absorber will clamp the unwanted high voltage and prevent it from flowing to the PLC power supply. When specifying a surge absorber, the present wiring system must be carefully reviewed. Some surge absorbers are designed to be placed into the main power distribution panel while others are designed to be installed in the field close to the PLC. It is always best to place the surge absorber as close to the PLC as possible.
- Surge absorbers can consist of either series resistors with capacitors that will couple the spike to ground, or Zener diodes that safely clamp the high voltage spikes or MOVs (Metal Oxide Varistors). Some surge absorbers will need replacement after they have suppressed a spike (similar to a fuse). Others can be reset. In specifying a surge absorber consider how often the surges are occurring and the maximum amplitude in volts or joules.



Some typical surge absorbers are listed in the following table. For actual installation and application details, refer to manufacturers manuals**.**

Model Name	Specifications	Manufacturer	Remarks
CHSA	470 V	Cutler-Hammer	120/240 V power
CHSA01	490 V	Cutler-Hammer	120/240 V power

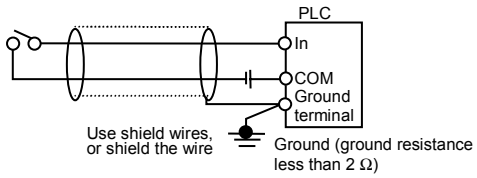
Burying Wire

- Cabling that is strung from pole to pole in free space is an antenna for lightning. When possible bury the cable underground. The earth acts like a shield and absorbs most if not all of the lightning induced noise signals before they are able to reach the cable.

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Shielding Cabling

- When the wiring for the I/O module is more than 165 ft (50 m), shield the wire by installing it in ferrous (steel) conduit and use shielded wire. Attach the conduit/shield to the ground at the PLC ground terminal as shown below.



- Separate the input and output module wiring, and power circuit cables. Make sure to properly ground the shields of each cable directly to ground. Do not create a daisy chain of ground jumpers over several feet and then pigtail one end lead to ground. This method allows multiple ground current paths to exist and can induce noise.

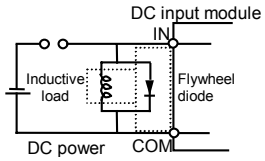
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Methods to Handle I/O Inductive Loads

Several methods exist for handling I/O inductive loads.

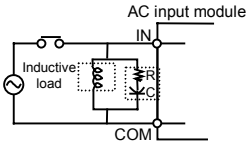
DC Input Module

Attach a diode in a reverse biased direction parallel to the inductive load, as close as possible to the load.



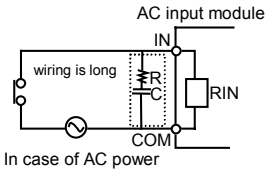
AC Input Module

Attach an RC network parallel to the inductive load.



Handling Long Cable Runs

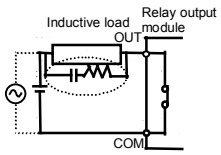
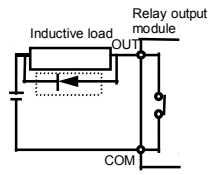
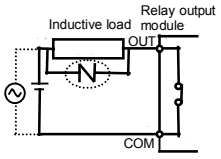
When a long cable run is needed to attach the AC input module to an external input device attach a surge suppressor parallel to the input module. When possible, convert the application so a DC input module can be used instead of the AC input module. The input circuitry of DC input modules inherently have filters that suppress noise and therefore are less affected by the noise from inductive loads and stray wiring capacitance.



Protecting Against Arcing

When a relay output module switches an inductive load, a surge voltage measured in thousands of volts is generated across the relay contacts. This causes arcing (an electrical discharge between two contact points that can vaporize the contact material) and shortens the contact life of the relay. Eventually this arcing can destroy the relay contacts. Below is a chart of some methods to protect the relay contacts.

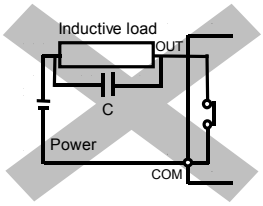
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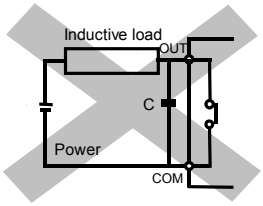
Countermeasures	Application		Characteristics	Selection of Parts
	AC Load	DC Load		
Attach a surge suppressor: 	○	○	If the load is a relay or a solenoid, the load is slow to return to the normal status. When using a DC power source, place the surge suppressor across the inductive load. When using an AC power source, place the surge suppressor across the switching relay contacts. The example shows how to connect the surge suppressor for a DC power source	For a contact voltage of 1 V and a contact current of 1 A, use the following C and R values: C: 0.5-1.0 μF R: 0.5-1.0 Ω Another example; for a contact current of 0.5 A and a contact voltage of 200 VAC use the following C and R values: C: 0.25-0.5 μF R: 100-200 Ω For DC circuits use a minimum of a 250 V rated capacitor. For AC circuits use a minimum of a 1000 V rated capacitor.
Attach a flyback diode: 	×	○	The diode connected in parallel allows the energy accumulated in the inductive load to flow back into the inductive load in the form of an electrical current. The energy is then dissipated as heat based on the resistance of the inductive load. The time required to return to the normal status is longer than the surge suppressor method.	Use diodes with low reverse leakage current and with a reverse voltage value that is at least three times greater than the nominal applied voltage. Verify the diode has the proper power rating. The steady state current that flows when the inductive load is turned on should be greater than the current produced when the inductive load is turned off.
Attach a varistor: 	○	○	A varistor functions as a voltage clamping device. When the applied voltage exceeds the rated voltage value of the varistor, the varistor turns on, creating a short circuit connection across the inductive load. This method has a slow recovery time. When using a DC power source, place the varistor across the inductive load. When using an AC power source, place the varistor across the switching relay contacts.	To specify the varistor do the following: Chose a maximum continuous voltage rating just above the expected applied voltage. Chose a varistor that can handle the energy level that will be generated by the inductive load BUT avoid overspecifying. As the varistors energy level capability goes up so does the capacitance which will slow down the response time of the system.

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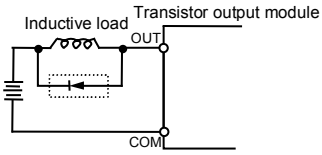
Warning

The following two protection methods should be avoided. Each of these methods can be effective in removing the sparks when power to the inductive load is turned off. However when power is turned on to the inductive load there will be a high inrush current applied across the relay contacts as they are mating. Since all relay contacts have some bounce while mating, arcing will occur and potentially melt the relay contact points. This is the reason for having the resistor in the RC network described earlier.

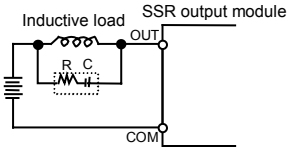




- Transistor Output Module—it is best to attach a flyback diode parallel to the inductive load, as close as possible to the load. In this configuration output switching frequency should be held to less than 20 times per minute.



- SSR Output Module—attach a surge suppressor parallel to the inductive load, as close as possible to the load. In this configuration output switching frequency should be held to less than 20 times per minute.



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Troubleshooting

- Noise from magnetic fields induced by other electrical/electronic equipment onto the PLC can be avoided by relocating the PLC during the design process, installing the PLC in a grounded steel enclosure, or attaching a filtering or suppression shield/circuit to the device which is generating the magnetic field.
- Noise from power cables can be corrected by using a different ground for the PLC, an isolation transformer, attaching a line/ground filter, or changing the power wire connection of the PLC so that it is closer to the source of the power, therefore lowering the power source impedance.
- Noise from lightning should be suppressed by use of surge suppressors that are specifically designed to protect electronic equipment from lightning.
- Whenever welding near an electronic device, care must be used to avoid connecting the ground cable of the welder to a ground of the electronic device. One method of protecting the PLC is to disconnect the PLC from power and lifting all power and ground connection. An alternate method is to establish two separate grounds, one for electronic equipment and one for welding. Test the ground separation carefully before having electronic equipment up and running while welding.
- The quickest way to avoid noise from shared cable trays is to have two cable tray runs. One for power and power control cabling and the other for electronic equipment and low level control wiring. Proper cable selection with good shielding properties in some instances will allow both types of cabling/wiring to co-exist in the same tray system.
- “Grandfather’d” plant wiring has to be analyzed on a case by case basis. The best approach is to always install new cabling, conduit, and cable tray runs. Though this may not always be practical, it removes the surprise of high noise and system problems during system startup.
- Static electricity suppression requires good grounding practices throughout the plant. Static electricity is a potential difference developed on a material surface due to the loss of protons or electrons. Since rubbing action can cause the build up of static electricity, the best protection is to have the electronic equipment enclosed in a grounded housing that requires the user to first make contact with a safe discharge path. In high static environments like styrofoam manufacturing or glass manufacturing, electronic equipment should always be protected from static electricity.



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Appendix A: D50 PLC Communication Protocol

A

The D50 PLC communication protocol provides a simple, yet complete method of communications between the Cutler-Hammer program loader software (GPC) and the PLC. Using the open protocol outlined in this appendix, the user can quickly and easily expand the capabilities of the overall PLC system by communicating to the PLC using a variety of peripheral communications equipment such as operator interfaces and computers. Additionally, the communications protocol allows for multiple Cutler-Hammer D50, D300, and D320 PLC's to communicate to a central computer on a single network using RS-485, at distances of up to 4000 ft (1.2 km).

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Communication Rules

Communication Environment

The D50 PLC communications protocol uses the following settings:

- Half Duplex Asynchronous
- No Parity
- 1 Stop bit
- Communication method: RS485
- Communication speed: 9600 bps
- Number of PLCs on a single network: Maximum of 32 (communicating 1:N using RS485)
- Maximum communication delay time: 3 sec

Communication Protocol

Step 1—Query (Q)

Set the network ID number for the PLC to communicate with and send a Q signal from the peripheral device to the PLC.

Step 2—Query Acknowledge (QA)

A QA signal is sent from the PLC to the peripheral device, indicating that the Q signal from the peripheral device was received.

Step 3—Response Request (RR)

An RR signal goes from the peripheral device to the PLC, indicating that the QA signal from the PLC was received, and requesting the final data response. This signal is sent when Q→QA is normal.

Step 4—Response (R)

When the PLC receives the RR from the peripheral device, it sends an R signal which gives the results of the original Q signal sent by the peripheral device. The communication cycle for one function code ends when the PLC sends the R.



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Step 5—Repeated Response

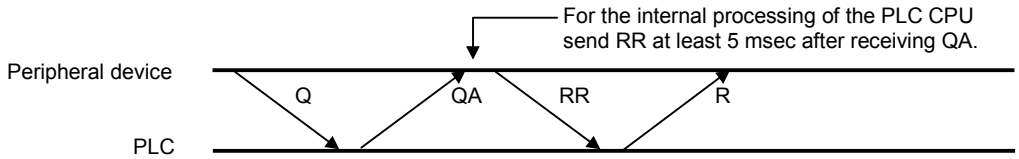
Once the original Q has been sent to the D50 PLC, the R message containing the requested data for that query can be repeatedly received by sending only the RR message again.

Communications Delay

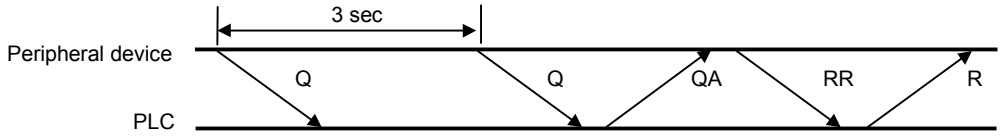
The D50 PLC will return a signal after receiving a Q or an RR within a specific time. However, due to errors in the communications network, CRC values, and communication speed flux, there are occasions when the PLC will not receive the signal from the peripheral device. The peripheral device should allow up to three seconds for a response from the PLC. If there are no responses to the Q or the RR message, the communication is considered to have failed, and the Q or RR should be sent again.

Example

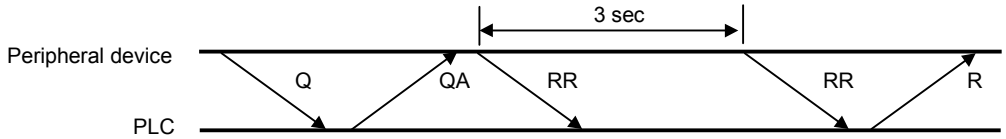
1. No communication error.



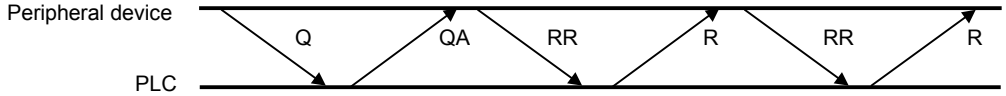
2. When QA is not received.



3. When R is not received.



4. Repeated Response communications.



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CPU ID

All devices connected to the network need a network ID number for communication. There is an available range of 0 to 191 network ID numbers. Redundancy is not permitted. When a single PLC and a peripheral device are connected, usually 0, 1, or 255 is assigned as the network ID number to the PLC. When the peripheral device wishes to communicate to a connected PLC regardless of its programmed network ID number, it can use global network ID number 255, to which any PLC will respond. When several CPU modules are connected to one communication network, they must use individual ID numbers from 0 to 191. The PLC's network ID number is configured using the GPC program loader software.

Function Codes Included in the Query

- Each function code is 1 byte. When the PLC receives a query (Q), the function code of the final response (R) is formed by adding $80 (hex) to the function code sent by the query.
- The function code of the R message can be used by the peripheral device to verify that the correct Q message has been received by the PLC.

Communication function
* $ notes hexadecimal notations

Communication Function	Query Function Code	Response Function Code
Read Bits	$01	$81
Write Bits	$02	$82
Read Words	$03	$83
Write Words	$04	$84
Read Bits and Words	$05	$85
Write Bits and Words	$06	$86
Read Program	$07	$87
Write Program	$08	$88
Read Instruction	$09	$89
Change Instruction	$0A	$8A
Change Parameter	$0B	$8B
Insert Instruction	$0C	$8C
Delete Instruction	$0D	$8D
Find Instruction	$0E	$8E
Find Parameter	$0F	$8F
Delete Section	$10	$90
No Service	$00	$00

Note: Function codes $07 to $10 are used for programming and system control functions, and are beyond the scope of this manual. Please contact Cutler-Hammer technical support for more information.

Note: The bit/word address assignment uses the absolute address method for reading memory locations. (See Chapter 5 for memory map.)

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Cyclic Redundancy Checking (CRC)

- The CRC is a 2-byte checksum that is calculated from the data of every message and then attached to the end of the message by the sender. It is used as an error-checking device to prevent loss or corruption of data during transmission of the message.
- The sender of the message calculates and attaches the CRC when it generates and sends the message. The receiver should also calculate the CRC from the data of the message and compare the calculated value to the CRC that was sent. If the calculated CRC does not match the CRC received, an error has occurred in the message during transmission.

CRC Calculation Range



The following subroutines illustrate the program code required to calculate the CRC for a message. The initial value of the CRC (CRC_Sum) is set to 65535 ($FFFF). Then one of these subroutines would be called once for each byte (data) of the CRC calculation range shown above.

CRC-16 Calculation Subroutine (BASIC)

```
        CRC_Sum: CRC-16 reserve code after the calculation (CRC content to be sent at end of message)
        Data: CRC-16 Data input to be calculated (Byte Data from message)
1000    CRC_Sum = CRC_Sum XOR Data
1010    FOR I=1 to 8
1020    CARRY=CRC_Sum AND 1
1030    CRC_Sum=CRC_Sum SHR 1
1040    IF CARRY=1 THEN CRC_Sum XOR 0A001H
1050    NEXT I
1060    RETURN
```

CRC-16 Calculation Subroutine (PASCAL)

```
Procedure CRC16(Data : Byte)
    Var i : Byte;
Begin
    CRC_Sum := CRC_Sum x or Data;
    for i : 1 to 8 do
    begin
        if((CRC_Sum and 1)=1) then CRC_Sum := (CRC_Sum shr 1) xor $A001;
                              else CRC_Sum := CRC_Sum shr 1;
    end;
End;
```

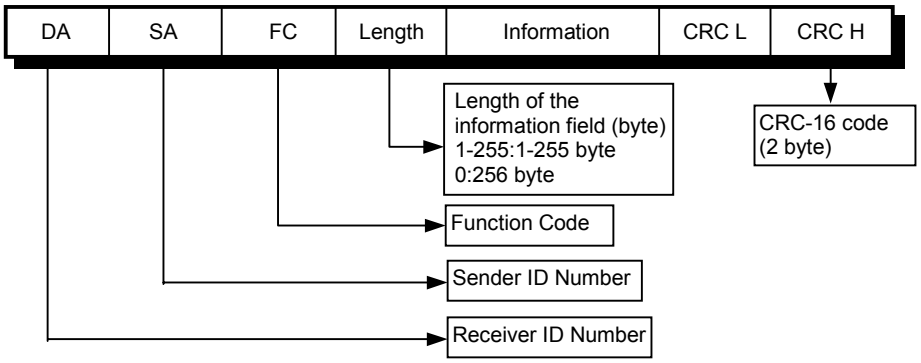
CRC-16 Calculation Subroutine (C)

```
void Crc16(unsigned int Data) {
    unsigned int i;
    Crc=Crc^(Data & 0x00FF);
    for(i=0;i<=7;I++) {
        if((Crc & 0x0001) == 0x0001) Crc=(Crc>>1)^0xA001;
        else Crc=Crc>>1;
    }
 }
```

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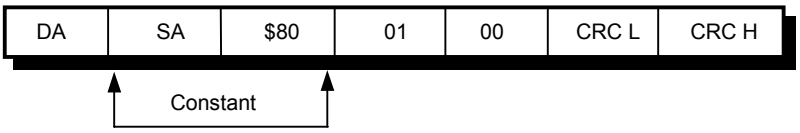
The Structure of the Communications Frame

Query and Response Frame

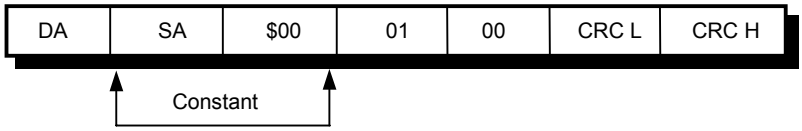


The frame is sent from the source address (SA) by the sender to the destination address (DA), the receiving device. For the query (Q) and the response request (RR), the SA is the address of the peripheral device, and the DA is the address of the PLC to which the message is being sent. For the query answer (QA) and the response (R), the PLC becomes the sender of the message, and so the PLC address is the SA and the peripheral device's address is the DA.

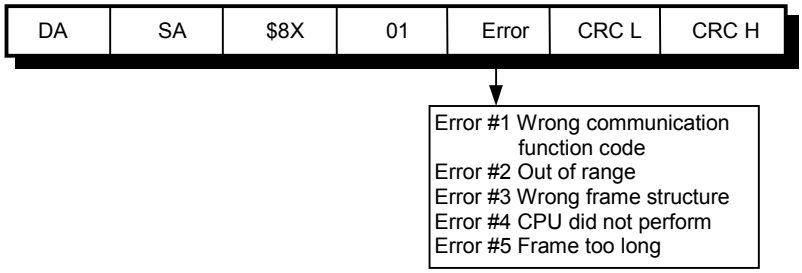
Query Acknowledge Frame



Response Request Frame



Response Frame for an Error



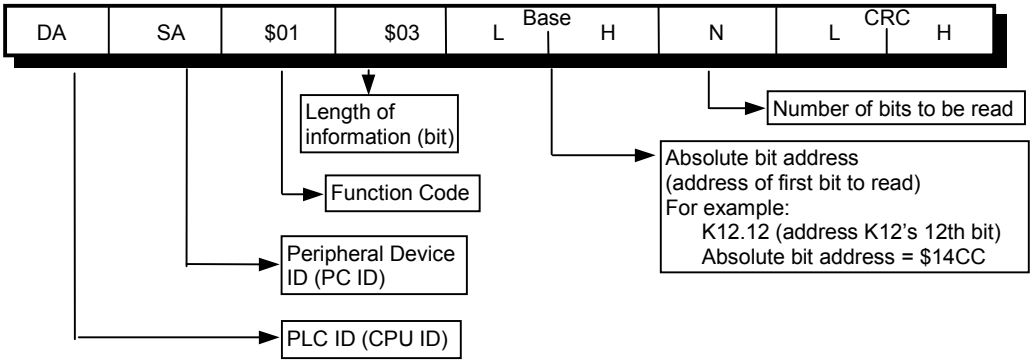
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Read Bits

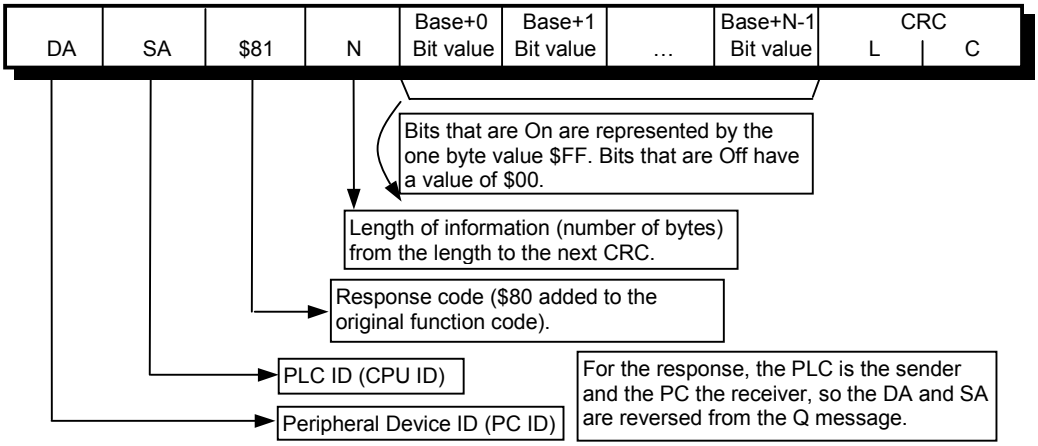
The following can be read:

- Bits stored in the absolute address (R, L, M, K, or F).
- N consecutive bit contents (On/Off).

Query (Q) frame



Response (R) Frame



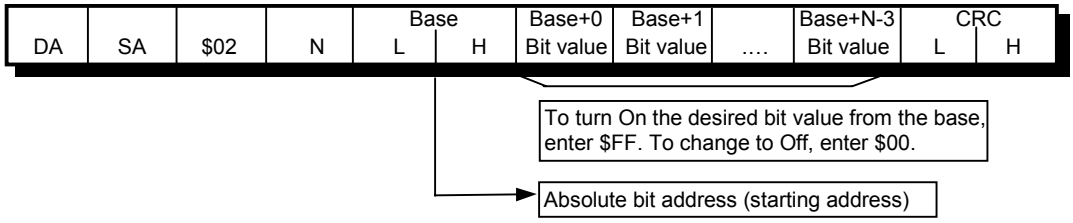
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Write Bits

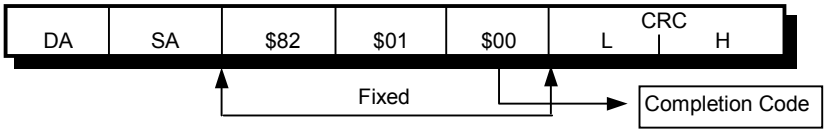
Writing bits allows you to:

- Modify the contents of the bits stored in the absolute address (R, L, M, K, or F).
- Change the bit state between On/Off.
- Change multiple consecutive bytes.

Query (Q) Frame



Response (R) Frame

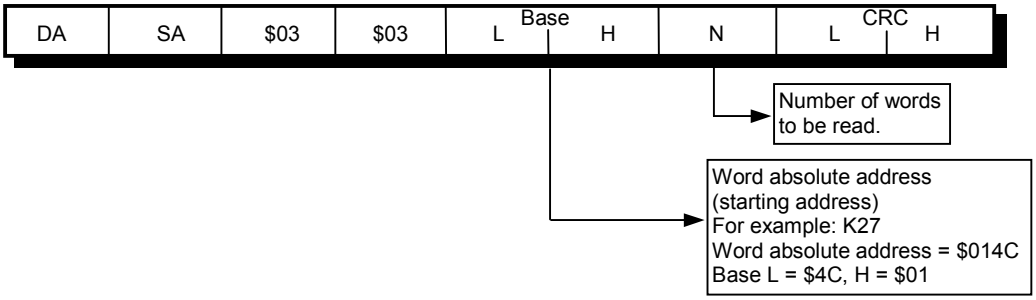


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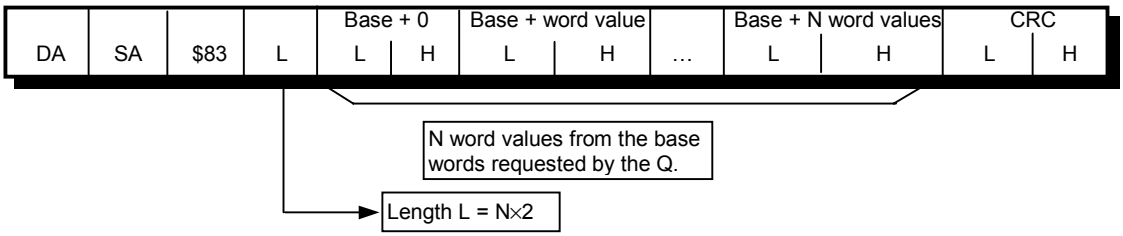
Read Words

- Read the content of the words (R, L, M, K, F, or W) assigned to the absolute address.
- Read n consecutive words.

Query (Q) Frame



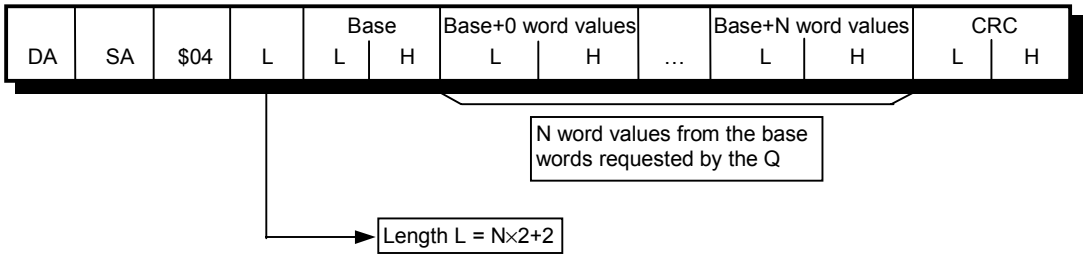
Response (R) Frame



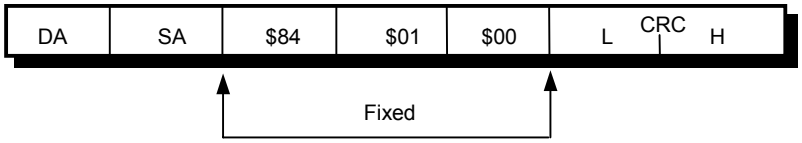
Write Words

- Changes the content of the words assigned to the absolute address (R, L, M, K, F, or W).
- Can change n consecutive word contents.

Query (Q) Frame



Response (R) Frame

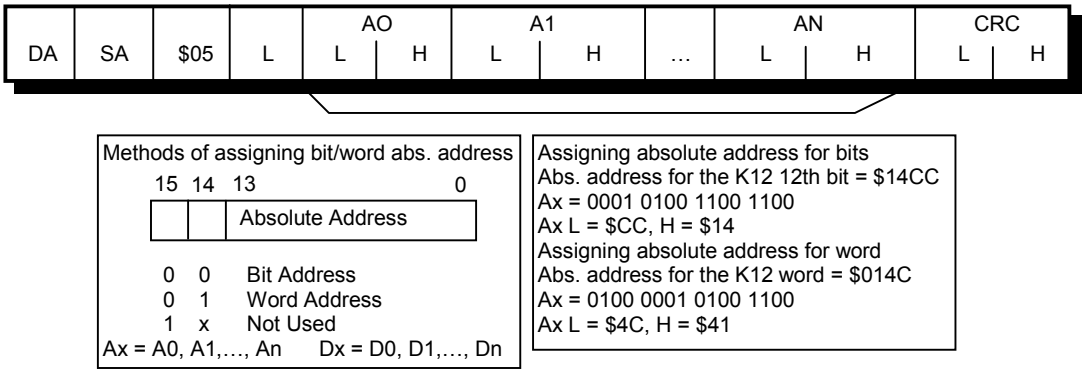


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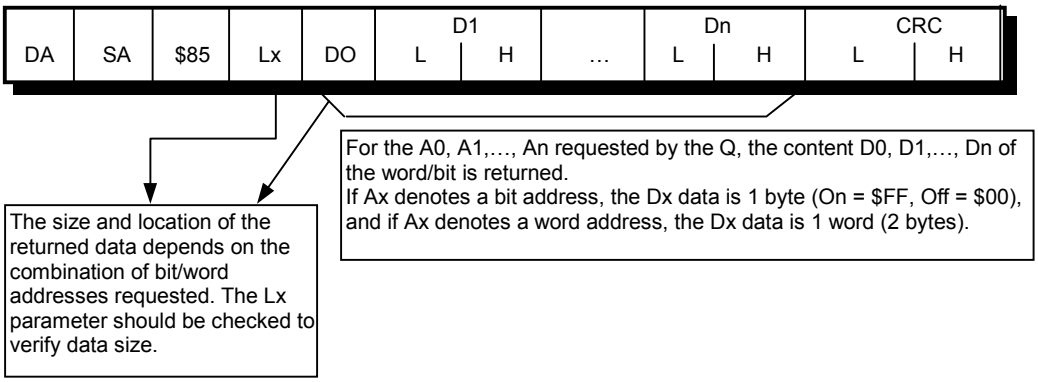
Read Bits and Words

- Reads the bits and/or word contents of the specified absolute addresses.
- Can read bits and words regardless of their order and location in memory.

Query (Q) Frame



Response (R) Frame

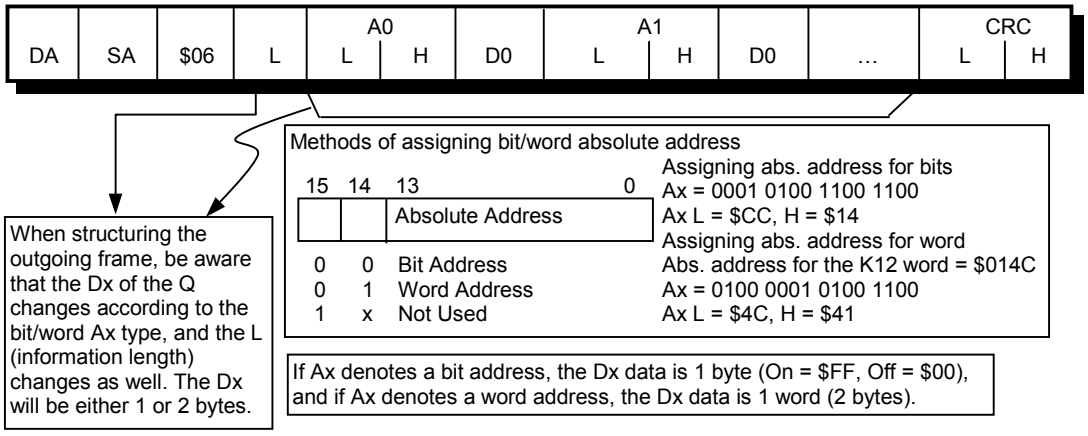


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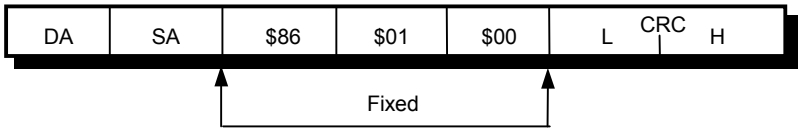
Write Bits and Words

- Changes the content of the bits or words at the specified absolute addresses.
- Words and bits may be modified regardless of their order and location in memory.

Query (Q) Frame



Response (R) Frame



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Communication Program Example

The following program is an example program written in C code to demonstrate the D50 PLC open communications protocol. This program consists of a header, the main program, and various subroutines. The buffers and a few variables needed to store the communication data are set as global variables, so that the main function and the various functions may have access. Notes are provided alongside the main program to help explain the exact purpose and function of the individual parts of the program. This particular program was written for the Cutler-Hammer D320 PLC, and so uses register addresses beyond the D50 limits. For use with a D50, adjust the register addresses used in this program (M000 to M127 and K000 to K127) to within the D50 range.

Note: This program is provided for illustrative purposes only. It is left to the responsibility of the user/programmer to ensure that any programs written based on, and using the information contained in this program, satisfy the requirements of their particular application.

Program	Notes
#include <stdio.h> #include <stdlib.h> #include <dos.h> #include <conio.h>	This program was written in Borland C++. It uses the peripheral device (PC) to read the M000 to M127 words, and stores them in the K000 to K127, and then compares the two registry values and indicates the results on the screen using the OK or the FAIL notation. The user may read or manipulate the various communication function codes and the information sent to control the PLC in various ways.
#define PC_ID 0xE2 #define Time_limit 28 #define retrial_limit 2 #define TRUE 1 #define FALSE 0 #define lower_byte(x) (unsigned int) ((x)& 0x00FF) #define upper_byte(x) (unsigned int) (((x)& 0xFF00)>>8)	This program consists of a header, the main program and various functions. The buffers and variables needed to store the communication data are set as global variables, so that the main and various other functions may reference them.
typedef int BOOL; unsigned int PORTADD,DIVISOR,sending_delay, receiving_delay; unsigned int sending_frame[262],receiving_frame[262]; unsigned int Crc; unsigned int card,i,ix,iy,smode; unsigned int port_number; unsigned int PlcID,OldID; BOOL Success; unsigned int data,JobID,retrialC; unsigned int Old,New,receiving_Index_max,sending_Index_max,index,watchdog; unsigned int M[128],K[128]; /* Example Register */	By using the COM1 and COM2 ports of the computer, serial communication is possible. By using the GPU-300 card, parallel communication is also enabled (NOTE: The GPU-300 card is not currently offered by Cutler-Hammer).
void RR_occurring(void); void Trsport(unsigned int); unsigned int Recport(void); BOOL sending_occurring(void); BOOL receiving_occurring(void); void Crc16(unsigned int); void Job(void); unsigned int communication(void); void Mword_reading(void); void Kword_writing(void);	The Qs, QAs, RRs, Rs are handled in the job functions. If there are communication errors or a frame breakdown, retry 3 times, then issue a communication error. The procedure of the communication, according to the JobID is: 1. Q sending 2. QA receiving 3. RR sending 4. R receiving When an error occurs in a frame, a retransmission should be made. **Major operations of the program**

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	1. Adjusts the initial communication port and the board rate for communication. Then initializes the variables. 2. Using the communication function codes, reads the data of the M field, reads the word values of the M0 to M127 area and stores them in the K0 to K127 word area. The K registers are the retentive registers. 3. Uses the communication code to read the data of the K area. 4. Compares the values of the M area and the values of the K area, and indicates OK when the values are the same.
void main(void) { unsigned int i; /* Selection of communication port */ clrscr(); printf("PORT : COM1[1]/ COM[2]/ GPC-232[3]/GPC-485[4]/ GPC-Parallel[5] = "); scanf("%d",&port_number); if ((port_number < 1) || (port_number > 5)) port_number=5; /* Selection of Baudrate for Serial communication */ sending_delay=10; if (port_number != 5) { printf("GPC «å BAUD-RATE : 9600[1]/ 4800[2]/ 2400[3] = "); scanf("%d",&i); if ((i < 1) || (i > 3)) i=1; if (i == 3) i=4; if ((port_number == 1) || (port_number == 2)) DIVISOR=12 * i; else DIVISOR=40 * i; receiving_delay=3 * i + 1; }	**Beginning of the main program** Select the port of the peripheral device for the communication: Serial 9 PIN, 25PIN Parallel GPU-300 parallel port Select board rate: 9600 bps (max) 4800 bps 2400 bps Set the communication environment (delay time) for the selected ports.
/* Initialization of GPC card */ if(port_number == 1) PORTADD=0x3F0; if(port_number == 2) PORTADD=0x2F0; if ((port_number >= 3) && (port_number <=5)) { PORTADD=0x300; outportb(0x303,0xC0);/* Mode=2 of 8255 */ outportb(0x303,0x05);/* PC2=1 of 8255 :Disable IRQ2 */ outportb(0x301,0xFF);/* PB0=1 of 8255 :sending Enable RS-485*/ outportb(0x303,0x01);/* PC0=1 of 8255 :Serial Input Enable*/ if(port_number == 3) outportb(0x303,0x02);/* PC1=0 of 8255 :Select RS-232 */ if(port_number == 4) outportb(0x303,0x03);/* PC1=1 of 8255 :Select RS-485 */ if(port_number == 5) outportb(0x303,0x00);/* PC0=0 of 8255 :Disable SerialInput*/ } else outportb(PORTADD+0x09,(inportb(PORTADD+0x09)&0xF0));/*Disable Interrupt*/ /* Initialization of USART-Chip : 8250 */ if (port_number != 5) { outportb(PORTADD+0x0B,0x80);/* Set of DLAB=1 */ outportb(PORTADD+0x09,0x00);/* Set of High Byte DIVISOR */ outportb(PORTADD+0x08,DIVISOR);/* Set of Low Byte DIVISOR */ outportb(PORTADD+0x0B,0x03); /* parity=None/Stop=1/ Length=8 */ } /* Processing communication of Read & Write */ for(; ;) {	**GPC-300 card Setting (8255chip setting):** Uses the communication card that is connected, and sets the environment according to the PLC communication spec., so that communication is possible. Not currently offered by Cutler Hammer.

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printf("----------\nPLC-ID (CPU ID) :"); scanf("%d",&PlcID); if(PlcID<256) { Mword_reading(); Kword_writing(); } else exit(0); } }	CPU-ID: Input PLC ID (0 to 255) Read the register value for the M area (M0 to M127) Store the value for the M area in the K area (K0 to K127)
void RR_occurring(void) { receiving_frame[2]=0; receiving_frame[3]=1; receiving_frame[4]=0; }	RR (Request Response) request function.
void Trsport(unsigned int data) { if (port_number == 5) outportb(PORTADD,data); else outportb(PORTADD+0x08,data); }	Sends data to the communication port.
unsigned int Recport(void) { unsigned int dt; if (port_number == 5) dt=inportb(PORTADD); else dt=inportb(PORTADD+0x08); return(dt); }	Reads the received data from the communication port.
BOOL sending_occurring(void) { BOOL tf; if (port_number == 5) tf=((inportb(PORTADD+0x02) & 0x80)==0x80); else tf=((inportb(PORTADD+0x0D) & 0x20)==0x20); return(tf); }	Outputs the data when a send event occurs.
BOOL receiving_occurring(void) { BOOL rf; if (port_number == 5) rf=((inportb(PORTADD+0x02) & 0x20)==0x20); else rf=((inportb(PORTADD+0x0D) & 0x01)==0x01); return(rf); }	Inputs the data when a Receive event occurs.
void Crc16(unsigned int data) { unsigned int i; Crc=Crc^(data & 0x00FF); for(i=0;i<=7;i++) { if((Crc & 0x0001) == 0x0001) Crc=(Crc>>1)^0xA001; /* 0x0001 : mult-nominal expression */ else Crc=Crc>>1; } }	**CRC Calculation**: Encodes the communication data in the byte stream. When one communication function is complete, it is attached to the most recent frame, or is compared with the attached CRC to check for data errors.
void Job(void) { /* JobID=0 : Change to sending-Mode for Serial port */ /* JobID=1 : Transmit sending-Frame */ /* JobID=2 : Change to receiving-Mode for Serial port */ /* JobID=3 : Address Polling of ACK from CPU */ /* JobID=4 : Receive ACK from CPU */ /* JobID=5 : Change to sending-Mode for Serial port */ /* JobID=6 : Transmit RR-Frame */	**Communication sequence functions**: Job ID=0~4 Q,QA Frame handling Job ID=5~9 RA,R Frame handling

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```
/* JobID=7  : Change to receiving-Mode for Serial port */
/* JobID=8  : Address Polling of RES from CPU   */
/* JobID=9  : Receive RES from CPU              */
/* JobID=10 : Success communication Processing  */
switch(JobID)
{
case 0: case 5:if (port_number != 5)
{
if (port_number == 4) outportb(0x301,0xFF);
else outportb(PORTADD+0x0C,(inportb(PORTADD+0x0C) | 0x02));
delay(sending_delay);
}
if (JobID == 5) RR_occurring();
watchdog=0; index=0; sending_Index_max=5; Crc=0xFFFF; JobID++;
break;
case 1: case 6:if (receiving_occurring()) data=Recport();
if (sending_occurring())
{
if (index<sending_Index_max-1)
{
Trsport(receiving_frame[index]);
Crc16(receiving_frame[index]);
if (index==3)
{
if (receiving_frame[3]==0) sending_Index_max=256+5;
else sending_Index_max=receiving_frame[3]+5;
}
}
else if (index==sending_Index_max-1)
{
receiving_frame[index]=lower_byte(Crc);
Trsport(receiving_frame[index]);
}
else if (index==sending_Index_max)
{
receiving_frame[index]=upper_byte(Crc);
Trsport(receiving_frame[index]); watchdog=0; JobID++;
}; index++;
}
break;
case 2: case 7:if (port_number != 5)
{
delay(receiving_delay);
if (port_number ==4) outportb(0x301,0x00);
else outportb(PORTADD+0x0C,(inportb(PORTADD+0x0C) & 0xFD));
}
JobID++;
break;
case 3:
case 8:if (receiving_occurring())
{
data=Recport();
if(data==PC_ID)
{
Crc=0xFFFF; index=1; receiving_Index_max=5;
receiving_frame[0]=data; Crc16(data); JobID++;
}
}
break;
case 4:
case 9:if(receiving_occurring())
{
if(index<receiving_Index_max-1)
{
receiving_frame[index]=Recport();
Crc16(receiving_frame[index]);
```

JobID 0,5:
A frame sends the data from the peripheral device to the PLC. It resets the watchdog and the CRC.
Use a delay after the send to avoid errors due to communications delays.

JobID 1,6:
Sends the Q and RR data.
When there are no errors, it resets the watchdog and proceeds on to the next sequence.

JobID=2,7:
A sequence that senses the sending of the QA and R data to the peripheral device after the completion of the functions that are received by the PLC from the previous frame.

JobID=3,8:
Handles the received data, and calculates the CRC of the received data.

JobID=4,9:
Stores the received data in the internal receivable buffer and compares the CRC value sent by the PLC to the calculated CRC value. It notifies the system that a successful communication is made when the two

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if(index==3) { if(receiving_frame[3]==0) receiving_Index_max=256+5; else receiving_Index_max=receiving_frame[3]+5; } } else if(index==receiving_Index_max-1) { receiving_frame[index]=Recport(); if(receiving_frame[index]!=lower_byte(Crc)) JobID=(JobID & 0x05); } else if(index==receiving_Index_max) { receiving_frame[index]=Recport(); if(receiving_frame[index]==upper_byte(Crc)) JobID++; else JobID=(JobID & 0x05); }; index++; } break; case 10:Success=TRUE; } }	values match, and proceeds on to the next sequence. JobID=10: Receiving
unsigned int communication(void) { struct time t; unsigned far *tm; int ret; Success=FALSE; receiving_frame[0]=PlcID;receiving_frame[1]=PC_ID; retrialC=retrial_limit; watchdog=0; JobID=0; index=0; sending_Index_max=5; Crc=0xFFFF; do { tm=(unsigned far *) 0x046C; New=*tm; Job(); if(watchdog>Time_limit) { watchdog=0; retrialC--; JobID=(JobID & 0x05); } if(!(((Old^New) & 0x02)==0)) { watchdog=watchdog+1; Old=New; } }while((retrialC!=0) && (Success==FALSE)); if(retrialC==0) ret=1; else ret=0; return(ret); }	If the frames that were sent have no response within 3 seconds, assumes it failed communication, and retransfers the data. The time from the sending and receiving is counted using the watchdog timer. Reset the watchdog timer when a retransfer is being made. No response after 3 retransmissions indicates a communication error. (Normal return value = 0, Abnormal return value = 1)
void Mword_reading(void) { /* Example of Read-Register */ int i; receiving_frame[2]=3;/* EXAMPLE READ WORD(M000-M0127) */ receiving_frame[3]=3;/* Number Of Byte For Information = 3 */ receiving_frame[4]=0xC0;/* BASE(M000=$00c0) */ receiving_frame[5]=0;/* BASE HIGH */ receiving_frame[6]=128;/* Number Of Byte M000-M127 */ if(communication() == 0) { printf("READ M0000-M0127 OK - "); for(i=0;i<=127;i++) M[i]=receiving_frame[i*2+4] +receiving_frame[i*2 +5]*256; }	**Reading Function of the register M.** Uses the communication function code number 3 (reading N consecutive words) to read the M area. Note: Sending frame[4] = The lower byte of the abs. address of the words to be read. Sending frame[5] = The upper byte of the abs. address of the word to be read. Abs. address of the M0 = 0x0C0

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else printf("communication error\n"); } void Kword_writing(void) { /* Example of Write-Register */ int i; receiving_frame[2]=4; /* EXAMPLE write WORD(K000-K063) */ receiving_frame[3]=130; /* Number Of Byte For Information */ receiving_frame[4]=0x40; /* BASE(K000=$0140) LOW */ receiving_frame[5]=1; /* BASE HIGH */ for(i=0;i<=63;i++) { receiving_frame[i*2 +6]= lower_byte(K[i]); receiving_frame[i*2 +7]= upper_byte(K[i]); } if(communication() == 0) printf("WRITE K0000-K0063 OK\n"); else printf("communication error\n"); receiving_frame[2]=4; /* EXAMPLE write WORD(K064-K0127) */ receiving_frame[3]=130; /* Number Of Byte For Information */ receiving_frame[4]=0x80; /* BASE(K000=$0180) LOW */ receiving_frame[5]=1; /* BASE HIGH */ for(i=0;i<=63;i++) { receiving_frame[i*2 +6]= lower_byte(K[i+64]); receiving_frame[i*2 +7]= upper_byte(K[i+64]); } if(communication() == 0) printf("WRITE K0064-K0127 OK\n"); else printf("communication error\n"); }	Note: Sending frame[6] = The number of words to be read. Sends a function code requesting to read the M area, and stores the received data in the buffer. **Writing Function of the K Register.** Uses the communication function code 4 (writing N consecutive words) to store the specified value in the K000 to K063 word. Note: Abs. address of K0 = 0x0140 **Writing Function of the K Register.** Uses the communication function code 4 (writing N consecutive words) to store the specified value in the K064 to K127 word. Note: Abs. address of K64 = 0x0180

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Appendix B: Special I/O Functions

B

The D50 PLC provides several special functions through the I/O built into the D50 controller. This appendix details the configuration and operation of the integrated special I/O functions, including the high-speed counters, pulse output, pulse catch input, and selectable input response delay.

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Overview

The D50 PLC provides several additional functions through the integrated I/O on the base unit. These special I/O functions expand the capabilities of the D50 PLC to allow for use in a variety of specialized applications. This appendix details those capabilities, and provides instructions on configuration, application, programming, and operation of the special I/O. Four types of advanced operation are available, as listed below.

Note: These special functions are only available on the controller units. They are not available through any of the digital expansion modules, only on the base module.

High Speed Counter

The D50 PLC provides two separate high-speed counter inputs. Each counter accepts 2 phase inputs to allow for up, down, up/down, quadrature, and ring count modes. The counters provide a 24-bit count for signals up to 10kHz (5kHz in 2-phase mode).

Configurable Input Response Delay

The eight inputs on the base unit can be configured to delay their response to an input signal. By programming a delay time on a digital input, input signals can be "de-bounced" to prevent false or multiple input signals where not desired.

Pulse Catch Input

In certain applications it is necessary to be able to detect a very high-speed, short duration pulse input. The Pulse Catch input will latch On for at least one scan any input signal of 150µsec or more.

Pulse Output

The D50 also provides one configurable output supporting two modes of pulse operation. The first mode allows the user to send out a configurable number of pulses, at a desired frequency (Pulse Mode). The second mode allows the user to set the output to continuous pulses at a given frequency, with a configurable duty cycle (PWM Mode).

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Special I/O Function Registers

To handle the requirements of configuration and operation of the special function I/O, the D50 provides 21 special I/O function registers. These registers are assigned to the various functions, and are programmed and edited by the user in the D50 PLC ladder program. The purpose of each individual register is outlined below.

Special I/O Function Registers

Register Address	Register Name	Special I/O Function	Description
R004	H0MODE	High-speed Counter Channel 0	Configuration register
R005	H0STRL		Low word of the 24-bit start value
R006	H0STRH		High word of the 24-bit start value
R007	H0ENDL		Low word of the 24-bit end value
R008	H0ENDH		High word of the 24-bit end value
R009	H0PVL		Low word of the 24-bit present value
R010	H0PVH		High word of the 24-bit present value
R011	PMODE	Pulse Output	Configuration register
R012	PFREQ		Pulse frequency (20Hz to 5kHz)
R013	PSV		Pulse start value/PWM Duty cycle
R014	PPV		Pulse present value
R019	H1MODE	High-speed Counter Channel 1	Configuration register
R020	H1STRL		Low word of the 24-bit start value
R021	H1STRH		High word of the 24-bit start value
R022	H1ENDL		Low word of the 24-bit end value
R023	H1ENDH		High word of the 24-bit end value
R024	H1PVL		Low word of the 24-bit present value
R025	H1PVH		High word of the 24-bit present value
R026	HFLAG	High-speed Counter	Comparison flags for both HSC channels
R027	FTIME	Input Delay	Delay time for digital inputs
R028	PCATCH	Pulse Catch	Configuration register for pulse catch inputs

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High Speed Counter

The D50 PLC provides two 24-bit, 10kHz high-speed counters (on the DC-input units only). Each of the two counters functions identically to the other. Each has a set of 7 registers allocated for its configuration and operation, plus an additional comparision register that they share. High-speed counter channel 0 uses registers R4 to R10, while channel 1 uses register R19 to R25. Register R26 is a shared comparison register that is used by both channels. The purpose of each register is described in greater detail below.

Register Descriptions

MODE (R004, R019)

The mode register is used to turn on the high-speed counter, configure which mode it will be operating in, and enable or disable the inputs used by the counter. Each bit in the low byte of the MODE register is used to turn On or Off a feature of the high-speed counter channel.

STR (R005/6, R020/21)

The STR registers are a pair of registers that the user places the START value for the counter channel into. When the register is configured for Ring Count Mode, or when the counter is reset using the Preset bit or the Preset input, the START value is loaded into the present value of the counter. Since the counter is a 24-bit value, two registers are required – the first holds the low 16 bits of the value, and the second holds the high 8 bits.

END (R007/8, R022/23)

The END registers are a pair of registers that hold the Set Value for the high-speed counter. When the present value is counting, bits are set in the comparison register that indicate when the counter is below, at, or above the END value (see FLAG below). The END value is also a 24-bit value requiring two registers, and is set by the user.

PV (R009/10, R024/25)

The PV registers are a pair of registers that hold the Present Value for the high-speed counter. The PV registers hold the actual counting value of the inputs coming into the PLC. Like STR and END, PV is a 24-bit value.

FLAG (R026)

The FLAG register provides comparison bits between the high-speed counter Present Values (PV) and End Values (END). Each counter channel has three bits in the FLAG register that indicate whether the PV is greater than (>), less than (<), or equal to (=) the END value. Since the equal to comparison is a latched bit, a fourth bit is provided to reset the = bit.

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Bit Registers

Three of the configuration registers used by the high-speed counters are bit registers – each bit in the register serves a different purpose. The three bit registers and the individual bit meanings are described in further detail below.

H0MODE – Mode Register R004

Bit #:	7	6	5	4	3	2	1	0	
Bit Name:	RUN	UD/2	RING	PRST	-	R2	R1	R0	**Description**
									Enable R0.0 as Up/Ph. A count input
									Enable R0.1 as Down/Ph. B count input
									Enable R0.2 as Preset input
									Not Used
									Preset Counter (STR → PV)
									Enable Ring Counter mode
									Enable Up/Down or 2-phase mode
									Run/Stop – Turn on Counter

H1MODE – Mode Register R019

Bit #:	7	6	5	4	3	2	1	0	
Bit Name:	RUN	UD/2	RING	PRST	-	R6	R5	R4	**Description**
									Enable R0.4 as Up/Ph. A count input
									Enable R0.5 as Down/Ph. B count input
									Enable R0.6 as Preset input
									Not Used
									Preset Counter (STR → PV)
									Enable Ring Counter mode
									Enable Up/Down or 2-phase mode
									Run/Stop – Turn on Counter

HFLAG – Comparison Register R026

Bit #:	7	6	5	4	3	2	1	0	
Bit Name:	EQ1D	GT1	LT1	EQ1	EQ0D	GT0	LT0	EQ0	**Description**
									PV = END on channel 0 (latched)
									PV < END on channel 0
									PV > END on channel 0
									Unlatch EQ0 bit (PV = END)
									PV = END on channel 1 (latched)
									PV < END on channel 1
									PV > END on channel 1
									Unlatch EQ1 bit (PV = END)

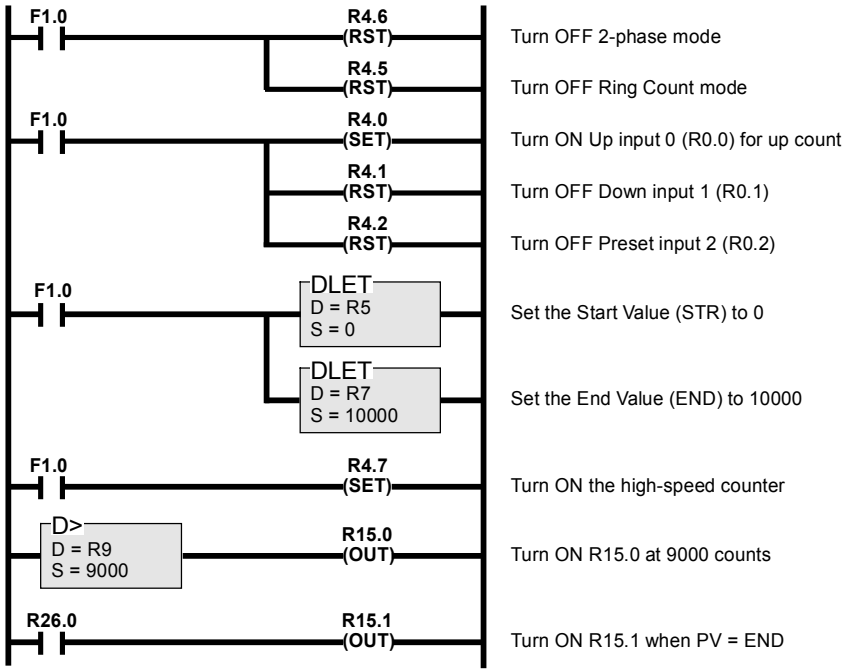
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Programming Procedure

The high-speed counter is very easy to use, and requires very little programming. The following steps outline the standard programming procedure to set up, turn on, and use the D50 high speed counter.

1. Configure the type of counter to be used by turning on the necessary mode bits in the MODE register. To set the counter up for 2-phase or Up/Down mode, set bit 6 (UD/2). To configure the counter as a ring counter, set bit 5 (RING). If the counter uses only a single input, and is not a ring counter, leave both bits off.
2. Enable the inputs required by the counter to count. On channel 0, set bit 0 (R0) of its MODE register R4 if the input on R0.0 will be a count input. Likewise set bit 1 (R1) if the input on R0.1 will be a count input (for example, for a down-counter or 2-phase counter). On channel 1, set bit 0 (R4) and bit 1 (R5) of its MODE register R19 based on which inputs, R0.4 and R0.5, will be used as count inputs. The Preset bits PRST are should be set if an external input will be used to reset the counter value.
3. Set the start value STR and the end value END for the counter, based on the application. The STR value will be used to reset the counter, while the END value is used by the comparison register HFLAG.
4. Turn on the counter channel. This is done simply by setting the RUN bit, bit 7, of the MODE register for that channel.
5. Use either the comparison register (HFLAG) or the D50 PLC's comparison instructions (>, <, =, >=, <=, <>) on the present value (PV) of the counter in the program, based on the application.

The following ladder program illustrates the above 5-step procedure for a simple counter application. For this example, a standard Up Counter is programmed, with an end value of 100. At the count of 9000, the program turns on the D50 PLC's first output R15.0, and at the count of 10000, the second PLC output R15.1 is turned on. Since this is an Up Counter, the first input of channel 0 is used to count input pulses.

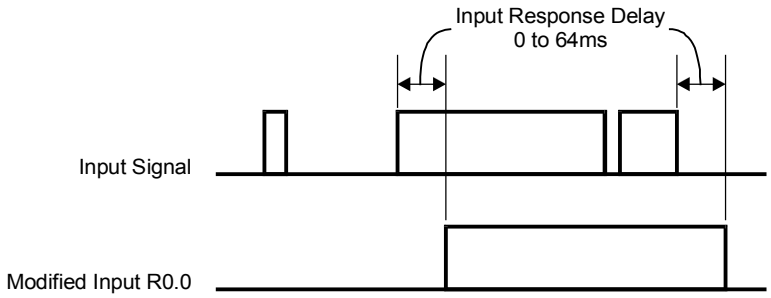


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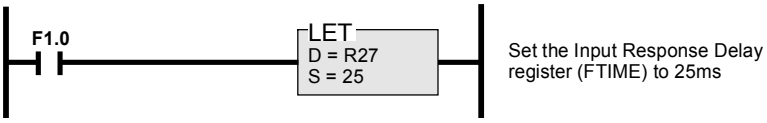
Configurable Input Response Delay

The special I/O function register FTIME (R27) controls the amount of time that an input must remain on before the input state is changed in the PLC I/O map. This amount of time is called the "Input Response Delay", and affects all eight inputs on the controller module (R0.0 to R0.7). This time is user-configurable from anywhere from 0 to 64ms in length. This allows the user to avoid false input signals due to contact bounce, input noise, or false signals of short duration. The delay is applied equally both to the turn On, and turn Off, of the input signal, as shown in the diagram below.

Note: Any of the eight inputs that are used for either high-speed counter or pulse catch are not affected by the Input Response Delay setting.



The Input Response Delay is automatically set for all the inputs when the new time value is loaded into the FTIME register, R27. The ladder example below illustrates setting the Input Response Delay time to a value of 25ms.

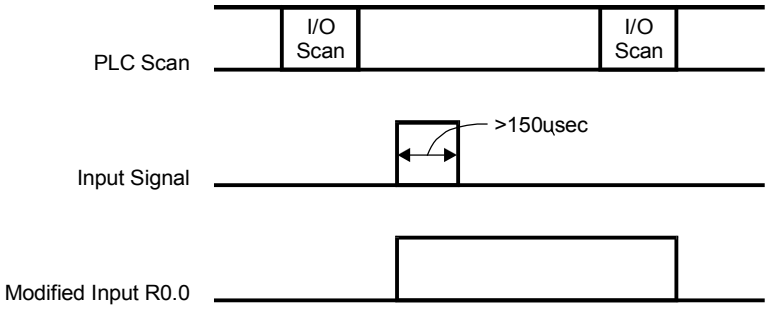


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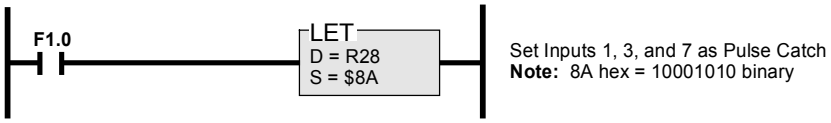
Pulse Catch Input

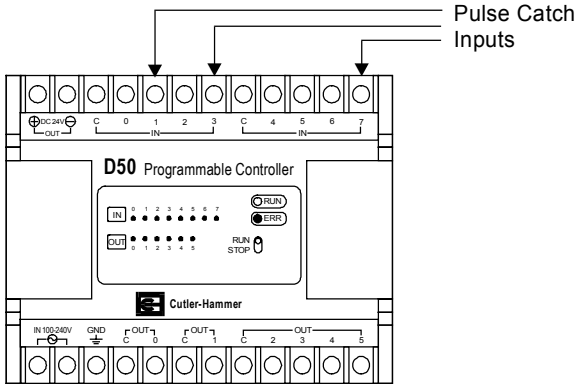
In many types of high-speed applications, such as products moving along a conveyor belt, the input signal to the PLC is of very short duration, often less than the scan time of the PLC. To allow the user program to detect those types of short-duration input signals, the D50 allows any or all of the digital inputs on the controller to be configured as "Pulse Catch" inputs.

When configured as a pulse catch input, any input signal of 150µsec or more is latched On for the next I/O scan. The input remains On for at lease one I/O scan, and turns Off on the next scan after the input signal has turned off.



The PCATCH special I/O function register determines which of the eight inputs on the controller are configured for pulse catch inputs, and which operate normally. Each bit in the PCATCH register R28 represents one of the eight inputs. If the bit is set On, then the corresponding input on the controller is configured as a pulse catch input. The logic required to set the PCATCH register R28 is shown below. In this example, inputs 1, 3, and 7 are set for Pulse Catch Inputs.





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Pulse Output

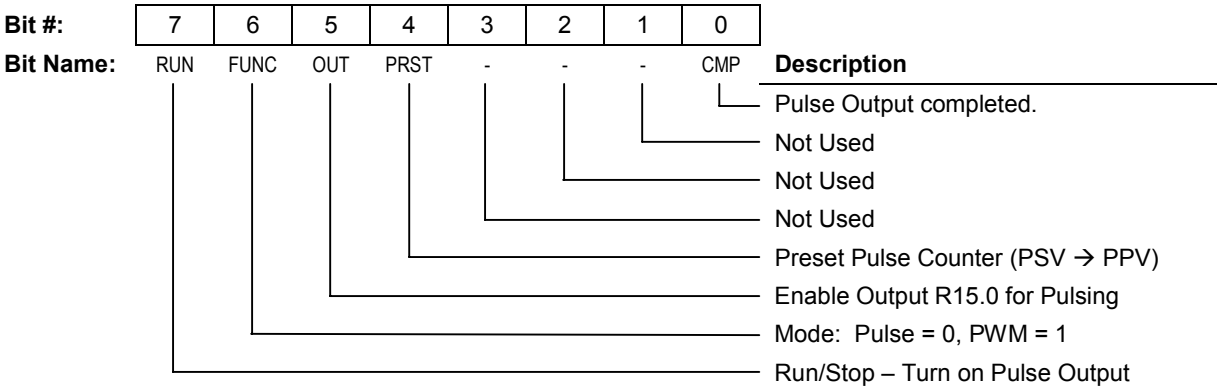
The D50 PLC provides two modes of Pulse Output on the first output contact of the controller. The first mode, Pulse Mode, sends out a given number of pulses at a user-defined frequency. The second mode, PWM (**P**ulse **W**idth **M**odulation) Mode, sends out a continuous stream of pulses, at a user-defined frequency and duty-cycle. Both modes use the same set of special I/O function registers (R11 to R14). The mode used by the D50 is determined by the configuration of the PMODE register, R11.

Register Descriptions

PMODE (R11)

The mode register is used to turn on the pulse output, configure which mode it will be operating in, enable the output used, and set up the pulse count. Each bit in the low byte of the PMODE register is used to turn On or Off a feature of the pulse output, as shown below.

PMODE – Mode Register R011



PFREQ (R012)

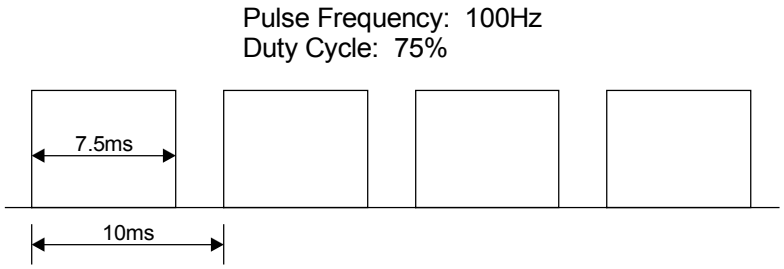
The PFREQ register sets the Pulse Frequency, from 20Hz to 5kHz, of the output. Whether in Pulse Mode, or PWM Mode, the output pulses will be sent at this rate.

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PSV (R013)

The PSV register is defined by the Mode of operation. In Pulse Mode, the PSV register holds the total number of Pulses to be sent out, from 0 to 65,535. When set to 0, the pulse output is continuous. In PWM Mode, the PSV register holds the duty cycle of the pulse, from 0 to 100%.

The Duty Cycle of the pulse is defined as the width of the pulse, from 0 (no pulse) to 100% (constant On). For example, a 100Hz pulse will generate 100 pulses every second, or 1 pulse every 10ms. If the duty cycle of the pulse is 75%, the pulse is ON for 75% of that 10ms, or for 7.5ms. It is OFF for the remaining 25%, or 2.5ms. This is illustrated by the diagram below.



PPV (R014)

The PPV register holds the Present Value of the Pulse Output when in Pulse Mode. The Present value counts down from the initial value, set by the PSV register. When the PPV register reaches 0, the pulses stop. In PWM Mode, the PPV register should always be 0.

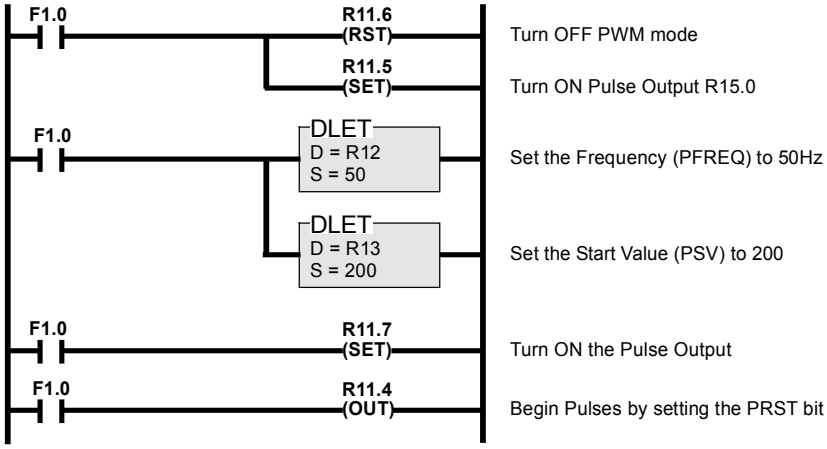
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Pulse Mode Programming Procedure

Programming the pulse output for Pulse Mode is a very simple procedure. The following steps allow the user to set the pulse output to send out the exact number of pulses required by the application.

1. Configure the pulse output for Pulse Mode by turning Off bit 6 of the PMODE register R11.
2. Enable the pulse output R15.0 by turning On bit 5 of the PMODE register R11.
3. Set the Pulse Frequency PFREQ (R12) for the pulses to be sent out.
4. Set the initial Pulse Value PSV (R13) for the total number of pulses to be sent out.
5. Turn on the Pulse Output by turning On bit 7 of the PMODE register R11.
6. Begin the Pulse Output by turning on the Preset bit (bit 4) of the PMODE register R11. This will move the total number of pulses into the Present Value register, and begin pulsing the outputs.

The following ladder program illustrates the above procedure by configuring a Pulse Output on the D50 PLC. The Pulse Output is set to send out exactly 200 pulses at a frequency of 50Hz, when the PLC is first placed into RUN.



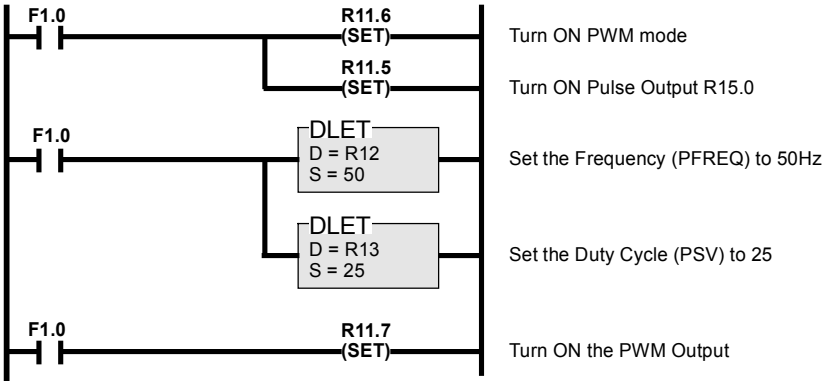
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PWM Mode Programming Procedure

Programming the PWM Mode is similar to the Pulse Mode. Rather than setting an initial value and triggering the PRST bit, the PWM mode simply requires the user to set the Frequency and Duty cycle. The following procedure should be followed to properly set and use the PWM Mode.

1. Configure the pulse output for PWM Mode by turning On bit 6 of the PMODE register R11.
2. Enable the pulse output R15.0 by turning On bit 5 of the PMODE register R11.
3. Set the Pulse Frequency PFREQ (R12) for the pulses to be sent out.
4. Set the Pulse Duty Cycle PSV (R13) for the width of the pulses, from 0 to 100%.
5. Turn on the Pulse Output by turning On bit 7 of the PMODE register R11.

The following ladder program illustrates the above procedure by configuring a PWM Output on the D50 PLC. The PWM Output is set to continuously send out pulses at a frequency of 50Hz and a duty cycle of 25%, when the PLC is first placed into RUN.



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Appendix C: D50PGM10 Pocket Editor

C

The D50PGM10 pocket editor provides a simple, convenient method of troubleshooting, monitoring and editing a D50 PLC on the shop floor. This appendix describes in detail the various functions of the pocket editor, and how to use them.

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Overview

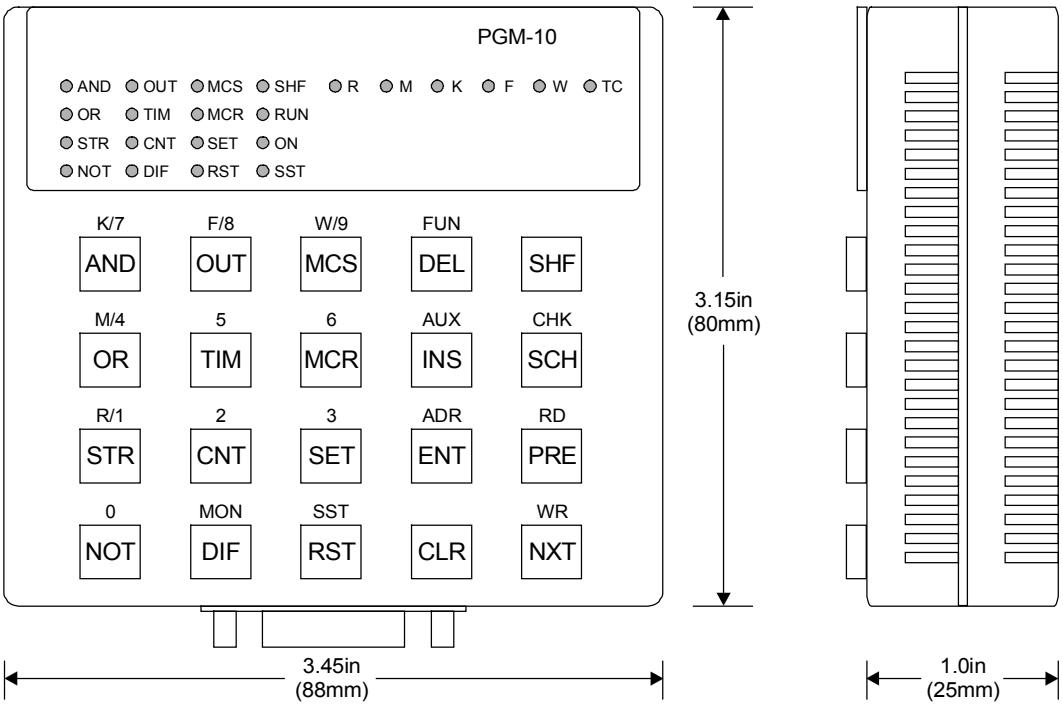
This appendix describes in detail the use of the D50PGM10 pocket editor for programming, monitoring, and troubleshooting the D50 PLC. The Pocket Editor provides mnemonic-only program loader support for the D50 PLC in a heavy-duty, light-weight industrial package. The various functions of the pocket editor are presented in a step-by-step procedural guide to simplify the use and operation of the editor.

Specifications

Operating Specifications

Item		Specification
Supported PLCs		D50
Power Supply		5VDC supplied from connected PLC
Display	Indicator	LED's and 7-segment display
	Capacity	22 LEDs; 5-digit 7-segment display
Keypad		20-key multifunction keypad

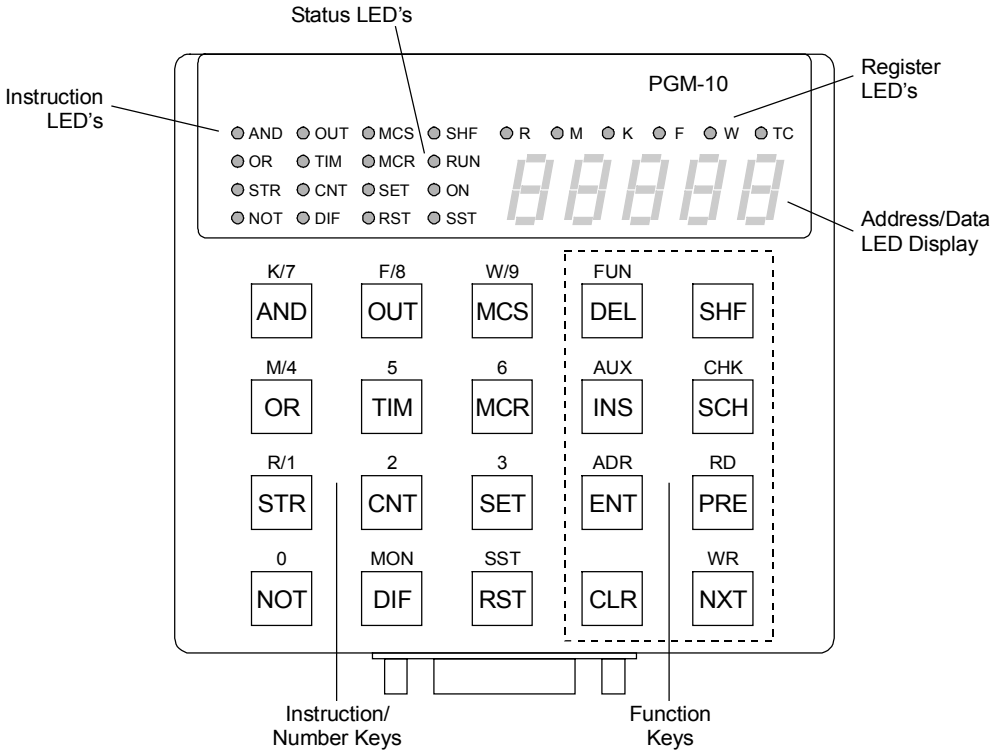
Dimensions



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Part Descriptions

The pocket editor is comprised of 13 Instruction LED's, 3 Status LED's, 6 Register LED's, a 5-digit Address/Data LED Display, and 20 keys that operate as instruction keys, number keys, and function keys. The diagram below points out the individual features of the pocket editor.



Instruction LED's

The instruction LED's are illuminated to indicate the basic instruction for a given step of the mnemonic program. When displaying a step in the program, one or more of these LED's will be lit.

Status LED's

The three status LED's on the pocket editor are the SHF, ON, and RUN LED's in the center.

- The SHF LED provides visual feedback that the user has pressed the shift (SHF) key.
- The RUN LED indicates when the D50 PLC is in the RUN mode.
- The ON LED indicates when a given contact or output point is turned On, when monitoring and instruction or bit register.

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Register LED's

The six register LED's indicate which address type is being displayed, when displaying a data value or address. The possible register types are R for external I/O, M for internal contacts, K for internal retentive (Keep) contacts, F for system flags, W for data words, and TC for timer/counter done contacts.

Address/Data LED Display

The address/data LED display is a 5-digit 7-segment display capable of showing numerical and character data. The display is used to show data values, register addresses, and step addresses.

- A 5-digit value is displayed to represent either a bit address (where the first three digits are the word, and the last two are the bit), or a constant value that is a parameter for an instruction.
- A 4-digit value represents a word address for a register
- Function numbers and timer/counter channel numbers are represented with the first two characters being Fn and ch, respectively.
- When displaying a step address in the mnemonic program, periods appear to the bottom-right of each digit in the 5-digit address.

Instruction Keys

There are 12 instruction keys on the pocket editor that are used for entering the 25 basic instructions on the D50 PLC. To enter certain of the basic instructions, more than one of the instruction keys may be combined. Refer to the Basic Instruction table at the end of this appendix for details.



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Function Keys

There are 8 function keys on the pocket editor, plus two functions that are accessed using the SHF key. The 10 functions each have multiple uses, based on the mode of operation the pocket editor is being used in.

Function Key Descriptions

Key	Function Descriptions
DEL	Delete a step of logic. To accept the Delete request, press the ENT key after the DEL key.
INS	Insert a step of logic in front of the current step. Clear the program. Change the PLC mode between RUN/STOP.
ENT	Enter a step of logic. Switch between displaying instruction and step number. Accept the requested function.
CLR	Cancel key input. Cancel the current display mode. Release a forced output.
SHF	Enable the shifted operation of each key.
SCH	Search for an instruction, step address, or register.
PRE	Return to the previously displayed step, or register.
NXT	Advance to the next step or register.

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Operating Procedures

There are seven separate types of operations that the D50PGM10 pocket editor can perform. These seven operations provide all of the functionality required to program, edit, monitor, and configure the D50 PLC. The seven operations are as follows:

- Clear Program – Deletes the entire program memory from the D50 PLC.
- Add Instruction – Allows the user to write a new program step by step.
- Monitor Program – View the D50 mnemonic program, one instruction at a time.
- Edit Program – Performs inserting, deleting, and changing of program instructions.
- Error Checking – Check the syntax of the program for errors.
- Monitor I/O – Allows the user to monitor and force register values.
- Run/Stop PLC – Switches the PLC between the RUN and STOP modes.

Key Operation Summary

Function		Key Operation	Mode
Clear Program		INS DEL ENT	STOP
Add Instruction	Basic	[Op-code key] [Register Type] [Register No.]	STOP
	Timer/Counter	OUT [Op-code key] [Channel No.] [Set Value]	
	Application	SHF FUN [Function No.] ENT [Operand 1] ENT [Operand 2] ENT [Operand 3] ENT	
Monitor Program	Sequential	NXT or PRE	RUN/STOP
	Search by Step	SHF 0 [Step No.] SCH	
	Search by Inst.	[Enter Instruction] SCH	
	Search by Reg.	SHF [Register Type] [Register No.] SCH	
Edit Program	Insert Inst.	[Enter Instruction] INS	STOP
	Delete Inst.	DEL ENT	
	Change Inst.	[Enter Instruction] ENT	
Error Checking		SHF CHK	RUN/STOP
Monitor I/O	Register Value	SHF [Register Type] [Register No.] MON Change: 0 [Register Value] ENT Next: NXT Previous: PRE	RUN
	Force I/O	Force On: SET ENT Force Off: RST ENT Clear Force: CLR	
Run/Stop PLC	PLC RUN	INS SET	STOP
	PLC STOP	INS RST	RUN

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Clear Program

The Clear Program function will clear out the program memory from the D50 PLC. All of the register memory will also be cleared, with the exception of the Keep (K) registers, and the Timer/Counter registers.

- Function: Clear the program in the D50 PLC
- PLC Mode: STOP

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
INS		AUX	Switches to Auxiliary Mode
DEL		ALL d	Confirm delete all?
ENT		End	Complete delete all

Note: To cancel the clear after pressing the DEL key, press the CLR key.

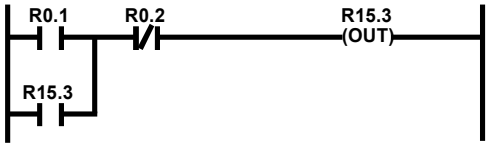
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Add Instruction

The Add Instruction procedure allows the user to enter new mnemonic programs, one instruction at a time. In the example below, the small rung of ladder shown is entered one step at a time, as described in the Operating Procedure table.

- Function: Add new program instructions to the D50 PLC
- PLC Mode: STOP

Ladder Program



Mnemonic Program

```
STR   R0.1
OR    R15.3
ANN   R0.2
OUT   R15.3
```

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
INS DEL ENT		End	Clears program
STR R 1 INS	STR R	1	STR R0.1
OR R 1 5 0 3 INS	OR R	1503	OR R15.3
AND NOT R 2 INS	AND NOT R	2	ANN R0.2
OUT R 1 5 0 3 INS	OUT R	1503	OUT R15.3
		End	

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Monitor Program

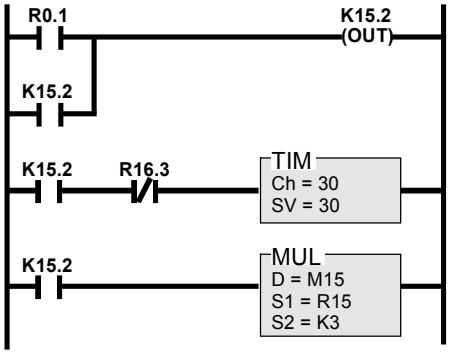
The Monitor Program procedure allows the user to view the currently running program in the D50 PLC. There are two ways to select the portion of the program to monitor, either by consecutively selecting the next or previous step, or by searching for a particular step.

Sequential Step Monitor

Using the next step (NXT) and previous step (PRE) keys, each step of the program is displayed in consecutive order, as is the state of the bit contact for that step, when applicable. The actual step number of the instruction can be viewed by pressing the ENT key. In the example below, the small rung of ladder shown is monitored one step at a time, using the NXT key as described in the Operating Procedure table.

- Function: Step forward (and back) through the program instructions in the D50 PLC
- PLC Mode: STOP or RUN

Ladder Program



Mnemonic Program

```
STR   R0.1
OR    K15.2
OUT   K15.2
STR   K15.2
ANN   R16.3
TIM   30     30
STR   TC30
MUL   M15    R15    K3
```

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Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
NXT	STR R	00001	STR R0.1
NXT	OR K	01502	OR K15.2
NXT	OUT K	01502	OUT K15.2
NXT	STR K	01502	STR K15.2
ENT		0.0.0.0.3.	Displays the step number
NXT		0.0.0.0.4.	Moves to the next step
ENT	AND NOT R	01603	ANN R15.3
NXT	OUT TIM	Ch030	**TIM** **30** 30
NXT		00030	TIM 30 **30**
NXT	STR TC	030	STR TC30
NXT		Fn039	**MUL** M15 R15 K3
NXT	M	00015	MUL **M15** R15 K3
NXT	R	00015	MUL M15 **R15** K3
NXT	K	00003	MUL M15 R15 **K3**
		End	

Note: By pressing the PRE key at any time, the previous instruction will be displayed.

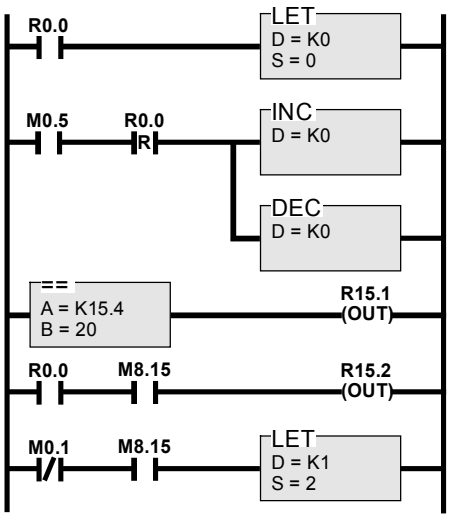
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Search Step Monitor

The Search key (SCH) can also be used to monitor the program, by searching for either the exact step number, or a contact or register within the step. In the example below, the small rung of ladder shown is monitored by searching for various steps in the program.

- Function: Search for a specific step in the D50 PLC
- PLC Mode: STOP or RUN

Ladder Program



Mnemonic Program

```
STR     R0.0
LET     K0      0
STR     M0.5
AND     DIF     R0.0
INC     K0
DEC     K0
STR==   K15.4   R15.1
OUT     R15.1
STR     R0.0
AND     M8.15
OUT     R15.2
STN     M0.1
AND     M8.15
LET     K1      2
```

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Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
SHF 0 9 9 9 SCH		End	Searches to End of program
SHF 0 0 SCH	STR R	00000	Search for first step (step 0)
SHF 0 3 SCH	AND DIF R	00000	Search for step 3
AND M 8 1 5 SCH	AND M	00815	Search for instruction
SCH	AND M	00815	Continue search
SHF 0 8 SCH	STR R	00000	Search for step 8
NXT	AND M	00815	
PRE	STR R	00000	
PRE	OUT R	01501	

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Edit Program

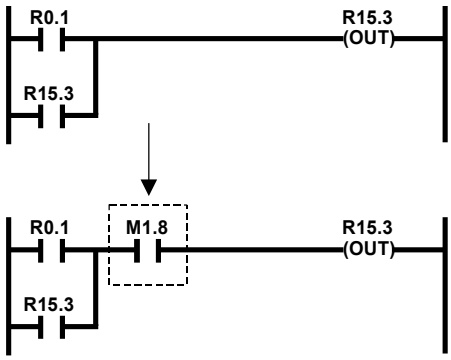
The D50PGM10 pocket editor provides the user the ability to insert, delete, or change an instruction in the D50 PLC. Each of the three procedures is illustrated on the following pages.

Insert Instruction

In the example below, one contact is inserted in the rung of ladder, as shown.

- Function: Insert a new step into the D50 PLC program
- PLC Mode: STOP

Ladder Program



Mnemonic Program

STR	R0.1			STR	R0.1
OR	R15.3	→		OR	R15.3
OUT	R15.3			AND	M1.8
				OUT	R15.3

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
OUT R 1 5 0 3 SCH	OUT R	01503	Search for instruction to add after
AND M 1 0 8 INS	AND M	108	Insert the new instruction
	OUT R	01503	Next instruction will be displayed
PRE	AND M	00108	Verify instruction was added

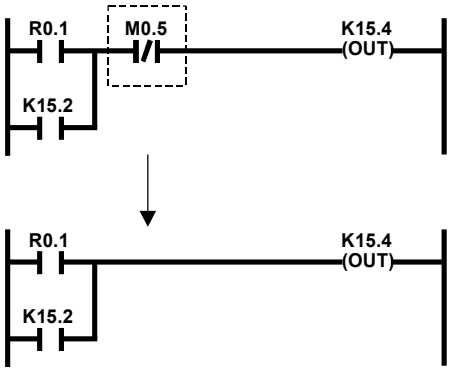
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Delete Instruction

In the example below, one contact is deleted from the rung of ladder, as shown.

- Function: Delete an existing step out of the D50 PLC program
- PLC Mode: STOP

Ladder Program



Mnemonic Program

STR	R0.1			STR	R0.1
OR	K15.2	→		OR	K15.2
ANN	M0.5			OUT	K15.4
OUT	K15.4				

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
AND NOT M 5 SCH	AND NOT M	5	Search for instruction to delete
DEL	AND NOT M	d.0005	Ready to delete – marked with d.
ENT	OUT K	01504	Next instruction will be displayed

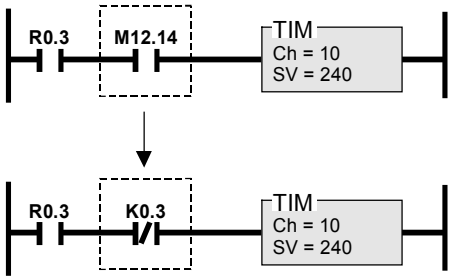
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Change Instruction

In the example below, the address of one contact is changed in the rung of ladder, as shown.

- Function: Change an existing step in the D50 PLC program
- PLC Mode: STOP

Ladder Program



Mnemonic Program

STR	R0.3			STR	R0.3	
AND	M12.14		→	ANN	K0.3	
TIM	10	240		TIM	10	240

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
AND M 1 2 1 4 SCH	AND M	01214	Search for instruction to change
AND NOT K 3 ENT	AND NOT K	3	Enter the changed instruction
NXT	OUT TIM	ch010	View next instruction
PRE	AND NOT K	00003	Verify instruction was changed

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Error Checking

The D50 has built-in error-checking routines that can check the PLC program for syntax errors such as multiple output coils using the same reference, invalid coil addresses, and so on. The D50 pocket editor can request an error check from the D50 PLC using the SHF and CHK keys.

To start the error check, press the SHF key, and then the CHK key. If errors are detected, the 5 digit display will show an "E" followed by a two-digit error code. If no errors are detected, the current instruction will be display with no change.

- Function: Check the program in the D50 PLC for syntax errors
- PLC Mode: STOP

Error Codes

Error Number	Error Name	Error Description
E10	I/O Overrange	I/O address specified in an instruction is too high or low
E11	T/C Overrange	T/C Channel number outside the range 0-255
E12	Word Overrange	Word register address specified is too high or low
E13	Illegal Code	An undefined function code has been used
E14	User Memory Error	Error occurred while writing an instruction to the user memory
E15	System Operation	Miscellaneous undefined error has occurred
E16	User Memory Failure	User program checksum error – invalid memory
E17	I/O Mismatch	Mismatch between physical I/O and program
E18	JMP/CALL	A jump or call to an undefined label or subroutine
E19	LBL Number Error	LBL instruction number has been duplicated
E20	JMPS/JMPE	The JMPS/JMPE instructions are not properly paired
E21	FOR/NEXT	The FOR/NEXT instructions are not properly paired
E22	SBR/RET	The SBR/RET instructions are not properly paired
E23	END	The END instruction is missing
E30	Not Found	Instruction searched for was not found
E31	CPU Running	Program may not be edited while CPU is in RUN mode
E32	Overrange Error	An operation has tried to use a value that is out of range

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Monitor I/O

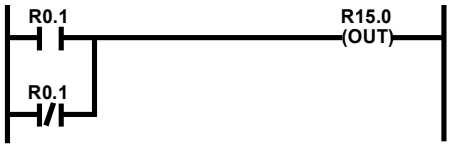
There are two types of monitoring that the pocket editor can perform. The first type is bit monitoring, which displays the state of a given contact or coil in the program. The second type of monitoring is register monitoring, which displays the 16-bit value of any user-specified register address. The monitor mode can also be used to force output bits to a given state, On or Off.

Bit Monitoring

I/O bits (contacts and coils) can only be monitored through the PLC program. At each step in the PLC program, the ON LED will reflect the state of the bit address in that step of the program. If the ON LED is lit, the bit address displayed is in the On state.

- Function: Monitor the state of a contact in the program
- PLC Mode: RUN

Ladder Program



Mnemonic Program

```
STR   R0.1
ORN   R0.1
OUT   R15.0
```

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
OUT R 1 5 0 0 SCH	OUT ON R	01500	Finds step, displays On/Off status

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Register Monitoring

Any valid register address can be monitored using the register monitor mode of the pocket editor. In this mode, the register is continuously updated from the D50 PLC, and can be changed by the user.

To enter the monitor register mode, press the SHF key, the register address, and then the MON (DIF) key. Use the NXT and PRE keys to move to the next or previous register address. To change the value, press the 0 (NOT) key, followed by the new value and the enter (ENT) key. To display the address of the register being monitored, press the ENT key. To exit the monitor register mode, press the Clear (CLR) key.

- Function: Monitor/Change the value of a register
- PLC Mode: RUN

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
SHF W 0 MON		00000	Displays the current value of W0
NXT		00000	Displays the current value of W1
ENT	W	00001	Displays the address W1
PRE	W	00000	Displays the address W0
ENT		00000	Displays the current value of W0
0		C	Enters the “Change Value” mode
1 2 3		123	Enter the new value for W0
ENT		00123	Displays the current value of W0
CLR		End	Exit monitor mode

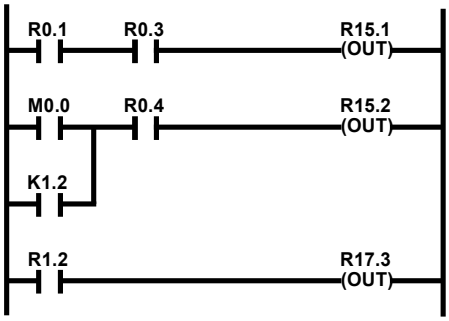
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Force Outputs

The states of output coils can be forced On or Off in the D50 PLC. The output to be forced must be an output that has been programmed in the PLC. The SET and RST keys are used for Force On and Force Off, respectively. Using the NXT or PRE keys will clear the force from the coil and move to the next or previous instruction. The CLR key will remove the force while continuing to display that instruction.

- Function: Force an output to either an On or Off state
- PLC Mode: RUN

Ladder Program



Mnemonic Program

```
STR   R0.1
AND   R0.3
OUT   R15.1
STR   M0.0
OR    K1.2
AND   R0.4
OUT   R15.2
STR   R1.2
OUT   R17.3
```

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
OUT R 1 5 0 1 SCH	OUT R	01501	Finds step, displays On/Off status
SET ENT	OUT ON R	01501	Force ON
RST ENT	OUT R	01501	Force OFF
SET ENT	OUT ON R	01501	Force ON
NXT	STR M	00000	Release force, go to next step
OUT R 1 7 0 3 SCH	OUT ON R	01703	Find instruction
RST ENT	OUT R	01703	Force OFF
SET ENT	OUT ON R	01703	Force ON
CLR	OUT ON R	01703	Release force, continue to display

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Run/Stop PLC

When the RUN/STOP switch on the D50 PLC is in the RUN position, the mode can be overridden by the pocket editor. To place the D50 PLC in STOP, press the INS key, followed by the RST key. To return the PLC to the RUN mode, press the INS key followed by the SET key.

- Function: Clear the program in the D50 PLC
- PLC Mode: STOP

Operating Procedure

Key Sequence	Display		Remarks
	LED	5-Digit Display	
INS	RUN	AUX	Switches to Auxiliary Mode
RST		End	PLC is stopped
INS		AUX	Switches to Auxiliary Mode
SET	RUN	End	PLC switched to RUN

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Instruction Codes

The following tables list the key sequences required to enter each of the mnemonic instructions supported by the D50 PLC.

Basic Instructions

Mnemonic Instruction	Key Sequence	Display	
		LED	5-Digit Display
STR	STR	STR	
STN	STR NOT	STR NOT	
AND	AND	AND	
ANN	AND NOT	AND NOT	
OR	OR	OR	
ORN	OR NOT	OR NOT	
ANB	AND MCS	AND MCS	
ORB	OR MCS	OR MCS	
OUT	OUT	OUT	
NOT	NOT	NOT	
MCS	MCS	MCS	
MCR	MCR	MCR	
SET	SET	SET	
RST	RST	RST	
STR DIF	STR DIF	STR DIF	
AND DIF	AND DIF	AND DIF	
OR DIF	OR DIF	OR DIF	
STR DFN	STR DIF NOT	STR DIF NOT	
AND DFN	AND DIF NOT	AND DIF NOT	
OR DFN	OR DIF NOT	OR DIF NOT	
TIM	OUT TIM	OUT TIM	ch
SST	OUT SST	OUT SST	ch
UC	OUT CNT	OUT CNT	UC
DC	OUT CNT NXT	OUT CNT	dC
UDC	OUT CNT NXT NXT	OUT CNT	Ud

Note: Instructions ANB, ORB, MCS, and MCR require no operand.

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Advanced Instructions

Instruction	Function No.
STR ==S1, S2	FUN 1
AND ==S1, S2	FUN 2
OR ==S1, S2	FUN 3
STR <> S1, S2	FUN 4
AND <> S1, S2	FUN 5
OR <> S1, S2	FUN 6
STR > S1, S2	FUN 7
AND > S1, S2	FUN 8
OR > S1, S2	FUN 9
STR <= S1, S2	FUN 10
AND <= S1, S2	FUN 11
OR <= S1, S2	FUN 12
STR >= S1, S2	FUN 13
AND >= S1, S2	FUN 14
OR >= S1, S2	FUN 15
STR < S1, S2	FUN 16
AND < S1, S2	FUN 17
OR < S1, S2	FUN 18
INC D	FUN 19
DEC D	FUN 20
INCB D	FUN 21
DECB D	FUN 22
ABS D	FUN 23
NEG D	FUN 24
NOT D	FUN 25
RLC D, N	FUN 26
RRC D, N	FUN 27
ROL D, N	FUN 28
ROR D, N	FUN 29
SHL D, N	FUN 30
SHR D, N	FUN 31
LET D, S	FUN 32
BCD D, S	FUN 33
BIN D, S	FUN 34

Instruction	Function No.
ADD D, S1, S2	FUN 35
ADC D, S1, S2	FUN 36
SUB D, S1, S2	FUN 37
SBC D, S1, S2	FUN 38
MUL D, S1, S2	FUN 39
DIV D, S1, S2	FUN 40
ADDB D, S1, S2	FUN 41
ADCB D, S1, S2	FUN 42
SUBB D, S1, S2	FUN 43
SBCB D, S1, S2	FUN 44
MULB D, S1, S2	FUN 45
DIVB D, S1, S2	FUN 46
WAND D, S1, S2	FUN 47
WOR D, S1, S2	FUN 48
XOR D, S1, S2	FUN 49
XNR D, S1, S2	FUN 50
XCHG D1, D2	FUN 51
LDR D, Sr	FUN 52
STO Sr, D	FUN 53
FOR D	FUN 54
STR D== S1,S2	FUN 55
AND D==S1, S2	FUN 56
OR D==S1, S2	FUN 57
STR D<> S1, S2	FUN 58
AND D<> S1, S2	FUN 59
OR D<> S1, S2	FUN 60
STR D> S1, S2	FUN 61
AND D> S1, S2	FUN 62
OR D> S1, S2	FUN 63
STR D<= S1, S2	FUN 64
AND D<= S1, S2	FUN 65
OR D<= S1, S2	FUN 66
STR D>= S1, S2	FUN 67
AND D>= S1, S2	FUN 68



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Instruction	Function No.
OR D>= S1, S2	FUN 69
STR D< S1, S2	FUN 70
AND D< S1, S2	FUN 71
OR D< S1, S2	FUN 72
DINC D	FUN 73
DDEC D	FUN 74
DINCB D	FUN 75
DDECB D	FUN 76
DABS D	FUN 77
DNEG D	FUN 78
DNOT D	FUN 79
DRLC D, N	FUN 80
DRRC D, N	FUN 81
DROL D, N	FUN 82
DROR D, N	FUN 83
DSHL D, N	FUN 84
DSHR D, N	FUN 85
DLET D, S	FUN 86
DBCD D, S	FUN 87
DBIN D, S	FUN 88
DADD D, S1, S2	FUN 89
DADC D, S1, S2	FUN 90
DSUB D, S1, S2	FUN 91
DSBC D, S1, S2	FUN 92
DMUL D, S1, S2	FUN 93
DDIV D, S1, S2	FUN 94
DADDB D, S1, S2	FUN 95
DADCB D, S1, S2	FUN 96
DSUBB D, S1, S2	FUN 97
DSBCB D, S1, S2	FUN 98
DMULB D, S1, S2	FUN 99
DDIVB D, S1, S2	FUN 100
DAND D, S1, S2	FUN 101

Instruction	Function No.
DOR D, S1, S2	FUN 102
DXOR D, S1, S2	FUN 103
DXNR D, S1, S2	FUN 104
DXCHG D1, D2	FUN 105
DLDR D, Sr	FUN 106
DSTO Sr, D	FUN 107
DFOR D	FUN 108
DIS D, Nd, Sr	FUN 109
UNI D, Sr, Nd	FUN 110
MOV D, Sr, Ns	FUN 111
FMOV D, Ns, V	FUN 112
BMOV D, Sr, Ns	FUN 113
BFMV D, Ns, V	FUN 114
BSET D, N	FUN 115
BRST D, N	FUN 116
BNOT D, N	FUN 117
BTST D, N	FUN 118
DECO D, S	FUN 119
ENCO D, S	FUN 120
SEG D, S	FUN 121
SUM D, S	FUN 122
JMP L	FUN 123
CALL Sb	FUN 124
LBL L	FUN 125
SBR Sb	FUN 126
JMPS	FUN 127
NEXT	FUN 128
SC	FUN 129
RC	FUN 130
CC	FUN 131
JMPE	FUN 132
RET	FUN 133
END	FUN 134

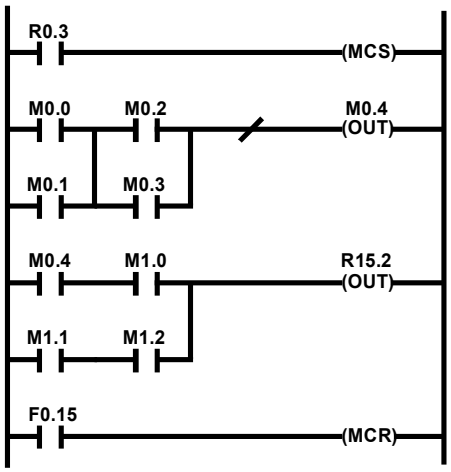
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Programming Examples

The following pages present some very basic programming examples, showing how to enter mnemonic code into the D50 PLC using the pocket editor. Each example program is devided into three sections; the ladder program, the equivalent mnemonic code, and the key sequence for entering the program using the pocket editor

Example 1 – Basic Instructions

Ladder Program



Mnemonic Program

```
STR     R0.3
MCS
STR     M0.0
OR      M0.1
STR     M0.2
OR      M0.3
ANB
NOT
OUT     M0.4
STR     M0.4
AND     M1.0
STR     M1.1
AND     M1.2
ORB
OUT     R15.2
STR     F0.15
MCR
```

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Operating Procedure

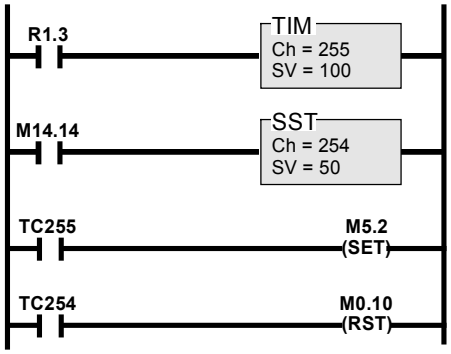
Key Sequence	Display		Mnemonic Instruction
	LED	5-Digit Display	
STR R 3 INS	STR R	3	STR R0.3
MCS INS	MCS		MCS
STR M 0 INS	STR M	0	STR M0.0
OR M 1 INS	OR M	1	OR M0.1
STR M 2 INS	STR M	2	STR M0.2
OR M 3 INS	OR M	3	OR M0.3
AND MCS INS	AND MCS		ANB
NOT INS	NOT		NOT
OUT M 4 INS	OUT M	4	OUT M0.4
STR M 4 INS	STR M	4	STR M0.4
AND M 1 0 0 INS	AND M	100	AND M1.0
STR M 1 0 1 INS	STR M	101	STR M1.1
AND M 1 0 2 INS	AND M	102	AND M1.2
OR MCS INS	OR MCS		ORB
OUT R 1 5 0 2 INS	OUT R	1502	OUT R15.2
STR F 1 5 INS	STR F	15	STR F0.15
MCR INS	MCR		MCR



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Example 2 – Timer Instructions

Ladder Program



Mnemonic Program

```
STR   R1.3
TIM   255    100
STR   M14.14
SST   254    50
STR   TC255
SET   M5.2
STR   TC254
RST   M0.10
```

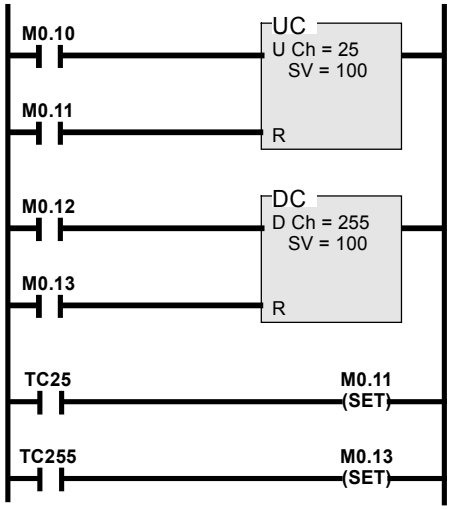
Operating Procedure

Key Sequence	Display		Mnemonic Instruction
	LED	5-Digit Display	
STR R 1 0 3 INS	STR R	103	STR R1.3
OUT TIM 2 5 5 ENT	OUT TIM	ch255	**TIM 255** 100
1 0 0 INS		100	TIM 255 **100**
STR M 1 4 1 4 INS	STR M	1414	STR M14.14
OUT SST 2 5 4 ENT	OUT SST	ch254	**SST 254** 50
5 0 INS		50	SST 254 **50**
STR TIM 2 5 5 INS	STR TC	255	STR TC255
SET M 5 0 2 INS	STR M	502	SET M5.2
STR TIM 2 5 4 INS	STR TC	254	STR TC254
RST M 1 0	RST M	10	RST M0.10

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Example 3 – Counter Instructions

Ladder Program



Mnemonic Program

```
STR     M0.10
STR     M0.11
UC      25      100
STR     M0.12
STR     M0.13
DC      255     100
STR     TC25
SET     M0.11
STR     TC255
SET     M0.13
```

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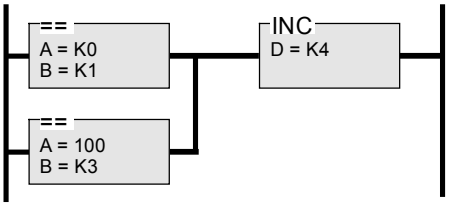
Operating Procedure

Key Sequence	Display		Mnemonic Instruction
	LED	5-Digit Display	
STR M 1 0 INS	STR M	10	STR M0.10
STR M 1 1 INS	STR M	11	STR M0.11
OUT CNT 2 5 ENT	OUT CNT	UC 25	**UC 25** 100
1 0 0 INS		100	UC 25 **100**
STR M 1 2 INS	STR M	12	STR M0.12
STR M 1 3 INS	STR M	13	STR M0.13
OUT CNT	OUT CNT	UC	-
NXT	OUT CNT	dC	**DC** 255 100
2 5 5 ENT	OUT CNT	dC255	DC **255** 100
1 0 0 INS		100	DC 255 **100**
STR TIM 2 5 INS	STR TC	25	STR TC25
SET M 1 1 INS	SET M	11	SET M0.11
STR TIM 2 5 5 INS	STR TC	255	STR TC255
SET M 1 3 INS	SET M	13	SET M0.13

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Example 4 – Comparison/Advanced Instructions

Ladder Program



Mnemonic Program

```
STR==  K0    K1
OR==   100   K3
INC    K4
```

Operating Procedure

Key Sequence	Display		Mnemonic Instruction
	LED	5-Digit Display	
SHF FUN 1		Fn 1	**STR==** K0 K1
ENT		S1	
K 0	K	0	STR== **K0** K1
ENT		S2	
K 1	K	1	STR== K0 **K1**
ENT		Fn 1	STR== K0 K1
INS		End	
SHF FUN 3		Fn 3	**OR==** 100 K3
ENT		S1	
0		0	
1 0 0		100	OR== **100** K3
ENT		S2	
K 3	K	3	OR== 100 **K1**
ENT		Fn 3	OR== 100 K1
INS		End	
SHF FUN 1 9		Fn 19	**INC** K4
ENT		d	
K 4	K	4	INC **K4**
ENT		Fn 19	INC K4
INS		End	

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