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CVME965
SINGLE BOARD COMPUTER

USER'S MANUAL

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Cyclone P/N 800-0965

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CHAPTER 1
INTRODUCTION

1.1 GENERAL INTRODUCTION

The CVME965 is a high-performance single board computer which has been optimized for intelligent I/O applications.

The board is based on an 80960HD processor, a VME64 interface and two Squall II Modules for interchangeable I/O modules. The board has been optimized for I/O handling by providing two separate memories: a private memory for the processor and a shared (or packet) memory for I/O communications. Another optimization is a powerful VMEbus DMA controller which can perform D32 and D64 block transfers from the local shared memory to other VME boards.

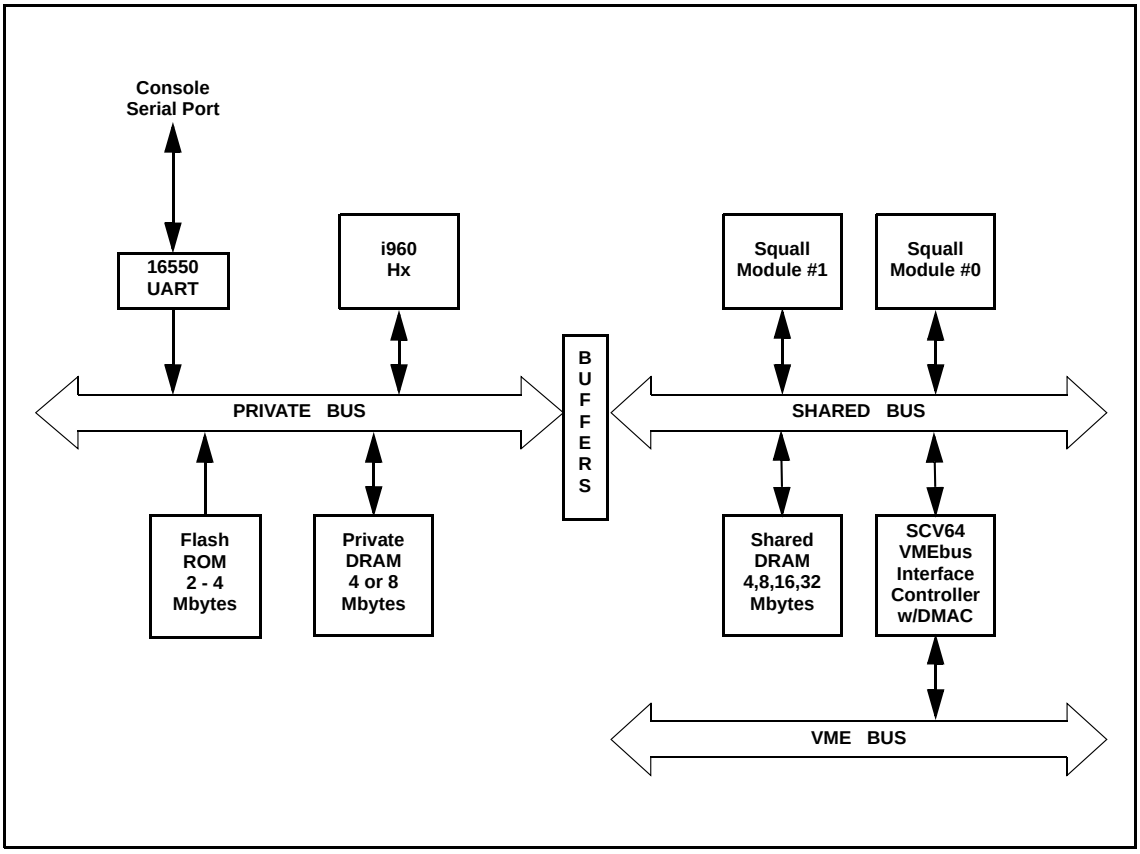


Figure 1-1. CVME965 Block Diagram

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1.2 FEATURES

80960HD Processor	The microprocessor is an Intel Superscalar 80960HD RISC device running at 33 MHz externally, 66 MHz internally. The processor boasts a 16 Kbyte instruction cache, a 8 Kbyte data cache and a 2 Kbyte data scratch memory.
Private DRAM	Four or eight Mbytes of EDO DRAM which resides on the processor bus and is accessible only by the processor in single or burst accesses.
Shared DRAM	Four, eight, sixteen or thirty-two Mbytes of EDO DRAM which may be accessed by the processor, VMEbus masters, the VMEbus DMA controller, and Squall Module devices with DMA Capability. The shared DRAM is located on a field-upgradeable memory module.
Squall II Modules	The CVME965 has two locations for Squall II Modules. The modules can contain I/O devices and may be accessed by the 80960HD processor. Devices with DMA capability on the Squall II Modules can access the shared DRAM.
VME64 Interface	The VMEbus interface is a master/slave interface which allows the 80960HD to access the VMEbus and VME masters to access the shared DRAM. The interface can be used in a decoupled mode, which uses a 15 transfer FIFO to post bus writes allowing them to complete independently and avoid tying up both the local and VMEbuses.
VME64 DMA Controller	The VME interface has a DMA controller which can perform D32 and D64 VMEbus block transfers between the local shared DRAM and a VME memory. The DMA controller makes use of the shared DRAM's EDO access mode and the VMEbus interface's 15 transfer FIFO for fast, efficient data movement.
Software Reset	The CVME965 includes a feature which allows VMEbus masters to reset the board by accessing a special A16 slave image on the VMEbus. This feature is useful during the debug cycle and in production systems when it is necessary to reset a board without human intervention.
Flash ROM	The CVME965 can be shipped with 2 or 4 Mbytes of sector programmable Flash ROM.
Console Serial Port	An asynchronous serial port is provided for a console terminal or workstation connection.
Counter/Timers	Two 32 bit counter/timers are built into the i960HD and can provide periodic interrupts or other timing functions.
Non-Volatile RAM	Non-volatile storage is provided by Flash ROM on the CVME965. One 64 Kbyte sector of the Flash ROM is reserved for the storage of non-volatile parameters. System calls for storing parameters in this memory are included in the Breeze Development Environment. Refer to the Software Development chapter of this manual for more information.

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Breeze Development Environment™

Cyclone includes a set of extensions to MON960 intended to ease the process of software development on the CVME965. Breeze consists of a number of System Services available to user applications, as well as autoboot functions and Flash memory programming support.

1.3 SPECIFICATIONS

Physical Characteristics

The CVME965 is a single slot, double high (6U) VMEbus Eurocard. Including properly designed Squall II Modules, the CVME965 resides in a single VMEbus card cage slot.

Height	9.187" (233.35 mm)	Double Eurcard (6U)
Depth	6.299" (160 mm)	
Width	0.8" (20.32 mm)	One VMEbus slot

Power Requirements

The CVME965 requires +5v, +12v and -12v which all should be available on VMEbus backplane. Both the P1 and P2 VMEbus backplanes should be used to insure proper power distribution to the CVME965. If Squall Modules are installed on the CVME965, the power requirements of the Modules should be added to the requirements listed below.

Table 1-1. Power Requirements*

Voltage	Maximum Current	Typical Current
+5v	5.0 Amps	3.75 Amps
+12v	0.05 Amps	0.05 Amps
-12v	0.05 Amps	0.05 Amps

* Does not include Squall Modules installed on the CVME965.

1.4 ENVIRONMENTAL

The CVME965 should be operated in a card cage with good air flow, as the card does dissipate 25 watts of power. The board can be operated at ambient air temperatures of 0-55 degrees Celsius, as measured at the board.

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Table 1-2. Environmental

Operating Temperatures	**0 to 55 Degrees Celsius**
Relative Humidity (non-condensing)	**0-95%**
Storage Temperatures	**-55 to 125 Degrees Celsius**

1.5 REFERENCE MANUALS

The following manuals are applicable to the circuitry found on the CVME965 and may provide additional helpful information to the user.

VMEbus Specification Manual
VMEbus International Trade Association
10229 North Scottsdale Road, Suite E
Scottsdale, Arizona 85253

80960HD User's Manual
Intel i960Hx Microprocessor Reference Manual Supplement
Order Number 272484-001
Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641
(800) 548-4725

SCV64 User Manual
Tundra Semiconductor
603 March Road
Kanata, Ontario
Canada K2K 2M5
(613) 592-0714

16C550 UART
Texas Instruments
Literature Response Center
P.O. Box 809066
Dallas, TX 75380-9066
(800) 477-8924

MON960 Debug Monitor User’s Guide
Order Number 484290-003
Intel Corporation
Literature Sales
P.O. Box 7641

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(800) 548-4725

1.6 CHANGES FROM CVME964 TO CVME965

The following is a list of changes and improvements we have made to the CVME965 from the CVME964.

1. Processor upgraded to i960HD-66.
2. Private DRAM upgraded to 4 or 8 Mbytes.
3. Shared DRAM performance improved. SCV64 burst reads improved to a two clock cycle access from a three clock cycle access.
4. ROM storage updated to Flash ROM and more capacity added.
5. MBLT64 or VME64 errata with the SCV64 corrected. 64 bit transfers now work properly.
6. Software reset capability added, allowing other VMEbus Masters to reset the CVME965.
7. Serial Controller 85C30 replaced with 16C550 UART.
8. Clock Frequency Status Register added.
9. Lower cost!

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CHAPTER 2
SWITCHES

2.1 RESET/NMI SWITCH

The front panel of the CVME965 contains a double throw toggle switch. Pushing the switch to the left generates a local reset signal, resetting all the functions of the board. This signal will not generate a VMEbus SYSRST* signal.

Pushing the switch to the right will generate an NMI (Non-Maskable Interrupt) to the 80960HD processor. Different real time kernel react slightly differently to this switch, but they all attempt to abort the current operation and return to the shell or monitor.

2.2 LED INDICATORS

The CVME965 has three LED indicators on the front panel, F (FAIL), SF (SYSFAIL) and RUN. The right most LED, F, is red and is connected to the 80960HD processor's FAIL* signal. The LED is lit while the processor is in the reset state. The LED remains lit after reset while the processor performs a self-test and a bus confidence test. Upon passing these tests, the LED is extinguished. If the LED remains asserted after reset, the processor has failed one of these tests. The bus confidence test is performed with a checksum stored in the Flash.

The center LED is yellow, SF, and indicates the status of the local SYSFAIL bit in the VMEbus SCV64 MISC control register. Upon reset this bit is set, asserting the VMEbus SYSFAIL* signal and illuminating the SYSFAIL LED. After the processor successfully performs a board level self-test, the SYSFAIL control bit is cleared, extinguishing the SYSFAIL LED and negating the SYSFAIL* VMEbus signal. Boards can monitor the SYSFAIL* signal to determine when and if all the boards in a system have successfully passed their self-tests.

The left LED is green, RUN, and driven by the processor's data enable signal. The LED is illuminated when the processor is using the local bus. The LED's intensity varies dependent on the access time of the device being accessed. Fast devices, such as the Private DRAM will result in a dimmer display, while slower devices, such as VMEbus read cycles, will result in a much brighter display.

2.3 FREQUENCY SWITCHES

The CVME965 is equipped with frequency selection switches. The board clock frequency can be changed by setting the switches to the values from Table 2-1 and resetting the board.

The frequency switches are located at position SW3 on the CVME965. The frequency setting can be read by software from the Clock Frequency Status Register, documented in section 4.9.

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Table 2-1. Frequency Switch Settings

Frequency	SW3-2	SW3-3	SW3-4
16 MHz	ON	OFF	ON
20 MHz	ON	OFF	OFF
25 MHz	OFF	ON	ON
33 MHz	OFF	ON	OFF

Note: Do not select a clock frequency higher than the rated speed of the installed i960 processor.

2.4 ROMSWAP SWITCH

The ROMSWAP switch is located at SW3-1. This switch controls the memory location of the factory ROM, and is intended for factory use only. It should be in the OFF position at all times.

2.5 VME SLAVE ADDRESS SWITCHES

Five switches are provided on the front panel to determine the VMEbus A32 slave address of the CVME965. The switches represent address lines A31 through A27. Setting a switch "on" sets the corresponding bit of the board's VME address to a "1". Setting the switch "off" sets the corresponding address bit to a "0". The resulting address will be aligned to a 128 Mbyte boundary. All address combinations shown in Table 2-2 allow the processor to access the shared memory at the VMEbus slave address.

The value of the slave address switches is also used to determine the location of the board's A16 slave image, which is used for software reset. This feature is discussed in section 5.5. The default A16 slave image location for the various switch settings is shown in Table 2-2. The A16 slave image location can be changed by software if necessary.

The value of the switches may be read by the processor by reading bits 7-3 of the switch and IPL Status Register (address B420 0000h). Please refer to section 4.11 for details. Cyclone boot code automatically loads this value into the SCV64 VMEBAR register to be used to determine the board VMEbus A32 slave base address.

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Table 2-2. VMEbus A32 Slave Address Switches

Switch Setting (A31 ... A27) (1=on 0=off)	VMEbus Slave Base Address (A32)	VMEbus Short Space Software Reset Address(A16) (Note 1)
00000	0000 0000h	E000h
00001	0800 0000h	E080h
00010	1000 0000h	E100h
00011	1800 0000h	E180h
00100	2000 0000h	E200h
00101	2800 0000h	E280h
00110	3000 0000h	E300h
00111	3800 0000h	E380h
01000	4000 0000h	E400h
01001	4800 0000h	E480h
01010	5000 0000h	E500h
01011	5800 0000h	E580h
01100	6000 0000h	E600h
01101	6800 0000h	E680h
01110	7000 0000h	E700h
01111	7800 0000h	E780h
10000	8000 0000h	E800h
10001	8800 0000h	E880h
10010	9000 0000h	E900h
10011	9800 0000h	E980h

Note 1: Accessing this image will cause the target CVME965 to be reset. These are default values, and can be changed if necessary. The software reset feature is documented in section 5.5.

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2.6 CONSOLE SERIAL PORT

A four conductor phone jack provides a serial port for asynchronous communications to a console terminal or development workstation. Section 4.7 describes the port in detail including connector pin assignments, cabling to a standard EIA-232 25 pin connector, and programming information. A cable connecting the phone jack to a standard DB-25 connector is supplied by Cyclone (Cyclone P/N 530-2002).



Figure 2-1. CVME965 Front Panel

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CHAPTER 3
PROCESSOR

3.1 80960 PROCESSOR

The 80960HD processor is a second generation RISC processor, utilizing a superscalar architecture which allows the execution of more than one instruction per clock cycle. The device features a 16 Kbyte instruction cache, a 8 Kbyte data cache and a 2 Kbyte on chip SRAM scratch pad memory. An on-chip register cache accelerates context switches and interrupt routines. These features make the processor an excellent choice for embedded control situations.

3.2 BYTE ORDERING

The 80960HD processor can access external devices in either big endian or little endian mode. The byte ordering determines which memory location stores the least significant byte of the operand. Little endian stores the least significant byte in the lowest address. Big endian stores the most significant byte in the lowest address.

The 80960HD can be configured to load and store data in big endian or little endian format. Unlike previous members of the i960 family, endian selection is handled by user-configurable memory templates, which allow endian control of regions as small as 4 Kbytes. Information on memory region programming can be found in section 3.4.

The user must to be careful to use the appropriate compiler switch to generate little or big endian code depending on how the memory region where the code will reside is configured.

3.3 80960HD CACHE AND SCRATCH PAD MEMORIES

The 80960HD has three separate cache and scratch pad memories. The instruction cache is a 16 Kbyte 4-way set associative cache. The default mode of the cache is enabled. The user may disable the cache or load and lock a program into portions of the cache. The remaining portion of the cache continues to operate as a normal instruction cache. Instruction cache control is performed via the icctl or sysctl assembly language instructions. Please refer to the Intel i960Hx Microprocessor User’s Manual for more details.

The data cache is a 8 Kbyte 4 way set associative data cache which can return a quad word (128 bits) to the register file in a single clock cycle on a cache hit. The cache has a separate valid bit for each work in the quad word tag line. The write policy is write through and write allocate. Data Cache Control is performed via the Logical Memory Configuration Registers and the dcctl assembly language instruction. Please refer to the Intel i960Hx Microprocessor User’s Manual for more details.

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3.4 MEMORY REGION PROGRAMMING

The i960HD divides its 4 Gigabyte address space into 16 memory regions. The characteristics of these memory regions are controlled by two separate sets of configuration registers on the processor. Physical Memory Configuration registers (PMCON0-PMCON15), of which there is one for each of the 16 memory regions, allow control over wait states, bursting, and data bus width for each region. The PMCON registers are memory-mapped on the i960HD and can be changed after initialization simply by writing to the appropriate memory-mapped location.

Logical Memory Configuration registers are used to control byte ordering and data cacheability. The i960HD has 15 pairs of Logical Memory Configuration registers, plus a default configuration register, DLMCON. Unlike the PMCON registers, Logical Memory Configuration registers have a programmable range, and allow great flexibility in the application of logical memory parameters. They can be used to enable or disable the data cache or alter the byte ordering of small blocks of memory within a region. See the i960Hx Processor User's Guide for detailed programming information. Table 3-3 contains the recommended Logical Memory Configuration register values for the CVME965.

The i960HD also contains a 2 Kbyte scratch pad SRAM memory on the chip. This memory is mapped from addresses 0000 0000h to 0000 0800h in the i960's address space. Data from this memory is accessed with zero wait states 128 bits at a time. Unlike data caches, which attempt to predict the data which will be used again, data storage in the internal RAM is under software control. Applications can take advantage of the internal data RAM for critical variable storage to provide high speed and deterministic access to data.

Table 3-1. Physical Memory Configuration Register Entries

Register	Region	PMCON Value	Description
PMCON0-9	0-9	3080 0000h	VMEbus
PMCON10	A	3080 0000h	Private DRAM
PMCON11	B	3000 0000h	Flash / I/O / UART
PMCON12	C	2080 0000h (Note 1)	Squall Module 0
PMCON13	D	2080 0000h (Note 1)	Squall Module 1
PMCON14	E	3080 0000h	Shared Memory
PMCON15	F	3080 0000h	VMEbus/SCV64/IACK
PMCON15	F (Note 2)	A003 0000h	EPROM

Note 1: Default value, may be changed after reading EEPROM from Squall Module.
Note 2: At initialization region F will be set to the region B value. Afterwards, region F will be set to the VMEbus/SCV64/IACK value.

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Table 3-2. Logical Memory Configuration Register Entries

Register	Value	Description
DLMCON	0000 0000h	Little endian, data cache disabled.
LMAR14	F000 0001h	Template 14 starting address F000 0000h, big endian region (required for the SCV64 device).
LMMR14	F000 0001h	Template 14 mask and enable bit.
LMAR0	A000 0002h	Template 0 starting address A000 0000h, little endian region, data cache enabled.
LMMR0	F000 0001h	Template 0 mask and enable bit.

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3.5 MEMORY MAP

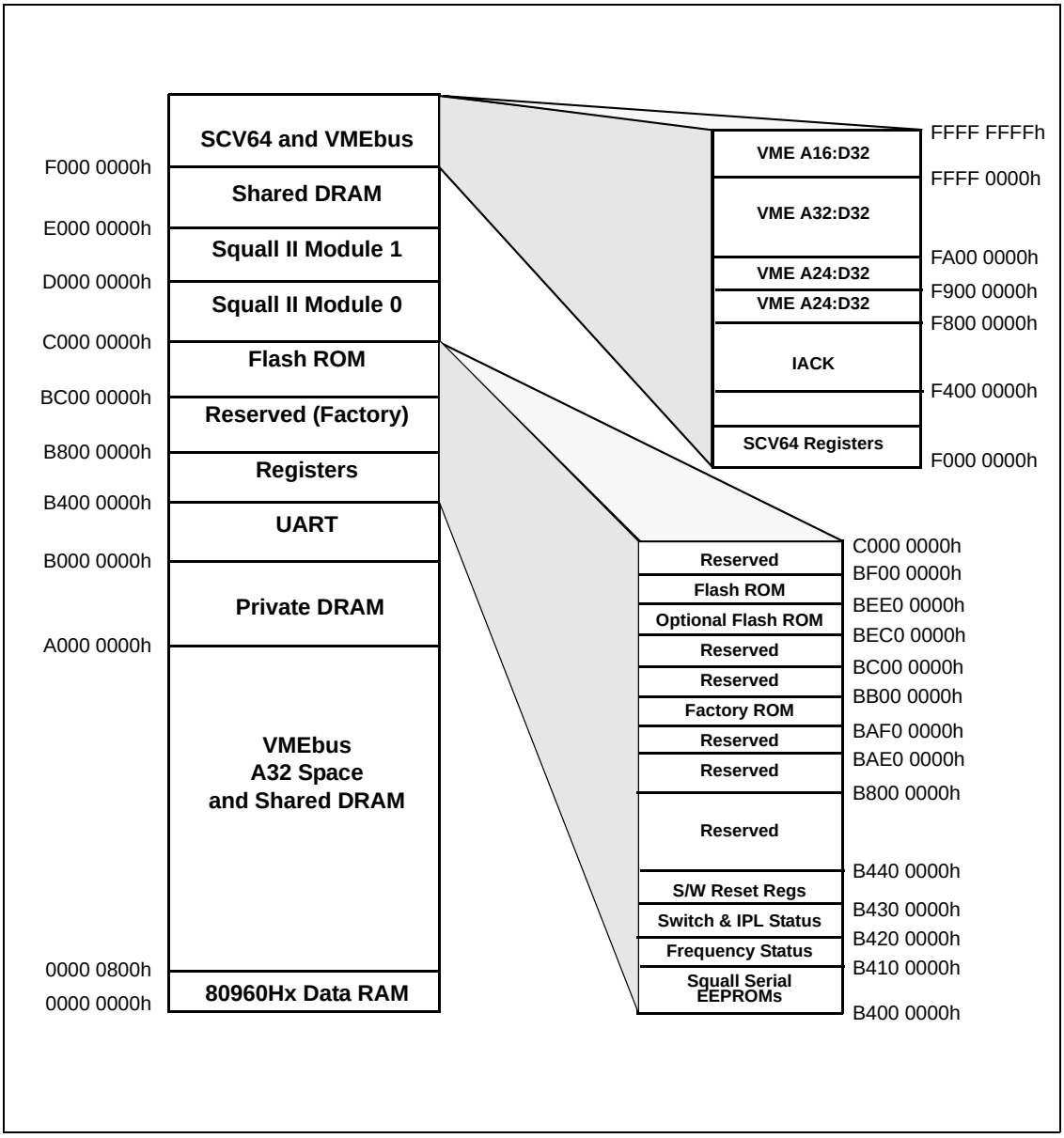


Figure 3-1. CVME965 Memory Map

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3.6 INTERRUPTS

The CVME965 uses the i960HD's internal programmable interrupt controller to handle the on board interrupt sources. VMEbus interrupts and SCV64 interrupts are all handled as a single interrupt to the i960HD processor. The interrupt service routine may then emulate a 68000 interrupt acknowledge cycle to receive a VMEbus interrupt vector. The interrupt structure of the CVME965 is shown in Figure 3-2. The interrupt structure internal to the SCV64 is shown in Figure 3-3.

The CVME965 is designed to use the i960HD's interrupt handler in dedicated interrupt mode. In this mode each XINT pin generates a unique interrupt to the processor. Dedicated mode is determined by the interrupt control (ICON) register bit 0 and 1. (Please refer to Interrupt Control (ICON) Register section 3.7 for more details). The vectors for these interrupts are determined internally by the i960HD processor via the IMAP2-IMAP0 registers.

Table 3-3. CVME965 Interrupt Sources

Interrupt	Name	Description
NMI	Abort	Abort Switch
XINT7	IRQUART	Interrupt Request from UART (16C550)
XINT6	Not used	
XINT5	SQ0IRQ1	Squall Module 0 Interrupt Request 1
XINT4	SQ0IRQ0	Squall Module 0 Interrupt Request 0
XINT3	SQ1IRQ1	Squall Module 1 Interrupt Request 1
XINT2	SQ1IRQ0	Squall Module 1 Interrupt Request 0
XINT1	IRQSCV64	See Table 3.3
XINT0	SCV64BERR	Local Bus ERROR Signal from SCV64

Table 3-4. IRQSCV64 Interrupt Sources

Interrupt	Name	Description
L7IACF	ACFAIL	VMEbus ACFAIL* Signal
L7ISYF	SYSFAIL	SCV64 SYSFAIL Bit
BIMODE	BIMODE	SCV64 Bimode Bit
LIRQ5	VMEINT	This interrupt covers the sources from the SCV64 CDSR register, including:
	CERR	SCV64 Configuration Error
	DLBER	DMA Local Bus Error Occurred

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Interrupt	Name	Description
	LBERR	Local BERR Signal Received in Decoupled Mode
	VBERR	VMEbus BERR* Received while in Decoupled Mode
	DONE	DMA Done Indicator
LIRQ2	LMINT	Location Monitor, Mailbox FIFO Written to Interrupt
VIRQ7	VIRQ7	VMEbus Interrupt 7
VIRQ6	VIRQ6	VMEbus Interrupt 6
VIRQ5	VIRQ5	VMEbus Interrupt 5
VIRQ4	VIRQ4	VMEbus Interrupt 4
VIRQ3	VIRQ3	VMEbus Interrupt 3
VIRQ2	VIRQ2	VMEbus Interrupt 2
VIRQ1	VIRQ1	VMEbus Interrupt 1

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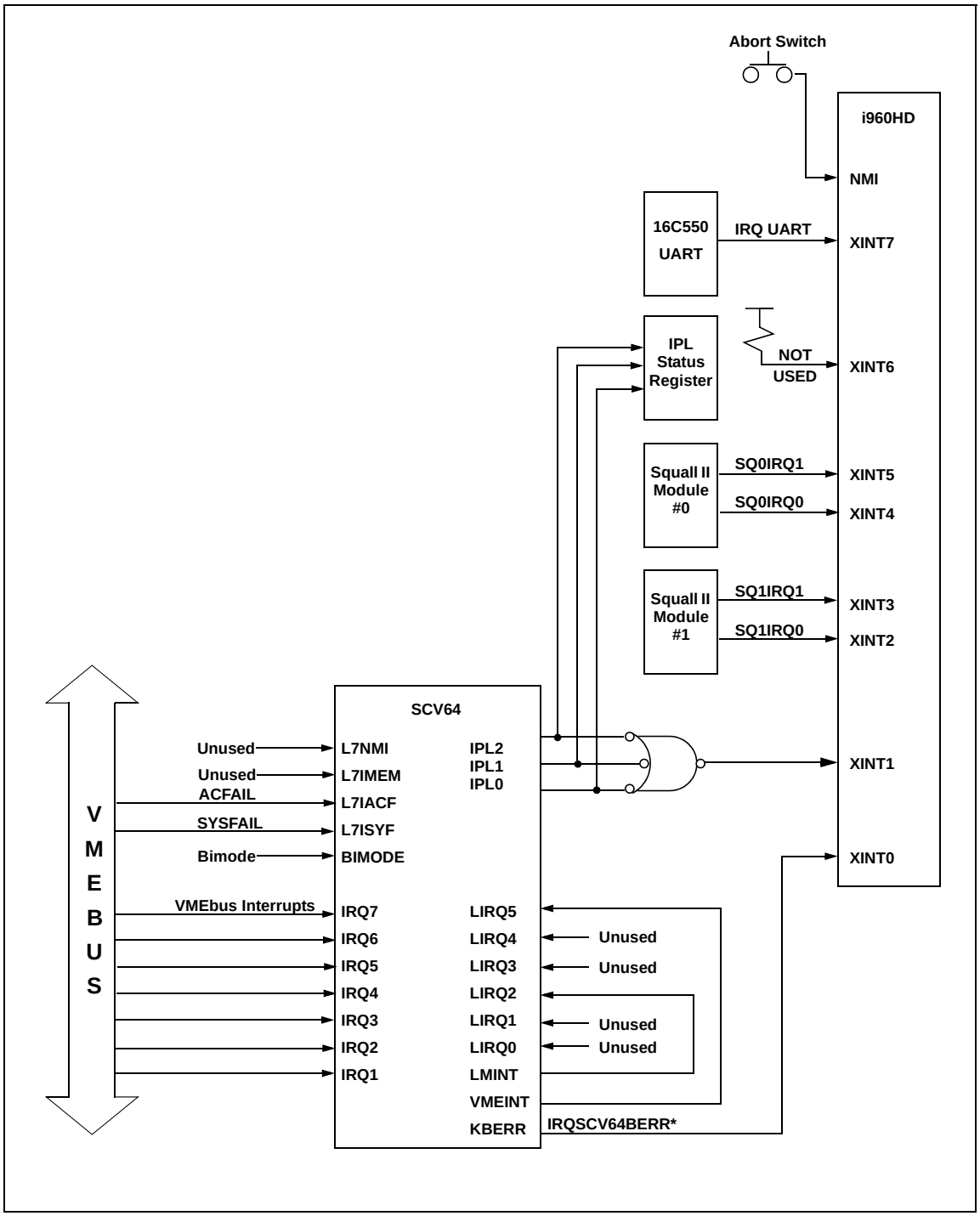


Figure 3-2. CVME965 Interrupt Structure

(Refer to Figure 3-3 for Interrupt Structure Internal to SCV64)

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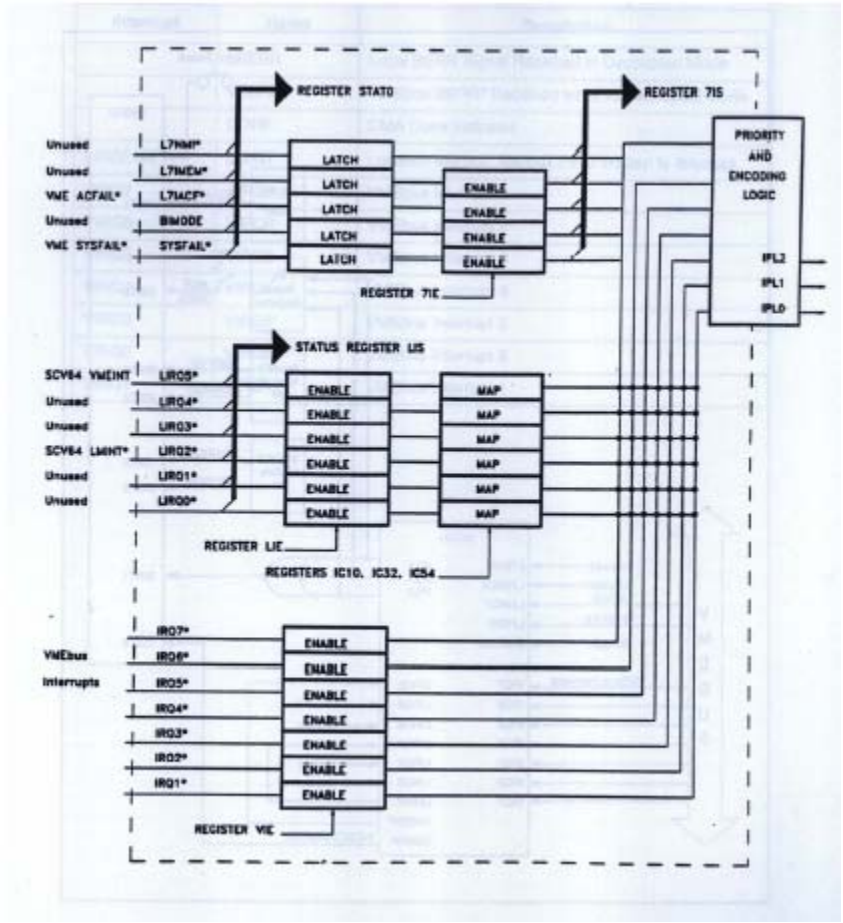


Figure 3-3. Interrupt Structure Internal to SCV64

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3.7 INTERRUPT CONTROL (ICON) REGISTER

The CVME965 has been designed to be used with the i960HD's dedicated interrupt mode. The ICON register also determines the signal detection mode and other interrupt operation parameters, see Figure 3-4 for details.

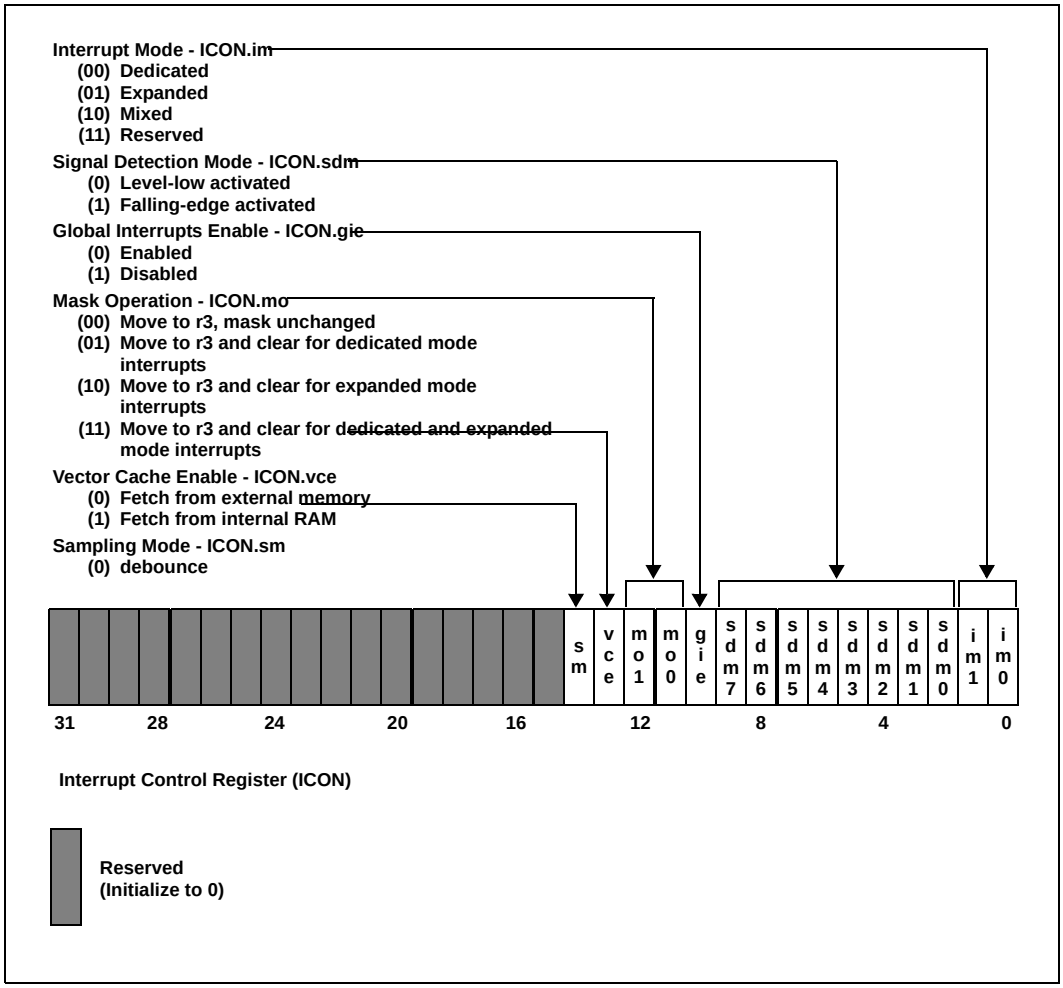


Figure 3-4. Interrupt Control (ICON) Register

3.8 OTHER I960HD INTERRUPT REGISTERS

The i960HD processor has several different internal registers to facilitate the handling of interrupts which are briefly mentioned below. These registers are memory-mapped on the i960HD and can be read and written by software. Please refer to the Intel i960HD User's Manual for more details.

IMAP2-IMAP0 Three Interrupt Mapping (IMAP) Registers are used in dedicated mode to assign the upper four bits of each interrupt's vector. In dedicated mode the lower four bits of all interrupt vectors except NMI are fixed at 0010.

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IPND — The Interrupt Pending (IPND) Register posts the interrupt signals as pending.

IMSK — The Interrupt Mask (IMSK) Register allows software to mask any of the eight dedicated interrupt signals as well as the two internal timer interrupts.

3.9 VMEBUS AND SCV64 INTERRUPT HANDLER

Interrupts for all the SCV64 and VMEbus interrupt sources (except the Local Bus Error on XINT0) are requested to the processor via XINT1 (IRQSCV64, refer to Table 3-4). Interrupt handling is performed in a two layer approach. The first layer, called by the XINT1 vector internal to the i960HD processor, must determine the IPL level of the pending interrupt. With the IPL level the interrupt service routing can determine the source of the interrupt by polling registers in the SCV64 and performing an IACK cycle (a read to one of the seven IACK locations). Upon determining the source of the VMEbus or SCV64 interrupt the XINT1 interrupt service routine may then call the appropriate service routine (second level) to respond to the interrupt request.

In order to simplify interrupt handling LIRQ5 (connected to VMEINT) and LIRQ2 (connected to LMINT) should be mapped as level 7 interrupts. This is done by loading the IC54 Register (address F000 00BCh) with the value 0x000000F8 and the IC32 Register (address F000 00B8h) with the value 0x0000008F. This will cause all interrupts generated internal to the SCV64, not VMEbus IRQ7-1, to generate level 7 interrupts.

The first level (i960) interrupt service routine must determine the source or vector of the interrupt and call an appropriate interrupt handler. The service routine first determines the IPL level being requested by reading bits 2-0 of the Front Panel Switch and IPL Status Register (address B420 0000h, byte read) which correspond to IPL2 through IPL0 respectively. Because the IPL bits may change at any time, this value should be repeatedly read until the same value is read twice.

For IPL levels 1-6 the service routine may now access the appropriate IACK location with a byte read to generate a VMEbus IACK (Interrupt Acknowledge) cycle. The interrupting slave VMEbus board will return a byte vector during this cycle. Table 3-5 gives the IACK addresses.

IPL level 7 is unique in that all the internal SCV64 interrupts may generate IPL level 7 interrupts. The service routine must first check the level 7 Interrupt Status Register (7IS) and the Local Interrupt Status Register (LIS) for active requests. If no requests are active, a level 7 IACK cycle should be run to receive a vector from the VME board generating the level 7 interrupt. A level 7 IACK cycle is performed by reading a byte from the location given in Table 3-5.

An active LIRQ2 interrupt indicates a Location Monitor (LMINT) mailbox interrupt.

An active LIRQ5 interrupt indicates an SCV64 VMEINT indicating one or more of the following SCV64 interrupts: CERR; DLBER; LBERR; VBERR; or DONE. The source can be determined by interrogating the Control and Status Register (DCSR) at address F000 000Ch.

The SCV64 signals bus errors on either XINT1, if the cycle that generated the error was decoupled, or XINT0, if the cycle was coupled. VMEbus reads will always be coupled; writes are decoupled unless atomic instructions are used or the FIFOs are disabled. Since XINT0 is only used to signal one type of interrupt, no multiple-layer handling scheme is required.

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Table 3-5. IACK Addresses

IPL#	Address to Generate VMEbus IACK Cycle
1	F400 0013h
2	F400 0007h
3	F400 0017h
4	F400 000Bh
5	F400 001Bh
6	F400 000Fh
7	F400 001Fh

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CHAPTER 4
MEMORY AND I/O

4.1 ON BOARD MEMORY

The CVME965 has a unique memory architecture. The architecture addresses the problem of the processor being starved out of the memory by the high speed DMA controllers located on the Squall II Modules and the SCV64 VME Interface controller. The CVME965 has been designed with two banks of DRAM memory, a shared or public memory and a private memory. The shared or public memory is accessible by everyone: the processor, DMA controllers on the Squall Modules, DMA controller in the SCV64 VME Interface and other VMEbus masters. The private memory is accessible by only the processor, allowing the processor uninterrupted access at code, stacks, and other private data structures. The CVME965 also contains Flash ROM memory which includes space reserved for a non-volatile parameter memory.

4.2 PRIVATE MEMORY

The 960HD processor has a 4 or 8 Mbyte private EDO DRAM memory. Private memory is intended for the storage of code and data which will be accessed only by the processor, thereby increasing the available bandwidth on the shared bus and ensuring that the processor is not starved off the bus. Table 4-1 shows the performance of the processor and the private memory. Only the processor can access private memory.

Table 4-1. Private Memory Access Time for the Processor

Access	Wait States	Clock Cycles	Bandwidth
Read	2	4,1*	27 Mbytes/sec
Write	2	4,1*	27 Mbytes/sec
Burst Read (4 accesses)	2, 0, 0, 0	4, 1, 1, 1, 1*	66 Mbytes/sec
Burst Write (4 accesses)	2, 1, 1, 1	4, 2, 2, 2, 1*	48 Mbytes/sec

* The extra cycle is the overhead for DRAM precharge time. The DRAM precharge time only impacts back to back cycles. The bandwidths stated are sustained bandwidths, not peak.

4.3 SHARED DRAM MEMORY

The CVME965 Shared DRAM memory is located on a field upgradeable module. Modules may be installed with 4, 8, 16, or 32 Mbytes of EDO DRAM memory. The board autoconfigures to the installed module, requiring no jumper or software changes.

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Shared memory is accessible by the processor, DMA controllers located on the Squall Modules, the SCV64 DMA Controller and other VMEbus masters. The memory is accessible by the processor and Squall Module DMA controllers at address E000 0000h and the VMEbus slave address loaded into the SCV64 register VMEBAR. The shared DRAM memory is accessible by the VMEbus masters at the address loaded into the SCV64 register VMEBAR. The address loaded into the VMEBAR register may by determined from the front panel switches, see section 2.3. Table 4-2 shows the performance of the shared DRAM.

Table 4-2. Shared DRAM Access Time

Master	Access	Clock Cycles	Bandwidth
Processor	Read	5	26 Mbytes/sec
Processor	Write	5	26 Mbytes/sec
Processor	Burst Read (4 accesses)	5, 2, 2, 2	48 Mbytes/sec
Processor	Burst Write (4 accesses)	5, 2, 2, 2	48 Mbytes/sec
Squall	Read	4, 1*	27 Mbytes/sec (Note 1)
Squall	Write	4, 1*	27 Mbytes/sec (Note 1)
Squall	Burst Read (4 accesses)	4, 2, 2, 2, 1*	48 Mbytes/sec (Note 1)
Squall	Burst Write (4 accesses)	4, 2, 2, 2, 1*	48 Mbytes/sec (Note 1)
Squall	Burst Long (32 accesses)	4, 2, 2, 2 ... 2, 1	64 Mbytes/sec (Note 1)
SCV64 DMA	Read	4, 1*	27 Mbytes/sec
SCV64 DMA	Write	4, 1*	27 Mbytes/sec
SCV64 DMA	Burst Read (32 accesses)	5, 2, 2, 2... 2, 1*	63 Mbytes/sec
SCV64 DMA	Burst Write(32 accesses)	5, 2, 2, 2 ... 2, 1*	63 Mbytes/sec

* The extra cycle is to allow for DRAM precharge time. The precharge time only delays back to back cycles. The Bandwidths stated are sustained bandwidths, not peak.

Note 1: Assumes a Squall Module based DMA Controller, transferring 32 bits per access and keeping up with the memory.

4.4 SHARED DRAM ARBITRATION

The shared DRAM is arbitrated for by all the devices requesting access, the processor, SCV64 VMEbus Interface Controller, DMA Controller and DMA control devices located on the Squall Modules. The arbitration scheme is a full Round Robin. The arbitration circuitry records the last device to be granted by memory. DRAM requests are then dealt with in a rotational priority arbitration.

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4.5 FLASH ROM

The CVME965 provides 2 or 4 Mbytes of sector-programmable Flash ROM for non-volatile code storage. The Flash ROM is mapped to address BEE0 0000h or BEC0 0000, depending on how much Flash is present. After reset, the Flash ROM is mapped to address FEE0 0000h or FEC0 0000h so the i960HD processor can read the Initialization Boot Record (IBR) located in the upper 256 bytes of the ROM. The Breeze initialization code automatically performs this memory map reconfiguration operation after reset while initializing the board. Table 4-3 specifies the types of Flash ROM which may be installed and the resulting amount of memory.

Table 4-3. Flash ROM Memory Types

Device	Amount of Memory
28F016	2 Mbytes
28F032	4 Mbytes

4.6 NON-VOLATILE PARAMETER MEMORY

One 64 Kbyte sector of the Flash ROM on the CVME965 is reserved for the storage of application parameters. The boot parameter block is divided into 4 Kbyte sections, each of which may be used for the storage of a set of boot parameters. The layout and location of the boot parameter block is documented in section 7.6 of this manual. MON960 includes a user command to alter the contents of the boot parameter block. The sysWriteBootBlock() function, supplied by the Breeze Development Environment, can be used by applications to write the block (see section 7.8).

4.7 CONSOLE SERIAL PORT

A single console serial port with an RS-232 line interface has been included on the CVME965. The port is connected to an RJ-11 style phone jack on the adapter, and can be connected to a host system using the included phone jack to DB-25 cable (Cyclone P/N 530-2002).

The serial port is based on a 16C550 UART clocked at 1.843 MHz. The device may be programmed to use this clock with the internal baud rate counters. The serial port is capable of operating at speeds from 300 to 115200 bps, and can be operated in interrupt-driven or polled mode. The 16C550 register set is shown in Table 4-4. For a detailed description of the registers and device operation refer to the 16C550 databook.

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Table 4-4. UART Register Addresses

Address	Read Register	Write Register
B000 0000h	Receive Holding Register	Transmit Holding Register
B000 0004h	Interrupt Enable Register	
B000 0008h	Interrupt Status Register	FIFO Control Register
B000 000Ch	Line Control Register	
B000 0010h	Modem Control Register	
B000 0014h	Line Status Register	
B000 0018h	Modem Status Register	
B000 001Ch	Scratchpad Register	Scratchpad Register LSB of Divisor Latch MSB of Divisor Latch

4.8 COUNTER/TIMERS

On the CVME965, two 32 bit counter/timers are provided by the i960HD processor. Users should refer to the i960Hx Processor User's Manual for the functionality and programming of the counters. The actual clock frequency on these adapters will not exactly match the nominal frequency selected with the frequency switches, and since the internal timers are driven by the system clock, the actual frequencies must be used to calculate timer frequencies. The actual frequencies are given in Table 4-5.

Cyclone provides system calls as part of the Breeze Environment to setup and enable/disable the timers on the CVME965. These calls are documented in section 7.8 of this manual.

Table 4-5. i960 Hx CPU Clock Rates

CPU Frequency Switch Setting	CPU Clock Frequency
16 MHz	16.11 MHz
20 MHz	20.05 MHz
25 MHz	25.06 MHz
33 MHz	33.41 MHz

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4.9 CLOCK FREQUENCY STATUS REGISTER

The operating frequency of the CVME965 can be determined by reading the Clock Frequency Status Register at address B410 0000h. The lowest 3 bits of this register reflect the status of the Frequency Select Switches on the adapter: a 0 in a bit position indicates that the corresponding switch is on; a 1 indicates that the corresponding switch is off. Table 2-1 describes the Frequency Select Switch settings. The Clock Frequency Status Register is a read only register.

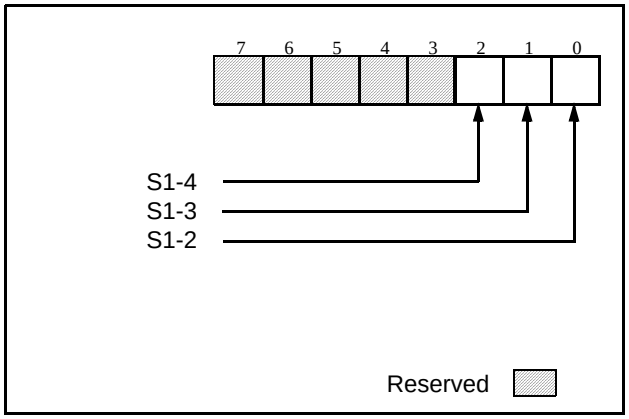


Figure 4-1. Clock Frequency Status Register

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4.10 SERIAL EEPROM INTERFACE REGISTER

Squall II Modules designed by Cyclone include a serial EEPROM used for the storage of Squall II Module parameters. This register acts as an interface to the Squall EEPROM and is used by the initialization code in the Breeze Development Environment™. The Serial EEPROM Interface Register is located at B400 0000h, and is defined below. Squall initialization is handled by Breeze; users whose code will need to access the Serial EEPROM on a Squall Module should consult the MON960 source code provided on the Companion Diskette.

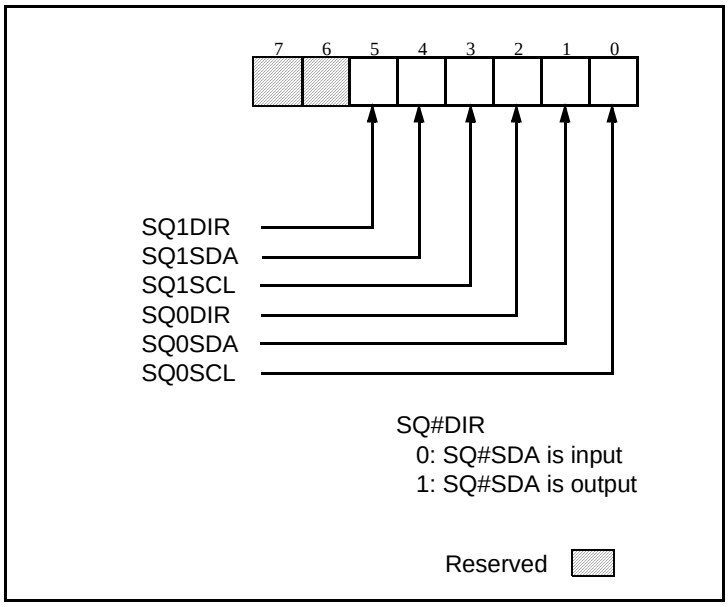


Figure 4-2. Serial EEPROM Interface Register

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4.11 SWITCH AND IPL STATUS REGISTER

A byte register at address B420 0000h is available to allow the processor to read the value of the front panel VME slave address switches and the value of the SCV64 IPL signals. Bits 7-3 correspond to switches A31-A27 respectively. Bits 2-0 read the value of IPL signals 2-0 respectively. The IPL signals can change value at any time. To determine the correct value, the IPL bits should be read repeatedly until the same value appears twice.

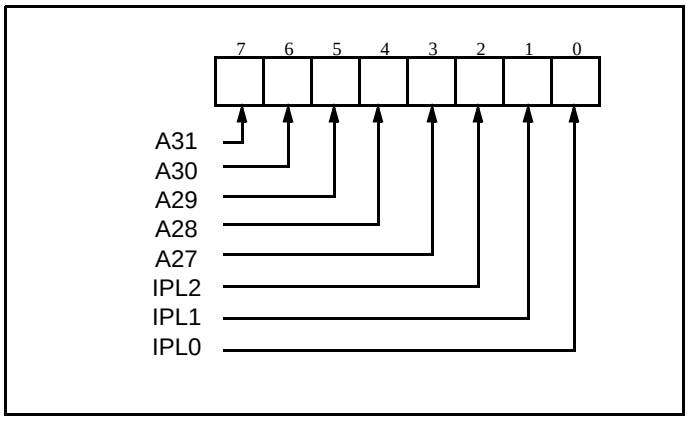


Figure 4-3. Switch and IPL Status Register

4.12 SOFTWARE RESET REGISTERS

Two registers on the CVME965 are used to determine the location of the A16 (VME short space) slave image used to perform a software reset of the board. Both of these registers are byte-wide, and they are located at addresses B430 0000h and B430 0004h. These registers together determine the settings for A7-A15 of the VME short space address. Software Reset Register 0, located at B430 0000h, determines the values for A7-A11 of the short space address. A7 is stored in bit 0 of this register; A11 is stored in bit 4. The remainder of the bits are not writeable. Software Reset Register 1, at address B430 0004h, determines the values for A12-A15 of the short space address, with A12 stored in bit 0 and A15 in bit 3. Bits 4 through 7 of this register are not writeable.

Breeze initialization code will set Software Reset Register 0 to the values of the front panel VME address switches, and Software Reset Register 1 to 0Eh. The resulting short space addresses are shown in Table 2-1, and occupy up to 4Kbytes of A16 space starting at address E000h. If these default addresses conflict with other resources in A16 VME space, they may be changed by user code simply by changing the values stored in the Software Reset Registers.

The Software Reset Registers are write-only registers.

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The software reset feature of the CVME965 is documented fully in section 5.5.

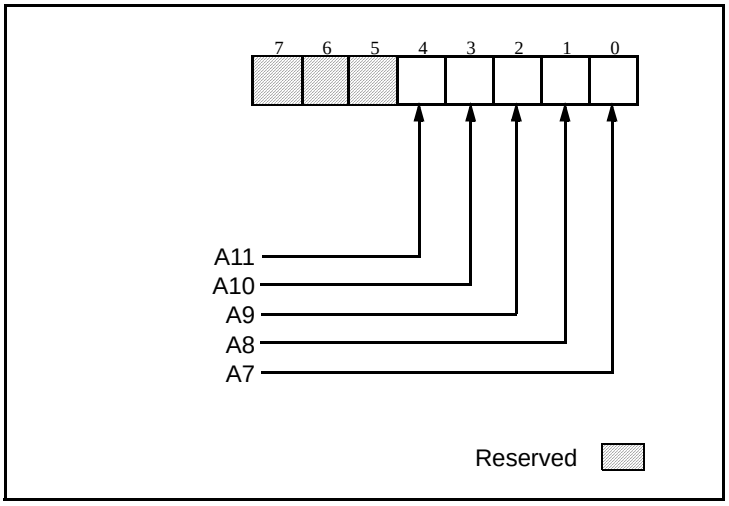


Figure 4-4. Software Reset Register 0

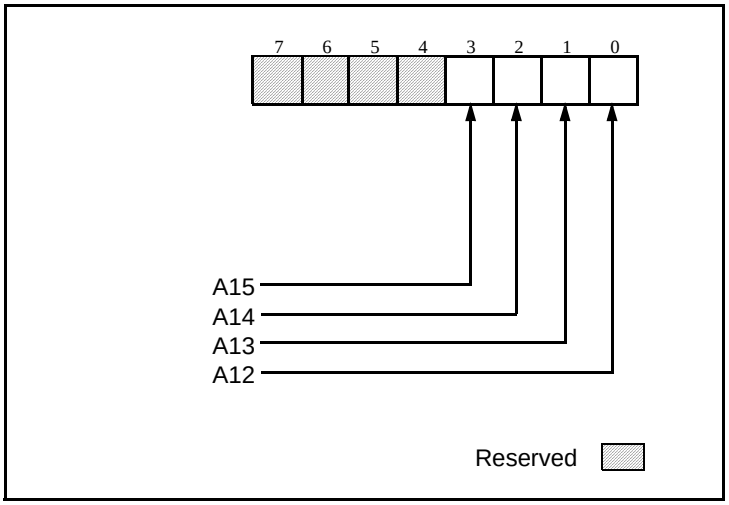


Figure 4-5. Software Reset Register 1

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CHAPTER 5
VME INTERFACE

5.1 VME INTERFACE

The CVME965 uses a SCV64 to provide a very complex and complete VMEbus interface. The SCV64 offers the following features:

- 15 Deep Transmit and Receive FIFOs
- A64, A32, A24, D64, D32 d16 DMA Controller
- Auto SYSCON Identification and Enabling, Without a Jumper
- Location Monitor, Mailbox with 31 Deep Message FIFO
- Full Master/Slave Interface
- Programmable VMEbus Slave Addresses
- VMEbus Interrupter and Interrupt Handler

The SVC64 also "decouples" the local bus and VMEbus by using its transmit and receive FIFOs to perform write posting. Write cycles from one bus are latched in the SCV64 FIFOs and acknowledged. They are then performed on the destination bus without making the source bus wait. Decoupling the busses increases performance by allowing simultaneous pipelined activity to occur on both the local and VME busses.

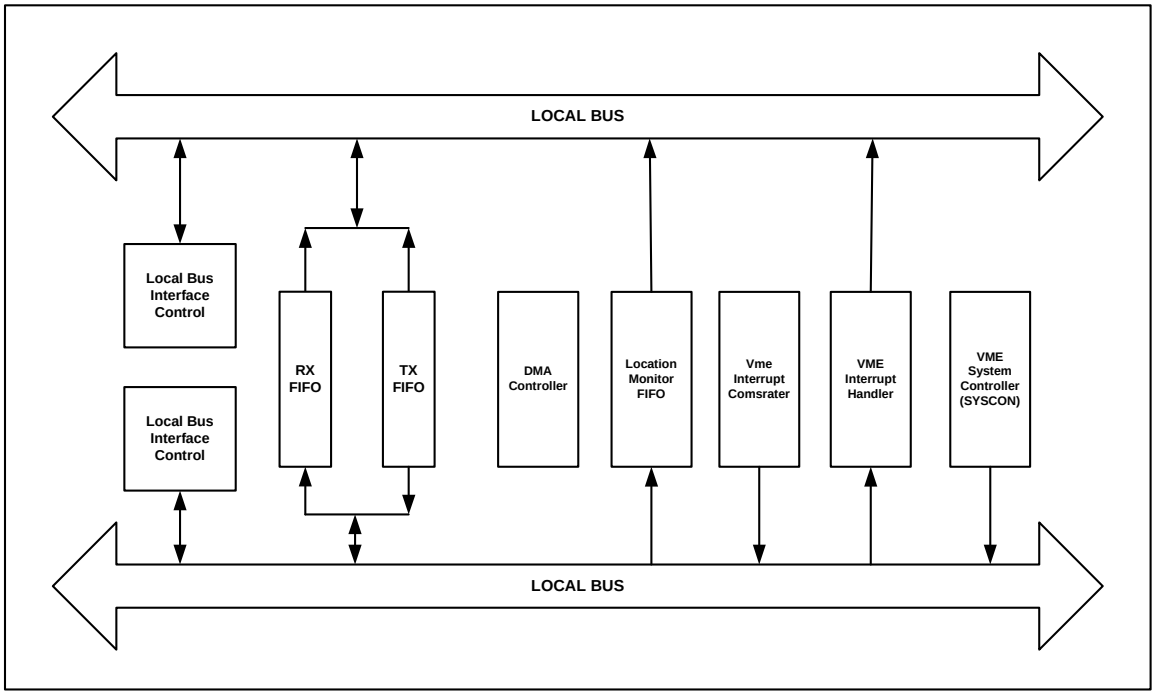


Figure 5-1. SCV64 Block Diagram

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5.2 VMEBUS SYSTEM CONTROLLER

The CVME965 can perform the function of VMEbus System Controller if installed in Slot 0 of a VMEbus card cage. The SCV64 device automatically determines if the CVME965 is the first card on the backplane by sampling the state of the BG3IN* signal during reset. If the signal is being driven by another board the SCV64 determines it should not be system controller. If the BG3IN* signal is not driven by another card, the SCV64 assumes it is in the first slot and enables the system controller functions. The CVME965 can incorrectly decide to be system controller if empty slots are not properly jumpered for the BG3IN* daisy chain signal.

When the system controller functions are enabled, The SCV64 will provide a VMEbus arbiter, SYSCLK signal on the VMEbus, and programmable timeout for cycles on the Data Transfer Bus.

The VMEbus arbiter may be programmed to operate with one of four arbitration schemes. The type of arbitration is controlled by bits 0 and 1 of the SCV64 VARB register at address F400,0094h. Table 5-1 lists the schemes. The default is the full round robin scheme.

The data transfer timeout will determine VMEbus data transfers with the VMEbus BERR* signal. The timeout may be programmed to a period of 16, 32, or 64 usec, or "never". The default value is 64 usecs. Since the i960CF processor does not implement bus faults, a VMEbus cycle terminated with a BERR* is acknowledged on the CVME965 board with unknown data and a VMEBERR interrupt is generated to the processor. This interrupt may be indicated to the processor as a XINT0 if the VMEbus cycle was coupled or as an XINT1 (IRQSCV64) if the cycle was decoupled. Please refer to section 3.9 for handling these interrupts.

Table 5-1. VMEbus Arbitration

ARB1 (VARB bit 1)	ARB0 (VARB bit 0)	Arbitration Mode
0	0	Full Round Robin (Default)
0	1	Priority 3, Round Robin 2, 1, 0
1	0	Priority 3, 2, Round Robin 1, 0
1	1	Full Priority

5.3 VMEBUS MASTER INTERFACE

The SCV64 device provides VMEbus interface control for the CVME965. The SCV64 will implement master VMEbus cycles for the following conditions:

- Transmit FIFO Contains CPU Write Cycles
- CPU Begins a VMEbus Read Cycle
- SCV64 Performs VMEbus IACK Cycle
- SCV64 DMA Controller Initiates VMEbus Read Operation

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The SCV64 can address A32, A24, and A16 VMEbus address spaces and A64, A32 using the DMA controller. D32, D16, D8E0 cycles may be initiated by the processor while D64 and D32 cycles may be initiated by the DMA controller. Table 5-2 shows the levels of VMEbus compliance.

Table 5-2. VMEbus Cycle Types

Characteristic	VMEbus Specification
VMEbus Master	A32, A16, A24/D32, D16, D08(EO), UAT, RMW, BLT, A32/D32, A24/D32, A32/D16, MBLT A64/D64
VMEbus Slave	A32, A24/D32, D16, D08(EO), BLT A32/D32, A32/D64, A32/D16, A24/D32, D08(EO), MBLT A64/D64, A32/D64, RMW, ADO, UAT
Location Monitor (Mailbox)	A32/D32, A24/D32
Interrupt Handler	IH(1-7), D08(O)
Interrupt Generator	I(1-7), D08(O), ROAK

5.3.1 Master Coupled and Decoupled Modes

The receive and transmit channels of the SCV64 can be programmed to operate in coupled or decoupled mode. In coupled master mode accesses, the CPU transfer is not queued by the transmit FIFO but rather the CPU is directly linked to the VMEbus after ownership has been granted. The CPU enters wait states until a VMEbus DTACK* or BERR* is generated by the VMEbus slave. The SCV64 then acknowledges the transfer to the CPU, which then ends the cycle.

CPU read cycles are always coupled, as are read-modify-write operations (also known as RMW or atomic cycles). If the SCV64 transmit channel is in decoupled mode, a pending coupled cycle from the CPU must wait until all the write cycles queued in the FIFO are completed. Data coherency is maintained by preventing read cycles from skipping ahead of uncompleted write cycles.

The SCV64 defaults to decoupled mode. Decoupled mode may be disabled in the SCV64 MODE register at address F400,003C. Setting (1) (bit TXATOM - bit 11, and bit RXATOM - bit 12) disables decoupled mode in the transmit and receive channels respectively.

Processor write cycles to the VMEbus are completed with no wait states when the SCV64 transmit channel is in decoupled mode. The transmit FIFO queues the 32 bit address, 32 bit data and all the control signals needed to perform the cycle on the VMEbus when the cycle arrives at the front of the FIFO. The SCV64 FIFO is 15 stages deep. The SCV64 will request the VMEbus whenever there are entries in the FIFO, or can be programmed to wait until the FIFO is full before requesting the VMEbus. This option is selected by setting the FILL bit (bit 21) in the SCV64 MODE register at address F400,003C. The default of the FILL bit is zero, or request the VMEbus whenever there are entries in the FIFO.

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The SCV64 begins cycles after it has obtained the VMEbus operating with near minimum VMEbus specified timing to start and end each cycle. Address pipelining is used, where the address for the next cycle is placed on the bus as soon as an acknowledge for the current cycle is received.

When a VMEbus BERR* is received by the SCV64, it stops performing VMEbus cycles, sets VBERR (bit 2) in the control and status register, asserts VMEINT* and relinquishes the VMEbus.

The transmit FIFO remains frozen until bit VBERR is cleared by the CPU, and then the SCV64 resumes sending cycles to the VMEbus. To assure data coherency, read and IACK cycles to the VMEbus are blocked until all FIFO entries are processed. The TXCTL, TXADDR, and TXDATA registers in the SCV64 reflect the values that are present at the output stage of the FIFO when the error occurred. They may be read by the CPU to obtain the address, data and control codes in the failed write cycle. This information can be examined by software to determine the fault, or used to rerun the cycle. The failed cycle is not re-run by the SCV64 when the VBERR bit is cleared, as it is no longer in the FIFO, and must be regenerated.

Note that apart from the address there is no information to differentiate CPU cycles from DMA cycles.

If the FIFO is full when the CPU writes to the VMEbus, the SCV64 does not respond until room is available, causing the CPU to enter wait states. The CPU waits for more than 512 usecs for access to the VMEbus, then a timeout is generated to the CPU. This condition is indicated by setting bit LTO flag in the SCV64 Status Register 0 at address F400,0080.

5.3.2 VMEbus Bus Errors (BERR)

VMEbus Slaves generate Bus Error (BERR) signal for several different types of calamities, such as parity errors, accesses to restricted memory spaces, or bus timeouts. Intel's i960 processor family has no provision for BERR exceptions. The CVME965 properly terminates VMEbus cycles which generate BERRs with a READY acknowledge to the i960 processor. An interrupt is then generated to indicate to the processor that garbage has been read or that the write was lost. Coupled VMEbus cycles (all reads, and writes only if the SCV64 is in coupled mode) generate an IRQSCVBERR interrupt on XINT0. Coupled writes and DMA transfers which result in the VMEbus BERR signal being asserted generate the SCV64 signal VMEINT*. VMEINT* is connected to the SCV64 LIRQ5 which in turn generates an XINT1 interrupt the processor. Section 3.6 explains the interrupt structure in more detail. Example code for resolving VMEbus BERRs is available through Cyclone Microsystems.

Note that all VMEbus Errors (BERRs) cause the Transmit FIFO to be locked. The VBERR bit in the MODE register on the SCV64 must be reset in order to continue to use the VMEbus.

5.3.3 Master Read-Modify-Write or Atomic Cycles

The SCV64 supports read-modify-write (RMW) or Atomic Cycles by treating them as a locked group of coupled transfers. The i960CF processor will perform atomic cycles on aligned words only, and therefore the VMEbus specified RMW cycles with AS* active will work as the VMEbus specifies. These include the TASCON bit in the SCV64 MODE register which must be set to a one for proper RMW operation. This bit defaults to zero but is set to one by all Cyclone board initialization software.

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5.4 VMEBUS SLAVE INTERFACE

The CVME965 provides VMEbus master access to the shared DRAM via the SCV64 VMEbus interface controller. VMEbus masters may perform reads, writes, block transfer reads and writes, read modify writes (RMW) cycles, and unaligned transfers to the shared memory. VMEbus masters may also write to the Location Monitor and Mailbox FIFO for inter-processor or inter-process communications. Separate slave images can be set up for A32 and A24 spaces. An A64 slave image is provided for A64 block transfers.

The processor can access its own slave image at the programmed address base without actually requesting the VMEbus. The SCV64 will act as an address decoder to the local shared memory bus, as well as the VMEbus, routing any local bus request for the slave image directly to the shared DRAM. Accessing the shared DRAM in this method is several clock cycles slower than accessing it directly at address E000 0000h but the self access capability can greatly simplify the architecture and implementation of multiprocessor systems.

The CVME965 also presents an A16 slave image on the VMEbus. VMEbus masters accessing this image will cause the target board to be reset. The location of the A16 image in VME short space varies depending on the address switch setting on the front panel of the CVME965. The software reset capability is discussed in section 5.5.

5.4.1 Slave Image Configuration

A32 and A24 slave images are defined in the SCV64 Slave Base Address (VMEBAR) Register. The A32 image base can be programmed to any 128 Mbyte boundary and to any size from 4Kbytes to 128 Mbytes. Cyclone boot ROMs read the front panel VMEbus slave address switches and determine the size of the shared DRAM. The SCV64 is initialized using the front panel switches as the base address of the A32 slave image and the size of the shared DRAM as the size of the slave image.

All values of the front panel VMEbus slave address switches generate acceptable VMEbus slave images, but only the values shown in Table 2-1 allow the processor to access its own slave image.

The SCV64 can also be programmed to present an A24 image which may be programmed to a 512 Kbyte, 1, 2, or 4 Mbyte size. Because of the large size of the shared DRAM and the small size of the A24 address space, Cyclone boot ROMs do not enable A24 address space. Users may enable this space by programming the SCV64 VMEBAR Register with a base address, size value and the MODE Register bit 10 (A24SLVEN) to enable the A24 slave image.

The CVME965 cannot present an A16 slave image to other VMEbus. This image is used for software reset only; none of the memory on the CVME965 is accessible through it. See section 5.5 for more information on the software reset function.

5.4.2 Access Protection

All or part of the A24 and A32 slave image can be protected from VMEbus writes, or reads and writes. If access to a protected area is attempted from the VMEbus, a VMEbus BERR* signal is generated. Protection is not implemented for memory accesses by the local processor to its own slave images.

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Bits 0-3 of the Access Protection Boundary Register (APBR) of the SCV64 device select the protection for the lower part of the slave image. Table 5-3 shows the setting for these bits. Cyclone boot ROMs initialize this register to a default setting of zero, or no protection.

Table 5-3. Access Protect Boundary Settings

Bits 0-3	Function
0	No Protection
1	Lower 64 Kbytes
2	Lower 128 Kbytes
3	Lower 256 Kbytes
4	Lower 512 Kbytes
5	Lower 1 Mbyte
6	Lower 2 Mbytes
7	Lower 4 Mbytes
8	Lower 8 Mbytes
9	Lower 16 Mbytes
A	Lower 32 Mbytes
B	Lower 64 Mbytes
C-F	Entire 128 Mbyte Space

5.4.3 Slave Coupled and Decoupled Mode

VMEbus slave reads always operate in coupled mode. Upon recognizing a request for its slave image, the SCV64 requests the local shared bus and then performs the read to the shared memory. This transfers the data to the VMEbus and asserts the VMEbus DTACK* signal as the data becomes available.

VMEbus slave writes may operate in coupled mode where the VMEbus cycle is acknowledged when the shared memory write has been completed. VMEbus slave writes may also operate in decoupled mode (write posting). In decoupled mode, the writes from the VMEbus are immediately loaded into the receive FIFO, and the VMEbus DTACK* signal is asserted to acknowledge the transfer. The VMEbus is now free to perform other operations. The write is then performed on the local shared DRAM as the resource becomes available. As many as 15 writes can be queued in this fashion. Cyclone boot ROMs enable decoupled slave writes.

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5.4.4 Slave Read-Modify-Write Cycles

The VMEbus implements a locked read-modify-write cycle by maintaining AS* low between the read and the write cycles that form the RMW. During this time the SCV64 retains control of the local shared memory to ensure that the two cycles, the read and write, are one atomic activity and no other device has been able to access the shared memory in between.

5.5 SOFTWARE RESET

The CVME965 includes a software reset function, which allows VMEbus masters to reset the 965 by accessing a special slave image in VME short (A16) space. The location of the software reset image is determined by two Software Reset Registers, which are documented in section 4.12. When a VMEbus master performs a read or write access to the A16 slave image location, logic on the CVME965 will cause the SCV64 to assert a localresest to the CVME965. This will reset the processor and all on-board devices, with the exception of certain VME interface portions of the SCV64. No additional action is necessary; the reset signal will be removed by the SCV64 after 0.25 seconds, and the CVME965 will begin its boot sequence. The system as a whole can continue to function while the CVME965 is in reset. A CVME965 can reset itself using this feature.

The software reset feature is implemented using the $\overline{\text{EXTRST}}$ input to the SCV64. When a read or write to the A16 slave image is letected by on-board logic, the $\overline{\text{EXTRST}}$ signal is asserted, which causes the SCV64 to assert $\overline{\text{LRST}}$, the local reset signal on the CVME965. $\overline{\text{LRST}}$ will be held low for 0.25 seconds, then de-asserted, at which point the CVME965 will boot. Only a short space access will generate the software reset; the on-board logic detects a short space access by monitoring the VME address modifier bits. Address modifiers 29h and 2Dh indicate a short space access. Since the software reset feature is implemented separately from the rest of the VME interface on the CVME965, it will function even if the shared bus on the 965 has somehow been locked and the board is effectively crashed.

The software reset image consumes 128 bytes of VME short space. Any access to any portion of this image, read or write, will cause a reset. The location of the image is determined by the Software Reset Registers. The default settings for the Software REset Registers are described in section 4.12, and can be changed if necessary to prevent address conflicts. The default scheme uses the settings of the VME address switches on the front panel of the CVME965 to fill one of the two registers, and the resulting addresses are shown in Table 2-1. Unless your systme includes other targets which use VME short space addresses E000h through EFFFh, you will not need to change the Software Reset Registers.

5.6 LOCATION MONITOR AND FIFO MAILBOX

The Location Monitor is provided to assist in inter-processor or inter-process communication. It includes a 32 bit wide, 31 entry deep, message FIFO loaded from the data bus, so that either 16 or 32 bit messages or memory pointers can be sent between processes. If an even word is written, the upper 16 bits in the FIFO entry are set to one (1). While there are entries in the FIFO, SCV64 keeps LMINT* asserted to generate an interrupt to the local processor.

The Location Monitor exists at the top longword, and the lower (even) word of the top longword, in each of the A32 and A24 slave images. It is accessible from both the local bus and VMEbus. The Location Monitor replaces the longword of memory which otherwise exists at that address. As a result, writes to the Location Monitor do not enter into memory. A read access to the Location Monitor address asserts BERR* on the VMEbus.

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When the processor writes to its own Location Monitor through a slave image, the transfer does not involve use of the transmit FIFO or the VMEbus. The Location Monitor does not exist at the top of the basic image of local memory, which is selected by address E000 0000h, nor does it respond to accesses to the upper word of the top longword or misaligned-aligned transfers.

The Location Monitor is an address detector which controls the message FIFO. The message FIFO is 32 bits wide by 31 longwords deep and queues the data which is present on the bus writing to it. If the FIFO is full when a Location Monitor write is made, no response is made to the cycle. If the local processor reads an item from the other end of the FIFO while a write is waiting at the other end, then a position becomes available and the write is accepted. Otherwise, the bus expires and ends the cycle with a Bus Error.

When both the processor and VMEbus write to the Location Monitor at the same time, priorities are resolved and both writes are queued according to priorities, as long as there is room for them.

The SCV64 asserts LMINT* while there are entries in the queue and negates it when the queue becomes empty. The LMHD status bit in the SCV64 Control and Status Register is high while the FIFO has data.

Messages in the FIFO are read from SCV64 LMFIFO Register. When the FIFO is empty, further reads return undefined data. The SCV64 does not signal this as an error condition. LMINT* is only asserted while there are entries in the FIFO, so software can poll the signal or use an interrupt service routine to support the Location Monitor.

The default programming of Memory Region F is Big Endian. The Read register of the Location Monitor (Mailbox) FIFO is in region F. A Little Endian processor may have left the data in the FIFO. Software will have to reorganize the bytes to resemble the original data.

5.7 VMEBUS INTERRUPTER

The SCV64 can assert a VMEbus interrupt request signal and issue an interrupt vector during a VMEbus IACK cycle. Interrupt request is asserted via the SCV64 VINT Register. Bits 2-0 indicate the Interrupt Level (7-1) to assert (zero is "no interrupt"). Setting bit 3 to a (1) sets the interrupt active. During an IACK the vector located in the SCV64 IVECT Register is driven onto the VMEbus.

5.8 DMA CONTROLLER

The DMA Controller in the SCV64 can transfer longwords or double longwords from local memory to any A32:D32, A24:D32, A32:D64 or A64:D64 address on the VMEbus. The decoupled mode is used to minimize local and VMEbus ownership. Transfers are always done in longwords (D32 on the VMEbus), in blocks up to 1M longwords (4 Mbytes).

Each D64 transfer is converted to or from two indivisible longword cycles on the local bus. In A64 mode, the high 32 address bits are provided by the Master A64 Base Address Register (MA64BAR) and the lower 32 bits are provided by the DMA VMEbus Address Register (DMAVAR). Data transfers can be configured to occur in discrete, block or multiplexed block modes. Discrete and block modes can be further configured as D32 or D16 widths. These modes are selected in the Mode Control Register. The SCV64 DMAC may transfer up to 4 Mbytes of data, inserting address phases when necessary on the local bus and VMEbus.

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A single read on the local bus is used for each longword, since the DMA loads the VMEbus address directly into the transmit FIFO during the ready cycle. The DMA uses both transmit FIFO and receive FIFO in decoupled mode to support reads from the VMEbus in addition to writes to the VMEbus. DMA transfer direction is controlled by the DMARD bit in the Mode Control Register.

All DMA operations use decoupled mode. Bits RXATOM and TXATOM in the Mode Control Register must be cleared before DMA transfers can be performed.

Five registers are involved in controlling the DMA, one of which is the SCV64 Mode Control Register. Bit DMA24 in this register determines whether DMA transfers occur in the A32 or A24 address space on the VMEbus.

In A24 mode, the SCV64 uses AM code 39 (standard non-privileged data access) and sets A31-A24 to (1) when using the bus, regardless of how those bits are programmed in the DMA Destination Register. In A32 mode, the SCV64 uses AM code 09 (extended non-privileged data access) and uses the destination register as programmed. The DMA24 bit overrides the addressing mode that is implied by the VMEbus address being transferred (A24:D16, etc.). Bit A24PO in the SCV64 Mode Control Register has no effect on the DMA transfers. The SCV64 provides a programming bit in the Mode Control Register that enables selection of the privileged type, either supervisory or non-privileged, for all DMA transfers.

The SCV64 DMA Local Address register provides the local memory address and always points to the next longword to be read. Although the register can be programmed to transfer from any local address in the 0 to 128M range, there are restrictions similar to those on the valid slave image base addresses described earlier. The DMA must transfer data from a block entirely within the slave image.

Advanced features are provided in the SCV64 to tune DMAC and VME performance.

- The transmit FIFO can be configured to begin transfers as soon as data is received, or configured to wait until the FIFO is full. This option is programmed by the FILL bit in the Mode Control Register.
- The bit NOREL (No Release) in the Mode Control Register causes the SCV64 to keep ownership of the VMEbus until the bit is turned off, or the VMEbus ownership timer in the SCV64 can be used in conjunction with the NOREL bit to throttle DMAC use of the VMEbus.

The SCV64 has a DMA VMEbus Address Register (DMAVAR) and a DMA Local Address Register (DMALAR). This provides a consistent register for programming VME and local addresses independent of transfer direction. DMAVAR must always be programmed with the VMEbus address, either as a source or destination. The DMALAR must always be programmed with the local bus address, either as a source or destination.

The SCV64 Transfer Count Register (DMATC) can be programmed to transfer 1,048,576 longwords or 4 Mbytes. This extended transfer count range is enabled only when DTCSIZ is set in the Mode Control Register. When the DTCSIZ bit is set to 0, the DMATC register functions using bits 0-11. When the DTCSIZ bit is set to (1), the SCV64 uses bits 0-19. While DMA is running, the register shows the number of transfers remaining, the DMA stops when the register counts down to zero.

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An additional register, DMA VMEbus Transfer Count (DMAVTC), is provided to indicate the number of VMEbus transfers remaining during DMA BLT and MBLT transfers. The DMA Transfer Count Register (DMATC) indicates the number of local transfers remaining. These values may differ as cycles are queued in the transmit and receive FIFOs.

Before attempting to start a DMA transfer, the following bits must be set by programming the MA64BAR register and the VMEbar register:

- MODE register bit A64BARDY and bit BARDY
- DCSR register bit A64 BARDY and bit BARDY

DMA transfers using A64 must ensure that both the MA64BAR and the VMEBAR registers are programmed as indicated by the corresponding bits A64BARDY and BARDY in the CDSR register before attempting to start a DMA transfer.

The Control and Status Register contains the DMA start and stop control bits DMAGO and DONE. These bits are managed by both the CPU and DMA.

- DMA is started by setting DMAGO to one (1). To set this bit:
  the SCV64 transmit FIFO must be in decoupled mode;
  the slave image must be programmed (indicated by BARDY high); and
  the VBERR and DLBER flags must be cleared.
- Normally the DMA completes the transfer and stops by itself. The DMAGO bit is cleared by the DMA, the DONE bit is set, the VMEINT pin is asserted, and VMEINT is negated when the bit DONE flag in the Control and Status Register is cleared.

The DMA can also be stopped when the CPU writes (0) to the DMAGO bit. The DMA then completes any cycles already pending (one or two). The DMA stops if:

- the SCV64 receives a VMEbus BERR* while writing to the destination; or
- the SCV64 receives a late bus error when BERRCHK is set.

When these errors occur, the DLBER flag or the VBERR flag, in the Control and Status Register, is set, the bit DMAGO is cleared by the DMA and VMEINT is asserted. The DONE bit is not set, as the programmed transfers are not finished by the DMA at this point. VMEINT is negated when the bit DLBER and bit VBERR flags are cleared.

Configuration Errors: If a DMA transfer is attempted when the DMA is incorrectly programmed the CERR bit in the DCSR register is set, and signal VMEINT is asserted. The following configurations result in CERR being set:

MBLT set	and	BLT set
MBLT set	and	D16 set
DMAA64 set	and	MBLT cleared
DMAA64 set	and	DMA24 set
DMARD set	and	RXATOM set
DMARD set	and	LPBK set

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5.9 SCV64 REGISTERS

The SCV64 Control and Status Registers are located at base address $F000,0000. Table 5-4 lists the registers and their functions. The registers must be accessed as 32 bit values. Both this manual and the Newbridge Microsystem manuals refer to specific bits in the registers. The byte ordering assumed is Big Endian. Cyclone boot ROMs set Memory Region F to Big Endian. Thus the bits referred to in the SCV64 are those found in the processors registers. If, for some reason, this region must be set to Little Endian, the software would have to swap the bytes before writing to the SCV64 and after reading the SCV64.

A detailed description of the SCV64 Registers may be found in Appendix A.

Table 5-4. SCV64 Register Map

Longword Register Address	Register	Description
F000 0000h	DMALAR	DMA Local Address
F000 0004h	DMAVAR	DMA VMEbus Address
F000 0008h	DMATC	DMA Transfer Count
F000 000Ch	DCSR	Control and Status
F000 0010h	VMEBAR	VMEbus Slave Base Address
F000 0014h	RXDATA	Rx FIFO Data
F000 0018h	RXADDR	Rx FIFO Address Register
F000 001Ch	RXCTL	Rx FIFO Control Register
F000 0020h	BUSSEL	VMEbus/VSB Bus Select
F000 0024h	IVECT	VMEbus Interrupter Vector
F000 0028h	APBR	Access Protect Boundary
F000 002Ch	TXDATA	Tx FIFO Data Output Latch
F000 0030h	TXADDR	Tx FIFO AM Code and Control Bit Latch
F000 0034h	TXCTL	Location Monitor FIFO Read Port
F000 0038h	LMFIFO	SCV64 Mode Control
F000 003Ch	MODE	Slave A64 Base Address
F000 0040h	SA64BAR	Master A64 Base Address
F000 0044h	MA64BAR	Local Address Generator
F000 0048h	LAG	Local Address Generator
F000 004Ch	DMAVTC	DMA VMEbus Transfer Count

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Longword Register Address	Register	Description
F000 0050h to F000 007Fh	RESERVED	RESERVED
F000 0080h	STAT0	Status Register 0
F000 0084h	STAT1	Status Register 1
F000 0088h	GENCTL	General Control Register
F000 008Ch	VINT	VMEbus Interrupter Requester
F000 0090h	VREQ	VMEbus Requester Register
F000 0094h	VARB	VMEbus Arbiter Register
F000 0098h	ID	ID Register
F000 009Ch	CTL2	Control and Status Register
F000 00A0h	7IS	Level 7 Interrupt Status Register
F000 00A4h	LIS	Local Interrupt Status Register
F000 00A8h	7IE	Level 7 Interrupt Enable Register
F000 00ACh	LIE	Local Interrupt Enable Register
F000 00B0h	VIE	VMEbus Interrupt Enable Register
F000 00B4h	IC10	Local Interrupts 1 and 0 Control Register
F000 00B8h	IC32	Local Interrupts 3 and 2 Control Register
F000 00BCh	IC54	Local Interrupts 5 and 4 Control Register
F000 00C0h	MISC	Miscellaneous Control Register
F000 00C4h to F000 00D0h	RESERVED	RESERVED

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CHAPTER 6
SQUALL II MODULE

6.1 SQUALL II MODULE INTERFACE

This chapter provides design information, electrical and physical specifications of the Squall II Modules allowing users to design and integrate their own Squall Modules. If you are using a standard Squall Module, please refer to the specific module's manual for information on the operation of that module.

The CVME965 contains two locations for Squall II Modules. The modules allow different I/O interfaces to be added to the base single board computer. The modules take advantage of the i960HD's capabilities as an embedded processor and I/O server. Devices on the module may be accessed by the processor in slave mode. Devices with DMA controllers on the Squall Modules may access the shared (packet) DRAM in master mode. I/O signals and connectors may be located on the front panel, each Squall Module having up to 3.3 inches of front panel space. For systems which do not want I/O connectors on the front panel, modules installed in location 1 may make use of the J7 connector to exit I/O signals via the host CVME965's P2 connector. Backplane rows A and C of the P2 connector which are unused by the VMEbus and unbussed by most available backplanes. The J7 connector provides direct connection to the P2 connector pins, rows A and C.

Each Squall Module contains a serial EEPROM which allows the processor to determine the type, revision, and programming information of the specific module. The EEPROM is read via the Squall Serial EEPROM Register. Section 6.4 outlines the use of the EEPROM. Cyclone Microsystems is continuously designing new Squall II Modules. Currently available Squall II Modules are:

SQ01	10 Mbit Ethernet Interface/AUI
SQ02	10 Mbit Ethernet Interface/AUI with VSB interface
SQ04	Two 10baseT Ethernet
SQ06	10/100BaseT4 Ethernet Coprocessor
SQ10	SCSI-2 using NCR53C710
SQ11	SCSI-2 Wide and Fast with SYB 53C720
SQ20	Two high speed serial ports supporting 8 Mbit/sec communications. Ports have EIA-422 drivers and receivers and EIA-530 connectors.
SQ30	ATM interface with DS3 line mapping and physical interface.
SQ32	ATM interface with OC3 155 Mbit/sec Fiber Optics
SQ40	20 bit Parallel Input Port.

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6.2 PHYSICAL ATTRIBUTES

The Squall II Modules are printed circuit boards of which two single sized or one double sized may be mounted on a CVME965 Single Board Computer. Figures 6-1 and 6-3 show the dimensions of the single and double sized Squall II Modules respectively. Figure 6-2 shows the component clearance which applies to both single and double sized modules. The CVME965 has a cutout for both module locations along the front panel to provide larger connecter clearance.

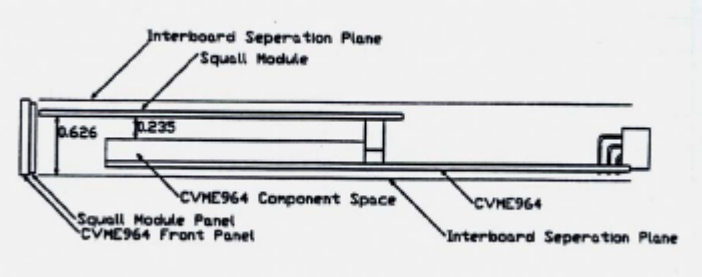


Figure 6-1. Squall II Module Component Height Allowance

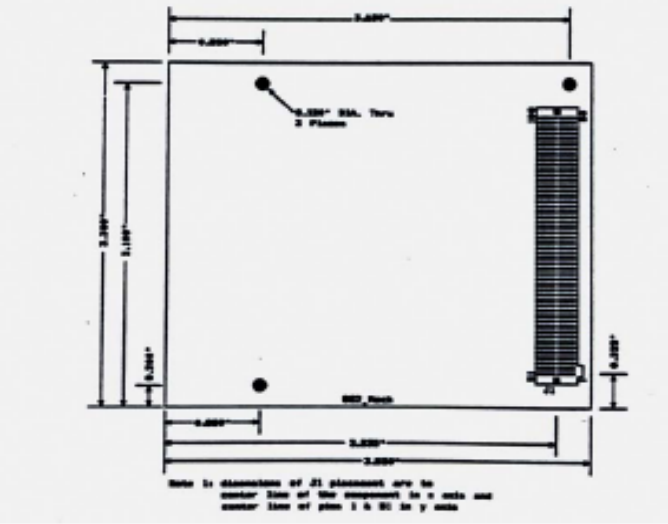


Figure 6-2. Single Sized Squall II Module Dimensions

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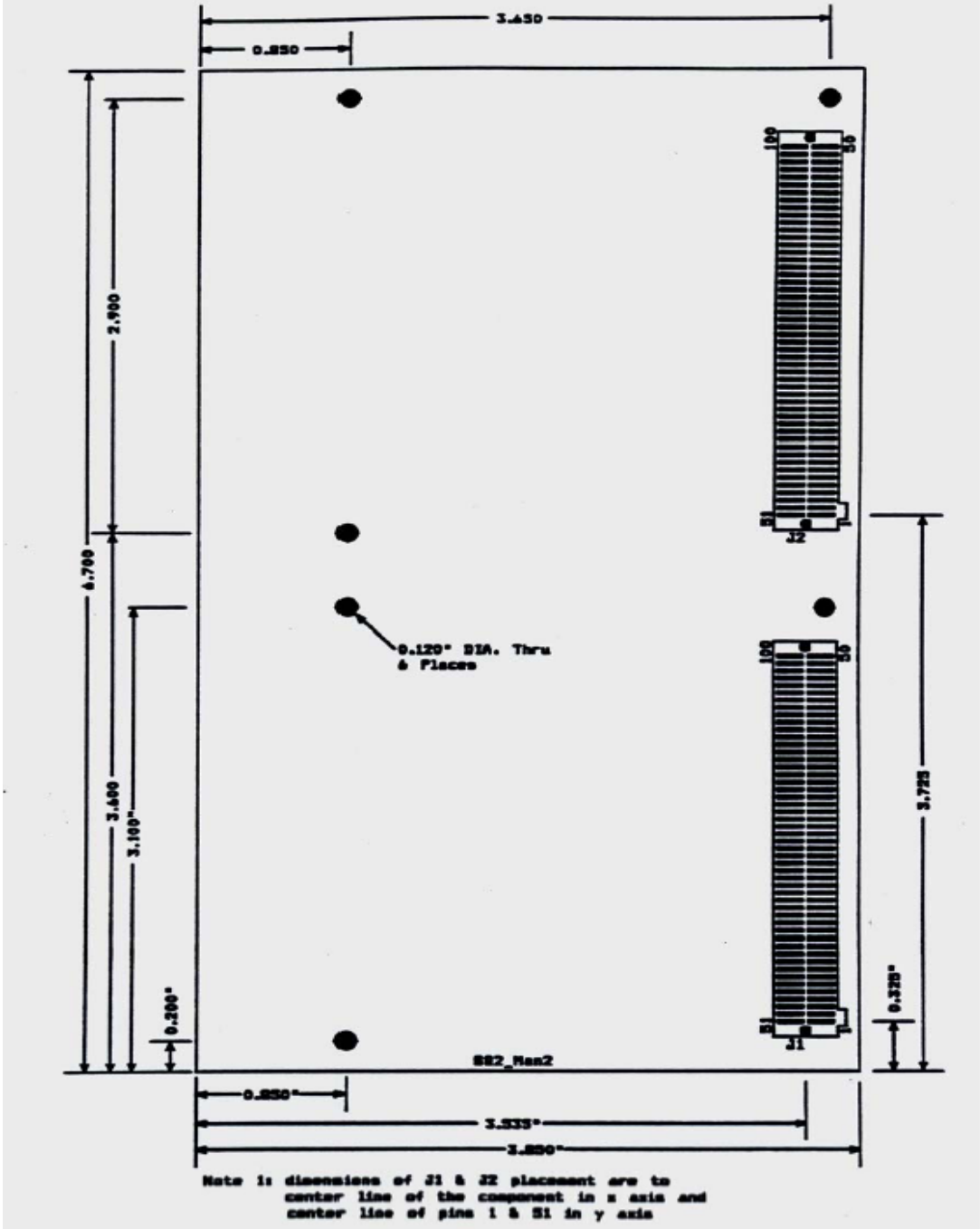


Figure 6-3. Double Sized Squall II Module Dimensions

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6.3 POWER REQUIREMENTS

The Squall Module connectors supply +5v, +12v and -12v. Designers should be careful not to exceed the Amperes listed in Table 6-1. If power is lead off the module via the front panel or the J6/P2 connector, a fuse should be used to prevent damaging the CVME965 due to an incorrect connection.

Table 6-1. Power Supply

Volts	Squall Connector Pins	Maximum Amps
+5v	5 pins	2.5 Amps Maximum
+12v	1 pin	0.5 Amps Maximum
-12v	1 pin	0.5 Amps Maximum
GND	10 pins	-

6.4 SQUALL II MODULE SERIAL EEPROM

Every Squall II Module has a 24C08 serial EEPROM which is used by the host processor to identify the type and revision of the installed module, and to store any system parameters which might be module dependent.

The EEPROMs are read and written serially using Squall Serial EEPROM register at B400 0000h. Users may refer to a data sheet of the 24C08 (section 1.5) for information on how to use the device. Cyclone has already written routines to access these devices. Every boot ROM for the CVME965 reads the serial EEPROMs to properly configure the board. Users wishing to access this code should contact Cyclone's Applications Engineers and indicate a preference in media.

The first 10 bytes have been assigned by Cyclone and have the same function for all Squall Modules. The rest of the memory is assignable by the module's designer and users should refer to the particular module's User's Manual.

The first 4 bytes, (addresses 0-3), contain the module's region configuration word, stored in little endian byte ordering (bits 7-0 in address 0).

The next byte, (address 4), contains two bits indicating the interrupt detection mode of the Squall II Module's interrupts. Interrupts are software configurable in the 80960CA/CF ICON (Interrupt Control Register) to be level low activated or falling edge activated. Bit 0 corresponds to SQIRQ0*, XINT2*, or XINT4*, depending on which location the module is installed. Bit 1 corresponds to SQIRQ1*, XINT3*, or XINT5*. A zero (0) indicates the interrupt is level low activated. A one (1) indicates the interrupt is falling edge activated.

Bytes 5 and 6 are reserved. Bytes 7 and 8 contain the Squall II Module version number in ASCII. Users designing their own modules should request a number from Cyclone Microsystems. Address 9 contains the module's revision level in binary. This field is assigned and incremented by the designer of the module. Bytes 00Ah-7FFh are specific to the module. Please refer to the particular module's User's Manual.

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Like the onboard EEPROM, bytes are read from, and written to, the 24C08 EEPROM most significant bit (bit 7) first and least significant bit (bit 0) last.

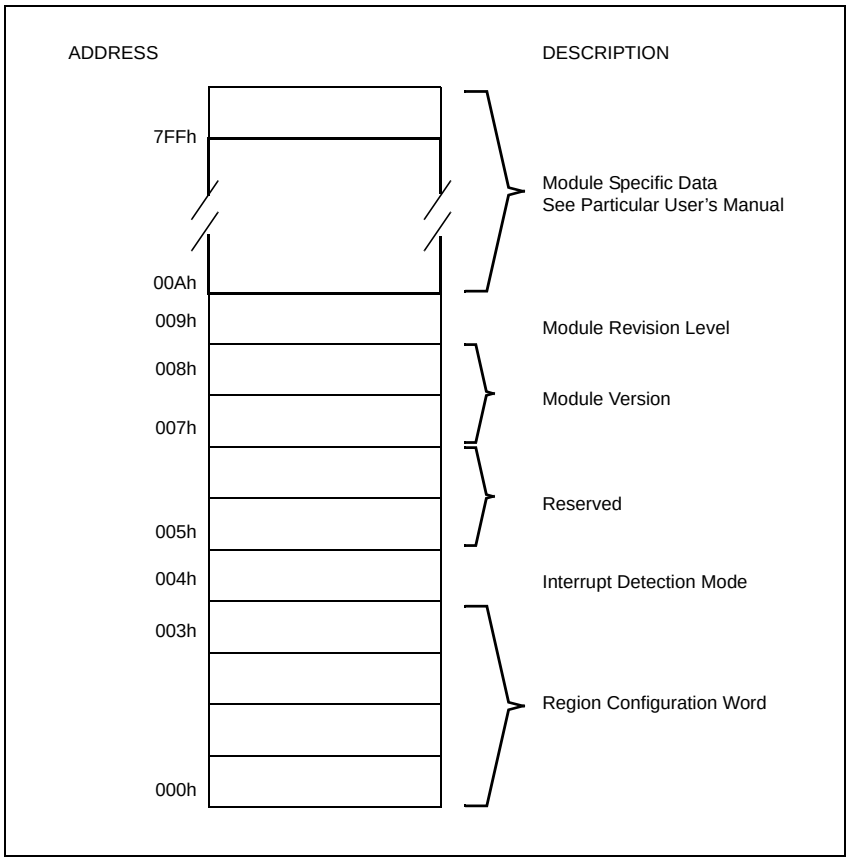


Figure 6-4. Squall II Module EEPROM Memory Map

6.5 SQUALL II MODULE SIGNAL DEFINITIONS

Squall Module devices can be accessed by the processor and may access the shared memory via a 100 pin connector. This section describes the signals provided on the Squall Module interface connector. The signals are an enhanced set of the i960HD external bus signals. Familiarity with the operation of the i960HD external bus will help the user in understanding the Squall Module Interface. Refer to the i960CA Microprocessor User's Manual for detailed explanations.

The signals are described relative to the circuitry on the Squall Module (an input to the CPU or memory would be an output from the Squall Module). Master and slave designations are used to describe different operating modes of the Squall Interface. The Squall Module is a slave when it is being accessed by the processor (SQBG* inactive). The Squall Module is a master when its circuitry has been granted mastership of the shared memory bus (SQBG* asserted by arbitration circuitry in response to a SQBR*). All output and I/O pins have been provided with the proper pull up resistors on the host board and may be left unconnected if desired. Table 6-2 presents the legend for interpreting the pin descriptions.

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Table 6-2. Pin Description Nomenclature

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin may be either an input or an output
-	Pin must be connected as described
S	Synchronous. Inputs are synchronous to PCLK. Outputs must meet setup and hold times relative to PCLK.
A( )	Asynchronous. Outputs may be asynchronous to PCLK. A(E) Edge sensitive output A(L) Level sensitive output
SL( )	While EHOLD* and EHLDA* are inactive, the pin functions in the slave mode. SL(O) Output SL(I) Input SL(I/O) As an input or an output
M( )	When EHOLD* and HLDA* are asserted, the module is in master mode. M(I) Input M(O) Output M(I/O) As an input or output

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6.6 SQUALL II MODULE SIGNAL DESCRIPTIONS

Table 6-3. Squall Module Signal Descriptions

Name	Type	Description
S_A[02:31]	SL (I) M(O) S	Address Bus carries the upper 30 bits of address. The byte enable signals indicate the selected byte in each word.
S_D[00:31]	I/O S	Data Bus carries 32, 16 or 8 bit data depending on the bus width S configured in the Memory Region Table. For a bus width of 8 bits, data lines D[00:07] are used. For 16 bits, D[00:15] are used. For 32 bits, the full bus is used. In master mode, all transfers with the memory use full data bus.
S_BE3* S_BE2* S_BE1* S_BE0*	SL(I) M(O) S	Byte Enables select which of the four bytes addressed by A[02:31] are active during an access to a memory region configured as 32 bits data bus width. The following describes the usage of the Byte Enable Signals in different data bus configurations. 32 bit bus: BE3* - Byte Enable 3 - Enable D[24:31] BE2* - Byte Enable 2 - Enable D[16:23] BE1* - Byte Enable 1 - Enable D[08:15] BE0* - Byte Enable 0 - Enable D[00:07] 16 bit bus: BE3* - Byte High Enable - Enable D[08:15] BE2* - Not Used BE1* - Address bit 1 - A[01] BE0* - Byte Low Enable - Enable D[00:07] 8 bit bus: BE3* - Not used BE2* - Not used BE1* - Address Bit 1 - A[01] BE0* - Address Bit 0 - A[00]
S_W/R	SL (I) M (O) S	Write/Read is low for read accesses and high for write accesses. The operation, read or write, is relative to the bus master.
S_ADS*	SL (I) M (O) S	Address Strobe indicates valid address and the start of a new bus access. S)ADS* is asserted for the first clock of an access.

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Name	Type	Description
S_READY*	SL (O) M (I) S	Ready signals the termination of a data transfer. S_READY* is used to indicate that read data on the bus is valid or that a write data transfer has been completed. In slave mode, the S_READY* signal should be asserted to terminate a cycle indicated by SQSEL*. S_READY* should be tristated until a cycle is indicated by SQSEL*. S_READY* can be enabled at SQSEL* or at the clock cycle prior to the assertion of S_READY*. S_READY* should remain enabled until one clock after the deassertion of S_READY*. In master mode, the memory control circuit asserts S_READY* to indicate that valid read data is on the data bus or that a write transfer is complete.
SQSEL*	I S	Select Squall is a select signal for a processor's 256 Mbyte memory region. The memory region is determined by which module location the Squall Module is installed on. Squall Module 0, the base address is $C000,0000. Squall Module 1, the base address is $D000,0000. The designer must return S_READY* to the processor when this signal is active. SQSEL* is asserted on the rising edge of PCLK if S_ADS* is asserted and A[28:31] = $C or $D is negated on the rising edge of PCLK with S_BLAST* and S_READY* asserted.
S_BLAST*	SL (I) M (O) S	Burst Last indicates the last transfer in a bus access. In slave M(O)mode S_BLAST* is asserted in the data transfer of burst and nonburst accesses after the processor's wait state counter reaches zero. S_BLAST* remains active until the clock following the last cycle of the last data transfer of a bus access. If S_READY* signal is used to extend wait states, the S_BLAST* signal remains active until S_READY* terminates the access. In master mode, this signal should be used to indicate to the shared memory the last cycle of a burst access.
S_EXTEND*	SL (I) M (O) S	Extend may be used by slow Squall Module masters to extend a shared memory read or write cycle. Extend has no meaning for slaves and will always be inactive during slave cycles.
RESET*	I A	Reset asserted should cause all the devices and circuitry on the Squall Module to return to a known state. RESET* will be asserted for a minimum of 200ms. RESET* will always be asserted following power-up.
S_LOCK*	SL (I) M (O) S	Bus Lock indicates that an atomic ready-modify-write operation is in progress.
SQBR*	O	Shared Bus Request signals that the Squall Module circuitry requested access to the shared memory. The local bus arbiter will assert SQBR* to grant the Squall Module bus mastership.

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Name	Type	Description
SQBG*	I S	Shared Bus Grant indicates to a bus requestor that the other shared bus masters have relinquished control of the bus. The Squall Module circuitry may not use the shared bus to access the on board shared memory.
PCLK	I	Processor Output Clock provides a timing reference for all input and output to the processor and the memory.
SQIRQ0*	O	Interrupt Request 0 is directly connected to the processor's external interrupt pin XINT2* or XINT4* depending on which module location the module is installed. This pin may be programmed within the processor as a level (low) or edge (falling) activated interrupt source. The interrupt priority of this pin may also be programmed within the processor.
SQIRQ1*	O	Interrupt Request 1 is the same as SQIRQ0* except that it is connected to the processor's external interrupt pin XINT3* or XINT5* depending on which location the module is installed.
SQSDA	I/O	Serial EEPROM Data
SQSCL	I	Serial EEPROM Clock

6.7 SQUALL II MODULE TIMING

The Squall Interface signals are an enhanced set of the i960HD bus signals. The interface has two modes of operation, slave and master. In slave mode the processor is accessing devices on the Squall Module. In master mode a Squall Module based DMA controller is accessing the shared memory.

6.7.1 Squall II Module Slave Timing

This section outlines the signal timing of the shared memory bus when the i960 processor is reading and writing to the Squall II Module. There are two mandatory conditions. Because the shared memory bus is arbitrated between several masters, and does not use the i960's Hold/Holda signals to perform the arbitration, the Squall II Module memory region must be programmed with ready enabled. The Squall II Module circuitry must also return ready for all assertions of SQSEL*.

The timing diagram in Figures 6-5 and 6-6 shows the timing relationship between the various signals. The diagram shows multiple wait states for read and write cycles and a single wait state for read and write bursts. The number of wait states actually used is totally dependent on the designer of a new Squall II Module.

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Table 6-4. Squall II Module Slave Timing

Name	Minimum	Maximum	Comment
t1	2	18	Clock to Output ADS*
t2	2	10	Clock to Output, S ADS* and SQxSEL*
t4	10		Read S DATA Setup to Clock
t5	2		S DATA hold from Clock
t6	5	20	Clock to Output, S BLAST*, BE<3:0>*
t7	4	18	Clock to Output, S ADDR <31:02>
t8	3	22	Clock to Output, S W/R
t9	12		S READY* Setup to Clock
t10	0		S READY* Hold from Clock
t11	5	20	Clock to Output, S DATA (Write)

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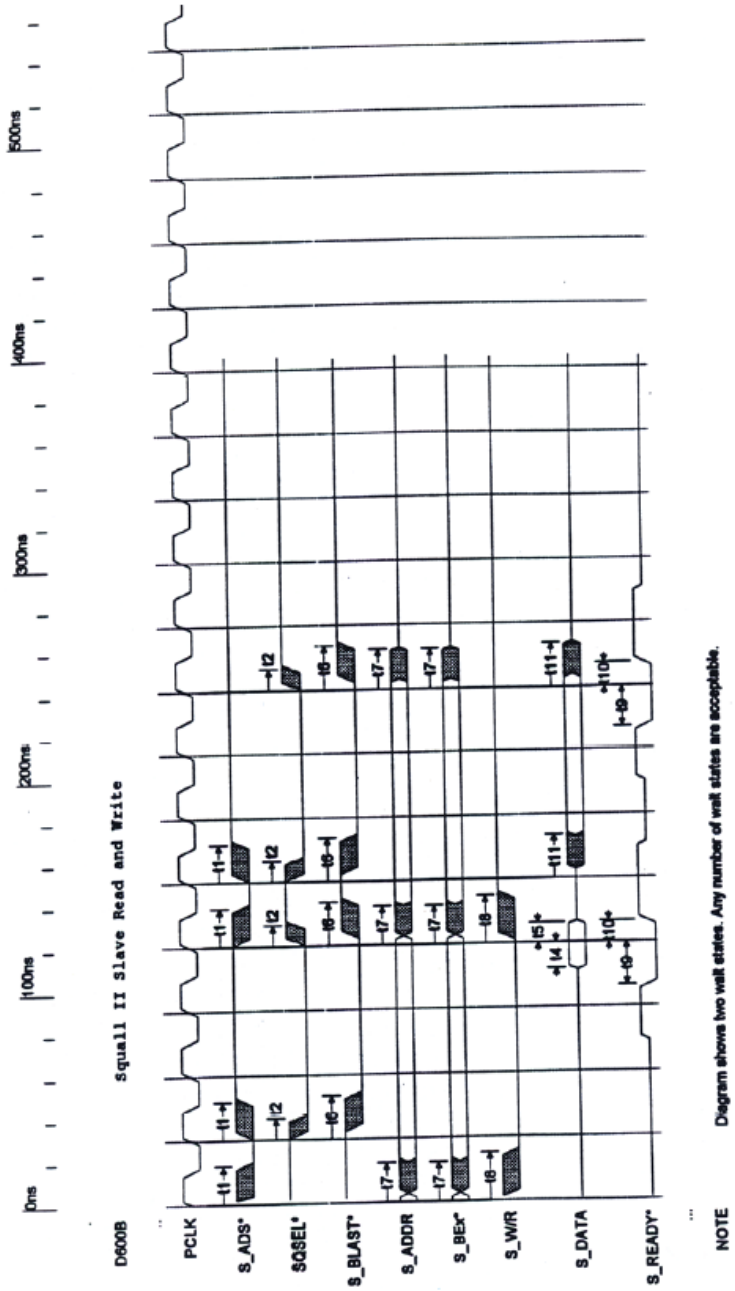


Figure 6-5. Squall II Slave Read and Write Timing Diagram

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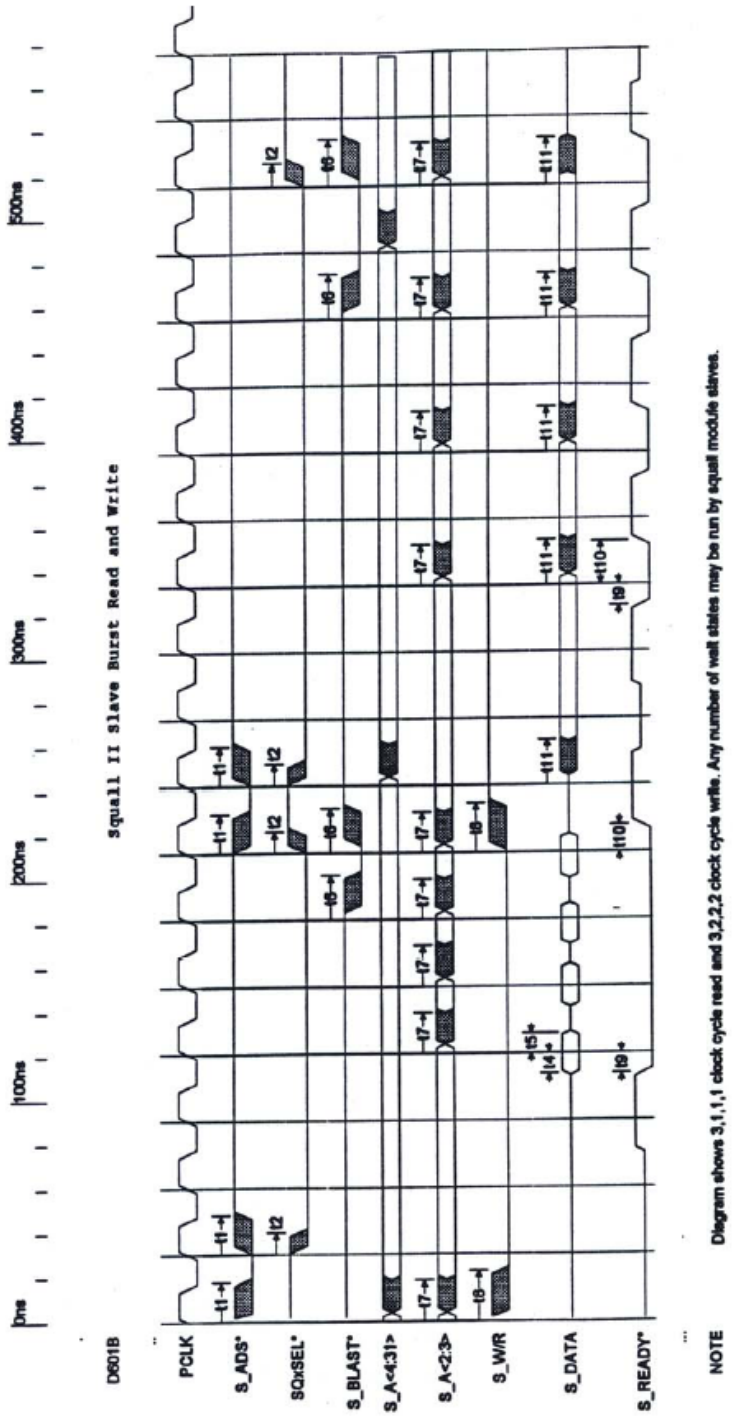


Figure 6-6. Squall II Slave Burst Read and Write Timing Diagram

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6.7.2 Squall II Module Master Timing

Squall II Module circuits may become masters of the shared bus to perform DMA operations to the shared DRAM. DMA controllers gain control of the bus via the SQBR* and SQBG* signals.

All signals, except the interrupt signals, are synchronous to the processor's clock (PLCK). Set up and hold times must be observed for every rising clock edge. Because of the high clock rates, all signals must be driven high before they are tristated. This will ensure that valid levels are observed on every rising clock edge.

DMA controllers gain control of the bus via the SQBR* and SQBG* signals. Memory cycles may then proceed with the same ADS*, BLAST*, and READY* protocol used by the i960HD processor.

Table 6-5. Squall II Module Master Timing

Name	Minimum	Maximum	Comment
t1	3	10	Clock to output SQBG*
t2	10		Setup to clock rising edge for SQBR*, S_ADS*, S_BLAST, S_A[31:02], S_W/R, S_BE[3:0]*
t3	0	20	Clock to output D[31:00], Read Cycle
t4	5		D[31:00] hold from clock, read cycle
t5	3	10	Clock to output READY*
t7	10		Write data setup to clock
t8	0		Write data hold from clock
t9	0	30	SQBG* Inactive to control signals tristated
t10	0		Hold from clock rising edge for SQBR*, S_ADS*, S_BLAST, S_A[31:02], S_W/R, S_BE[3:0]*
t11	0		SQBR* asserted to control outputs driven

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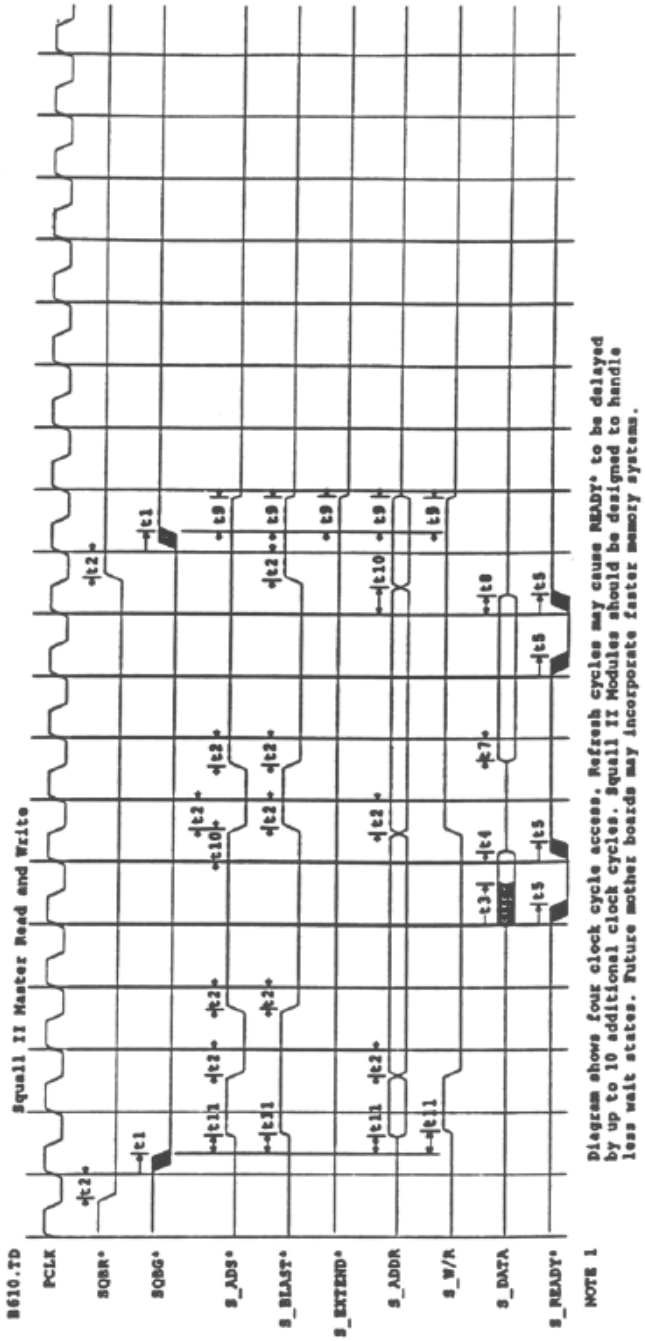


Figure 6-7. Squall II Master Read and Write Timing Diagram

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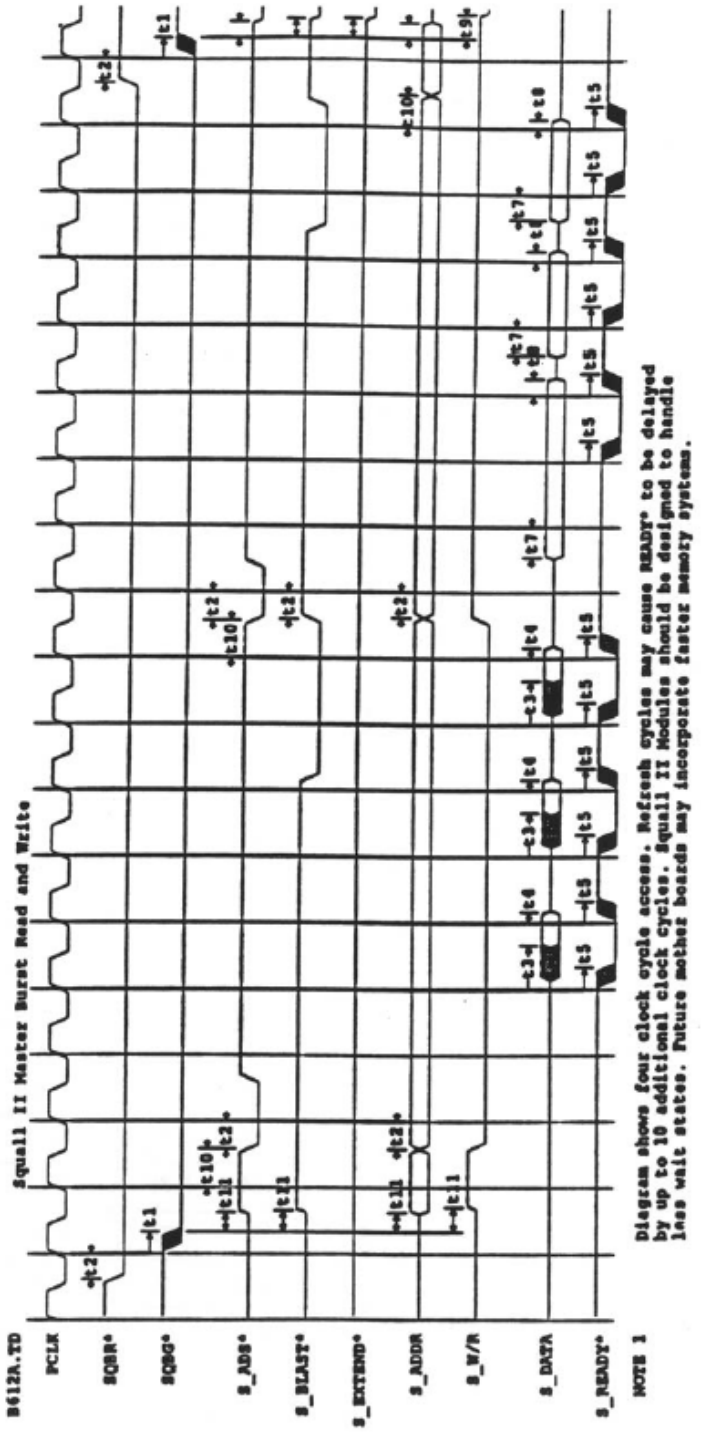


Figure 6-8. Squall II Master Burst Read and Write Timing Diagram

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6.8 SQUALL II MODULE CONNECTOR

The Squall II Module interface uses a 100 pin surface mount connector plug. Samtec part number for the connector is TFM-150-32-SDLC. Table 6-6 gives the pin assignments for the Squall II Module connector.

Table 6-6. Squall II Module Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	S_ADS	21	S_EXTEND*	41	GND	61	S_A22	81	S_A03
2	GND	22	GND	42	S_D15	62	S_A21	82	S_A02
3	PCLK	23	+5V	43	S_D14	63	S_A20	83	+5V
4	GND	24	S_D31	44	S_D13	64	S_A19	84	S_D07
5	S_BLAST*	25	S_D30	45	S_D12	65	S_A18	85	S_D06
6	S_LOCK*	26	S_D29	46	S_D11	66	S_A17	86	S_D05
7	S_W/R	27	S_D28	47	S_D10	67	S_A16	87	S_D04
8	GND	28	S_D27	48	S_D09	68	+5V	88	S_D03
9	S_READY*	29	S_D26	49	S_D08	69	S_A15	89	S_D02
10	RESET*	30	S_D25	50	GND	70	S_A14	90	S_D01
11	S_BE0*	31	S_D24	51	S_A31	71	S_A13	91	S_D00
12	S_BE1*	32	GND	52	S_A30	72	S_A12	92	GND
13	S_BE2*	33	S_D23	53	S_A29	73	S_A11	93	+5V
14	S_BE3*	34	S_D22	54	S_A28	74	S_A10	94	--
15	SQSEL*	35	S_D21	55	S_A27	75	S_A09	95	--
16	GND	36	S_D20	56	S_A26	76	S_A08	96	GND
17	SQIRQ1*	37	S_D19	57	S_A25	77	S_A07	97	SQSDA
18	SQIRQ0*	38	S_D18	58	S_A24	78	S_A06	98	SQSCL
19	SQBR*	39	S_D17	59	+5V	79	S_A05	99	+12V
20	SQBG*	40	S_D16	60	S_A23	80	S_A04	100	-12V

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6.9 SQUALL II MODULE SIGNAL LOADING AND LOGIC SELECTION

Selection of logic families for Squall II Modules deals mostly with the edge rate of the outputs. CMOS logic families, although they use less power than their bipolar predecessors, can be very noisy due to very fast edges transitioning full 5 volt swings from rail to rail. The high speed 5 volt transitions can result in large under and over shoots, ringing, and ground bounce. Logic families such as ACT, FCT, and ACL all exhibit such tendencies.

We recommend using newer Bic CMOS Logic families such as BCT or ABT. These families, like older TTL logic, switch between 3.5 volts and ground, and contain edge control circuitry.

The same consideration is true for programmable logic. Some manufacturers boast of higher speed parts, but achieve that objective by increasing the signal edge transitions. Designers should evaluate the transitions before deciding to use a part in a Squall II Module design.

The loading of the Squall II Module interface signals is very important. The majority of the signals are bussed between the two Squall II Module connectors, the shared memory, the processor interface, and the VMEbus interface. These signals should be restricted to two loads on each Squall II Module. Some signals are routed to an individual Squall II Module and, therefore, may be more heavily loaded. Refer to Table 6-7 for specific loading restrictions.

Table 6-7. Squall II Module Signal Loading

Signal	Loads
S_A, S_D, S_BE*, S_W/R, S_ADS*, S_READY*, S_BLAST*, S_EXTEND*, S_LOCK*	2
SQSEL*	6
RESET*	10
SQBG*	6
PCLK	5

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6.10 SQUALL II MODULE CLOCK TERMINATION

Individual clock signals are driven to each Squall II Module. The clock signals should be terminated with an AC termination of 470pF and 51 ohms to ground as shown in Figure 6-9. Care should be taken to locate the loads close to the end of the signal, especially in double sized modules.

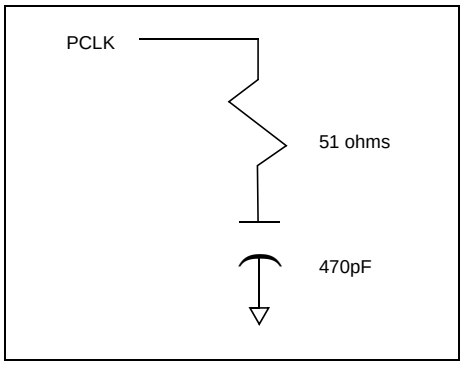


Figure 6-9. Squall II Module Clock Termination

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CHAPTER 7
SOFTWARE DEVELOPMENT

7.1 INTRODUCTION

Developing software for embedded systems can be a difficult, time-consuming task. To simplify the process, Cyclone has created the Breeze Development Environment™ for the CVME965. Breeze is a set of extensions to MON960, the ROM monitor software included with the CVME965, and it incorporates a number of initialization and hardware control routines. Although the Breeze Development Environment is based on MON960, it is accessible from a real-time operating system or user application as well.

The Breeze Development Environment has been designed to make the development cycle on CVME965 as simple as possible. Breeze dispenses with the need for boot PROMs containing application or operating system code, since all downloaded code can be stored in the Flash ROM and started automatically on power up. If no application is selected, or if the autoboot function is aborted, MON960 will assume control of the system. MON960 is present on all CVME965s and its debugging facilities are available during the development cycle. See the MON960 Debug Monitor User's Guide for more information on the operation of the ROM monitor.

Breeze also provides an array of functions which can be called by applications. These functions support local and VME interrupt handling, and processor timer control. They provide the developer with a simple, documented interface to a number of fairly complex hardware functions. The functions are accessed through the i960's system call interface, and are therefore accessible to applications running with MON960, or with a real-time operating system.

Developers should be sure to read Chapter Four of the MON960 User's Guide before building applications for the CVME965. MON960 provides a great deal of support for application development and debugging which is not covered here. In particular, support for console input and output over the serial port is included in MON960, and can be accessed transparently through the standard C libraries provided with the GNU Tools. Consult the MON960 User's Guide, page 5-8 for information on accessing console I/O functions through MON960. In addition, the Command Reference in Chapter 3 explains the commands used to erase the Flash ROM and download code to the CVME965.

7.2 BREEZE DEVELOPMENT ENVIRONMENT™ FEATURES

- Automatic Board-Level Initialization on Reset or Power Up.
- Support for Downloading Application Code
- Erasure and Programming of Flash ROM
- User-Configurable System Boot Parameters Allowing an Application to be Started Automatically After System Initialization
- Timer Control Functions
- Interrupt Handler Installation and Control Functions

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7.3 INITIALIZATION OF THE CVME965

The Breeze Development Environment automatically initializes the CVME965 after a reset or power-up. System DRAM is configured, sized, and cleared, all on-board devices are initialized to a known state, and all interrupts are disabled. The VME bus interface is configured and the necessary memory region information is programmed into its registers (see section 5.1). When initialization is complete control is passed to the autoboot function. If no application is selected for autobooting, or if the autoboot sequence is aborted, MON960 will assume control of the adapter.

7.4 DOWNLOADING CODE

Code is downloaded to the CVME965 via the serial port using the download command in MON960. The object files must be COFF files. Non-COFF-format object files must be converted to COFF files before they can be downloaded through MON960; consult your compiler documentation for information on doing this. Serial downloads are supported at baud rates up to 115,200, and the XModem protocol is used to ensure file integrity. On PC hosts, the Intel application program MONDB can be used to perform file downloads using the command line arguments documented in the MON960 Debug Monitor User's Guide. As the file is downloaded, MON960 examines it to determine what address it has been linked for, and places it there. Incorrectly linked files will cause the download to be aborted. When the download is complete, MON960 will display some information about the downloaded file, and will return to its command prompt.

Applications built with real-time operating systems tend to be fairly large, and downloading them over the serial port can be time consuming. Fortunately, most real-time operating systems allow the creation of a boot PROM, which allows applications to be downloaded to the target board through a faster interface, such as Ethernet. Board support packages for the CVME965 are available from Cyclone for the pSOSystem and VxWorks operating systems, and both of these will allow applications to be downloaded to the adapter via an Ethernet or SCSI interface. The boot PROMs made from these board support packages on the CVME965 are simply applications stored in Flash ROM, and do not perform hardware initialization on the system board, as this will already have been done by the Breeze Development Environment. Additional information can be found in the documentation accompanying the board support packages.

7.5 FLASH ROM PROGRAMMING

The erasure and programming of Flash ROM is actually a standard feature of MON960, but is explained briefly here since it is an integral part of the development cycle.

CVME965 are equipped with 2 or 4 MBytes of sector-programmable Flash ROM. This memory can be erased and reprogrammed in 64Kbyte sectors using programming algorithms included in MON960. Erasure of the Flash ROM is accomplished with the MON960 Erase Flash command, documented in the MON960 Debug Monitor User's Guide. The Flash will be programmed transparently by MON960 during file download, if the object file has been linked for the Flash addresses.

While a file is being downloaded to CVME965, MON960 examines it to determine what address it has been linked for, and places it at that address. Applications linked for the range of memory occupied by Flash ROM will be transparently programmed into Flash ROM by MON960 during downloading (the Flash ROM must be erased first, using the MON960 Erase Flash command). The application may be larger than one Flash sector, as MON960 will transparently program multiple sectors. Flash ROM may be treated as one contiguous memory space from the viewpoint of the linker. Note however that

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MON960 is itself resident in the upper three sectors of Flash ROM (See Figure 7-1), and one additional sector is reserved for the storage of boot parameters. MON960 will not allow these sectors to be erased or programmed, as doing so would render the system unbootable. On systems with 2 MBytes of Flash ROM installed, the Flash begins at address BEE0 0000h. On systems with 4 MBytes, the Flash begins at address BEC0 0000h. Flash "grows downward" so that the boot code stored in the upper sector of the Flash ROM will be located in the correct place regardless of the amount of Flash ROM installed.

Flash ROM is 8-bit wide memory. Performance will be greatly enhanced if applications stored in Flash ROM are copied to system RAM before being executed. The CVME965 Companion Diskette includes a C Runtime Startup file which demonstrates how this is done. Applications linked with this file will automatically be relocated to RAM. Cyclone also includes sample linker directive files on the CVME965 Companion Diskette for linking applications for Flash ROM or RAM. These files will work with the Intel GNU tools; they must be adapted for other compilers.

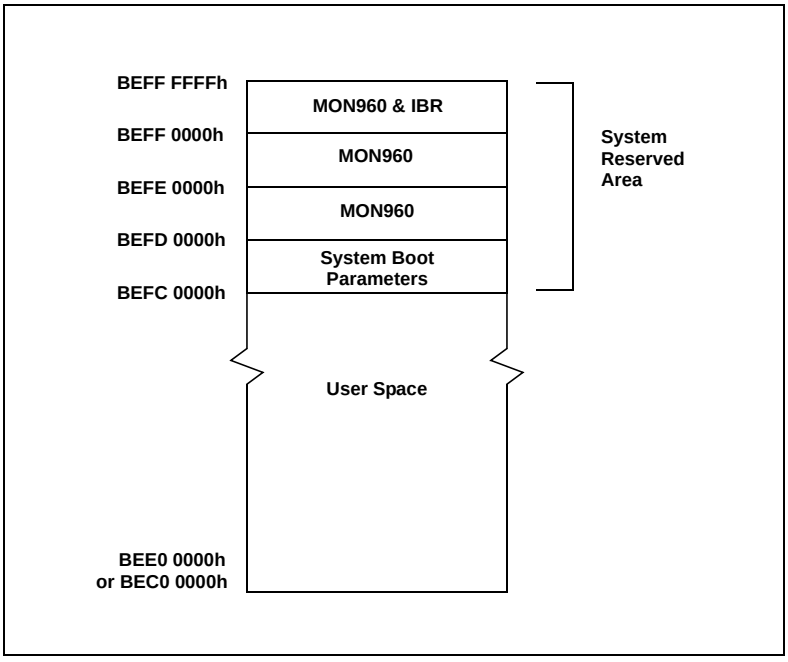


Figure 7-1. Basic System Flash ROM Address Map

7.6 AUTOBOOTING

When system initialization is complete, the Breeze Development Environment checks the contents of the Boot Parameters Sector of the Flash ROM (see section 7.6.1). If the contents are valid, a countdown is started based on the timeout value stored in the Boot Parameters Sector. If communication is initiated over the serial port before the timeout expires, the autoboot will be aborted, and Breeze will start MON960. If the timeout is allowed to expire, Breeze will autoboot using the information contained in the Boot Parameters Sector. Control will be passed to the address stored in the selected boot block, and the application or operating system will be started.

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Autoboot parameters are set from the MON960 command prompt. The sboot command has been added to MON960 to display and modify the contents of the Boot Parameters Sector. The sboot command are documented in section 7.6.2 of this manual.

7.6.1 Boot Parameters Sector

One of the 64 Kbyte sectors in the Flash ROM is reserved for boot parameters. The sector is logically subdivided into sixteen 4 Kbyte boot blocks. The following data structure definitions describe the partitioning of the Boot Parameters Sector. The contents of these structures can be modified using the MON960 sboot command documented in section 7.6.2 and the sysWriteBootBlock call documented in section 7.8.7.

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.

```
typedef struct
{
        long boot_device;
        long boot_timeout;          /* countdown until autoboot */
        long boot_block_id;         /* boot block id to use (VxWorks, pSOS, etc.) */
        unsigned char data_area[4084];
} MON960_BOOT_BLOCK;

typedef struct
{
        unsigned long *start_address;
        unsigned char data_area[4092];
} VXWORKS_BOOT_BLOCK;

typedef struct
{
        unsigned long *start_address;
        unsigned char data_area[4092];
} PSOS_BOOT_BLOCK;


typedef struct
{
        unsigned long *start_address;
        unsigned char data_area[4092];
} USER_BOOT_BLOCK;

typedef struct
{
        MON960_BOOT_BLOCK    mon960;
        VXWORKS_BOOT_BLOCK   vxworks;
        PSOS_BOOT_BLOCK      psos;
        USER_BOOT_BLOCK      user1;
        USER_BOOT_BLOCK      user2;
        USER_BOOT_BLOCK      user3;
        USER_BOOT_BLOCK      user4;
        USER_BOOT_BLOCK      user5;
        USER_BOOT_BLOCK      user6;
        USER_BOOT_BLOCK      user7;
        USER_BOOT_BLOCK      user8;
        USER_BOOT_BLOCK      user9;
        USER_BOOT_BLOCK      user10;
        USER_BOOT_BLOCK      user11;
        USER_BOOT_BLOCK      user12;
} BOOT_PARAMETER_SECTION;
```

Figure 7-2. Boot Parameters Sectors Structures

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7.6.2 sboot MON960 Command

The sboot command (sb) is used to display and modify the contents of the Boot Parameters Sector of the Flash ROM. This command allows the user to set the autoboot timeout and select the boot block in the Boot Parameters Sector which will be used to start the user's application. The sboot facility is accessible only through the command prompt in MON960.

The sboot function accepts three parameters, all of which are optional. If parameters are omitted, the values presently recorded in Flash ROM will be retained. The syntax for the sboot command is:

sb [<autoboot timeout>] [<boot block>] [<start address>]

The autoboot timeout parameter determines the number of seconds the CVME965 will delay before starting the selected application. If a key is hit before this timer expires MON960 will be started instead. The boot block parameter determines which of the 15 boot blocks in the Boot Parameters Sector is used to determine the application starting address. The final parameter is the starting address of the user application and will be stored in the selected boot block. The starting address of MON960 is fixed and cannot be changed.

Entering ‘sb’ with no parameters will display the current autoboot settings.

7.7 SYSTEM CALL SUPPORT

To provide a uniform interface between Breeze System Services and the real-time operating system or user application, the CVME965 employs a system call interface. The system services functions are resident in the Breeze Development Environment and are accessed using the "calls" interface of the i960 processor. The system call mechanism is implemented using the System Procedure Table, a data structure used for storing pointers to system procedures. The procedures are referenced using an index into the table. To access the procedure, the "calls" assembly language instruction is used with the table index as an argument. Figure 7-3 depicts the interface between an application and the Breeze System Services. See the "Procedure Calls" section of the appropriate i960 Processor User's Manual for information regarding the system call mechanism on the i960 processor. Arguments are passed to the Breeze System Services by forcing a C language wrapper routine to pass control to the system function without altering the contents of the global registers used for argument passing in the C language i960 argument mechanism.

In order for the Breeze System Services to function, the current System Procedure Table must contain the System Service entries. If a new PRCB is created the System Service entries must be placed in it. Breeze stores the relevant system procedure information (indices and pointers) in the processor's internal Data RAM. Once the new system procedure table has been established, the system procedure information can be copied from the internal Data RAM to the system procedure table. A routine to perform this copying is included in the CVME965 Companion Diskette.

The header file breeze.h included on the Companion Diskette provides prototypes for the Breeze System Services. The wrapper functions can be found in breeze_asm.s.

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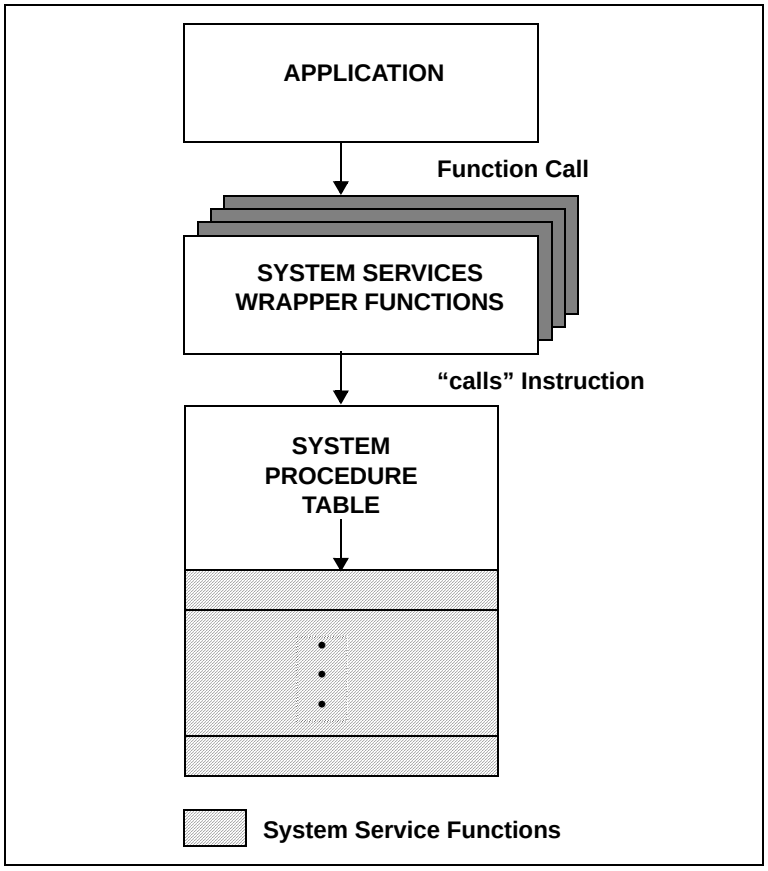


Figure 7-3. CVME965 System Services Hierarchy

7.8 CVME965 SERIES UTILITY ROUTINES

The Breeze Development Environment provides several hardware initialization and control functions. On the CVME965, these consist of interrupt and timer control functions and a routine to write the Flash ROM Boot Sector. The routines are resident in the Breeze Development Environment and are accessed using the system call mechanism described above. The following functions are supported.

In the following descriptions, a return value OK is defined as 0, ERROR is defined as -1.

- sysTimer0Initialization()
- sysTimer1Initialization()
- sysTimer0Enable()
- sysTimer1Enable()
- sysTimer0Disable()
- sysTimer1Disable()
- sysWriteBootBlock()
- sysIsrConnect()
- sysIsrDisconnect()

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- sysVmeIsrConnect()
- sysVmeIsrDisconnect()
- sysVmeIntEnable()
- sysVmeIntDisable()
- sysVmeIntGenerate()

7.8.1 sysTimer0Initialization

This function initializes CPU Timer 0 to act as a periodic interval timer. This routine accepts, as an argument the number of ticks per second (timer interrupts) which should be generated by Timer 0. Periodic interrupts occurring at or below the order of the system interrupt overhead time serve no useful purpose because they cannot be reliably serviced and are therefore not allowed. If an illegal counter value is encountered, this routine will set up the timer for the maximum count or minimum count depending on the input value. Legal values for the ticks per second argument are 1 to 10,000.

Syntax:

```
int sysTimer0Initialization (
    int ticks_per_second
    );
```

Return value: This function returns OK if the timer is successfully initialized. This function returns ERROR if the counter period is invalid.

7.8.2 sysTimer1Initialization

This function initializes CPU Timer 1 to act as a periodic interval timer. This routine accepts as an argument the number of ticks per second (timer interrupts) which should be generated by Timer 1. Periodic interrupts occurring at or below the order of the system interrupt overhead time serve no useful purpose because they cannot be reliably serviced and are therefore not allowed. If an illegal counter value is encountered, this routine will set up the timer for the maximum count or minimum count, depending on the input value. Legal values for the ticks per second argument are 1 to 10,000.

Syntax:

```
int sysTimer1Initialization (
    int ticks_per_second
    );
```

Return value: This function returns OK if the timer is successfully initialized. This function returns ERROR if the counter period is invalid.

7.8.3 sysTimer0Enable

This function enables Timer 0 and its associated interrupt. Before calling this routine, application software should ensure that a Timer 0 interrupt handler is in place and that the system is ready to receive interrupts (i.e. processor priority will allow interrupt service).

Syntax:

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void sysTimer0Enable (void);

Return value: Not applicable.

7.8.4 sysTimer1Enable

This function enables Timer 1 and its associated interrupt. Before calling this routine, application software should ensure that a Timer 1 interrupt handler is in place and that the system is ready to receive interrupts (i.e. processor priority will allow interrupt service).

Syntax:

void sysTimer1Enable (void);

Return value: Not applicable.

7.8.5 sysTimer0Disable

This function disables Timer 0 and its associated interrupt. Timer operation can be resumed using the sysTimer0Enable function. Because Timer 0 is often used as a system clock, caution should be exercised when using this function under a real-time operating system. Disabling the system timer in a multi-tasking environment can cause the system scheduler/dispatcher to become inoperable.

Syntax:

void sysTimer0Disable (void);

Return value: Not applicable.

7.8.6 sysTimer1Disable

This function disables Timer 1 and its associated interrupt. Timer operation can be resumed using the sysTimer1Enable function.

Syntax:

void sysTimer1Disable (void);

Return value: Not applicable.

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7.8.7 sysWriteBootBlock

This routine is used to set or modify one of the system Flash ROM boot blocks in the system boot parameter section. Although the actual data structure of each block is dependent on the application, each block is generically a 4 Kbyte data block. Therefore, a character pointer can be used to access the new data. Since the Flash data is written as an entire block, modifications should be made by first reading the entire 4 Kbyte block from the Flash into a buffer, modifying the buffer, and using this function to write the buffer into the boot parameters sector. This function will replac e the block at array-index with the 4 Kbyte block pointed to by new-block. The array-index parameter corresponds to the values of BOOT_PARAMETER_SECTION shown in Figure 7-2. A 0 indicates the MON960 boot block; 14 indicates User boot block 12. Values greater than 14 are not allowed.

Syntax:

```
int sysWriteBootBlock (
    unsigned char *new_block,
    int array_index
    );
```

Return value: This function returns OK if the Flash ROM write is successful. This function returns ERROR if the index is illegal or if the Flash ROM operation fails.

7.8.8 sysIsrConnect

This function connects an interrupt service routine to a system interrupt. The "xint" parameter is the XINT pin of the i960 processor (0-7). The processor Interrupt Mask Register (IMSK) must be modified by the application after connecting the interrupt service routine to enable the interrupt. Cyclone recommends clearing the appropriate Interrupt Pending Register (IPND) bit before connecting to and enabling an interrupt to prevent spurious interrupt indications. The "handler" parameter is a pointer to an interrupt handler which accepts an integer as an argument and has a void return value. The "arg" parameter is the argument to be passed to the handler when called.

Syntax:

```
int sysIsrConnect (
    int     xint,
    void    (*handler)(int),
    int     arg
    );
```

Return value: This function returns OK if the service routine is successfully connected or ERROR if an argument is invalid.

7.8.9 sysIsrDisconnect

This function disconnects an interrupt service routine from a system interrupt. The "xint" parameter indicates which processor XINT pin the service routine should be disconnected from. This routine disables the appropriate XINT pin in the processor's IMSK register after disconnecting the service routine.

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Syntax:

```
int sysIsrDisconnect (
    int     xint
    );
```

Return value: This function returns OK if the service routine is successfully disconnected or ERROR if an argument is invalid.

7.8.10 sysVMEIsrConnect

This function is used to connect an interrupt handler to a VME interrupt. VME interrupts are serviced by a central routine connected to XINT1 on the CVME965; this function connects the routine at the address pointed to by the handler parameter to the central ISR. If the central ISR detects a VME interrupt with a vector matching that passed in with this function, it will call the user's handler with the argument specified by the arg parameter. This call does not automatically enable the associated VME interrupt; a call to sysVMEIntEnable() may be used for this purpose.

```
int sysVMEIsrConnect (
    int     vector,
    void    (*handler)(int, int),
    int     arg
    );
```

Return value: This function returns OK if the handler is successfully connected or ERROR if one of the input parameters is invalid.

7.8.11 sysVMEIsrDisconnect

This function will disconnect a user handler previously connected via the sysVMEIsrConnect() call. The vector parameter must match the vector passed in during the call to sysVMEIsrConnect(). Disconnecting the handler does not automatically disable the associated VME interrupt; a call to sysVMEIntDisable() may be used for this purpose.

```
int sysVMEIsrDisconnect (
    int     vector
    );
```

Return value: This function returns OK if the handler was disconnected successfully, or ERROR if the vector was invalid.

7.8.12 sysVMEIntEnable

This function is used to enable VME interrupts at the level specified by the input parameter. VME interrupts are masked by level at the SCV64 device; this routine simply clears the interrupt mask for the specified level. Note that multiple VME interrupts may be signaled on the same level. This routine does not enable interrupts from the SCV64 to the i960 processor.

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```
int sysVMEIntEnable (
    int level
    );
```

Return value: This function returns OK if the interrupt level was enabled successfully, or ERROR if the input parameter was invalid.

7.8.13 sysVMEIntDisable

This function is used to disable VME interrupts at the level specified by the input parameter. VME interrupts are masked by level at the SCV64 device; this routine simply sets the interrupt mask for the specified level. Note that multiple VME interrupts may be signaled on the same level. This routine does not disable interrupts from the SCV64 to the i960 processor.

```
int sysVMEIntDisable (
    int level
            );
```

Return value: This function returns OK if the interrupt level was disabled successfully, or ERROR if the input parameter was invalid.

7.8.14 sysVMEIntGenerate

This function is used to generate a VME interrupt on the backplane at the specified level and vector. The user should ensure that a board in the VME system is set up to handle VME interrupts before calling this function. The CVME965 will respond to an IACK cycle on the VME bus by placing the vector specified in the call to this function on the VME bus. This function does not guarantee that previous VME interrupts have been acknowledged before generating a new one.

```
int sysVMEIntGenerate (
    int level,
    int vector
    );
```

Return value: This function returns OK if the VME interrupt was generated successfully, or ERROR if one of the input parameters was illegal. This function does not wait for the interrupt to be acknowledged before it returns.

7.9 CVME965 SERIES DIAGNOSTICS

A suite of board-level diagnostics are included in the CVME965, and are accessed through the MON960 command prompt. To start the diagnostics, type 'po' at the MON960 prompt. The tests are selected from a menu.

These diagnostics are intended to be used only if a problem is suspected with the CVME965 hardware.

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APPENDIX A
SCV64 REGISTERS

The following appendix contains a detailed description of the SCV64 Registers. Along with the description is shown the register's value upon reset. Some bits must be set to specific values for proper operation of the CVME965, their values are indicated and should not be altered. Initialization Code, VMEbus Interrupt Handling, VMEbus Generation Code, and DMA Operation Example Code are available from Cyclone Microsystems. Table A-1 is a list of the registers, followed by individual register descriptions.

Table A-1. SCV64 Register Map

Longword Register Address	Register	Description
F000 0000h	DMALAR	DMA Local Address
F000 0004h	DMAVAR	DMA VMEbus Address
F000 0008h	DMATC	DMA Transfer Count
F000 000Ch	DCSR	Control and Status
F000 0010h	VMEBAR	VMEbus Slave Base Address
F000 0014h	RXDATA	Rx FIFO Data
F000 0018h	RXADDR	Rx FIFO Address Register
F000 001Ch	RXCTL	Rx FIFO Control Register
F000 0020h	BUSSEL	VMEbus/VSB Bus Select
F000 0024h	IVECT	VMEbus Interrupter Vector
F000 0028h	APBR	Access Protect Boundary
F000 002Ch	TXDATA	Tx FIFO Data Output Latch
F000 0030h	TXADDR	Tx FIFO Address Output Latch
F000 0034h	TXCTL	Tx FIFO AM Code and Control Bit Latch
F000 0038h	LMFIFO	Location Monitor FIFO Read Port
F000 003Ch	MODE	SCV64 Mode Control
F000 0040h	SA64BAR	Slave A64 Base Address
F000 0044h	MA64BAR	Master A64 Base Address
F000 0048h	LAG	Local Address Generator
F000 004Ch	DMAVTC	DMA VMEbus Transfer Count
F000 0050h to F000 007Fh	RESERVED	RESERVED

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Longword Register Address	Register	Description
F000 0080h	STAT0	Status Register 0
F000 0084h	STAT1	Status Register 1
F000 0088h	GENCTL	General Control Register
F000 008Ch	VINT	VMEbus Interrupter Requester
F000 0090h	VREQ	VMEbus Requester Register
F000 0094h	VARB	VMEbus Arbiter Register
F000 0098h	ID	ID Register
F000 009Ch	CTL2	Control and Status Register
F000 00A0h	7IS	Level 7 Interrupt Status Register
F000 00A4h	LIS	Local Interrupt Status Register
F000 00A8h	7IE	Level 7 Interrupt Enable Register
F000 00ACh	LIE	Local Interrupt Enable Register
F000 00B0h	VIE	VMEbus Interrupt Enable Register
F000 00B4h	IC10	Local Interrupts 1 and 0 Control Register
F000 00B8h	IC32	Local Interrupts 3 and 2 Control Register
F000 00BCh	IC54	Local Interrupts 5 and 4 Control Register
F000 00C0h	MISC	Miscellaneous Control Register
F000 00C4h to F000 00D0h	RESERVED	RESERVED

Table A-2. DMA Local Address Register

Register Name: DMALAR		Register Number: F000 0000h	
Bits	**Function**		
31 - 24	Not Used (5 bits)	DLA (DMA Local Address)	
23 - 16	DLA (DMA Local Address) - Byte 2		
15 - 08	DLA (DMA Local Address) - Byte 1		
07 - 00	DLA (DMA Local Address) - Byte 0 (Total 27 bits)		0

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Table A-3. DMALAR Description

Name	Type	Condition after Reset	State	Function
DLA 26 - 01 DLA 00	R/W R	U 0	 0	DMA Local Address bits 26 - 01 DMA Local Address bit 00 is always 0

Table A-4. DMA VMEbus Address Register

Register Name: DMAVAR	Register Number: F000 0004h
Bits	**Function**
31 - 24	DVA (DMA VME bus Address) - Byte 3
23 - 16	DVA (DMA VME bus Address) - Byte 2
15 - 08	DVA (DMA VME bus Address) - Byte 1
07 - 00	DVA (DMA VME bus Address) - Byte 0

Table A-5. DMAVAR Description

Name	Type	Condition after Reset	State	Function
DVA 31 - 01 DVA 00	R/W R	U 0	 0	DMA VME bus Address bits 31 - 01 DMA VME bus Address bit 00 is always 0

Table A-6. DMA Transfer Count Register

Register Name: DMATC		Register Number: F000 0008h
Bits	**Function**	
31 - 24	Not Used	
23 - 16	Not Used	DTC (DMA Transfer Count)
15 - 08	DTC (DMA Transfer Count)	DTC (DMA Transfer Count)
07 - 00	(DMA Transfer Count) (Total 20 bits)	

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Table A-7. DMATC Description

Name	Type	Condition after Reset	State	Function	
DTC 19 - 00	R/W	U		DMA Transfer Count: specifies the number of local bus transfers to perform. Summarized as follows:	
				DMA Mode	Register Value
				Non-block, D16 Non-block, D32 BLT, D16 BLT, D32 MBLT	Words Longwords Words Longwords Longwords (Note 1)

Note 1: Bit 00 is read-only value 0, as MBLT VMEbus transfers are double longwords.

Table A-8. Control and Status Register

Register Name: DCSR				Register Number: F000 000Ch				
Bits	Function							
31 - 24	Not Used				Reserved			
23 - 16	Not Used							CERR
15 - 08	TXSHIFT	RETRY	RMCERR	A64BARDY	1	RXSHIFT	RXRST	TXRST
07 - 00	RXHD	TXHD	DLBER	LMHD	LBERR	VBERR	DONE	DMAGO

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Table A-9. DCSR Description

Name	Type	Condition after Reset	State	Function
CERR	R/W	0		Configuration error: asserts VMEINT while 1 Clear by writing 0 to this bit.
			0	No conflicting configurations set
			1	Incompatible options are set
TXSHIFT	R/W	0		Transmit FIFO shift
			R	Clears self: always reads zero
			W0	No effect
			W1	TX FIFO shifts one forward
RETRY	R/W	0		State of VMEbus RETRY* signal during last failed cycle
			0	Not asserted
			1	Asserted
RMCERR	R/W	0		RMC cycle lockup flaf
			R0	Last KBERR was not issued due to RMW lockup
			R1	Last KBERR was issued to RMW lockup
			W0	Clear
			W1	No effect
A64BARDY	R	0		A64 base address ready flag
			0	MA64BAR and SA64BAR registers not programmed yet
			1	Master and slave A64 base addresses are programmed
RXSHIFT	R/W	0		Receive FIFO shift
			R	Clears self: always reads zero
			W0	No effect
			W1	RX FIFO shifts one forward
RXRST	R/W	0		Receive FIFO reset
			R	Clears self: always reads zero
			W0	No effect
			W1	Resets entire receive FIFO

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Name	Type	Condition after Reset	State	Function
TXRST	R/W	0		Transmit FIFO reset
			R	Clears self: always reads zero
			W0	No effect
			W1	Resets Entire Transmit FIFO and any VME-out cycle in progress
RXHD	R	0		Receive FIFO status
			0	Receive FIFO is empty
			1	Receive FIFO has entries
TXHD	R	0		Transmit FIFO status
			0	Transmit FIFO is empty
			1	Transmit FIFO has entries
DLBER	R/W	0		DMA Local Bus Error indicator: asserts VMEINT pin while 1
			R0	No error indicated
			R1	DMA received a local bus error
			W0	Clears DLBER indicator
			W1	No effect
LMHD	R	0		Location Monitor FIFO status: asserts LMINT pin while 1
			0	LM FIFO is empty
			1	LM FIFO has entries

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Name	Type	Condition after Reset	State	Function
LBERR	R/W	0		Local KBERR received while in decoupled mode: asserts VMEINT pin while 1
			R0	No error indicated
			R1	Local bus error received
			W0	Clears LBERR indicator
			W1	No effect
VBERR	R/W	0		VMEbus BERR* received while in decoupled mode: freezes TXFIFO and asserts VMEINT pin while 1
			R0	No error indicated
			R1	VMEbus BERR* received
			W0	Clears BERR* indicator
			W1	No effect
DONE	R/W	0		DMA Done Indicator: asserts VMEINT pin while 1
			R0	DMA not done yet
			R1	DMA finished or stopped by CPU: not set if stopped due to BERR*
			W0	Clear DONE bit
			W1	No effect
DMAGO	R/W	0		DMA Go bit
			R0	DMA is stopped, by self or CPU
			R1	DMA is running
			W0	DMA stop request
			W1	Starts DMA

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Table A-10. VMEbus Slave Base Address Register

Register Name: VMEBAR			Register Number: F000 0010h	
Bits	Function			
31 - 24	Not Used			
23 - 16	Not used	A24SIZ (2 bits)	A24BA (5 bits)	
15 - 08	Not Used			A32SIZ
07 - 00	A32SIZ (Total 4 bits)		A32BA (5 bits)	

Table A-11. VMEBAR Description

Name	Type	Condition after Reset	State	Function
A24SIZ	R/W	U	 0 1 2 3	Sets size of A24 slave image 512K 1M 2M 4M
A24BA	R/W	U	00-1F	Sets base address of A24 slave image. Programmed size of the image will force bits 17 & 16 to zero as appropriate. Bits 20-16 will be compared against VMEbus address bits A23-A19.
A32SIZ	R/W	U	see below	Sets size of A32 slave image
A32BA	R/W	U	see below	Sets base address of A32 image

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Table A-12. A32 Slave Image Size (4 Bit Field)

State	A32 Slave Image Size	State	A32 Slave Image Size	State	A32 Slave Image Size	State	A32 Slave Image Size
0	4K	4	64K	8	1M	C	16M
1	8K	5	128K	9	2M	D	32M
2	16K	6	256K	A	4M	E	64M
3	32K	7	512K	B	8M	F	128M

Table A-13. A32 Slave Image Base Address (5 Bit Field)

State	A32 Slave Image Base Address	State	A32 Slave Image Base Address	State	A32 Slave Image Base Address	State	A32 Slave Image Base Address
0	0000 0000h	8	4000 0000h	10	8000 0000h	18	C000 0000h
1	0800 0000h	9	4800 0000h	11	8800 0000h	19	C800 0000h
2	1000 0000h	A	5000 0000h	12	9000 0000h	1A	D000 0000h
3	1800 0000h	B	5800 0000h	13	9800 0000h	1B	D800 0000h
4	2000 0000h	C	6000 0000h	14	A000 0000h	1C	E000 0000h
5	2800 0000h	D	6800 0000h	15	A800 0000h	1D	E800 0000h
6	3000 0000h	E	7000 0000h	16	B000 0000h	1E	F000 0000h
7	3800 0000h	F	7800 0000h	17	B800 0000h	1F	F800 0000h

Table A-14. RXFIFO Data Register

Register Name: RXDATA	Register Number: F000 0014h
Bits	**Function**
31 - 24	Data Lane at Output Stage of Receive FIFO - Byte 3
23 - 16	Data Lane at Output Stage of Receive FIFO - Byte 2
15 - 08	Data Lane at Output Stage of Receive FIFO - Byte 1
07 - 00	Data Lane at Output Stage of Receive FIFO - Byte 0

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Table A-15. RXDATA Description

Name	Type	Condition after Reset	State	Function
RDATA 31 - 00	R	U		Receive FIFO output data

Table A-16. RXFIFO Address Register

Register Name: RXADDR	Register Number: F000 0018h
Bits	**Function**
31 - 24	Address Lane at Output Stage of Receive FIFO - Byte 3
23 - 16	Address Lane at Output Stage of Receive FIFO - Byte 2
15 - 08	Address Lane at Output Stage of Receive FIFO - Byte 1
07 - 00	Address Lane at Output Stage of Receive FIFO - Byte 0

Table A-17. RXADDR Description

Name	Type	Condition after Reset	State	Function
RADDR 31 - 00	R	U		Receive FIFO output address, except during multiplexed block data transfers in which case D63-D32 are provided here. Upper address bits are zeroed according to the size of slave image programmed that accepted the transfer. No zeroing effect on data received during MBLT transfers.

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Table A-18. RXFIFO Control Register

Register Name: RXCTL				Register Number: F000 001C				
Bits	**Function**							
31 - 24	Not Used							
23 - 16	Not Used							
15 - 08	Not Used							0
07 - 00	0	BLKST	MBLT	BLT	SIZ1	SIZ0	SPC1	SPC0

Table A-19. RXCTL Description

Name	Type	Condition after Reset	State	Function
BLKST	R	U		Flags the start of a block in the FIFO
			0	This cycle is not the start of a block
			1	This cycle is the start of a block
MBLT	R	U		Identifies the entry as being part of an MBLT block
			0	This cycle is not part of an MBLT block
			1	This cycle is part of an MBLT block
BLT	R	U		Identifies the entry as being part of a BLT block
			0	This cycle is not part of a BLT block
			1	This cycle is part of a BLT block
SIZ0, 1	R	U		Data size
			0,0	Longword
			0,1	Byte
			1,0	Word
			1,1	Tri-byte
SPC0, 1	R	U		Receive FIFO TC1, 0 output bits
			0,0	User program space
			0,1	User data space
			1,0	Supervisor program space
			1,1	Supervisor data space

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Table A-20. VMEbus/VSB Bus Select

Register Name: BUSSEL	Register Number: F000 0020h
Bits	**Function**
31 - 24	VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) - Byte 3
23 - 16	VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) - Byte 2
15 - 08	VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) - Byte 1
07 - 00	VSBEN (VMEbus/VSB Data Transfer Cycle Routing Bits) - Byte 0

Table A-21. BUSSEL Description

Name	Type	Condition after Reset	State	Function
VSBEN 31 - 00	R/W	0		Should always be set to 0 for proper operation of CVME965

Table A-22. VMEbus Interrupter Vector

Register Name: IVECT	Register Number: F000 0024h
Bits	**Function**
31 - 24	Not Used
23 - 16	Not Used
15 - 08	Not Used
07 - 00	IVECT (Interrupt Vector)

Table A-23. IVECT Description

Name	Type	Condition after Reset	State	Function
IVECT 07 - 00	R/W	0		VMEbus interrupt vector bits

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Table A-24. Access Protect Boundary Register

Register Name: APBR						Register Number: F000 0028h
Bits	**Function**					
31 - 24	Not Used					
23 - 16	Not Used					
15 - 08	Not Used					
07 - 00	Not Used	APB03	APB02	APB01	APB00	

Table A-25. APBR Description

Name	Type	Condition after Reset	State	Function
APB 03 - 00	R/W	0		Access protection boundary: protection enforced below
			0	No protection
			1	Lower 64 KB
			2	Lower 128 KB
			3	Lower 256 KB
			4	Lower 512 KB
			5	Lower 1 MB
			6	Lower 2 MB
			7	Lower 4 MB
			8	Lower 8 MB
			9	Lower 16 MB
			A	Lower 32 MB
			B	Lower 64 MB
			C	Entire 128 MB
			D	Entire 128 MB
			E	Entire 128 MB
			F	Entire 128 MB

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Table A-26. TXFIFO Data Output Latch Register

Register Name: TXDATA	Register Number: F000 002Ch
Bits	**Function**
31 - 24	Data at Output Stage of Transmit FIFO - Byte 3
23 - 16	Data at Output Stage of Transmit FIFO - Byte 2
15 - 08	Data at Output Stage of Transmit FIFO - Byte 1
07 - 00	Data at Output Stage of Transmit FIFO - Byte 0

Table A-27. TXDATA Description

Name	Type	Condition after Reset	State	Function
TDATA 31 - 00	R	U		Data at transmit FIFO data lane output stage. During D64 cycles this will be D31-D00.

Table A-28. TXFIFO Address Output Latch Register

Register Name: TXADDR	Register Number: F000 0030h
Bits	**Function**
31 - 24	Address Lane at Output Stage of Transmit FIFO - Byte 3
23 - 16	Address Lane at Output Stage of Transmit FIFO - Byte 2
15 - 08	Address Lane at Output Stage of Transmit FIFO - Byte 1
07 - 00	Address Lane at Output Stage of Transmit FIFO - Byte 0

Table A-29. TXADDR Description

Name	Type	Condition after Reset	State	Function
TADDR 31 - 00	R	U		Address at transmit FIFO stage for discrete or non-block DMA transfers. D63-D32 data during multiplexed block transfers.

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Table A-30. Transmit FIFO AM Code and Control Bit Latch

Register Name: TXCTL				Register Number: F000 0034h				
Bits	**Function**							
31 - 24	Not Used							
23 - 16	Not Used							
15 - 08	Not Used							
07 - 00	MBLT	BLT	SIZ1	SIZ0	SPC1	SPC0	SUPER	TYPE

Table A-31. TXCTL Description

Name	Type	Condition after Reset	State	Function
MBLT	R	U		MBLT transfer type flag
			0	This transfer is not part of a MBLT block
			1	This transfer is part of a MBLT block
BLT	R	U		BLT transfer flag
			0	This transfer is not part of a BLT block
			1	This transfer is part of a BLT block

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Name	Type	Condition after Reset	State	Function
SIZ0-1	R	U		Transfer size
			0,0	Longword
			0,1	Byte
			1,0	Word
			1,1	Tri-byte
SPC0-1	R	U		Address space
			0,0	A32
			0,1	Reserved
			1,0	A16
			1,1	A24
SUPER	R	U		Privilege level of transfer
				User
				Supervisor
TYPE	R	U		Data type is CPU transfer
			0	Program
			1	Data
				Data type is DMA transfer
			0	MBLT
			1	BLT or non-block

Table A-32. Location FIFO Read Port

Register Name: LMFIFO	Register Number: F000 0038h
Bits	**Function**
31 - 24	LM (Location Monitor FIFO Output Stage Data) Byte 3
23 - 16	LM (Location Monitor FIFO Output Stage Data) Byte 2
15 - 08	LM (Location Monitor FIFO Output Stage Data) Byte 1
07 - 00	LM (Location Monitor FIFO Output Stage Data) Byte 0

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Table A-33. LMFIFO Description

Name	Type	Condition after Reset	State	Function
LM 31 - 00	R	U		Data at output stage of Location Monitor FIFO

Table A-34. Mode Control

Register Name: MODE				Register Number: F000 003Ch				
Bits	Function							
31 - 24	DCTSIZ	Reserved	RMCRETRY	DMABEN	RMCPIN	BUSSIZs	SWAP	0
23 - 16	DPRIV	NOREL	FILL	DMA64	MBLT	BLT	DMAD16	DMARD
15 - 08	FIFOBEN	BLEN (2 bits)		RXATOM	TXATOM	A24SLVEN	DMA24	BERRCHK
07 - 00	TASCON	A24PO	LPBK	DISRX	A24D1	A16D1	PROT	VINEN

Table A-35. MODE Description

Name	Type	Condition after Reset	State	Function
DTCZIZ	R/W	0	 1	Sets the DMA transfer count size 20 bit transfer count (2M) (Should always be set)
RMCRETRY	R/W	0	 1	Response to RMW cycle deadlock Should always be set to 1 for proper operation
DMABEN	R/W	0	 0 1	DMA local bus burst enable Burst mode disabled for DMA Burst mode enabled for DMA
RMCPIN	R/W	0		RMC pin configuration Not applicable to CVME965
BUSSIZ	R/W	0	 1	Dynamic bus sizing request enable Should always be set to 1 for proper operation

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Name	Type	Condition after Reset	State	Function
SWAP	R/W	0		Work Swap Enable
			0	Should always be set to 0 for proper operation
DPRIV	R/W	0		DMAC privilege type for VMEbus cycles
			0	DMAC uses non-privileged AM codes
			1	DMAC uses supervisory AM codes
NOREL	R/W	0		VMEbus no-release mode
			0	SCV64 will release VMERQ when done
			1	SCV64 will keep VMERQ asserted until VMEGR is negated or until bit is cleared
FILL	R/W	0		Transmit FIFO fill mode
			0	Request VMEbus when any entries are in the FIFO
			1	If DMA is running, wait for FIFO full before requesting VMEbus. If DMA is not running, same as FILL=0
DMAA64	R/W	0		A64 mode control for the DMA
			0	DMAC does not use A64 mode
			1	DMAC uses A64 mode and Master A64 Base Address Register
MBLT	R/W	0		Multiplexed block transfer mode DMAC control
			0	DMAC does not use MBLT mode
			1	DMAC uses MBLT mode
BLT	R/W	0		Non-multiplexed block transfer mode control for DMAC
			0	DMAC does not use BLT mode
			1	DMAC uses BLT mode
DMAD16	R/W	0		Data size for DMAC in non-block and BLT block modes
			0	DMAC uses D32 transfers
			1	DMAC uses D16 transfers
DMARD	R/W	0		DMAC read or write mode
			0	DMAC transfers from local memory to VMEbus
			1	DMAC transfers from VMEbus into local memory

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Name	Type	Condition after Reset	State	Function
FIFOBEN	R/W	0		Receive FIFO burst enable
			0	Disable burst mode for receive FIFO
			1	Enable burst mode for receive FIFO
BLEN 1-0	R/W	0		Local bus maximum burst length
			0	4longwords
			1	8longwords
			2	16longwords
			3	32longwords (not supported)
RXATOM	R/W	0		Receive FIFO coupled and decoupled
			0	RX FIFOs used in decoupled mode
			1	RX FIFOs bypassed (coupled mode)
TXATOM	R/W	0		Transmit FIFO coupled and decoupled
			0	TX FIFOs used in decoupled mode
			1	TX FIFOs bypassed (coupled mode)
A24SLVEN	R/W	0		A24 slave image enable
			0	Image will not respond
			1	Image is enabled
DMA24	R/W	0		DMA destination address size
			0	DMA operates as A32 master
			1	DMA operates as A24 master
BERRCHK	R/W	0		Local late bus error enable
			0	No extra delay inserted
TASCON	R/W	0		AS* modifier for RMW cycles
			0	AS* negated between every VMEbus cycle
			1	AS* not negated between cycles while CPU RMC is asserted
A24PO	R/W	0		VMEbus A24 space address
			0	A24 space located at F800 0000h
			1	A24 space located at 0000 0000h
LPBK	R/W	0		Loopback enable bit
			0	No loopback
			1	Loopback through FIFOs enabled

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Name	Type	Condition after Reset	State	Function
DISRX	R/W	0		Receive FIFO disable bit
			0	Normal operation
			1	FIFO emptied by RXSHFT control bit only
A24D1	R/W	0		Page 0 VMEbus A24 disable bit
			0	A24 responds per A24P0 bit
			1	A24 disabled if in page 0
A16D1	R/W	0		VMEbus A16 disable bit
			0	VMEbus A16 located at FFFF 0000h
			1	A16 space disabled
PROT	R/W	0		Access protection type
			0	Write protection only
			1	Read and Write protection
VINEN	R/W	0		Slave images enabling
			R0	All slave images are disabled
			R1	All programmed images enabled
			W0	Disable all slave images
			W1	Enable all programmed images

Table A-36. Slave A64 Base Address Register

Register Name: SA64BAR	Register Number: F000 0040h
Bits	**Function**
31 - 24	A63 - A56 Address Bits for Slave A64 Base Address
23 - 16	A55 - A48 Address Bits for Slave A64 Base Address
15 - 08	A47 - A40 Address Bits for Slave A64 Base Address
07 - 00	A39 - A32 Address Bits for Slave A64 Base Address

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Table A-37. SA64BAR Description

Name	Type	Condition after Reset	State	Function
SA64B 31 - 00	R/W	U	x	This parameter defines the base address for slave A64 accesses

Table A-38. Master A64 Base Address Register

Register Name: MA64BAR		Register Number: F000 0044h
Bits	Function	
31 - 24	A63 - A56 Address Bits for Master A64 Base Address	
23 - 16	A55 - A48 Address Bits for Master A64 Base Address	
15 - 08	A47 - A40 Address Bits for Master A64 Base Address	
07 - 00	A39 - A32 Address Bits for Master A64 Base Address	

Table A-39. MA64BAR Description

Name	Type	Condition after Reset	State	Function
MA64B 31 - 00	R/W	U	x	A64-A32 address bits during master A64 DMA transfers

Table A-40. Local Address Generator

Register Name: LAG		Register Number: F000 0048h
Bits	Function	
31 - 24	Not Used (5 bits)	Local Address Generator Value
23 - 16	Local Address Generator Value	
15 - 08	Local Address Generator Value	
07 - 00	Local Address Generator Value (Total 27 bits)	

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Table A-41. LAG Description

Name	Type	Condition after Reset	State	Function
LAG 26 - 00	R/W	U	x	This is the next local address to be used in block mode transfers received from the VMEbus, either as a slave or by DMAC transfers from the VMEbus to a local memory

Table A-42. DMA VMEbus Transfer Count

Register Name: DMAVTC		Register Number: F000 004Ch
Bits	Function	
31 - 24	Not Used	
23 - 16	Not Used	DMA VMEbus Transfer Count
15 - 08	DMA VMEbus Transfer Count	
07 - 00	DMA VMEbus Transfer Count (Total 20 bits)	

Table A-43. DMAVTC Description

Name	Type	Condition after Reset	State	Function
DMAVTC 19 - 00	R	U	0	The number of VMEbus cycles remaining to perform in the BLT or MBLT DMA transfer

Table A-44. Status Register 0

Register Name: STAT0				Register Number: F000 0080h				
Bits	Function							
07 - 00	CLRDOG	CLRTIK	LTO	VI1	SYFIP	ACFIP	MEMIP	NMIIP

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Table A-45. STAT0 Description

Name	Type	Condition after Reset	State	Function
CLRDOG	R/W	0		Watchdog clear and restart
			W0	No effect
			W1	If 0 before write, resets
				If 1 before write, no effect
CLRTIK	R/W	0		Clear TICK signal
			R	Always reads as zero
			W0	TICK pin cleared to high
			W1	No effect
LTO	R/W	0		Local Bus Time Out flag
			R0	No time-out has occurred
			R1	Local bus time-out occurred
			W0	Clears LTO bit to zero
			W1	No effect
VI1	R	X		VMEbus IRQ1* (BI-mode line)
			0	IRQ1* is not asserted
			1	IRQ1* is asserted
SYFIP	R	X		SYSFAIL* pin
			0	Pin is not asserted
			1	Pin is asserted
ACFIP	R	X		L7IACF Interrupt Pin
			0	Pin is not asserted
			1	Pin is asserted
MEMIP	R	X		L7IMEM Interrupt Pin
			0	Pin is not asserted
			A	Pin is asserted
NMIIP	R	X		L7INMI Interrupt Pin
			0	Pin is not asserted
			1	Pin is asserted

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Table A-46. Status Register 1

Register Name: STAT1				Register Number: F000 0084h				
Bits	Function							
07 - 00	1	0	SYSC	BI	PWRUP	IDGOT	BG2IN	BG1IN

Table A-47. STAT1 Description

Name	Type	Condition after Reset	State	Function
SYSC	R/W	X		VMEbus SYSCON mode bit
			0	SCV64 is not SYSCON
			1	SCV64 is SYSCON
BI	R	1		BI-mode indicator
			0	SCV64 is not in BI-mode
			1	SCV64 is in BI-mode
PWRUP	R	X		Power-up indicator
			0	Last reset was not by power up
			1	Last reset was due to power up
IDOGT	R	X		Auto-ID completion indicator
			0	Auto-ID cycle not done yet
			1	Auto-ID cycle completed
BG2IN	R	X		Bus Grant 2 In pin
			0	BG2IN* is low or SCV64 isn't SYSCON
			1	BG2IN* is high and SCV64 is SYSCON
BG1IN	R	X		Bus Grant 1 In pin
			0	BG1IN* is low or SCV64 isn't SYSCON
			1	BG1IN*A is high and SCV64 is SYSCON

Table A-48. General Control Register

Register Name: GENCTL				Register Number: F000 0088h				
Bits	Function							
07 - 00	SWRST	ABI	SBI	TLEN1	TLEN0	LTOEN	IDTST	VI1BI

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Table A-49. GENCTL Description

Name	Type	Condition after Reset	State	Function
SWRST	R/W	0		Software Initiated System Reset
			0	No effect
			1	Initiates reset
ABI	R/W	0		Assert BI-mode line (IRQ1*)
			0	De-assert IRQ1*
			1	Assert IRQ1*
SBI	R/W	0		Self BI-mode line (IRQ1*)
			0	De-assert self BI-mode control
			1	Set self into BI-mode
TLEN1 TLEN0	R/W	3		Tick timer length code Norm
			0	5 ms
			1	10 ms
			2	50 ms
			3	100 ms
LTOEN	R/W	1		Local Bus Time-out Enable
			0	Disable time-out
			1	Enable time-out
IDTST	R/W	0		Auto-ID Test bit
			W0	No effect
			W1	If previously 0, increment ID
			W1	If previously 1, no effect
VI1BI	R/W	1		IRQ1* Configuration Control bit
			0	IRQ1* as interrupt only
			1	IRQ1* as BI-mode line only

Table A-50. VMEbus Interrupt Requester

Register Name: VINT				Register Number: F000 008Ch				
Bits	Function							
07 - 00	0	0	0	0	INT	IL2	IL1	IL0

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Table A-51. VINT Description

Name	Type	Condition after Reset	State	Function
INT	R/W	0		Interrupt Control and Status bit
			R0	No interrupt is pending
			R1	Interrupt is presently asserted
			W0	No effect: does not change to 0
			W1	Assert interrupt
IL2 IL1 IL0	R/W	0	 0 1-7	Interrupt Level Interrupter clears itself Sets interrupt level

Caution: Changing the interrupt level while INT is state 1 may cause improper operation in the IACK DCD logic.

Table A-52. VMEbus Requester Register

Register Name: VREQ				Register Number: F000 0090h				
Bits	Function							
07 - 00	OTEN	BCEN	REL	REQ	OT1	OT2	LVL1	LVL0

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Table A-53. VREQ Description

Name	Type	Condition after Reset	State	Function
OTEN	R/W	1		VMEbus Ownership Timer Enable
			0	Disable timer
			1	Enable timer
BCEN	R/W	0		Bus Clear Recognition Control
			0	Ignore BCLR* signal
			1	Release bus if BCLR* asserted
REL	R/W	1		VMEbus Release Mode Control
			0	Release on request (ROR)
			1	Release when done (RWD)
REQ	R/W	1		VMEbus Request Mode Control
			0	Fair
			1	Demand
OT1 OT0	R/W	3		VMEbus Ownership Timer (Time-out Period)
			0	Zero
			1	2 usec
			2	4 usec
			3	8 usec
LVL1 LVL0	R/W	3		VMEbus Request Level
			0	Level 0

Table A-54. VMEbus Arbiter Register

Register Name: VARB				Register Number: F000 0094h				
Bits	Function							
07 - 00	0	0	VXL1	VXL0	0	ATEN	ARB1	ARB0

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Table A-55. VARB Description

Name	Type	Condition after Reset	State	Function
VXL1 VXL0	R/W	3	 0 1 2 3	Data Transfer Time-out Period Never 16 usec 32 usec 64 usec
ATEN	R/W	1	 0 1	Arbitration Time-out Enable Disable arbitration time-out Enable arbitration time-out
ARB1 ARB0	R/W	0	 0 1 2 3	Arbitration Mode Round Robin all four levels Priority 3, Round Robin 2, 1, 0 Priority 3, 2, Round Robin 1, 0 Priority all four levels

Table A-56. ID Register

Register Name: ID				Register Number: F000 0098h				
Bits	Function							
07 - 00	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Table A-57. ID Description

Name	Type	Condition after Reset	State	Function
ID	R	0	 n	Auto-ID Card Slot ID Value of ID counter

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Table A-58. Control and Status Register

Register Name: CTL2				Register Number: F000 009Ch				
Bits	Function							
07 - 00	0	0	MYBBSY	1	0	LBRAM	MEMIM	TICKM

Table A-59. CTL2 Description

Name	Type	Condition after Reset	State	Function
MYBBSY	R	0		SCV64 BBSY* Output
			0	BBSY* is not asserted
			1	BBSY* is driven low
LBRAM	R/W	0		Local Bus Requester Mode
			0	Channels 0 and 1 fair
			1	Channel 1 pre-empts channel 0
MEMIM	R/W	1		L7IMEM effect on requester
			0	L7IMEM does not affect requester
			1	L7IMEM forces requester to release VMEbus
TICKM	R/W	0		Tick Speed
			0	Normal rates
			1	Fast rates

Table A-60. Level 7 Interrupt Status Register

Register Name: 7IS				Register Number: F000 00A0h				
Bits	Function							
07 - 00	0	0	0	BIS	SYFIS	ACFIS	MEMIS	NMIIS

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Table A-61. 7IS Description

Name	Type	Condition after Reset	State	Function
BIS	R/W	X		BI-mode Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
SYFIS	R/W	0		SYSFAIL* Pin Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
ACFIS	R/W	0		L7IACF Pin Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
MEMIS	R/W	0		L7IMEM Pin Interrupt
			0	Interrupt is not asserted
			1	Interrupt is asserted
NMIIS	R/W	X		L7INMI Pin Interrupt (Not Used)

Table A-62. Local Interrupt Status Register

Register Name: LIS				Register Number: F000 00A4h				
Bits	Function							
07 - 00	0	0	LI5	LI4	LI3	LI2	LI1	LI0

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Table A-63. LIS Description

Name	Type	Condition after Reset	State	Function
LI5	R/W	X		Local Interrupt Five (LIRQ5)
			0	LIRQ5 pin is not asserted
			1	Interrupt pin is asserted
LI4	R/W	X		Local Interrupt Four (LIRQ4)
			0	LIRQ4 pin is not asserted
			1	Interrupt pin is asserted
LI3	R/W	X		Local Interrupt Three (LIRQ3)
			0	LIRQ3 pin is not asserted
			1	Interrupt pin is asserted
LI2	R/W	X		Local Interrupt Two (LIRQ2)
			0	LIRQ2 pin is not asserted
			1	Interrupt pin is asserted
LI1	R/W	X		Local Interrupt One (LIRQ1)
			0	LIRQ1 pin is not asserted
			1	Interrupt pin is asserted
LI0	R/W	X		Local Interrupt Zero (LIRQ0)
			0	LIRQ0 pin is not asserted
			1	Interrupt pin is asserted

Table A-64. Level 7 Interrupt Enable Register

Register Name: 7IE				Register Number: F000 00A8h				
Bits	Function							
07 - 00	0	0	0	BIE	SYFIE	ACFIE	MEMIE	NMIIE

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Table A-65. 7IE Description

Name	Type	Condition after Reset	State	Function
BIE	R/W	0		BI-mode Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
SYFIE	R/W	0		SYSFAIL* Pin Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
ACFIE	R/W	0		L7IACF Pin Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
MEMIE	R/W	0		L7IMEM Interrupt Enable
			0	Disable interrupt
			1	Enable interrupt
NMICLR	R/W	1		L7INMI Pin Interrupt Clear
			R	Always reads one
			W0	Clear interrupt: remains enabled
			W1	No effect: always enabled

Table A-66. Local Interrupt Enable Register

Register Name: LIE				Register Number: F000 00ACh				
Bits	Function							
07 - 00	0	0	L5E	L4E	L3E	L2E	L1E	L0E

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Table A-67. LIE Description

Name	Type	Condition after Reset	State	Function
L5E	R/W	0		Local Interrupt 5 (LIRQ5) Enable
			0	Disable interrupt
			1	Enable interrupt
L4E	R/W	0		Local Interrupt 4 (LIRQ4) Enable
			0	Disable interrupt
			1	Enable interrupt
L3E	R/W	0		Local Interrupt 3 (LIRQ3) Enable
			0	Disable interrupt
			1	Enable interrupt
L2E	R/W	0		Local Interrupt 2 (LIRQ2) Enable
			0	Disable interrupt
			1	Enable interrupt
L1E	R/W	0		Local Interrupt 1 (LIRQ1) Enable
			0	Disable interrupt
			1	Enable interrupt
L0E	R/W	0		Local Interrupt 0 (LIRQ0) Enable
			0	Disable interrupt
			1	Enable interrupt

Table A-68. VMEbus Interrupt Enable Register

Register Name: VIE				Register Number: F000 00B0h				
Bits	Function							
07 - 00	0	V7E	V6E	V5E	V4E	V3E	V2E	V1E

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Table A-69. VIE Description

Name	Type	Condition after Reset	State	Function
V7E	R/W	0	 0 1	VMEbus Interrupt 7 Enable Interrupt disabled Interrupt enabled
V6E	R/W	0	 0 1	VMEbus Interrupt 6 Enable Interrupt disabled Interrupt enabled
V5E	R/W	0	 0 1	VMEbus Interrupt 5 Enable Interrupt disabled Interrupt enabled
V4E	R/W	0	 0 1	VMEbus Interrupt 4 Enable Interrupt disabled Interrupt enabled
V3E	R/W	0	 0 1	VMEbus Interrupt 3 Enable Interrupt disabled Interrupt enabled
V2E	R/W	0	 0 1	VMEbus Interrupt 2 Enable Interrupt disabled Interrupt enabled
V1E	R/W	0	 0 1	VMEbus Interrupt 1 Enable Interrupt disabled Interrupt enabled

Table A-70. Local Interrupts 1 and 0 Control Register

Register Name: IC10				Register Number: F000 00B4h				
Bits	Function							
07 - 00	1	1L2	1L1	1L0	1	0L2	0L1	0L0

Note: Has no function on the CVME965.

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Table A-71. Local Interrupts 3 and 2 Control Register

Register Name: IC32				Register Number: F000 00B8h				
Bits	**Function**							
07 - 00	**1**	**3L2**	**3L1**	**3L0**	**1**	**2L2**	**2L1**	**2L0**

Note: Should be set to 0000 008Fh for proper operation.

Table A-72. Local Interrupts 5 and 4 Control Register

Register Name: IC54				Register Number: F000 00B8h				
Bits	**Function**							
07 - 00	**5AV**	**5L2**	**5L1**	**5L0**	**4AV**	**4L2**	**4L1**	**4L0**

Note: Should be set to 0000 00F8h for proper operation

Table A-73. Miscellaneous Control Register

Register Name: MISC		Register Number: F000 00C0h		
Bits	**Function**			
31 - 24	**Reserved**			
23 - 16	**Reserved**			
15 - 08	**Reserved**	**EXTKIACK**	**ARBBYP**	**AUTOBAR**
07 - 00	**Reserved**		**ENDOG**	**SYSFAIL**

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Table A-74. MISC Description

Name	Type	Condition after Reset	State	Function
EXTKIACK	R	Config-urable	0 1	Internal KIACK Decode External KIACK Decode
ARBBYP	R	Config-urable	0 1	Local Arbiter active Local Arbiter bypassed
AUTOBAR	R	Config-urable	0 1	AUTOBAR disabled AUTOBAR enabled
ENDOG	R/W	0	0 1	Watchdog Timer disabled Watchdog Timer enabled
SYSFAIL	R/W	1	0 1	Release SYSFAIL* and SYSFLED Assert SYSFAIL* and SYSFLED

Table A-75. Delay Line Control Register

Register Name: DLCT	Register Number: F000 00C4h

Caution: Always write 0 to these bits. Writing values other than 0 to this area will cause unpredictable SCV64 operation.

Table A-76. Delay Line Status Register 1

Register Name: DLST1	Register Number: F000 00C8h

Note: Refer to Cyclone initialization code.

Table A-77. Delay Line Status Register 2

Register Name: DLST2	Register Number: F000 00CCh

Note: Refer to Cyclone initialization code.

Table A-78. Delay Line Status Register 3

Register Name: DLST3	Register Number: F000 00D0h

Note: Refer to Cyclone initialization code.

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Table A-79. Mailbox Register 0

Register Name: MBOX0	Register Number: F000 00D4h

Note: Not implemented.

Table A-80. Mailbox Register 1

Register Name: MBOX1	Register Number: F000 00D8h

Note: Not implemented.

Table A-81. Mailbox Register 2

Register Name: MBOX2	Register Number: F000 00DCh

Note: Not implemented.

Table A-82. Mailbox Register 3

Register Name: MBOX3	Register Number: F000 00E0h

Note: Not implemented.

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