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SECTION B
SQUALL INTERFACE

B.1 SQUALL MODULE INTERFACE

This Appendix provides design information, electrical and physical specifications of the Squall Module interface allowing users to design and integrate their own Squall II Modules. If you are using a standard Squall Module, please refer to the specific module's manual for information on the operation of that module.

911 Series adapters contain two locations for Squall Modules. The first of these locations will accept Squall II Modules; the other will accommodate Squall IIE or IIET Modules which have different mechanical specifications. Squall Modules allow different I/O interfaces to be added to the base single board computer. The modules take advantage of the i960 processor's capabilities as an embedded processor and I/O server. Devices on the module may be accessed by the processor in slave mode. Squall Modules which include DMA controllers may access the DRAM on the PCI adapter in master mode. I/O signals and connectors may be located on the slot plate.

Each Squall Module contains a serial EEPROM which allows the processor to determine the type, revision, and programming information of the specific module. The EEPROM is read via the Squall Serial EEPROM Register on all 911 Series adapters. Section B.3 outlines the use of the EEPROM.

Cyclone Microsystems is continuously designing new Squall Modules. Currently available Squall Modules are listed in section 3.10 of this manual. Mechanical specifications for Squall II, IIE and IIET Modules are included in Appendix A.

B.2 POWER REQUIREMENTS

The Squall Module connectors supply +5v, +12v and -12v. Designers should be careful not to exceed the Amperes listed in Table B-1. If power is lead off the module via an external connector, a fuse should be used to prevent damaging the 911 Series adapter due to an incorrect connection.

Table B-1. Power Supply

Volts	Squall Connector Pins	Maximum Amps
+5V	5 pins	2.5 Amps Maximum
+12V	1 pin	0.5 Amps Maximum
-12V	1 pin	0.5 Amps Maximum
GND	10 pins	---

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B.3 SQUALL MODULE SERIAL EEPROM

Every Squall Module has a 24C08 serial EEPROM which is used by the host processor to identify the type and revision of the installed module, and to store any system parameters which might be module dependent.

The EEPROMs are read and written serially using the Squall Serial EEPROM Register on the 911 Series adapter. Users may refer to a data sheet of the 24C08, listed in section 1.6, Reference Manuals, for information on how to use the device. Cyclone has already written routines to access these devices. Initialization code on all 911 Series adapters reads the serial EEPROMs to properly configure the board. The on-board diagnostics (accessible from the MON960 prompt with "po" command) can be used to initialize Squall EEPROMs.

The first 10 bytes of the EEPROM have been specified by Cyclone and have the same function for all Squall Modules. The rest of the memory is assignable by the module's designer and users should refer to the particular module's User's Manual.

The first 4 bytes, (addresses 0-3), contain the module's region configuration word, stored in little endian byte ordering (bits 7-0 in address 0).

The next byte, (address 4), contains two bits indicating the interrupt detection mode of the Squall Module's interrupts. Interrupts are software configurable in the i960 processor's ICON (Interrupt Control Register) to be level low activated or falling edge activated. Bit 0 corresponds to SQIRQ0*, which will be XINT3* or XINT5* depending on which location the module is installed in. Bit 1 corresponds to SQIRQ1*, XINT2*, or XINT4*. A zero (0) indicates the interrupt is level low activated. A one (1) indicates the interrupt is falling edge activated.

Bytes 5 and 6 are reserved. Bytes 7 and 8 contain the Squall Module version number in ASCII. Users designing their own modules should use designators $90 - $9F. Address 9 contains the module's revision level in binary. This field is assigned and incremented by the designer of the module. Bytes $00A-$7FF are specific to the module. Please refer to the particular module's User's Manual.

Like the onboard EEPROM, bytes are read from, and written to, the 24C08 EEPROM most significant bit (bit 7) first and least significant bit (bit 0) last.

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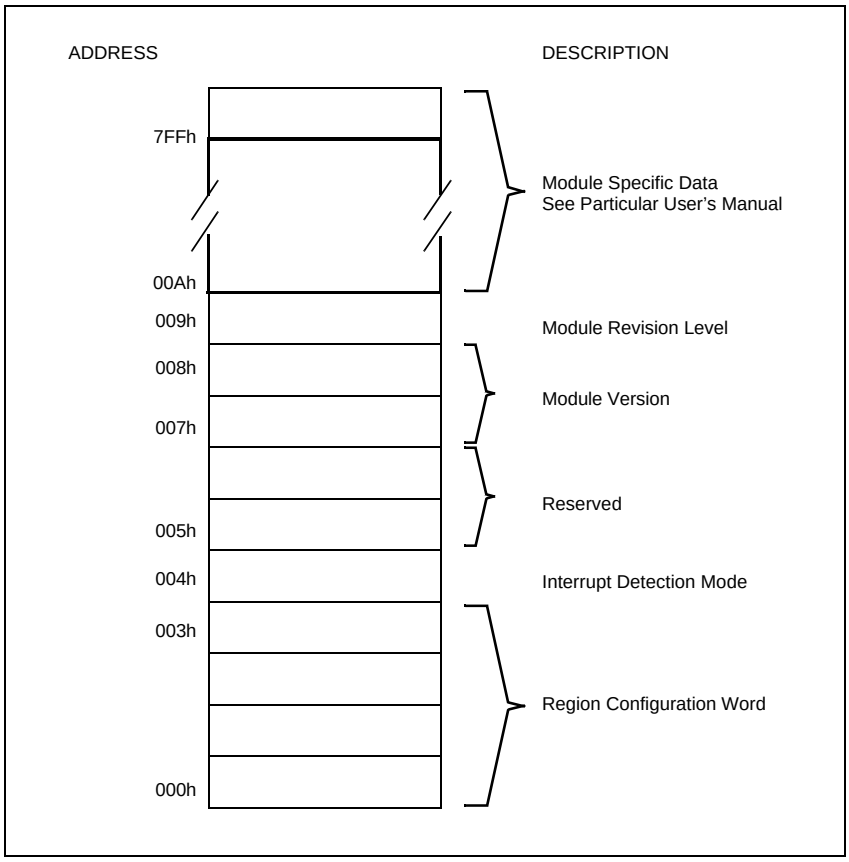


Figure B-1. Squall Module EEPROM Memory Map

B.4 SQUALL MODULE SIGNAL DEFINITIONS

Squall Module devices can be accessed by the processor and may access the DRAM on the adapter via a 100 pin connector. This section describes the signals provided on the Squall Module interface connector. The signals are an enhanced set of the i960 external bus signals. Familiarity with the operation of the i960 external bus will help the user in understanding the Squall Module Interface. Refer to the i960 Processor User's Manual for detailed explanations.The signals are described relative to the circuitry on the Squall Module (an input to the CPU or memory would be an output from the Squall Module). Master and slave designations are used to describe different operating modes of the Squall Interface. The Squall Module is a slave when it is being accessed by the processor (SQBG* inactive). The Squall Module is a master when its circuitry has been granted mastership of the shared memory bus (SQBG* asserted by arbitration circuitry in response to a SQBR*). All output and I/O pins have been provided with the proper pull up resistors on the host board and may be left unconnected if desired. Table B-2 presents the legend for interpreting the pin descriptions.

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Table B-2. Pin Description Nomenclature

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin may be either an input or an output
-	Pin must be connected as described
S	Synchronous. Inputs are synchronous to PCLK. Outputs must meet setup and hold times relative to PCLK.
A( )	Asynchronous. Outputs may be asynchronous to PCLK. A(E) Edge sensitive output A(L) Level sensitive output
SL( )	While SQBR* and SQBG* are inactive, the pin functions in the slave mode. SL(O) Output SL(I) Input SL(I/O) As an input or an output
M( )	When SQBR* and SQBG* are asserted, the module is in master mode. M(I) Input M(O) Output M(I/O) As an input or output

Table B-3. Squall Module Signal Descriptions

Name	Type	Description
S_A[02:31]	SL (I) M(O) S	Address Bus carries the upper 30 bits of address. The byte enable signals indicate the selected byte in each word.
S_D[00:31]	I/O S	Data Bus carries 32, 16 or 8 bit data depending on the bus width S configured in the Memory Region Table. For a bus width of 8 bits, data lines D[00:07] are used. For 16 bits, D[00:15] are used. For 32 bits, the full bus is used. In master mode, all transfers with the memory use full data bus.

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Name	Type	Description
S_BE3* S_BE2* S_BE1* S_BE0*	SL(I) M(O) S	Byte Enables select which of the four bytes addressed by A[02:31] are active during an access to a memory region configured as 32 bits data bus width. The following describes the usage of the Byte Enable Signals in different data bus configurations. 32 bit bus: BE3* - Byte Enable 3 - Enable D[24:31] BE2* - Byte Enable 2 - Enable D[16:23] BE1* - Byte Enable 1 - Enable D[08:15] BE0* - Byte Enable 0 - Enable D[00:07] 16 bit bus: BE3* - Byte High Enable - Enable D[08:15] BE2* - Not Used BE1* - Address bit 1 - A[01] BE0* - Byte Low Enable - Enable D[00:07] 8 bit bus: BE3* - Not used BE2* - Not used BE1* - Address Bit 1 - A[01] BE0* - Address Bit 0 - A[00]
S_W/R	SL (I) M (O) S	Write/Read is low for read accesses and high for write accesses. The operation, read or write, is relative to the bus master.
S_ADS*	SL (I) M (O) S	Address Strobe indicates valid address and the start of a new bus access. S)ADS* is asserted for the first clock of an access.
S_READY*	SL (O) M (I) S	Ready signals the termination of a data transfer. S_READY* is used to indicate that read data on the bus is valid or that a write data transfer has been completed. In slave mode, the S_READY* signal should be asserted to terminate a cycle indicated by SQSEL*. S_READY* should be tristated until a cycle is indicated by SQSEL*. S_READY* can be enabled at SQSEL* or at the clock cycle prior to the assertion of S_READY*. S_READY* should remain enabled until one clock after the deassertion of S_READY*. In master mode, the memory control circuit asserts S_READY* to indicate that valid read data is on the data bus or that a write transfer is complete.

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Name	Type	Description
SQSEL*	I S	Select Squall is a select signal for a processor's 256 Mbyte memory region. The memory region is determined by which module location the Squall Module is installed on. Squall Module 0, the base address is $A000,0000. Squall Module 1, the base address is $C000,0000. The designer must return S_READY* to the processor when this signal is active. SQSEL* is asserted on the rising edge of PCLK if S_ADS* is asserted and A[28:31] = $A or $C is negated on the rising edge of PCLK with S_BLAST* and S_READY* asserted.
S_BLAST*	SL (I) M (O) S	Burst Last indicates the last transfer in a bus access. In slave mode, S_BLAST* is asserted in the data transfer of burst and nonburst accesses after the processor's wait state counter reaches zero. S_BLAST* remains active until the clock following the last cycle of the last data transfer of a bus access. If S_READY* signal is used to extend wait states, the S_BLAST* signal remains active until S_READY* terminates the access. In master mode, this signal should be used to indicate to the shared memory the last cycle of a burst access.
S_EXTEND*	M (O) S	Extend may be used by slow Squall Module masters to extend a shared memory read cycle. Extend has no meaning for slaves and will always be inactive during slave cycles.
RESET*	I A	Reset asserted should cause all the devices and circuitry on the Squall Module to return to a known state. RESET* will be asserted for a minimum of 200ms. RESET* will always be asserted following power-up.
S_LOCK*	SL (I) M (O) S	Bus Lock indicates that an atomic ready-modify-write operation is in progress.
SQBR*	O	Shared Bus Request signals that the Squall Module circuitry requested access to the shared memory. The local bus arbiter will assert SQBG* to grant the Squall Module bus mastership.
SQBG*	I S	Shared Bus Grant indicates to a bus requestor that the other shared bus masters have relinquished control of the bus. The Squall Module circuitry may not use the shared bus to access the on board shared memory, until SQBG* is asserted.
PCLK	I	Processor Output Clock provides a timing reference for all input and output to the processor and the memory.

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Name	Type	Description
SQIRQ0*	O	Interrupt Request 0 is directly connected to the processor's external interrupt pin XINT2* or XINT4* depending on which module location the module is installed. This pin may be programmed within the processor as a level (low) or edge (falling) activated interrupt source. The interrupt priority of this pin may also be programmed within the processor.
SQIRQ1*	O	Interrupt Request 1 is the same as SQIRQ0* except that it is connected to the processor's external interrupt pin XINT3* or XINT5* depending on which location the module is installed.
SQSDA	I/O	Serial EEPROM Data
SQSCL	I	Serial EEPROM Clock

B.5 SQUALL MODULE TIMING

The Squall Interface signals are an enhanced set of the i960 bus signals. The interface has two modes of operation, slave and master. In slave mode the processor is accessing devices on the Squall Module. In master mode a Squall Module based DMA controller is accessing the adapter DRAM.

B.5.1 Squall Module Slave Timing

This section outlines the signal timing of the shared memory bus when the i960 processor is reading and writing to the Squall Module. There are two mandatory conditions. Because the shared memory bus is arbitrated between several masters, and does not use the i960's Hold/Holda signals to perform the arbitration, the Squall Module memory region must be programmed with ready enabled. The Squall Module circuitry must also return ready for all assertions of SQSEL*.

The timing diagrams in Figures B-2 and B-3 show the timing relationship between the various signals. Figure B-2 shows multiple wait states for non-burst read and write cycles. Figure B-3 shows a 2,0,0,0 wait state burst read and a 2,1,1,1 wait state burst write. The number of wait states actually used is totally dependent on the designer of a new Squall Module.

Table B-4. Squall Module Slave Timing

Name	Minimum	Maximum	Comment
t1	2	18	Clock to Output ADS*
t2	2	10	Clock to Output, S ADS* and SQxSEL*
t4	10		Read S DATA Setup to Clock
t5	2		S DATA hold from Clock
t6	5	20	Clock to Output, S BLAST*, BE<3:0>*

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Name	Minimum	Maximum	Comment
t7	4	18	Clock to Output, S ADDR <31:02>
t8	3	22	Clock to Output, S W/R
t9	12		S READY* Setup to Clock
t10	0		S READY* Hold from Clock
t11	5	20	Clock to Output, S DATA (Write)

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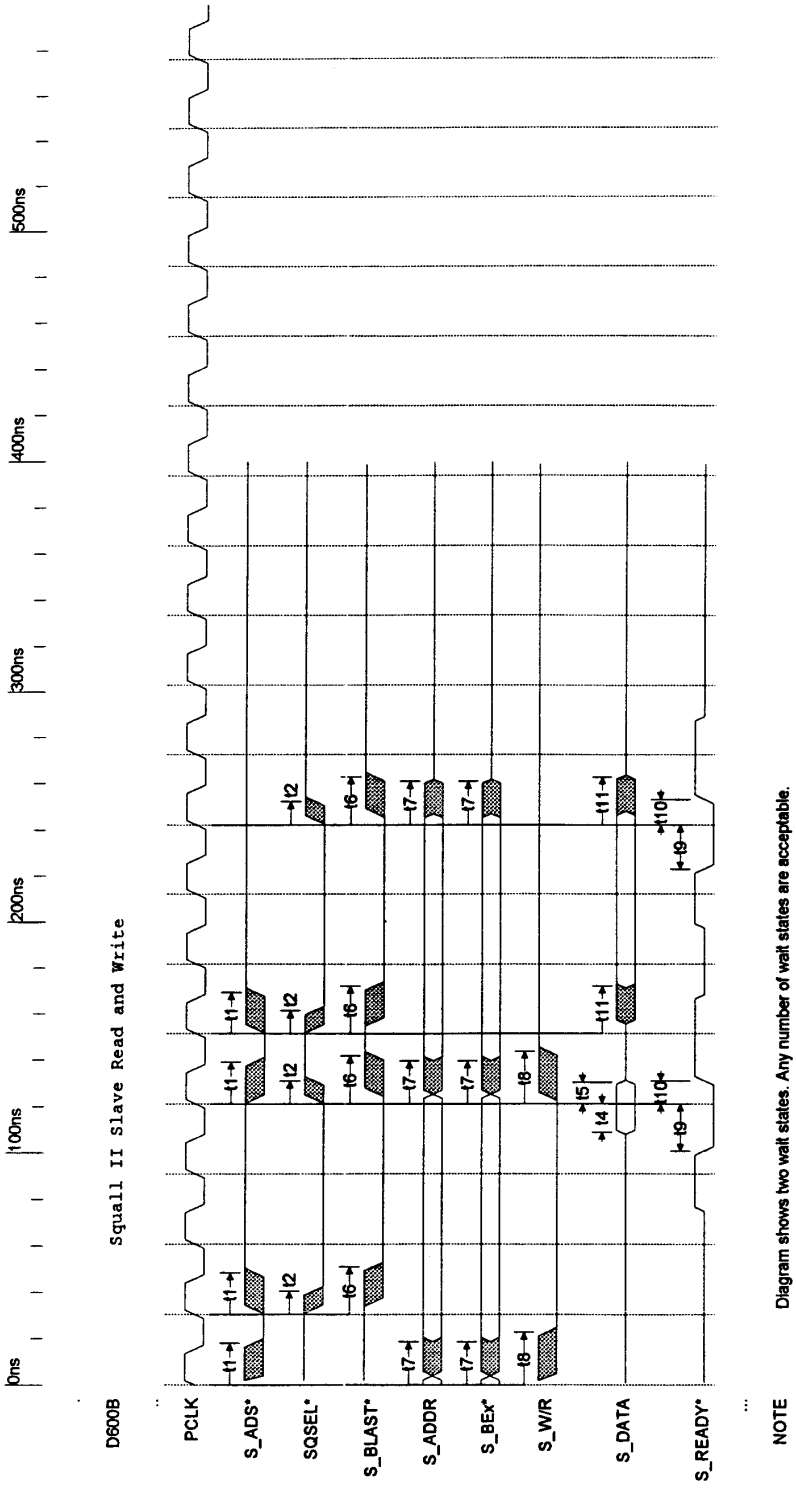


Figure B-2. Squall Slave Read and Write Timing Diagram

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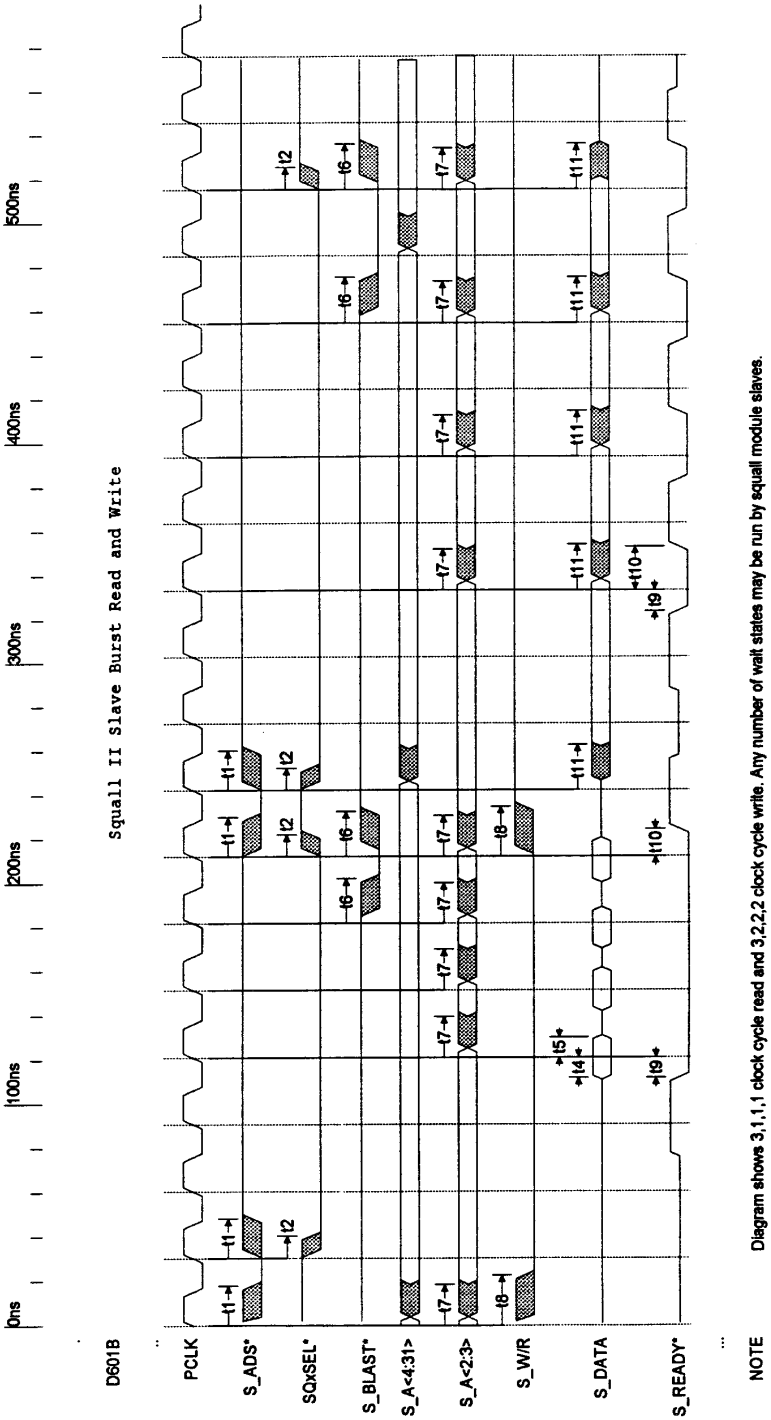


Figure B-3. Squall Slave Burst Read and Write Timing Diagram

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B.5.2 Squall Module Master Timing

Squall Module circuits may become masters of the shared bus to perform DMA operations to the shared DRAM. DMA controllers gain control of the bus via the SQBR* and SQBG* signals.

All signals, except the interrupt signals, are synchronous to the processor's clock (PLCK). Set up and hold times must be observed for every rising clock edge. Because of the high clock rates, all signals must be driven high before they are tristated. This will ensure that valid levels are observed on every rising clock edge.

DMA controllers gain control of the bus via the SQBR* and SQBG* signals. Memory cycles may then proceed with the same ADS*, BLAST*, and READY* protocol used by the i960CF processor.

Squall Modules are permitted to burst up to 16 longwords (64 bytes) of data when performing master cycles to or from host memory on 911 Series adapters.

Table B-5. Squall Module Master Timing

Name	Minimum	Maximum	Comment
t1	3	10	Clock to output SQBG*
t2	10		Setup to clock rising edge for SQBR*, S_ADS*, S_BLAST, S_A[31:02], S_W/R, S_BE[3:0]*
t3	0	20	Clock to output D[31:00], Read Cycle
t4	5		D[31:00] hold from clock, read cycle
t5	3	10	Clock to output READY*
t7	10		Write data setup to clock
t8	0		Write data hold from clock
t9	0	30	SQBG* Inactive to control signals tristated
t10	0		Hold from clock rising edge for SQBR*, S_ADS*, S_BLAST, S_A[31:02], S_W/R, S_BE[3:0]*
t11	0		SQBR* asserted to control outputs driven

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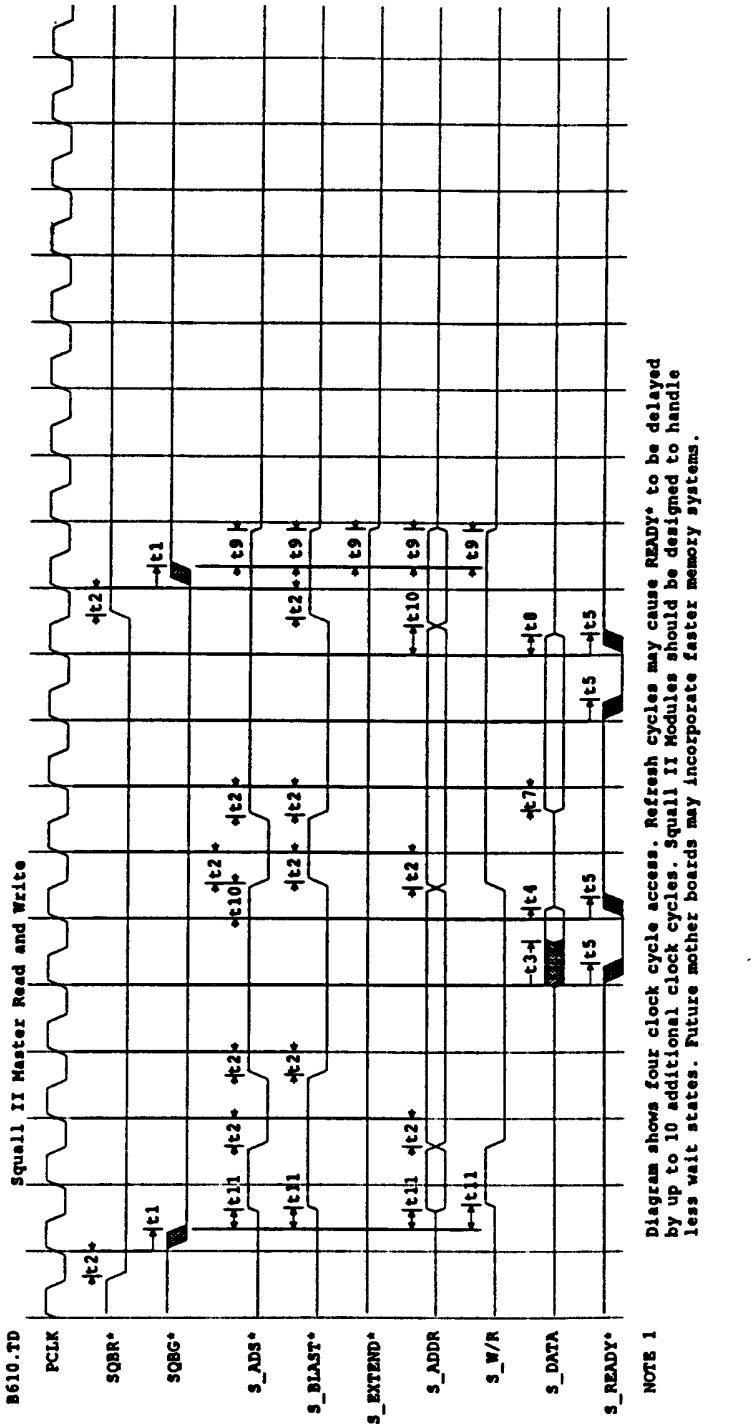


Figure B-4. Squall Master Read and Write Timing Diagram

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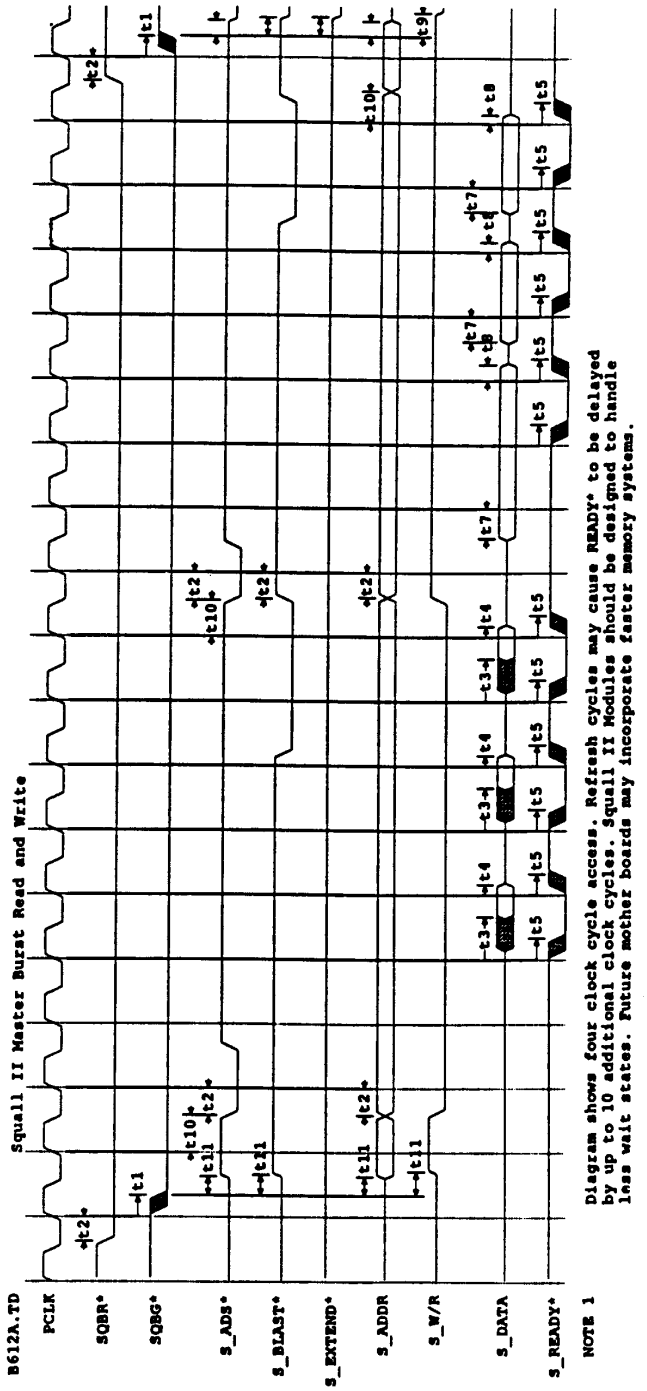


Figure B-5. Squall Master Burst Read and Write Timing Diagram

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B.6 SQUALL MODULE CONNECTOR

Different physical connectors are used for Squall and IIE/IIET Modules. This pinout for both connectors, however, is the same. Table B-6 gives the pin assignments for the Squall Module connector.

Table B-6. Squall Module Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	S_ADS	21	S_EXTEND*	41	GND	61	S_A22	81	S_A03
2	GND	22	GND	42	S_D15	62	S_A21	82	S_A02
3	PCLK	23	+5V	43	S_D14	63	S_A20	83	+5V
4	GND	24	S_D31	44	S_D13	64	S_A19	84	S_D07
5	S_BLAST*	25	S_D30	45	S_D12	65	S_A18	85	S_D06
6	S_LOCK*	26	S_D29	46	S_D11	66	S_A17	86	S_D05
7	S_W/R	27	S_D28	47	S_D10	67	S_A16	87	S_D04
8	GND	28	S_D27	48	S_D09	68	+5V	88	S_D03
9	S_READY*	29	S_D26	49	S_D08	69	S_A15	89	S_D02
10	RESET*	30	S_D25	50	GND	70	S_A14	90	S_D01
11	S_BE0*	31	S_D24	51	S_A31	71	S_A13	91	S_D00
12	S_BE1*	32	GND	52	S_A30	72	S_A12	92	GND
13	S_BE2*	33	S_D23	53	S_A29	73	S_A11	93	+5V
14	S_BE3*	34	S_D22	54	S_A28	74	S_A10	94	--
15	SQSEL*	35	S_D21	55	S_A27	75	S_A09	95	--
16	GND	36	S_D20	56	S_A26	76	S_A08	96	GND
17	SQIRQ1*	37	S_D19	57	S_A25	77	S_A07	97	SQSDA
18	SQIRQ0*	38	S_D18	58	S_A24	78	S_A06	98	SQSCL
19	SQBR*	39	S_D17	59	+5V	79	S_A05	99	+12V
20	SQBG*	40	S_D16	60	S_A23	80	S_A04	10 0	-12V

B.7 SQUALL MODULE SIGNAL LOADING AND LOGIC SELECTION

Selection of logic families for Squall Modules deals mostly with the edge rate of the outputs. CMOS logic families, although they use less power than their bipolar predecessors, can be very noisy due to very fast edges transitioning full 5 volt swings from rail to rail. The high speed 5 volt transitions can result in large under and over shoots, ringing, and ground bounce. Logic families such as ACT, FCT, and ACL all exhibit such tendencies.

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We recommend using newer Bicmos Logic families such as BCT or ABT. These families, like older TTL logic, switch between 3.5 volts and ground, and contain edge control circuitry.

The same consideration is true for programmable logic. Some manufacturers boast of higher speed parts, but achieve that objective by increasing the signal edge transitions. Designers should evaluate the transitions before deciding to use a part in a Squall Module design.

The loading of the Squall Module interface signals is very important. The majority of the signals are bussed between the two Squall Module connectors, the shared memory, the processor interface, and the VMEbus interface. These signals should be restricted to two loads on each Squall Module. Some signals are routed to an individual Squall Module and, therefore, may be more heavily loaded. Refer to Table B-7 for specific loading restrictions.

Table B-7. Squall Module Signal Loading

Signal	Loads
S_A, S_D, S_BE*, S_W/R, S_ADS*, S_READY*, S_BLAST*, S_EXTEND*, S_LOCK*	2
SQSEL*	6
RESET*	10
SQBG*	6
PCLK	5

B.8 SQUALL MODULE CLOCK TERMINATION

Individual clock signals are driven to each Squall Module. The clock signals should be terminated with an AC termination of 470pF and 51 ohms to ground as shown in Figure B-6. Care should be taken to locate the loads close to the end of the signal, especially in double sized modules.

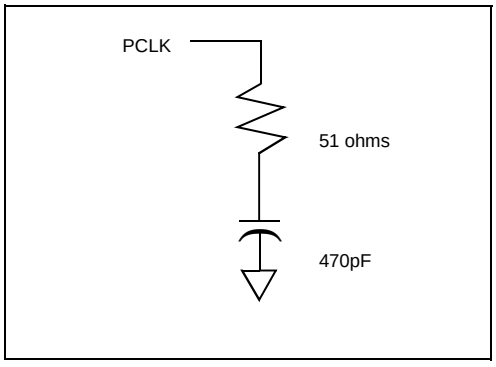


Figure B-6. Squall Module Clock Termination

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