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CYPRESS SEMICONDUCTOR

PALC22V10

Reprogrammable CMOS PAL® Device

Features

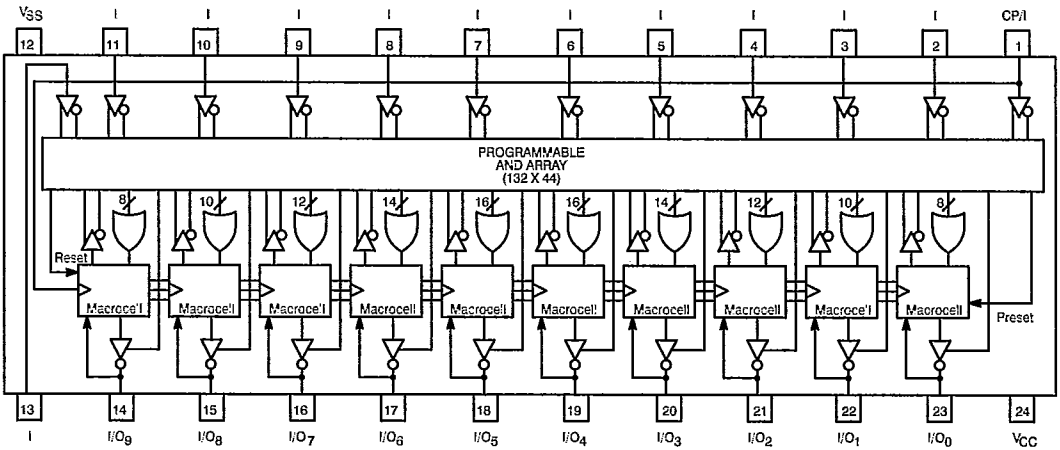
- Advanced second-generation PAL architecture
- Low power
  - 55 mA max. "L"
  - 90 mA max. standard
  - 120 mA max. military
- CMOS EPROM technology for reprogrammability
- Variable product terms
  - 2 x (8 through 16) product terms
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
- 20, 25, 35 ns commercial and industrial
- 25, 30, 40 ns military
- Up to 22 input terms and 10 outputs
- High reliability
  - Proven EPROM technology
  - 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, and PLCC available

Functional Description

The Cypress PALC22V10 is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "programmable macrocell."

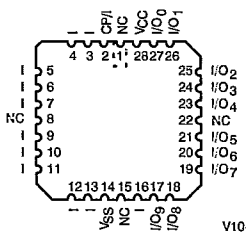
The PALC22V10 is available in 24-pin 300-mil molded DIPs, 300-mil windowed cerDIPs, 28-lead square ceramic leadless chip carriers, 28-lead square plastic leaded chip carriers, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10 is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as registered or combinatorial. Polarity of each output may also be individually selected, allowing complete flexibility of output configuration. Further configurability is provided through array-configurable output enable for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis, or alternately used as a combination I/O controlled by the programmable array.

Logic Block Diagram (PDIP/CDIP)



Pin Configuration

LCC/PLCC Top View



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Functional Description (continued)

PALC22V10 features a variable product term architecture. There are five pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure, the PALC22V10 is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unusable product terms and lower performance.

Additional features of the Cypress PALC22V10 include a synchronous preset and an asynchronous reset product term. These product terms are common to all macrocells, eliminating the need to dedicate standard product terms for initialization function. The device automatically resets on power-up.

For testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high-impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A 0 on the I/O pin preloads the register with a 0, and a 1 preloads the register with a 1. The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed and pin 8 is returned to a normal TTL voltage. Again, care should be exercised to power sequence the device properly.

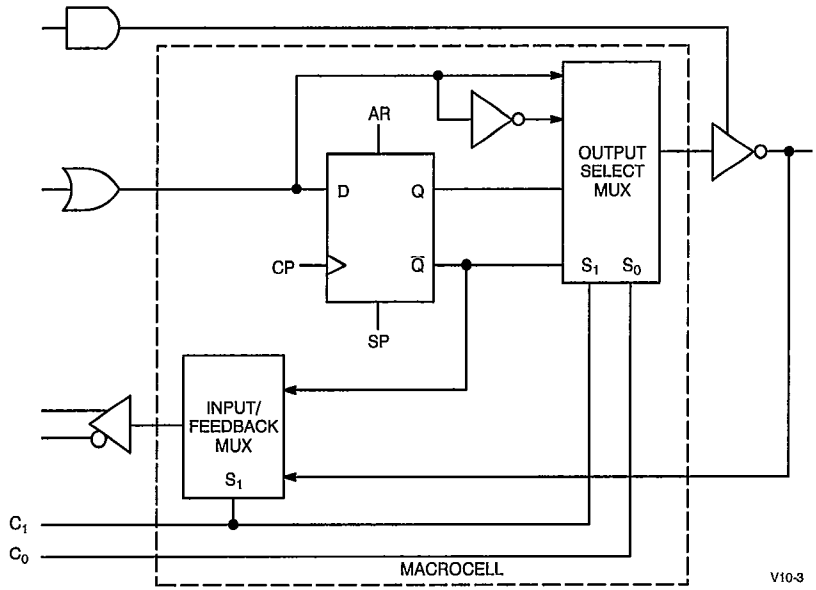
The PALC22V10 featuring programmable macrocells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output and down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled using product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macrocell. These macrocells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array, providing current status information to the array. This information is available for establishing the next result in applications such as control state machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macrocell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of a programmable logic.

Along with this increase in functional density, the Cypress PALC22V10 provides lower-power operation through the use of CMOS technology and increased testability with a register preload feature. Preload facilitates testing programmed devices by loading initial values into the registers.

Configuration Table

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

Macrocell



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Selection Guide

Generic Part Number	I_{CC1} (mA)			t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
	"L"	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
22V10–20		90		20		12		12	
22V10–25	55	90	100	25	25	15	18	15	15
22V10–30			100		30		20		20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V

DC Input Voltage ..... – 3.0V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

UV Exposure ..... 7258 Wsec/cm^2

DC Programming Voltage 14.0V

Latch-Up Current ..... >200 mA

Static Discharge Voltage ..... >500V (per MIL–STD–883, Method 8015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Industrial	– 40°C to +85°C	5V ±10%
Military[1]	– 55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 3.2 mA	Com'l/Ind	2.4		V
			I_{OH} = – 2 mA	Mil			
V_{OH2}	HIGH Level CMOS Output Voltage[3]	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = – 100 µA		V_{CC}–1.0V		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l/Ind		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[4]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[4]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			– 10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			– 40	+40	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3, 5]			– 30	– 90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open for Unprogrammed Device		"L"		55	mA
				Com'l/Ind		90	mA
				Mil		100	mA
I_{CC2}	Operating Power Supply Current	f_{toggle} = F_{MAX}[3]		"L"		65	mA

Capacitance[3]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		10	pF

Notes:

1. t_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.
4. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
5. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

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Commercial and Industrial Switching Characteristics PALC22V10[2, 6]

Parameter	Description	−20		−25		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		20		25	ns
t_{EA}	Input to Output Enable Delay		20		25	ns
t_{ER}	Input to Output Disable Delay[8]		20		25	ns
t_{CO}	Clock to Output Delay[9]		12		15	ns
t_S	Input or Feedback Set-Up Time	12		15		ns
t_H	Input Hold Time	0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	24		30		ns
t_{WH}	Clock Width HIGH[3]	10		12		ns
t_{WL}	Clock Width LOW[3]	10		12		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	41.6		33.3		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 11]	50.0		41.6		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	45.4		35.7		MHz
t_{CF}	Register Clock to Feedback Input[13]		10		13	ns
t_{AW}	Asynchronous Reset Width	20		25		ns
t_{AR}	Asynchronous Reset Recovery Time	20		25		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		25		25	ns
t_{SPR}	Synchronous Preset Recovery Time	20		25		ns
t_{PR}	Power-Up Reset Time[14]	1.0		1.0		µs

Notes:

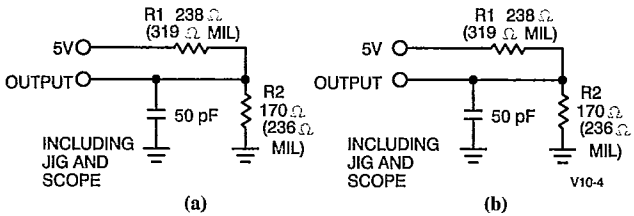
6. Part (a) of AC Test Loads and Waveforms used for all parameters except t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}. Part (b) of AC Test Loads and Waveforms used for t_{EA}, t_{ER}, t_{PZX}, and t_{PXZ}.
7. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction which may be subtracted from t_{PD} for cases in which fewer outputs are changing state per access cycle.
8. This parameter is specified as the time after output disable input during which the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5V below V_{OH} min. or a previous LOW level has risen to 0.5V above V_{OL} max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
9. This specification is guaranteed for all device outputs changing state in a given access cycle. See part (d) of AC Test Loads and Waveforms for the minimum guaranteed negative correction that may be subtracted from t_{CO} for cases in which fewer outputs are changing state per access cycle.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see Note 12 above) minus t_S.
14. The registers in the PALC22V10 have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

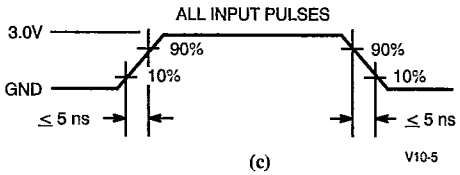
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Military Switching Characteristics PALC22V10[2, 6]

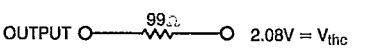
Parameter	Description	−25		−30		Unit
		Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		25		30	ns
t_{EA}	Input to Output Enable Delay		25		25	ns
t_{ER}	Input to Output Disable Delay[8]		25		25	ns
t_{CO}	Clock to Output Delay[9]		15		20	ns
t_S	Input or Feedback Set-Up Time	18		20		ns
t_{IH}	Input Hold Time	0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	33		40		ns
t_{WH}	Clock Width HIGH[3]	14		16		ns
t_{WL}	Clock Width LOW[3]	14		16		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	30.3		25.0		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 11]	35.7		31.2		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	32.2		28.5		MHz
t_{CF}	Register Clock to Feedback Input[13]		13		15	ns
t_{AW}	Asynchronous Reset Width	25		30		ns
t_{AR}	Asynchronous Reset Recovery Time	25		30		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		25		30	ns
t_{SPR}	Synchronous Preset Recovery Time	25		30		ns
t_{PR}	Power-Up Reset Time[14]	1.0		1.0		μs

AC Test Loads and Waveforms



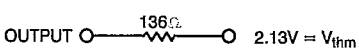


Equivalent to: THEVENIN EQUIVALENT (Commercial)



V10-6

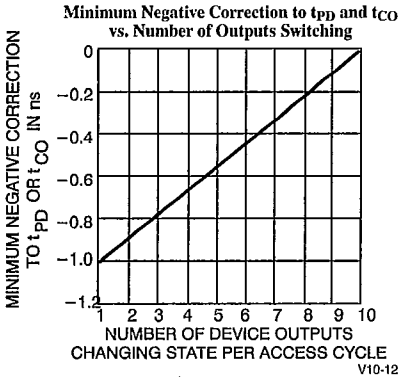
Equivalent to: THEVENIN EQUIVALENT (Military)



V10-7

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AC Test Loads and Waveforms (continued)

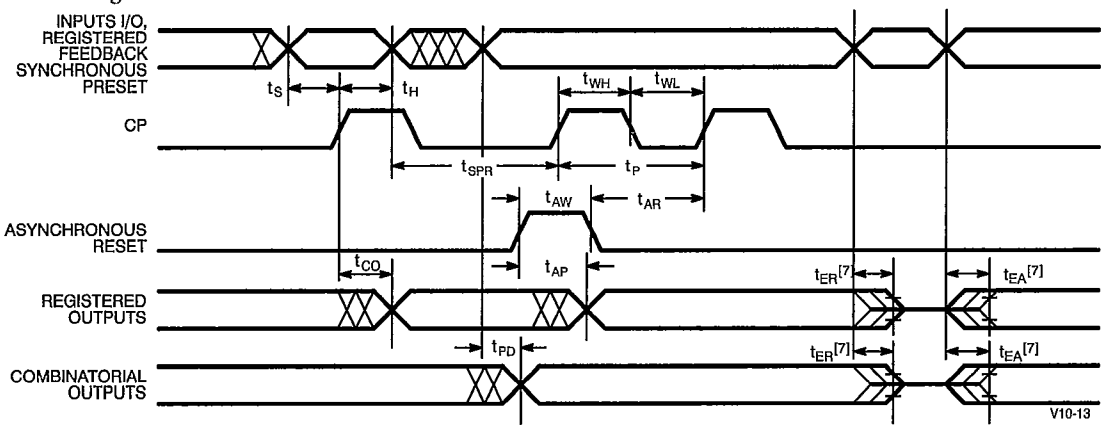


(d)

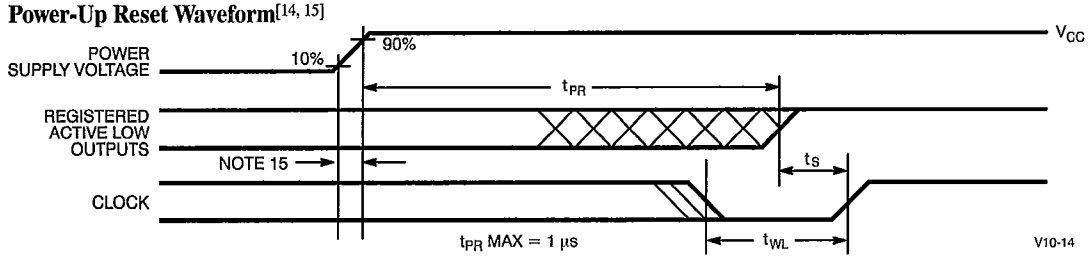
Parameter	V_X	Output Waveform—Measurement Level
t_{ER} (−)	1.5V	V_{OH}, 0.5V, V_X — V10-8
t_{ER} (+)	2.6V	V_{OL}, 0.5V, V_X — V10-9
t_{EA} (+)	V_{thc}	V_X, 0.5V, V_{OH} — V10-10
t_{EA} (−)	V_{thc}	V_X, 0.5V, V_{OL} — V10-11

(e) Test Waveforms

Switching Waveform



Power-Up Reset Waveform[14, 15]

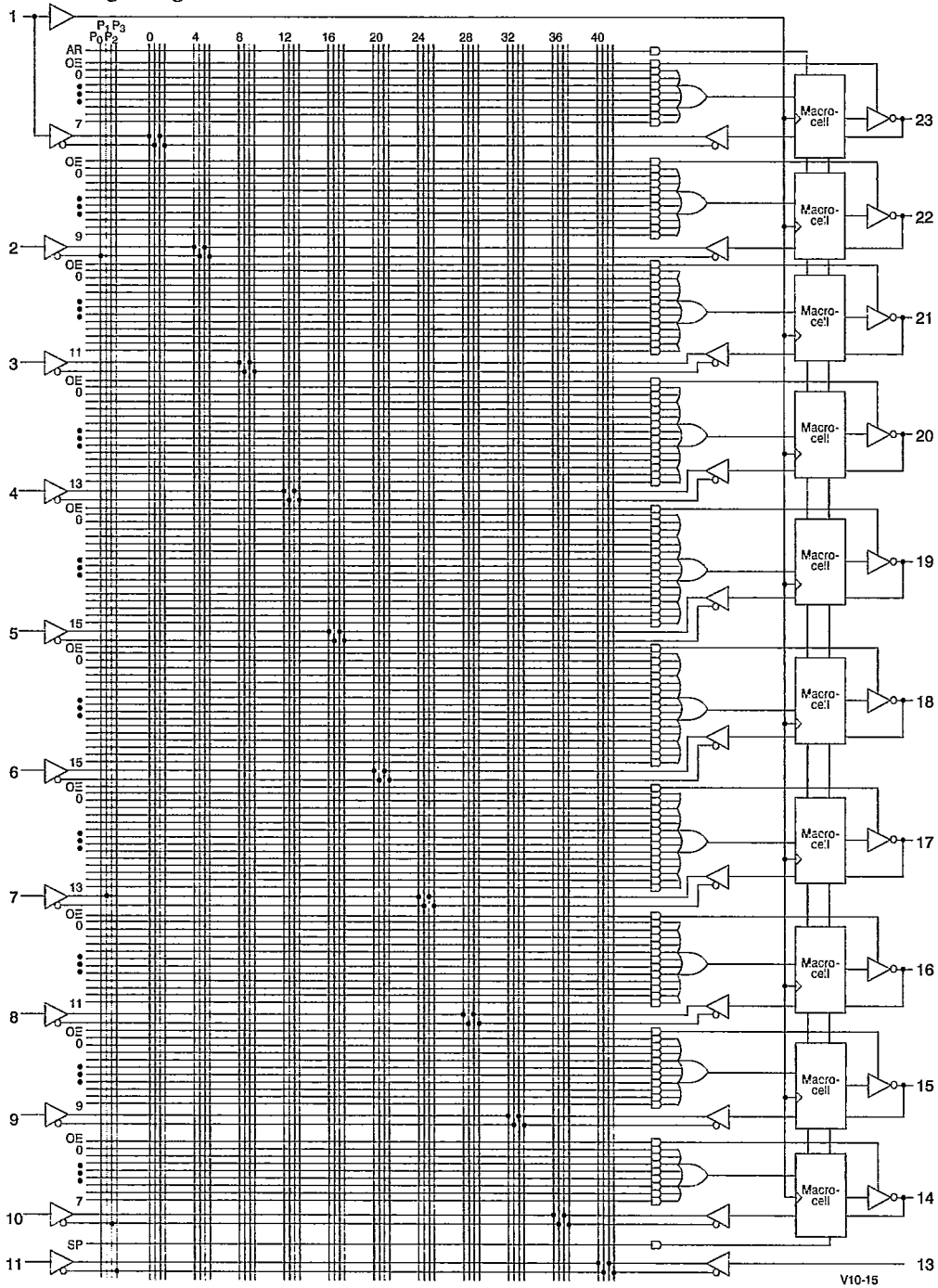


Note:

15. The clock signal input must be in a valid LOW state (V_{IN} less than 0.8V) or a valid HIGH state (V_{IN} greater than 2.4V) prior to occurrence of the 10% level on the monotonically rising power supply voltage as shown in Power-Up Reset Waveform. In addition, the clock input signal must remain stable in that valid state as indicated until the 90% level on the power supply voltage has been reached. The clock signal may transition LOW to HIGH to clock in new data or to execute a synchronous preset after the indicated delay ($t_{PR} + t_S$) has been observed.

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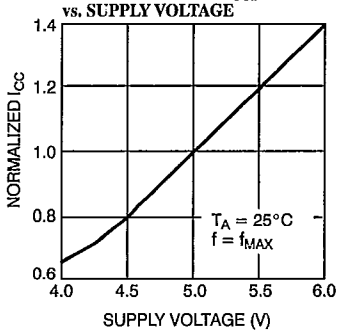
Functional Logic Diagram for PALC22V10



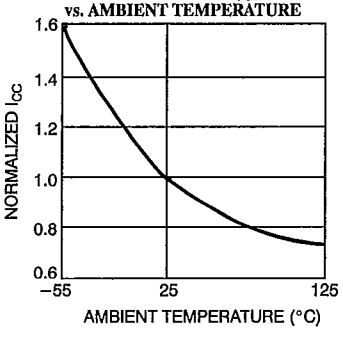
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Typical DC and AC Characteristics

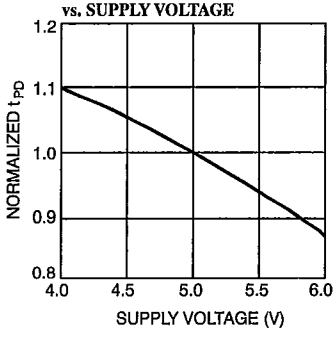
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. SUPPLY VOLTAGE



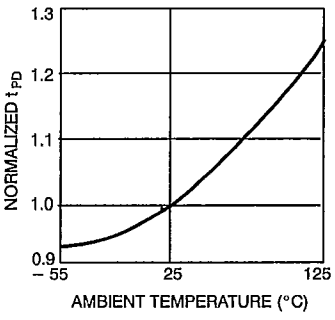
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. AMBIENT TEMPERATURE



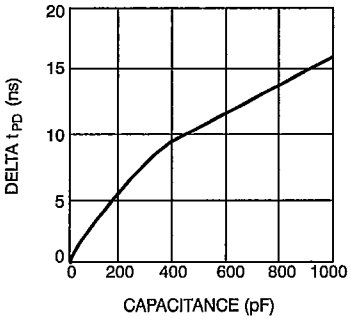
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



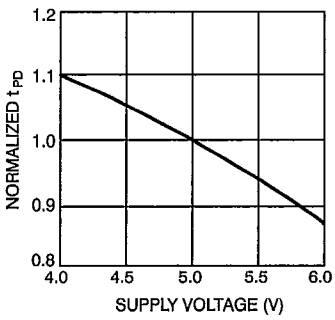
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



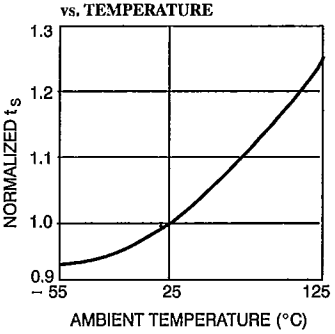
DELTA PROPAGATION TIME vs. OUTPUT LOADING



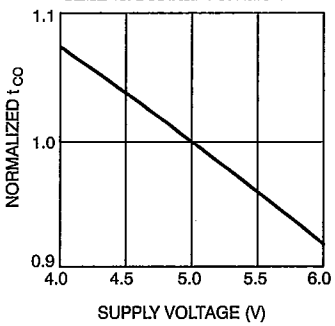
NORMALIZED SET-UP TIME vs. SUPPLY VOLTAGE



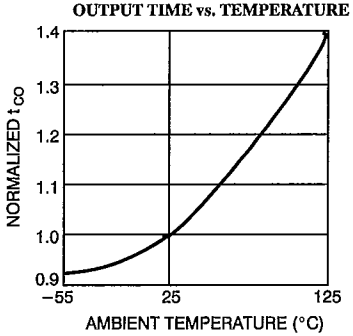
NORMALIZED SET-UP TIME vs. TEMPERATURE



NORMALIZED CLOCK-TO-OUTPUT TIME vs. SUPPLY VOLTAGE



NORMALIZED CLOCK-TO-OUTPUT TIME vs. TEMPERATURE

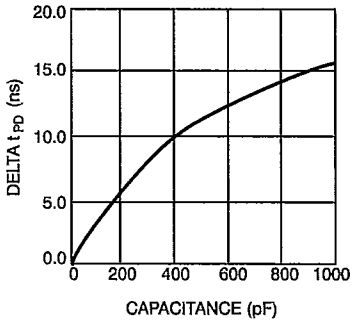


V10-16

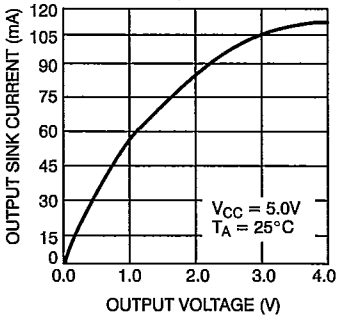
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Typical DC and AC Characteristics (continued)

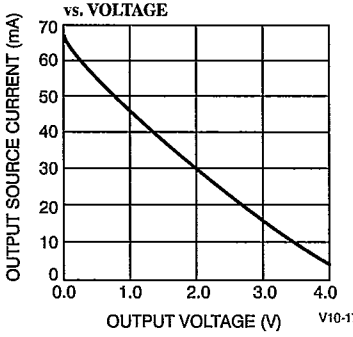
DELTA CLOCK-TO-OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



Erasure Characteristics

Wavelengths of light less than 4000Å begin to erase the PALC22V10. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high-ambient light levels can create hole-electron pairs that may cause blank check failures or verify errors when programming windowed parts. This phenomenon can be avoided by placing an opaque label over the window during programming in high-ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537Å for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PALC22V10 needs to be placed within one inch of the lamp during erasure. Permanent damage may result if the device is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Ordering Information 22V10

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
90	20	12	12	PALC22V10–20HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
				PALC22V10–20JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10–20PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PALC22V10–20WC/WI	W14	24-Lead (300-Mil) Windowed CerDIP	
55	25	15	15	PALC22V10L–25HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial
				PALC22V10L–25JC	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10L–25PC	P13	24-Lead (300-Mil) Molded DIP	
				PALC22V10L–25WC	W14	24-Lead (300-Mil) Windowed CerDIP	
90	25	15	15	PALC22V10–25HC	H64	28-Pin Windowed Leaded Chip Carrier	Commercial/ Industrial
				PALC22V10–25JC/JI	J64	28-Lead Plastic Leaded Chip Carrier	
				PALC22V10–25PC/PI	P13	24-Lead (300-Mil) Molded DIP	
				PALC22V10–25WC/WI	W14	24-Lead (300-Mil) Windowed CerDIP	
100	25	18	15	PALC22V10–25DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10–25KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10–25LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10–25QMB	Q64	24-Pin Windowed Leadless Chip Carrier	
				PALC22V10–25WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

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Ordering Information 22V10 (continued)

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Name	Package Type	Operating Range
100	30	20	20	PALC22V10–30DMB	D14	24-Lead (300-Mil) CerDIP	Military
				PALC22V10–30KMB	K73	24-Lead Rectangular Cerpack	
				PALC22V10–30LMB	L64	28-Square Leadless Chip Carrier	
				PALC22V10–30QMB	Q64	24-Pin Windowed Leadless Chip Carrier	
				PALC22V10–30WMB	W14	24-Lead (300-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t_{PD}	9, 10, 11
t_{CO}	9, 10, 11
t_S	9, 10, 11
t_{II}	9, 10, 11

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CYPRESS SEMICONDUCTOR

PLCC and CLCC Packaging for High-Speed Parts

The semiconductor industry is constantly searching for package options that enhance the capabilities of high-performance devices. For fast device performance with minimal ground bounce, electrical characteristics must include low inductance and capacitance from external pin to die bond-wire pad. A package should also furnish good thermal characteristics for reliability over extended temperature ranges.

Other major properties sought after are low cost, as well as standardized outline/pin configurations for compatibility, ease of manufacturing, and handling throughput. The package must also work with surface mount technology and have a small footprint to save board space.

The package that best meets all these requirements is the PLCC (plastic leaded chip carrier). In the past, utilization of PLCCs was not practical for high-power, bipolar devices. However, the advent of low-power bipolar and BiCMOS ECL-compatible SRAMs and PLDs now provides the opportunity for high-volume usage. As manufacturers switch from bipolar to BiCMOS, the lower power dissipation of high-density ECL SRAMs and complex PLDs promise to give PLCC packages a bright future. For military applications and extended temperature environments or for devices with higher power dissipation, you can substitute the CLCC (ceramic leaded chip carrier).

The PLCC has many desirable qualities:

- Suitable for surface mounting with J-type leads
- Small footprint to save board space
- Low inductance and capacitance for high speed with little ground-bounce
- Good thermal characteristics for reliability over temperature range
- Ease of manufacturing and handling for production throughput
- Low cost compared to CERDIP, flatpack, LCC
- Standard package outline and pin-configuration compatibility

The PLCC's J-type surface-mount leads have the advantage over gull-wing leads, which are susceptible to fatigue. J leads also enhance handling ease in test and burn-in fixtures. The PLCC's 1-pF capacitance compares favorably with the 3 and 6 pF for plastic DIPs and CERDIPs, and inductance is equally impressive: 2 nH versus 6 and 11 nH for plastic DIP and CERDIP. Unlike flatpacks, PLCCs are available in standard tooling. PLCCs come in a variety of pin configurations, from 18 to over 200 pins, versus a maximum of 40 pins for plastic DIPs.

The Ceramic Leaded Chip Carrier

For high-temperature environments and high-power devices, you can make use of the ceramic leaded chip carrier (CLCC, Y package), which can also be surface mounted. The Y package has the same footprint and J leads as the PLCC (*Figure 1*) and works well for the faster PLDs and SRAMs.

If you do not know system temperature in the early stages of a design, you can substitute the Y package for the PLCC and vice versa, so long as the device's die junction temperature does not exceed 150°C. The Y package is slightly more expensive than the PLCC, but with a thermal resistance from junction to ambient (Θ_{JA}) of 35°C/W at 500 LFPM, the Y package can dissipate heat more efficiently.

Reliability

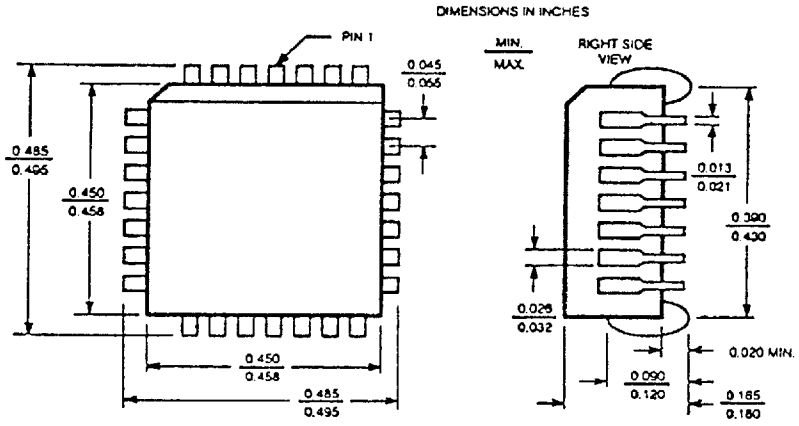
Cypress's bipolar and BiCMOS products in PLCC and CLCC packages go through extensive burn-in and testing at elevated temperature to guarantee package integrity. Cypress strongly recommends 500-LFPM system forced air flow but guarantees reliability in systems with or without the flow if the ambient air does not cause the junction temperature (T_J) to exceed 150°C.

The PLCC's Θ_{JA} is approximately 45°C/W. The SRAMs have power dissipation that ranges from 780 mW max for the CY100E422L-5 up to 1097 mW max for the CY10E474L-5. This dissipation results in junction temperature rises from 35 to 49°C. The 16P4-type PLD (CY100E302L-6) has a temperature rise of 39°C, and the

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T-90-20

28-Lead Plastic Leaded Chip Carrier J64



28-Pin Ceramic Leaded Chip Carrier Y64

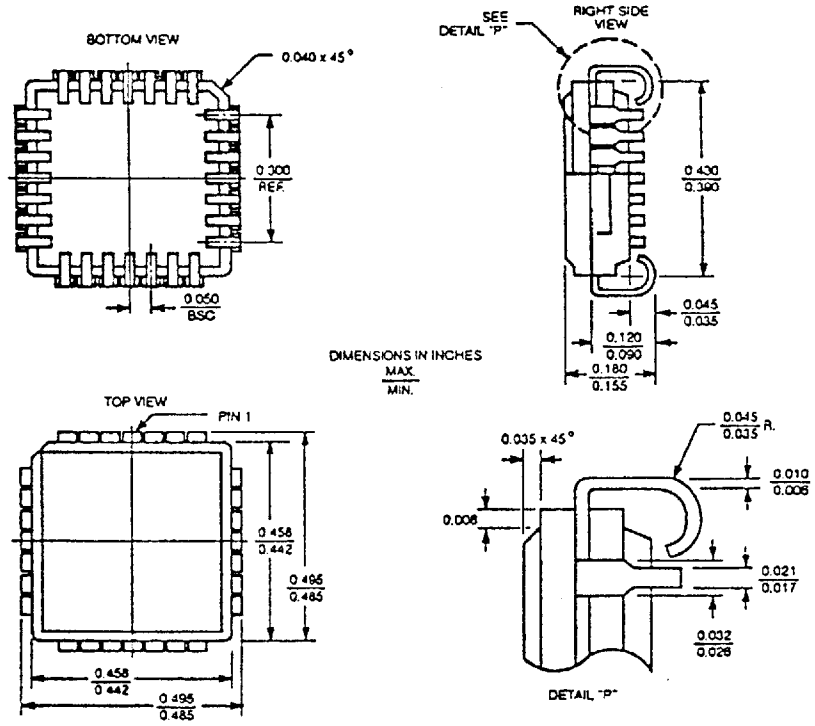


Figure 1. Diagrams of 28-Lead Chip Carriers

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16P8-type PLD (CY10E301L-6) has a temperature rise of 47°C. The CLCC package's Θ_{JA} equals 35°C/W for temperature rises of up to 55°C (CY10E474-3).

Finding Chip-Level Junction Temperature

The following relationship determines chip-level junction temperature for the PLCC package:

$T_J = \Delta T + T_A$

where

$\Delta T = P_D \times \Theta_{JA}$

and

$\Theta_{JA} = \Theta_{JC} + \Theta_{CS} + \Theta_{SA}$

To calculate worst case junction temperature (T_J) use maximum supply V_{EE} and I_{EE} for power dissipation and maximum T_A for the temperature range of interest. For the 10K/10KH CY10E301L in a PLCC, for example, device I_{EE} = 170 mA max and V_{EE} = 5.46V max for P_D = 928 mW. Add 15 mW per output for a total output P_D = 120 mW. Therefore, the total P_D = 1048 mW.

For a PLCC, Θ_{JA} = 45°C/W at 500 LFPM, and Θ_{JA} = 64°C/W for still air.

For a CLCC, Θ_{JA} = 35°C/W at 500 LFPM, and Θ_{JA} = 54°C/W for still air.

Because

T_J = total $P_D \times \Theta_{JA} + T_A$

and

T_A = 75°C worst-case commercial temperature range, for the PLCC:

T_J = (1.048 W)(45°C/W) + 75°C = 122°C at 500 LFPM

T_J = (1.048 W)(64°C/W) + 75°C = 142°C in still air

This calculation is for absolute worst-case data sheet conditions. The burn-in temperature used by Cypress (T_J) is much higher than the device will ever see in a system. Note that *most systems will not run at worst case due to guard-banding*. For this reason, use V_{EENOM} = 5.2V or 4.5V and I_{EENOM} = (I_{EEMAX})(85%) for nominal-condition calculations.

Real-World Values

Obviously, most systems do not operate at the worst-case conditions. Therefore, *Figures 2* through *5* show graphs over different operating conditions to determine failures in time (FITs) and mean time between failure (MTBF) for a typical system or in a worst-case scenario.

The graphs are based on a linear method of interpreting the failures observed at burn-in and indicate the long-term reliability of Cypress devices. You can use the graphs to determine MTBF and FITs for any Cypress device in any package after calculating the appropriate ΔT.

The X-axis on the graphs indicates junction temperature. These values are determined by adding the ΔT to ambient temperature, as described earlier. As an example, *Figures 2* and *3* note the following critical points for a CY10E301L ECL PLD under three different operating conditions:

- Point A — 10K/10KH typical data sheet conditions: 25°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 64°C, FITs = 7, MTBF = 18,000 yrs.
- Point B — 10K/10KH typical operating conditions: 55°C ambient, nominal V_{EE} and I_{EE}, 50Ω loads, 500 LFPM air flow, T_J = 94°C, FITs = 45, MTBF = 2800 yrs.
- Point C — 10K/KH absolute worst-case conditions: 75°C ambient, 5.46 V max and 170 mA max, 50Ω loads, 500 LFPM air flow, T_J = 122°C, FITs = 225, MTBF = 525 yrs.

The activation energy used for the MTBF and FITs information is 0.7 eV. This is an average number for die-surface-related defects, such as metal and oxide pinholes, etc., but is very conservative for silicon defects or mechanical interfaces to packages. The number is usually 1.0 eV. A small change here results in a significant change in MTBF or FITs. A change to 0.8 eV equates to a 33% reduction in FITs rate or a 50% increase in MTBF.

The Packages of Choice

The PLCC and CLCC are accepted as the packages of choice by many manufacturers of high-speed devices. Motorola Semiconductor uses the PLCC as the only package for the company's very high speed ECL$_{INPS}$ ECL logic family, which stands for "ECL in picoseconds" and is pronounced "eclipse." This family has set-up times and propagation delays in the sub-nanosecond range, with power dissipation of over 1W. Fully compatible with Cypress SRAMs and PLDs, the ECL$_{INPS}$ family includes many 10K, 10KH, and 100K standard logic gates, building blocks, and transceivers.

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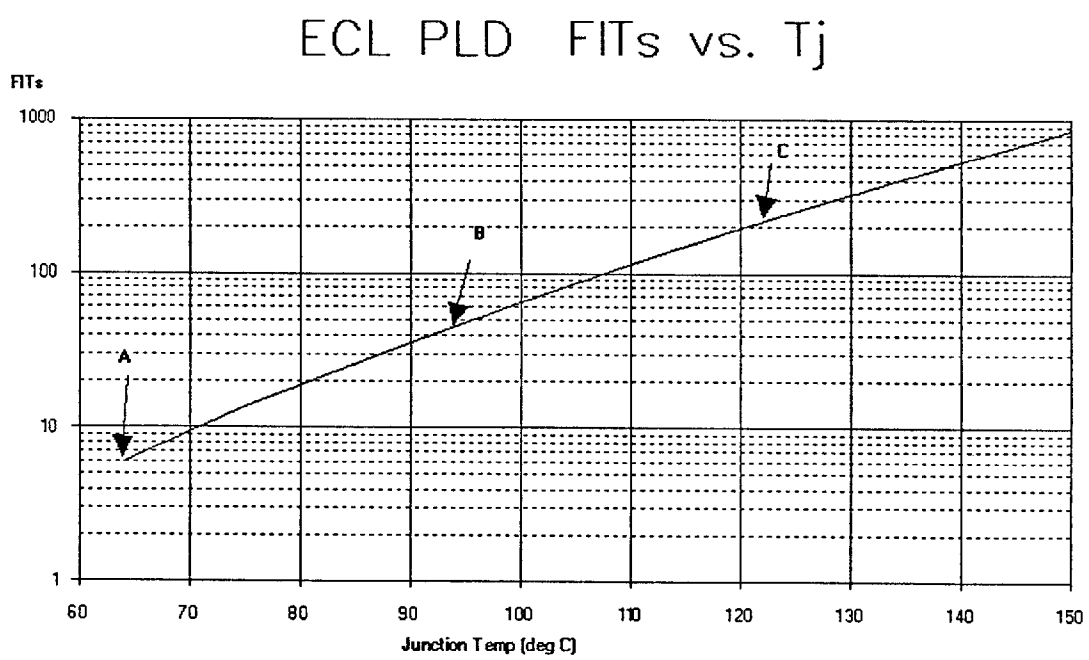


Figure 2. Failures in Time vs Junction Temperature

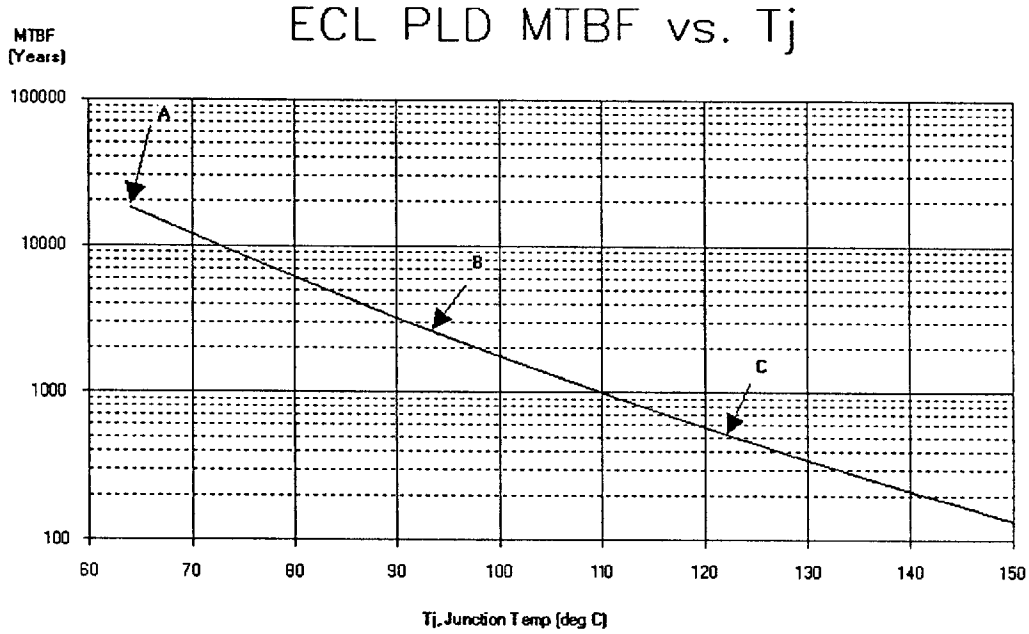


Figure 3. Mean Time Between Failures vs Junction Temp.

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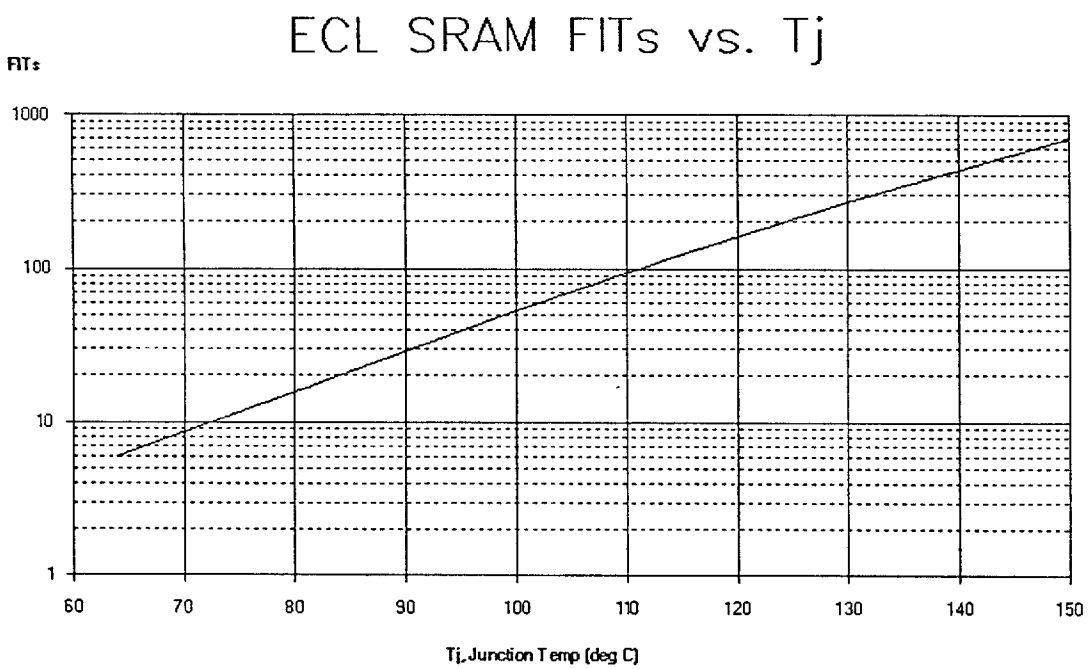


Figure 4. Failures in Time vs Junction Temperature

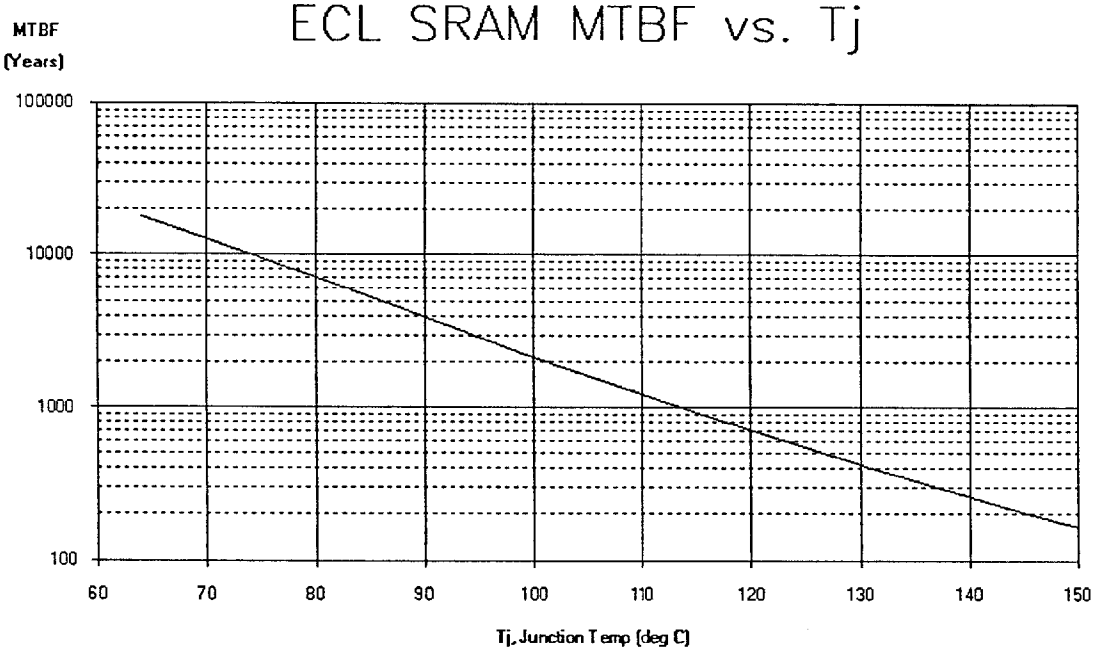


Figure 5. Mean Time Between Failure vs Junction Temp.

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