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PCVision*plus*®

Hardware

Reference Manual

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PCVision*plus*® Hardware
Reference Manual
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PREFACE

The PCVision*plus* frame grabber captures images from analog monochrome cameras at frequencies up to 53 MHz. The PCVision*plus* provides interface to a host computer through the PCI-bus.

- Chapter 1, “Overview” introduces the PCVision*plus* and provides operating specifications.
- Chapter 2, “Theory of Operation” describes the operation of the PCVision*plus*.
- Chapter 3, “Registers” provides detailed descriptions of every register and bit that controls the PCVision*plus*.
- Chapter 4, “DAC and PLL Programming” provides detailed descriptions of the serial interfaces and programming examples for PLL and XTAL modes.
- Appendix A, “Connectors and Cables” gives the pin-out of the connectors, and illustrates some of the cables currently available for the PCVision*plus*.
- Appendix B, “Using Opto-Isolators” gives some examples of using the opto-isolated trigger input, and connecting an opto-isolator to the PCVision*plus* outputs.

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DOCUMENTATION CONVENTIONS

The following conventions are used throughout this manual:

Example	*Description*
CAUTION	A caution calls attention to a hazard to the equipment or software; a condition, practice, or procedure that must be observed to avoid damage to or destruction of equipment.
NOTE	A note calls attention to essential information of special importance, interest, or assistance in operation.
X	When used within a table, this notation indicates an irrelevant bit value, also called a “don’t care”.
R/W	The bit or register supports both read and write access.
R-O	The bit or register supports read access only.
W-O	The bit or register supports write access only.
0x3F0, 03F0H	Hexadecimal numbers are preceded by 0x or followed by H.
0110B	Binary numbers are followed by a B.
lsb, msb	Least significant *bit*, most significant *bit*. The use of lower case letters means bits.
LSB, MSB	Least significant *byte*, most significant *byte*. The use of capitals letters means bytes.
DWORD	A 32-bit address or data value.
WORD	A 16-bit address or data value.
BYTE	An 8-bit address or data value.
LEN	Line Enable: digital signal that corresponds to horizontal timing signal on analog video, and HDRIVE in some digital cameras. When LEN is true or active, it corresponds to the active line time, and pixel data is valid. When LEN is disabled or false, it corresponds to the horizontal reset or horizontal blank timing.
FEN	Frame Enable: digital signal that corresponds to vertical timing signal on analog video, and VDRIVE in some digital cameras. When FEN is true or active, it corresponds to the active frame time, and pixel data is valid. When FEN is disabled or false, it corresponds to the vertical reset or vertical blank timing.
PLL	Phase-Locked Loop.
PTG	Programmable Timing Generator
PWG	Programmable Window Generator

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CHAPTER 1
INTRODUCTION

The PCVision*plus*® frame grabber digitizes monochrome analog video to 8 or 12 bits, at sample frequencies up to 53 MHz. The PCVision*plus* supports broadcast standard timing (RS170, CCIR), progressive scan and non-standard (variable scan) timing. The PCVision*plus* can support two monochrome cameras.

The high data transfer rate of the PCI-bus eliminates the need for on-board processing or display circuitry. Image display and processing is handled by the host computer resources. The linear format image memory allows acquisition of a variety of image sizes. The image memory behaves as a temporary buffer between the camera interface and the host PCI-bus system. The PCVision*plus* incorporates a hardware "scatter gather" table for highly efficient, fully automated image transfers from the image memory.

The PCVision*plus* is capable of bus mastering image data directly to a destination memory within the PCI-bus system, such as system memory or VGA memory. Transfer rates up to the theoretical PCI-bus limit of 133MB/s can be sustained, depending upon the host capabilities. Images can be transferred to host memory in a fraction of the time that they were acquired. By minimizing the PCI-bus transfer time and CPU overhead, more bandwidth is available for processing or other system resources.

1.1 PCI INTERFACE

The PCI-bus interface allows the PCVision*plus* to operate as both PCI-bus master and target (slave). Only DWORD (32-bit) access is supported. The PCVision*plus* is capable of bus mastering data from image memory directly to a destination within the system (system memory or another PCI target, such as VGA display memory). The PCVision*plus* interface also supports target access to the registers and image memory. PCI-bus interrupts may be generated based on events occurring on the PCVision*plus*. The PCVision*plus* provides configuration registers required by the PCI specification which allow the board to be recognized on power-up for automatic system configuration ("plug-and-play").

The PCVision*plus* contains a sophisticated bus master controller (BMC) with hardware scatter gather table. The host CPU is free to perform processing during bus master transfers rather than controlling the transfer operation. The BMC has multiple frame ping-pong source and destination capabilities which allow the application to program the PCVision*plus* to establish the needed amount of processing time. The BMC uses a programmable scatter gather table that supports up to 32K host memory segments. The scatter gather table is also used to transfer images in an x,y format directly to VGA memory for display, or re-interlace image fields from interlaced or dual-tap sources.

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1.2 PCVision*plus* SPECIFICATIONS

- The PCVision*plus* video connectors are pin-compatible with the previous PCVision PCI-bus frame grabber and camera cables. New cables support new camera features.
- A hardware jumper selects the power-up state of the OPTO-22 compatible I/O port. All parallel port outputs have an initial setting of either all 0 or all 1 based on the jumper setting. This feature adds flexibility when interfacing with LEDs and module racks. Refer to Figure 1–4.
- All addresses are assigned by the PCI-bus host computer. All configurable hardware characteristics are software controlled.

1.2.1 PCVision*plus* Video Inputs

- Standard RS170 or CCIR (monochrome).
- Progressive scan and non-standard (variable scan) up to 53 MHz. VCR and VTR are not supported.
- Two AC-coupled video inputs, terminated into 75 ohms.
- DC Restoration – automatic clamp pulse from stripped sync or programmable clamp pulse; programmable clamp voltage 0 to 2.5 Volts.
- Low-Pass Filters – 6.5 MHz and 12.5 MHz.
- Input gain – 2.1 (fixed)
- Programmable ADC positive and negative voltage references from 13-bit DACs, range 0 to 3.3 Volts.
- 12-bit 53 MHz ADC

1.2.2 PCVision*plus* Timing Inputs (Standard Video)

- Composite analog sync on video from CAM0 or CAM1.
- Separate Horizontal and Vertical digital sync; negative voltages not allowed.
- Programmable Sync Stripper line rate: 15 KHz to 66.5 KHz, supports non-standard line rates in PLL mode.

		VSYNC, HSYNC
Vi	0 to 5 V	Input voltage range
Vh min	2 V	Minimum high–level voltage
Vl max	0.8 V	Maximum low–level voltage
R	10 kohms	PCVision*plus* pull-up resistors

- Three miscellaneous camera control inputs.

1.2.3 Variable Scan Timing Inputs

- Area scan cameras up to 4K pixels by 4K lines. Line scan is not supported.
- Variable Scan inputs LEN, FEN, CLK digital timing from CAM0 or CAM1, negative voltages not allowed.

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- **CLK, Pixel Clock Input:** single-ended TTL, programmable polarity, Frequency 10 KHz to 53 MHz.
- **LEN, Line Enable Input:** single-ended TTL, programmable polarity. Minimum de-asserted or inactive (reset) pulse duration is one CLK period.
- **FEN, Frame Enable Input:** single-ended TTL, programmable polarity. minimum de-asserted or inactive (reset) pulse duration is one CLK period.

The sync stripper can be used in variable scan mode to strip field information from a composite sync signal, if available.

Table 1–1. Variable Scan Timing Parameters

Parameter	*Definition*	*Minimum*	*Maximum*
/FENmin	Minimum FEN inactive	1 CLK cycle	
/LENmin	Minimum LEN inactive	1 CLK cycle	
V*p*	CLK period	18.86 ns	100 ns
V*h*	CLK high	9.43 ns	50 ns
V*l*	CLK low	9.43 ns	50 ns
T*su*	LEN, FEN set–up to CLK rising edge	10 ns	
T*h*	LEN, FEN hold time from CLK rising edge	10 ns	
T*su*	LEN, FEN set–up to CLK falling edge (clock inverted)	10 ns	
T*h*	LEN, FEN hold time from CLK falling edge (clock inverted)	10 ns	

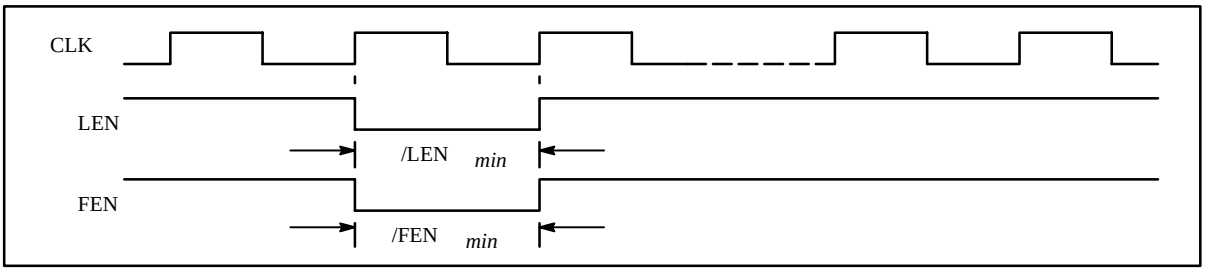


Figure 1–1. Line and Frame Timing

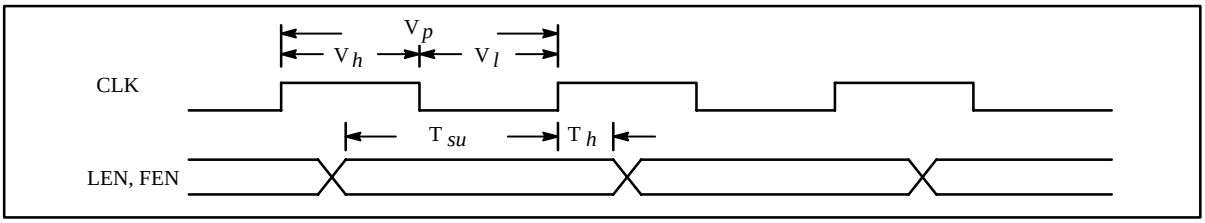


Figure 1–2. Set Up and Hold Timing

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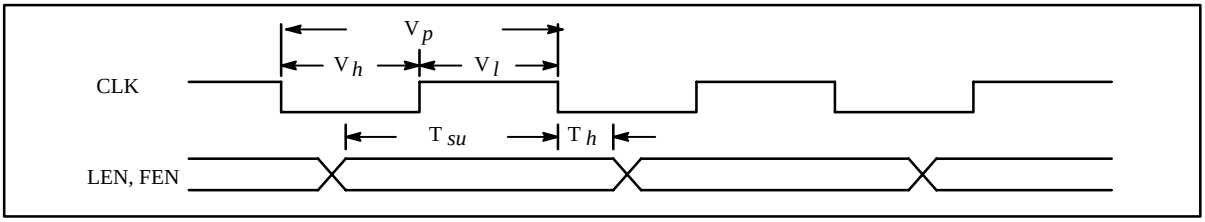


Figure 1–3. Set Up and Hold Timing, Clock Inverted

1.2.4 PCVision*plus* Trigger Inputs

- Trigger – 250 ns minimum pulse width, programmable edge-triggered.
- Two Opto-isolator Trigger Inputs: HP HPCL-0631 dual-channel isolator (maximum ratings in Appendix B)

Ifl	0 to 250 uA	Low-level input current range
Ifh	5 to 15 mA	High-level input current range
Vf	1.4 to 1.75 V	Forward voltage @ If= 10 mA
	250 ns	Minimum trigger pulse width

- Three TTL Inputs, with Schmitt filters

Vi	0 to 5.5 V	Input voltage range
Vh min	2 V	Minimum high-level voltage
Vl max	0.5 V	Maximum low-level voltage
Ii max	+/– 1 uA	Maximum input current
H	0.4/1.6 V	Minimum/Maximum hysteresis
R	10 kohms	PCVision*plus* pull-up resistors
	250 ns	Minimum trigger pulse width

- Two differential input, RS-422 and RS-423 compatible

V max	+/– 7 V	Maximum differential input voltage
Vth	+/– 200 mV	differential input threshold
R	100 ohm	Input termination
H	70 mV	Typical input hysteresis
	250 ns	Minimum trigger pulse width

1.2.5 PCVision*plus* Timing Outputs

- Strobe – two simultaneous pulse outputs, programmable delay, programmable polarity, one horizontal line duration.

I min	+/–100 mA	Maximum continuous output current
Ipk	+/–2 A	Peak output current

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- Frame Reset – two simultaneous pulse outputs; programmable delay, programmable pulse length, programmable polarity. (optionally may be used as clock inputs).

		FRST (Frame Reset)
Vh min	3 V	Minimum high-level voltage output
Vl max	0.55 V	Maximum low-level voltage output
Ih max	–32 mA	Maximum high-level output current
Il max	64 mA	Maximum low-level output current

- Programmable Timing Generator (PTG) – up to 2K by 2K (2048 by 2048).
- Horizontal and vertical syncs output to two cameras. (no composite output, no clock output)

		VSYNC, HSYNC
Vh min	3 V	Minimum high-level voltage output
Vl max	0.55 V	Maximum low-level voltage output
Ih max	–32 mA	Maximum high-level output current
Il max	64 mA	Maximum low-level output current

- Three miscellaneous camera control outputs

		MISC_IO_OUT
Vh min	2.4 V	Minimum high-level output voltage
Vl max	0.55 V	Maximum low-level output voltage
Ih max	–15 mA	Maximum high-level output current
Il max	64 mA	Maximum low-level output current

1.2.6 Image Memory

- 4MB linear mapped SGRAM.
- Acquires at camera data rate up to 53 MHz. Transfers to host at PCI-bus data rate (up to 133MB/s theoretical maximum).
- Mapped into PCI-bus memory address space, 32-bit access only.
- Programmable “valid video window” timing – 1 to 4K pixels per line, 1 to 4K lines per frame.

1.2.7 Output Scatter Gather Table

- “DMA Table” performs “destination scatter gather” for bus master transfer from image memory to PCI-bus host.
- Mapped into PCI-bus memory address space with control registers

1.2.8 Output Control Table

- Performs “source scatter gather” for bus master transfer from image memory to PCI-bus host.
- Re-sequences interlaced camera data in real time.
- Mapped into PCI-bus memory address space with control registers.

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1.2.9 Host Access

- Registers, LUT and Image Memory are mapped into PCI-bus 32-bit memory address space.
- Registers, LUT and Image Memory support target access.

1.2.10 Bus Master Transfer

- Transfer rates up to 133MB/s theoretical limit of PCI-bus; limited by bus traffic, block size, and capability of destination device.
- Bus Master Transfer to PCI-bus host memory, VGA, or other PCI-bus system resource.
- Hardware “scatter gather” table provides efficient automated transfer.
- Programmable horizontal zoom by 2 or 4 performed during bus master transfer.
- Horizontal decimation by 2 performed during bus master transfer, allows 12-bit image data to be sent directly to VGA memory as 8-bit data.
- Optional clipping during bus master transfer to VGA memory removes “color dots” in Windows (Windows reserved colors).
- Optional padding 8-bit data to 16-bit during bus master transfer to VGA secondary surface, for 4:2:2 display (16-bit “secondary surface”).

1.2.11 Parallel I/O Port

- One parallel I/O port: 8-bit TTL input, 8-bit TTL/CMOS output.
- 50-pin header is pin-compatible with OPTO22 I/O.
- F244 output buffers source 5 mA and sink 64 mA.

		IN7–0 Input Data
Vi	0 to 5 V	Input voltage range
Vh min	2 V	Minimum high-level input voltage
Vl max	0.8 V	Maximum low-level input voltage
Ih max	20 uA	Maximum high-level input current
Il max	–1.6 mA	Maximum low-level input current
		OUT7–0 Output Data
Vh min	2.4 V	Minimum high-level output voltage
Vl max	0.55 V	Maximum low-level output voltage
Ih max	–15 mA	Maximum high-level output current
Il max	64 mA	Maximum low-level output current

- Strobe input for latching input data, programmable rising or falling edge.
- Strobe output for latching output data.

I min	+/–100 mA	Maximum continuous output current
Ipk	+/–2 A	Peak output current

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- Interrupt input, programmable rising or falling edge.
- Supply +5 Volts at 500 mA with resetting fuse. Fuse is reset by disconnecting chassis power.
- A hardware jumper selects the default state of the parallel port. All parallel port outputs have an initial power up setting of either all 0 or all 1 based on the switch setting. See Figure 1–4.

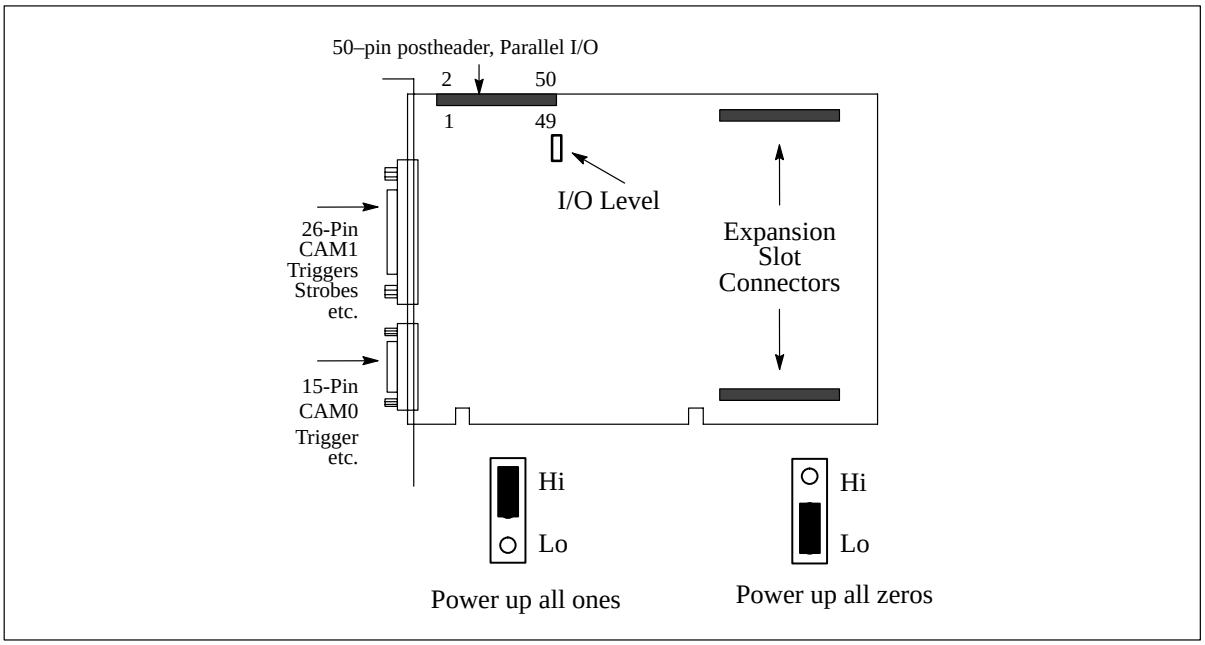


Figure 1–4. PCVision*plus* Connectors and Jumper

1.2.12 Environmental

- Board Size – PCI short card: 6.88 by 4.205 inches, 17.73 by 10.65 mm.
- Operating Temperature – 10-60 degrees Celsius.
- Relative Humidity – 0-90% non-condensing.
- Power Requirements (typical) - 1 Ampere at +5 Volts,
  5 Volt to 3.3 Volt conversion performed on the PCVision*plus* board.

1.2.13 Camera Power

- +12 Volts at 500 mA to cameras CAM0 and CAM1 from the PCI-bus chassis.
- Resetting switches disconnect power to the camera in an overload condition. The switches are reset by disconnecting chassis power.

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CHAPTER 2
THEORY OF OPERATION

This chapter describes the PCVision*plus* host interface and PCI-bus interrupts, memory architecture, image acquisition, bus master operations, and camera acquisition interface.

2.1 OVERVIEW

The PCVision*plus* digitizes standard and non-standard monochrome cameras using a 12-bit 53 MHz ADC (Analog to Digital Converter). An analog video multiplexer (MUX) supports two monochrome camera inputs.

The 8-bit or 12-bit data is input to a 16-by-16-bit LUT (Look-Up Table) for simple point transformation (or oversampling in 8-bit mode). The LUT data is output to image memory. Figure 2–1 is a block diagram of the PCVision*plus* frame grabber.

2.2 HOST INTERFACE

The PCVision*plus* provides direct access to the host system PCI-bus and can operate as both Bus Master and Target (slave). In Bus Master mode, the PCVision*plus* supplies both data and addresses to the bus, with the image memory frame being the data source. Only Bus Master write (PCVision*plus* writing data to the PCI-bus) is supported. As a target, the PCVision*plus* can be accessed by other Bus Masters in the host system. The PCVision*plus* supports read and write target access.

2.2.1 Memory Access

The PCVision*plus* image memory is occupies 4MB in the host system memory address space. During power-up, the PCI-bus host system assigns a base address to this region, written in the Base Address Four (BADR4) configuration register. The PCVision*plus* uses dual ported memory. One port supports image acquisition. The second port supports host PCI-bus access. Both ports can be accessed simultaneously.

PCVision*plus* has a linear memory architecture that provides flexibility for incoming images. There is no maximum size for horizontal and vertical sizes of acquired data (within size of the memory frame). Host access to the memory is always on DWORD (32-bit) boundaries. Every access provides four bytes. Bytes or WORDs can only be accessed by reading or writing on 32-bit address boundaries and masking or disregarding the extra bytes within the DWORD.

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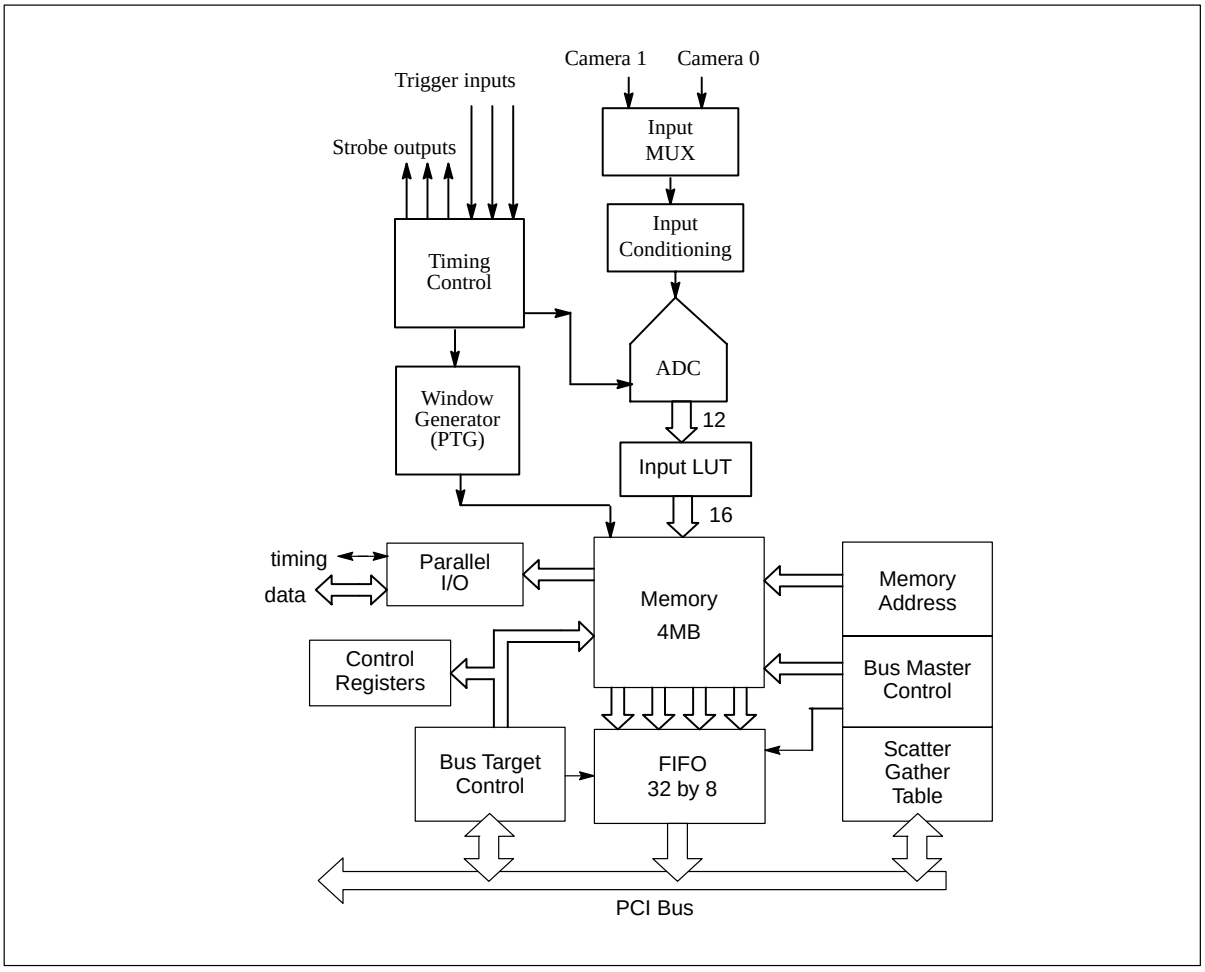


Figure 2–1. PCVision*plus* Block Diagram

2.2.2 Register Access

The PCVision*plus* registers are organized as five groups, each having different control over the board operation. All five sets of registers must be properly initialized for operation of PCVision*plus*.

2.2.2.1 PCI Configuration Registers

The PCI Configuration Registers are required for compliance with the PCI Specification. These registers are loaded by a boot PROM with information about the PCVision*plus*, (memory size, register size, type of device) which the PCI-bus host uses, in conjunction with information from all other PCI-bus devices in the system, to determine an optimum configuration. All configuration information is contained in these registers. No address jumpers or

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switches are required on the PCVision*plus*. Access to these registers is accomplished through special PCI-bus configuration cycles. A separate base address is not required for this register set.

2.2.2.2 PCI Interface Control Registers

The PCI Interface Control Registers control bus transfer configuration, interrupt configuration, and mailbox operations. These registers require a separate base address which is determined by the system on power-up and written into the Base Address Zero Register (BADR0) of the Configuration register set. Software can determine the base address of these registers by executing a configuration register read cycle to the BADR0 register.

2.2.2.3 Board ID Registers

The Board Identity registers contain the build status and board revision information, and load the FPGAs (field programmable gate arrays). These registers require a separate base address which is determined by the system on power-up and written into the Base Address One Register (BADR1) of the Configuration register set. Software can determine the base address of these registers by executing a configuration register read cycle to the BADR1 register.

2.2.2.4 Acquisition Module Control Registers

The Acquisition Module (AM) Control registers control the camera interface and timing. These registers require a separate base address which is determined by the system on power-up and written into the Base Address Two Register (BADR2) of the Configuration register set. Software can determine the base address of these registers by executing a configuration register read cycle to the BADR2 register. The input LUT is mapped with these registers.

2.2.2.5 Frame Buffer Control Registers

The Frame Buffer Control Registers control image memory frames, interrupts, image acquisition, scatter gather table, output control table, and the bus master controller. These registers require a separate base address which is determined by the system on power-up and written into the Base Address Three Register (BADR3) of the Configuration register set. Software can determine the base address of these registers by executing a configuration register read cycle to the BADR3 register.

2.2.3 PCI-bus Interrupts

PCVision*plus* provides the capability to generate a PCI-bus interrupt based on various events. All interrupts are combined and sent to the PCI-bus as a single interrupt signal.

Interrupts can be broken down into several categories: Acquisition interrupts, Frame Memory Interrupts, Bus Master Interrupts, and PCI interface interrupts. Several levels of control are required for these different sets of interrupts. Common to all interrupts are two registers found in the PCI Configuration register set: Interrupt Line (INTLN) and Interrupt Pin (INTPIN). INTPIN is initialized on power up to define the PCI-bus interrupt pin used by PCVision*plus* as #INTA (this is required for PCVision*plus*). The INTLN register is initialized to select the system interrupt line. On the next level, in the PCI Interface Control Register Set is a register called Interrupt Control Status (INTCTL_32) register, which enables and monitors all interrupts. Within the INTCTL_32 register is a bit (INTEN) common to all interrupts, which must be set for any source to generate a PCI-bus interrupt. In addition, there are two control registers used for acquisition interrupt control and source selection.

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2.2.3.1 Master/Target Abort Interrupts

Once the configuration register INTLN and the INTEN bit in the INTCTL_32 register are initialized, the BMC monitors all PCI-bus transactions and generate an interrupt if it encounters either a Master or Target Abort. Master Abort occurs when the PCVision*plus* attempts to transfer data to a non-existent or disabled Target. Target Abort occurs when the PCVision*plus*, in the process of a bus master transfer, encounters a target abort response from the destination of the transfer operation (typically indicating some sort of error in the transfer). These two interrupt sources are always enabled if INTEN is set, and can be monitored or cleared by two bits (MAINT and TAINT) in the INTCTL_32 register.

2.2.3.2 Bus Master Transfer Interrupts

PCVision*plus* can be configured to generate an interrupt when a bus master transfer has completed. When the Bus Master Transfer count (BMXC_32) decrements to zero, only the current segment transfer is complete, not the whole transfer. The BMINT bit in the INTSTAT register indicates the last segment transfer is complete (end of scatter gather table entries).

2.2.3.3 Acquisition Interrupts

PCVision*plus* has multiple acquisition related interrupt sources. start of trigger cycle, end of trigger cycle, hardware timer/counter, parallel I/O port interrupt input, acquire address, vertical blank (even, odd or any) and end of frame are all sources available to generate PCI-bus interrupts. The INTLN register and the INTEN bit of the INTCTL_32 register must both be set properly for any of the sources. The AMINTEN and INTENREG registers enable the interrupt sources. The AMINTCLR and INTSTAT registers contain status bits for all interrupt sources. Interrupt sources with an enable bit in the AMINTEN register require two levels of enabling and monitoring. In addition, the INTCTL_32 register contains an enable bit (INTEN) required to enable all PCVision*plus* interrupts, and status bit (INTST). The following order of setting and clearing acquisition interrupts must be followed:

- Set the desired interrupt source(s) in the AMINTEN and INTENREG registers.
- Set the INTEN bit in the INTCTL_32 register (required for all interrupts)
- Clear any pending acquisition interrupt by writing the INCLR bit in the BMCTL_32 register to one.
- Clear the interrupt status bits in the AMINTCLR and INTSTAT registers (by writing all ones) to eliminate any previous interrupts.
- Once an interrupt occurs, read the INTCTL_32 register (INTST bit will be set if the source(s) selected in the INTENREG and AMINTEN registers caused the interrupt) the INTSTAT register and the AMINTCLR register
- Once it is determined (from the status bits in INTSTAT and AMINTCLR) that an acquisition interrupt occurred, first clear the status bit in AMINTCLR, then clear the status bit in INTSTAT, and then clear the INTST bit in the INTCTL_32 register.

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2.3 IMAGE MEMORY

The PCVision*plus* image memory is mapped as a 4MB region in the host system memory region. During power-up, a base address to this region is assigned by the PCI-bus host system and stored in the Base Address Four (BADR4) configuration register. PCVision*plus* provides simultaneous access for host access and image acquisition.

The linear memory architecture provides flexibility for incoming images. There is no maximum limit for x,y sizes of acquired data (within size of the image frame). Host access to the memory is always on DWORD (32-bit) boundaries. Every access provides four 8-bit pixels, two 16-bit pixels, or one 32-bit pixel.

2.3.1 Image Acquisition

The PCVision*plus* supports interlaced or non-interlaced camera data. Interlaced data is stored as two separate fields, and re-interlacing is accomplished by the bus master controller. Images can be any size within the 4MB size of memory, on 8-byte (8 pixel) boundaries. Two types of image acquisition are available, External Trigger and Normal. Normal acquisitions into memory are based only on camera frame timing. External Trigger acquisitions are based on external trigger signals (and camera timing).

2.3.1.1 Normal Acquisition

The beginning and ending of a normal acquisition is based on the framing signal FEN (frame enable) out of the PWG. FEN is the digital version of the Vertical Blank signal. A snap command performs a single frame acquire beginning at the next FEN rising edge. A grab command performs continuous acquisition beginning on the next FEN rising edge. A freeze command will stop a grab at the next falling edge of FEN. When acquiring interlaced images, a snap lasts for two fields (1 frame). When acquiring non-interlaced images, a snap lasts for one field (1 frame). Interlaced image acquire can be programmed to start on the even field, odd field, or next field. Figure 2–2 shows an example of a non-interlaced snap.

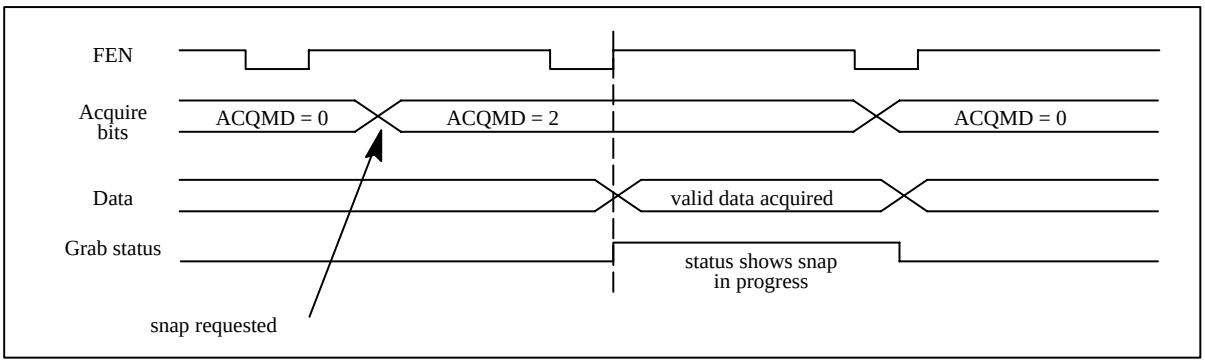


Figure 2–2. Non-interlaced Acquire

Figure 2–3 shows an example of an interlaced snap with the field select bits set for odd field acquire. Field select bits are used to determine which field of the interlaced image will be acquired first. Setting these bits for next field allows either field, even or odd, to be acquired next.

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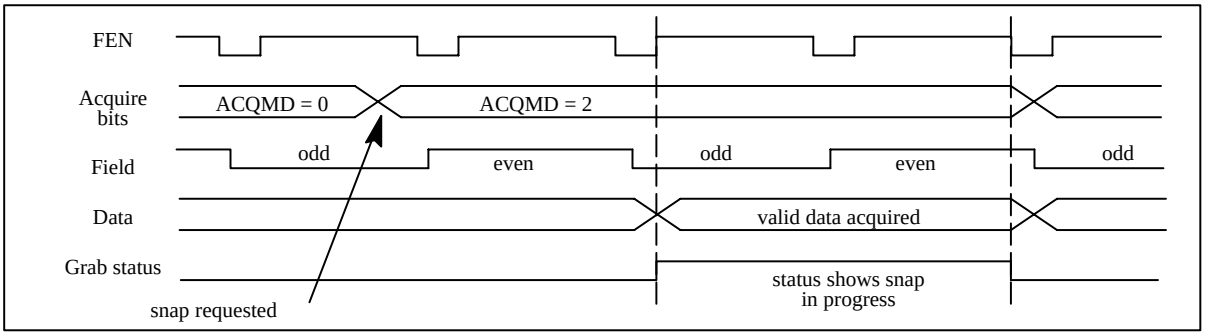


Figure 2–3. Interlaced Acquire

2.3.1.2 External Trigger Acquisition

External Trigger allows image acquisition to be synchronized to external events. When acquiring an image in external trigger mode, the acquisition will not start until the PCVision*plus* receives a trigger signal. Acquisition begins with the next valid frame after the trigger. When performing external trigger acquisition, be sure the starting field bits are set for next field. Figure 2–4 shows an example of triggered acquire. The trigger input remains armed after the acquire completes, ready for the next trigger input.

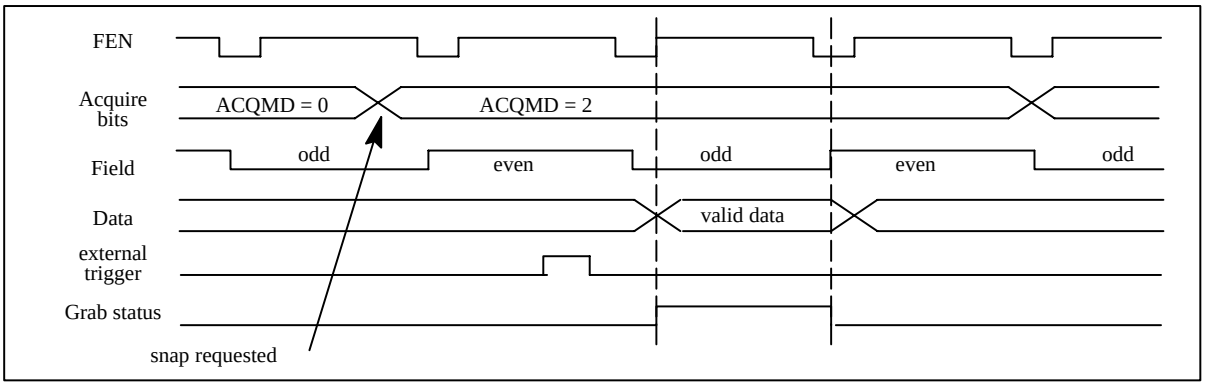


Figure 2–4. Triggered Acquire

2.3.1.3 Multiple Frame Acquire Mode

PCVision*plus* has the ability to acquire and store up to eight images sequentially into image memory, with the execution of one snap command. Program the Frame Count bits (FCNT) to the desired number of frames (1 to 8). For non-interlaced or interlaced acquisitions the multiple acquire mode count (FCNT) always refers to full frames.

In Normal mode, the frame count is set for 1 to 8 images. When a Snap command is executed, the programmed number of images is acquired sequentially into a memory frame. In Grab mode, the program number of images is acquired and then the acquire address resets back to the Start of Acquire address, and continues, overwriting the previous images. It is also possible to disable this reset to the Start of Acquire address, and the acquire continues

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stepping through the memory addresses sequentially, without resetting. The image size must be taken into account when acquiring multiple images. The memory is 4MB and wraps around if the number of incoming pixels fills the buffer.

In Triggered mode (snap or grab) each incoming external trigger will acquire one frame and advance the frame count. In triggered snap mode, each incoming trigger acquires a frame until the frame count is reached and the snap operation ends. In triggered grab mode, each incoming trigger acquires a frame until the frame count is reached, the frame count resets, the acquire address resets (unless reset is disabled), and the triggered acquire continues until a freeze command is issued.

Using multiple frame mode with bus mastering allows simultaneous acquire and transfer without loss of video. A typical application would use a frame count of two and program a grab acquire. At the end of the first image, a request is sent to the bus master controller which processes the request and transfers the first image. Simultaneously, the second image is acquired into the next "frame" location in the memory frame. No data gets written over as long as the transfer of the first image is completed prior to the end of the second image acquire. The operation repeats when the second image finishes, a second request for transfer is sent to the bus master controller. The second image is transferred and the acquire operation switches back to the first frame. This sets up a "ping–pong" acquire buffer, which can be useful to maintain acquire and transfer rates.

2.4 BUS MASTER OPERATION

During a bus master operation the PCVision*plus* is granted control of the PCI-bus and becomes the source of both address and data to some other target location within the system.

Before any type of bus master transfer can begin, the the destination address (in the host) and the transfer count (number of bytes or pixels to transfer) as well as the source address (in PCVision*plus* memory frame) must be programmed into PCVision*plus* registers, and several other registers and bits controlling and enabling the transfer mode must be set.

2.4.1 Scatter Gather

When a software application requests a host destination buffer, typically a group of small segmented pages are given rather than a large contiguous block of system memory. The "small pages" are where the image data is scattered throughout the host memory, like a fragmented file on a hard disk. The host keeps track of these "small pages" to gather the data during processing, much like the file record allows processing fragmented files.

To transfer the source image to a segmented buffer in system memory, multiple "small page" transfers must be executed which normally requires the host to poll throughout the transfer operation. The host sets up each small page transfer, polls for completion, and executes the next page transfer until the entire segment is complete. End of transfer interrupts can not be used, because the pages are too small (typically 4KB in x86 systems). Using a hardware scatter gather table eliminates the need for polling, and speeds up the transfer process.

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2.4.2 Scatter Gather Table

The scatter gather table (or “DMA table”) performs “destination scatter gather”. The scatter gather table has 32K Destination Descriptors, which define the size and address of the “small pages” of the destination buffers in host memory. The Segment Size (SGSZ) register indicates how many Destination Descriptors are programmed in the DMA Table. The Bus Master Controller automatically uses all of the programmed descriptors during the bus master operation until the complete frame or image is transferred.

Each Destination Descriptor contains a destination address followed by a transfer count size. This allows support for different transfer count sizes for each data block (dynamic transfer count).

2.4.3 Output Control Table

The Output Control Table (OCT) performs “source scatter gather”. The OCT is programmed to take advantage of the storage format. Each table entry in the OCT is 32-bits and controls the transfer of up to 256 bytes of image data from the buffer to the PCI interface circuitry. The addresses and count values are loaded into the bus master controller to indicate the source data for bus master operations. During bus master transfer, the PCVision*plus* reads the table entries sequentially and transfers image data to the PCI-bus interface as directed. The OCT provides a very high level of control and flexibility for bus master transfers. The OCT supports a variety of PCVision*plus* features including image re-sequencing and ROI (region of interest) output.

2.4.4 Output Formatting

The memory control and bus master controller work together to provide some additional hardware formatting during bus master transfer. Clipping and Padding are mutually exclusive operations.

2.4.4.1 Region of Interest

PCVision*plus* supports Region Of Interest (ROI) capability during bus master transfer. The OCT must be programmed to transfer an ROI subset of the image in PCVision*plus* image memory. This can reduce PCI-bus bandwidth requirements.

2.4.4.2 Zoom and Decimate

The PCVision*plus* bus master controller (BMC) provides horizontal zoom by 2, zoom by 4, and decimate by 2 (1/2 zoom). This does not change the data in the image buffer memory. Vertical zoom or decimate must be handled by the OCT. In 8-bit mode, each BYTE read is replicated in the BMC. In 12-bit mode, each WORD read is replicated in the BMC.

In 8-bit mode and zoom by 2, each BYTE (8-bit pixel) read from image buffer memory is replicated twice (duplicated) in the BMC before output to the PCI-bus, as shown in Figure 2–5. The transfer count must be doubled for zoom by 2. The data output is twice the data read from the image memory.

In 8-bit mode and zoom by 4, each BYTE (8-bit pixel) read from the image buffer memory is replicated four times in the BMC before output to the PCI-bus, as shown in Figure 2–5. The transfer count must be multiplied by four in zoom by 4. The data output is four times the data read from the image memory.

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In 12-bit mode and zoom by 2, each WORD read from the image buffer memory is replicated twice in the BMC before output to the PCI-bus, as shown in Figure 2–6. The transfer count must be doubled for zoom by 2. The data output is twice the data read from the image memory.

In 12-bit mode and zoom by 4, each WORD read form the image buffer memory is replicated four times in the BMC before output to the PCI-bus. It takes two 32-bit transfers to perform 12-bit zoom by 4. Figure 2–6 shows the first of two transfers for the zoom by 4. The transfer count must be multiplied by four in zoom by 4. The data output is four times the data read from the image memory.

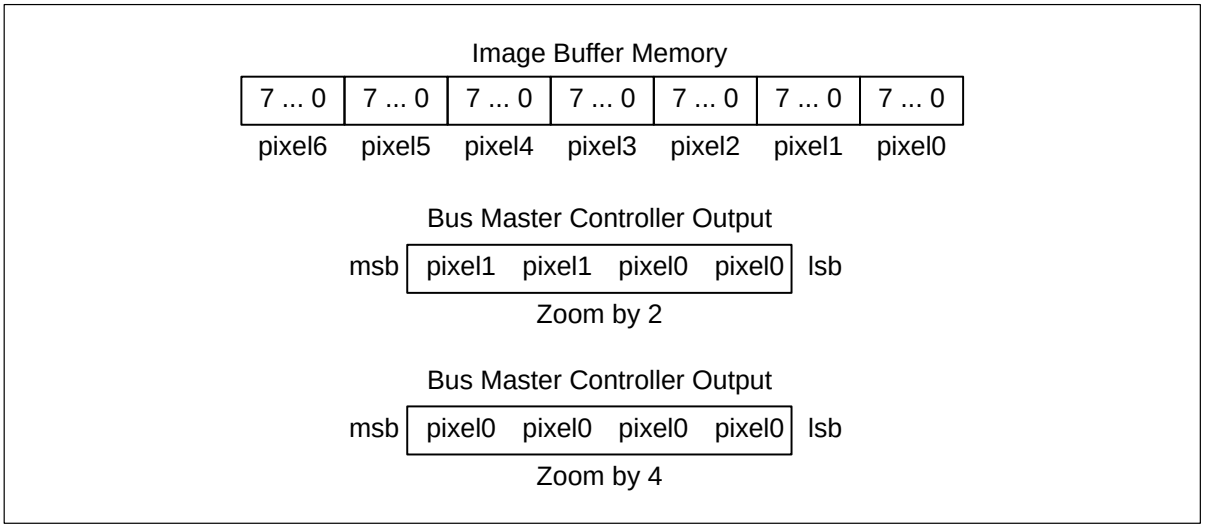


Figure 2–5. Bus Master Zoom, 8-bit Mode

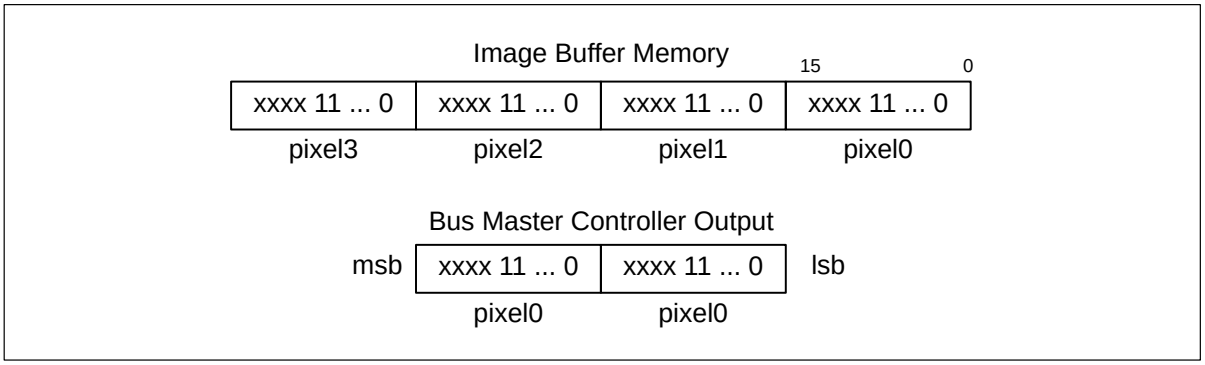


Figure 2–6. Bus Master Zoom 2, 12-bit Mode

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In 8-bit mode and Decimate by 2, the BMC transfers every other byte (pixel) read from the image memory buffer. The byte select bit (BYTESEL) selects the even or odd bytes for transfer, as shown in Figure 2–7. The transfer count must be divided by 2; the transferred output data is half the area of the original image data in the image buffer memory.

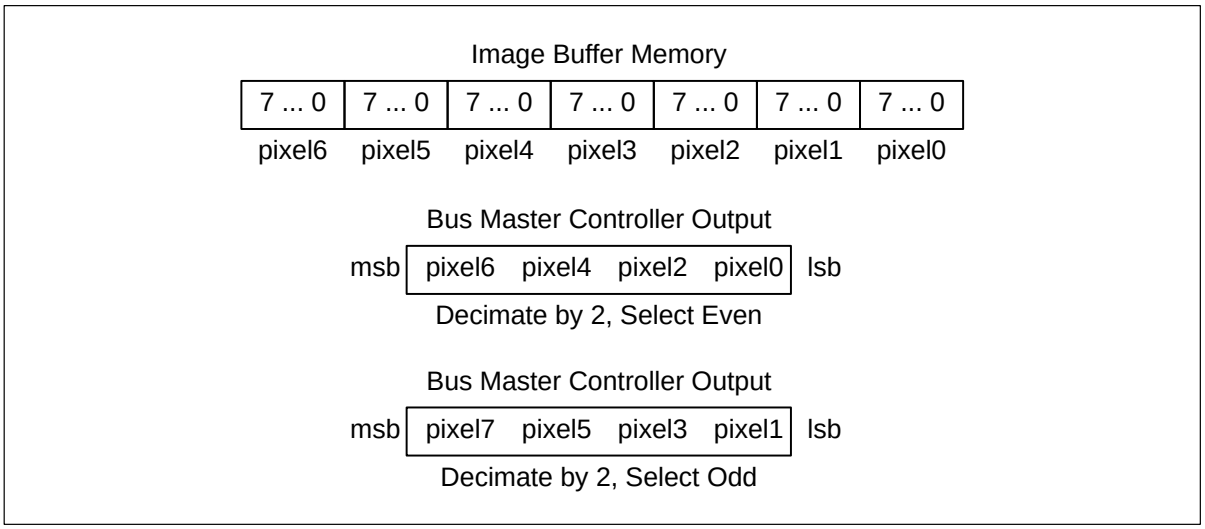


Figure 2–8. Bus Master Decimate, 8-bit Mode

In 12-bit mode, Decimate by 2 performs a shift and pack operation. This is very useful for quickly displaying 8-bit data from un-normalized 12-bit data, without using host computer resources for shift, zoom, decimate, or pack operations to get an 8-bit display from 12-bit data.

In 12-bit mode each 12-bit pixel occupies two bytes. If the data is not normalized to 16 bits by the input LUT, the low byte contains pixel bits 7 through 0, and the high byte contains pixel bits 11 through 8 with the upper 4 bits filled with “don’t care” values, as shown in Figure 2–9.

In 12-bit Decimate by 2 mode, the bus master controller reads a word of image buffer data, right-shifts four places, and packs only the new low byte for output to the PCI-bus. Each byte output contains the upper 8 bits (11–4) of the 12-bit pixel, with no “don’t care” bits.

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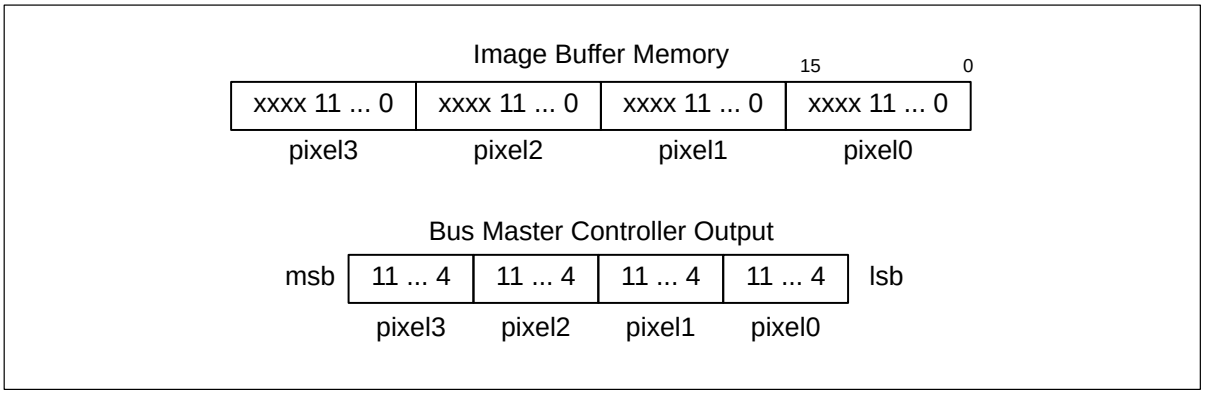


Figure 2–9. Bus Master Decimate, 12-bit Mode

2.4.4.3 Padding

The PCVision*plus* has the capability to pad 8-bit or 12-bit image data to 16-bit values during the bus master transfer. With pad mode enabled, a value of 0x80 is added to each 8-bit pixel value in the bus master FIFO. The 0x80 is the neutral or zero value of luminosity, the color component of the YCrCb data.

Each 32-bit bus master transfer contains two 16-bit (padded) pixels. The padded values are useful for display from the 16-bit Windows secondary surface (also referred to as the “YCrCb surface”, or a YCRCBMONO display sink) on VGA boards that support the secondary surface (also called streams processing). Padding is a function of the bus master interface and does not affect pixels in PCVision*plus* image memory. Because the PCVision*plus* transfer time is so fast, it becomes practical to transfer the unchanged 8-bit or 12-bit image data to the host for processing, and also transfer 16-bit padded data to the VGA memory for display.

Padding should not be enabled when clipping is enabled. Clipping is used for transfer to the primary display surface, and padding is used for transfer to the secondary display surface. The two features should never be used together.

In 8-bit mode, enable padding, enable zoom by 2, and double the transfer count. The zoom factor replicates each pixel value, and the padding mode overwrites the duplicate value in the FIFO with 0x80 before transferring, as shown in Figure 2–10.

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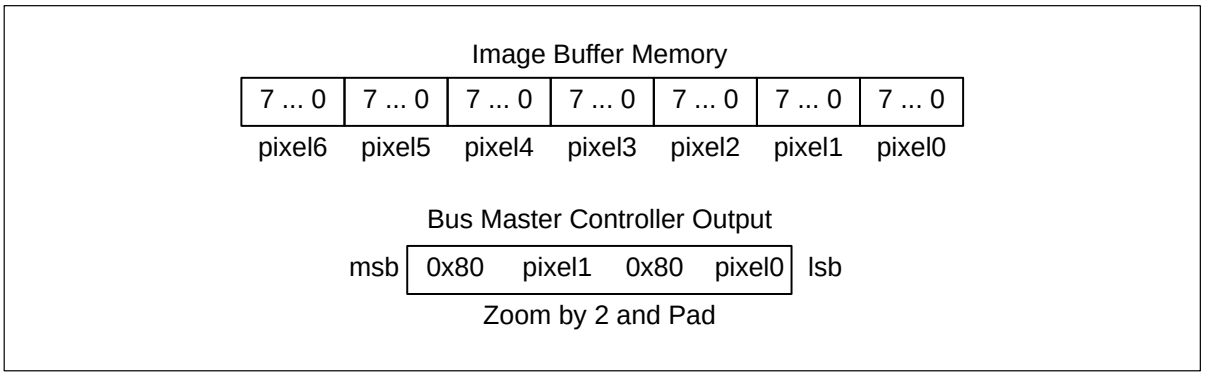


Figure 2–10. Padding 8-bit Data

In 12-bit mode, enable padding but do not enable zoom and do not change the transfer count. Each word read from the image buffer memory is right-shifted four bits, and the lower eight bits are written to the BMC FIFO, with 0x80 replacing the upper eight bits (now all “don’t care”) as shown in Figure 2–11.

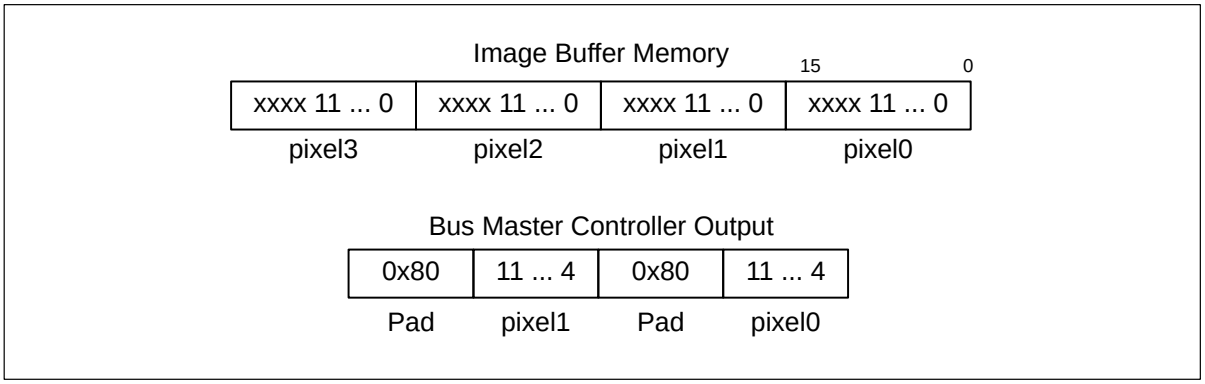


Figure 2–11. 12-bit Padding

2.4.4.4 Clipping

The PCVision*plus* provides an 8-bit data clipping feature that forces pixels with values between 0x0 and 0xF to the value 0x10, and forces pixels with values between 0xF0 and 0xFF to the value 0xEF. This clipping feature allows 8-bit image data to be bus mastered directly to a VGA target (primary surface) without seeing “color dots” (MS Windows reserved values). The clipping feature can be disabled to allow true pixel values to be sent directly to a PCI destination. Clipping is a function of the bus master interface and does not affect pixels in PCVision*plus* image memory. As a result, the same image could be bus mastered twice; to a VGA display memory with clipping enabled, and to host memory with clipping disabled. Because the bus master transfer speed is faster than acquisition speed, this method is not impractical.

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Clipping should not be enabled when padding is enabled. Clipping is used to transfer 8-bit image data to the primary (8-bit VGA) display surface, and padding is used to transfer 8-bit or 12-bit image data to the secondary (16-bit YCrCb) display surface. The two features should never be used together.

2.4.4.5 Bus Master Data Shift

The BMC includes a mode for internally shifting or normalizing 12-bit data to 16 bits. In 12-bit mode each 12-bit pixel occupies two bytes. If the data is not normalized to 16 bits by the input LUT, the low byte contains pixel bits 7 through 0, and the high byte contains pixel bits 11 through 8 with the upper 4 bits filled with “don’t care” values, as shown in Figure 2–12. With BMSHIFT enabled, each word read from the image buffer memory is left-shifted four places. The 12-bit image data was moved from the lower 12 bits of the data word to the upper 12 bits of the data word. This is also called “normalization to 16 bits”.

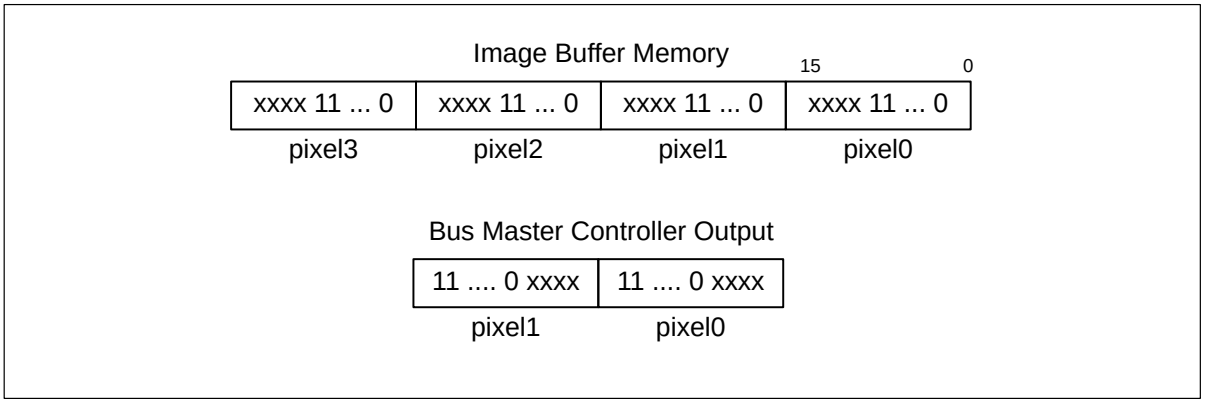


Figure 2–12. Bus Master Data Shift

2.4.5 Bus Master Latency

Transfer speed is mainly dependent on the host system and the target’s capabilities. Bus traffic (other bus masters arbitrating for and gaining bus ownership) and target capabilities (PCVision*plus* can only transfer data as fast as the target can receive it) have implications on overall transfer speed. Within the configuration register set are several registers which define the amount of time the PCVision*plus* requires for bus master operations. The Latency Timer register is set with a value (number of PCI-bus clocks) that defines the minimum guaranteed time PCVision*plus* will be allowed to hold bus ownership during a bus master transfer. This register acts as a counter during bus master transfers, and once it counts down from its programmed value any other bus master request will cause PCVision*plus* to lose bus ownership. This register can be set to prevent multiple bus disconnects during a PCVision*plus* transfer. Two other registers exist in the configuration register set which provide information to the system about the time the PCVision*plus* requires for bus master transfers. Minimum Grant is set to the maximum value, indicating the PCVision*plus* desires at least 64 us (microseconds) for each transfer. Maximum Latency is set to the minimum value, indicating the PCVision*plus* desires 250 ns (nanoseconds) in between bus master transfers. The use of these registers is system dependent, and not always required.

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2.5 CAMERA INTERFACE

The functional blocks that perform video input conditioning are: Input MUX, Gain and Offset, Low-Pass Filtering, DC restoration, programmable ADC references, and ADC.

2.5.1 Input MUX

The input stage is a 2:1 analog video multiplexer (MUX) which allows two monochrome analog inputs from the CAM0 and CAM1 connectors. The input is selected by software control. The timing is common to both inputs. Independent timing is not available. Asynchronous inputs are not supported by the PCVision*plus*. The timing and synchronization settings apply to both inputs synchronously. Multiple monochrome cameras must be externally genlocked or driven by the PCVision*plus* programmable timing. When using the sync stripper, the synchronization signals must be input on the composite video signal, or on a separate (horizontal and vertical) sync signals on the CAM0 or CAM1 connectors.

2.5.2 Gain

Data passes through a gain stage with a 2.1 gain setting. The 2.1 value, used with RS170 and CCIR video signals provides the correct gain needed for the desired 1.5 Vpp sampling window of the ADC. Standard video signal amplitude is 0.714 mV and 2.1 times 0.714 = 1.5 Volts. To achieve best performance, the video amplitude should fit the sampling range of the ADC as closely as possible. As shown in Figure 2–13, there are several ways to accomplish changing the video amplitude. The first step is always proper lighting at the video source, to achieve a good dynamic range of the input video signal. The next option is to increase the incoming video amplitude (before the ADC). The last resort should be adjusting the ADC sampling voltage range. The optimum range for the ADC used on the PCVision*plus* is 1.5 Volts peak-to-peak.

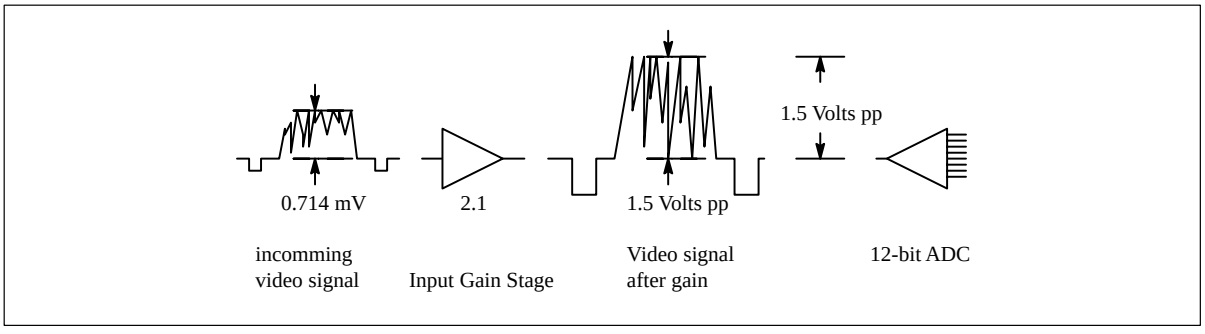


Figure 2–13. Input Gain Stage

Incoming video is terminated into 75 ohm resistors, as Figure 2–14 illustrates. Camera output is specified as voltage into a 75 ohm termination. The value at the video input connector (into 75 ohms) is half the measurable open circuit value (no cable connected) at the camera output connector.

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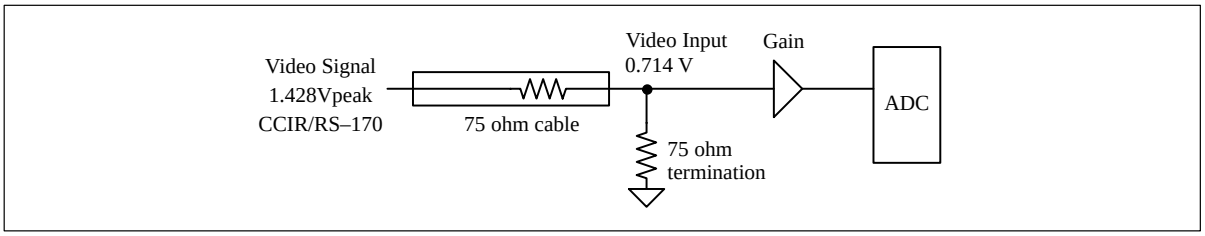


Figure 2–14. Input Voltage

2.5.3 Low-Pass Filters

Following the gain stage, the video passes through a selectable low-pass filter, optimized for standard video frequencies. The filter values are 6.5 MHz and 12.5 MHz (no bypass or disable). The low-pass filter strips high frequency signal content from the incoming video signal, to avoid sampling aliasing artifacts in the signal.

Standard video (RS170, CCIR, NTSC, PAL) has useful frequency content up to approximately 6.5 MHz. Frequencies above this can be eliminated using the low-pass filters. Sampling rates for standard video are 10 MHz up to 14 MHz. If frequencies at or above the sampling rate are present they represent noise rather than useful video. These frequencies can “alias” into the real video signal causing corruption. The low-pass filters can eliminate any high frequency signal content before digitization. Figure 2–15 illustrates the 6.5 MHz filter response.

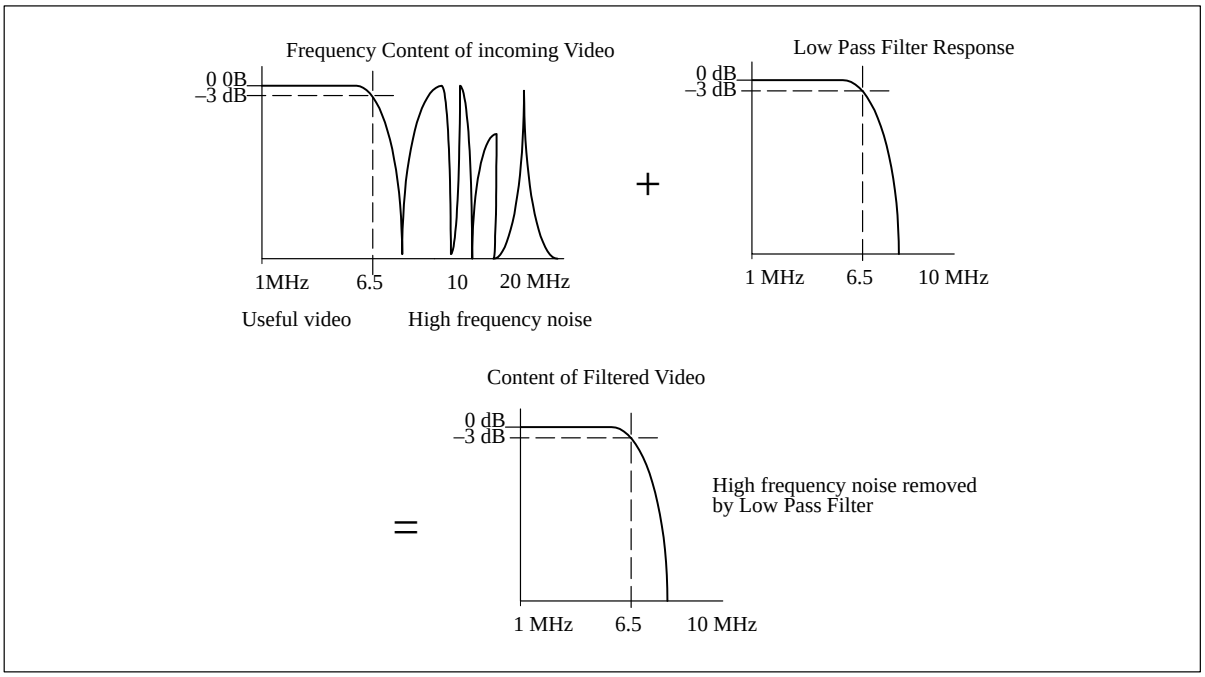


Figure 2–15. Low-pass Filtering

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The different signal response of the two low-pass filters creates a difference in the signal delay, of approximately 35 ns, between the two filter paths. This difference must be compensated for when switching between the low-pass filters. At a sample rate of 20 ns (50 MHz) the shift is approximately 0 to 1 pixel, worst case. At a sample rate of 60 ns (16.7 MHz) the shift is approximately 1 to 2 pixels, worst case. You may see a visible horizontal shift in the image when you select between the two low-pass filters. You can choose to ignore this shift, or you can adjust the values of HOFF and HACT, moving the video window 1 or 2 pixels right or left as needed, to realign the image.

2.5.4 DC Restoration

The video input is AC coupled. DC restoration is required to clamp the “back porch” of the video signal to the appropriate voltage level for digitization. The back porch is the reference “black level” voltage in analog video signals, and must be used by the ADC as a black reference. Two modes of generating a clamp pulse are provided; Sync Stripper Clamp and Programmable Clamp. Both use the programmable clamping voltage.

2.5.4.1 Sync Stripper Clamp Pulse

The sync stripper receives the composite video signal, and produces separate horizontal, vertical, composite, and field signals, as well as a clamp pulse positioned on the back porch of the incoming video signal. When the stripped clamp pulse is selected, the DC restore circuit clamps the back porch as illustrated in Figure 2–16. Sync Stripper clamping can only be used with standard RS170 and CCIR video signals.

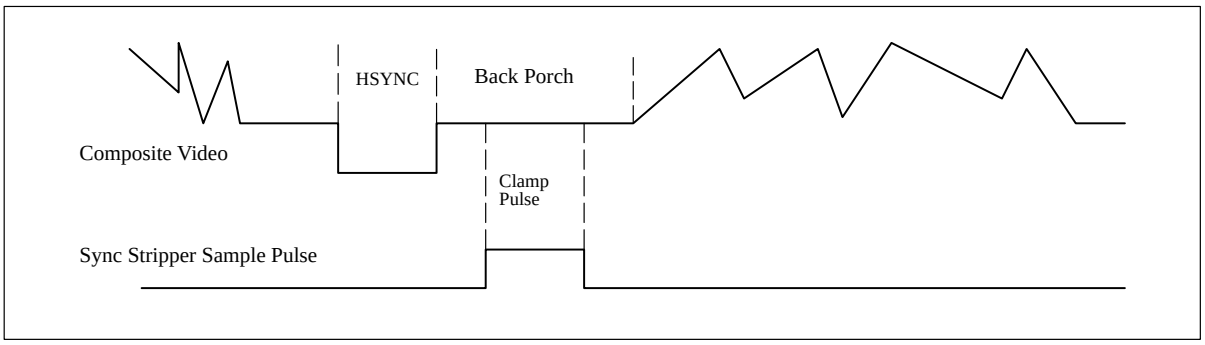


Figure 2–16. DC Restore with Sync Stripper Sample Pulse

In Figure 2–16 the clamp circuit samples the back porch voltage level of the AC-coupled video signal for every line, and adjusts (clamps) the back porch of the video signals to match a programmable clamp voltage in the Clamp Voltage DAC. The ADC uses this voltage level as the internal reference for black. The optimum setting for the clamp voltage is equal to the negative reference voltage (NREF) of the ADC (plus a small correction factor).

2.5.4.2 Programmable Clamp Pulse

A programmable clamp pulse is available, and gives better response than the Sync Stripper clamp. The programmable clamp pulse is referenced to horizontal sync input or PTG sync, and can be positioned by programming the beginning and end counts. The counters are clocked by the internal crystal clock in the PLL circuit, and are indepen-

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dent from the sample frequency or video frequency. The programmable clamp pulse gives the same affect of adjusting (clamping) the back porch of the video inputs to the voltage programmed in the Clamp Voltage DAC.

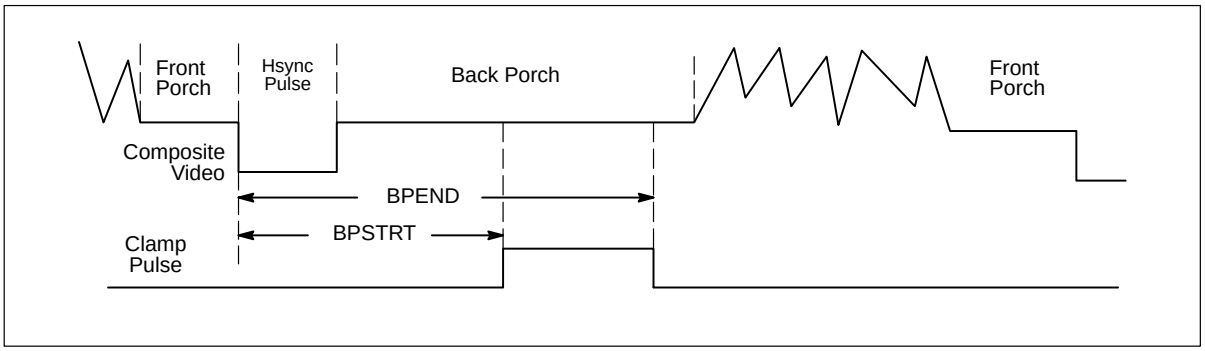


Figure 2–17. DC Restore with Programmable Clamp Pulse

In Figure 2–17 the falling edge (start) of HSYNC starts the programmable clamping counters. When the back porch start counter BPSTRT reaches zero, the back porch clamping pulse begins. When the back porch end counter BPEND reaches zero the pulse ends. The sampled voltage level is adjusted to match the voltage level of the Clamp Voltage DAC.

2.5.5 Programmable Clamp Voltage DAC

The PCVision*plus* DC restore circuit uses a DAC (digital to analog converter) to set the back porch clamp voltage used to establish the sampling black-level. The voltage of this DAC should be set to match the negative reference voltage of the ADC. The voltage swing of the DAC is 0 to 2.5 Volts. The default DAC setting for 1.75 Volts is 0x1666 (5734 decimal).

Desired Clamp Level = 1.75 V

DAC value = (desired clamp voltage level) / (2.5 V / 8192)

= 1.75/0.000305 = 5734 = 0x1666

2.5.6 Analog to Digital Converter

The PCVision*plus* uses a 53 MHz 12-bit flash ADC (Analog to Digital Converter). The ADC has programmable positive (PREF) and negative (NREF) voltage reference inputs that set the sampling window voltage range of the ADC. The ADC outputs 12-bit unsigned binary values from 0x0 to 0xFFF based on: the sampled analog input signal level, the ADC sampling window, and by the Clamping voltage level. The pixel clock used by the ADC comes from one of three sources: the PLL clock (PLL mode), the frequency synthesizer (XTAL mode), or the externally input variable scan clock (Vscan mode).

2.5.7 Programmable References

The positive and negative ADC references are programmable using independent 13-bit DACs. The voltage swing of the positive and negative reference DACs is 0 to +3.3 Volts, allowing voltage increments of 3.3/8192 = 0.4 mV. The

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optimal positive reference (PREF) setting is 3.25 Volts (register value 0xFC1). The optimal negative reference (NREF) setting is 1.75 Volt (register value 0x87C).

The absolute minimum difference between any PREF and NREF combination is 0.4 Volt. The absolute maximum difference between any PREF and NREF combination is 1.6 Volts. For best performance and accuracy, the difference between NREF and PREF should be 1.5 Volts.

Many “RS170 compatible” cameras output higher video levels, sometimes 800 mV or higher. In this situation, the video signal after the 2.1 gain is larger than 1.5 V and saturates the ADC, which in turn does not use the full dynamic range available (0 to 4096). You should calibrate the PREF and NREF for the dynamic range of the video signal you are using, without exceeding the 0.4 to 1.6 Volt range of the ADC.

All reference DACs of the PCVision*plus* are programmed through a serial interface. Refer to the DAC registers and programming information in Chapter 4.

2.5.8 Input LUT

The Input LUT is a 64K-by-16 (16-bit in 16-bit out) SRAM. The Input LUT can be programmed to perform any point transformation function.

The bit order is reversed at the LUT input. ADC output bit 11 is connnected to LUT input bit 0. The Oversample Enable bit (OVRSM) controls the input LUT configuration, which has a great affect on how the LUT is programmed. The Input Data Format bit (INMODE) controls how data is read from the LUT output, and packed and stored in the image memory. The LUT must compensate for the data input format, bit ordering, and both OVRSM and INMODE values.

In normal mode, the input LUT has 16 pages that are statically selected by register values under program control. The LUT does not provide a dynamic page mode (page switching under pixel data control). In oversample mode the LUT does not use the static page select.

With oversample disabled (OVRSM=0), the Input LUT provides sixteen pages for 16-bit input addressing, 12 bits from the ADC and four page select bits, as shown in Figure 2–18. You can load up to 16 different 12-bit data transforms and use the page select bits ILUTSADR (input LUT static address) to change transforms without reloading.

In 12-bit input mode (INMODE=1) all 16 LUT output bits are read and stored as a WORD in the image buffer memory, as shown in Figure 2–18. The LUT can be programmed for any point transformation, normalization, or data shift. The user must be aware that the Bus Master Controller pad, zoom, decimate and byte shift modes assume valid pixel data is positioned on bits 11 through 0. Bits 15 through 12 are usually treated as “don’t care” values, but may be useful as tag values.

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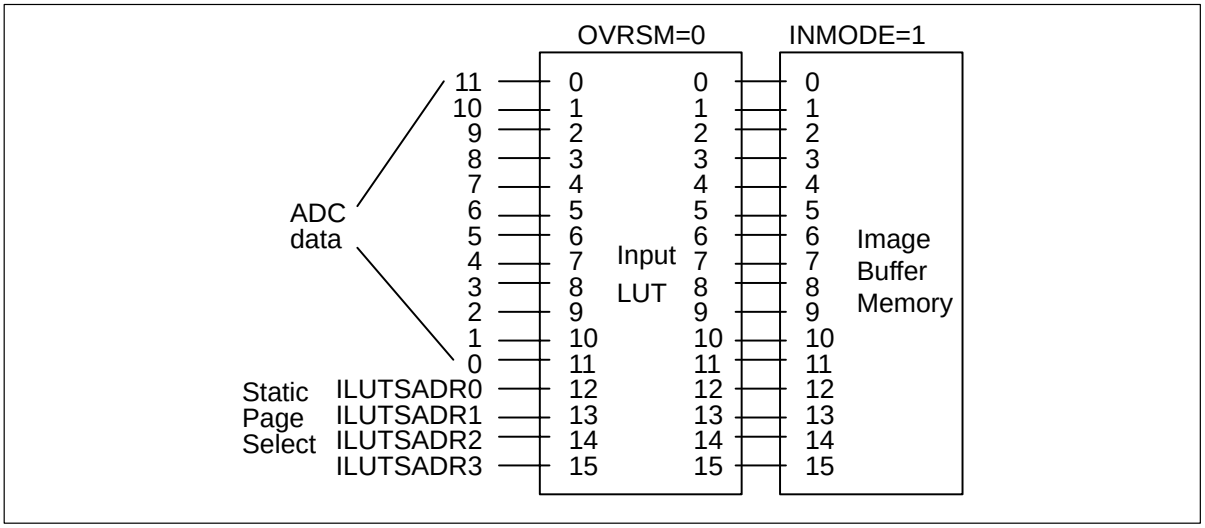


Figure 2–18. Input LUT 12-bit Mode

With oversample enabled (OVRSM=1), the Input LUT provides one page for 16-bit input addressing, and there are no page select bits available, as shown in Figure 2–19. You can load only one transform. If you are not oversampling the pixel data, program the LUT to ignore the high byte input (delayed pixel) by repeating the same data pattern. If you are oversampling, program the LUT to average the values input on the two address bytes.

In 8-bit input mode (INMODE=0) LUT output bits 11 through 4 are stored as a BYTE in the image buffer memory, as shown in Figure 2–19. Bits 15 through 12 are discarded, and bits 3 through 0 are discarded.

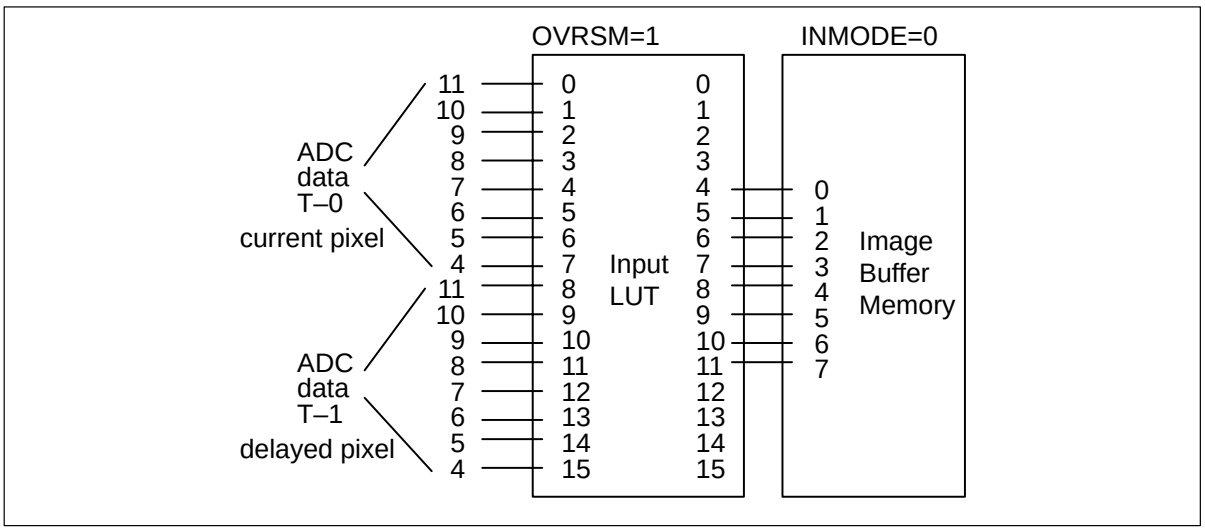


Figure 2–19. Input LUT Oversample Mode

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2.6 TIMING AND SYNCHRONIZATION

The PCVision*plus* has three major timing modes: PLL (Phase-Locked Loop), Internal timing (XTAL), or Variable Scan (Vscan). There are two PLL modes; stripping sync from composite video, or locking to separate horizontal and vertical sync inputs.

2.6.1 Sync Stripper PLL Mode

The first PLL mode uses the sync stripper to separate sync information from the video input. The PLL and PWG use the stripped sync to generated clocking and timing. The PLL is programmed based on the timing requirements of the incoming video. The PLL receives the stripped horizontal sync and outputs a clock PLLCLK, which is line-locked to the incoming video and is used to digitize video and generate frame timing. The PTG is not used in PLL modes. The PWG is programmed to frame the video.

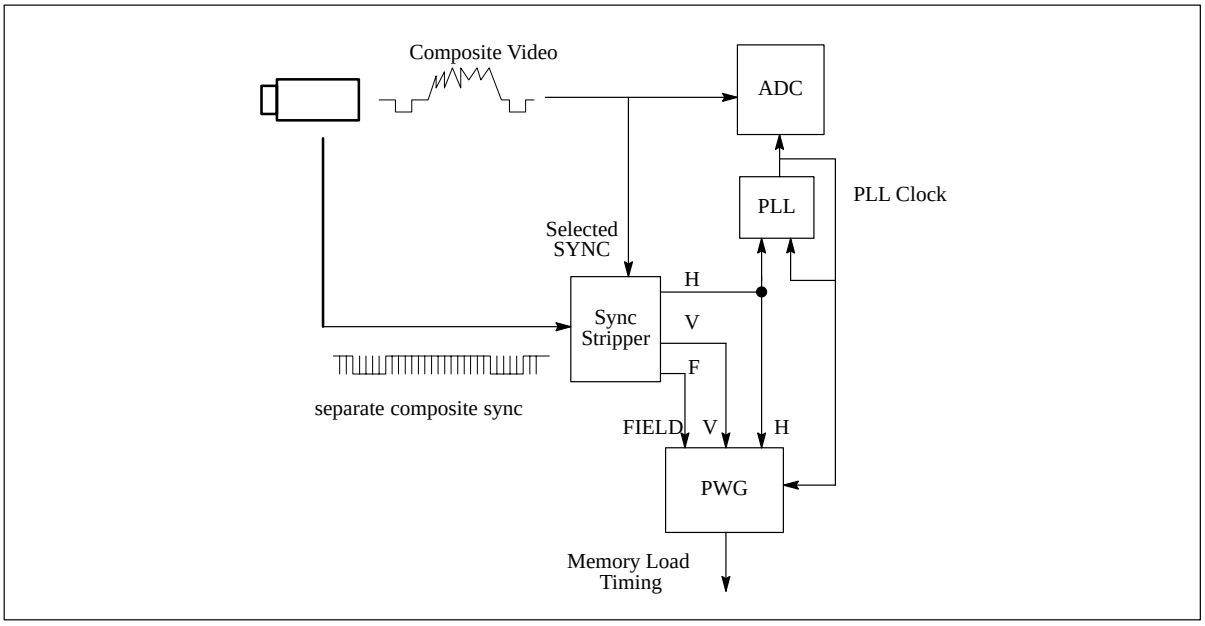


Figure 2–20. PLL Mode with Composite Sync

As shown in Figure 2–20, the PLL compares the stripped horizontal sync to the internal feedback, and generates the PLL clock. The ADC uses the PLL clock to digitize the video input. Program the PWG for the desired video frame; full frame or AOI. The PWG uses the PLL clock and the stripped horizontal, vertical, and field signals to frame the video output.

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2.6.2 Separate Sync PLL mode

The PCVision*plus* also supports PLL mode with separate horizontal and vertical sync inputs from cameras CAM0 or CAM1. The sync stripper is not used and the separate incoming timing signals drive the PLL and PWG directly as shown in Figure 2–21. Separate sync inputs must be referenced to ground. Analog or negative-going sync inputs are not supported in this mode. The polarity of the sync inputs is programmable, allowing positive or negative polarity input (active-high or active-low signals).

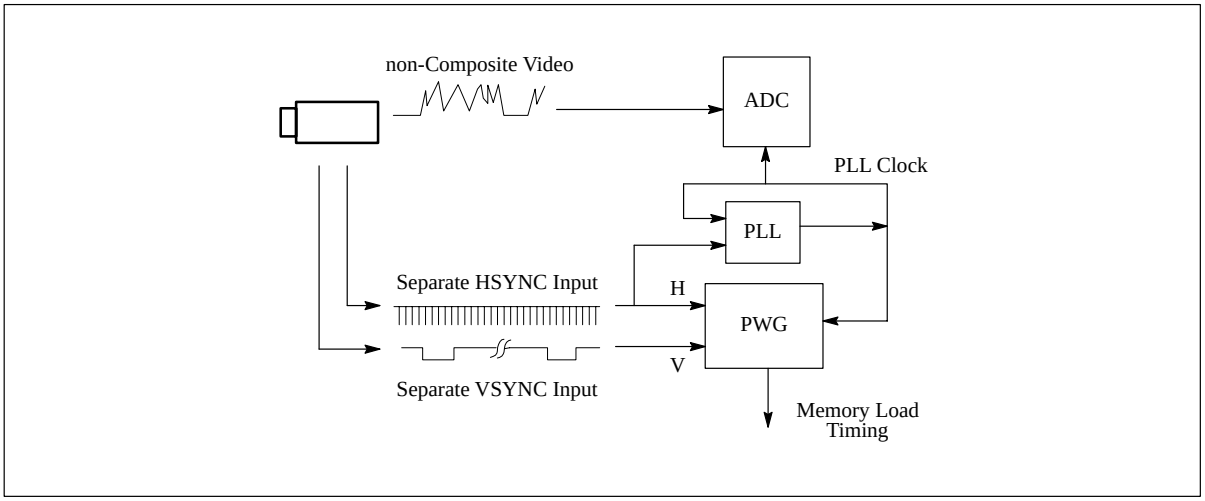


Figure 2–21. PLL Mode with Separate Syncs

As shown in Figure 2–21, the PLL compares the separate horizontal sync input to internal feedback, and generates the PLL clock. The ADC uses the PLL clock to digitize the video input. Program the PWG for the desired video frame; full frame or AOI. The PWG uses the PLL clock and the horizontal and vertical input signals to frame the video output.

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2.6.3 Internal Clock Mode (XTAL Mode)

In internal clock (XTAL) mode, a frequency synthesizer and the PTG are programmed to generate the desired pixel clock and time base signals. The PTG generates separate Horizontal and Vertical sync signals that match the desired video format. These signals are sent to the camera for gen-locking and to the PWG to frame the video. The sync outputs are available on CAM0 and CAM1. The PTG generates timing based on the clock output of the programmable clock synthesizer. The frequency synthesizer can be programmed to generate any clock frequency up to 53 MHz. The clock resolution is less than one nanosecond. This clock is also the sample clock of the ADC. In XTAL mode, the PTG can be programmed to standard and non-standard camera timing.

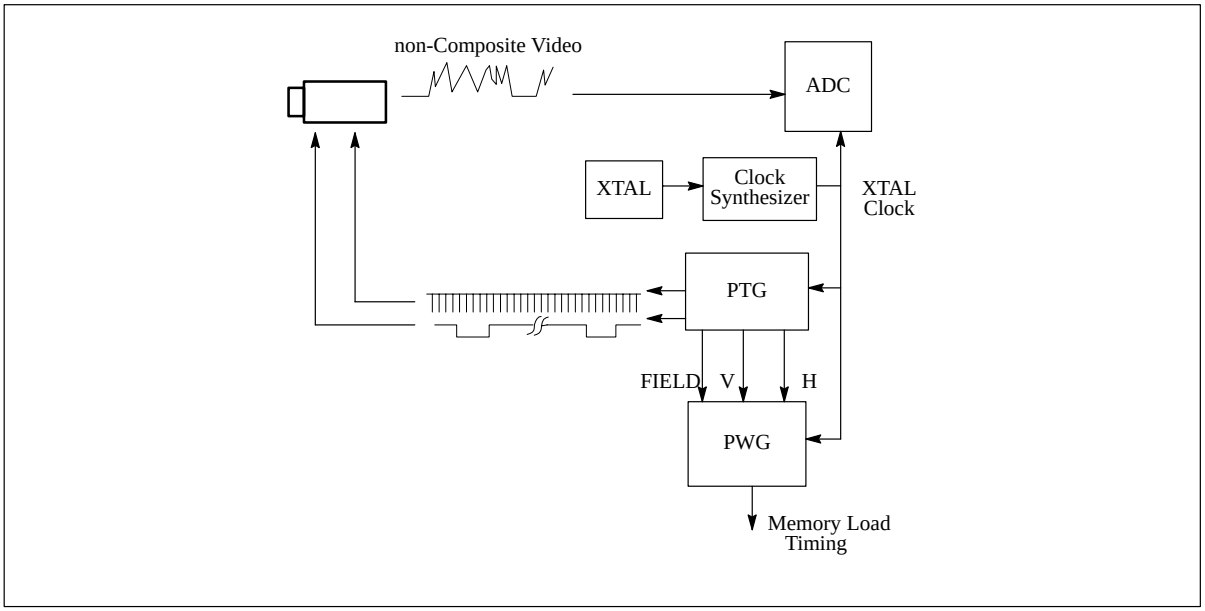


Figure 2–22. Internal Timing Mode (XTAL Mode)

Figure 2–22 illustrates internal timing mode. Select the internal clock (XTAL) mode, and program the PTG to match the video input format. The PTG uses the XTAL clock to generate the horizontal and vertical sync outputs. The vertical sync is always created, but output can be disabled by the VSYNCEN bit. The ADC uses the XTAL clock to digitize the video input. Program the PWG for the desired video frame; full frame or AOI. The PWG uses the internal clock and the PTG horizontal, vertical, and field signals to frame the video output. If the camera returns the sync information on the video signal, auto-clamping can be used. If the camera does not return sync information on the video, use the programmable clamp.

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2.6.4 Variable Scan Mode (VSCAN)

In Variable Scan Mode, the camera must supply line enable (LEN), frame enable (FEN), and Pixel Clock (CLK). These inputs drive the programmable window generator (PWG) and the ADC directly. The PTG and PLL are bypassed in variable scan mode. The PCVision*plus* supports area-scan format only, line-scan formats are not supported. The timing inputs used in variable scan mode are single-ended TTL only. The incoming signals must be referenced to ground. Negative-going analog signals are not supported for variable scan. Polarity of the incoming timing and clock signals is software programmable. If the video is interlaced and sync information is available on the video signal (composite sync on video) the sync stripper can be used to extract the field information.

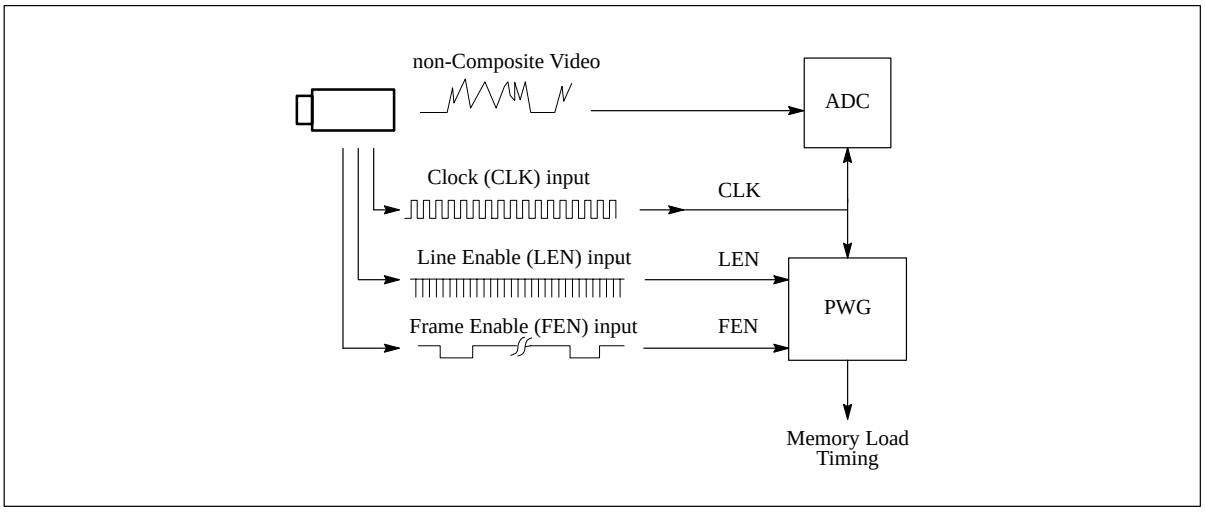


Figure 2–23. Variable Scan Mode

Figure 2–23 illustrates variable scan mode. The ADC uses the variable scan clock input (CLK) to digitize the video input. Program the PWG for the desired video frame. The PWG uses the variable scan inputs CLK, FEN, and LEN to frame the video output.

The Clock can be input on the CLKIN pins or on the FRESET pins at the video connectors. This additional flexibility supports some of the camera adapter cables developed for the earlier PCVision frame grabber.

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2.7 TIMING CONTROL

Figure 2–24 is a block diagram of the timing control on the PCVision*plus*. Timing control is accomplished by the following circuits:

- Variable Scan Input
- Sync Stripper
- Phase-Locked Loop
- Programmable Timing Generator (PTG)
- Programmable Window Generator (PWG)

2.7.1 Variable Scan Inputs

Variable scan refers to any camera format that does not follow any of the standard broadcasting formats (RS170, CCIR, NTSC, PAL). The standard input formats have pre-defined timing requirements which must be followed; making interface timing predictable. To interface to non-standard video, the interface circuitry must be capable of matching the non-standard timing input. The PTG (programmable timing generator), PWG (programmable window generator), and PLL (phase-locked loop) circuitry are fully programmable allowing acceptance of non-standard video formats.

The PCVision*plus* supports timing signal inputs: LEN (line enable), FEN (frame enable), CLK (variable scan clock) from CAM0 or CAM1. Only positive digital signals are supported in variable scan mode. Negative signals and analog timing are not supported. The clock can be input on the CLKIN or FRESET pins of the video connectors.

PCVision*plus* requires LEN, FEN, and Pixel Clock all be input in variable scan mode (Vscan mode). Line scan cameras are not supported. In Variable Scan mode the PLL, XTAL and PTG timing sources are disabled and the variable scan timing is input directly to the PWG for framing the output. Line scan cameras are not supported by the PCVision*plus* variable scan inputs. The following describes the required variable scan input timing signals:

CLK, Pixel Clock Input: single-ended TTL, programmable polarity, Frequency 10 KHz to 53 MHz.

LEN, Line Enable Input: single-ended TTL, programmable polarity. Minimum de-asserted or inactive (reset) pulse duration is one CLK period.

FEN, Frame Enable Input: single-ended TTL, programmable polarity. Minimum de-asserted or inactive (reset) pulse duration is one CLK period.

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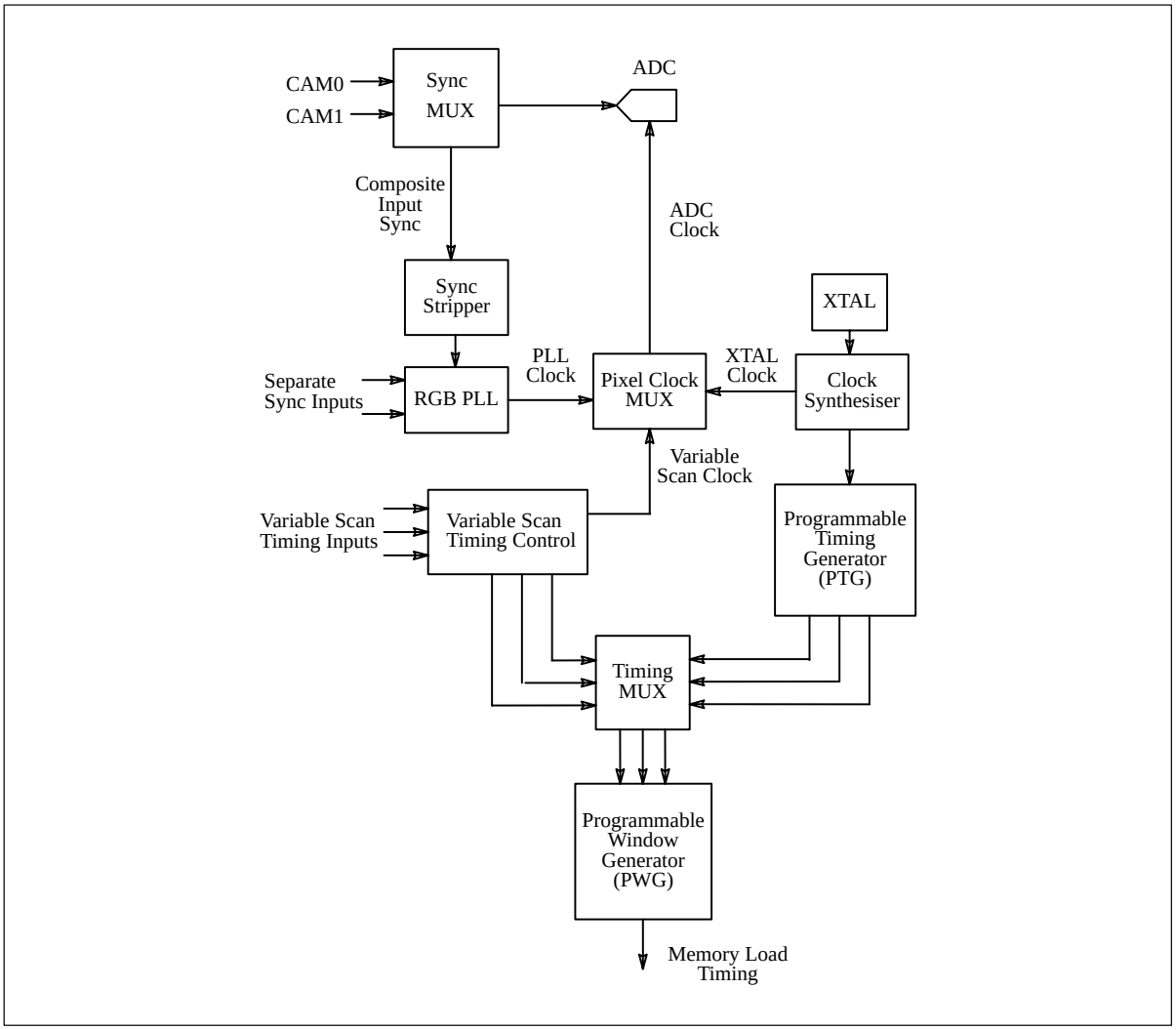


Figure 2–24. Timing Control

2.7.2 Sync Stripper

The sync stripper separates synchronization information from a composite video input on the video signal (CAM0 or CAM1). The horizontal sync (Hsync) output of the sync stripper is used in the PLL where it is compared to an internal PLL Hsync feedback. Phase differences in the PLL clock can then be measured and adjusted to maintain a line locked pixel clock. The stripper also removes Field and Vertical timing information and generates a back porch sample pulse used to DC restore the video input. The sync stripper outputs horizontal, vertical, and field signals. The

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programmable timing generator (PTG) and programmable window generator (PWG) use the sync stripper output for locking to and framing incoming video.

The sync stripper can be bypassed by selecting separate sync as the input to the PLL. In bypass mode, sync signals are input separately from CAM0 or CAM1 and are used by the programmable timing generator (PTG) and programmable window generator (PWG) for locking to and framing incoming video.

The sync stripper features a programmable horizontal line rate, from 15 KHz to 66.5 KHz. This provides support for non-standard horizontal line rates in PLL mode, such as the JAI M30 camera with a 32 KHz line rate. The line rate is controlled by a 13-bit DAC. The horizontal line rate is inversely proportional to the DAC voltage, as shown in Figure 2–25. The formula for calculating the Sync Stripper DAC value is:

NB = (1.7 – (line rate in KHz) / 45 KHz)) / 0.000169

Where NB is the programmed 13-bit DAC value.

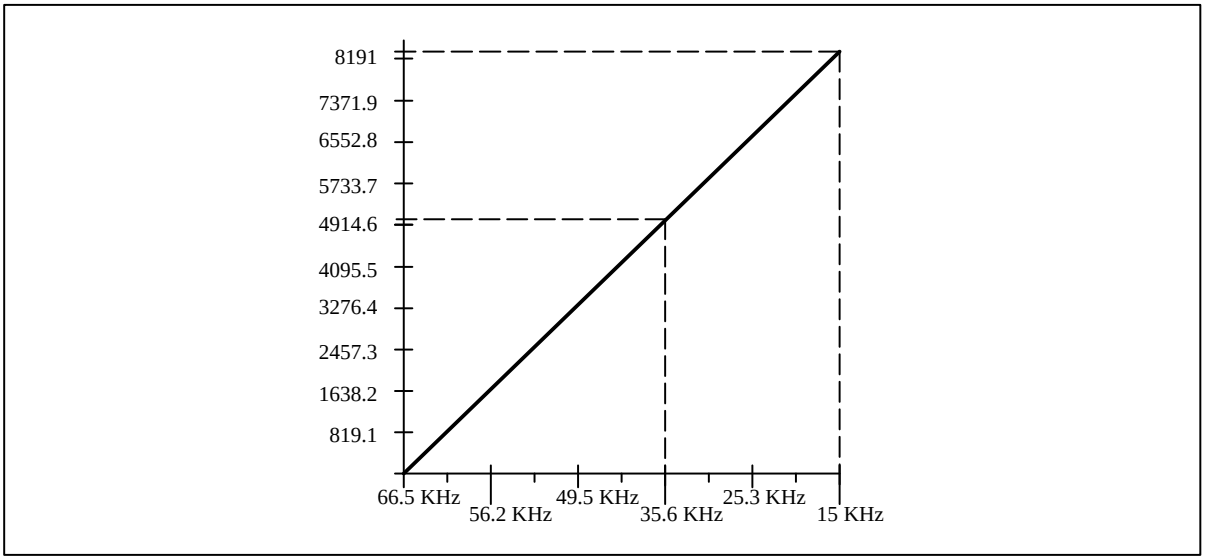


Figure 2–25. Sync Stripper Line Rate

2.7.3 Phase-Locked Loop

The Phase-Locked Loop (PLL) performs both the line locking function of the standard PLL mode and the frequency synthesis function of internal clock (XTAL) mode. The mode of operation affects the PLL programming. The PLL is programmed through a serial interface, described in the Chapter 4. Figure 2–26 illustrates the PLL/XTAL clock generator.

For PLL operation, the internal PLL feedback path selects the PLL clock output signal (selected by CLKSEL). The feedback path is programmed to divide the PLL clock to equal the incoming horizontal line frequency. The reference divider is 1 in PLL mode. The feedback path is input to the phase detector and compared to the selected PLL Hsync

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source (either stripped Hsync or separate Hsync) for phase alignment. Any detected phase difference generates an error voltage which modifies the VCO clock to correct for the difference. The VCO clock is passed to the output post scalar and the load counter to divide the high frequency VCO clock down to the desired PLL clock rate.

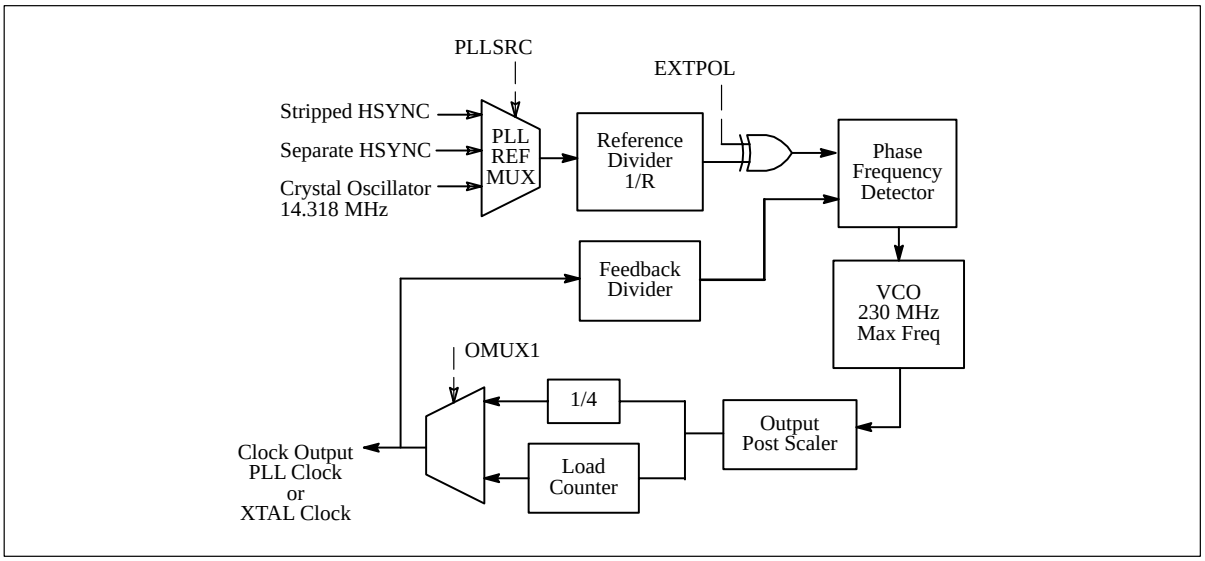


Figure 2–26. PLL and Clock Synthesizer

The VCO is optimized to run at a maximum frequency of 230 MHz. When programming the Output Post Scalar, Load Counter, and the feedback path, the goal is to achieve the highest VCO frequency without going over 230 MHz. In PLL mode, the same Hsync source input to the PLL also drives the PWG. The example that follows gives the details of how to program the PLL registers to achieve a desired clock rate.

For XTAL mode operation, the 14.318 MHz reference oscillator is selected, and the feedback path is also driven with the PLL clock output. The incoming reference frequency is divided by in the reference divider, and input to the phase detector. The feedback path is programmed to divide the PLL output clock down to match the divided reference oscillator frequency. The phase detector then checks the two signals for phase alignment and adjusts the VCO as needed. The VCO output is passed to the Output Post Scalar and the Load Counter which divide down the VCO clock to the required pixel clock rate. When programming the VCO, feedback path, and output path; the goal is to achieve maximum VCO operating frequency of 230 MHz. The PTG uses the XTAL clock to generate the Hsync and Vsync driven to the camera and to the PWG for video framing. The ADC uses this same XTAL clock for video sampling.

2.7.4 Programmable Time Base Generator (PTG)

The PTG is used in internal timebase (XTAL) mode to generate horizontal and vertical sync for gen-locking cameras. The PTG uses a clock derived from a reference oscillator and the PCVision*plus* frequency synthesizer to generate horizontal and vertical sync and Vertical reset (VRESET) to output to a camera. The PTG horizontal and vertical syncs are output to CAM0 and CAM1.

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The PTG must be programmed to match the camera in use. The PTG has a vertical and horizontal counter and several registers to determine the size of the sync pulses in pixel clocks or lines.

The horizontal sync is derived from two register settings HTOTAL and HESYNC. The HTOTAL value determines the number of pixel clocks in half of a horizontal sync line (up to 1024 clocks). The HTOTAL value is loaded into a counter which counts off the number of pixel clocks programmed. At the end of the count, the PTG outputs a low going Hsync pulse (polarity output to camera is programmable) and restarts the count. The sync pulse stays low the number of pixel clocks programmed in HESYNC (up to 256 clocks). Internal to the PTG, Hsync is formulated from HTOTAL and HESYNC as follows:

Total Hsync Time = HTOTAL x 2

and

Total Hsync low time = HESYNC

Because Hsync is derived from two times the horizontal register setting, the Hsync time is always on even pixel clock boundaries (increasing HTOTAL by 1 actually increases Hsync by two pixel clocks).

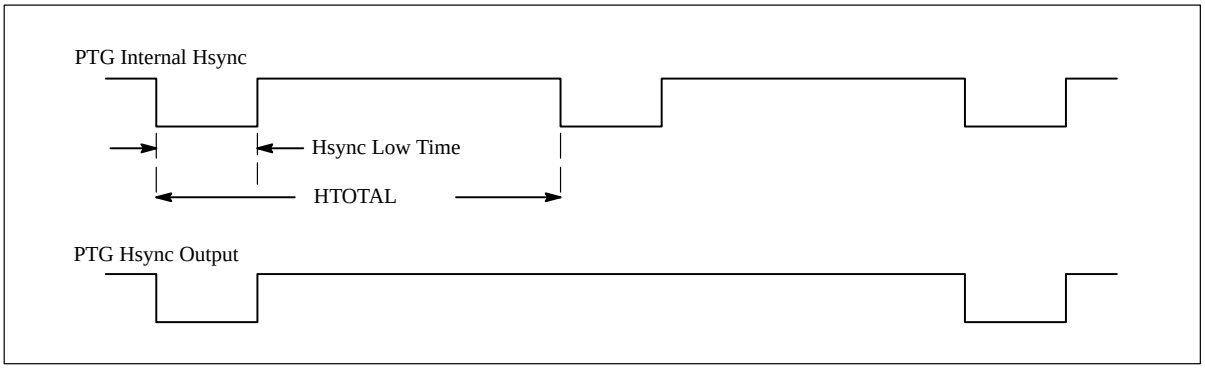


Figure 2–27. Timing Generator Horizontal Sync Output

In Figure 2–27, HESYNC determines when the PTG Horizontal Sync goes high, based on the horizontal counter. The PTG Horizontal Sync output is twice HTOTAL. This means the actual pixel resolution of sync output is two pixel clocks.

The maximum Hsync low time is 256 pixels and maximum Hsync high time is (2048 – Hsync low) pixels.

The PTG vertical sync is generated in a similar fashion by two values that determine the total number of half lines in a field/frame time and the number of half lines in the Vsync low period. VTOTAL sets the number of half lines and VSEND sets the Vsync low time. The PTG can generate both interlaced and non-interlaced frame timing based on the number of half lines programmed in the VTOTAL register. If VTOTAL is ODD (lsb=1) then frame timing is interlaced, if EVEN (lsb=0) then frame timing is non-interlaced.

The Maximum settings of the programmable timing generator are:

PTG max = 2K horizontal x 2K vertical, (2048 by 2048)

The active time for the programmable timing generator is:

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PTG active = (2K – Hsync low) x (2K – Vsync low)

The maximum Vsync low time is 16 lines and maximum Vsync high time is (1024 – Vsync low) lines.

The C/Hsync line is always driven in XTAL mode. Make sure there is nothing driving the HSYNC inputs on CAM0 or CAM1 prior to enabling XTAL mode (TIMEMD bits). Vsync can be programmed to not drive out in XTAL mode, which is useful in frame reset mode where some cameras require no Vsync input.

2.7.5 Programmable Window Generator (PWG)

The PWG generates horizontal and vertical blanking information used to load the load the image memory. The PWG consists of two counters and four values programmed to establish the desired frame input timing. The PWG can crop the incoming video frame in both the vertical and horizontal direction, allowing smaller than full frame areas of interest (AOI) to be captured.

The PWG must be driven by sync and pixel clock from one of the three time base sources: PLL, PTG, or Vscan. In PLL mode, either the sync stripper or separate sync inputs provide the necessary timing. In XTAL mode, the oscillator, frequency synthesizer and PTG provide the timing. In Vscan mode, the variable scan timing inputs LEN, FEN, and CLK provide the necessary timing. The timing source for the PWG is automatically selected based on the TIMEMD bits. Field information is also required by the PWG for interlaced video formats.

The PWG uses the incoming timing to start the internal horizontal and vertical counters. The values HOFF, HACT, VOFF, and VACT define the size of the Active video window loaded into memory. The horizontal active region must be programmed on even 8-pixel boundaries. The horizontal active window can be shifted on single pixel boundaries, but the 8-pixel size restriction must be maintained. Adding 1 pixel to the HACT requires adding 1 pixel to HOFF to maintain the 8 pixel even value. The maximum setting for HOFF and VOFF is 2048.

The PWG uses the selected vertical and horizontal timing signals to start its internal counters. Two registers determine the number of pixels loaded into the FIFO per line. The HACT value defines the pixel clock total per line (including blanking). When the programmed edge of the incoming Hsync triggers, the horizontal counter begins to count until the value programmed in HACT is reached at which time the counter stops and waits for the next Hsync input. The value programmed in HOFF determines the length of the horizontal offset period (no pixel load region) with respect to the horizontal count. When the value in HOFF is reached the memory begins loading with valid pixel data until the counter reaches the value programmed in HACT, at which time memory loading stops.

2.7.5.1 PWG in PLL Mode

In PLL mode, stripped Hsync is used to activate the PWG horizontal and vertical counters. Figures 2–28 and 2–29 show the timing relationship of the incoming video and memory loading.

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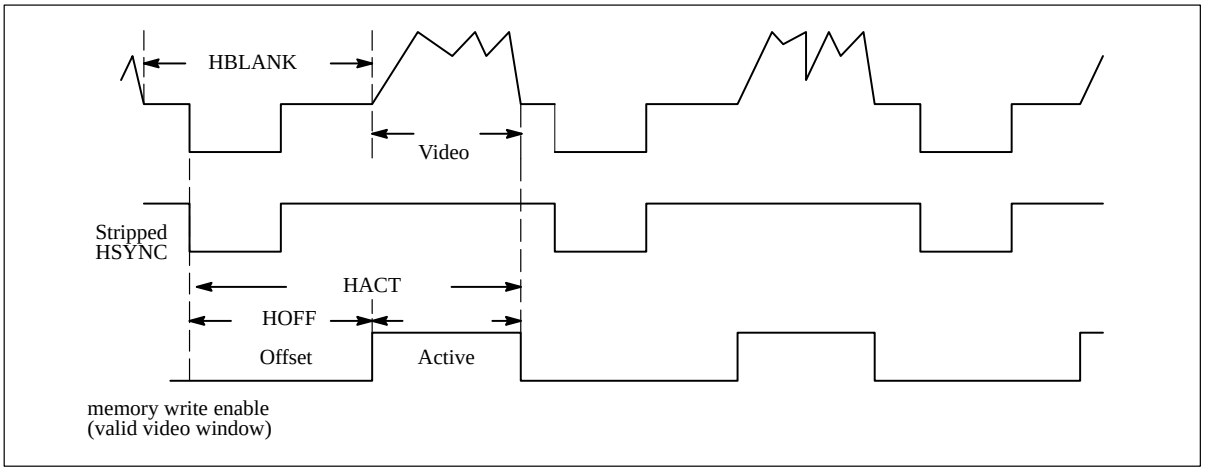


Figure 2–28. PWG Horizontal Window Timing

In Figure 2–28, HACT and HOFF are programmed to load the entire video region. The falling edge of stripped Hsync starts the horizontal counter. HOFF is programmed to the desired horizontal offset. This is a no-load region. HACT is programmed to the total horizontal line time. At the end of the HACT count (end of active period) the FIFO load is disabled and the horizontal counter resets and waits for the next stripped Hsync.

Figure 2–29 illustrates HACT and HOFF programmed to crop the incoming video in the horizontal direction, creating and AOI (PLL mode is illustrated).

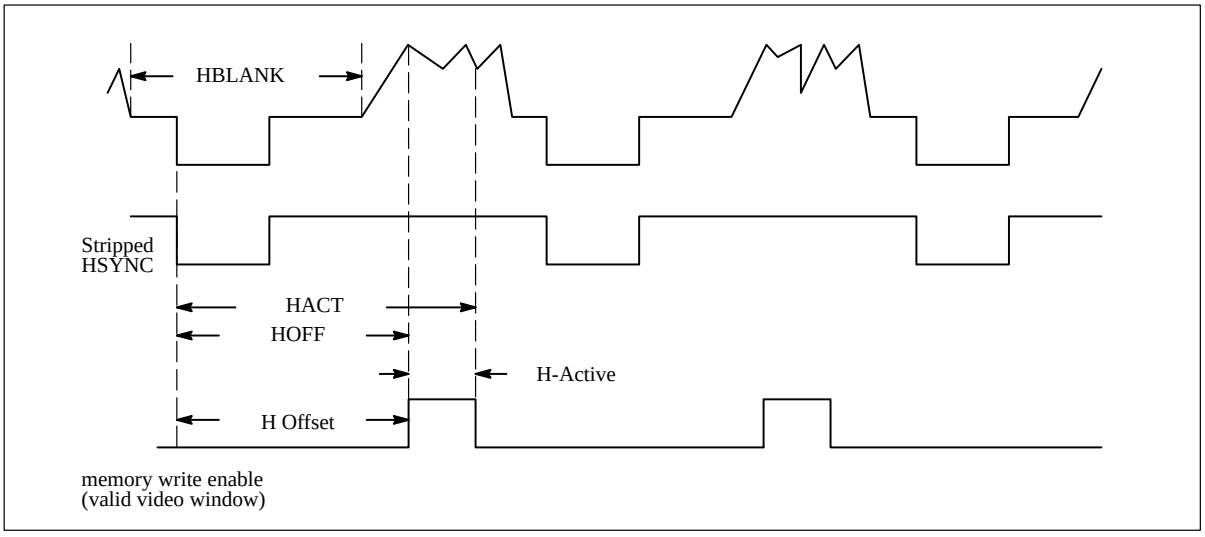


Figure 2–29. PWG Horizontal Timing with Cropping

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In Figure 2–29, HACT and HOFF are programmed to crop the active video region. HOFF is increased to contain part of the active video. HACT is decreased, shortening the active time and the memory load region. The region of active video that falls within the H-Active time is loaded into memory. The remainder of the video is cropped. HACT can be programmed to acquire all of the remaining video, from the end of HOFF to the end of the horizontal line; or a smaller part of the video, as pictured in Figure 2–29.

2.7.5.2 PWG in XTAL Mode

In internal timing or XTAL mode, the PTG Hsync is driven to the camera for gen-locking and to the PWG to activate the horizontal counters. When driving sync to a camera, the timing relationship of HOFF, HACT, HBLANK, and the active video region changes as shown in Figure 2–30, and must be accommodated by adjusting the appropriate register settings.

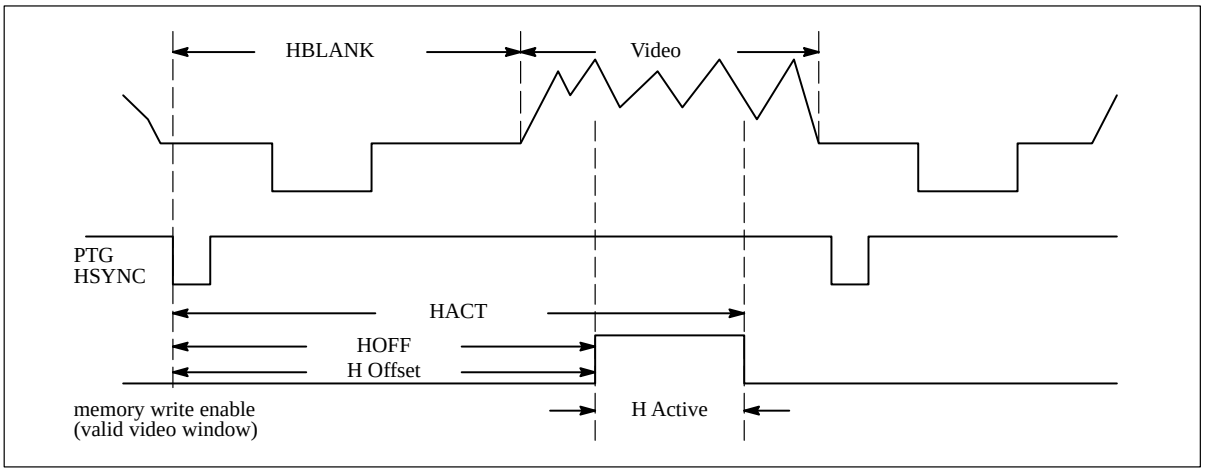


Figure 2–30. PWG Horizontal Timing, Internal Timing Mode

In Figure 2–30, HACT and HOFF are programmed to crop the active video region. The HSYNC driven to the camera has a different timing relationship to the video, requiring an adjustment to HOFF and HACT. The PTG Hsync aligns with the start of HBLANK, but in Figure 2–29 the stripped Hsync aligned with the Hsync inside the camera Hblank. The PTG Hsync starts the horizontal counter earlier, requiring HOFF to be increased. HACT is also adjusted to compensate for timing differences. The region of active video that falls within the HACT time is loaded into the memory.

2.7.5.3 PWG in Variable Scan Mode

In variable scan mode, the LEN input activates the PWG horizontal counters. The timing relationship of HOFF, HACT, HBLANK, and the active video region change as shown in Figure 2–31, and must be accommodated by adjusting the appropriate register settings.

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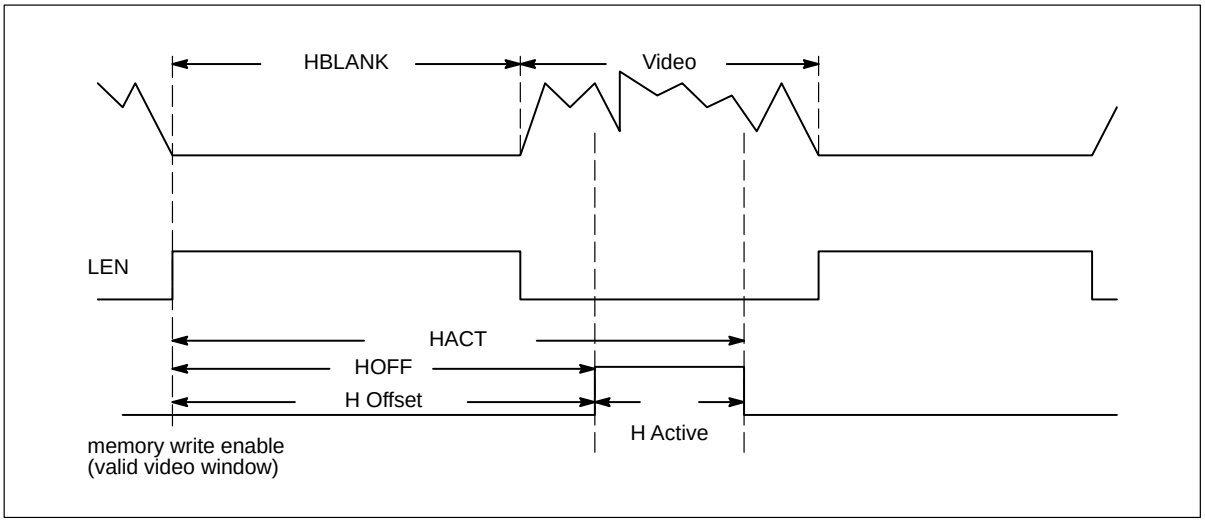


Figure 2–31. PWG Horizontal Timing, Variable Scan Mode

In Figure 2–31, HACT and HOFF are programmed to crop the active video region. The selected edge of LEN starts the horizontal counter; the positive or rising edge is shown in Figure 2–31. LEN starts the horizontal counter earlier, requiring HOFF to be increased (notice the lack of front porch and sync pulse). HACT is also adjusted to compensate for variable scan timing. The region of active video that falls within the HACT time is loaded into the memory. The remainder of the video is cropped.

2.7.5.4 PWG Vertical Timing

Two values determine the number of lines loaded into the FIFO per frame. VACT holds the number of lines per frame (including blanking). The selected edge of the incoming Vsync or FEN starts the vertical counter. The counter stops when it reaches the value programmed in VACT, and waits for the next Vsync or FEN input. The value programmed in VOFF determines the length of the vertical offset period (no line load region) with respect to the vertical count. When the value in the VOFF register is reached the memory begins loading with active lines of pixel data until the counter reaches the value programmed in VACT at which time loading stops. The two registers used together allow cropping the video in the vertical direction.

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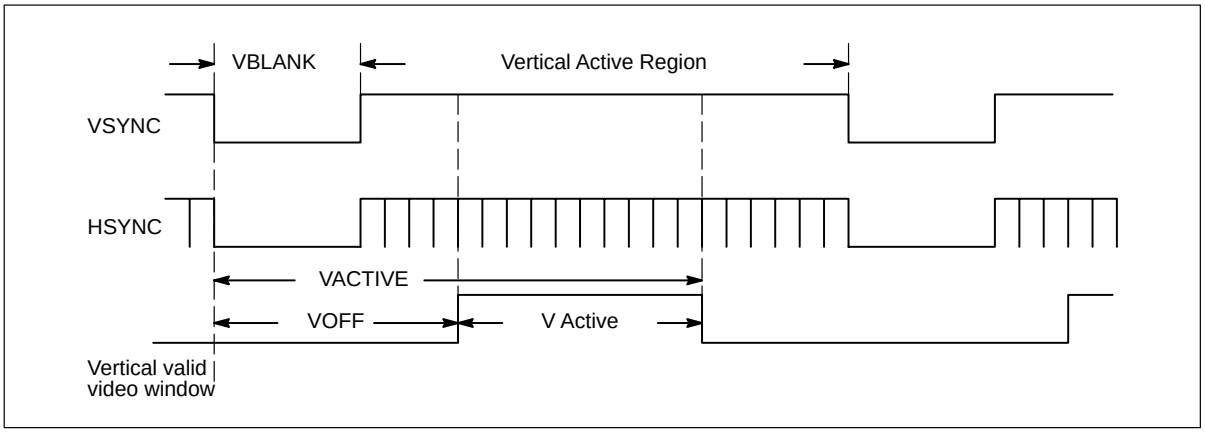


Figure 2–32. PWG Vertical Window Timing

In Figure 2–32, VACT and VOFF are programmed to crop the active video region. The PTG Vsync, stripped Vsync, or FEN input starts the vertical counter, depending on the acquisition and timing mode selection. The Vertical Active region is determined by VOFF and VACT. The region of active lines that fall within the VACT time are loaded into the memory. The remainder of the video is cropped, creating a vertical AOI.

2.7.6 Field Shift Mode

Field shift mode changes the alignment of the first line of video with respect to vertical blank. Field shift mode allows the PWG to crop the half lines in the beginning and end of the even and odd fields of interlaced video.

When the PWG is in interlaced mode, every setting in the vertical values VOFF and VACT affect each field equally. This means if the first line of a field is a half line. To crop this, the VOFF value is increased by one; but normally this also crops the first line of the odd field. Instead of cropping only one line, two lines get cropped; the first line of the even field (which is the 1/2 line targeted to crop) and the first line of the odd field which is valid data, but is lost due to the nature of the interlaced video and how the PWG does cropping.

The same thing happens on the last line of the field (in this case the odd field has the half line and the even field has a full line of video). Programming the VACT to chop the last line in the odd field also crops the last line in the even field. To crop the two half lines in an image, four lines get cropped.

For example, using 576 line CCIR format, two of those lines are half lines. Programming the PWG to crop the first half line, the result is 574 lines. If the PWG is programmed to also crop the last half line, the result becomes 572.

The FLDSHIFT bit changes the alignment of the first line of each field so the first 1/2 line of one field corresponds to a non-video line on the second field. Now programming the PWG to crop the half line, it cuts a non-video line from the second fields blank region. Therefore the half lines from the top and bottom of the video can be cropped without cutting an extra line of real video from the opposite field.

Field Shift mode changes which line is the first line in a frame (in non-field shift mode, the first line of the even field is the first line in the frame and in field shift mode, the first line of video is from the odd field). The field polarity is

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automatically changed to compensate for the field shift. The mother board acquires the image in the correct field order.

2.7.7 External Trigger and Strobe

The PCVision*plus* can acquire images based on an external event (external trigger input signal) and it can output a synchronous strobe signal coincident with the trigger cycle. The PCVision*plus* also supports a synchronous strobe and asynchronous frame reset outputs.

The external trigger input is a programmable edge trigger input with minimum pulse width of 250 ns. The selected edge of an external trigger input causes the frame memory to acquire a single frame at the next vertical blank. A software trigger is also provided allowing the user to simulate a trigger cycle through software. The trigger input can reset the PTG and PWG to synchronize them to the incoming video. A strobe output occurs at the next vertical blank (in slow mode) or the strobe can be programmed to occur coincident with the trigger input (in fast mode). An external frame reset pulse based on an external trigger input can be programmed and driven to a camera.

The INCON1 register controls triggered acquisition. The TRIGEN bit enables trigger mode. The TRGISEL bits select external input or software trigger. The TRIGPOL bit selects the rising or falling edge of the incoming external trigger pulse. The correct trigger event (software or external signal) causes the next frame of video to be acquired. The TRIGCYC and TRIGEN bits can be monitored to see the status of the trigger acquire cycle. A strobe pulse is output synchronous to the acquired frame on three pins of the video connector. The polarity of the output strobe pulse is programmable. The PCVision*plus* has several different modes of trigger and strobe operation: Trigger on Frame-Slow Strobe, Trigger on Frame-Fast Strobe, and Frame Reset Mode. The strobe mode is selected by the STRBMD bits.

2.7.7.1 Using Strobe Lights

When using strobe lights with cameras, executing a strobe illuminates the field(s) of video after the flash of light. Once Vsync occurs, you have missed the opportunity to illuminate and acquire the next full field of video and incur a one field delay in acquire. Cameras have a region immediately after Vsync where a strobe will not give the desired result. This no strobe region is when the camera is transferring the previous field from the camera. The following figures show scenarios with the strobe light firing at different positions. Both figures assume that fast strobe mode is selected.

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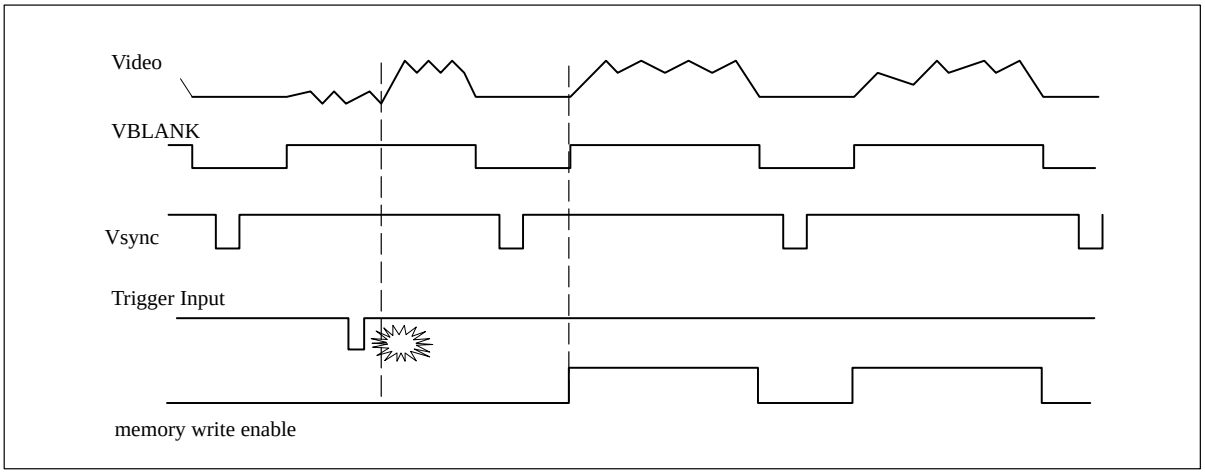


Figure 2–33. Strobe Light Effect

As shown in Figure 2–33, the strobe may partially illuminate the current field in which the trigger and flash occur, and must continue to illuminate the full frame (two fields for interlaced video) following after the field in which the strobe light fires. The field in which the strobe light fires is not useable.

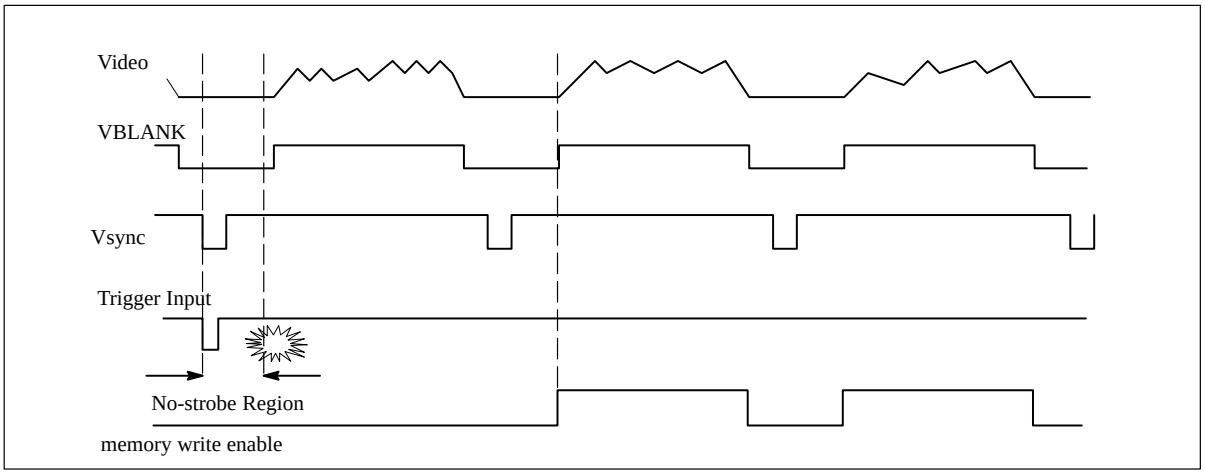


Figure 2–34. Coincident Strobe Effect

Figure 2–34 shows the effect when the trigger occurs coincident with Vsync. In this case, the camera has already begun a camera transfer and the strobe light must be delayed past this region. The acquire still does not start until the next vertical blank.

From Figures 2–33 and 2–34 it can be seen that when using strobes, the region from one Vsync falling edge to the next Vsync falling edge is the region to fire a strobe for the next fields to be acquired.

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2.7.7.2 Back To Back Trigger

Software may want to qualify back to back triggered acquires by polling VBLANK and then issuing a software trigger to execute an acquire. The problem with this method is, there is only a short period of time between the falling edge of VBLANK to the falling edge of Vsync, in which you can fire the software trigger to catch the next frame of video (if software trigger comes at or after Vsync, one field delay is incurred). To facilitate this desired mode of operation, PCVision*plus* allows the user to disable the strobe output (STRBEN bit). With strobe disabled, the Vsync signal is ignored, allowing a trigger cycle to execute if triggered anywhere within VBLANK (if the trigger is not received before the rising edge of VBLANK, the next field is missed). This feature gives software a full VBLANK time to execute the consecutive frame trigger cycles.

2.7.7.3 Stored Trigger

Another feature of the trigger circuit is stored trigger events. By setting the TRIGMD bit, the trigger event inputs can be latched if a trigger cycle is currently in progress. Normally, PCVision*plus* ignores trigger inputs if a trigger cycle is in progress. By setting TRIGMD, trigger events that occur during a trigger cycle will be latched and execute another trigger cycle immediately following the cycle in progress. This mode allows back to back cycles with strobes enabled, as the new cycle will start immediately prior to Vsync which was shown to incur a field delay.

2.7.7.4 Skip Field Mode

A “skip field” mode is available in all triggered acquire and frame reset cycles. Skip field mode forces the trigger circuit to skip the first field after the trigger, and acquire starting on the next field. Skip field can be used with cameras that require a one field delay after a frame reset cycle.

2.7.7.5 Trigger on Frame-Slow Strobe Mode

Slow strobe mode outputs a strobe pulse after the first vertical blank following an external trigger input. Vertical sync activates the STRBDLY counter which allows the strobe pulse to be positioned a programmable number on lines after the vertical sync. This allows positioning the strobe pulse with respect to the acquired frame. The strobe pulse is one line in duration and output polarity is programmable.

In Figure 2–35, the trigger cycle begins on the next vertical blank after the external trigger pulse. At the vertical sync pulse (Vsync), TRIGEN is cleared and TRIGCYC is set high, indicating the triggered acquire cycle has begun. The Vsync pulse also starts the strobe delay counter (STRBDLY). The strobe pulse occurs when the STRBDLY count reaches zero; a programmed number of lines after Vsync. The image memory load begins during the vertical active region. One or two fields are acquired and loaded into memory, according to the PWG registers.

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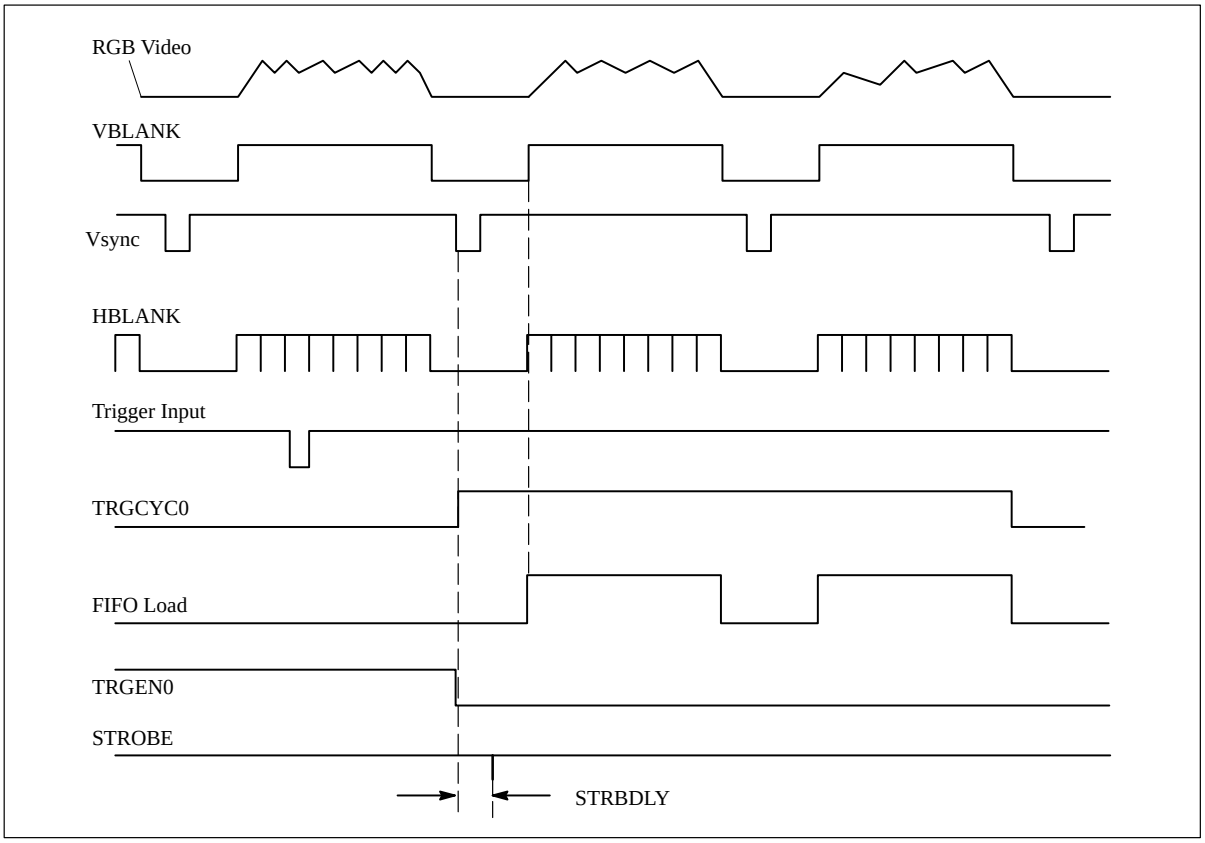


Figure 2–35. Triggered Acquire Cycle in Slow Strobe

2.7.7.6 Trigger on Frame-Fast Strobe Mode

Fast strobe mode outputs a strobe pulse immediately after an external trigger input, unless the trigger occurs in the “no-strobe region”. The no-strobe region is a number of lines from Vsync, programmed in the STRBDLY register. After the external trigger input, the next field or frame is loaded into the image memory and acquired by the frame memory. If the external trigger occurs coincident with VSYNC, the strobe is delayed past the no-strobe region and the acquire is delayed to the next field. The strobe pulse is one line in duration, and polarity is programmable.

In Figure 2–36, the trigger cycle begins on the next vertical blank after the external trigger pulse. The strobe pulse occurs immediately, or the strobe delay counter starts. If the trigger occurs in the no-strobe region, the strobe pulse will not occur until the end of the no-strobe region, at the end of the STRBDLY count. At the first Vsync pulse after the trigger, TRIGEN is cleared and TRIGCYC set high, indicating the triggered acquire cycle has begun. One or two fields are acquired and loaded into the image memory based on the PWG programming.

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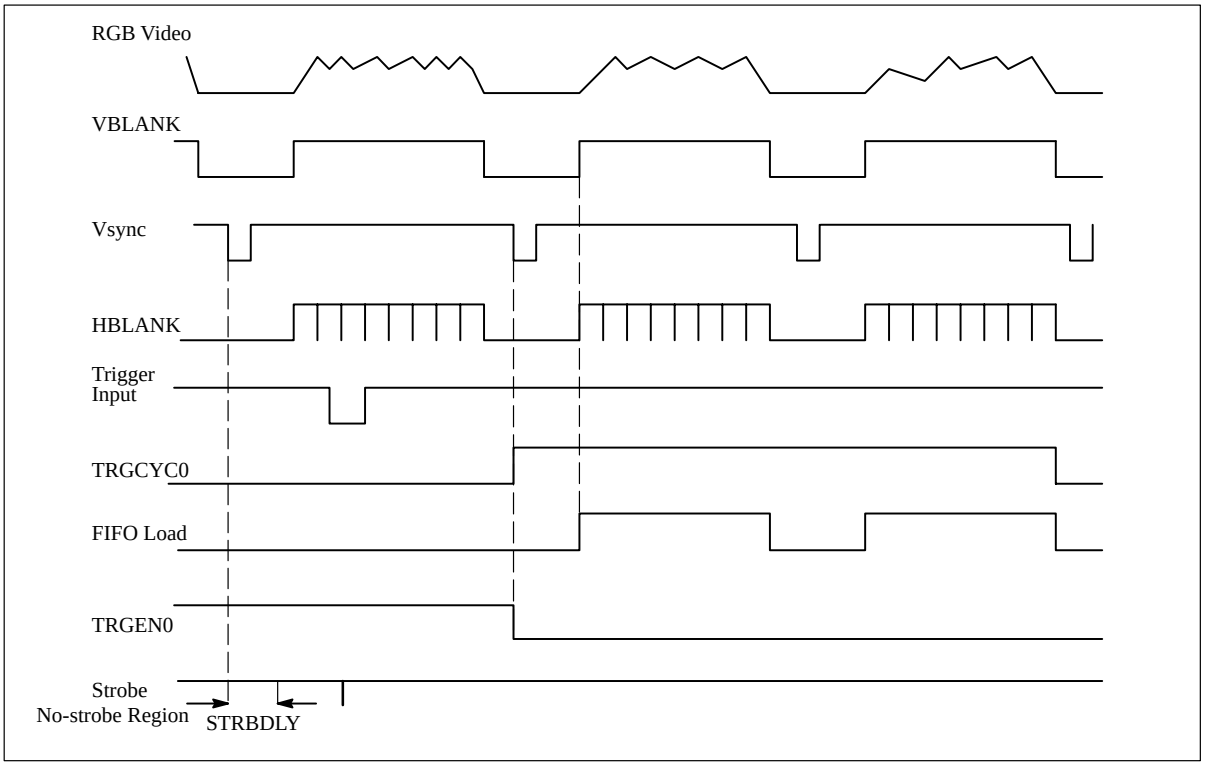


Figure 2–36. Triggered Acquire in Fast Strobe

2.7.7.7 Frame Reset Mode

In frame reset mode, the PWG is halted in vertical blank, waiting for an external trigger input. When the external trigger occurs, the frame reset counter is loaded and counts off the number of lines programmed in the FROFF register before starting the PWG counters. This extra delay count is only used for the first field of a frame reset cycle, and allows for extra delay associated with a camera frame reset. Once the frame reset delay counts down, the PWG resumes standard operation for one, two, or three fields based on the programmed mode of operation (Interlaced, non-interlaced, and skip field mode). After the frame is acquired, the PWG again halts in vertical blank.

A frame reset pulse is output on the video connector, coincident with the external trigger, to asynchronously reset the camera. The FRSTSZ bit selects the duration of the frame reset pulse as either one line or the number of lines programmed in the FROFF value. The polarity of the frame reset pulse is programmable. A strobe pulse (one line duration) is output when the PWG line counter reaches the STRBDLY count. After the extended vertical offset region (VOFF+FROFF) count expires, the memory begins acquiring the programmed active region (frame or field depending on interlacing mode). The TRIGEN and TRIGCYC bits indicate the progress of the triggered acquire cycle.

The PTG (used in XTAL mode) is reset by the frame reset. This causes the vertical sync output of the PTG to be reset coincident with the frame reset pulse output to the camera. Some cameras do not have a frame reset pulse input, but

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instead require the frame reset to occur by simply pulling the vertical sync input to the reset state, which is accomplished by this PTG feature. Some cameras require no vertical sync when in frame reset mode, which can be accommodated using the VSYNCEN bit to disable the PTG vertical sync output when in frame rest mode. The Hsync is not reset in this mode because frame reset does not require the horizontal timing to be reset. Using frame reset in PLL mode, incoming Hsync is not reset by the frame reset signal; therefore maintaining horizontal line lock.

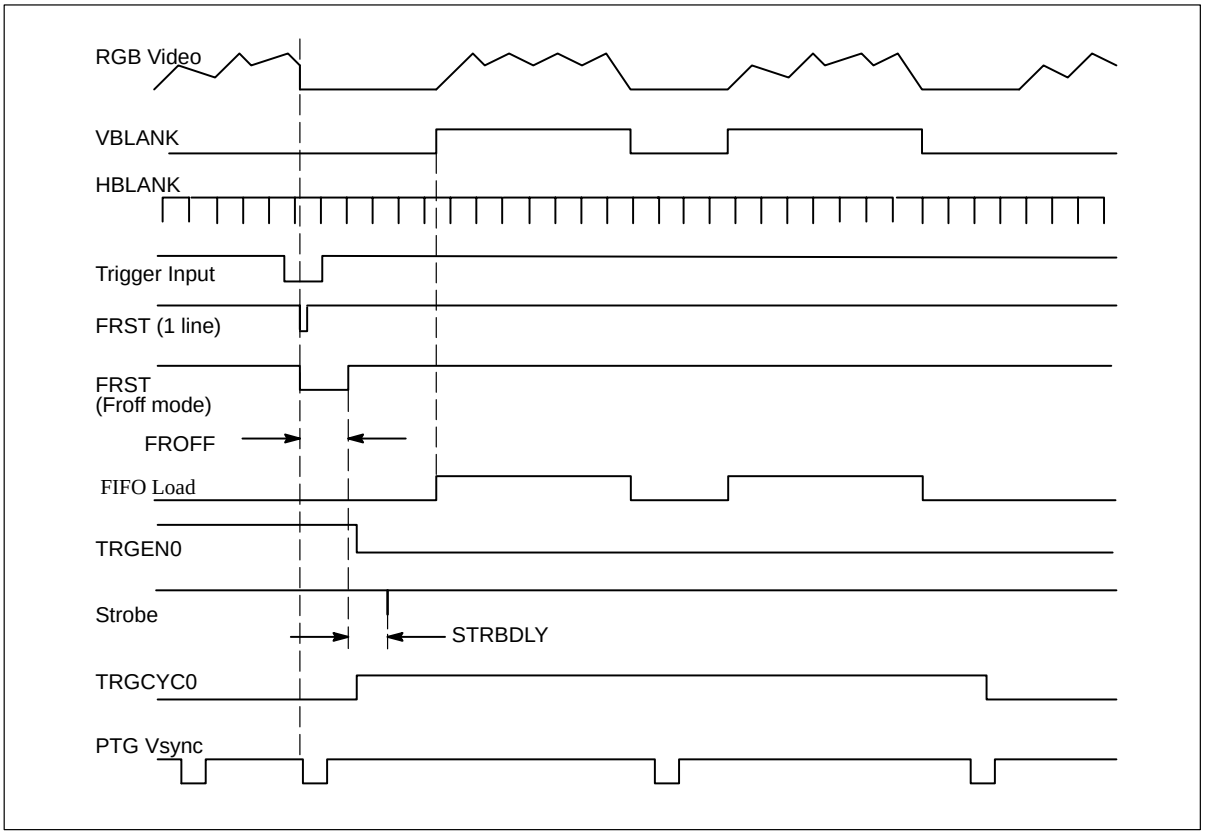


Figure 2–37. Triggered Acquire in Frame Reset

In Figure 2–37, the external trigger pulse immediately causes a Frame Reset pulse (FRST). The pulse duration is one line or the number of lines in the FROFF register. A strobe occurs immediately, or at the end of the STRBDLY count. The strobe output follows the same rules as Fast Strobe mode. STRBDLY is commonly increased to compensate for the FROFF delay. In XTAL mode the PTG Vsync is reset by FRST. The Frame Reset pulse resets the camera, forcing the camera video output into vertical blank. One line after the frame reset pulse TRIGCYC is set high and TRIGEN is cleared, indicating the acquire cycle has begun.

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CHAPTER 3
REGISTERS

This chapter provides a detailed description of all PCVision*plus* registers and bits. The PCVision*plus* contains five separate register groups: PCI Configuration Registers, PCI Interface Control Registers, Board ID Registers, Acquisition Control Registers, and Frame Buffer Registers. All registers support 32-bit access only.

The PCI Configuration Registers are required for PCI compliance and are located at predetermined address offsets. The PCI Interface Control Registers, Board ID Registers, Acquisition Control Registers, and Frame Buffer Control Registers each have a separate base address within the host system address region. Each base address is determined by the system on power up and loaded into the Base Address Zero, One, Two, and Three registers (BADR0, BADR1, BADR2, BADR3).

Figure 3–1 shows the mapping of the PCI Configuration Registers. Figure 3–2 shows the mapping of the PCI Interface Control Registers. Figure 3–3 shows the mapping of the Board ID Registers. Figure 3–4 shows the mapping of the Acquisition Control Registers. Figure 3–5 shows the mapping of the Frame Buffer Control Registers. The figures also give page number references for the register definitions.

The following conventions are used throughout this chapter. The R/W notation following a register or bit name indicates the register or bit supports both read and write access. The R-O notation following a register or bit name indicates the register or bit supports read access only. The W-O notation following a register or bit name indicates the register or bit supports write access only. The R/W1C notation following a bit name indicates the bit is read for status, and writing a one clears the bit “write 1 clear”.

NOTE *Upon power–up most of the PCVisionplus registers are in an unknown state. The host CPU must initialize these registers for proper operation. A system reset affects some but not all of these registers.*

NOTE ***Program all reserved bits and registers to zero unless otherwise indicated.***

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PCI Configuration Registers

These registers are loaded by a boot PROM with information about the PCVision*plus*, (memory size, register size, type of device, etc.) which the PCI-bus host uses in conjunction with information from all other PCI devices in the system to determine an optimum configuration. Access to these register is accomplished through special configuration cycles. A separate base address is not required for this register set.

Address offset		*Page #*
0x0–0x1	Vendor ID (VID)	3–6
0x2–0x3	Device ID (DID)	3–6
0x4–0x5	PCI Command (PCICMD)	3–7
0x6–0x7	PCI Status (PCISTAT)	3–9
0x8	Revision ID (RID)	3–11
0x9–0xB	Class Code (CLCD)	3–11
0xC	Cache Line Size (CALN)	3–11
0xD	Master Latency Timer (LAT)	3–11
0xE	Header Type (HDR)	3–12
0xF	Built-in Self Test (BIST)	3–12
0x10–0x13	Base Address 0 (BADR0)	3–12
0x14–0x17	Base Address 1 (BADR1)	3–13
0x18–0x1B	Base Address 2 (BADR2)	3–13
0x1C–0x1F	Base Address 3 (BADR3)	3–14
0x20–0x23	Base Adddress 4 (BADR4)	3–14
0x24–0x27	Base Address 5 (BADR5)	3–15
0x28–0x2F	*Reserved*	
0x30–0x33	Expansion ROM Base Address (EXROM)	3–15
0x34–0x3B	*Reserved*	
0x3C	Interrupt Line (INTLN)	3–15
0x3D	Interrupt Pin (INTPIN)	3–16
0x3E	Minimum Grant (MINGNT)	3–16
0x3F	Maximum Latency (MAXLAT)	3–16
0x40–0xFF	*Reserved*	

Figure 3–1. PCI Configuration Register Map

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PCI Interface Control Registers Address Space

The PCVision*plus* requires 16 DWORDs or 64 bytes of address space to map the PCI Interface Control Registers. Access is DWORD only.

BADR0 +		*Page #*
0x0	Mailbox 1 (MBOX1)	3–17
0x4	Mailbox 2 (MBOX2)	3–17
0x8	Mailbox3 (MBOX3)	3–17
0xC	Mailbox 4 (MBOX4)	3–17
0x10–0x20	*Reserved*	
0x24	Bus Master Destination Address (BMDST)	3–18
0x28	Bus Master Transfer Count (BMXC)	3–18
0x2C–0x34	*Reserved*	
0x38	Interrupt Control/Status (INTCTL)	3–19
0x3C	Bus Master Control/Status (BMCTL)	3–21

Figure 3–2. PCI Interface Control Register Map

Board ID Registers Address Space

The PCVision*plus* requires 16 DWORDs or 64 bytes of address space to map the Board ID Registers. The Board ID registers are defined as 32-bit (DWORD) access only.

BADR1 +		*Page #*
0x00	Board Status (BRDSTAT)	3–23
0x04	FPGA Programming (ORCAPRGM)	3–25
0x08	FPGA Reset (ORCARST)	3–25
0x0C–0x3C	*Reserved*	

Figure 3–3. Board ID Registers

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Acquisition Control Registers Address Space

The PCVision*plus* requires 256K DWORDs or 1MB of address space to map the Acquisition Control Registers. Access to this space is DWORD only.

BADR2 +		*Page #*
0x00	PTG Horizontal 1 (PTGH1)	3–27
0x04	*Reserved*	
0x08	PTG Vertical 1 (PTGV1)	3–29
0x0C	PTG Vertical 2 (PTGV2)	3–31
0x10	PWG Horizontal (PWGH)	3–33
0x14	PWG Vertical (PWGV)	3–35
0x18	Input Control 1 (INCON1)	3–38
0x1C	Input Control 2 (INCON2)	3–44
0x20	AM Interrupt Status (AMINTCLR)	3–49
0x24	AM Interrupt Control (AMINTEN)	3–51
0x28	Software Trigger (SOFTTRIG)	3–53
0x2C	Programmable Clamp (PCLAMP)	3–53
0x30	*Reserved*	
0x34	PLL Programming Port (PLLPROG)	3–56
0x38	DAC Programming Port (DACPROG)	3–56
0x3C	Timer Counter (TIMER)	3–57
0x40	Parallel Port Control (PORTCON)	3–58
0x44	PIO Output Port (OUTPORT)	3–60
0x48	PIO Input Port (INPORT)	3–60
0x4C	Alpha Control (ALPHA)	3–61
0x50–0x3FFFF	*Reserved*	
0x40000–0x7FFFF	Input LUT	3–61
0x80000–0xFFFFF	*Reserved*	

Figure 3–4. Acquisition Control Registers

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Frame Buffer Control Registers

The PCVision*plus* requires 64K DWORDs or 1MB of address space to map the Frame Buffer Control Registers. Access to this space is DWORD only.

BADR3 +		*Page #*
0x00	Acquisition Control (ACQREG)	3–64
0x04	*Reserved*	
0x08	*Reserved*	
0x0C	*Reserved*	
0x10	Bus Master Control (BMCTLX)	3–68
0x14	Memory Initialization (MEMINIT)	3–71
0x18	Acquisition Start Address (ACQSTRT)	3–72
0x1C	Acquire Interrupt Line (ACQLINEINT)	3–73
0x20	Segment Size (SGSZ)	3–74
0x24	OCT Start Address (OCTSTART)	3–75
0x28	Interrupt Status (INTSTAT)	3–75
0x2C	Interrupt Control (INTENREG)	3–77
0x30	Acquire Address (ACQADR)	3–78
0x30–0x3FFFF	*Reserved*	
0x40000–0x7FFFF	Output Control Table	3–79
0x80000–0xBFFFF	Scatter Gather Table	3–81
0xC0000	Add-On Interrupt Control (AINT)	3–82
0xC0004	Add-On General Control (AGCSTS)	3–83
0xC0008	Manual Destination Address (MDSTADR)	3–83
0xC000C	Manual Transfer Count (MXCNT)	3–84
0xC0010–0xFFFFF	*Reserved*	

Figure 3–5. Frame Buffer Control Registers

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3.1 PCI CONFIGURATION REGISTERS

Each PCI-bus device contains a unique 256-byte region called its “configuration header space”. The PCVision*plus* loads initial values into these registers at power-up. This section describes each of the configuration space fields, its address, and the default values loaded at power-up. Portions of this configuration header are mandatory for compliance with the PCI specification. Access to these registers requires a special PCI bus cycle called a configuration cycle. The map for these registers is given in Figure 3–1 on page 3–2.

3.1.1 Vendor Identification (VID) R-O

Address offset 0x0

7			VENDOR_ID				0
0	0	**1**	0	**1**	**1**	**1**	**1**

15							8
0	0	0	1	0	0	0	**1**

This register contains the Imaging Technology Incorporated (Coreco Imaging, Inc.) vendor identification number assigned by the PCI SIG (Special Interest Group). This register value 0x112F (4399 Decimal) identifies the PCVision*plus* as manufactured by Coreco Imaging, Inc.. This register is boot-loaded at power-up and is read only.

3.1.2 Device Identification (DID) R-O

Address offset 0x2

7			DEVICE_ID				0
0	0	0	0	0	1	1	1

15							8
0	0	0	0	0	0	0	0

This register contains a device identification number (0x07) assigned at Coreco Imaging, Inc. to identify this product as the PCVision*plus*. This register is boot-loaded at power-up and is read only.

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3.1.3 PCI Command (PCICMD) R/W

Address offset 0x4

PCICMD

7							0
0	PAREN	0	0	0	PCIBMEN	MEMEN	IOEN

15							8
0	0	0	0	0	0	FBB	SREN

This register provides coarse control over the PCVision*plus* ability to generate and respond to PCI-bus cycles. Individual bits are available to enable and disable the PCI interface. All bits shown as zero are reserved and read only. This register is initialized with the assertion of the PCI #RESET line.

Bit	*Mnemonic*	*Function*
0	IOEN	I/O Space Access Enable
1	MEMEN	Memory Space Access Enable
2	PCIBMEN	Bus Master Enable
3–5	Reserved	Must be zero
6	PAREN	Parrity Error Enable
7	Reserved	Must be zero
8	SEREN	System Error Enable
9	FBB	Fast Back-to-back Transfer Enable
10–15	Reserved	Must be zero

3.1.3.1 I/O Space Enable (IOEN) R/W

This bit allows the PCVision*plus* to decode and respond as a target to I/O cycles which are to regions defined as I/O space in the base address registers. This bit is initialized to zero at power-up. This bit should be written to one as part of the initialization routine.

IOEN	Function
0	Disable I/O access
1	Enable I/O access

3.1.3.2 Memory Space Enable (MEMEN) R/W

This bit allows the PCVision*plus* to decode and respond as a target to memory cycles which are to regions defined as memory space in the base address registers. This bit is initialized to zero at power-up. This bit should be written to one as part of the initialization routine.

MEMEN	Function
0	Disable memory access
1	Enable memory access

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3.1.3.3 Bus Master Enable (PCIBMEN) R/W

This bit allows the PCVision*plus* to function as a bus master in the PCI system. This bit is initialized to zero at power-up. This bit should be written to one as part of the initialization routine.

PCIBMEN	Function
0	Disable bus master mode
1	Enable bus master mode

3.1.3.4 Parity Error Enable (PAREN) R/W

This bit allows the PCVision*plus* to check for parity errors and generate the PCI signal #PERR when an error is detected. This bit is initialized to zero at power-up.

PAREN	Function
0	Disable parity detection
1	Enable parity detection

3.1.3.5 System Error Enable (SEREN) R/W

This bit allows the PCVision*plus* to drive the #SERR pin upon detection of a system error. #SERR driven usually indicates a parity error on the PCI address and control bus. This bit is initialized to zero at power-up.

SEREN	Function
0	Disable system error
1	Enable system error

3.1.3.6 Fast Back-to-Back Transfer Enable (FBB) R/W

This bit allows the PCVision*plus* to perform fast back-to-back bus master cycles. This bit is initialized to zero at power-up.

FBB	Function
0	Disable fast back-to-back transfer
1	Enable fast back-to-back transfer

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3.1.4 PCI Status (PCISTAT) R/W1C

Address offset 0x6

7			PCISTAT				0
1	0	0	0	0	0	0	0

15							8
DPARE	SSERR	RMABT	RTABT	STABT	0	0	DTPAR

This register contains PCI status information generated and received by the PCVision*plus*. All bits defined as 0 or 1 are reserved read-only bits. All others contain status information and are read/write-one-clear (this means if a bit is read as set, to clear it the bit must be written to one). Writing a status bit that is set to zero will have no effect.

Bit	*Mnemonic*	*Function*
0–6	Reserved	Must be zero
7	Reserved	Must be one
8	DTPAR	Data Parity Error Reported
9–10	Reserved	Must be zero
11	STABT	Signaled Target Abort
12	RTABT	Received Target Abort
13	RMABT	Received Master Abort
14	SSERR	Signaled System Error
15	DPARE	Detected Parity Error

3.1.4.1 Data Parity Reported (DTPAR) R/W1C

The DTPAR bit is set (1) whenever a data parity error is detected for transfers involving the PCVision*plus*. The Parity Error Enable bit (PAREN in PCICMD register) must be set (1) in order for this bit to be set. This bit is cleared by writing it to one (1), or by the assertion of the PCI #RESET signal.

DTPAR	Function
0	No data parity reported
1	Data parity reported

3.1.4.2 Signaled Target Abort (STABT) R/W1C

This bit is set whenever the PCVision*plus* aborts a cycle when addressed as a target. This bit is cleared by writing it to one (1).

STABT	Function
0	No target abort
1	Generated target abort

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3.1.4.3 Received Target Abort (RTABT) R/W1C

This bit is set whenever the PCVision*plus* receives a target abort response from the addressed target during a bus master write cycle initiated by the PCVision*plus*. This bit is cleared by writing it to one (1).

RTABT	Function
0	No target abort
1	Target abort received

3.1.4.4 Received Master Abort (RMABT) R/W1C

This bit is set whenever a master abort occurs. Master abort will occur if the PCVision*plus* generates a Bus Master Write Cycle to a target and the target doesn't respond. This bit is cleared by writing it to one (1).

RMABT	Function
0	No master abort
1	Master abort occurred

3.1.4.5 Signaled System Error (SSERR) R/W1C

This bit is set whenever the PCVision*plus* asserts the #SERR signal due to a system error. This bit is cleared by writing it to one (1).

SSERR	Function
0	No system error
1	System error

3.1.4.6 Detected Parity Error (DPARE) R/W1C

This bit is set whenever the PCVision*plus* detects a parity error. This bit functions independently from the state of the Parity Error Detection Enable bit (PAREN PCICMD register). This bit is cleared by writing it to one (1).

DPARE	Function
0	No data parity error
1	Data parity error

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3.1.5 Revision Identification (RID) R-O

Adress offset 0x8

7			REVID				0
REVID7	REVID6	REVID5	REVID4	REVID3	REVID2	REVID1	REVID0

This register contains a revision identification number assigned by Coreco Imaging, Inc. which will reflect the revision of the PCVision*plus*. This register is boot-loaded at power-up and is read-only.

3.1.5.1 Revision Field (REVID) R-O

The revision level will change with each functional change to the PCVision*plus* hardware design, allowing the software to identify the revision and the corresponding functionality.

3.1.6 Class Code (CLCD) R-O

Address offset 0x9

7			CLASSCODE				0
0	0	0	0	0	0	0	0

15							8
0	0	0	0	0	0	0	0

23							16
0	0	0	0	0	**1**	0	0

This register contains a class code for the PCVision*plus* as defined by PCI SIG. The PCVision*plus* is defined as a Multimedia Device (Base Class = 0x04) of type Video (Sub-Class =0x00). This register is boot-loaded at power-up and is read-only.

3.1.7 Cache Line Size (CALN) R-O

Address offset 0xC

7			CALN				0
0	0	0	0	0	0	0	0

This configuration register does not apply to the PCVision*plus* and is hard-wired to zero. This register is read only.

3.1.8 Latency Timer (LAT) R/W

Address offset 0xD

7			LAT				0
LAT4	LAT3	LAT2	LAT1	LAT0	0	0	0

This register defines the number of PCI clocks a bus master cycle will be guaranteed. Setting this register will guarantee the PCVision*plus* will be granted the bus during bus master operations for the set amount of time. The value set by LAT(4–0) = # of clocks x 8. The three lsbs (least significant bits) are read only. This register is boot-loaded at power-up to a value of zero.

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3.1.9 Header Type (HDR) R-O

Address offset 0xE

7			HDR				0
0	0	0	0	0	0	0	0

This register is used to define the configuration header layout for bytes at address 0x10 thru 0x3F. It also defines the PCVision*plus* as a single function PCI device. This register is boot-loaded at power-up to a value of zero and is read only.

3.1.10 Built-In Self-Test (BIST) R-O

Address offset 0xF

7			BIST				0
0	0	0	0	0	0	0	0

Built-In Self-Test is not supported on the PCVision*plus*. This register is boot-loaded at power-up to a value of zero and is read only.

3.1.11 Base Address Zero (BADR0) R-O

Address offset 0x10

7			BADR0				0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This register is boot-loaded at power-up with a value that indicates the amount of address space required for the PCI Interface Control Registers (16 DWORDs or 64 bytes are required). During power-up the PCI host system reads this register to determine the size of the address region and assigns a base address. The PCI host writes the assigned base address in this register. The user application can determine the assigned address by reading Base Address Zero (BADR0). Access to this space is DWORD only. This register is read-only to the user application.

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3.1.12 Base Address One (BADR1) R-O

Address offset 0x14

BADR1

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This register is boot-loaded at power-up with a value that indicates the amount of address space required for the Board ID Registers (16 DWORDs or 64 bytes are required). During power-up the PCI host system reads this register to determine the size of the address region and assigns a base address. The PCI host writes the assigned base address in this register. The user application can determine the assigned address by reading Base Address One (BADR1). This register is read only to the user application. The Board ID Register space is defined as 32-bit (DWORD) access only.

3.1.13 Base Address Two (BADR2) R-O

Address offset 0x18

BADR2

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This register is boot-loaded at power-up with a value that indicates the amount of address space required for the Acquisition Control registers and LUTs (256K DWORDs or 1MB required). During power-up the PCI host system reads this register to determine the size of the address region and assigns a base address. The PCI host writes the assigned base address in this register. The user application can determine the assigned address by reading Base Address Register Two (BADR2). This register is read only to the user application. The Acquisition Control Register Address space is defined as 32-bit (DWORD) access only.

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3.1.14 Base Address Three (BADR3) R-O

Address offset 0x1C

BADR3

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This register is boot-loaded at power-up with a value that indicates the amount of address space required for the Frame Buffer Control registers, Output Control Table and Scatter Gather Table (256K DWORDs or 1MB required). During power-up the PCI host system reads this register to determine the size of the address region and assigns a base address. The PCI host writes the assigned base address in this register. The user application can determine the assigned address by reading Base Address Register Three (BADR3). This register is read only to the user application. The Frame Buffer Control Register Address space is defined as 32-bit (DWORD) access only.

3.1.15 Base Address Four (BADR4) R-O

Address offset 0x20

BADR4

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This register is boot-loaded at power-up with a value that indicates the amount of address space required for the PCVision*plus* Image memory (4MB required). During power-up the PCI host system reads this register to determine the size of the address region and assigns a base address in the memory address region (always memory mapped). The PCI host writes the assigned base address in this register. The user application can determine the assigned address by reading Base Address Register Three (BADR3). This register is read only to the user application. Access to the image memory is 32-bit (DWORD) only.

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3.1.16 Base Address Five (BADR5)

Address offset 0x24

BADR5

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This address register is not used by the PCVision*plus* and returns all zeros if read. This register is read only.

3.1.17 Expansion ROM Base Address (XROM) R-O

Address offset 0x30

XROM

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

Expansion ROM is not supported on the PCVision*plus*. This register is reserved and will return all zeros if read. This register is read only.

3.1.18 Interrupt Line (INTLN) R/W

Address offset 0x3C

INTLN

7							0
INTLN7	INTLN6	INTLN5	INTLN4	INTLN3	INTLN2	INTLN1	INTLN0

This register indicates the interrupt routing for the PCVision*plus*. The ultimate value for this register is system-architecture specific. In x86 based systems, the values in this register correspond with the established interrupt numbers associated with the dual 8259 controllers used in those machines. In x86 based PC systems, the values of 0 through 15 correspond with IRQ0 through IRQ15, and the values from 16 to 254 are reserved. This register is boot-loaded at power-up with 0xFF (255) indicating an unknown or unconnected system interrupt. This register is read/write.

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3.1.19 Interrupt Pin (INTPIN) R-O

Address Offset + 0x3D

7			INTPIN				0
0	0	0	0	0	0	0	**1**

This register indicates the PCI interrupt pin used by the PCVision*plus*. This register is boot-loaded at power-up with a value of 0x1 indicating PCI interrupt pin #INTA is connected to the PCVision*plus*. This register is read only.

3.1.20 Minimum Grant (MINGNT) R-O

Base Address + 0x3E

7			MINGNT				0
1	1	1	1	1	1	1	1

This register provides information to the host PCI system indicating the minimum amount of time the PCVision*plus* will require for bus master write transfers. The register is boot-loaded at power-up with a value of 0xFF (255) which indicates a desired minimum bus master access time of 64 microseconds (255 x 250 ns). This register is read-only.

3.1.21 Maximum Latency (MAXLAT) R-O

Address offset + 0x3F

7			MAXLAT				0
0	0	0	0	0	0	0	**1**

This register provides information to the host PCI system indicating how often the PCVision*plus* needs to gain access to the PCI bus as bus master. The register is boot-loaded at power-up with a value of 0x01 (1) which indicates a desired maximum latency between master access of 250 nanoseconds (1 x 250 ns). This register is read-only.

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3.2 PCI INTERFACE CONTROL REGISTERS

The PCVision*plus* requires 16 DWORDs of address space to map several registers used to control the PCI host interface circuitry. This section describes each of the registers function, address offset, and initial power-up values. The Interface Control Registers are mapped into system 32-bit address space specified by the Base Address Zero (BADR0) register. The map for these registers appears in Figure 3–2 on page 3–3. Target access is supported by this register set.

This register set controls the PCI-bus interface chip. Some functions built into this chip are replicated in the Bus Master Controller. In some cases the fields in this set are used with the BMC. In some cases the fields in this set are not used.

3.2.1 Mailbox Registers (MBOX1, MBOX2, MBOX3, MBOX4) R/W

BADR0 + 0x0, 0x4, 0x8, 0xC

MBOXn

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
15							8
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
23							16
DATA23	DATA22	DATA21	DATA20	DATA19	DATA18	DATA17	DATA16
31							24
DATA31	DATA30	DATA29	DATA28	DATA27	DATA26	DATA25	DATA24

These four DWORD registers provide a method for software to pass commands or status information between applications running simultaneously. These registers do not directly control the PCVision*plus* hardware.

NOTE *The IFC-SDK software and display utilities use the mailbox registers for communication. Writing to these registers while a library, application, or utility is running may interfere with operation.*

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3.2.2 Bus Master Destination Address (BMDST) R-O

BADR0 + 0x24

BMDST

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This register indicates the status of the PCI destination address for data moving from the image memory to the PCI-bus during Bus Master write operations. This register is continually updated during the transfer process and will always point to the next unwritten location. Reading this register during the transfer process (a read causes the transfer to halt and the PCI interface to operate in target mode) is permitted and may be used to monitor the progress of the transfer. This register is read only.

The real destination address is loaded in the scatter gather table. *The destination address must be on DWORD (32-bit) boundaries* to allow the PCVision*plus* to send data anywhere within the defined PCI address range (ADR1 and ADR0 must be zero). The two lsbs (least significant bits) will be zero during the address phase of a bus master write transfer indicating to the target that the data from the PCVision*plus* is in linear format and that the PCVision*plus* is burst capable (therefore the target should not arbitrarily disconnect after the first data transfer).

3.2.3 Bus Master Transfer Count (BMXC) R-O

BADR0 + 0x28

BMXC

7							0
BMXC7	BMXC6	BMXC5	BMXC4	BMXC3	BMXC2	BMXC1	BMXC0
15							8
BMXC15	BMXC14	BMXC13	BMXC12	BMXC11	BMXC10	BMXC9	BMXC8
23							16
Reserved	Reserved	BMXC21	BMXC20	BMXC19	BMXC18	BMXC17	BMXC16
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register indicates the status of the transfer count during a bus master transfer. This register is continually updated during the transfer operation. The value in this register decrements with each byte written during the bus master operation until the count reaches zero. Upon reaching zero, the write transfer operation ceases An end-of-transfer interrupt can be generated to the PCI bus interface.

The actual transfer count is loaded in the scatter gather table. The transfer count must be on DWORD (32-bit) boundaries to allow the PCVision*plus* to send data anywhere within the defined PCI address range.

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3.2.4 PCI Interrupt Control and Status (INTCTL) R/W

BADR0 + 0x38

INTCTL

7							0
0	0	0	0	0	0	0	0
15							**8**
Reserved	BINTEN	0	INTEN	**1**	**1**	**1**	**1**
23							**16**
Reserved	0	TAINT	MAINT	Reserved	BINTST	INTST	Reserved
31							**24**
0	0	0	0	0	0	0	0

This register provides a method for choosing conditions that produce an interrupt to the PCI bus, a method for viewing the cause of the interrupt, and a method for acknowledging (removing) the interrupt's assertion. This register must be used in conjunction with the many other interrupt enable and clear registers and bits on the PCVision*plus*. The following conditions could produce a PCI-bus interrupt: Bus Master Transfer Count reaches zero, Target Abort, Master Abort, or a PCVision*plus* interrupt defined in the INTENREG or AMINTEN registers. *Always program bits defined as zero or one to their respective values.*

Bit	*Mnemonic*	*Function*
0–7	Reserved	Must be zero
8–11	Reserved	Must be one
12	INTEN	PCI Interrupt Enable
13	Reserved	Must be zero
14	BINTEN	Interrupt on Bus Master Transfer Done
15–16	Reserved	"Don't Care"
17	INTST	PCI Interrupt Status
18	BINTST	Bus Master Interrupt Status
19	Reserved	"Don't Care"
20	MAINT	Master Abort Interrupt Status
21	TAINT	Target Abort Interrupt Status
22	Reserved	Must be zero
23	Reserved	"Don't Care"
24–31	Reserved	Must be zero

3.2.4.1 PCI Interrupt Enable (INTEN) R/W

This bit enables the interrupt source set by the INCON0, INCON1 and AMINTEN registers to generate an interrupt on the PCI-bus.

INTEN	Function
0	Disable the PCVision*plus* based interrupt
1	Enable the PCVision*plus* based interrupt

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3.2.4.2 Interrupt on Bus Master Transfer Done (BINTEN) R/W

This bit enables a PCI-bus interrupt to be generated when the Bus Master Transfer Count reaches a value of zero during a bus master write transfer from the PCVision*plus* (transfer count zero indicates transfers is done).

BINTEN	Function
0	Disable Transfer-done interrupt
1	Enable Transfer-done interrupt

3.2.4.3 PCI Interrupt Status (INTST) R/W1C

This bit indicates that a PCI-bus interrupt was generated by the source selected in the BMCINTEN register. The INTEN bit must be one for this bit to operate. This bit is always zero if the INTEN is zero. This bit operates as read/write-one-clear. Writing one to this bit resets it to zero. Writing zero has no effect. Refer to Chapter 2 for the correct sequence for setting and clearing interrupts.

INTST	Function
0	No PCVision*plus* interrupt pending
1	PCVision*plus* interrupt pending

3.2.4.4 Bus Master Interrupt Status (BINTST) R/W1C

This bit indicates that a PCI-bus interrupt was generated due to the bus master transfer count register reaching a value of zero indicating the completion of the transfer. The BINTEN bit must be one for this bit to operate. This bit is always zero if the BINTEN is zero. This bit operates as read/write-one-clear. Writing one to this bit resets it to zero. Writing zero has no effect.

BINTST	Function
0	No transfer-done interrupt pending
1	Transfer-done interrupt pending

3.2.4.5 Master Abort Interrupt Status (MAINT) R/W1C

This bit indicates that a PCI-bus interrupt was generated by the PCVision*plus* encountering a Master Abort on the PCI-bus. A Master Abort occurs when there is no target response to a PCI bus cycle. This interrupt source is always enabled. This bit operates as read/write-one-clear. Writing one to this bit resets it to zero. Writing zero has no effect.

MAINT	Function
0	No master-abort interrupt pending
1	Master-abort interrupt pending

3.2.4.6 Target Abort Interrupt Status (TAINT) R/W1C

This bit indicates that a PCI-bus interrupt was generated by the PCVision*plus* encountering a Target Abort during a PCI Bus cycle in which the PCVision*plus* was bus master. This interrupt source is always enabled. This bit operates as read/write-one-clear. Writing one to this bit resets it to zero. Writing zero has no effect.

TAINT	Function
0	No target-abort interrupt pending
1	Target-abort interrupt pending

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3.2.5 Bus Master Host Control/Status (BMCTL) R/W

BADR0 + 0x3C

BMCTL

7							0
BMDONE	Reserved	FIFOEM	FIFO4P	FIFOFL	Reserved	Reserved	Reserved
15							8
0	0	0	0	0	0	0	1
23							16
0	0	0	0	0	0	0	0
31							24
0	0	0	0	0	0	0	RST

Always program bits defined as zero or one to their respective values. Reserved bits are “don’t care” unless otherwise defined.

Bit	*Mnemonic*	*Function*
0–2	Reserved	“Don’t Care”
3	FIFOFL	FIFO Full
4	FIFO4P	FIFO 4 Plus
5	FIFOEM	FIFO Empty
6	Reserved	“Don’t Care”
7	BMDONE	Bus Master Transfer Done
8	Reserved	Must be one
9–23	Reserved	Must be zero
24	RST	Software Reset
25–31	Reserved	Must be zero

3.2.5.1 FIFO Full (FIFOFL) R-O

This bit is set to one when the FIFO becomes full during a bus master transfer from the PCVision*plus* to the PCI-bus. FIFO Full indicates 8 DWORDs of the bus master transfer are in the FIFO waiting to be written to the destination address of the transfer. This bit is read only.

FIFOFL	Status
0	FIFO is not full
1	FIFO is full

3.2.5.2 FIFO 4 Plus (FIFO4P) R-O

This bit is set to one when,the FIFO has four or more DWORDs ready for bus master transfer from the PCVision*plus* to the PCI bus. This bit is read only.

FIFO4P	Status
0	FIFO as less than 4 DWORDs
1	FIFO has more than 4 DWORDs

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3.2.5.3 FIFO Empty (FIFOEM) R-O

This bit is set to one when the FIFO becomes empty, during a bus master transfer from the PCVision*plus* to the PCI-bus. FIFO empty indicates data is not available for transfer during a bus master cycle. This bit is read only.

FIFOEM	Function
0	FIFO is not empty
1	FIFO is empty

3.2.5.4 Bus Master Done (BMDONE) R-O

This bit is set to one when a bus master transfer from the PCVision*plus* to the PCI-bus completes. Completion of a bus master cycle is when the value in the Bus Master Transfer Count register reaches zero. This bit is read only.

BMDONE	Function
0	Bus master cycle not done
1	Bus master cycle done

3.2.5.5 Software Reset (RST) R/W

This bit can be used by software to reset the PCVision*plus* internal hardware. Writing a one to this bit causes a reset to the PCVision*plus*. This bit must be set to zero to remove the reset for proper operation of the PCVision*plus*.

RST	Function
0	No reset
1	Reset the PCVision*plus*

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3.3 BOARD ID REGISTERS

These registers are used to check the build status and revision of the PCVision*plus*, and to load the FPGAs during board initialization. The 64 DWORDs are mapped into system address space starting at the address in the BADR1 register. Figure 3–6 shows the register map for the Board ID registers

BADR1 +		*Page #*
0x00	Board Status (BRDSTAT)	3–23
0x04	FPGA Programming (ORCAPRGM)	3–25
0x08	FPGA Reset (ORCARST)	3–25
0x0C–0x3C	*Reserved*	

Figure 3–6. Board ID registers

3.3.1 Board Status (BRDSTAT) R-O

BADR1 + 0x00

PCP_BLDSTAT_32

7							0
REV1	REV0	CM PRESENT	PIOLSTAT	FPGARDY	FPGA DONE	BLD STAT1	BLD STAT0
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register contains status bits for build options and revision of PCVision*plus*.

Bit	*Mnemonic*	*Function*
0–1	BLDSTAT	Build Status
2	FPGADONE	FPGA Loading Done Status
3	FPGARDY	FPGA Ready Status
4	PIOLSTAT	PIO Level Jumper Setting
5	CMPRESENT	Expansion Module Present
6–7	REV	Revision
8–31	Reserved	“Don’t care”

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3.3.1.1 Build Status (BLDSTAT) R-O

The two BLDSTAT bits reflect the build status (options) of PCVision*plus*.

BLDSTAT	Status
0	Standard version
1	*Reserved*
2	*Reserved*
3	*Reserved*

3.3.1.2 FPGA Loading Done (FPGADONE) R-O

The FPGADONE bit gives the load status of the FPGAs on PCVision*plus*.

FPGADONE	Status
0	Load not complete
1	Load completed

3.3.1.3 FPGA Ready Status (FPGARDY) R-O

This is a status bit used in loading the FPGA files. This bit must be checked after each byte is written to the FPGA. This bit has no effect once the FPGA is loaded and the board is ready for use. Application software should ignore this bit.

FPGARDY	Status
0	Byte load not complete
1	Byte load completed

3.3.1.4 PIO Level Jumper Setting (PIOLSTAT) R-O

This status bit indicates the setting of the jumper which defines the power-up state of the parallel port outputs.

PIOLSTAT	Status
0	PIO power-up level set to 0
1	PIO power-up level set to 1

3.3.1.5 Expansion Module Present (CMPRESENT) R-O

This status bit indicates if an optional expansion module or daughter board is installed on the PCVision*plus*.

CMPRESENT	Status
0	No module installed
1	Expansion module installed

3.3.1.6 Revision (REV) R-O

The two REV bits reflect the revision of the PCVision*plus* hardware. These bits allow software to identify functionality changes to the PCVision*plus* hardware.

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3.3.2 FPGA Programming (ORCAPRGM) R/W

BADR1 + 0x04

PCP_ORCAPRGM_32

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The FPGAs must be loaded with a bit-map file at power-up and every time the host system is reset. *Applications must never read or write to this address*.

3.3.3 FPGA Reset (ORCARST) W-O

BADR1 + 0x08

PCP_ORCARST_32

7							0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Writing any value to this register clears the FPGAs. The FPGAs are cleared at power up and when the system reset line is activated. *Applications must never read or write to this address*.

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3.4 ACQUISITION MODULE CONTROL REGISTERS

These registers control the analog input section of the PCVision*plus*. This 1MB group of addresses is organized into two 64K DWORD areas: AM Control, and Input LUT DWORD access. The AM Control registers are mapped into system address space starting at the address in the BADR2 register. Figure 3–7 shows the register map for the AM Control registers.

BADR2 +		*Page #*
0x00	PTG Horizontal 1 (PTGH1)	3–27
0x04	*Reserved*	
0x08	PTG Vertical 1 (PTGV1)	3–29
0x0C	PTG Vertical 2 (PTGV2)	3–31
0x10	PWG Horizontal (PWGH)	3–33
0x14	PWG Vertical (PWGV)	3–35
0x18	Input Control 1 (INCON1)	3–38
0x1C	Input Control 2 (INCON2)	3–44
0x20	AM Interrupt Status (AMINTCLR)	3–49
0x24	AM Interrupt Control (AMINTEN)	3–51
0x28	Software Trigger (SOFTTRIG)	3–53
0x2C	Programmable Clamp (PCLAMP)	3–53
0x30	*Reserved*	
0x34	PLL Programming Port (PLLPROG)	3–56
0x38	DAC Programming Port (DACPROG)	3–56
0x3C	Timer Counter (TIMER)	3–57
0x40	Parallel Port Control (PORTCON)	3–58
0x44	PIO Output Port (OUTPORT)	3–60
0x48	PIO Input Port (INPORT)	3–60
0x4C	Alpha Control (ALPHA)	3–61
0x50–0x3FFFF	*Reserved*	
0x40000–0x7FFFF	Input LUT	3–61
0x80000–0xFFFFF	*Reserved*	

Figure 3–7. AM Control Register Map

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3.4.1 PTG Horizontal 1 (PTGH1) R/W

BADR2 + 0x00

PCP_PTGH1_32

7							0
HTOTAL7	HTOTAL6	HTOTAL5	HTOTAL4	HTOTAL3	HTOTAL2	HTOTAL1	HTOTAL0
15							**8**
HESYNC5	HESYNC4	HESYNC3	HESYNC2	HESYNC1	HESYNC0	HTOTAL9	HTOTAL8
23							**16**
Reserved	Reserved	Reserved	Reserved	XTALMD HPOL	HSYNCPOL	HESYNC7	HESYNC6
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The PTGH1 register defines the horizontal timing for the Programmable Timing Generator (PTG).

Bit	*Mnemonic*	*Function*
0–9	HTOTAL	Horizontal Sync Pixel Count Total
10–17	HESYNC	Horizontal Sync End
18	HSYNCPOL	Horizontal Sync Output Polarity
19	XTALMDHPOL	Internal Timing Horizontal Sync Polarity
20–31	Reserved	“Don’t care”

3.4.1.1 Horizontal Sync Pixel Count Total (HTOTAL) R/W

HTOTAL defines the Programmable Timing Generator (PTG) horizontal total line time. The 10-bit value is the number of pixel clocks in half the horizontal line time or sync time (duty cycle), including both sync high and sync low time. In internal timing (XTAL) mode, the PTG generates the horizontal sync (Hsync) output to the camera and to the PWG to gen-lock the system. The Maximum total line length is 2048 pixel clocks.

“Total Line Time” includes the sync, blank, and active regions. The pixel clock rate is the clock rate programmed into the frequency synthesizer in XTAL mode. The Total Line Time for RS170 is 63.556 us. The Total Line Time for CCIR is 64 us. The pixel clock time varies from 50 to 100 ns based on the number of samples per line.

Use the following formula for calculating HTOTAL. Also, refer to the example of XTAL mode programming in Appendix A.

HTOTAL = [(Total Line Time (ns)/2) / pixel clock time (ns)] –1

HTOTAL	Function
0	1/2 hsync total = 1 pixel clock
1	1/2 hsync total = 2 pixel clocks
2	1/2 hsync total = 3 pixel clocks
3	1/2 hsync total = 4 pixel clocks
. . .	. . .
1023 (0x3FF)	1/2 hsync total = 1024 pixel clocks

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3.4.1.2 Horizontal Sync End (HESYNC) R/W

HESYNC defines the Programmable Timing Generator (PTG) horizontal sync pulse duration. The 8-bit value is the number of pixel clocks the horizontal sync pulse (Hsync) is low.

The Hsync pulse time for RS170 is 4.7 us. The Hsync pulse time for CCIR is 4.7 us. The pixel clock time varies from 50 to 100 ns based on the number of samples per line.

Use the following formula for calculating HESYNC:

HESYNC = (Hsync pulse time (ns) / pixel clock time (ns)) – 1

HESYNC	Function
0	hsync low = 1 pixel clock
1	hsync low = 2 pixel clocks
2	hsync low = 3 pixel clocks
3	hsync low = 4 pixel clocks
. . .	. . .
255 (0xFF)	hsync low = 256 pixel clocks

3.4.1.3 Horizontal Sync Output Polarity (HSYNCPOL) R/W

The HSYNCPOL bit defines the polarity of the horizontal sync signal driven out onto the camera connectors, in internal timing mode (XTAL). HSYNC is used internally in XTAL mode, and always available (driven) if XTAL mode is enabled.

HSYNCPOL	Function
0	Hsync is active low
1	Hsync is active high

3.4.1.4 Internal Timing Horizontal Sync Polarity (XTALMDHPOL) R/W

This bit only affects the PTG Hsync input to the PWG, and does not affect the signals output to the camera interface, or any other timing circuits. This bit gives additional flexibility to programming the PWG with cameras that respond slowly to the Hsync from the PCVision*plus*.

XTALMDHPOL	Function
0	Normal operation
1	Invert Hsync into PWG

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3.4.2 PTG Vertical 1 (PTGV1) R/W

BADR2 + 0x08

PCP_PTGV1_32

7							0
VTOTAL7	VTOTAL6	VTOTAL5	VTOTAL4	VTOTAL3	VTOTAL2	VTOTAL1	VTOTAL0
15							**8**
VSEND3	VSEND2	VSEND1	VSEND0	VTOTAL11	VTOTAL10	VTOTAL9	VTOTAL8
23							**16**
Reserved	Reserved	Reserved	Reserved	VERROR	EDONP	VSYNCPOL	VSEND4
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The PTGV1 register defines the vertical timing for the Programmable Timing Generator (PTG).

Bit	*Mnemonic*	*Function*
0–11	VTOTAL	Vertical Sync Total
12–16	VSEND	Vertical Sync Low Time
17	VSYNCPOL	Vertical Sync Polarity
18	EDONP	E-Donpisha Mode Enable
19	VERROR	Vertical Error Status
20–31	Reserved	“Don’t care”

3.4.2.1 Vertical Sync Total (VTOTAL) R/W

VTOTAL defines the Programmable Timing Generator (PTG) vertical sync time or total frame time. The 12-bit value is the total number of half lines in the Vsync duty cycle, including sync low and sync high time. When bit 0 (VTOTAL0) is high (even number of 1/2 lines), the PTG timing is non-interlaced. When bit 0 is low (odd number 1/2 lines), the PTG timing is interlaced.

The total number of lines per field for RS170 is 525/2 = 262.5. The total number of lines per field for CCIR is 625/2 = 312.5.

Use the following formula to calculate VTOTAL for interlaced formats:

VTOTAL = (Total number of lines per Field – 0.5) x 2

VTOTAL must be an even number for interlaced frames.

Use the following formula to calculate VTOTAL for Non-interlaced formats:

VTOTAL = (Total number of lines per Frame – 0.5) x 2

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VTOTAL must be an odd number for non-interlaced frames.

VTOTAL	Function
0	0.5 lines per frame
1	1 line per frame
2	1.5 lines per frame
3	2 lines per frame
. . .	. . .
4095 (0xFFF)	2048 lines per frame

3.4.2.2 Vertical Sync Low Time (VSEND) R/W

VSEND defines the duration of the Programmable Timing Generator (PTG) vertical sync pulse. The 5-bit value is the time vertical sync is low, in half lines. For RS170, Vsync is low for 3 lines. For CCIR Vsync is low for 2.5 lines.

Use the following formula to calculate VSEND:

VSEND = (number of lines in Vsync – 0.5) x 2

VSEND	Function
0	Vsync low = 0.5 line
1	Vsync low = 1 line
2	Vsync low = 1.5 lines
3	Vsync low = 2.0 lines
. . .	. . .
31 (0x1F)	Vsync low = 16 lines

3.4.2.3 Vertical Sync Polarity (VSYNCPOL) R/W

The VSYNCPOL bit defines the polarity of the vertical sync signal in internal timing mode (XTAL). The Vsync output on the camera connector can be disabled by the VSYNCEN bit (INCON2 register). This bit is “don’t care” in PLL modes.

VSYNCPOL	Function
0	Vsync is active low
1	Vsync is active high

3.4.2.4 E-Donpisha Mode Enable (EDONP) R/W

This bit enables the “E-Donpisha” or “Electronic Donpisha” mode, which changes the relationship between Vsync and Frame Reset, to control the camera shutter and integration time for E–Donpisha II cameras. The TIMEMD bits must select XTAL mode, SMODE must select non-interlaced, FRSTMD must enable Frame Reset mode, and the FRSTONV bit must enable Frame Reset output on the VSYSNC connection.

The PCVision*plus* frame reset line must be connected to the camera’s external trigger input. Following an external trigger input to the PCVision*plus*, the Frame Reset pulse drives the camera trigger. The length of the Frame Reset

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Pulse determines the camera's shutter speed. At the end of the Frame Reset pulse, the camera's VD (vertical drive) is driven after a fixed four-line period (integration) after which the camera outputs its frame image.

EDONP	Function
0	Normal operation (disable E–Donpisha)
1	Enable E-Donpisha

3.4.2.5 Vertical Error Status (VERROR) R-O

This status bit indicates that the camera or acquisition scan mode (SMODE) was changed from interlaced to non-interlaced, without the necessary adjustment to the VTOTAL value.

VERROR	Function
0	Normal operation
1	Error condition

3.4.3 PTG Vertical 2 (PTGV2) R/W

BADR2 + 0x0C

PCP_PTGB2_32

7							0
VGSTRT7	VGSTRT6	VGSTRT5	VGSTRT4	VGSTRT3	VGSTRT2	VGSTRT1	VGSTRT0
15							**8**
VGEND3	VGEND2	VGEND1	VGEND0	VGSTRT11	VGSTRT10	VGSTRT9	VGSTRT8
23							**16**
Reserved	Reserved	Reserved	Reserved	VGEND7	VGEND6	VGEND5	VGEND4
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The PTGV2 register defines the vertical gate region used when Frame Reset and VSYNC are both driven to a camera, from the PTG.

Bit	*Mnemonic*	*Function*
0–11	VGSTRT	Vertical Gate Start
12–19	VGEND	Vertical Gate End
20–31	Reserved	"Don't care"

3.4.3.1 Vertical Gate Start (VGSTRT) R/W

VGSTRT defines the start of a vertical gate region (VGATE), for the Programmable Timing Generator (PTG). The PTG vertical gate prevents a **frame reset** pulse from occurring during the vertical sync region. This is needed with some cameras, when operating in internal timing mode, and both Vsync and Frame Reset signals are driven to the camera. For some cameras, the image output is corrupted if the frame reset pulse occurs within the Vsync region. If a trigger occurs during the programmed VGATE region, the frame reset pulse is delayed until the PTG timing has exited the VSYNC region.

The 12-bit value is the interval between vertical sync low and the start of the vertical gate interval.

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The front porch region is the number of lines from the end of active video to the start of Vsync low. The RS170 front porch is 3 lines, and VGSTRT = 262.5 – 3 = 259.5. The CCIR front porch is 2.5 lines, and VGSTRT = 312.4 – 2.5 = 310.

Use the following formula to calculate VGSTRT for interlaced formats.

VGSTRT= (Total # lines per field – # lines in front porch – 0.5) x 2

Use the following formula to calculate VGSTRT for Non-interlaced formats:

VGSTRT= (# lines per frame – # lines in front porch – 0.5) x 2

VGSTRT	Function
0	Vgate start 0.5 lines after Vsync low
1	Vgate start 1 lines after Vsync low
2	Vgate start 1.5 lines after Vsync low
3	Vgate start 2.0 lines after Vsync low
. . .	. . .
4095 (0xFFF)	Vgate start 2048 lines after Vsync low

3.4.3.2 Vertical Gate End (VGEND) R/W

VGEND defines the duration of the Programmable Timing Generator (PTG) Vertical Gate interval. The 8-bit value is the time in half lines between vertical sync start and vertical gate end. Bit VGEND7 is always zero. Vertical gate is defined to prevent frame reset pulses from occurring during the vertical sync region of the camera. Refer to Figure 3–8.

For RS170, VGEND = 6 lines. For CCIR, VGEND = 5 lines.

Use the following formula to calculate VGEND:

VGEND = [(# lines from Vsync to end of Vgate region) – 0.5] x 2

VGEND	Function
0	VGATE Active 0.5 lines
1	VGATE Active 1.0 lines
2	VGATE Active 1.5 lines
3	VGATE Active 2.0 lines
. . .	. . .
127 (0x7F)	VGATE Active 64 lines

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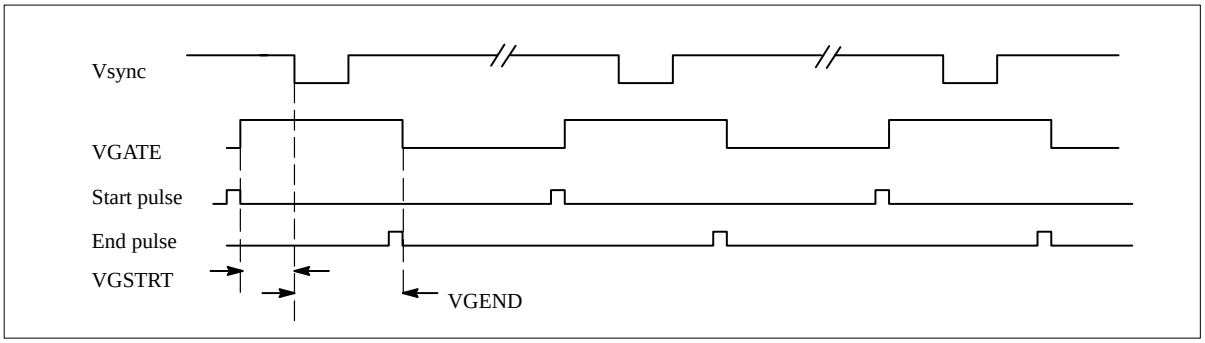


Figure 3–8. PTG Vertical Gate Generation

VGSTRT defines the start of the vertical gate region, and VGEND defines the end of the vertical gate region. This area is defined to prevent a frame reset from occurring within the vertical sync.

3.4.4 PWG Horizontal (PWGH) R/W

BADR2 + 0x10

PCP_PWGH_32

7							0
HOFF7	HOFF6	HOFF5	HOFF4	HOFF3	HOFF2	HOFF1	HOFF0
15							**8**
HACT5	HACT4	HACT3	HACT2	HACT1	HACT0	HOFF9	HOFF8
23							**16**
Reserved	Reserved	HACT11	HACT10	HACT9	HACT8	HACT7	HACT6
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The PWGH register defines the horizontal timing for the Programmable Window Generator (PWG).

Bit	*Mnemonic*	*Function*
0–9	HOFF	Horizontal Offset
10–21	HACT	Horizontal Active
22–31	Reserved	“Don’t care”

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3.4.4.1 Horizontal Offset (HOFF) R/W

HOFF defines the horizontal offset for the Programmable Window Generator (PWG). The 10-bit value determines the location of the first valid pixel of each line relative to the selected edge of the Hsync input. Hsync is defined by the programmed timing mode; XTAL or PLL. The PWG horizontal counter is loaded and enabled with the selected edge of LEN and will count until the last pixel is loaded into the memory frame. HOFF defines the count that starts loading memory. Refer to Chapter 2 “Programmable Window Generator” (starting on page 2–29) for details on the relationship of HOFF to HACT and Hsync.

Use the following formula to calculate HOFF:

HOFF = (number of pixels from LEN to active video) – 2

HOFF	Function
0	Start loading memory 1 pixel Clock after LEN edge
1	Start loading memory 2 pixel Clocks after LEN edge
2	Start loading memory 3 pixel Clocks after LEN edge
3	Start loading memory 4 pixel Clocks after LEN edge
. . .	. . .
1023 (0x3FF)	Start loading memory 1024 pixel Clocks after LENedge

3.4.4.2 Horizontal Active (HACT) R/W

HACT determines the amount of valid pixels in each horizontal line. The 12-bit value is the pixel count of the horizontal counter on which to stop loading the memory. The Programmable Window Generator (PWG) horizontal counter starts counting off the selected edge of Hsync. HACT determines the number of pixel clocks to stop loading the memory. When the counter stops, the EOL (end of line) is loaded. PCVision*plus* uses the EOL to determine the end of a horizontal line. The horizontal active region (HACT – HOFF) must be a whole multiple of 8.

Use the following formula to calculate HACT:

HACT = # pixels from LEN to end of desired active video region – 2

HACT	Function
0	End loading memory 1 pixel clock after LEN edge
1	End loading memory 2 pixel clocks after LEN edge
2	End loading memory 3 pixel clocks after LEN edge
3	End loading memory 4 pixel clocks after LEN edge
. . .	. . .
4095 (0xFFF)	End loading memory 4096 pixel clocks after LEN edge

NOTE *The number of active pixels must be divisible by 8.*
 # active pixels = (HACT +2) – (HOFF + 2)

Changing HOFF will change the active region loaded into the memory; therefore, you must compensate any change in HOFF by an equal amount in HACT. If you increase HOFF by 1 pixel, you must reduce the number of active pixels loaded into memory by 1. If the active region was previously divisible by 8, the 1 pixel change in offset causes the active to no longer be divisible by 8. Compensate for the change in HOFF by changing HACT to maintain the 8 pixel

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boundary. If the number of active pixels is not divisible by 8, the memory controller will acquire undesired pixels up to the next 8-pixel boundary.

3.4.5 PWG Vertical (PWGV) R/W

BADR2 + 0x14

PCP_PWGV_32

7							0
VOFF7	VOFF6	VOFF5	VOFF4	VOFF3	VOFF2	VOFF1	VOFF0
15							**8**
VACT5	VACT4	VACT3	VACT2	VACT1	VACT0	VOFF9	VOFF8
23							**16**
EXTRIG STAT1_26	EXTRIG STAT0_15	VACT11	VACT10	VACT9	VACT8	VACT7	VACT6
31							**24**
Reserved	Reserved	Reserved	DIFF STAT1	DIFF STAT0	OPTO STAT1	OPTO STAT0	EXTRIG STAT0_26

The PWGV register defines the vertical timing for the Programmable Window Generator (PWG).

Bit	*Mnemonic*	*Function*
0–9	VOFF	Vertical Offset
10–21	VACT	Vertical Active
22	EXTRIGSTAT0_15	15-pin TTL Trigger 0 Status
23	EXTRIGSTAT1_26	26-pin TTL Trigger 1 Status
24	EXTRIGSTAT0_26	26-pin TTL Trigger 0 Status
25	OPTOSTAT0	Opto-isolator Trigger 0 Status
26	OPTOSTAT1	Opto-isolator Trigger 1 Status
27	DIFFSTAT0	Differential Trigger 0 Status
28	DIFFSTAT1	Differential Trigger 1 Status
29–31	Reserved	“Don’t care”

3.4.5.1 Vertical Offset (VOFF) R/W

VOFF defines the vertical offset period for the Programmable Window Generator (PWG). The 10-bit value determines the first valid line of each frame relative to the selected edge of the FEN input.

The PWG vertical counter starts counting on the selected edge of FEN and stops counting and loading when the last line is loaded into the memory (defined by VACT). VOFF is the vertical count from the selected edge of FEN to the first valid line.

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Use the following formula to calculate VOFF:

VOFF = number of lines from FEN to the start of active video – 1

VOFF	Function
0	Start loading memory 1 line after FEN edge
1	Start loading memory 2 lines after FEN edge
2	Start loading memory 3 lines after FEN edge
3	Start loading memory 4 lines after FEN edge
. . .	. . .
1023 (0x3FF)	Start loading FIFO 1024 lines after Vsync edge

3.4.5.2 Vertical Active (VACT) R/W

VACT defines the number of valid lines loaded by the Programmable Window Generator (PWG). The 12-bit value is the vertical line count that stops loading data into the memory frame.

The PWG vertical counter starts counting on selected edge of FEN and stops counting and loading when the last line is loaded into the memory. VACT is the vertical count of the last valid line (stop counter). VOFF is the vertical count of the first valid line (start loading memory). The memory loads all lines between VOFF and VACT.

Use the following formula to calculate VACT. For interlaced images use number of lines per field and for non-interlaced use number of lines per frame.

VACT = # lines from FEN to the end of active video – 1

VACT	Function
0	End loading memory 1 line after FEN edge
1	End loading memory 2 lines after FEN edge
2	End loading memory 3 lines after FEN edge
3	End loading memory 4 lines after FEN edge
. . .	. . .
4095 (0xFFF)	End loading memory 4096 lines after FEN edge

3.4.5.3 15-Pin TTL Trigger 0 Status (EXTRIGSTAT0_15) R-O

This read only bit reflects the status of the TTL Trigger 0 input on the 15-pin video connector.

EXTRIGSTAT0_15	Status
0	Trigger input is 0
1	Trigger input is 1

3.4.5.4 TTL Trigger 1 Status (EXTRIGSTAT1) R-O

This read only bit reflects the status of the TTL Trigger 1 input on the 26-pin video connector.

EXTRIGSTAT1_26	Status
0	Trigger input is 0
1	Trigger input is 1

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3.4.5.5 15-Pin TTL Trigger 0 Status (EXTRIGSTAT0_15) R-O

This read only bit reflects the status of the TTL Trigger 0 input on the 26-pin video connector.

EXTRIGSTAT0_26	Status
0	Trigger input is 0
1	Trigger input is 1

3.4.5.6 Opto-Isolator Trigger 0 Status (OPTOSTAT0) R-O

This read only bit reflects the status of the Opto-isolator Trigger 0 input.

OPTOSTAT0	Status
0	Trigger input is 0
1	Trigger input is 1

3.4.5.7 Opto-Isolator Trigger 1 Status (OPTOSTAT1) R-O

This read only bit reflects the status of the Opto-isolator Trigger 1 input.

OPTOSTAT1	Status
0	Trigger input is 0
1	Trigger input is 1

3.4.5.8 Differential Trigger 0 Status (DIFFSTAT0) R-O

This read only bit reflects the status of the Differential Trigger 0 input.

DIFFSTAT0	Status
0	Trigger input is 0
1	Trigger input is 1

3.4.5.9 Differential Trigger 1 Status (DIFFSTAT1) R-O

This read only bit reflects the status of the Differential Trigger 1 input.

DIFFSTAT1	Status
0	Trigger input is 0
1	Trigger input is 1

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3.4.6 Input Control 1 (INCON1) R/W

BADR2 + 0x18

PCP_INCON1_32

7							0
WENMD	SKPFLDMD	TRIGCYC	TRIGPOL	TRIGSEL2	TRIGSEL1	TRIGSEL0	TRIGEN
15							**8**
STRBDLY3	STRBDLY2	STRBDLY1	STRBDLY0	STRBEN	STRBPOL	STRBMD	Reserved
23							**16**
FROFF1	FROFF0	FRSTONV	FRSTSZ	FRSTPOL	FRSTMD	STBDLY5	STRBDLY4
31							**24**
Reserved	TRIGMD	FROFF7	FROFF6	FROFF5	FROFF4	FROFF3	FROFF2

The INCON1 register controls trigger, strobe, and frame reset functions. All of these functions are associated with triggered acquisition.

Bit	*Mnemonic*	*Function*
0	TRIGEN	Trigger Enable
1–3	TRIGSEL	Trigger Source Select
4	TRIGPOL	Trigger Polarity Select
5	TRIGCYC	Trigger Cycle Status
6	SKPFLDMD	Skip Field Mode
7	WENMD	WEN Mode
8	Reserved	“Don’t care”
9	STRBMD	Strobe Mode Select
10	STRBPOL	Strobe Polarity Select
11	STRBEN	Strobe Output Enable
12–17	STRBDLY	Strobe Delay
18	FRSTMD	Frame Reset Mode Select
19	FRSTPOL	Frame Reset Polarity Select
20	FRSTSZ	Frame Reset Size
21	FRSTONV	Frame Reset on Vertical Sync Output Enable
22–29	FROFF	Frame Reset Offset Duration
30	TRIGMD	Trigger Mode
31	Reserved	“Don’t care”

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3.4.6.1 Trigger Enable (TRIGEN) R/W

This bit enables external trigger mode. The TRIGSEL bits select the software trigger or external input trigger pulse. The trigger remains enabled and ready for the next trigger input until disabled by writing a zero to this bit. The trigger input is ignored if a trigger cycle is currently in progress and TRIGMD disables the latch. If TRIGMD enables the latch, trigger signals occurring during a triggered acquire cycle are latched, and executed when the current cycle ends.

TRIGEN	Function
0	Trigger disabled
1	Trigger cycle enabled

3.4.6.2 Trigger Source Select (TRIGSEL) R/W

The three TRIGSEL bits define which of seven trigger signals begins a trigger cycle. PCVision*plus* has one software trigger, three TTL-level Schmidt Trigger inputs, two Opto-coupled trigger inputs, and one RS-422 differential trigger input. The status of all external trigger inputs is available in the PWGV register.

TRIGSEL	Selected trigger input
0	Software trigger
1	15-pin TTL trigger input 0
2	26-pin TTL trigger input 1
3	26-pin TTL trigger input 0
4	Opto-coupled trigger input 0
5	Opto-coupled trigger input 1
6	Differential trigger input 0
7	Differential trigger input 1

3.4.6.3 Trigger Polarity Select (TRIGPOL) R/W

This bit defines the polarity of the external trigger pulse input selected by the TRIGSEL bits. The trigger cycle begins on a positive going edge.

TRIGPOL	Function
0	External trigger pulse is active low (invert internally)
1	External trigger pulse is active high (no change)

Figure 3–9 illustrates the effect of this bit. Internally, the trigger is fired by the positive edge. In an active high signal, this is the leading edge. In an active low signal, the positive edge is the trailing edge. Programming TRIGPOL to zero causes the active low input to be inverted internally, so that the positive edge is the leading edge.

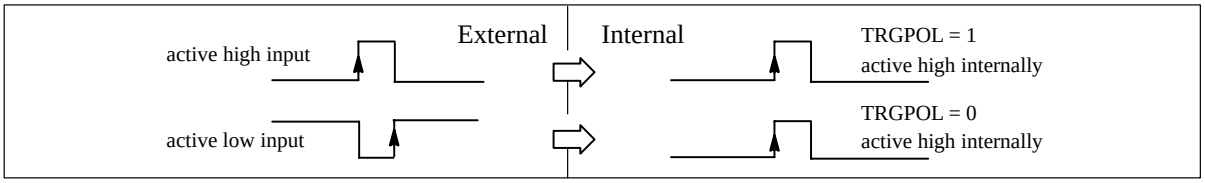


Figure 3–9. Trigger Polarity

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3.4.6.4 Trigger Cycle Status (TRIGCYC) R-O

This bit reflects the status of the trigger cycle.

TRGCYC	Function
0	No trigger cycle in progress
1	Trigger cycle in progress

3.4.6.5 Skip Field Mode (SKPFLDMD) R/W

This bit forces a triggered acquisition to skip one field after an external trigger cycle. The Programmable Window Generator (PWG) waits for one field before acquiring the number of fields indicated by the SMODE bit. This mode is useful with cameras that require a one field delay after a frame reset.

SKPFLDMD	Function
0	Disable skip field mode
1	Enable skip field mode

3.4.6.6 WEN Mode (WENMD) R/W

This bit enables a frame reset mode that uses the camera WEN input for vertical and ignores the vertical sync or vertical drive (VSYNC, VDrive or VD) output from the camera.

WENMD	Function
0	Disable WEN mode
1	Enable WEN mode

3.4.6.7 Strobe Mode Select (STRBMD) R/W

This bit selects fast strobe or slow strobe mode. The strobe pulse output is always one horizontal line duration.

In Fast Strobe mode, a 1-line strobe output pulse occurs immediately after the external trigger input starts the trigger cycle, if the trigger does not fire during the “no-strobe” region defined by the STRBDLY register. If the external trigger does occur during the no-strobe region, the strobe pulse is output at the end of the no-strobe region (strobe delay counter reaches zero).

In Slow Strobe mode, a 1-line strobe output pulse occurs after the programmed amount of lines defined by the STRBDLY register, after vertical sync.

STRBMD	Function
0	Fast strobe mode
1	Slow strobe mode

3.4.6.8 Strobe Polarity Select (STRBPOL) R/W

This bit selects the polarity of the strobe output. The strobe output driver is always enabled. If STRBEN disables the pulse output, the driver assumes the inactive state defined by this bit.

STRBPOL	Function
0	Strobe output active high pulse (low inactive)
1	Strobe output active low pulse (high inactive)

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3.4.6.9 Strobe Output Enable (STRBEN) R/W

This bit enables the strobe output during trigger cycles. The signal driver is always on; this bit disables the pulse generation internally. If the pulse output is disabled, the driver takes the “inactive” state defined by the STRBPOL bit (STROBEx pins are low if STRBEN is 1 and STRBPOL is 0).

STRBEN	Function
0	Enable strobe pulse output
1	Disable strobe pulse output

3.4.6.10 Strobe Delay (STRBDLY) R/W

STRBDLY defines the strobe delay count. The 6-bit value is loaded into the strobe delay line counter. STRBDLY determines when a strobe occurs in Slow Strobe mode, or when a strobe *does not* occur (the “no-strobe” region) in Fast Strobe mode.

In Slow Strobe Mode, the trigger input starts the strobe delay counter (and the vertical line counter). The strobe pulse is output when the line count reaches the 6-bit STRBDLY value (a number of lines after trigger). The duration of the strobe pulse is always one horizontal line.

In Fast Strobe Mode, VOFF starts the strobe delay counter. If a trigger occurs before the strobe delay counter reaches STRBDLY, the strobe output occurs when the strobe delay counter reaches the STRBDLY value (a number of lines after trigger). If the trigger occurs after the strobe delay counter reaches STRBDLY, the strobe pulse is output immediately after the trigger pulse input. The duration of the strobe pulse is always one horizontal line.

Use the following formula to calculate STRBDLY:

STRBDLY = number of lines to delay strobe – 1

STRBDLY	*Slow Strobe Mode*	*Fast Strobe Mode*
0	Strobe occurs 1 line after trigger	No-strobe ends 1 line after VOFF
1	Strobe occurs 2 lines after trigger	No-strobe ends 2 lines after VOFF
2	Strobe occurs 3 lines after trigger	No-strobe ends 3 lines after VOFF
3	Strobe occurs 4 lines after trigger	No-strobe ends 4 lines after VOFF
. . .	. . .	. . .
63 (0x3F)	Strobe occurs 64 lines after trigger	No-strobe ends 64 lines after VOFF

3.4.6.11 Frame Reset Mode Select (FRSTMD) R/W

The FRSTMD bit selects standard trigger cycle or frame reset trigger cycle. In frame reset mode, the Programmable Window Generator (PWG) is halted and waits in vertical blank. When the external trigger occurs, a frame reset pulse is sent to the camera, the PWG, and the PTG. This pulse resets the PTG into vertical sync. The FROFF value is loaded into the PWG for the first field of a frame reset cycle.

FRSTMD	Function
0	Frame Reset Disabled, standard trigger cycle
1	Frame Reset Enabled

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3.4.6.12 Frame Reset Polarity Select (FRSTPOL) R/W

This bit selects the polarity of the frame reset pulse output on the camera connector during a frame reset cycle. Program this bit to match the pulse polarity required by the camera in use. The length of the Frame Reset pulse is selected by the FRSTSZ bit.

FRSTPOL	Function
0	Frame reset pulse active high
1	Frame reset pulse active low

3.4.6.13 Frame Reset Size (FRSTSZ) R/W

The FRSTSZ bit determines the length of the frame reset pulse output to camera. The pulse duration can be one line, or the entire programmed FROFF time.

FRSTSZ	Function
0	Frame reset pulse is true for FROFF period
1	Frame reset pulse is one line

3.4.6.14 Frame Reset On Vertical Sync Output Enable (FRSTONV) R/W

The FRSTONV bit disables the VSYNC output, and directs the Frame Reset pulse onto the VSYNC output pin, in addition to the separate frame reset pin on the camera connector. Some cameras require the frame reset pulse occur on the vertical sync input line, not on a separate pin.

FRSTONV	Function
0	Vsync is vertical sync output
1	Vsync is Frame Reset output

3.4.6.15 Frame Reset Offset Duration (FROFF) R/W

FROFF defines a delay between the trigger pulse and the start of the Programmable Window Generator (PWG) counters. FROFF also defines the length of the frame reset pulse output to the camera when FRSTSZ=0. The 8-bit value is a number of lines to delay the counters. This delay count compensates for some additional delay between the time the frame reset pulse triggers and the time the camera enters its vertical blank region. Program FROFF to equal the expected additional line delay when using frame reset mode. The PWG counters are delayed the programmed number of lines in FROFF, for the first field of a frame reset cycle.

Use the following formula to calculate FROFF:

FROFF = number of lines to delay PWG count from trigger input – 1

FROFF	Function
0	Delay PWG count 1 line after receiving trigger
1	Delay PWG count 2 lines after receiving trigger
2	Delay PWG count 3 lines after receiving trigger
3	Delay PWG count 4 lines after receiving trigger
. . .	. . .
255 (0xFF)	Delay PWG count 256 lines after receiving trigger

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3.4.6.16 Trigger Mode (TRIGMD) R/W

The TRIGMD bit enables a trigger latch. With the latch disabled, additional triggers that occur during a triggered acquisition are ignored. With the latch enabled, triggers that occur during a triggered acquisition are latched, and another triggered acquire begins immediately following completion of the current triggered acquire cycle.

TRIGMD	Function
0	Disable latch; ignore triggers if a triggered acquisition cycle is in progress
1	Enable latch; latch triggers if a triggered acquisition cycle is in progress

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3.4.7 Input Control 2 (INCON2) R/W

BADR2 + 0x1C

PCP_INCON2_32

7							0
VSCLK SEL	VIDEO INSEL	LPFSEL	TIMEMD2	TIMEMD1	TIMEMD0	DACCS	PLLCS
15							**8**
VSYNCEN	FLDSHFT	FLDSEL	FLDPOL	FENPOL	LENPOL	VCLKPOL	OVRSM
23							**16**
MISCIN2	MISCIN1	MISCIN0	MISCOUT2	MISCOUT1	MISCOUT0	VSCANTST	SMODE
31							**24**
Reserved	Reserved	Reserved	Reserved	ILUT SADR3	ILUT SADR2	ILUT SADR1	ILUT SADR0

The INCON2 register selects the timing mode, input signal conditioning, and controls the output timing signals.

Bit	*Mnemonic*	*Function*
0	PLLCS	PLL Chip Select
1	DACCS	DAC Chip Select
2–4	TIMEMD	Timing Mode Select
5	LPFSEL	Low-Pass Filter Select
6	VIDEOINSEL	Video Input Select
7	VSCLKSEL	VSCAN Clock Select
8	OVRSM	Oversample Input Mode Select
9	VCLKPOL	Variable Scan Clock Input Polarity
10	LENPOL	Line Enable Input Polarity Select
11	FENPOL	Frame Enable Input Polarity Select
12	FLDPOL	Field Input Polarity Select
13	FLDSEL	Field Source Select
14	FLDSHFT	Field Shift Mode
15	VSYNCEN	Vertical Sync Output Enable
16	SMODE	Input Scan Mode Select
17	VSCANTST	VSCAN Test Mode
18–20	MISCOUT	Miscellaneous Outputs
21–23	MISCIN	Miscellaneous Inputs
21–23	ILUTSADR	Input LUT Static Address
24–31	Reserved	“Don’t care”

3.4.7.1 PLL Chip Select (PLLCS) R/W

This bit enables programming the PLL registers. Refer to “PLL Programming” in Chapter 4 for details.

PLLCS	Function
0	PLL in program mode
1	PLL in normal operation mode

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3.4.7.2 DAC Chip Select (DACCS) R/W

This bit enables programming the DAC registers. Refer to “DAC Programming” in Chapter 4 for details.

DACCS	Function
0	DAC in program mode
1	DAC in normal operation mode

3.4.7.3 Timing Mode Select (TIMEMD) R/W

These three bits define the timing mode to be external timing (PLL), Internal (XTAL), or Variable Scan (VSCAN). These bits also define the sync inputs used, and the pixel clock source. The TIMEMD bits define the timing input to the PWG; either the PTG Hsync and Vsync in XTAL mode, or the stripped sync or separate sync inputs in PLL mode. In XTAL mode the sync output drivers are enabled to drive the PTG sync outputs to a camera. Make sure the cables are connected properly prior to setting a channel in XTAL mode. CAM0 and CAM1 have separate CLK and Frame Reset pins. If VSCLKSEL=0, the clock is input on the CLKIN0 and CLKIN1 pins. If VSCLKSEL=1, the clock is input on the FRESET0 and FRESET1 pins.

TIMEMD	Function
0	PLL Mode 0: sync stripper on camera selected by VIDEOINSEL; strip H, V, and Field from composite video
1	PLL Mode 1: CAM0 separate H & V sync inputs, FLDSEL selects field
2	PLL Mode 2: CAM1 separate H & V sync inputs, FLDSEL selects field
3	Reserved
4	XTAL Mode: Internal PTG created H, V, and Field
5	VSCAN Mode 0: CAM0 timing inputs
6	VSCAN Mode 1: CAM1 timing inputs
7	Reserved

3.4.7.4 Low-Pass Filter Select (LPFSEL) R/W

The LPFSEL bit selects the low pass filter. Two filters are available; there is no bypass.

LPFSEL	Function
0	6.5 MHz low-pass filter
1	12.5 MHz low-pass filter

3.4.7.5 Video Input Select (VIDEOINSEL) R/W

The VIDEOINSEL bit selects between CAM0 and CAM1 input.

VIDEOINSEL	Function
0	CAM0 selected
1	CAM1 selected

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3.4.7.6 VSCAN Clock Input Select (VSCLKSEL) R/W

In variable scan mode, the clock can be input on the CLKIN0 and CLKIN1 pins, or on the FRESET0 and FRESET1 pins. This added flexability allows support for some of the camera adapter cables developed for the earlier PCVision frame grabber.

VSCLKSEL	Function
0	Clock input on CLKIN inputs
1	Clock input on FRESET inputs

3.4.7.7 Oversample Input Mode Select (OVRSM) R/W

The OVRSM bit defines the data input to the Input LUT as one 12-bit pixel from the ADC with four static page select bits, or two 8-bit pixels, odd and even, made from 12-bit data with the 4 lsbs (least significant bits) truncated. To perform oversampling, program the pixel clock to twice the normal sample rate and program the Input LUT to average the two adjacent pixel values.

OVRSM	Function
0	Normal mode: 12-bit pixels and 4 page bits
1	Oversample mode: two 8-bit odd and even pixels

3.4.7.8 Variable Scan Clock Input Polarity Select (VCLKPOL) R/W

The VCLKPOL bit can invert the incoming variable scan clock when PCVision*plus* is in variable scan mode. Internal circuits sample the video signal on the rising edge of the clock. If your camera uses a falling edge clock, enable the invert.

VCLKPOL	Function
0	Disable invert (do not invert clock input)
1	Enable invert (invert the clock input)

3.4.7.9 Line Enable Input Polarity Select (LENPOL) R/W

This bit selects which edge of the LEN input enables the PWG horizontal counter, starting horizontal window generation. Program this bit to zero for XTAL and PLL modes. Only use this bit to invert the LEN input for VSCAN modes.

LENPOL	Function
0	Falling edge enables horizontal timing
1	Rising edge enables horizontal timing

3.4.7.10 Frame Enable Input Polarity Select (FENPOL) R/W

The FENPOL bit selects which edge of the FEN input enables the PWG vertical counter, starting vertical window generation. Program this bit to zero for XTAL and PLL modes. Only use this bit to invert the FEN input for VSCAN modes.

FENPOL	Function
0	Falling edge enables vertical timing
1	Rising edge enables vertical timing

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3.4.7.11 Field Polarity Input Select (FLDPOL) R/W

The FLDPOL bit defines the polarity of the selected field output from the PWG (for interlaced images only) in VSCAN mode and separate sync input PLL mode. The convention used here is, Field=0 is an Even field, and Field=1 is an Odd field. This FLDPOL bit allows compensation for other standards by inverting the field input. This bit should be zero for XTAL mode and stripped sync PLL mode.

FLDPOL	Function
0	Field input low is Odd field or second field
1	Field input low is Even field or first field

3.4.7.12 Field Source Select (FLDSEL) R/W

The FLDSEL bit selects the field source in variable scan mode and in the separate sync input PLL modes. If the video signal has composite sync, use the stripper to extract the field information. “Generated field” comes from comparing the separate TTL sync inputs or LEN and FEN. The field is even (low) when Vsync/FEN occurs coincident with Hsync/LEN, and odd (high) when Vsync/FEN occurs without Hsync/LEN (during the active video half line). Vsync/FEN must be greater than two horizontal line times to use generated field mode.

FLDSEL	Function
0	Sync stripper field
1	Generated field

3.4.7.13 Field Shift Mode (FLDSHFT) R/W

This bit enables the PWG Field Shift mode, which allows cropping of the 1/2 lines output with some standard interlaced video formats (RS170 and CCIR). This mode is only available for either of the stripped sync PLL modes or XTAL mode. Separate Sync PLL mode and VSCAN mode are not supported in Field Shift mode. This mode is not used for non-interlaced video.

FLDSHFT	*PLL RS170*	*PLL CCIR*	*All XTAL Modes*
0	Crop 1/2 line mode	Normal mode	Crop 1/2 line mode
1	Normal mode	Crop 1/2 line mode	Normal mode

3.4.7.14 Vertical Sync Output Enable (VSYNCEN) R/W

The VSYNCEN bit enables or disables the vertical sync output driver when XTAL mode is selected. This bit should be disabled in PLL mode.

VSYNCEN	Function
0	VSYNC output disabled
1	VSYNC output enabled

3.4.7.15 Input Scan Mode Select (SMODE) R/W

The SMODE bit selects interlaced or non-interlaced camera input mode. This bit flags the image memory address controller for the video format.

SMODE	Function
0	Interlaced video format
1	Non-interlaced video format

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3.4.7.16 VSCAN Test Mode (VSCANTST) R/W

This bit enables a diagnostic test mode. Applications should not enable this bit.

VSCANTST	Function
0	Normal mode
1	VSCAN Test mode

3.4.7.17 Misc Output (MISCOUT2, MISCOUT1, MISCOUT0) R/W

These three bits control output drivers for the external outputs (MISC_IO_OUT2, MISC_IO_OUT1, MISC_IO_OUT0) on the video connectors. Each output is driven high or low, as defined by these bits. MISC_IO_OUT2 is located on the 15-pin connector. MISC_IO_OUT1 and MISC_IO_OUT0 are located on the 26-pin connector.

MISCOUTx	Function
0	OUTx is low
1	OUTx is high

3.4.7.18 Misc Input (MISCIN2, MISCIN1, MISCIN0) R-O

These three bits reflect the current state of the external inputs (MISC_IO_IN2, MISC_IO_IN1, MISC_IO_IN0) on the video connectors. MISC_IO_IN2 is located on the 15-pin connector. MISC_IO_IN1 and MISC_IO_IN0 are located on the 26-pin connector.

MISCINx	Status
0	INx is low
1	INx is high

3.4.7.19 Input LUT Static Address (ILUTSADR) R/W

The four ILUTSADR bits are the four msb (most significant bits) of the input LUT address in 12-bit input mode, when the OVRSM bit is zero (normal mode). These bits are ignored if the OVRSM bit is one (oversample mode).

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3.4.8 AM Interrupt Status (AMINTCLR) R/W1C

BADR2 + 0x20

PCP_AM_INTCLR_32

7							0
Reserved	VBODD INTSTAT	VBEVEN INTSTAT	VBLANK INTSTAT	TCNTINT STAT	PIOINT STAT	EOTINT STAT	SOTINT STAT
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register provides status on, and clears, the interrupts from the acquisition module, timer, and parallel I/O port.

Bit	*Mnemonic*	*Function*
0	SOTINTSTAT	Start of Trigger Cycle Interrupt Status
1	EOTINTSTAT	End of Trigger Cycle Interrupt Status
2	PIOINTSTAT	Programmable I/O Interrupt Status
3	TCNTINTSTAT	Timer Interrupt Status
4	VBLANKINTSTAT	Vertical Blank Interrupt Status
5	VBEVENINTSTAT	Vertical Blank Odd Field Interrupt Status
6	VBODDINTSTAT	Vertical Blank Even Field Interrupt Status
7–31	Reserved	“Don’t care”

3.4.8.1 Start of Trigger Cycle Interrupt Status (SOTINTSTAT) R/W1C

This bit reflects the status of the “Start of Trigger” interrupt. This interrupt is enabled by the SOTINTEN bit in the AM Interrupt Control register (AMINTEN). Writing one to this status bit clears the interrupt request.

SOTINTSTAT	Status
0	No interrupt request
1	Start of Trigger interrupt request pending

3.4.8.2 End of Trigger Cycle Interrupt Status (EOTINTSTAT) R/W1C

This bit reflects the status of the “End of Trigger” interrupt. This interrupt is enabled by the EOTINTEN bit in the AM Interrupt Control register (AMINTEN). Writing one to this status bit clears the interrupt request.

EOTINTSTAT	Status
0	No interrupt request
1	End of Trigger interrupt request pending

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3.4.8.3 Programmable I/O Interrupt Status (PIOINTSTAT) R/W1C

This bit reflects the status of the Parallel Port interrupt input. This interrupt is enabled by the PIOIEN bit in the AM Interrupt Control register (AMINTEN). Writing one to this status bit clears the interrupt request.

PIOINTSTAT	Status
0	No interrupt request pending
1	Parallel Port interrupt request pending

3.4.8.4 Timer Interrupt Status (TCNTINSTAT) R/W1C

This bit reflects the status of the Timer interrupt. This interrupt is enabled by the TCNTINTEN bit in the AM Interrupt Control register (AMINTEN). Writing one to this status bit clears the interrupt request.

TCNTINTSTAT	Status
0	No interrupt request pending
1	Timer interrupt request pending

3.4.8.5 Vertical Blank Interrupt Status (VBLANKINTSTAT) R/W1C

This bit reflects the status of the Vertical Blank interrupt. This interrupt is enabled by the VBLANKINTEN bit in the AM Interrupt Control register (AMINTEN). Writing one to this status bit clears the interrupt request.

VBLANKINTSTAT	Status
0	No interrupt request pending
1	Vertical blank interrupt request pending

3.4.8.6 Vertical Blank Even Field Interrupt Status (VBEVENINTSTAT) R/W1C

This bit reflects the status of the Vertical Blank Even Field interrupt. This interrupt is enabled by the VBEVENINTEN bit in the AM Interrupt Control register (AMINTEN). Writing one to this status bit clears the interrupt request.

VBEVENINTSTAT	Status
0	No interrupt request pending
1	Vertical blank even field interrupt request pending

3.4.8.7 Vertical Blank Odd Field Interrupt Status (VBODDINTSTAT) R/W1C

This bit reflects the status of the Vertical Blank Odd Field interrupt. This interrupt is enabled by the VBODDINTEN bit in the AM Interrupt Control register (AMINTEN). Writing one to this status bit clears the interrupt request.

VBODDINTSTAT	Status
0	No interrupt request pending
1	Vertical blank odd field interrupt request pending

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3.4.9 AM Interrupt Control (AMINTEN) R/W

BADR2 + 0x24

PCP_AM_INTEN_32

7							0
Reserved	VBODD INTEN	VBEVEN INTEN	VBLANK INTEN	TCNT INTEN	PIOINTEN	EOTINTEN	SOTINTEN
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register controls the external interrupt sources: triggers, timing, and the I/O port.

Bit	Mnemonic	Function
0	SOTQIEN	Start of Trigger Interrupt Enable
1	EOTQIEN	End of Trigger Interrupt Enable
2	PIOIEN	Parallel I/O Port Interrupt Enable
3	TCNTINTEN	Timer Count Interrupt Enable
4	VBLANKINTEN	Vertical Blank Interrupt Enable
5	VBEVENINTEN	Vertical Blank Even Field Interrupt Enable
6	VBODDINTEN	Vertical Blank Odd Field Interrupt Enable
7–31	Reserved	“Don’t care”

3.4.9.1 Start of Trigger Interrupt Enable (SOTINTEN) R/W

This bit enables an interrupt that occurs at the start of a triggered acquisition. The input polarity is defined by the TRIGPOL bit. If enabled, an interrupt is set and latched *at the transition* of the external trigger input that causes a triggered acquisition. The status and clear bit for this register is SOTINTSTAT, in the AMINTCLR register. This interrupt source is only active if TRIGEN enables trigger operation, and fires prior to the trigger cycle start.

SOTIEN	Function
0	Disable Start Of Trigger interrupt
1	Enable Start Of Trigger interrupt

3.4.9.2 End of Trigger Interrupt Enable (EOTINTEN) R/W

This bit enables an interrupt that occurs at the end of a triggered acquisition. If enabled, an interrupt is set and latched at the completion of the triggered acquire cycle. The status and clear bit for this interrupt is EOTINTSTAT, in the AMINTCLR register.

EOTIEN	Function
0	Disable End Of Trigger interrupt
1	Enable End Of Trigger interrupt

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3.4.9.3 Input Port Interrupt Enable (PIOIEN) R/W

The PIOIEN bit enables the interrupt input bit on the input port. The input is edge triggered. The polarity is selected by the IPINTPOL bit. The status and clear bit for this interrupt is PIOINTSTAT, in the AMINTCLR register.

PIOIEN	Function
0	Disable interrupt input
1	Enable interrupt input

3.4.9.4 Timer Count Interrupt Enable (TCNTINTEN) R/W

The TCNTINTEN bit enables an interrupt that occurs when the timer count reaches zero. The status and clear bit for this interrupt is TCNTINTSTAT, in the AMINTCLR register.

TCNTINTEN	Function
0	Disable timer interrupt
1	Enable timer interrupt

3.4.9.5 Vertical Blank Interrupt Enable (VBLANKINTEN) R/W

The VBLANKINTEN bit enables an interrupt that occurs when the PWG vertical blank signal goes low, indicating the start of the PWG vertical blank region defined by the VOFF and VACT register values. The status and clear bit for this interrupt is VBLANKINTSTAT, in the AMINTCLR register.

VBLANKINTEN	Function
0	Disable PWG Vertical Blank interrupt
1	Enable PWG Vertical Blank interrupt

3.4.9.6 Vertical Blank Even Field Interrupt Enable (VBEVENINTEN) R/W

The VBEVENINTEN bit enables an interrupt that occurs when the PWG vertical blank signal goes low, and the PWG field signal is low. The field signal low indicates an even field. Vertical blank going low indicates the start of the PWG vertical blank region defined by the VOFF and VACT register values. The status and clear bit for this interrupt is VBEVENINTSTAT, in the AMINTCLR register.

VBEVENINTEN	Function
0	Disable PWG Vertical Blank Even Field interrupt
1	Enable PWG Vertical Blank Even Field interrupt

3.4.9.7 Vertical Blank Odd Field Interrupt Enable (VBODDINTEN) R/W

The VBODDINTEN bit enables an interrupt that occurs when the PWG vertical blank signal goes low, and the PWG field signal is high. The field signal high indicates an odd field. Vertical blank going low indicates the start of the PWG vertical blank region defined by the VOFF and VACT register values. The status and clear bit for this interrupt is VBODDINTSTAT, in the AMINTCLR register.

VBEVENINTEN	Function
0	Disable PWG vertical blank odd field interrupt
1	Enable PWG vertical blank odd field interrupt

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3.4.10 Software Trigger (SOFTTRIG) W-O

BADR2 + 0x28

PCP_SOFTTRIG_32

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
15							8
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
23							16
DATA23	DATA22	DATA21	DATA20	DATA19	DATA18	DATA17	DATA16
31							24
DATA31	DATA30	DATA29	DATA28	DATA27	DATA26	DATA25	DATA24

Writing any value to this register starts a triggered acquire cycle when TRIGEN is enabled and TRIGSEL selects software trigger. This register is write only.

3.4.11 Programmable Clamp (PCLAMP) R/W

BADR2 + 0x2C

PCP_PCLAMP_32

7							0
BPSTRT6	BPSTRT5	BPSTRT4	BPSTRT3	BPSTRT2	BPSTRT1	BPSTRT0	CLMPSRC
15							8
BPEND7	BPEND6	BPEND5	BPEND4	BPEND3	BPEND2	BPEND1	BPEND0
23							16
NO CLAMP7	NO CLAMP6	NO CLAMP5	NO CLAMP4	NO CLAMP3	NO CLAMP2	NO CLAMP1	NO CLAMP0
31							24
Reserved	Reserved	Reserved	CNTEN SRC	NO CLAMP11	NO CLAMP10	NO CLAMP9	NO CLAMP8

This register contains bits to control the clamp pulse generator used for DC restoration of the incoming video. The sync stripper clamp is only available for PLL mode. Programmable clamp is recommended for all modes because it gives a better clamp response time.

Bit	*Mnemonic*	*Function*
0	CLMPSRC	Clamp Pulse Source
1–7	BPSTRT	Back Porch Start Position
8–15	BPEND	Back Porch End Position
16–27	NOCLAMP	No Clamp Region
28	CNTENSRC	Clamp Counter Enable Source
29–31	Reserved	“Don’t care”

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3.4.11.1 Clamp Pulse Source (CLAMPSRC) R/W

The CLAMPSRC bit determines which clamp pulse performs the DC restoration. The programmable clamp pulse is recommended for variable scan (VSCAN) and internal timing (XTAL) modes. The sync stripper clamp pulse is usually only available for PLL mode. You can use the sync stripper if a composite sync signal is available with the variable scan timing or from a camera using internal timing.

CLMPSRC	Function
0	Sync Stripper Clamp Pulse
1	Programmable Clamp Pulse

3.4.11.2 Back Porch Start Position (BPSTRT) R/W

The seven BPSTRT bits define the start of the programmable clamp pulse, used for DC restoration (clamping) during the “back porch” of the video signal. The start of the clamp pulse is a number of clocks from the beginning of the Hsync pulse (falling edge of HSYNC, assuming an active low horizontal sync). The 14.318 MHz crystal in the Frequency Synthesizer (PTG) drives the programmable clamp counters. The CNTENSRC bit in this register selects which Hsync enables the clamp position counters: Sync Stripper timing or timing selected by the TIMEMD bits. The value of BPEND must be greater than the value of BPSTRT.

The start and end count positions must not fall within the worst case margins for the external video variance and the internal circuit. Every camera or video source has slightly different timing, and calculations must accommodate the worst case possibilities. Refer to the RS170 and CCIR signal specifications for the margins of error for the actual positions of the front porch and back porch. There is a fixed delay of three clock periods from the falling edge of Hsync to the start of the back porch counters. Re-syncing of the PCVision*plus* internal circuitry adds a margin of error of one clock period of the crystal clock (69.84 ns) used to control the clamp circuit.

BPSTRT	Typical Start Position	Worst Case Start Position
0	(3 + 0) x 69.84 ns	(4 + 0) x 69.84 ns
1	(3 + 1) x 69.84 ns	(4 + 1) x 69.84 ns
2	(3 + 2) x 69.84 ns	(4 + 2) x 69.84 ns
. . .	. . .	. . .
127	(3 + 127) x 69.84 ns	(4 + 127) x 69.84 ns

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3.4.11.3 Back Porch End Position (PBEND) R/W

The eight BPEND bits define the end of the programmable clamp pulse, used for DC restoration (clamping) during the “back porch” of the video signal. The end of the clamp pulse is a number of clocks from the falling edge of HSYNC (assuming an active low horizontal sync). The 14.318 MHz crystal in the Frequency Synthesizer (PTG) drives the programmable clamp counters. The CNTENSRC bit in this register selects which Hsync enables the clamp position counters. The value of BPEND must be greater than the value of BPSTRT.

BPEND	Typical End Position	Worst Case End Position
0	(3 + 0) x 69.84 ns	(4 + 0) x 69.84 ns
1	(3 + 1) x 69.84 ns	(4 + 1) x 69.84 ns
2	(3 + 2) x 69.84 ns	(4 + 2) x 69.84 ns
. . .	. . .	. . .
127	(3 + 127) x 69.84 ns	(4 + 127) x 69.84 ns

3.4.11.4 No Clamp Region (NOCLAMP) R/W

The twelve NOCLAMP bits define the End of the Clamping Region, or the Start of a “No Clamping” Region, from the end of the Vsync pulse (rising edge of VSYNC, assuming an active low vertical sync). The CNTENSRC bit in this register selects which Vsync enables the clamp position counters: Sync Stripper timing or timing selected by the TIMEMD bits. Use the Sync Stripper timing for standard RS170 and CCIR video sources.

The “No Clamping” region disables clamping during the serration and Equalization region of the video signal on interlaced video. Program NOCLAMP to the number of lines from the end of the Vsync pulse (rising edge) to the start of the serration region or the video source (round down the the nearest half line). The Clamping circuit automatically detects the end of the serration region and turns clamping back on.

NOCLAMP	Clamping Duration	Start of No-Clamp Region
0	1 line	1 line from Vsync end
1	2 lines	2 lines from Vsync end
2	3 lines	3 lines from Vsync end
. . .	. . .	. . .
4095	4096 lines	4096 lines from Vsync end

3.4.11.5 Clamp Counter Enable Source (CNTENSRC) R/W

The CNTENSRC selects the timing source that enables the Clamping counters for Back Porch Start and End, Front Porch Start and End, and the No Clamping Region. Use the Sync Stripper timing for standard RS170 and CCIR video sources.

CNTENSRC	Function
0	Sync Stripper Hsync and Vsync
1	Separate Sync inputs or PTG, selected by TIMEMD bits

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3.4.12 PLL Programming Port (PLLPROG) R/W

BADR2 + 0x34

PCP_PLLPROG_32

7							0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PLLSDATA
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register is the serial data port for the programmable Phase-Locked Loop (PLL).

3.4.12.1 PLL Serial Data (PLLSDATA) R/W

The PLLSDATA bit is the serial data input and output to the PLL registers. The PLL is accessed through a serial programming interface. Data is programmed using this register and the PLLCS bit in the INCON2 register. The PLL registers and programming examples appear in Chapter 4.

3.4.13 DAC Programming Port (DACPROG) R/W

BADR2 + 0x38

PCP_DACPROG_32

7							0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DACSDATA
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register is the serial data port for the four programmable DACs. These DACs control the ADC Reference Voltages, Clamping Voltage, and Sync Stripper frequency range.

3.4.13.1 DAC Serial Data (DACSDATA) R/W

The DACSDATA bit is the serial data input to the DAC registers. The DACs are accessed through a serial programming interface. Data for each 13-bit DAC must be programmed 1 bit at a time using this register and the DACCS bit in the INCON2 register. Refer to “DAC Programming” in Chapter 4.

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3.4.14 Timer Counter (TIMER) R/W

BADR2 + 0x3C

PCP_TIMER_32

7							0
CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
15							8
CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8
23							16
CNT23	CNT22	CNT21	CNT20	CNT19	CNT18	CNT17	CNT16
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register controls a general purpose 24-bit down-counter. The counter is clocked by the PCI-bus clock, divided by 4 (33 MHz/4 = 8.25 MHz). If the PCI-bus clock is 33 MHz, the counter range is approximately 2 seconds. Reading this register gives the current count value.

Bit	*Mnemonic*	*Function*
0–23	TIMERCNT	Timer Count
24–31	Reserved	“Don’t care”

3.4.14.1 Timer Count (TIMERCNT) R/W

The TIMERCNT bits define a starting value for the down counter. Writing to this register immediately loads a new value into the counter, and the count continues from that value. The down counter is clocked by the PCI-bus clock divided by four (33 MHz/4 = 8.25 MHz). The resolution is 121 nanoseconds (ns). The maximum count is approximately two seconds. The counter wraps from 0x000000 to 0xFFFFFF. The counter wraps from zero to 0xFFFFFF. An interrupt is generated when the counter reaches zero, if the interrupt is enabled by the TCNTINTEN bit (AMINTEN register). Reading this register gives the current count value. Software can subtract the read value from the written value to time events.

TIMERCNT	Down-count interval
0	121 ns
1	242 ns
2	363 ns
. . .	. . .
0xFFFFFF	2 seconds

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3.4.15 Parallel IO Port Control (PORTCON) R/W

BADR2 + 0x40

PCP_PORTCON_32

7							0
Reserved	STRBIN STAT	INTINSTAT	INPORT IPOL	INREGCLR	INSTRBPOL	INREGENB	OUTSTB
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register controls the functions of the parallel input and output port. Reserved bits always read zero.

Bit	Mnemonic	Function
0	OUTSTB	Output Port Strobe
1	INREGENB	Input Buffer Enable
2	INSTRBPOL	Input Port Strobe Polarity
3	INREGCLR	Input Port Buffer Clear
4	IPINTPOL	Input Port Interrupt Polarity
5	INTINSTAT	Input Port Interrupt Input Status
6	STRBINSTAT	Input Port Strobe Input Status
7–31	Reserved	“Don’t care”

3.4.15.1 Output Port Strobe (OUTSTB) R/W

This bit determines the state of the Output Port Strobe signal (STROBE_O). This bit is cleared during power up and system reset.

OUTSTB	Function
0	Strobe output pin driven low
1	Strobe output pin driven high

3.4.15.2 Input Buffer Enable (INREGENB) R/W

This bit enables the input port buffer. With the buffer enabled, the input strobe clocks the state of the input pins into the input port buffer, and the Input Port register INPORT reads the data in the buffer. With the buffer disabled, the input strobe has no effect, and the Input Port register INPORT reads the state of the input pins directly. This bit is cleared during power up and system reset.

INREGENB	Function
0	Disable input buffer and strobe; INPORT reads input pins
1	Enable input buffer and strobe; INPORT reads buffer data

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3.4.15.3 Input Port Strobe Polarity (INSTRBPOL) R/W

This bit defines which edge of the input strobe clocks data into the input buffer. This bit is ignored if INREGENB is zero. This bit is cleared during power up and system reset.

INSTRBPOL	Function
0	Rising edge clocks data into buffer
1	Falling edge clocks data into buffer

3.4.15.4 Input Buffer Clear (INREGCLR) R/W

This bit clears the input port buffer. This bit forces the buffer contents to zero. This bit is cleared during power up and system reset.

INREGCLR	Function
0	Enabled; normal operation
1	Cleared; all zeros

3.4.15.5 Input Port Interrupt Polarity (IPINTPOL) R/W

This bit defines the edge used to register an interrupt input on the parallel port. The PIOIEN bit enables the interrupt. This bit is cleared during power up and system reset.

IPINTPOL	Function
0	Rising edge trigger
1	Falling edge trigger

3.4.15.6 Input Port Interrupt Input Status (INTINSTAT) R-O

This bit shows the current state of the interrupt pin (IO_INT) on the parallel connector. This bit is read only.

INTINSTAT	Status
0	Low input
1	High input

3.4.15.7 Input Port Strobe Input Status (STRBINSTAT) R-O

This bit reflects the current state of the strobe input pin (STROBE_I), on the input port connector.

STRBINSTAT	Status
0	STROBE_I input is low
1	STROBE_I input is high

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3.4.16 PIO Output Port (OUTPORT) R/W

BADR2 + 0x44

PCP_OUTPORT_32

7							0
OUTP7	OUTP6	OUTP5	OUTP4	OUTP3	OUTP2	OUTP1	OUTP0
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The eight bits in this register define the values applied to the Output Port data pins. Reading this register shows the state of the output port data buffer, not the actual output pins. This register is cleared during power up and system reset.

3.4.17 PIO Input Port (INPORT) R-O

BADR2 + 0x48

PCP_INPORT_32

7							0
INP7	INP6	INP5	INP4	INP3	INP2	INP1	INP0
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The eight bits in this register indicate either the state (level) of the Input Port pins, or the state of the input port data buffer. The INREGENB bit selects which location is read. The reserved bits in this register always read zero.

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3.4.18 Alpha Control (ALPHA) R/W

BADR2 + 0x4C

PCP_ALPHA_32

7							0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
15							**8**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							**16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register must be initialized to zero for normal operation of the PCVision*plus* image memory. Application programs must not write to this register.

3.4.19 LUT Programming

BADR2 + 0x40000–0x7FFFF

Low LUT Word Access

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
15							**8**
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
23							**16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The Input LUT is a 16-bit in 16-bit out Look-Up Table. The 16-bit data written to this register is stored in the LUT. The bit order is reversed at the LUT input. ADC output bit 11 is connnected to LUT input bit 0. The Oversample Enable bit (OVRSM) controls the input LUT configuration, which has a great affect on how the LUT is programmed. The Input Data Format bit (INMODE) controls how data is read from the LUT output, and packed and stored in the image memory. The LUT must compensate for the data input format, bit ordering, and both OVRSM and INMODE values.

With OVRSM=0 (oversample disabled), the Input LUT provides sixteen pages for 16-bit input addressing: 12 bits from the ADC and four page select bits, as shown in Figure 3–10. You can load up to 16 different 12-bit data transforms and use the page select bits ILUTSADR (input LUT static address) to change transforms without reloading.

With INMODE=1 (12-bit input mode) all 16 LUT output bits are read and stored as a WORD in the image buffer memory, as shown in Figure 3–10. The LUT can be programmed for any point transformation, normalization, or data shift. The user must be aware that the Bus Master Controller pad, zoom, decimate and byte shift modes assume valid pixel data is positioned on bits 11 through 0. Bits 15 through 12 are usually treated as “don’t care” values, but may be useful as tag values.

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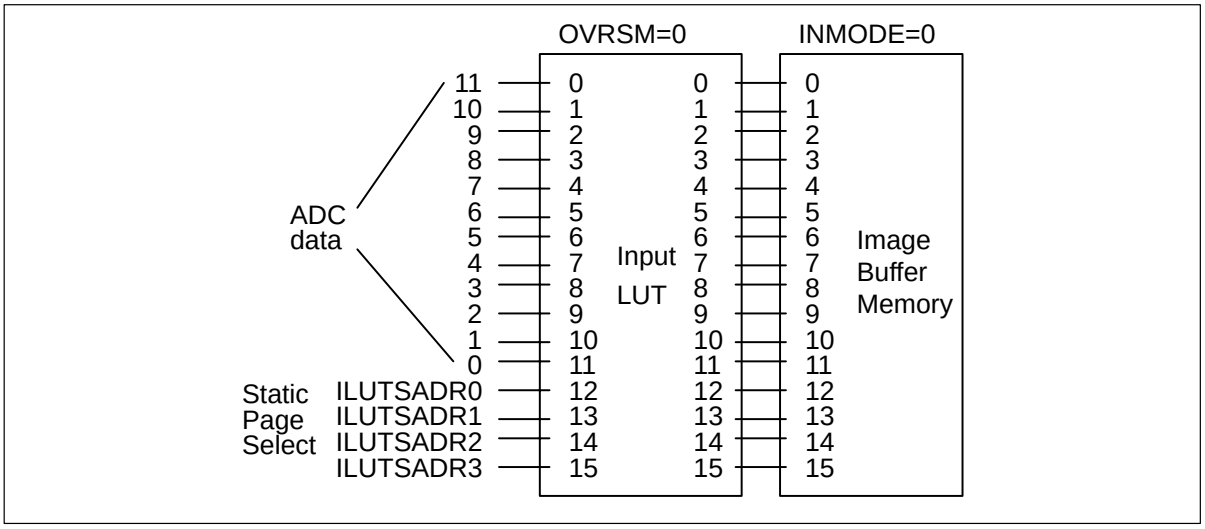


Figure 3–10. Input LUT 12-bit Mode

With OVRSM=1 (oversample enabled), the Input LUT provides one page for 16-bit input addressing, and there are no page select bits available, as shown in Figure 3–11. You can load only one transform. If you are not oversampling the pixel data, program the LUT to ignore the high byte input (delayed pixel) by repeating the same data pattern. If you are oversampling, program the LUT to average the values input on the two address bytes.

With INMODE=0 (8-bit input mode) LUT output bits 11 through 4 are stored as a BYTE in the image buffer memory, as shown in Figure 3–11. Bits 15 through 12 are discarded, and bits 3 through 0 are discarded.

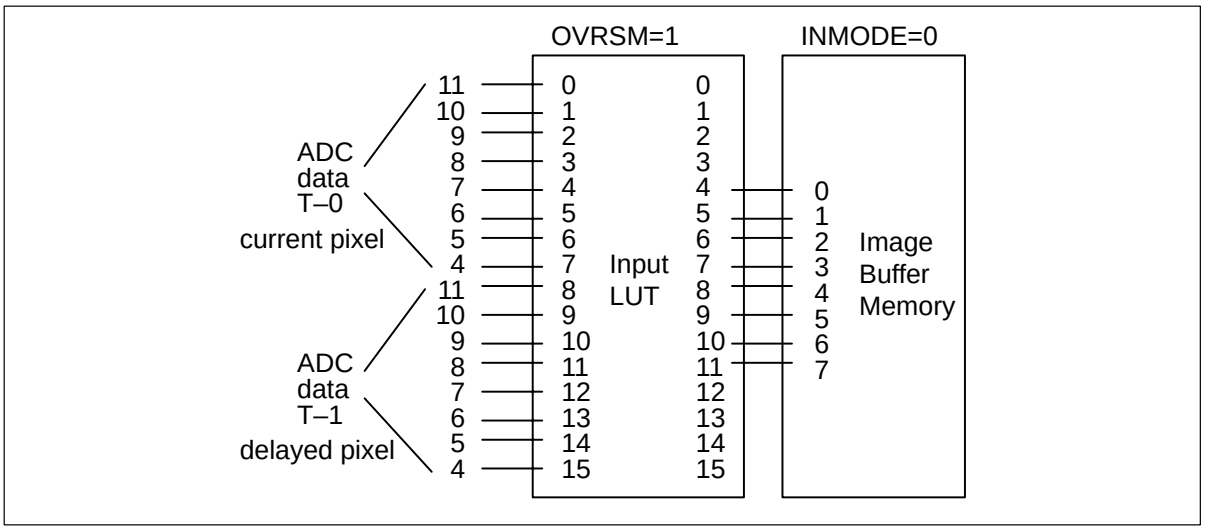


Figure 3–11. Input LUT Oversample Mode

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3.5 FRAME BUFFER CONTROL REGISTERS

These registers control data acquisition into the frame buffer memory. This 1MB group of addresses is organized into four 64K DWORD areas: Frame Control registers, Output Control Table, Scatter Gather (or DMA) Table, AMCC Add-on registers. The Frame Buffer Control registers are mapped into system address space starting at the address in the BADR3 register. Figure 3–12 shows the register map for the Frame Buffer Control registers.

BADR3 +		*Page #*
0x00	Acquisition Control (ACQREG)	3–64
0x04	*Reserved*	
0x08	*Reserved*	
0x0C	*Reserved*	
0x10	Bus Master Control (BMCTLX)	3–68
0x14	Memory Initialization (MEMINIT)	3–71
0x18	Acquisition Start Address (ACQSTRT)	3–72
0x1C	Acquire Interrupt Line (ACQLINEINT)	3–73
0x20	Segment Size (SGSZ)	3–74
0x24	OCT Start Address (OCTSTART)	3–75
0x28	Interrupt Status (INTSTAT)	3–75
0x2C	Interrupt Control (INTENREG)	3–77
0x30	Acquire Address (ACQADR)	3–78
0x30–0x3FFFF	*Reserved*	
0x40000–0x7FFFF	Output Control Table	3–79
0x80000–0xBFFFF	Scatter Gather Table	3–81
0xC0000	Add-On Interrupt Control (AINT)	3–82
0xC0004	Add-On General Control (AGCSTS)	3–83
0xC0008	Manual Destination Address (MDSTADR)	3–83
0xC000C	Manual Transfer Count (MXCNT)	3–84
0xC0010–0xFFFFF	*Reserved*	

Figure 3–12. Frame Buffer Control Register Map

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3.5.1 Acquisition Control (ACQREG) R/W

BMADR3 + 0x00

PCP_ACQREG_32

7							0
Reserved	Reserved	FLDSEL1	FLDSEL0	FCNT2	FCNT1	FCNT0	ACQADR RST
15							**8**
AMFLD STAT	AMVB STAT	PREVFLD START	FLDSTART	GSTAT	NEWAQ	ACQMD1	ACQMD0
23							**16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	INMODE1	INMODE0
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register controls and provides status on the memory acquire port.

Bit	Mnemonic	Function
0	ACQADRRST	Acquire Address Reset
1–3	FCNT	Frame Count
4–5	FLDSEL	Starting Field Select
6–7	Reserved	“Don’t care”
8–9	ACQMD	Acquire Command
10	NEWAQ	New Acquire
11	GSTAT	Grab Status
12	FLDSTART	Field Start Status
13	PREVFLDSTART	Previous Field Start Status
14	AMVBSTAT	Acquisition Vertical Balnk Status
15	AMFLDSTAT	Acquisition Field Status
16–17	INMODE	Input Data Format
18–31	Reserved	“Don’t care”

3.5.1.1 Acquire Address Reset (ACQADRRST) R/W

The ACQADRRST bit affects the operation of the acquire address generator at at the end of frame or frame count acquires. When this bit is zero (normal operation), the acquire address is reloaded with the value set in the ACQ-START register at the end of FCNT acquired frames. When this bit is one, the ACQSTART address is only reloaded when the ACQMD bits are set. This bit works with grab mode to acquire large frame and multiple frame images.

ACQADRRST	Function
0	Reload (reset) acquire address at the end of frame count
1	No reset at the end of every frame count

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3.5.1.2 Frame Count (FCNT) R/W

The three FCNT bits determine the number of images stored in memory after each acquire command (snap, grab, or triggered acquire). The FCNT bits allow up to eight images. The image size also determines the number of images that will fit into a 4MB memory frame.

FCNT	Function
0	Acquire 1 image
1	Acquire 2 images
. . .	. . .
7	Acquire 8 images

A snap command or triggered snap acquires FCNT number of images and stops. A grab command or triggered grab stores FCNT images before wrapping back to the acquire start address and continuing to acquire.

3.5.1.3 Starting Field Select (FLDSEL) R/W

The two FLDSEL bits determine which field of an interlaced image will begin the acquire cycle. Program FLDSEL to zero for non-interlaced images.

FLDSEL1	FLDSEL0	Function
0	0	Start acquire on next field
0	1	Reserved
1	0	Start acquire on next even field
1	1	Start acquire on next odd field

3.5.1.4 Acquire Command (ACQMD) R/W

The two ACQMD bits initiate the various camera acquisition modes into image memory, and also indicate when an acquisition has ended.

ACQMD	Function
0	Freeze (stop acquire)
1	*Invalid*
2	Snap (single frame acquire)
3	Grab (continuous acquire)

These bits change immediately when they are written, however they are sampled with vertical blank or trigger. The start of an acquire is sampled at the end of vertical blank and the end of an acquire is sampled at the beginning of vertical blank. An acquire starts at the end of the next vertical blank.

If the two ACQMD bits are both 1, the acquire will be continuous *grab*. During a *grab* the ACQMD bits will be read back as a 3 until either a snap or freeze command is issued.

If the ACQMD bits are programmed to 2, the acquire will be a single frame *snap*. During a *snap* the ACQMD bits will be read back as a 2 until the acquisition is complete. Non-interlaced acquisition completes at the start of next vertical blank. Interlaced acquisition completes at the start of the second vertical blank.

A *freeze* command will terminate an acquisition at the start of the next vertical blank. After a freeze command the ACQMD bits will be read back as 0 immediately, however the acquire will not actually end until the start of the next

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vertical blank. It is recommended that the *grab* status bit GSTAT in this register be monitored to determine when the acquisition is complete.

3.5.1.5 New Acquire (NEWAQ) R-O

This bit is set to one whenever a snap or grab command is written to the ACQMD bits and is cleared automatically when acquisition begins.

NEWAQ	Function
0	No acquire pending
1	Acquire pending

3.5.1.6 Grab Status (GSTAT) R-O

This bit provides acquisition status. When using the frame count bits (FCNT) to acquire multiple frames, the acquire command bits (ACQMD) should be used to monitor the status of the acquire. The grab status bit GSTAT is set only during the active portion of vertical blank for multi-frame acquires and therefore should not be used to determine acquire status.

GSTAT	Function
0	No acquire in progress
1	Acquire in progress

3.5.1.7 Field Start Status (FLDSTART) R-O

This status bit reflects which field an interlaced acquisition started on.

FLDSTART	Function
0	Acquire started on even field
1	Acquire started on odd field

3.5.1.8 Previous Field Start Status (PREVFLDSTART) R-O

This bit latches the state of the FLDSTART bit at the time the end of field interrupt is set. This bit is useful in multiple frame acquires, to track the field status of more than one frame.

PREVFLDSTART	Function
0	Acquire started on even field
1	Acquire started on odd field

3.5.1.9 Acquisition Vertical Blank Status (AMVBSTAT) R-O

The AMVBSTAT bit reflects status of the vertical blank from the AM interface, used to frame the video input to memory.

AMVBSTAT	Function
0	In vertical blank
1	Not in vertical blank

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3.5.1.10 Acquisition Field Status (AMFLDSTAT) R-O

The AMFLDSTAT bit reflects the current field of the video input from the AM interface, used to a frame the video input to memory.

AMFLDSTAT	Function
0	Even field
1	Odd field

3.5.1.11 Input Data Format (INMODE) R/W

The two INMODE bits define the data format of the image and how data is packed and stored in the image memory. The 8-bit modes store data as four bytes or four pixels per DWORD. In 8-bit mode, the Input LUT must be programmed to output pixel data on bits 11–4 out of the LUT. Bits 15–12 and 3–0 of the LUT output are ignored in 8-bit mode. In 12-bit mode, all 16 bits of the LUT output are stored. The application can program the LUTs for any data shift or normalization; however the Bus Master Controller pad, zoom, decimate and byte shift modes assume valid pixel data is positioned on bits 11–0. See also to “LUT Programming” on page 3–61.

INMODE	Function
0	8-bit mode: store bits 11–4
1	12-bit mode: store bits 16–0
2	Reserved
3	Reserved

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3.5.2 Bus Master Control (BMCTLX) R/W

BADR3 + 0x010

PCP_BMCTLX_32

7							0
SCANDIR	CLIPEN	PADEN	BMZOOM1	BMZOOM0	BMBYTE SEL	BMSHIFT	BMEN
15							**8**
DMA START7	DMA START6	DMA START5	DMA START4	DMA START3	DMA START2	DMA START1	DMA START0
23							**16**
Reserved	DMA START14	DMA START12	DMA START12	DMA START11	DMA START10	DMA START9	DMA START8
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register enables bus master transfer of image memory data, and controls the formatting.

Bit	Mnemonic	Function
0	BMEN	Bus Master Enable
1	BMSHIFT	Bus Master Data Shift Enable
1	BMBYTESEL	Bus Master Byte Lane Select
3–4	BMZOOM	Bus Master Zoom
5	PADEN	Pad Enable
6	CLIPEN	Clip Enable
7	SCANDIR	Bus Master Scan Direction
8–22	DMASTART	DMA Table Start Address
23–31	Reserved	“Don’t care”

3.5.2.1 Bus Master Enable (BMEN) R/W

The BMEN bit enables the bus master port for a memory data transfer onto the PCI-bus. BMEN should be disabled prior to changing any of the other bus master settings, to avoid affecting a current bus master operation. This bit must be zero during host read or write access to the image memory buffer.

BMEN	Function
0	Disable Bus Master port
1	Request a transfer to the BMC

3.5.2.2 Bus Master Data Shift Enable (BMSHIFT) R/W

The BMSHIFT bit is only valid in 12-bit input mode (INMODE=1). This bit has no effect in 8-bit mode. In 12-bit mode, enabling this bit left-shifts the input data by four bit positions. Bit 11 of the input data gets shifted into bit position 15. Bit 0 of the input data gets shifted into bit position 4. This is also called “normalizing to 16 bits.” The 4 lsbs (least significant bits) are don’t care after the shift. This bit is ignored if BMZOOM = 0x03 or if PADEN is enabled.

BMSHIFT	Function
0	Disable shift
1	Enable shift: left-shift 4

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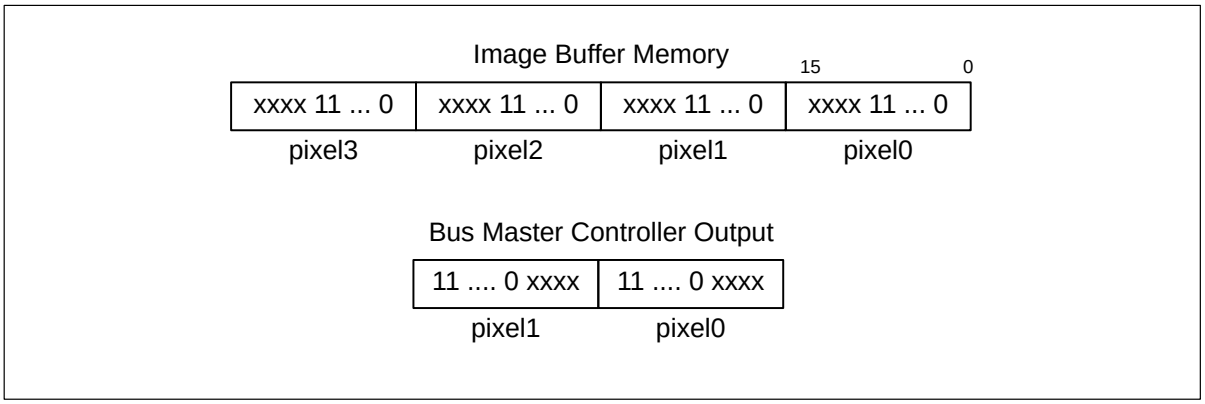


Figure 3–13. Bus Master Data Shift

3.5.2.3 Bus Master Byte Select (BMBYTESEL) R/W

The BMBYTESEL bit is only valid in 8-bit input mode (INMODE=0) with “decimate by 2” mode (BMZOOM = 0x3). This bit has no effect in 12-bit mode, or if BMZOOM is not 0x03. This bit selects the even or odd pixel for decimation.

BMBYTESEL	Function
0	Transfer even pixels, decimate odd
1	Transfer odd pixels, decimate even

3.5.2.4 Bus Master Zoom (BMZOOM) R/W

Two BMZOOM bits select the output data zoom factor. Zoom factor forces pixel replication in the horizontal direction. In 8-bit mode each BYTE is replicated. In 12-bit mode each WORD is replicated. The data stored in the frame memory buffer is not affected by BMZOOM. The bus master Transfer Count must be adjusted for the zoom factor. Double the transfer count for zoom by 2. Multiply the transfer count by four for zoom by 4. Half the transfer count for decimate by 2. Refer to Chapter 2 for additional discussion and illustrations.

BMZOOM	Function
0	Zoom by 1 (normal)
1	Zoom by 2
2	Zoom by 4
3	Decimate by 2

Decimate by 2 can be used in both 8-bit and 12-bit modes. In 8-bit mode every second pixel is dropped. The BMBYTESEL bit selects the odd or even pixel for decimation. In 12-bit mode decimate by 2 is used to convert 12-bit pixels into 8-bit pixels, to reduce the transfer size or for 8-bit display. In 12-bit mode, decimate by 2 packs pixel data bits 11–4 in each adjacent bytes in the bus master controller’s output data path (four different values; not replicated). The effect is a right-shift by 4 places. Data bits 15–12 and 3–0 are ignored. The data stored in the image memory is not changed. Only the transferred data is modified. The BMSHIFT bit is ignored if decimate by 2 is selected. This is a

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separate, automatic right-shift of 12-bit data. BMSHIFT is a left-shift. In both 8-bit and 12-bit modes, the transfer count should be half the original image value in bytes.

A 1024 pixel line of 12-bit pixels occupies 2048 bytes or 512 DWORDs in image memory. The transfer count should be 512 DWORDs if no decimation occurs. The transfer count should be 256 DWORDs if decimate by 2 is enabled.

3.5.2.5 Pad Mode Enable (PADEN) R/W

The PADEN bit enables pad mode for bus master cycles. Pad mode modifies data bytes in the Bus Master FIFO. The BMC inserts a byte of 0x80 in every other pixel location as data is passed to the PCI-bus. This mode is useful when displaying 8-bit monochrome image data on the 16-bit secondary (or YCrCb) surface (leaving the primary surface for Windows and Overlay).

In 8-bit mode (8-bit image data in the frame memory), the zoom factor (BMZOOM bits) must be programmed to "zoom by 2" or "zoom by 4" when using pad mode, and the transfer count must be multiplied by 2 or 4, to account for the extra data added to the image. Zoom by 2 doubles the image data sent to the bus master controller, and padding replaces the second (replicated) copy of each pixel with 0x80 in the upper byte of each WORD in the FIFO. Zoom by 4 with pad mode produces a padded zoom by 2 (horizontal) image.

In 12-bit mode, the pixel data is left-shifted by 4 and stored in the low byte of each WORD of the FIFO, and 0x80 stored in the upper byte of each WORD. BMSHIFT and Decimate by 2 are not used with PADEN in 12-bit mode. This is a separate and independent shift. Refer to Chapter 2 for additional discussion and illustrations.

PADEN	Function
0	Disable pad mode
1	Enable pad mode

3.5.2.6 Clip Mode Enable (CLIPEN) R/W

The CLIPEN bit enables clip mode for bus master cycles. Clip mode modifies data bytes in the Bus Master FIFO. Any pixel value between 0x00 and 0x0F is forced to 0x10 and any value between 0xF0 and 0xFF is forced to 0xEF. Clipping these pixel value ranges allows for direct image transfer to a VGA display without seeing color dots.

CLIPEN	Function
0	Disable clipping
1	Enable clipping

3.5.2.7 Bus Master Scan Direction (SCANDIR) R/W

The SCANDIR bit defines the direction or order for reading data from the DWORD memory location to the DWORD FIFO in the Bus Master Controller (BMC).

SCANDIR	Function
0	Normal forward scan
1	Reverse scan

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3.5.2.8 DMA Start Address (DMASTART) R/W

The 15 bit DMASTART address defines the first DMA Table address location used in a bus master transfer. The DMA Table address range is 0 to 32767 (or 0x7FFF).

DMASTART	Function
0	Start address = 0
1	Start address = 1
. . .	. . .
32767 or 0x7FFF	Start address = 0x7FFF (or 32767)

3.5.3 Memory Initialization (MEMINIT) W-O

BADR3 + 0x14

PCP_MEMINIT_32

7							0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
15							**8**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							**16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register must be written once after a file download to the FPGAs.

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3.5.4 Acquisition Start (ACQSTRT) R/W

BMADR3 + 0x18

PCP_ACQSTRT_32

7							0
ADDR14	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8	ADDR7
15							**8**
Reserved	ADDR21	ADDR20	ADDR19	ADDR18	ADDR17	ADDR16	ADDR15
23							**16**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The acquire start address bits determine the first address in a memory frame for writing or storing an acquired image. The acquire start address is programmable on 128-byte boundaries. If the image acquire reaches the maximum memory address (0x7FFF DWORDs), the acquire wraps back to zero. The acquired image size must be on 8-byte (2 DWORD) boundaries; or 16-byte boundaries in horizontal sub-sample by 2. The remaining locations of the last 8-byte write will be filled with garbage data to satisfy the 8-byte boundary.

ACQSTRTADDR	Acquire Start Address
0x0	0x0 (DWORD address)
0x1	0x00080
0x2	0x00100
. . .	. . .
0x7FFE	0x3FFF00
0x7FFF	0x3FFF80

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3.5.5 Acquire Line Interrupt (ACQLINEINT) R/W

BMADR3 + 0x1C

PCP_ACQ_LINE_INT_32

7							0
INTADR14	INTADR13	INTADR12	INTADR11	INTADR10	INTADR9	INTADR8	INTADR7
15							**8**
LSBMASK0	INTADR21	INTADR20	INTADR19	INTADR18	INTADR17	INTADR16	INTADR15
23							**16**
Reserved	Reserved	Reserved	Reserved	Reserved	LSBMASK3	LSBMASK2	LSBMASK1
31							**24**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register controls the acquire line interrupt address.

Bit	*Mnemonic*	*Function*
0–14	INTADR	Acquire Interrupt Address
15–18	LSBMASK	Interrupt Address LSB Mask
19–31	Reserved	“Don’t care”

3.5.5.1 Acquire Interrupt Address (INTADR) R/W

The 12-bit Acquire Interrupt Line Address (INTADR) held in this register define a memory line address that causes an interrupt when the image acquire writes to this address. The interrupt must be enabled by the ALINEINTEN bit in the ACQREG register (one for each memory frame). The interrupt is also controlled by the BMC. The LSBMASK bits change the resolution of this address. The interrupt address is programmed on 64 DWORD (256 byte) boundaries when the LSBMASK is zero (no masking).

INTADR	Acquire interrupt address
0x0	0x00000
0x1	0x00040
0x2	0x00080
. . .	. . .
0xFFE	0x3FF80
0xFFF	0x3FFC0

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3.5.5.2 Interrupt Address LSB Mask (LSBMASK) R/W

The four LSBMASK bits enable masking the lower order bits in the Acquire Interrupt Address. Masking changes the resolution of the acquire line interrupt. Only the settings shown below are valid. A higher order bit can only be masked off if all lower bits are also masked off.

LSBMASK	Function
0x0	No mask; 256 byte resolution
0x1	Mask off INTADR0; 512 byte resolution
0x3	Mask off INTARD1 and INTADR0; 1024 byte resolution
0x7	Mask off INTADR(2–0); 2048 byte resolution
0xFF	Mask off INTADR(3–0); 4096 byte resolution

3.5.6 Segment Size (SGSZ) R/W

BMADR3 + 0x20

PCP_SGSZ_32

7							0
SGSZ7	SGSZ6	SGSZ5	SGSZ4	SGSZ3	SGSZ2	SGSZ1	SGSZ0
15							8
Reserved	SGSZ14	SGSZ13	SGSZ12	SGSZ11	SGSZ10	SGSZ9	SGSZ8
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register defines the number of valid destination entries (descriptor pairs) defined in the DMA Table. The DMA Table can hold up to 32K descriptors. A bus master transfer always begins at the start location defined by the DMA Start Address in the BMCTLX register.

SGSZ	Function
0	Process 1 DMA Table entry during transfer
1	Process 2 DMA Table entries during transfer
. . .	. . .
0x7FF	Process 32K DMA Table entries during transfer

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3.5.7 OCT Start Address (OCTSTART) R/W

BADR3 + 0x24

PCP_OCT_START_32

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The 16-bit OCT Start Address (OCTSTARTADR) defines the first OCT address location used in a bus master transfer. The OCT address range is 0 to 65535 (0xFFFF).

OCTSTART	Function
0	Start address = 0
1	Start address = 1
. . .	. . .
0xFFFF	Start address = 0xFFFF

3.5.8 Interrupt Status (INTSTAT) R/W1C

BMADR3 + 0x28

PCP_INTSTAT_32

7							0
Reserved	Reserved	Reserved	Reserved	EOFINT STAT	AMINT STAT	BMINT STAT	ACQLINE INTSTAT
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register provides status and clear bits for all PCVision*plus* interrupt sources.

Bit	Mnemonic	Function
0	ACQLINEINTSTAT	Acquire Line Interrupt Status
1	BMINTSTAT	Bus Master Complete Interrupt Status
2	AMINTSTAT	AM Interrupt Status
3	EOFINTSTAT	End of Frame Interrupt Status
4–31	Reserved	“Don’t care”

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3.5.8.1 Acquire Line Interrupt Status (ACQLINEINTSTAT) R/W1C

The ACQLINEINTSTAT bit indicates an image acquire has occurred to the memory address programmed in the ALINEINT register. The interrupt source is enabled by the ALINEINTEN bit in the INTENREG register. Read this bit to check the status. Write one to this bit to clear the interrupt request. Writing zero to this bit has no effect.

ACQLINEINTSTAT	Read Status	Write Command
0	No interrupt	No effect
1	Acquire line interrupt request	Clear interrupt request

3.5.8.2 Bus Master Complete Interrupt Status (BMINTSTAT) R/W1C

The BMINTSTAT bit indicates an interrupt is posted from completion of a bus master operation. Write one to this bit to clear the interrupt request. Writing zero to this bit has no effect.

BMINTSTAT	Read Status	Write Command
0	No interrupt	No effect
1	Bus master interrupt request	Clear interrupt request

3.5.8.3 AM Interrupt Status (AMINTSTAT) R/W1C

The AMINTSTAT bit indicates an interrupt is posted from AMINTCLR. Writing one to this bit clears the interrupt request in the BMC, but does not clear the cause of the interrupt. AM interrupts are cleared in the AMINTCLR register. Write one to this bit to clear the interrupt request.

AMINTSTAT	Read Status	Write Command
0	No interrupt	No effect
1	AM interrupt request	Clear interrupt request

3.5.8.4 End of Frame Interrupt Status (EOFINTSTAT) R/W1C

The EOFINTSTAT bit indicates the completion of an image acquire into a memory frame. The interrupt source is enabled by EOFINTEN in the INTENREG register. Write one to this bit to clear the interrupt request. Writing zero to this bit has no effect.

EOFINTSTAT	Read Status	Write Command
0	No interrupt	No effect
1	EOF interrupt request	Clear interrupt request

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3.5.9 Interrupt Control (INTENREG) R/W

BMADR3 + 0x2C

PCP_INTENREG_32

7							0
Reserved	Reserved	Reserved	Reserved	EOFINTEN	AMINTEN	BMINTEN	ACQLINE INTEN
15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register enables interrupt requests to the host. All interrupts are ORed together on a single PCI-bus interrupt line.

Bit	Mnemonic	Function
0	ACQLINEINTEN	Acquire Line Interrupt Enable
1	BMINTEN	Bus Master Complete Interrupt Enable
2	AMINTEN	Acquisition Module Interrupt Enable
3	EOFINTEN	End of Frame Interrupt Enable
4–31	Reserved	“Don’t care”

3.5.9.1 Acquire Line Interrupt Enable (ACQLINEINTEN) R/W

The ACQLINEINTEN bit enables an interrupt that occurs when the acquire operation writes to the line address equal to the contents of the ALINEINT register for a memory frame. The interrupt gets latched in the BMC Interrupt Status register INTSTAT for arbitration and processing.

ACQLINEINTEN	Function
0	Disable acquire line interrupt
1	Enable acquire line interrupt

3.5.9.2 Bus Master Complete Interrupt Enable (BMINTEN) R/W

The BMINTEN bit enables an interrupt that occurs when a bus master operation from memory completes. The interrupt gets latched in the BMC Interrupt Status register INTSTAT for arbitration and processing.

BMINTEN	Function
0	Disable bus master coomplete interrupt
1	Enable bus master complete interrupt

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3.5.9.3 Acquisition Module Interrupt Enable (AMINTEN) R/W

This bit enables AM interrupt sources to post an interrupt to the PCI Controller. The interrupts are enabled in AMINTEN and cleared in AMINTCLR.

AMINTEN	Function
0	Disable AM interrupts
1	Enable AM interrupts

3.5.9.4 End of Frame Interrupt Enable (EOFINTEN) R/W

The EOFINTEN bit enables the end of an acquire operation to cause an interrupt. The interrupt gets latched in the BMC Interrupt Status register INTSTAT. The End of Frame occurs immediately after a frame is acquired into a memory buffer. In multiple frame modes, EOFINT will set for every frame of the multiple frame acquire operation.

EOFINTEN	Function
0	Disable EOF interrupt
1	Enable EOF interrupt

3.5.10 Acquire Address (ACQADR) R-O

BMADR3 + 0x30

PCP_ACQADR_32

7							0
ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8	ADR7
15							8
Reserved	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16	ADR15
23							16
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register provides status of the current PCVision*plus* memory acquire address.

ACQADR	Acquire Address
0x0	0x0 (DWORD address)
0x1	0x00080
0x2	0x00100
. . .	. . .
0x7FFE	0x3FFF00
0x7FFF	0x3FFF80

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3.5.11 Output Control Table (OCTDATA) R/W

BADR3 + 0x40000–0x7FFFC

OCTDATA

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
XCNT3	XCNT2	XCNT1	XCNT0	Reserved	ADR18	ADR17	ADR16
31							24
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

The Output Control Table (OCT) controls how data is read from the frame buffer memory.

Bit	Mnemonic	Function
0–18	ADR	Start Address
19	Reserved	“Don’t care”
20–23	XCNT	Transfer Count
24–31	Reserved	“Don’t care”

3.5.11.1 Start Address (ADR) R/W

The 19-bit start address supports image buffers up to 4MB. This address does not wrap at the 4MB size of the PCVision*plus* image memory. Addresses over 4MB (0x7FFFF) will attempt to address non-existing memory. The PCVision*plus* image memory is partitioned into 2048-byte pages. An OCT entry must access data within a single 2048-byte page. Page boundary crossing is not allowed during a bus master transfer.

ADR	Function
0	ADR = 0
1	ADR = DWORD 1
2	ADR = DWORD 2
. . .	. . .
0x7FFFC	ADR = DWORD 7FFFC, or 4MB – 1 DWORD

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3.5.11.2 Transfer Count (XCNT) R/W

The four XCNT bits define the transfer count for the data block defined by this pointer. The transfer count is the number of DWORDs to transfer before going to the next OCT entry. Programming XCNT greater than 1024K DWORDs (0x00100000) transfers more than the entire 4MB memory frame. For example, programming XCNT to 2048K DWORDs transfers the entire memory frame twice. The PCVision*plus* image memory is partitioned into 2048-byte pages. An OCT entry must access data within a single 2048-byte page. Page boundary crossing is not allowed during a bus master transfer.

DATA	Function
0	Not valid
1	XCNT = 1 DWORD
2	XCNT = 2 DWORDs
. . .	. . .
0xF	XCNT =16 DWORDs (64 bytes)

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3.5.12 Scatter Gather Table (DPDATA) R/W

BADR3 + 0x80000–0xBFFFC

DPDATA

7							0
DPDATA7	DPDATA6	DPDATA5	DPDATA4	DPDATA3	DPDATA2	DPDATA1	DPDATA0
15							8
DPDATA15	DPDATA14	DPDATA13	DPDATA12	DPDATA11	DPDATA10	DPDATA9	DPDATA8
23							16
DPDATA23	DPDATA22	DPDATA21	DPATAT20	DPDATA19	DPDATA18	DPDATA17	DPDATA16
31							24
DPDATA31	DPDATA30	DPDATA29	DPDATA28	DPDATA27	DPDATA26	DPDATA25	DPDATA24

The Bus Master Controller uses the scatter gather table to define a destination buffer for bus master transfers to the PCI-bus. The table contains destination pointers. Each pointer takes two DWORD locations in the scatter gather table. The even addresses contain PCI-bus destination addresses. The odd addresses contain transfer count values. The Segment Size register (SGSZ) defines how many of these destination pointers are used in a bus master transfer operation. The DMASTART address in the BMCTLX register define the first destination pointer used for a data transfer. Once the BMEN bit is set, the BMC loads the Transfer Count and Destination Address information form the Scatter Gather Table and sends data to the host buffer defined.

BMADR3+		
0x80000	DSTADR 0	32-bit destination start address
0x80004	XCNT 0	transfer count
0x80008	DSTADR 1	32-bit destination start address
0x8000C	XCNT 1	transfer count
. . .	. . .	
0xBFFF8	DSTADR 32767	32-bit destination start address
0xBFFFC	XCNT 32767	transfer count

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3.5.13 Add-On Registers

These four registers are used to initialize the PCI-bus controller and perform diagnostic testing. Four DWORD registers are mapped into system address space after the FPGA loading is completed. These registers use the first location in the Scatter Gather table as a data hold area prior to loading the desired value into the add-on registers of the PCI-bus controller. Any data in the Scatter Gather table will be corrupted when accessing these registers. the BMEN bit in the BMCTL register must be zero to access these registers.

BADR3 +		*Page #*
0xC0000	Add-On Interrupt Control (AINT)	3–82
0xC0004	Add-On General Control (AGCSTS)	3–83
0xC0008	Manual Destination Address (MDSTADR)	3–83
0xC000C	Manual Transfer Count (MXCNT)	3–84

Figure 3–14. Add-On Register Map

3.5.13.1 Add-On Interrupt Control (AINT) W-O

BADR3 + 0xC0000

PCP_AINT_32

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
15							8
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
23							16
DATA23	DATA22	DATA21	DATA20	DATA19	DATA18	DATA17	DATA16
31							24
DATA31	DATA30	DATA29	DATA28	DATA27	DATA26	DATA25	DATA24

This register must be programmed once during PCVision*plus* initialization, after power up and FPGA loading. The BMEN bit in the BMCTLX register (Frame Buffer Control registers) must be zero to access this register. Write the value 0x0024 4000 in location zero of the scatter gather table (DMA table) then write any value to this address to transfer the value into the correct location.

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3.5.13.2 Add-On General Control (AGCSTS) W-O

BADR3 + 0xC0004

PCP_AGCSTS_32

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
15							8
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
23							16
DATA23	DATA22	DATA21	DATA20	DATA19	DATA18	DATA17	DATA16
31							24
DATA31	DATA30	DATA29	DATA28	DATA27	DATA26	DATA25	DATA24

This register initializes the PCVision*plus* bus master port, and must be programmed once during PCVision*plus* initialization, after power up and FPGA loading. The BMEN bit in the BMCTLX register (Frame Buffer Control registers) must be zero to access this register. Write the value 0x1000 0000 in location zero of the scatter gather table (DMA table) then write any value to this address to transfer the value into the correct location.

3.5.13.3 Manual Destination Address (MDSTADR) W-O

BADR3 + 0xC0008

PCP_MDSTADR_32

7							0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
15							8
ADR15	ADR14	ADR13	ADR12	ADR11	ADR10	ADR9	ADR8
23							16
ADR23	ADR22	ADR21	ADR20	ADR19	ADR18	ADR17	ADR16
31							24
ADR31	ADR30	ADR29	ADR28	ADR27	ADR26	ADR25	ADR24

This register is for diagnostic purposes only. Writing a value into this register checks the BMC ability to load a destination address into the PCI-bus Controller chip. The BMEN bit in the BMCTLX register (Frame Buffer Control registers) must be zero to access this register. Write the desired address in location zero of the scatter gather table (DMA table) then write any value to this address to transfer the address into the correct location. The value can be read back through the BMDST register.

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3.5.13.4 Manual Transfer Count (MXCNT) W-O

BADR3 + 0xC000C

PCP_MXCNT_32

7							0
XCNT7	XCNT6	XCNT5	XCNT4	XCNT3	XCNT2	XCNT1	XCNT0
15							**8**
XCNT15	XCNT14	XCNT13	XCNT12	XCNT11	XCNT10	XCNT9	XCNT8
23							**16**
XCNT23	XCNT22	XCNT21	XCNT20	XCNT19	XCNT18	XCNT17	XCNT16
31							**24**
XCNT31	XCNT30	CXNT29	XCNT28	XCNT27	XCNT26	XCNT25	XCNT24

This register is for diagnostic purposes only. Writing a value into this register checks the BMC ability to load a transfer count into the PCI-bus Controller chip. The BMEN bit in the BMCTLX register (Frame Buffer Control registers) must be zero to access this register. Write the desired count in location zero of the scatter gather table (DMA table) then write any value to this address to transfer the count into the correct location. The value can be read back through the BMXC register.

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CHAPTER 4
DAC and PLL PROGRAMMING

4.1 DAC REGISTERS

PCVision*plus* contains two Dual-DAC (Digital to Analog Converter) devices. Each of the two devices contains two 13-bit DACs that control the ADC reference voltages, DC Restore (clamp) Voltage and the Sync Stripper Line Rate. The DACs have a serial interface. The serial interfaces of these two devices are daisy-chained together, accessing both devices using one serial port. The DACCS bit (INCON2 register) and the serial data bit in the DACPRG register interface to and program the DACs.

4.1.1 DAC Interface

The 3-wire serial interface requires a Chip Select (CS, active low), Serial Clock (SCLK, active high), and Data In (DIN). The DACCS bit (in INCON2 register) drives the CS pin. Programming DACCS to zero enables loading data. Writing to the DACPRG register generates SCLK. The write pulse is connected to SCLK of the two DACs. Every write to DACPRG causes a SCLK pulse. The DACSDATA bit in the DACPRG register is connected to the DAC "Data In" bit (DIN) pin and clocked into the DAC by this SCLK pulse. The DAC "Data Out" pin is connected to the DACSDATA bit in the DACPRG register. DACSDATA performs both write and read back functions.

Reading the DACSDATA bit is used in diagnostics to verify the serial daisy chain is connected. The internal DAC values can not be read back through the DACSDATA bit.

Each data load command requires a 32-bit load, containing two 16-bit address+command+data values in an internal shift register with the DACCS bit set low. When the DACCS bit is written high, the 32-bit command in the shift register is transferred in and executed. Each time DACCS is brought low 32 bits must be loaded. After 32 register writes to the DACPRG register with DACCS set low, the internal shift register is ready to execute the two loaded commands by bringing the DACCS high.

NOTE *Use IFC library functions to program the reference DACs. These functions are written to handle the timing and protocol of this serial interface.*

All 32-bit data values use the following format:

32		PCLAMP or RATE			16	15		PREF or NREF			0
A0	C1	C0	D12	D11 – D1	D0	A0	C1	C0	D12	D11 – D1	D0

Load 32 bits at one time, starting with bit 31. Bit 31 is the first bit written to DACPRG; bit 0 is the last bit written. The two 16-bit values access the two Dual-DACs in two distinct groups. The upper word always accesses either the

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PCLAMP DAC or the RATE DAC. The lower word always accesses either the PREF DAC or the NREF DAC. The address bit (31 and 15) determines which DAC.

1st Address		*2nd Address*	
bit 31	DAC accessed	*bit 15*	DAC accessed
0	PCLAMP	0	PREF
1	RATE	1	NREF

Only one commands is supported on the PCVision*plus*. Each 32-bit transfer programs two new DAC values, and updates all four DACs from the internal buffers. No other values of address and commands are supported.

A0	*C1*	*C0*	*Data*	Command
x	1	1	13-bit value	Load new data, update all DACs from internal buffers
0	0	0	all zeros	NOP, no operation

4.1.2 ADC Reference DACs

The ADC requires both positive (PREF) and negative (NREF) reference voltages. The PREF and NREF DACs establish the positive and negative voltage references independently. The absolute minimum difference between any PREF and NREF combination is 0.4 Volt. The absolute maximum difference between any PREF and NREF combination is 1.6 Volts. For best performance and accuracy, the difference between NREF and PREF should be 1.5 Volts.

The fixed input gain provides an incoming peak-to-peak range of 1.5 volts; assuming CCIR or RS170 video levels of 1 volt peak-to-peak open circuit, 0.286 sync and 0.714 video.

For all DACs the VOUT formula is as follows:

$$VOUT = (NB \times VREF\ Volts) / 8192$$

Where NB is the numerical value of the DACs binary input code.

The DAC reference voltage for the NREF and PREF DACs is 3.3 Volts. The 13-bit DACs produce 8192 voltage steps, with 3.3/8192=0.4 mV steps.

Data	Output Voltage
0x00	0 mV
0x01	0.4 mV
0x02	0.8 mV
. . .	. . .
0x1FFF	3.3 V

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4.1.3 DC Restore Reference DAC

This DAC programs the clamp voltage (PCLAMP) used to DC Restore the AC coupled video input. The incoming video signal is sampled during the back porch and is clamped to the voltage level programmed in this DAC.

The voltage of this DAC should be set to match the negative reference voltage of the ADC. The voltage swing of the DAC is 0 to 2.5 Volts. The 13-bit DAC produces 8192 voltage steps with 2.5/8192=0.3 mV steps. The default DAC setting for 1.75 Volts is 0x1666 (5734 decimal).

Desired Clamp Level = 1.75 V

DAC value = (desired clamp voltage level) / (2.5 V / 8192)

= 1.75/0.000305 = 5734 = 0x1666

Data	Output Voltage
0x00	0 mV
0x01	0.3 mV
0x02	0.6 mV
. . .	. . .
0x1FFF	2.5 V

4.1.4 Sync Stripper Horizontal Line Rate

This DAC programs the voltage used to define the horizontal line rate of the Sync Stripper. The Reference voltage for this DAC is +2.5 Volts. The 13-bit DAC produces 8192 voltage steps with 2.5/8192=0.3 mV steps. The formula for calculating the sync stripper DAC value is:

DAC Value = (1.7 – (line rate in KHz) / 45 KHz)) / 0.000169

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4.2 PLL REGISTERS

PCVision*plus* contains a PLL (Phase Lock Loop) for line locked clock operations (PLL mode) and for frequency synthesis (XTAL mode). The PLL internal registers are accessed through a serial interface.

4.2.1 PLL Interface

The PLLCS bit in the INCON2 register and the PLLPRG register program the PLL. Holding the PLLCS bit low puts the PLL in programming mode. Every access to the PLLPRG register (read or write) will generate a serial clock to the shift data in or out of the PLL registers, depending on the cycle type. Read and write access is available on the PLL serial port. Data is loaded in the lsb (least significant bit) of the PLLPRG register.

Every access to the PLL requires sixteen register reads/writes to the PLLPRG register, as shown in the Figure 4–1. First the PLLCS bit must be set low, followed by the sixteen PLLPRG register cycles. The PLL has seven 11-bit registers which are accessed by writing the appropriate value into the address bits A(2–0) bits. All registers must be setup for proper PLL or XTAL mode operation. Single bit changes can be made by addressing the appropriate PLL register and writing only 11-bits of data; it is not required to reload all PLL registers every time, but all 11 bits in one register must be loaded.

NOTE *Use the IFC library functions to program the PLL registers. These functions are written to handle the timing and protocol of this serial interface.*

4.2.2 PLL Serial Write Cycles

PLLSDATA is loaded into an internal PLL shift register on every write of the PLLPRG register while PLLCS is low (in the INCON2 register; set before accessing PLLPRG register). The first bit loaded is the R/W bit which is 0 to indicate the cycle is a write cycle. Next, three address bits A(2–0) are loaded, which point to one of seven PLL internal registers. Finally, 11 data bits are loaded. The PLLCS bit must then be set high in the the INCON2 register, followed by a dummy read or write access to PLLPRG register which performs the actual transfer of the 15-bit shift register data into the addressed PLL register (PLLSDATA is “don’t care” for the dummy operation). 15 register writes are required with PLLCS low and 1 register write is required after PLLCS is written high.

4.2.3 PLL Serial Read Cycles

Read cycles require two operations. First, a write must be executed as described in previous section with the R/W bit high, to indicate a read cycle. The three address bits are loaded followed by 11 bits of ”don’t care” data (only need the R/W bit and three address bits, but you must clock the PLLSCLK 11 more times to move the serial data into the correct position in the internal 15-bit shift register). Write PLLCS high in the INCON2 register and execute a dummy read or write to PLLPRG register, which loads the Read command and the selected address. At the end of the dummy cycle, the Serial Data becomes an output and the contents of the addressed register are loaded into the shift register (3 address bits and 11 data bits). To complete the read cycle, reset the PLLCS bit low and execute 15 read cycles to PLLPRG. Each read will shift one bit out of the PLL internal shift register. After all bits are read, set PLLCS high and execute one last dummy cycle to PLLPRG to end the read cycle.

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Notice the difference between the 15 reg writes in a write cycle and the 15 reg reads in a read cycle. During the read, the first clock is associated with valid data (A0), but in a write the first clock is associated with the R/W bit. Due to this different alignment, the three address bits and the 11 data bits are read with the first 14 clocks (last data D10 is read out with the 14th clock). However a 15th clock is still required with PLLCS low, which disables the read command. After the 15th read, discard this data and bring the cycle to an end as shown, by bringing PLLCS high and executing a final 16th clock by writing the PLLPRG one more time.

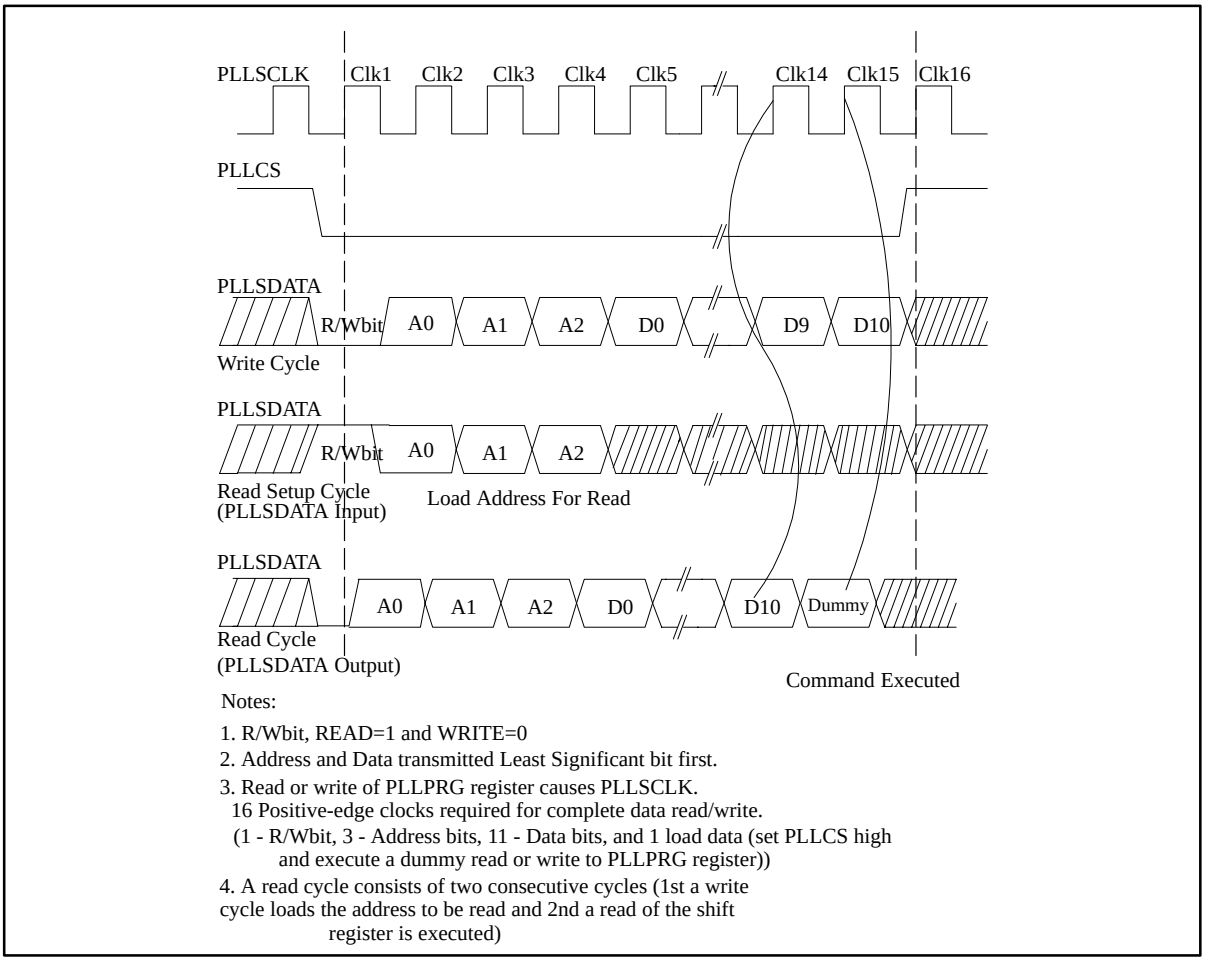


Figure 4–1. PLL Serial Programming Timing

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4.2.4 PLL Register 0 (PLLA0)

PLL Address 0x0

PCR_PLLA0_16

7							0
FDIV7	FDIV6	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	FDIV10	FDIV9	FDIV8

Bit	Mnemonic	Function
10–0	FDIV	FeedBack Divider
15–11	Reserved	Don’t care

4.2.4.1 FeedBack Divider (FDIV) R/W

The eleven FDIV bits control the PLL feedback divider which divides the VCO by the set Modulus. The Modulus = FDIV + 1. The minimum setting is 64 and the maximum is 2048. Default FDIV setting at power up is 0x04F (79) so the default Modulus = 80 at power-up. Refer to the Examples for programming PLL and XTAL mode, for calculating PLL register values.

4.2.5 PLL Register 1 (PLLA1)

PLL Address 0x1

PCR_PLLA1_16

7							0
LO7	LO6	LO5	LO4	LO3	LO2	LO1	LO0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Mnemonic	Function
7–0	LO	Feedback Sync Pulse Low
15–8	Reserved	Don’t care

4.2.5.1 Feedback Sync Pulse Low (LO) R/W

These bits program an additional PLL feedback divider output with a programmable phase, which can be selected at Output 3. The default setting is 0x3. PCVision*plus* does not use this mode of the PLL, and this register *should always be programmed to 0x0.*

4.2.6 PLL Register 2 (PLLA2)

PLL Address 0x2

PCR_PLLA2_16

7							0
HI7	HI6	HI5	HI4	HI3	HI2	HI1	HI0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Bit	Mnemonic	Function
7–0	HI	Feedback Sync Pulse High
15–8	Reserved	Don’t care

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4.2.6.1 Feedback Sync Pulse High (HI) R/W

These bits program an additional feedback divider output but with a programmable phase, which can be selected at Output 4. The default setting is 0x6. PCVision*plus* does not use this mode of the PLL, and this register *should always be programmed to 0x0.*

4.2.7 PLL Register 3 (PLLA3)

PLL Address 0x3

PCR_PLLA3_16

7							0
RDIV7	RDIV6	RDIV5	RDIV4	RDIV3	RDIV2	RDIV1	RDIV0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	REFPOL	RDIV9	RDIV8

Bit	Mnemonic	Function
9–0	RDIV	Reference Divider
10	REFPOL	Reference Polarity
15–11	Reserved	Don't care

4.2.7.1 Reference Divider (RDIV) R/W

These bits control the PLL reference divider Modulus which divides the XTAL/EXTREF by the set modulus. The modulus range is 1 to 1024. The modulus = RDIV + 1. The Default RDIV is 0x013 (19) and Modulus = 20. Use the following formulas to calculate RDIV:

For PLL mode: RDIV always = 0x0 or modulus = 1

For XTAL mode: RDIV = (14.318 MHz / line rate)

For RS-170: line rate = 15.734 KHz.

For CCIR: line rate = 15.625 KHz.

4.2.7.2 Reference Polarity (REFPOL) R/W

This bit sets the external reference signals polarity. The default setting is 0. *This bit should always be programmed to one.*

REFPOL	Function
0	Positive Edge *Not Supported*
1	Negative Edge *always*

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4.2.8 PLL Register 4 (PLLA4)

PLL Address 0x4

PCR_PLLA4_16

7							0
INTFLT	PDEN	PFD2	PFD1	PFD0	VCO2	VCO1	VCO0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	1	CLKSEL	INTVCO

This register contains several control bits for the VCO (voltage controlled oscillator) and the phase detector. Bit 10 must always be one. Program the reserved bits to zero.

Bit	Mnemonic	Function
2–0	VCO	VCO Gain
5–3	PFD	Phase Frequency Detector Gain
6	PDEN	Phase Frequency Detector Enable
7	INTFLT	Loop Filter Select
8	INTVCO	VCO Select
9	CLKSEL	Feedback Divider Clock Select
10	Reserved	Must be one
15–11	Reserved	Don’t care

4.2.8.1 VCO Gain (VCO) R/W

These bits control the PLL VCO Gain. The default setting is 4.

VCO	*VCO Gain*
0	10 MHz / Volt
1	15 MHz / Volt
2	20 MHz / Volt
3	25 MHz / Volt
4	45 MHz / Volt
5	60 MHz / Volt
6	75 MHz / Volt
7	90 MHz / Volt

Use the following formula to calculate the value for VCO Gain:

For both XTAL and PLL mode:

$$\text{VCO gain} = (\text{PDA} \times \text{LCOUNT} \times \text{Fdesired}) / 3.5\text{Volts}$$

Program VCO(2–0) to the next value greater than the calculated VCO gain. For example, if the calculated value is 12, use 15 MHz (not 10).

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4.2.8.2 Phase Frequency Detector Gain (PFD) R/W

These bits control the PLL Phase Frequency Detector Gain. The default setting is 3. *Always program these bits to 3* or 111 B.

PFD	*PFD Gain*	*Fine Phase Adjust*
0	*0.2344uA/2πrad*	*3ns/V*
1	*0.9375uA/2πrad*	*3ns/V*
2	*3.750uA/2πrad*	*3ns/V*
3	**15.00uA/2πrad**	**3ns/V always use this value**
4	*1.875uA/2πrad*	*6ns/V*
5	*7.500uA/2πrad*	*6ns/V*
6	*30.00uA/2πrad*	*1.5ns/V*
7	*120.0uA/2πrad*	*.375ns/V*

4.2.8.3 Phase Frequency Detector Enable (PDEN) R/W

This bit enables the PLL phase frequency detector. The default setting is 1 (enabled). *Always program to 1.*

PDEN	Function
0	PFD disabled *not supported*
1	PFD enabled

4.2.8.4 Loop Filter Select (INTFLT) R/W

This bit selects between external and internal loop filter mode. The PCVision*plus* uses an external loop filter. *This bit should always be 0.* Power-up default setting is 1, which must be changed to 0.

INTFLT	Function
0	External Loop Filter *always*
1	Internal Loop Filter *not supported*

4.2.8.5 VCO Select (INTVCO) R/W

This bit selects between internal and external VCO operation of the PLL. Set to internal VCO for proper operation. Power-up default setting is 1.

INTVCO	Function
0	External VCO *not supported*
1	Internal VCO *always*

4.2.8.6 Feedback Divider Clock Select (CLKSEL) R/W

This bit selects the input clock to the feedback divider. PCVision*plus* uses OUT1 feedback for PLL mode and VCO feedback for XTAL mode. Power-up default setting is 0.

CLKSEL	Function
0	*Not supported*
1	OUT1 clock feeds Feedback divider *always*

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4.2.9 PLL Register 5 (PLLA5) R/W

PLL Address 0x5

PCR_PLLA5_16

7							0
PDB1	PDB0	PDA1	PDA0	SWLW	ADD	FBKPOL	FBKSEL

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	1	FINEEN	LDLG

This register controls the PLL feedback divider. Bit 10 in this register must always be one.

Bit	Mnemonic	Function
0	FBKSEL	Feedback Select
1	FBKPOL	Feedback Polarity
2	ADD	Addition of 1 VCO Cycle
3	SWLW	Removal of 1 VCO Cycle
5–4	PDA	Output Post Scaler
7–6	PDB	Feedback Post Scaler
8	LDLG	Fine Phase Adjust Lead/Lag
9	FINEEN	Fine Phase Adjust Enable
10	Reserved	Must be one
15–11	Reserved	Don’t care

4.2.9.1 Feedback Select (FBKSEL) R/W

This bit selects internal feedback mode of the PLL. Default setting is 1. Always program this bit to one.

FBKSEL	Function
0	*External feedback not supported*
1	Internal Feedback selected

4.2.9.2 Feedback Polarity (FBKPOL) R/W

This bit selects the polarity of the external feedback signal if selected by FBKSEL. Defaults setting is 0.

FBKPOL	Function
0	Positive Edge *default*
1	Negative Edge

4.2.9.3 Addition of 1 VCO cycle (ADD) R/W

This bit is used to fine adjust the PLL. Toggle this bit from 0 to 1 to 0 to add one VCO cycle. The default setting is zero.

4.2.9.4 Removal of 1 VCO cycle (SWLW) R/W

This bit is used to fine adjust the PLL. Toggle this bit from 0 to 1 to 0 to remove one VCO cycle. The default setting is zero.

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4.2.9.5 Output Post Scaler (PDA) R/W

These two bits define the divide by value of the output post scaler. The default setting is 0. Refer to the Examples for Programming PLL and XTAL mode for calculating PLL register values.

PDA	Function
0	Divide by 8
1	Divide by 4
2	Divide by 2
3	Divide by 1

4.2.9.6 Feedback Post Scaler (PDB) R/W

This bit controls the divider value of the feedback post scaler. Default setting is 3. Always program to 3.

4.2.9.7 Fine Phase Adjust Lead/Lag (LDLG) R/W

This bit sets the lead/lag relationship at the input to the PFD (programmable frequency detector). Default setting is 1. *Always use the default value of 1.*

LDLG	Function
0	*FBK will lag REF at input to PFD do not use*
1	FBK will lead REF at input to PFD *always*

4.2.9.8 Fine Phase Adjust Enable (FINEEN) R/W

This bit enables an external fine adjustment of the PLL. This mode of the PLL is not used and should always be set to disabled. The default setting is 0. *Always use the default value of 0.*

FINEEN	Function
0	Fine adjust disabled, *always*
1	*Fine adjust enabled, do not use*

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4.2.10 PLL Register 6 (PLLA6)

PLL Address 0x6

PCR_PLLA6_16

7							0
DACRST	OMUX4	OMUX3	OMUX2	OMUX1	LCOUNT2	LCOUNT1	LCOUNT0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	EXTREF	AUXCLK	AUXEN

Bit	Mnemonic	Function
2–0	LCOUNT	Load Counter
3	OMUX1	Output 1 Select
4	OMUX2	Output 2 Select
5	OMUX3	Output 3 Select
6	OMUX4	Output 4 Select
7	DACRST	DAC Reset
8	AUXEN	Output Test Mode
9	AUXCLK	Output Clock for Test Mode
10	EXTREF	EXTREF Select
15–11	Reserved	Don’t care

4.2.10.1 Load Counter (LCOUNT) R/W

These bits define the divide ratio of the PLL Load Counter. Default setting is 7. Refer to the Examples for Programming PLL and XTAL mode for finding LCOUNT values.

LCOUNT	Function
0	3 (1–pos, 0–neg)
1	4 (pos edge)
2	4 (neg edge)
3	5 (1–neg, 0–pos)
4	6 (pos edge)
5	8 (pos edge)
6	8 (neg edge)
7	10 (neg edge)

4.2.10.2 Output 1 Select (OMUX1) R/W

The OMUX1 bit selects the source to output clock 1 which is the clock output used on PCVision*plus*. Always program to zero.

OMUX1	Function
0	Select Load Counter Output
1	*not supported*

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4.2.10.3 Output 2 Select (OMUX2) R/W

The OMUX2 bit selects the source to output clock 2, which is not used on the PCVision*plus*. Always program OMUX2 to zero.

4.2.10.4 Output 3 Select (OMUX3) R/W

The OMUX3 bit selects the source to output clock 3, which is not used on the PCVision*plus*. Always program OMUX3 to zero.

4.2.10.5 Output 4 Select (OMUX4) R/W

The OMUX4 bit selects the source to output clock 2, which is not used on the PCVision*plus*. Always program OMUX2 to 0.

4.2.10.6 DAC Reset (DACRST)

This bit must be zero for proper operation. Always program DACRST to zero.

4.2.10.7 Output Test Mode (AUXEN) R/W

This bit puts the PLL circuit into test mode for diagnostic purposes only. This bit should always be zero.

4.2.10.8 Output Clock for Test Mode (AUXCLK) R/W

This bit is only used in diagnostic test mode, and should always be zero.

4.2.10.9 EXTREF Select (EXTREF) R/W

This bit selects the input to the PLL. Default setting is 0. Always program this bit to 1.

EXTREF	Function
0	*Cyrstal input, not supported.*
1	External Reference Input Operation

4.2.11 PLL Register 7 (PLLA7) N/A

PLL Address 0x7

PLLA7

7							0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register is not used and access to it is prohibited.

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4.3 PROGRAMMING EXAMPLE FOR PLL MODE

This example provides detailed calculations for programming the PLL and PWG registers in PLL mode. Either the "total horizontal line time" or the "active time" is required, and the desired number of pixels in the output; either active or total. The "total horizontal line time" includes the active, sync, and blank regions. Use the following worksheet to calculate the required register settings:

PLL MODE: Format_____

Active pixel resolution: H=_____ x V=_____

Total pixel resolution: H=_____ x V=_____

1. Determine desired Clock Rate (in us) using one of the following formulas (both give the same result):

Pclk = (Total horizontal line time / total number of pixels desired)

or

Pclk = (Active line time / Active number of pixels)

Pclk = _____ / _____ = _____ (time in us)

Fdesired = 1 / Pclk = _____ (frequency in MHz)

For RS-170; the total line time is 63.556 us and the active time is 52.656 us.

For CCIR; the total line time is 64 us and the active time is 51.95 us.

2. Determine PDA and LCOUNT:

Let ODA (Output Divider Actual) = PDA x LCOUNT

Find ODD (Output Divider Desired) using the following formula:

ODD = 230MHz / Fdesired

ODD = 230 MHz / _____ = _____

Use the four tables at the end of this chapter to find a combined value of PDA and LCOUNT which comes closest to ODD: however, ODA ~~< ODD~~ or (PDA x LCOUNT) ~~< ODD~~

Selected PDA = _____

Selected LCOUNT = _____

LCOUNT has two register settings for 4 and two settings for 8; use either setting.

3. Calculate the VCO gain using the following formulas:

First find the Fvco using PDA, LCOUNT and Fdesired:

Fvco = PDA x LCOUNT x Fdesired

Fvco = _____ x _____ x _____ = _____

Use Fvco to find VCO Gain:

VCO Gain = Fvco / 3.5Volts

VCO Gain = _____ / 3.5Volt = _____ MHz/Volt

Program the VCO bits to the value which is equal to or greater than the value calculated for VCO Gain (see register definition for VCO bits). If the calculated gain is 12, use the next highest value for VCO of 15, not 10.

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4. Calculate the divider ratio for the feedback path:

Always set PDB to 1 (register value of 0x3) and find Fdiv using the following formula:

Fdiv = [Total number of pixels in horizontal period / 1]

or

Fdiv = [Fdesired / Horizontal Line Rate]

Fdiv = _____ / _____ = _____

Both give the same result. Set the FDIV register bits as follows:

FDIV = Fdiv – 1

FDIV = _____ – 1 = _____

5. Set the following PLL reg bits as indicated:

PLLA0 = FDIV

PLLA1 and PLLA2 both = 0x0

PLLA3 = 0x400

RDIV=0 (Rdiv = 1 RDIV = Rdiv – 1 = 1 – 1 = 0)

REF_POL = 1

PLLA4 = 0x75[1xxx] (where xxx = VCO calculated above)

VCO= from VCO Gain calculation above

PFD = 0x3 (PFD gain always set to 15uA/2pi-rad)

PDEN = 1 (phase detector enabled)

INTFLT = 0 (external loop filter selected)

CLKSEL = 1 (select OMUX0 as feedback source)

MSB = 1 (reserved bit must be 1)

PLLA5 = 0x5[11xx]3 (where xx= PDA bits form value found in tables)

FBKSEL = 1 (always select internal feedback)

FBKPOL = 1 (always select negative edge)

ADD = 0 (use default)

SWLW = 0 (use default)

PDA bits = Use value found in tables above.

PDB[0:1] = 0x3 (always use PDB = 1)

LDLG = 1 (use default)

FINEEN = 0 (use default)

MSB = 1 (reserved bit must be 1)

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PLLA6 = 0x44[0xxx] (where xxx = LCOUNT bits, from value found in tables)

LCOUNT = use bit definition for the value found in tables.

OMUX1 = 0 (use default)

EXTREF = 1 (external reference Input operation)

6. Calculate Window Generator Horizontal settings as follows:

HACTIVE = [total # of pixels from hsync to end of the active region] – 2
= (Active + Hsync + Back Porch – Crop-End) – 2

HOFF = [Total # of pixels from Hsync to the start of active video]
= (Hsync + Back Porch + Crop-start)

Use the following formulas to determine the number of pixels in each region of the HACTIVE/HOFF formulas:

Active = Active time / Pclk (in us)

Hsync = HSync Time / Pclk (in us)

Back Porch = Back Porch Time / Pclk (in us)

Crop-End = Number of pixels to Crop from the end of active video region

Crop-Start = Number of pixel to Crop from start of active video region

For RS-170: Active = 52.656 us Hsync = 4.7 us Back Porch = 4.7 us

For CCIR: Active = 51.95 us Hsync = 4.7 us Back Porch = 5.8 us

NOTE *The Active region **must** be divisible by 8.*

NOTE *Any change to HOFF will shrink or expand the number of active pixels loaded in the horizontal direction. You must maintain the x4 restriction. Changes to HOFF must be accounted for in HACTIVE.*

7. Set the Window Generator Vertical settings as follows:

VACTIVE = [# of lines from Vsync to the end of Active video] – 1
= (Vactive + Vsync + Vblank – Vcrop-End) – 1

VOFF = [# of lines from Vsync to the start of Active video] – 1
= (Vsync + Vblank + Vcrop-Start) – 1

Vactive = # of lines per field/frame

Vsync = # of lines in Vsync

Vblank = # of lines from Vsync to the start of active video

Crop-End = # of lines to Crop from the end of active video region

Crop-Start = # of lines to Crop from start of active video region

For RS-170:

Total Lines per Frame = 525

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Total Line per Field = 262.5

Line per Vsync = 3

Lines in Vblank = 14

Lines in Active Max = 242.5 (use 240)

For CCIR:

Total Lines per Frame = 625

Total Line per Field = 312.5

Line per Vsync = 2.5

Lines in Vblank = 19.5

Lines in Active Max = 288 (use 287)

4.3.1 Notes on Programming PLL Mode

Many video sources vary slightly from the defined RS-170/CCIR values which will require fine tuning of the PWG and PLL settings. Rounding errors can also occur, causing the pixel clock (Pclk) value to be off slightly from the desired value.

Once the register settings are programmed, the user can check the image being acquired and verify the correct number of samples per line/frame are being captured. Specifically check the start and end of the horizontal line and verify valid pixel data is present (this can be done by saturating the video source). Two adjustments can be made to compensate for discrepancies. First the HOFF and HACTIVE values can be changed to move the ACTIVE video window left or right and the video is then re-checked. If there is no combination of HOFF and HACTIVE which compensate for differences, the Fdiv value can be increased or decreased which will cause the Pixel clock rate to increase or decrease slightly giving larger or smaller samples.

When programming the PLL registers, the ideal is to program the pixel clock to exactly match the active video region of the camera. As you change the pixel clock value, the number of pixels sampled within the fixed total line time (or fixed active time) will vary. Slight oversampling within the active region can also be used to establish a desired resolution. For example, you want 640 pixels within the active video region of a RS-170 camera. Set the desired number of pixels to 644. This will cause the pixel clock calculation to give a slightly smaller Pclk producing more pixels from the fixed active time. Cropping can be adjusted to display only 640 pixels.

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4.4 PROGRAMMING EXAMPLE FOR XTAL MODE

This example provides detailed calculations for programming the PLL and PWG registers in XTAL mode. The formulas are only slightly different from the ones used for PLL mode. The total horizontal line time or active time is required as well as the desired number of output pixels, either active or total. Use the following worksheet to calculate the required register settings:

XTAL MODE: Format_____

Active pixel resolution: H=_____ x V=_____

Total pixel resolution: H=_____ x V=_____

1. Determine desired Clock Rate (in ns) using one of the following formulas (both give the same result):

Pclk-d = (Total horizontal line time / total number of pixels desired)

or

Pclk-d = (Active line time / Active number of pixels)

Pclk-d = _____ / _____ = _____ (time in us)

Fdesired = 1 / Pclk-d = _____ (frequency in MHz)

For RS-170: the total line time is 63.556 us and the Active time is 52.656 us

For CCIR: the total line time is 64 us and the Active time is 51.95 us

2. Determine PDA and LCOUNT:

Let ODA (Output Divider Actual) = PDA x LCOUNT

Find ODD (Output Divider Desired) using the following formula:

ODD = 230MHz / Fdesired

ODD = 230MHz / _____ = _____

Use the four tables at the end of this chapter to find a combined value of PDA and LCOUNT which comes closest to ODD; however, ODA ~~< ODD~~ or (PDA x LCOUNT) ~~< ODD~~

Selected PDA = _____

Selected LCOUNT = _____

3. Calculate the VCO Gain using the following formulas:

First find the Fvco using PDA, LCOUNT and Fdesired:

Fvco-1 = PDA x LCOUNT x Fdesired

Fvco-1 = _____ x _____ x _____ = _____

Use Fvco-1 to find VCO Gain:

VCO Gain = Fvco-1 / 3.5Volts

VCO Gain = _____ / 3.5 Volts = _____ MHz/Volt

Program the VCO bits to the value which is equal to or greater than the value calculated for VCO Gain (see register definition for VCO bits).

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4. Calculate the divider ratio Rdiv. Rdiv divides the fixed XTAL source down to match the frequency of the feedback path.

Rdiv = Fixed clock source / line rate = 14.318 MHz / line rate

For NTSC and RS-170: line rate = 15.734 KHz.

For PAL and CCIR: line rate = 15.625 KHz.

Rdiv = 14.318 MHz / _____ = _____

Set the RDIV register bits as follows:

RDIV = Rdiv – 1

RDIV = _____ – 1 = _____

5. Calculate the divider ratio Fdiv for the feedback path:

Always use PDB = 1 (register value of 0x3). Find Fdiv using the following formula:

Fdiv = [Total number of pixels in horizontal period / 1]

or

Fdiv = [Fdesired / Horizontal Line Rate]

Fdiv = _____ / _____ = _____

Both give the same result. Set the FDIV register bits as follows:

FDIV = Fdiv – 1

FDIV = _____ – 1 = _____

6. Calculate the actual Pixel Clock frequency to use in the PTG settings:

Fclk = [(Fdiv x 14.318 MHz) / Rdiv]

Fclk = [(_____ x 14.318 MHz) / _____] = _____ (frequency in MHz)

Pclk = 1 / Fclk = _____ (time in us)

Use Pclk when calculating PWG and PTG register values.

7. Set the following PLL reg bits as indicate:

PLLA0 = FDIV

PLLA1 and PLLA2 both = 0x0

PLLA3 = 01xx xxxx xxxx (where x's = RDIV)

RDIV = Rdiv – 1 (from step 4)

REF_POL = 1

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PLLA4 = 0x75[1xxx] (where xxx = VCO[0:2])

VCO bits = (calculated in step 3)

PFD = 0x3 (PFD gain always set to 15uA/2pi-rad)

PDEN = 1 (phase detector enabled)

INTFLT = 0 (external loop filter selected)

CLKSEL = 1 (select Pclk as feedback source)

MSB = 1 (reserved bit must be 1)

PLLA5 = 0x5[11xx]3 (where xx= PDA bits for PDA value in tables)

FBKSEL = 1 (always select internal feedback)

FBKPOL = 1 (always select negative edge)

ADD = 0 (use default)

SWLW = 0 (use default)

PDA = bit settings for PDA value found in tables (step 2)

PDB = 0x3 (always use PDB value = 1 if possible)

LDLG = 1 (use default)

FEN = 0 (use default)

MSB = 1 (reserved bit must be 1)

PLLA6 = 0x44[0xxx] (where xxx = LCOUNT bits for the value found in tables)

LCOUNT = bit setting for value found in tables

OMUX1 = 0 (use default)

EXTREF = 1 (external reference Input operation)

8. Calculate Window Generator Horizontal settings as follows:

$$\text{HACTIVE} = [\text{total \# of pixels from hsync to end of the active region}] - 2$$
$$= (\text{Active} + \text{Hsync} + \text{Back Porch} - \text{Crop-End}) - 2$$

$$\text{HOFF} = [\text{Total \# of pixels from Hsync to the start of active video}]$$
$$= (\text{Hsync} + \text{Back Porch} + \text{Crop-start})$$

Use the following formulas to determine the number of pixels in each region of the HACTIVE/HOFF formulas:

Active = Active time / Pclk (in us)

Hsync = HSync Time / Pclk (in us)

Back Porch = Back Porch Time / Pclk (in us)

Crop-End = Number of pixels to Crop from the end of active video region

Crop-Start = Number of pixel to Crop from start of active video region

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For RS-170: Active = 52.656 us Hsync = 4.7 us Back Porch = 4.7 us

For CCIR: Active = 51.95 us Hsync = 4.7 us Back Porch = 5.8 us

NOTE *The Active region **must** be divisible by 8.*

NOTE *Any change to HOFF will shrink or expand the number of active pixels loaded in the horizontal direction. You must maintain the x4 restriction. Changes to HOFF must be accounted for in HACTIVE.*

9. Set the Window Generator Vertical settings as follows:

VACTIVE = [# of lines from Vsync to the end of Active video] – 1
= (Vactive + Vsync + Vblank – Vcrop-End) – 1

VOFF = [# of lines from Vsync to the start of Active video] – 1
= (Vsync + Vblank + Vcrop-Start) – 1

Vactive = # of lines per field/frame

Vsync = # of lines in Vsync

Vblank = # of lines from Vsync to the start of active video

Crop-End = # of lines to Crop from the end of active video region

Crop-Start = # of lines to Crop from start of active video region

For RS-170:

Total Lines per Frame = 525

Total Line per Field = 262.5

Line per Vsync = 3

Lines in Vblank = 14

Lines in Active Max = 242.5 (use 240)

For CCIR:

Total Lines per Frame = 625

Total Line per Field = 312.5

Line per Vsync = 2.5

Lines in Vblank = 19.5

Lines in Active Max = 288 (use 287)

10. Calculate the PTG settings using defined sync times and Pclk (in us) as follows:

Htotal = [(Horizontal Line Time / 2) / Pclk] – 1

Htotal = [(_____ / 2) / _____] – 1 = _____

HESYNC = [Hsync time / Pclk] – 1

HESYNC = [___ / ___] – 1 = _____

for Interlaced: VTOTAL = [(Total lines per frame / 2) – .5] x 2

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Interlaced: VTOTAL = [(_____ / 2) – .5] x 2 = _____

for Non-interlaced: VTOTAL = [(Total lines per frame) – .5] x 2

Non-interlaced: VTOTAL = [(_____) – .5] x 2 = _____

VSEND = (# of lines in Vsync – .5) x 2

VSEND = (_____ – .5) x 2 = _____

For RS-170:

horizontal lines time = 63.556 us

hsync time = 4.7 us

Total lines per frame = 525

Total lines per field = 525/2 = 262.5

Lines in vertical front porch = 3

Lines in Vsync = 3

For CCIR:

horizontal lines time = 64us

hsync time = 4.7us

Total lines per frame = 625

Total lines per field = 625/2 = 312.5

Lines in vertical front porch = 2.5

Lines in Vsync = 2.5

4.4.1 Notes on Programming XTAL Mode

Many video sources vary slightly from the defined RS-170/CCIR values which will require fine tuning of the PWG and PLL settings. Rounding errors can also occur, causing the pixel clock (Pclk) value to be off slightly from the desired value.

Once the register settings are programmed, the user can check the image being acquired and verify the correct number of samples per line/frame are being captured. Specifically check the start and end of the horizontal line and verify valid pixel data is present (this can be done by saturating the video source). Two adjustments can be made to compensate for discrepancies. First the HOFF and HACTIVE values can be changed to move the ACTIVE video window left or right and the video is then re-checked. If there is no combination of HOFF and HACTIVE which compensate for differences, the Fdiv value can be increased or decreased which will cause the Pixel clock rate to increase or decrease slightly giving larger or smaller samples.

When programming the PLL registers, the ideal is to program the pixel clock to exactly match the active video region of the camera. As you change the pixel clock value, the number of pixels sampled within the fixed total line time (or fixed active time) will vary. Slight oversampling within the active region can also be used to establish a desired resolution. For example, you want 640 pixels within the active video region of a RS-170 camera. Set the desired number

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of pixels to 644. This will cause the pixel clock calculation to give a slightly smaller Pclk producing more pixels from the fixed active time. Cropping can be adjusted to display only 640 pixels.

Variations in Pclk not only effect the pixel sample rate but also the PTG sync outputs which are driven to the camera. Large changes to Pclk will require recalculating all PTG settings based on the new Pclk value.

When driving the camera with internal timing in XTAL mode, the camera video signal may delayed with respect to the PTG output timing, used in sampling, clamping, and driving the PWG. The PWG horizontal and vertical settings may have to be increased to compensate for this delay.

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4.5 TABLES FOR PROGRAMMING EXAMPLES

PDA bits = 0x3: (PDA value = 1)

PDA value	LCNT value	PDA x LCNT
1	3	3
1	4 +/–	4
1	5	5
1	6	6
1	8 +/–	8
1	10	10

PDA bits = 0x2: (PDA value = 2)

PDA value	LCNT value	PDA x LCNT
2	3	6
2	4 +/–	8
2	5	10
2	6	12
2	8 +/–	16
2	10	20

PDA bits = 0x1: (PDA value = 4)

PDA value	LCNT value	PDA x LCNT
4	3	12
4	4 +/–	16
4	5	20
4	6	24
4	8 +/–	32
4	10	40

PDA bits = 0x0: (PDA value = 8)

PDA value	LCNT value	PDA x LCNT
8	3	24
8	4 +/–	32
8	5	40
8	6	48
8	8 +/–	64
8	10	80

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APPENDIX A
VIDEO CONNECTIONS

CONNECTORS

The PCVision*plus* provides three connections to the outside world. On the I/O plate there are two D-Sub connectors (15 and 26-pin) for camera and miscellaneous interface connections. Each D-Sub connector supports one camera. Internal to the PC, at the top edge of the PCB, is a 50-pin dual row post header connector. This provides parallel I/O capability in the form of 8 input and 8 output, high-drive TTL channels.

A jumper labeled “I/O Level” on the PCVision*plus* board sets the power-up state of the parallel port outputs. All parallel port outputs have an initial setting of either all 0 or all 1 based on the jumper setting. Refer to Figure A–1.

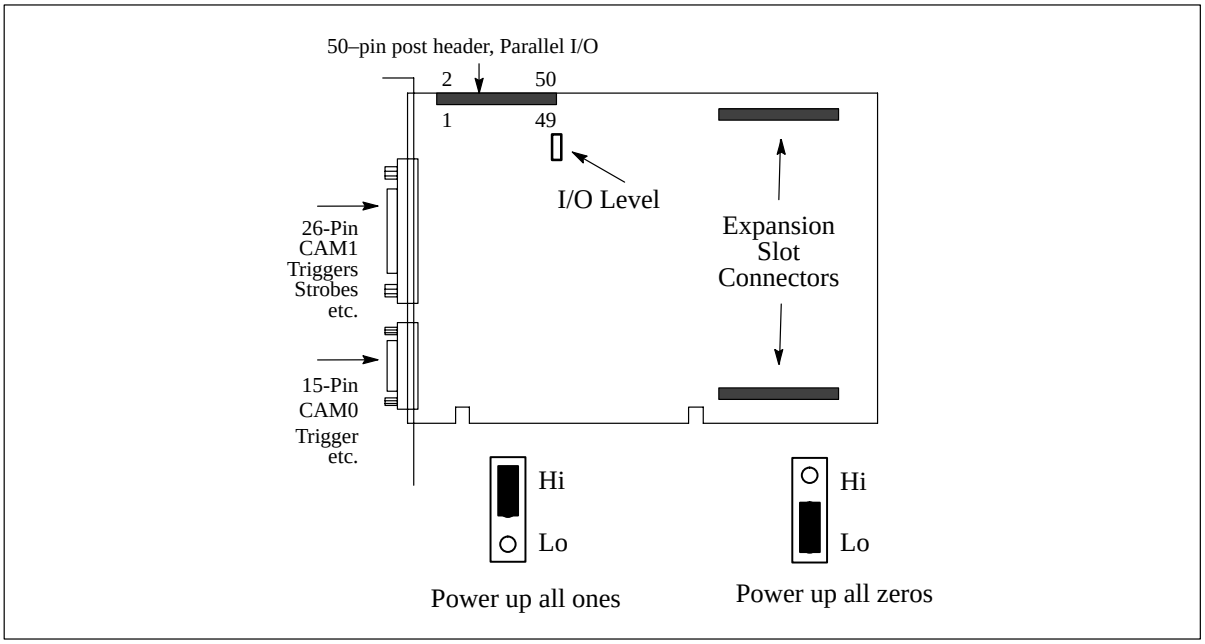


Figure A–1. PCVision*plus* Board, Connectors and Jumper

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15-Pin D-Sub

The 15-pin D-Sub connector is pin compatible with standard camera adapter cables for single camera interfacing. This connector supports one camera. The PCVision*plus* can supply up to 1A at 12V from chassis power. (new signals have been added to pins that supported a second camera on the PCVision frame grabber.)

Table A–1. 15-Pin Connector

Pin #	*Signal name*	*Description*
1	–	no connection
2	CAM0	Video input – camera 0
3	Trig_In_0_15	Trigger 0 TTL Input (this input is available on both video connectors)
4	CLKIN_0	Clock Input – camera 0
5	DGND0	Digital ground – camera 0
6	Strobe_0	Strobe 0 Output
7	AGND0	Analog ground
8	Misc_IO_Out2	Miscellaneous Output 2
9	FRESET0	Frame reset – camera 0 (optional VSCAN clock input 0)
10	+12VRET	Power return
11	Misc_IO_In2	Miscellaneous Input 2
12	–	no connection
13	HSYNC0	Horizontal Sync (LEN) - camera 0
14	VSYNC0	Vertical Sync (FEN) - camera 0
15	+ 12V	Power +12V D.C.

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26-Pin D-Sub

The 26-pin D-Sub connector supports one camera, and provides additional signals for trigger, strobe and I/O. The PCVision*plus* can supply up to 1A at 12V from chassis power.

Table A–2. 26-Pin Connector

Pin #	*Signal name*	*Description*
1	Opto_In1+	Trigger 1 Opto-Isolator positive input
2	CAM1	Video input - camera 1
3	DGND	Digital ground
4	Misc_IO_In1	Miscellaneous input 1
5	Misc_IO_Out1	Miscellaneous output 1
6	Strobe_0	Strobe 0 output
7	Strobe_1	Strobe 1 output
8	Opto_In0+	Trigger 0 Opto-Isolator positive input
9	Opto_In0–	Trigger 0 Opto-Isolator negative input
10	Opto_In1–	Trigger 1 Opto-Isolator negative input
11	AGND	Camera ground
12	CLKIN_1	Clock Input – camera 1
13	FRESET1	Frame reset - camera 1 (optional VSCAN clock input 1)
14	+12V_Ret	Power return
15	Misc_IO_In0	Miscellaneous input 0
16	Misc_IO_Out0	Miscellaneous output 0
17	Trig_In0_26	Trigger 0 TTL input (this input is available on both connectors)
18	Trig_In1	Trigger 1 TTL input
19	Diff_In0+	Trigger 0 Differential positive input
20	Diff_In0–	Trigger 0 Differential negative input
21	HSYNC1	Horizontal Sync (LEN) - camera 1
22	VSYNC1	Vertical Sync (FEN) - camera 1
23	+12V	+12V supply
24	DGND	Digital ground
25	Diff_In1+	Trigger 1 Differential positive input
26	Diff_In1–	Trigger 1 Differential negative input

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Parallel I/O Connector

Digital I/O is available on a 50-pin dual row post header connector. This provides parallel I/O capability of 8 input and 8 output, high-drive TTL channels. This port allows controlling or monitoring external events. The pin-out is OPTO22 compatible. All even numbered pins are connected to Digital Ground.

A jumper labeled “I/O Level” on the PCVision*plus* board sets the power-up state of the parallel port outputs. Refer to Figure A–1.

Table NO TAG–3. 50-Pin Dual-Row Header

Pin #	*Signal name*	*Description*
1	+5V	+5 V power output
3, 5	–	no connection
7, 9	–	no connection
11	STROBE_O	Strobe Output / Output data latch
13	STROBE_I	Strobe Input / Input data latch
15	I/O_INT	Interrupt Input
17	IN7	Digital Input pin 7
19	IN6	Digital Input pin 6
21	IN5	Digital Input pin 5
23	IN4	Digital Input pin 4
25	OUT7	Digital Output pin 7
27	OUT6	Digital Output pin 6
29	OUT5	Digital Output pin 5
31	OUT4	Digital Output pin 4
33	IN3	Digital Input pin 3
35	IN2	Digital Input pin 2
37	IN1	Digital Input pin 1
39	IN0	Digital Input pin 0
41	OUT3	Digital Output pin 3
43	OUT2	Digital Output pin 2
45	OUT1	Digital Output pin 1
47	OUT0	Digital Output pin 0
49	+5V	+5 V power output
2, 4, 6, 8, 10, 12, 14,		Digital Ground
16, 18, 20, 22, 24, 26,		Digital Ground
28, 30, 32, 34, 36, 38,		Digital Ground
40, 42, 44, 46, 48, 50		Digital Ground

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CABLES

This appendix covers some of the cables available from Coreco Imaging, Inc. for interfacing cameras to the PCVision*plus*.

Break-out cables plug into the 15-pin and 26-pin D-Sub connectors, and split their signals into more connectors.

Adapter cables plug into the camera, and connect to either a break-out cable or directly into the PCVision*plus* board 15-pin connector.

Break-Out Cables

The following break-out cables are available for camera interfacing CAM1. No break-out cable is needed for the CAM0 connector.

Table A–4. Break-out Cables for PCVision*plus*

Order Code	*Label #*	*Description*
509-00065-00	509-00065-00	PCVision*plus* Breakout cable. Converts 26-pin D-Sub to a 15-pin connector and a 26-pin connector for Miscellaneous interface signals.
509-00066-00	509-00066-00	PCVision*plus* Miscellaneous cable. Converts 26-pin D-Sub to 8 BNC connectors and 4 pairs of wire hookup connectors for interface signals.

CAUTION *The PCVision cables should* ***not*** *be used with the* PCVision*plus. Damage can result to the camera,* PCVision*plus, or other devices. Active signals are shorted to ground by using these adapter cables.*

BCBL-PCV1	19-4814	PCVision Breakout cable 1. ***not recommended, supports only 1 camera***
BCBL-PCV2	19-4815	PCVision Breakout cable 2. ***not recommended, causes noise on video***
ACBL-PCVM1	19-4811	PCVision Miscellaneous cable 1. ***do not use with* PCVision*plus, causes shorts***
ACBL-PCVM2	19-4812	PCVision Miscellaneous cable 2. ***do not use with* PCVision*plus, causes shorts***
ACBL-PCVM4	19-4813	Miscellaneous cable 4. ***do not use with* PCVision*plus, causes shorts***

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Table A–5. Breakout Cable 509-00066-00 Pin-out

CAM1 15-pin	*Signal Description*	**PCVision*plus*** 26-pin Male
2	Video input 1 CAM1	2
4	Clock Input 1 CLKIN_1	12
5	Digital Ground DGND	3,24
7	Analog Ground AGND	11
9	Frame Reset 1 FRESET1	13
10	12 Volts return +12V_Ret	14
13	Horizontal Sync 1 HSYNC1	21
14	Vertical Sync 1 VSYNC1	22
15	+12 Volts supply	23
1,3,6,8,11,12	no connection	–
MISC 26-pin F		
1	Trigger 1 Opto positive input, Opto_In1+	1
3,24	Digital Ground	3,24
4	Miscellaneous Input 1 Misc_IO_In1	4
5	Miscellaneous Output 1 Misc_IO_Out1	5
6	Strobe 0 output Strobe_0	6
7	Strobe 1 output Strobe_1	7
8	Trigger 0 Opto positive input, Opto_In0+	8
9	Trigger 0 Opto negative input, Opto_In0–	9
10	Trigger 1 Opto negative input, Opto_In1–	10
15	Miscellaneous Input 0 Misc_IO_In0	15
16	Miscellaneous Output 0 Misc_IO_Out0	16
17	Trigger 0 TTL input Trig_In0_26	17
18	Trigger 1 TTL input Trig_In1	18
19	Trigger 0 Differential positive Diff_In0+	19
20	Trigger 0 Differential negative Diff_In0–	20
25	Trigger 1 Differential positive Diff_In1+	25
26	Trigger 1 Differential negative Diff_In1–	26
2,11,12,13, 14,21,22,23	no connection	–

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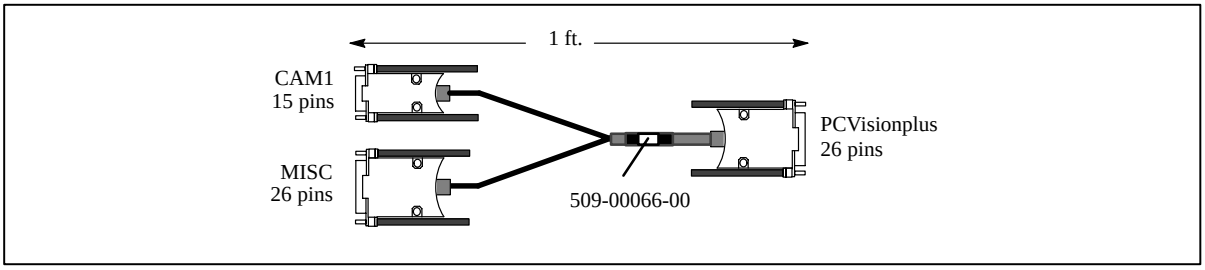


Figure A–2. PCVision*plus* Breakout Cable

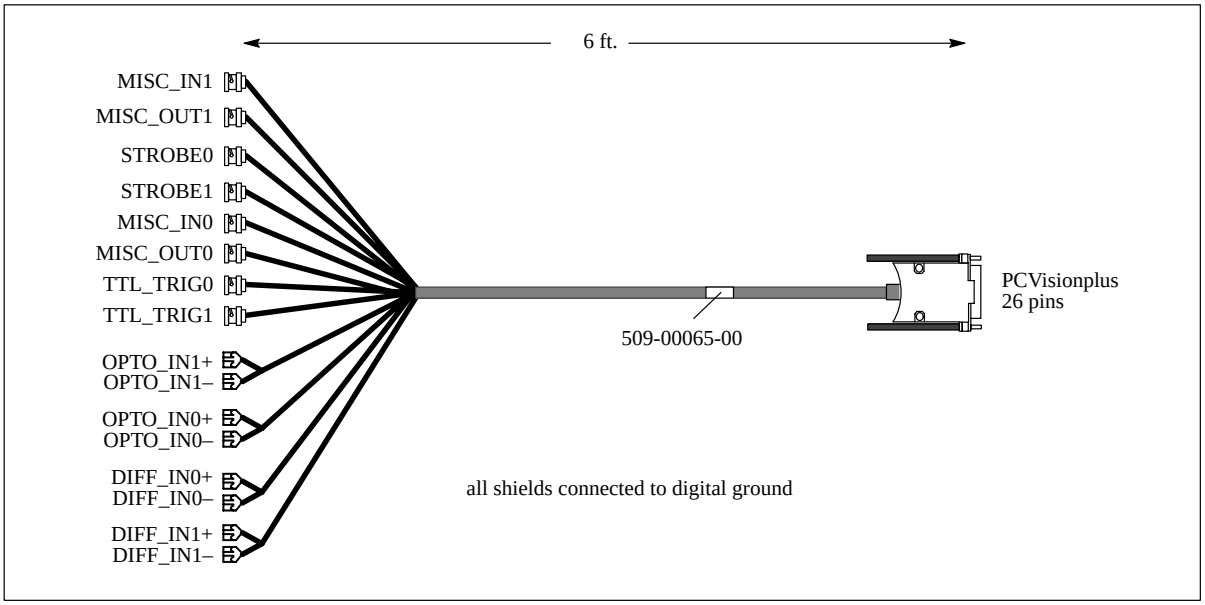


Figure A–3. PCVision*plus* Miscellaneous Cable

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Table A–6. Miscellaneous Cable 509-00065-00 Pin-out

		PCVision*plus*
BNC Label	Signal Description	26-pin Male
MISC_IN1	Miscellaneous Input 1 Misc_IO_In1	4
MISC_OUT1	Miscellaneous Output 1 Misc_IO_Out1	5
STROBE0	Strobe Output 0 Strobe_0	6
STROBE1	Strobe Output 1 Strobe_1	7
MISC_IN0	Miscellaneous Input 0 Misc_IO_In0	15
MISC_OUT0	Miscellaneous Output 0 Misc_IO_Out0	16
TTL_TRIG0	Trigger 0 TTL input Trig_In0_26	17
TTL_TRIG1	Trigger 1 TTL input Trig_In1	18
all shells	Cable Shield, Digital Ground	3,24
Wire Label		
OPTO_IN1+	Trigger 1 Opto-isolator positive input	1
OPTO_IN1–	Trigger 1 Opto-isolator negative input	10
OPTO_IN0+	Trigger 0 Opto-isolator positive input	8
OPTO_IN0–	Trigger 0 Opto-isolator negative input	9
DIFF_IN0+	Trigger 0 Differential positive input	19
DIFF_IN0–	Trigger 0 Differential negative input	20
DIFF_IN1+	Trigger 1 Differential positive input	25
DIFF_IN1–	Trigger 1 Differential negative input	26

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Camera Adapter Cables

The camera adapter cables plug into the 15-pin D-Sub connectors on the PCVision*plus* or on the break-out cables, and have camera connectors at the other end. This appendix covers some of the cables available. **Other adapter cablesmay be available;** consult your sales representative or Coreco Imaging, Inc..

BNC Camera Adaptor

This cable is compatible with monochrome video cameras with BNC connectors. The ordering code for this cable is ACBL-BNC1. Table A–7 gives the pin-out, and Figure A–4 illustrates this cable. This cable is also used with the Cidtec 2250 and 3750 cameras in non-interlaced RS-170 compatible mode.

Table A–7. ACBL-BNC Cable Pin-Out

BNC Label	Signal Description	15-pin
CAMERA	Video input (single-ended)	2
”	Shield AGND	7
MISC	FRESET, frame reset	9
”	Shield DGND	5
HSYNC	horizontal sync	13
”	Shield DGND	5
VSYNC	Vertical sync	14
”	Shield DGND	5
CLOCK	no connection or CLKIN_0 (see note)	4
”	Shield DGND	5

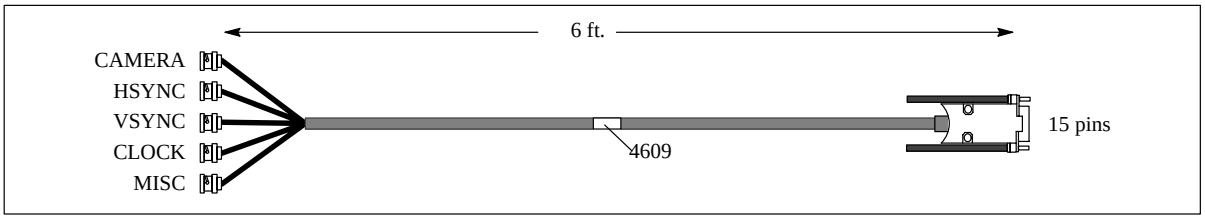


Figure A–4. ACBL-BNC Adaptor Cable

NOTE *The clock input has no connection when used with the break out cables BCBL-PCV1 and BCBL-PCV2. The clock input is supported when plugged directly into the 15-pin connnector on the* PCVision*plus board, or the 509-00066-00 cable.*

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Hirose (JIT) 1

This camera is compatible with the Sony XL series, and the Panasonic GPMF series analog monochrome cameras. The order code for this cable is ACBL-HIR1. Table A–8 gives the pin-out, and Figure A–5 illustrates this cable.

Table A–8. ACBL-HIR1 Cable Pin-Out

12-Pin	Signal Description	15-pin
1	+12 Volt return	10
2	+12 Volts DC	15
3	Analog ground	7
4	Video input (single-ended)	2
5	Digital ground	5
6	HDRIVE composite/horizontal sync	13
7	VDRIVE Vertical sync	14
8	Digital ground	5
9	no connection or CLKIN_0 (see note)	4
10	no connection	—
11	no connection	—
12	Digital ground	5

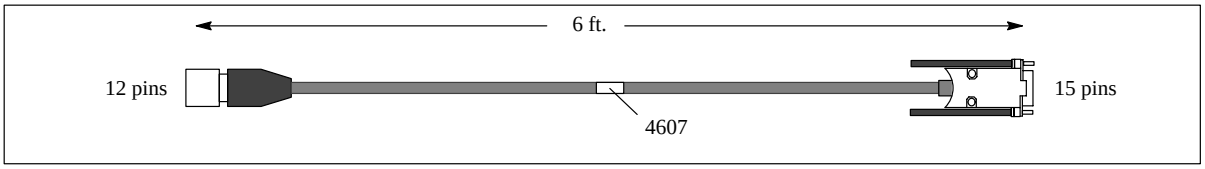


Figure A–5. ACBL-HIR1 Adaptor Cable

The following cameras have been tested with the #4607 adapter cable: Sony models XC77RR, XC77, XC75, XC-7500; and Panasonic models MF702 analog, CD-4D, MF502, MF552.

NOTE *The clock input has no connection when used with the break out cables BCBL-PCV1 and BCBL-PCV2. The clock input is supported when plugged directly into the 15-pin connnector on the* PCVision*plus board, or the 509-00066-00 cable.*

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Hirose (JIT) 2

This camera is compatible with the Pulnix TM Series analog monochrome cameras. The order code for this cable is ACBL-HIR2. Table A–9 gives the pin-out, and Figure A–6 illustrates this cable.

Table A–9. ACBL-HIR2 Cable Pin-Out

12-pin	Signal Description	15-pin
1	+12 Return	10
2	+12 Volts DC	15
3	Analog ground	7
4	Video input (single-ended)	2
5	no connection	—
6	no connection	—
7	VDRIVE vertical sync	14
8	Digital ground	5
9	HDRIVE composite/horizontal sync	13
10	no connection	—
11	no connection	—
12	Digital ground	5

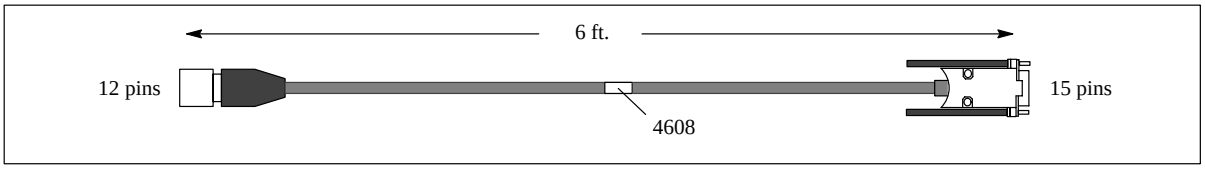


Figure A–6. ACBL-HIR2 Adaptor Cable

The following cameras have been tested with the ACBL-HIR2 adapter cable: Pulnix models 440, 640, 740, 760, 745, 765, 840, 845, 865.

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JAI CV-M10E/C

This cable is compatible with the CV-M10E and CV-M10C Progressive Scan analog monochrome camera. The order code for this cable is CBVM10-6. Table A–10 gives the pin-out, and Figure A–7 illustrates this cable. The PCVision*plus* must be programmed to output separate horizontal and vertical sync signals for this camera. A different cable is needed for the CV-M10BX camera.

Table A–10. CBVM10-6 Cable Pin-Out

trigger-in	Video/sync	Signal Description	15-pin
1,2	–	no connection	–
3	–	Digital ground	5
4,6	–	no connection	–
5	–	CVM10 trigger input, Frame Reset out of PCVision*plus*	9
	1	+12 Volt return	10
	2	+12 Volts DC	15
	3	Analog ground	7
	4	Video input (single-ended)	2
	5	Digital ground	5
	6	HDRIVE horizontal sync	13
	7	VDRIVE Vertical sync	14
	8	Digital ground	5
	9,10	no connection	–
	11,12	no connection	–

NOTE *The "CVM10 Trigger–in" connector carries the Frame Reset signal from the* PCVision*plus to trigger the camera. This is not a trigger input to the* PCVision*plus.*

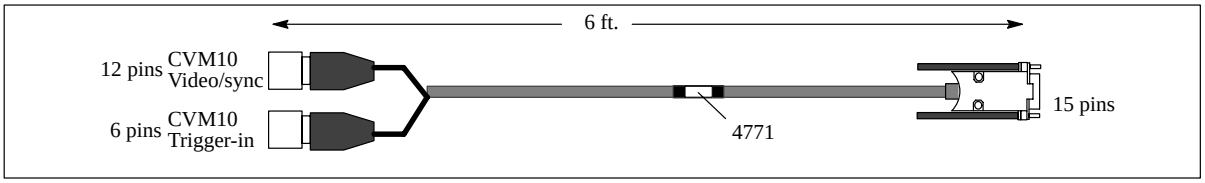


Figure A–7. CBVM10-6 Adaptor Cable

CAUTION *The CVBM10–6 cable before revision* I/P2, *is* ***not*** *compatible with the 15-pin connector on the* PCVision*plus or* PCVision*. The earlier revision cable should only be used with a break-out cable, and not be plugged directly into the 15-pin connector on the frame grabber.*

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JAI CV-M10BX

This cable is compatible with the CV-M10BX Progressive Scan analog monochrome camera. The BX version outputs a pixel clock, and is therefore suitable for Variable Scan mode. The order code for this cable is ACBL–VSCAN. Table A–11 gives the pin-out, and Figure A–8 illustrates this cable. The PCVision*plus* must be programmed to input the Clock on the Frame Reset pin.

Table A–11. ACBL–VSCAN Cable Pin-Out

12-Pin	Signal Description	15-pin
1	+12 Volt return	10
2	+12 Volts DC	15
3	Analog ground	7
4	Video input (single-ended)	2
5	Digital ground	5
6	HD or HDRIVE	13
7	WEN or VDRIVE	14
8	Digital ground	5
9	FRESET out or clock in	9
10	no connection	—
11	no connection	—
12	Digital ground	5

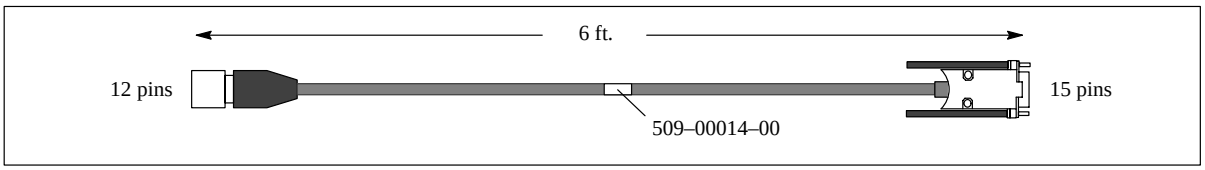


Figure A–8. ACBL–VSCAN Adaptor Cable

NOTE *The CV-M10BX should be triggered using the "Trigger–in" connector on the* ***camera****.*

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APPENDIX B
USING OPTO-ISOLATORS

When connecting industrial equipment to computers and peripherals, it is always recommended you use optically coupled isolators, or opto-isolators. The input plus and minus connections are the two sides of the LED (light emitting diode). The output plus and minus connections are the collector and emitter of an NPN transistor. Figure B–1 shows a single opto-isolator.

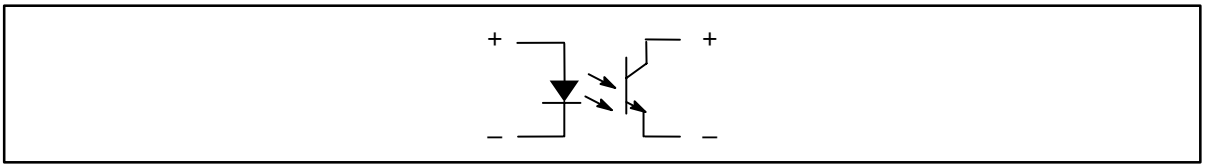


Figure B–1. Basic Opto-Isolator

The PCVision*plus* uses the HPCL-0631 for its opto-isolatoed trigger input. Chapter 1 lists the recommended operating current and voltage values. Do not exceed the absolute maximum ratings of the diode in these devices.

- **Diode Absolute Maximum Ratings** (no derating up to 85° C)

If	15 mA	Forward Current (on)
Vr	5 V	Reverse Voltage (off)
Pi	40 mW	Power Dissipation

- **Transistor Absolute Maximum Ratings**

Vcc	7 V	Supply Voltage (1 minute maximum)
Ve	Vcc + 0.5 V	Enable Input Voltage
Ie	5 mA	Enable Input Current
Io	50 mA	Output Collector Current
Po	60 mW	Output Collector Power Dissipation

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Input Circuits

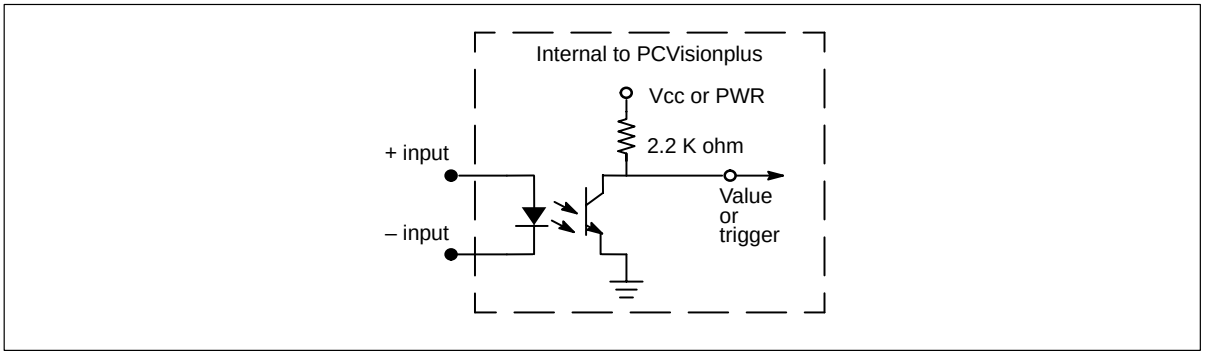


Figure B–2. Opto-Coupled Input Circuit

Figure B–2 shows the internal circuitry in the opto-coupled input. When the diode is excited, the transistor is on, and the internal Value is zero. When the diode is off, the transistor is off, and the internal Value is one. This circuit is used on the otpot-coupled trigger inputs.

Figure B–3 shows a few examples for using the input. The positive input is connected to your logic or signal, and the negative input is connected to ground through a resistor (330 ohm 1/8 Watt shown). The resistor limits current through the diode. The external resistor (1 K ohm shown) limits the voltage across the diode. When the external input goes high the diode turns on, and the internal *Value* (input) becomes zero. When the external input goes low the diode turns off, and the internal *Value* becomes one. The diode and resistors are the Load connected to a sensor output.

The component values depend upon the voltage and current of your circuits. Do not exceed the Absolute Maximum Ratings of the input diode (page NO TAG).

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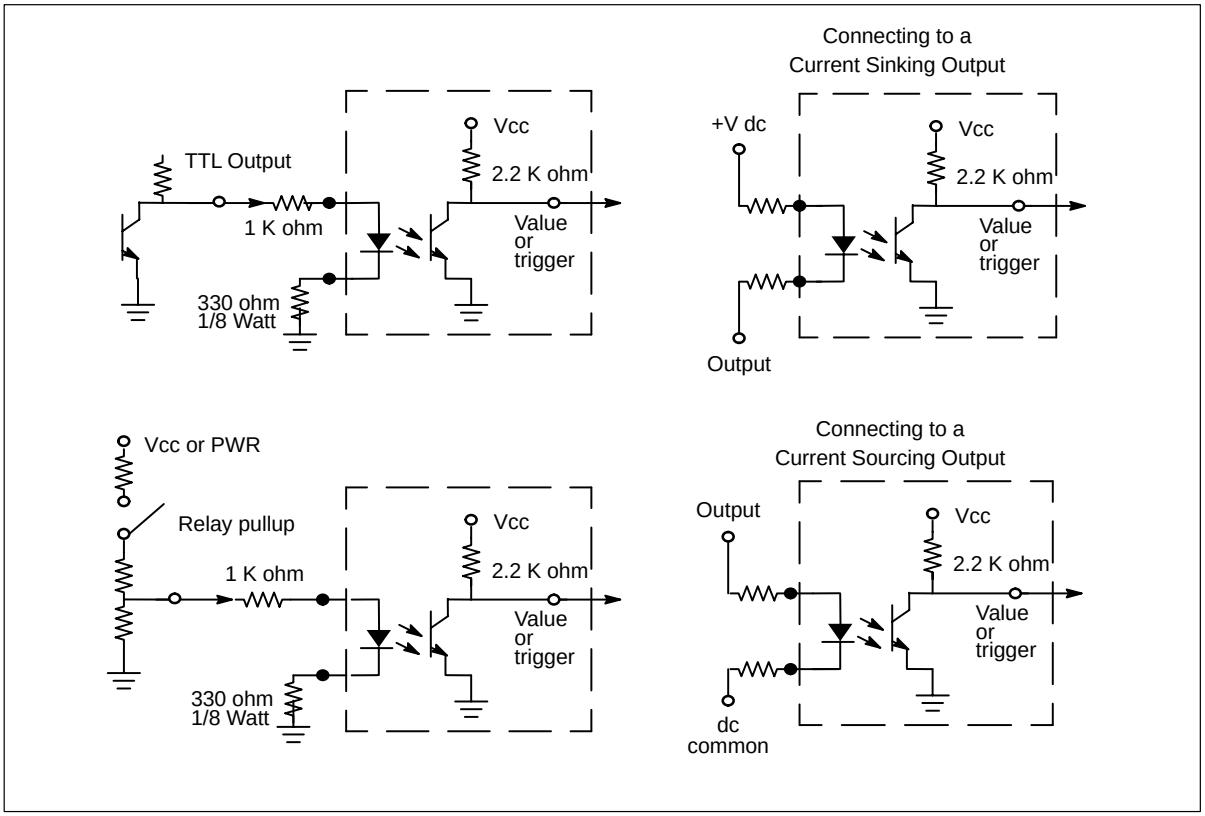


Figure B–3. Input to Opto-Coupled Circuit

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Output Circuits

When connecting industrial equipment to computers and peripherals, it is always recommended you use optically coupled isolators, or opto-isolators. Figure B–4 shows circuitry for connecting an opto-isolator to the PCVision*plus*. The PCVision*plus* does not incorporate opto-isolators, the outputs are TTL and CMOS logic. The positive side of the LED (light emitting diode) is connected to the logic output of the PCVision*plus*. The optional 1K ohm resistor limits the voltage across the diode. The negative side of the LED is connected to ground. The optional 330 ohm 1/8 Watt resistor to limits current through the diode. The opto-isolator output plus and minus connections are the collector and emitter of an NPN transistor. These should be connected to the inputs of your other equipment. When the output is one, the diode turns on and the transistor is turned on. When the output is zero, the diode and the transistor are off.

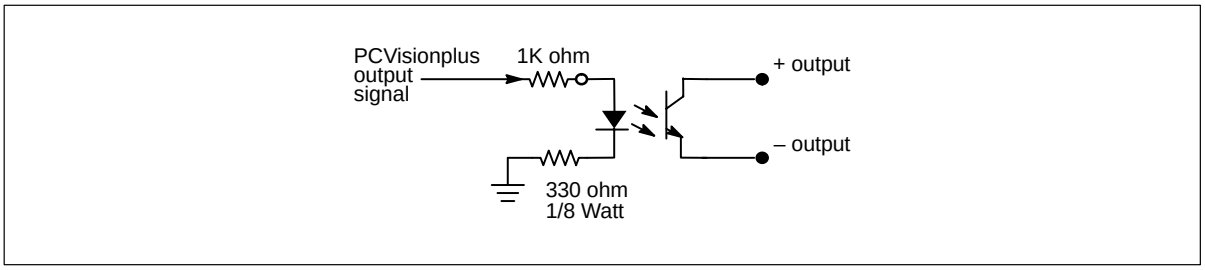


Figure B–4. Opto-Coupled Output Circuit

Figure B–5 shows examples for using opto-isolators on the PCVision*plus* outputs. The positive diode input is connected the PCVision*plus* output, and the negative input is connected to ground. When the PCVision*plus* output goes high the diode turns on, and the internal value becomes zero. When the external input goes low the diode turns off, and the internal Value becomes one. The output transistor can be connected as a Current Sinking Output.

The component values depend upon the voltage and current of your circuits. Do not exceed the Absolute Maximum Ratings of the output transistor.

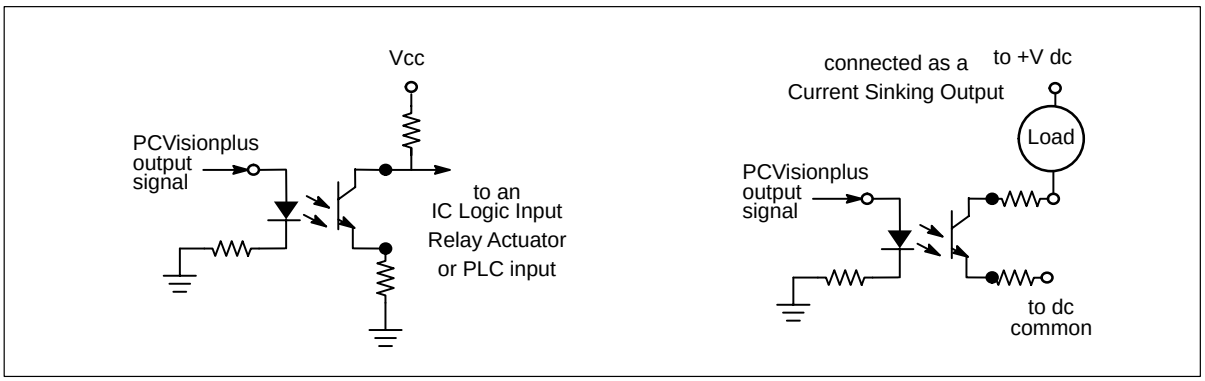


Figure B–5. Output using Opto-Coupled Circuit

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