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In the Ratiohmic™ resistance measurement technique, a voltage is connected across a range-selected accurately calibrated resistance in series with the unknown resistance, and the voltage drop across the unknown resistance is treated as an unknown DC voltage to be measured as before. In phase 3, however, the voltage drop across the calibrated resistance is used as the reference. Because the unknown and standard resistors are in series, the ratio of voltage drops is a direct measure of unknown resistance.

Attenuation components in the Signal Conditioning block are relay operated in response to control signals. These may be initiated by operating the front panel push buttons at the DMM, by control signals transmitted from a remote station via the rear panel connector, or by control signals generated within the DMM when in AUTO ranging.

4.4 TRI-PHASIC A/D CONVERTER BLOCK DIAGRAM (Figure 4-2)

The three phases of performance of the TRI-PHASIC A/D Converter are:

Phase 1: Accumulation and storage of offset

Phase 2: Integration of Input minus offset

Phase 3: Integration of Reference minus offset

In Phase 1 - -

a. Inputs are disconnected from the A/D Converter;

b. Amplifier is clamped;

c. Long-term non-zero offsets are servo-accumulated and stored for later use;

d. Offset is updated continuously until the DMM phase 1 action ends in response to the trigger command.

In Phase 2 - -

a. Clamp is removed and input is connected to the amplifier;

b. Integration of input signal, algebraically reduced by the stored offset value, proceeds for 100 milliseconds as determined by Crystal Clock;

c. Result of the 100-millisecond integration appears as a voltage of the integrating capacitor.

In Phase 3 - -

a. Input is disconnected from A/D;

b. Voltage of opposite polarity is selected from ISO-Polar reference, algebraically reduced by value of stored offset, and the difference integrated to discharge the integrating capacitor linearly to zero;

c. At the zero crossover, end of conversion is generated, and transmitted to digital control circuitry.

4.5 TRIGGER GENERATOR AND CLOCK (Digital Block Diagram, Figure 4-3)

Primary control for DMM measurement is the trigger which initiates each conversion (start of phase 2). The trigger, in its internal DMM circuitry, is generated by the discharge of a capacitor after an RC path charges a capacitor to a unijunction transistor break-down voltage. The trigger is factory selected for a pulse repetition rate of approximately 3 per second.

The trigger may be blocked and a conversion cycle delayed indefinitely by grounding the ENABLE input for as long as desired. The display, or BCD equivalent, is held until a new trigger is generated. In addition, each conversion may be remotely triggered from an external source.

4.6 DECADE COUNTER CHAIN, LATCH, AND DECODER. (Digital Block Diagram, Figure 4-3)

The decade counter chain, latch, and decoder are composed of monolithic IC units (one for each of five decimal digits in each of the counter, latch, and decoder blocks) under control of digital control flip flops.

During phase 2, the counter fills up to 99,999, and the 5th decade carry pulse switches the actions of the Analog block from phase 2 to phase 3 operations.

During phase 3, the counter continues counting until it is stopped by digital control initiated by the EOC (end of conversion) pulse from the A/D Converter block.

The digital control also enables the transfer from decade counter chain to the Latch which acts as an isolating circuit and storage memory. The BCD data are connected to decoder drivers where they activate appropriate decimal lines in the 7-segment plasma display.

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4.7 RANGING (Digital Block Diagram)

Range scaling is accomplished by relays which may be activated in any one of three ways:

a. Manually - by pushing front panel range select push buttons;

b. Automatically - by logic control;

c. Remotely - when in remote trigger control, a discrete range scale may be selected, by grounding directly, or by a logic low level command.

4.8 POWER SUPPLY BLOCK

The Power Supply block may be connected for either a 115-volt or 230-volt AC Source of frequency from 47 to 63 Hz. The block is essentially two separate sets of supplies, driven from the same input transformer primary. The analog supply is triple shielded, floating, and incorporated in a "guarded" area for proper isolation. It develops $\pm$ 15V regulated supply voltage for the analog circuitry, -5V for the digital control in this section, and develops the 6.2 volt, oven controlled, extremely low temperature coefficient, reference source for the A/D Converter. Common ground for the precise reference is used as the high voltage for the isolated digital control section, where the low voltage level is the -5 volts.

The transformer primary drives three additional secondaries whose outputs are rectified and provide +20 volts for relay operation, +180 volts for display operation, and a regulated +5 volts for digital logic. These appear in the digital section of the converter and use the digital ground as their return.

4.9 DETAILED OPERATION

A more complete function diagram of the Model 3500 DMM is illustrated in Figure 4-5. The major blocks comprising the unit are divided into subunits or are repeated to indicate the several functions performed sequentially by the block, and this division forms a basis for complete systems understanding, detailed circuit explanation, and maintenance. Complete schematics, from which simplified schematics and block diagrams have been derived, are contained in Section 6 and are prepared as fold-outs for convenient reference when reading the following text.

The sequence of functions illustrated in Figure 4-5 consists of the following:

1. Measuring Mode and Range are selected. Proper attenuation elements for the selected range are connected in the Signal Conditioning block, and in the pre-amplifier block.

2. Input signal is applied.

3. Prior to the trigger pulse starting a conversion measurement, the A/D Converter input is clamped, and the Signal Conditioning output is removed from the A/D Converter. During that time, phase 1 drift integration proceeds and the self zeroing circuit determines the A/D amplifier accumulated drift and stores it for phase 2 and phase 3 operation.

4. Following the trigger pulse generated in the Timing & Control unit;

   a. The clamp is removed from the A/D Converter.

   b. The Signal Conditioner Output is connected to the input of the A/D Converter.

   c. The self-zeroed drift is introduced as an algebric negative offset.

   d. The counter is reset to zero and starts its fixed count for the phase 2 integration.

5. When the count has reached 100,000 (100 millisec.),

   a. The second integration is stopped.

   b. The sign of the input is interrogated by strobing the integrator output.

   c. The unknown signal input is removed from the integrator.

   d. The appropriate polarity of internal reference voltage is applied to the A/D input.

   e. The reference voltage reduced algebraically by the stored drift (as in phase 2) is integrated during phase 3 integration.

6. When the integrated reference compensates the integrated unknown input (when the output of the integration returns to the starting point),

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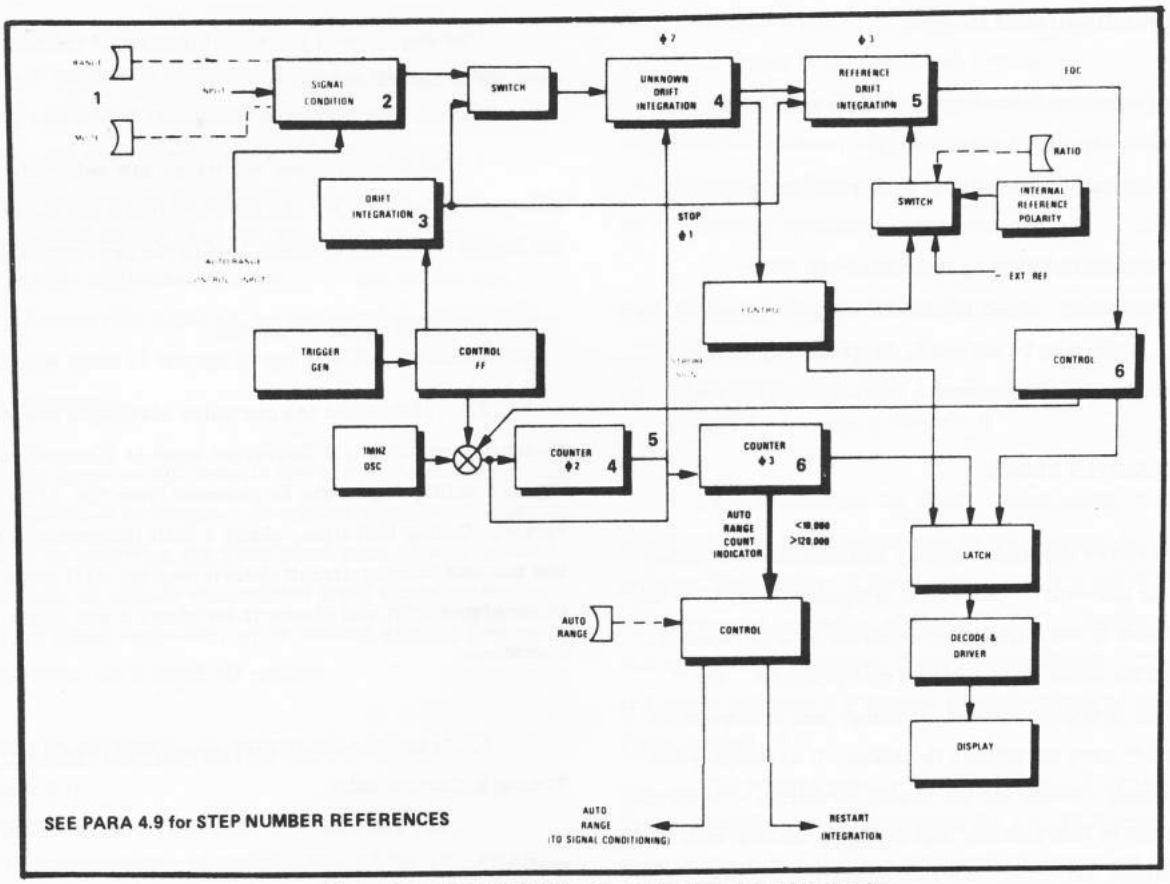


Figure 4-5 Model 3500 Functional System Block Schematic

a. Phase 3 integration process ends.

b. The input clamp is reestablished.

c. The clock input to the counter is stopped.

d. A READ OUT signal is transmitted indicating End of Conversion.

e. The accumulated count is transferred to the display.

The timing sequence is illustrated in the chart of Figure 4-6, indicating the three phases of the operation.

Detailed explanations of these functions are presented in the following sequence:

a. Input signal conditioning (Figure 4-5A)

b. Phase 1 Drift Integration

c. Phase 2 Unknown-Drift Integration (Figure 4-5C)

d. Phase 3 REFERENCE-DRIFT Integration (Figure 4-5D)

e. Digital Control and Display (Figure 4-5E)

f. Ranging circuits and Remote display and control functions.

4.10 SIGNAL CONDITIONING DETAILS

a. DC VOLTAGE

Input DC voltages are applied through the HI and LO input terminal, and connected to the input attenuator network through the contacts of Mode Switch S12 and S13 when placed in DC Volts Mode. Replay actions of K1 and K2, determined by the range selection, then establish the attenuator actions.

A simplified schematic of the DC Voltage signal Conditioning action is shown in Figure 4-7.

The relay pair (K1A and K1B) and relay K2A provide four range selections from 1V Full Scale to 1000V Full Scale. (Range change from 1.0V to 0.1V Full Scale is accomplished in the A/D Converter.) Action of the relays and resultant attenuation of the input signal on the different range scales are summarized by the table below.

Full Scale Range Select	Relay K1 1/100	Relay K2 1/10	Result. Atten.
1 Volt	OFF	OFF	1
10 Volts	OFF	ON	1/10
100 Volts	ON	OFF	1/100
1000 Volts	ON	ON	1/1000

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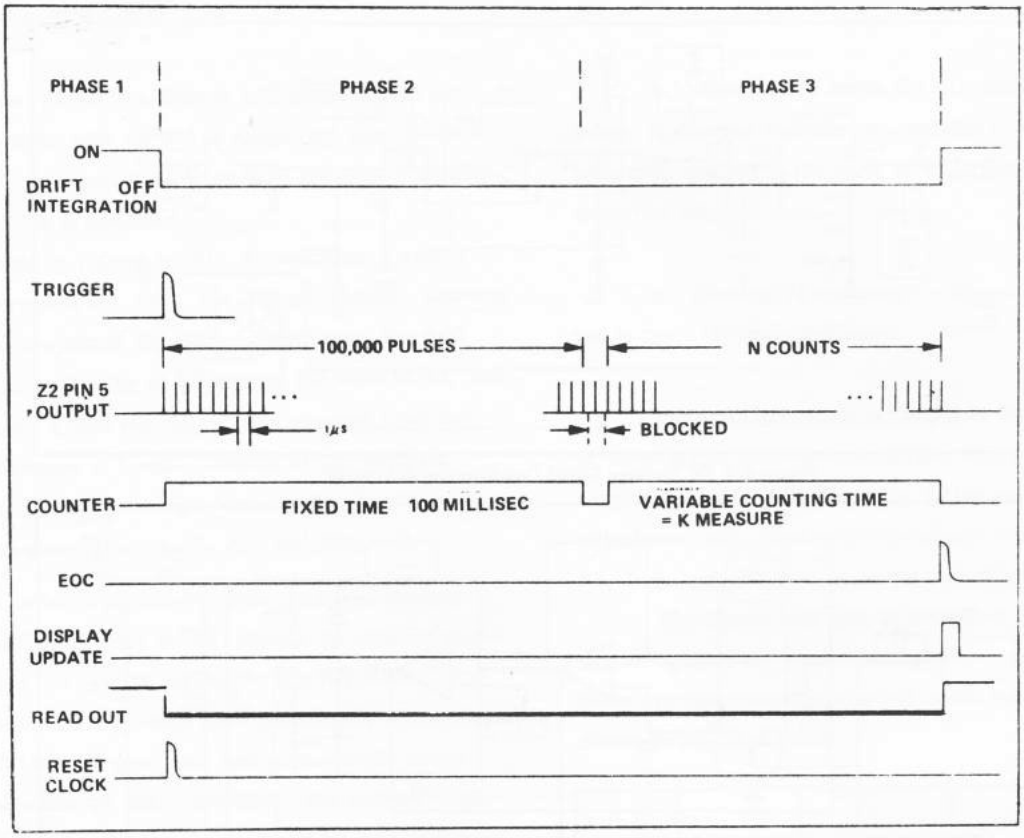


Figure 4-6 Tr-Phasic logic and control waveforms.

Full scale voltage delivered to the A/D Converter is 1 volt on all ranges except the 0.1 Volt scale. In that range the full scale output of the Signal Conditioning block is 0.1 volt. In all cases, overrange values, up to 120% of full scale are converted accurately in the A/D Converter, up to a maximum input of 1000 volts DC.

The signal conditioner amplifier is a high impedance, unity gain, isolation unit, provided with voltage and current offset adjustments. It is connected only when relay K2 is activiated. The input network, including R121 and R117 and the biasing diodes, is designed to protect the Multimeter from accidental connection of high voltages up to ± 1000 volts regardless of the range selector setting.

When not in DC Volt Measurement Mode, the input is removed from the indicated circuitry.

b. AC Voltage

In AC Voltage Mode, the input is connected to a broad band active attenuator followed by an active rectifier and filter. Networks in the feedback path of the input amplifier determine the attenuation for the selected full scale range. Capacitor trimmers are adjusted to maintain constant feedback ratios over the range of input signal frequencies. Manual push button action or automatic ranging signals control the relay-operated selection of the appropriate attenuation decade. A simplified schematic of the circuit is shown in Figure 4-8. This illustrates the amplifier Z26 and its feedback decades, the half-wave rectification of the second amplifier Z Z27 output, and the low pass filter R27, C26, which passes the average DC component of the rectified output.

The filtered, rectified DC Voltage output is thus scaled to the RMS value of the applied input signal and connected to A/D Converter via the switching circuit.

4.11 RATIOHMIC RESISTANCE INPUT CONDITIONING DETAILS

Connections for Resistance measurements are shown in the schematic of Figure 4-9. The unknown resistor R_x is made part of a resistance series set consisting of a selected range scale resistor, R_S, the undetermined contact resistances Rc_1 and Rc_2, and itself. This set is driven from the temperature controlled +6.2V reference voltage.

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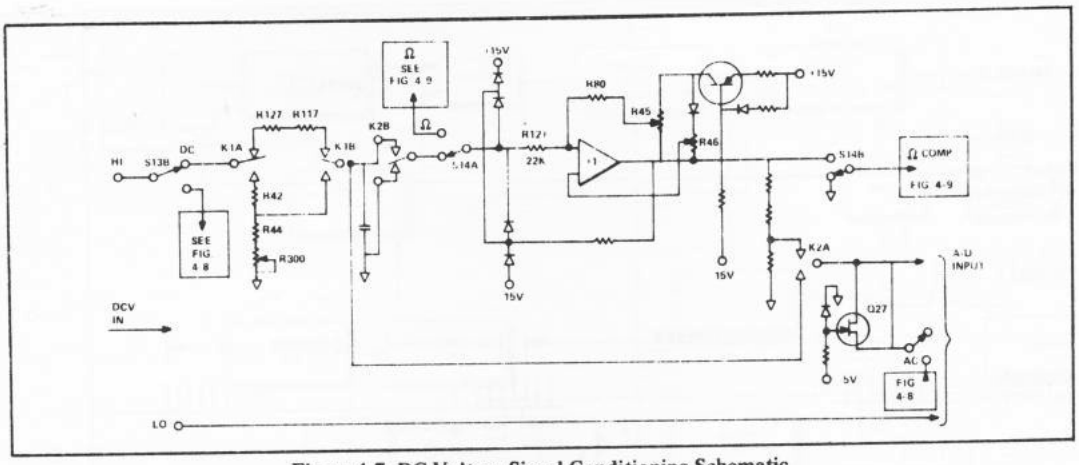


Figure 4-7 DC Voltage Signal Conditioning Schematic

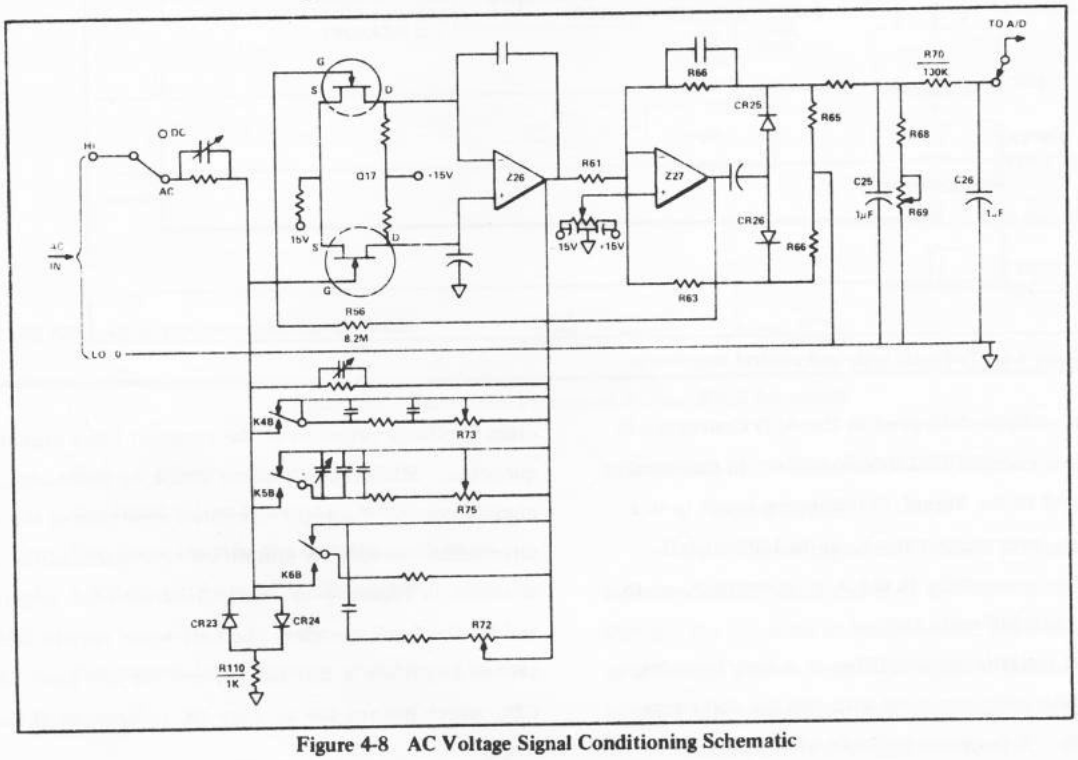


Figure 4-8 AC Voltage Signal Conditioning Schematic

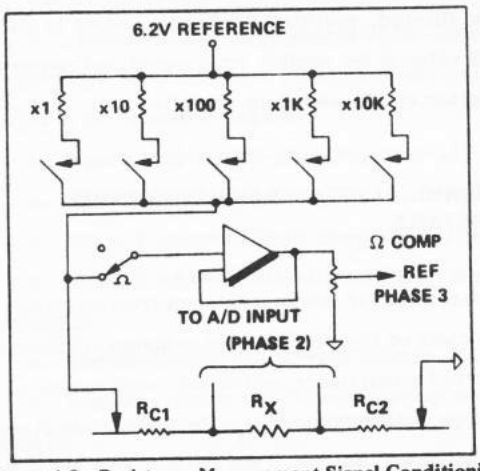


Figure 4-9 Resistance Measurement Signal Conditioning

During phase 2, the voltage drop across Rx is connected to the A/D Converter where it is processed in the same manner as a DC input signal. During phase 3, the voltage drop across the selected range scale resistor is buffered by the unity gain amplifier, divided by 6.2 using the calibrated divider network, and connected to the converter as the Reference input.

The indicated circuit operation features the following:

a. The same current develops the unknown and reference voltage signals.

b. The contact resistance voltage drops do not affect performance.

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4.12 A/D CONVERTER DETAILS

Operation of the Tri-Phasic A/D Converter in its 3 phases is described with the aid of simplified schematics of Figure 4-10A and Figure 4-10B, derived from the complete reference drawing in Section 6.

Referring to Figure 4-10A, during phase 1 switch Q1 is open, switches Q2, Q23, and Q25 are closed. Opening of Q1 removes the Signal Conditioned input from the A/D preamplifier A1. Closing of Q2 clamps the input to A1, and, with Q23, closes a path whereby C34 is charged from the ISO-Polar reference to 1 volt. Closing of Q25 permits capacitor C36 to store a charge compensating for the accumulated non-zero offset in A1, A2, and Z29.

Appearance of the trigger pulse in the secondary of transformer T2 (Figure 4-10B) signals the start of phase 2, and initiates the control actions by flip flop Z31A. The trigger causes pin 5 to go high and consequently Q1 to close. The output Z31B pin 8 goes low, and consequently opens transistor switches Q2, Q23, and Q25. The actions of Q3 and Q4 are determined by the selection of 1V or .1V range.

a. Opening Q23 opens the charging path to C34 (Figure 4-10A) and leaves C34 charged to 1 volt and isolated during phase 2.

b. Opening Q25 opens the charging path of C36 and leaves it charged with the accumulated compensation for zero drift applied to the input of the differential integrating amplifier A2.

c. Closing Q1 connects the Signal Conditioned output to the A/D Converter input.

Phase 2 integration action takes place in the chain of three active elements: amplifier A1, amplifier A2, and amplifier Z29. Amplifier A1 is a high gain, high input impedance, low offset amplifier whose feedback resistors R9, R10, and R15 determine the closed loop gain.

The closed loop gain of amplifier A1 is either 8 or 80 depending upon the condition of switches Q3 and Q4, and these are determined by the full scale range selection as shown in the table below.

F.S.R. Select	Q3	Q4	AMP Gain	
			Ø2	Ø3
Not .1	0	1	8	8
.1	$\overline{Ø3}$	$\overline{Ø2}$	80	8

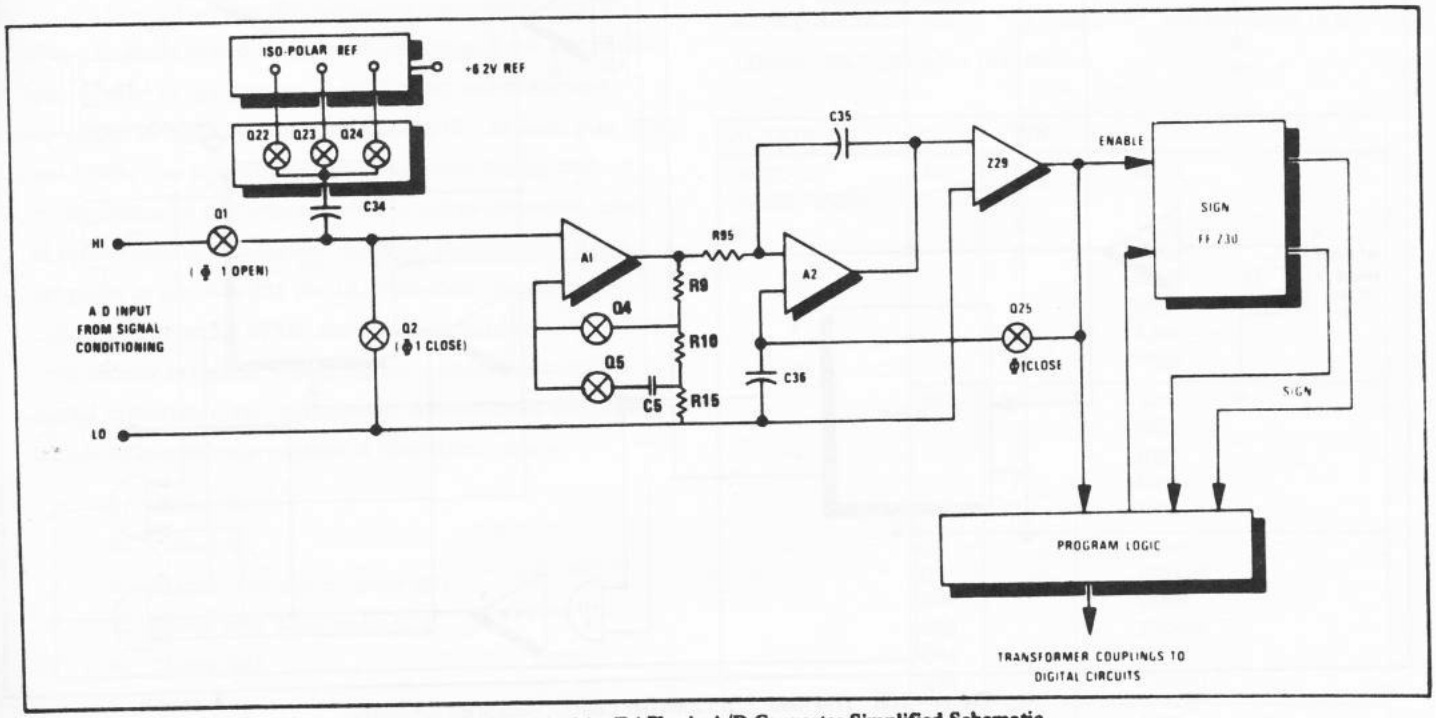


Figure 4-10A Tri-Phasic A/D Converter Simplified Schematic

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As indicated in the table above, the amplifier gain is 8 for both signal input integration and for reference input integration for all range scales except .1. On the .1 range scale, the gain is changed by a factor of 10 from ϕ2 integration (signal input) to ϕ3 integration (reference input). Thus, a 0.1 volt full scale input is conditioned to the 1V full scale so that the precision reference and voltage need not be changed. The values of R9, R10, and R15 accomplishing this scale factor change are 7.1 5K, 900, and 100 ohms, respectively.

The function of C5 is to maintain the amplifier offset in the circuit through the switching action.

The output of amplifier A1 is one input to integrating amplifier A2 whose integration constant is determined by C35 and R95. The other input to amplifier A2 is the voltage on C36, the stored value of the voltage compensating for the accumulated zero offset dervied in phase 1.

Output of amplifier A2 drives high gain amplifier Z29 to saturation during phase 2. Its output polarity is used to indicate the sign of the unknown input.

Phase 2 integration proceeds until the appearance across the secondary of T4 of a positive-going pulse signalling a 10^5 carry from the digital block. This now appears as a negative pulse clocking flip flop Z30A pin 2 and as a direct set for flip flop Z31A (pin 4). The resulting actions controlled by these flip flops initiate the phase 3 operation of the A/D Converter.

The output, pin 5, of Z31A, which had been high from the start of phase 2, now goes low, opening Q1, and thereby removing the signal input from the A/D amplifier. Action of flip flop Z30A in response to the clocking pulse depends upon its input conditions just prior to receiving that pulse. This in turn was determined by the output of amplifier Z29 during phase 2. Amplifier Z29 was driven to saturation in the positive or negative direction corresponding to the sign of the input signal.

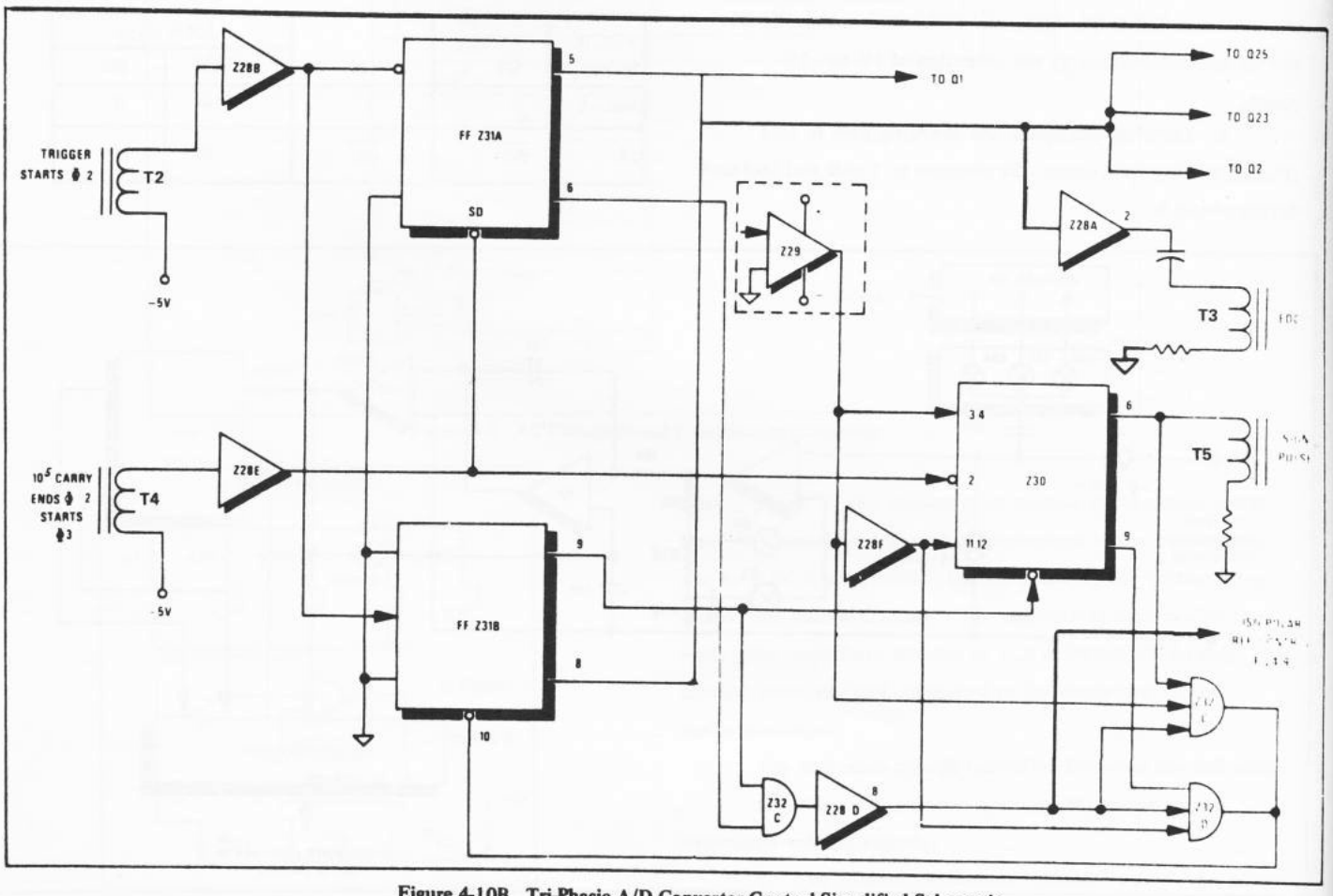


Figure 4-10B Tri-Phasic A/D Converter Control Simplified Schematic

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If the input signal had been positive, Z30A pin 11 would have been low and the clocking pulse would not have changed the high level at pin 6, thus producing no pulse across the primary of "sign" pulse transformer L5. If the input signal had been negative, Z30A pin 11 would have been high and the clocking pulse would cause Z30A pin 6 to go low producing a pulse across the transformer T5 primary and transmitting a negative sign indication to the Digital circuitry. The voltage level deveoped by flip flop Z30 at pin 9 controls the sign of the reference signal to be switched to the amplifier input at the start of phase 3. (Refer to Figure 4-11 in conjunction with Figure 4-10B.)

During phase 2, both Q22 and Q24 are open. The low level output at Z30 pin 9 had kept Q22 open; and the output of Z28 pin 6 had been clamped low through CR28 to Z28D, keeping Q24 open. If the input signal had been positive, Z30 pin 9 would have remained low, keeping Q22 open. The carry pulse control action removes the clamp on the Z28 pin 6 output permitting the output of Z28 pin 6 to go high, closing Q24. This action places the high side of C34 at reference zero potential and negative one volt at the A/D amplifier input. If the input signal had been negative, Z30 pin 9 would go high, closing Q22 and connecting the high side of C34 to reference +2V causing a positive one volt at the A/D amplifier input.

Control actions for the end of conversion (end of phase 3) are initiated by the zero crossing of the Z29 output, sensed by the gating action of Z32C and Z32D, and developed in digital control flip flops Z31. At each gate Z32C and Z32D, two of the three inputs are high during phase 3. As the output of Z29 crosses zero in either direction, one of these gates is enabled and develops the negative direct set pulse at flip flop Z31 pin 10. The Z31D output goes high, is inverted by Z28A, and develops a pulse across EOC transformer primary, signalling end of conversion to the digital circuitry. The Z31D output also controls the resetting of A/D converter to phase 1 operation. It - -

a. Closes Q25
b. Closes Q2
c. Clamps Z28 pin 6; opens Q24
d. Direct sets Z30; opens Q22
e. Closes Q23
f. Opens Q1.

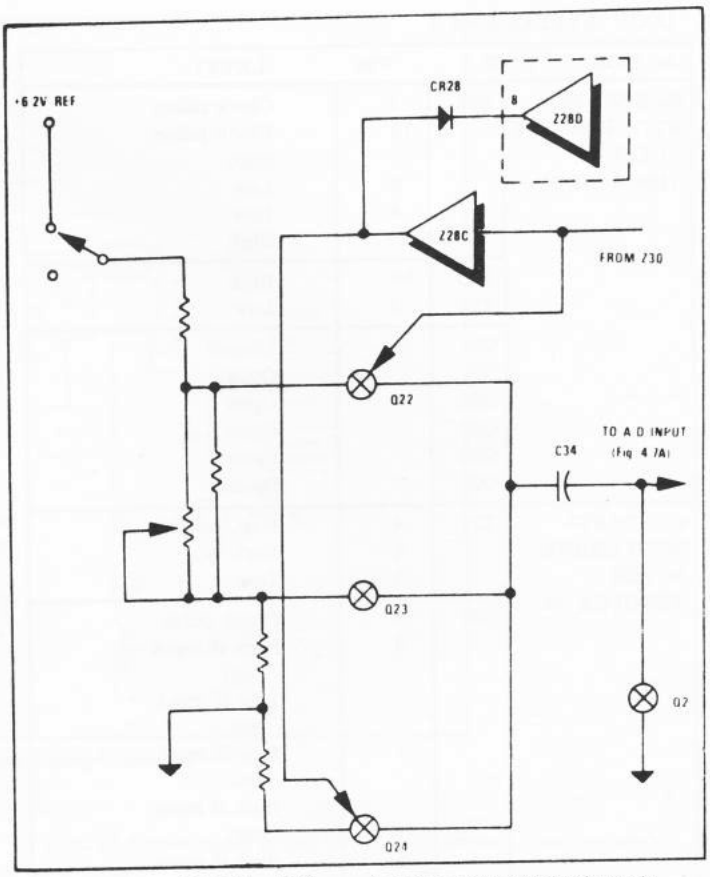


Figure 4-11 ISO-Polar Reference Switching Simplified Schematic

In summarizing the actions of the A/D converter circuitry during the three phases of operation, the levels and signals of the gates, flip flops, etc. are tabulated in the LOGIC LEVELS tables that follow.

ACTION	Z	PIN	LEVEL
INITIAL CONDITIONS Ø1	Z31	1	High
		2	High
		4	High
		5	Low
		6	High
		8	High
		9	Low
		10	High
	Z30	10	Low
		3	High
		6	High
		9	Low
		11	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
	Z28	8	Low

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LOGIC LEVELS (cont.)

ACTION	COMP	PIN	LEVEL
Ø2 STARTS WITH POSITIVE PULSE THROUGH T2	Z31	1	Clock pulse
		13	Clock pulse
		5	High
		6	Low
		8	Low
		9	High
	Z30	10	High
	Z28	8	Low
	Q1		Closed
	Q2		Open
	Q22		Open
	Q23		Open
	Q24		Open
	Q25		Open
Ø3 STARTS WITH CARRY PULSE THROUGH T4	Z31	4	Neg. pulse
		6	High
		5	Low
	Z30	2	Clock pulse
		3	High if input pos. Low if input neg.
		11	Low if input pos. High if input neg.
		6	High if input pos. Low if input pos.
		9	High if input neg. Low if input neg.
	T5		Pulse if input neg. No pulse if input pos.
	Z28	8	High
	Q1		Open
	Q2		Open
	Q22		Closed if input neg. Open if input pos.
	Q23		Open
	Q24		Open if input neg. Closed if input pos.
	Q25		Open
END OF Ø3; Z29 PIN 7 CROSSES ZERO	Z32	6 or 8	Goes Neg. pulse
	Z31	10	Low
		8	High
		9	Low
END OF CONVERSION; NEGATIVE PULSE THROUGH T3	Z30	10	Low
		6	High
		9	Low
	Z32	8	High
		6	High
	Z28	8	Low
	Q1		Open
	Q2		Closed
	Q22		Open
	Q23		Closed
	Q24		Open
	Q25		Closed
RETURNING TO Ø1 OPERATION			

4.13 TRIGGER GENERATOR AND COUNTER

a. Trigger Generation

The trigger pulse initiating each conversion process may originate either from an external source or from internal circuitry shown in the simplified form of Figure 4-12. Capacitor C1 charges toward +5V through R15 until the firing voltage of Q40 is reached. A pulse approximately 100 μsec wide and 4 volts magnitude is developed across R16 and connected to J input of the control flip flop (Z2 pin 2). The sawtooth charge-discharge singal and the resulting trigger timing signal waveforms are shown in Figure 4-12.

The trigger control signal is inverted through Z21-, and then is gated through Z21- External input at terminal J, ENABLE, is normally high, permitting the internally generated trigger signal to be gated to flip-flop Z2A, where it is connected to the J terminal as a high logic level input.

Flip-flop Z2A, which has been reset by the end of conversion pulse, will have a low level on output pin 5 and a high level on pin 6. At the first clock pulse after the trigger, Z2A transfers the high J input level to the output, pin 5, which then enables gate Z3B and transmits succeeding clock pulses through to the counter chain. Z2A pin 6 goes low at the same time and, through inverter Z1-12 generates a counter reset pulse. An invested reset pulse is used to reset the under-and over-range flip-flops Z20A and Z20B.

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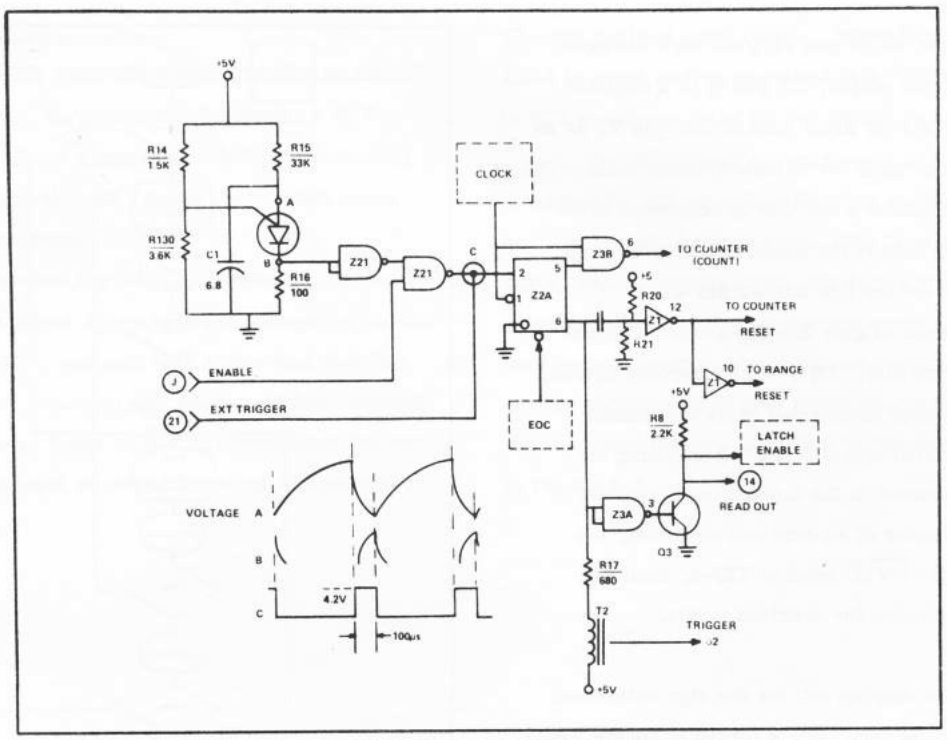


Figure 4–12 Trigger and Timing Generator

The low level on pin 6 of Z2A also transmits a pulse through transformers T2, to initiate phase 2 of the triphasic conversion cycle.

After inversion through Z3 pin 3, transistor Q3 conducts; its collector goes low, isolating the latching circuit from the counter. The latch and display retain the stored count until the next conversion update, and an output signal, READOUT, is available at the rear panel connector to indicate this event in the cycle. This is a High (T^2L/DTL) output level between conversions.

The leading edge of the negative going waveform is differentiated (C5, CR20, and R21) as the input to Z1 (pin 12), inverted, and generates a positive going pulse to reset the decade counter IC's, Z4 through Z8.

The inverted counter reset pulse, at the output of Z1 (pin 10) presets the range control flip flops Z20 pin 10 and pin 4, and Z2 pin 10.

b. Counter Chain (Figure 4-12)

The crystal-controlled clock is a series-mode crystal circuit consisting of crystal Y1 and inverter Z1. It develops 1 MHz pulses which are gated into the counter during phases 2 and 3. The counter registers accumulate the count during phases 2 and 3 until receipt of the EOC (End of Conversion) pulse at the EOC transformer secondary. This resets flip flop Z2A, and pin 5 goes low, blocking the timing pulses at gate Z3 5-6. Simultaneously, Z2 pin 6 goes high cutting off Q5, collector voltage goes high, permitting the count in Z4-Z8 and Z2B to be transferred to the latches, and through them to the decoding and display driving registers Z15 and Z19.

Outputs of the counter chain are transferred through the latching registers as BCD data. These are immediately available at the tab connector of the DMM rear panel for remote display or control purposes. In the DMM, the decoding registers Z15 through Z19 convert BCD to decimal signals.

If the DMM is in a manual range selection, and the developed count in phase 3 is less than 120,000, the conversion cycle is complete.

c. Overload

If an end of conversion pulse is not received during phase 3 by the time the counter reaches 120,000 (a display of 120,000), an OVERLOAD condition exists, and this event is sensed at gate Z3. One input to Z3 (pin 9) is set at a high level by the toggled output of Z20 pin 5 when the count reaches 10^5 in phase 3. When the counter reaches

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20000, the second input to Z8 (pin 10) goes high and activates the gate. The gate output, Z3 (pin 8) is a negative waveform, available at rear panel connection, pin Y, as an OVERLOAD indicating signal for remote transmission. The overload indicating negative level also is connected at the output of Z1 pin 2 and acts in the same circuitry through Z11 pin 2 as a direct set for flip flop Z2 pin 4.

The OVLD output of gate Z3-8 is a control signal for the most significant digit, DS1, via its decoder driven, Z23. At the start of each conversion cycle the counter is reset, and this control signal is high, permitting the "1" to be lighted if present in the latched count register. Then, if the conversion is of an overload condition, the "1" is turned off by the $\overline{\text{OVLD}}$ input to Z23-4, resulting in the blinking MSD display for overload inputs.

d. Sign

DS1 is also the display unit for the sign indication. It is enabled in DC mode only, and is turned on by the action of the sign pulse transformer T5 via latch flip flops Z14. It is strobed into the first latch at carry pulse and transferred to second latch at EOC.

4.14 RANGING

4.14.1 General

As shown in Figure 6-4, all range scale selections are controlled by the actions of Relays K1 through K7, and decimal point selection is slaved to the relay action. Each relay activation is controlled by drivers contained in integrated circuit Z34, and they, in turn, may be controlled either by the operation of the automatic ranging digital logic, or by the manual operation of front-panel push buttons or remote signals. Signals controlling the relay drivers simultaneously operate the appropriate transistor control of the displayed decimal point.

Figure 6-4 also includes a matrix chart relating the states of the relays for each selected range scale. It also includes the necessary states of the 3 auto range flip-flops for the same results.

4.14.2 Auto-Ranging

The auto-ranging logic responds to the measured input when less than 10000 counts or more than 120000 counts according to the logic flow shown in Figure 4-13.

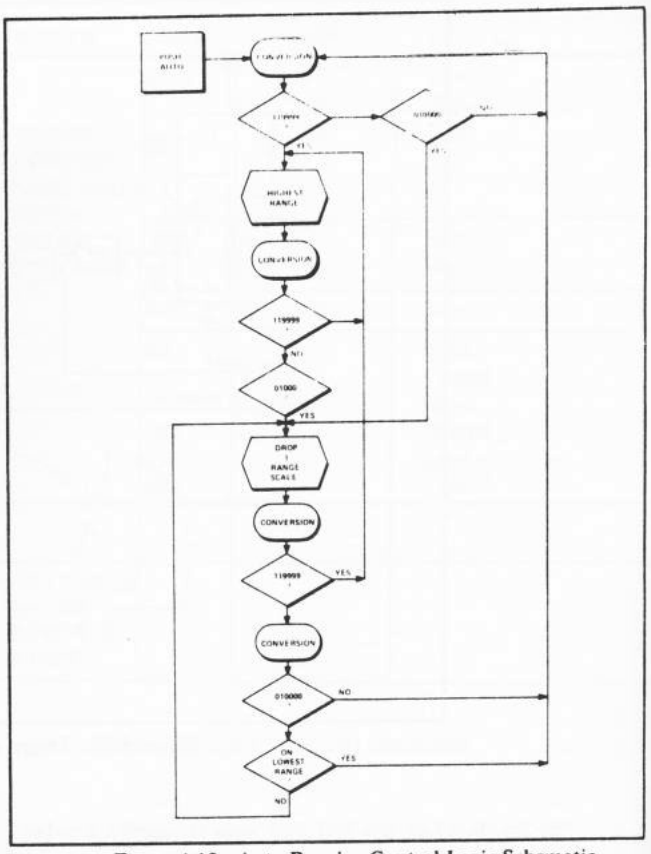


Figure 4-13 Auto-Ranging Control Logic Schematic

After the AUTO push button is operated, each conversion is sensed by the DMM circuitry, which responds as shown in Figure 4-13, and as described below.

a. At any time that a value greater than 119999 counts is sensed, the cricuitry switches the meter to the highest range (1K for voltage, 10K for ohms) for the next conversion.

b. If, after switching to the highest range, the next conversion measures a value less than 10000, this underrange condition is sensed, and the circuitry drops the range scale to the next lower range.

c. Thereafter, two successive underrange conversions are required before the range scale is changed to the next lower one.

d. Lower range scales are switched in until the lowest scale has been selected.

e. An overrange sensing causes a highest range scale selection at any time it is sensed.

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4.14.3 Auto Ranging Instrumentation

The auto ranging instrumentation includes an underrange storage flip flop, three control flip-flops, a BCD to decimal converter, and a hex-driver integrated circuit, in addition to the decimal point drivers, overrange sense gates, and manual switches.

Gate Z21-3 senses the overload condition (10^5 and 2×10^4 inputs). Its output direct sets for voltage (or resets for ohms) flip-flop Z26, and sets both of the dual J-K flip Z22. In the overload condition, all outputs of these control flip-flops are low level (logic "0"). Z27 translates the 000 input to place a high level on output terminal 1 to energize K7, and decimal point $DP10^4$. When in voltage measurement Z26A is reset so that its output is a "1", and the 100 input to Z27 results in relay K6 and $DP10^3$ being activated.

The underrange measurement (under 10000 counts) is sensed by Z24 when that flip-flop is enabled by the $\overline{\text{READ}}$ control (at end of conversion). The Q output of Z24 toggles Z26A, which, together with Z22 forms a binary counter up to the count of 6 (101), so that the seven states 000 to 101 may be translated by the binary-to decimal decoder Z27, and the outputs of Z27 may select the correct relays and decimal point drivers according to the tabular array included in Figure 6-4.

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Chapter 5

MAINTENANCE

5.1 GENERAL

Model 3500 Digital Multimeter usessolid state components and integrated circuits (except for display tubes), and are designed for reliable long-life operation. Except for calibration verification, no operator maintenance should be required, and there should be no normal requirement for opening the DMM case. Should any malfunction require corrective action within the warranty period, arrangements should be made to obtain factory assistance.

CAUTION

Data Precision provides this maintenance information primarily for users of Model 3500 Digital Multimeters in need of repair after the expiration of the Warranty period. The information is intended for users who are qualified and competent to effect any needed repairs. The equipment may be returned for repairs at a nominal fee if the user should elect to have the factory make repairs.

Should the qualified user attempt to troubleshoot and repair the DMM, he will find that Model 3500 DMM contains a number of features especially designed for simplified unambiguous troubleshooting and fault indication. Among these are:

a. Full and complete design and parts data in this Instruction Manual;

b. A positive troubleshooting procedure intended for effective use by competent technical personnel in isolating and correcting all but the most subtle and intricate problem sources;

c. Mechanical parts layout and identification for logical and easy location.

5.2 PARTS GROUPING AND THE TEST STAND-OFF GRID

The printed circuit board is etched to show the grouping into major functions of the components (Figure 5-1). These correspond, genrally, to the schematics in Section 6. The separate groups are individually named, the designations appearing along the edge of the board. When the Guard Shield is removed, the floating Analog power supply and the analog portion of the A/D Converter and Signal Conditioner are revealed. The two amplifiers of the A/D Converter and the CLAMP/UNCLAMP switching module are separate modular components. They are mounted on the base PC board as integral component assemblies.

Verifying signal values throughout the circuit is considerably simplified mechanically by strategically positioned stand-offs, connected to circuit components for easy access to points where performance may be monitored. Each installed stand-off is identified by an E-number on the schematics, and etched on the PC board. Access to every major critical portion of the circuit has been assured.

The troubleshooting and maintenance procedures are intended for experienced technicians. Use of the flow chart directs the technician to the appropriate circuitry and reference schematic for subsequent detailed component fault isolation, replacement and repair.

5.3 THE TROUBLESHOOTING FLOW CHART

Figure 5-2 is a coded plan for troubleshooting Model 3500 DMM. The chart presents the logical sequence for performing tests so that an interpretation of test results will isolate the circuit components that are functioning properly. The complete sequence then leads the technician to the only components that may be the source of trouble.

Signal tracing the isolated faulty circuit group and reference to the schematic for correct values normally will uncover the faulty component.

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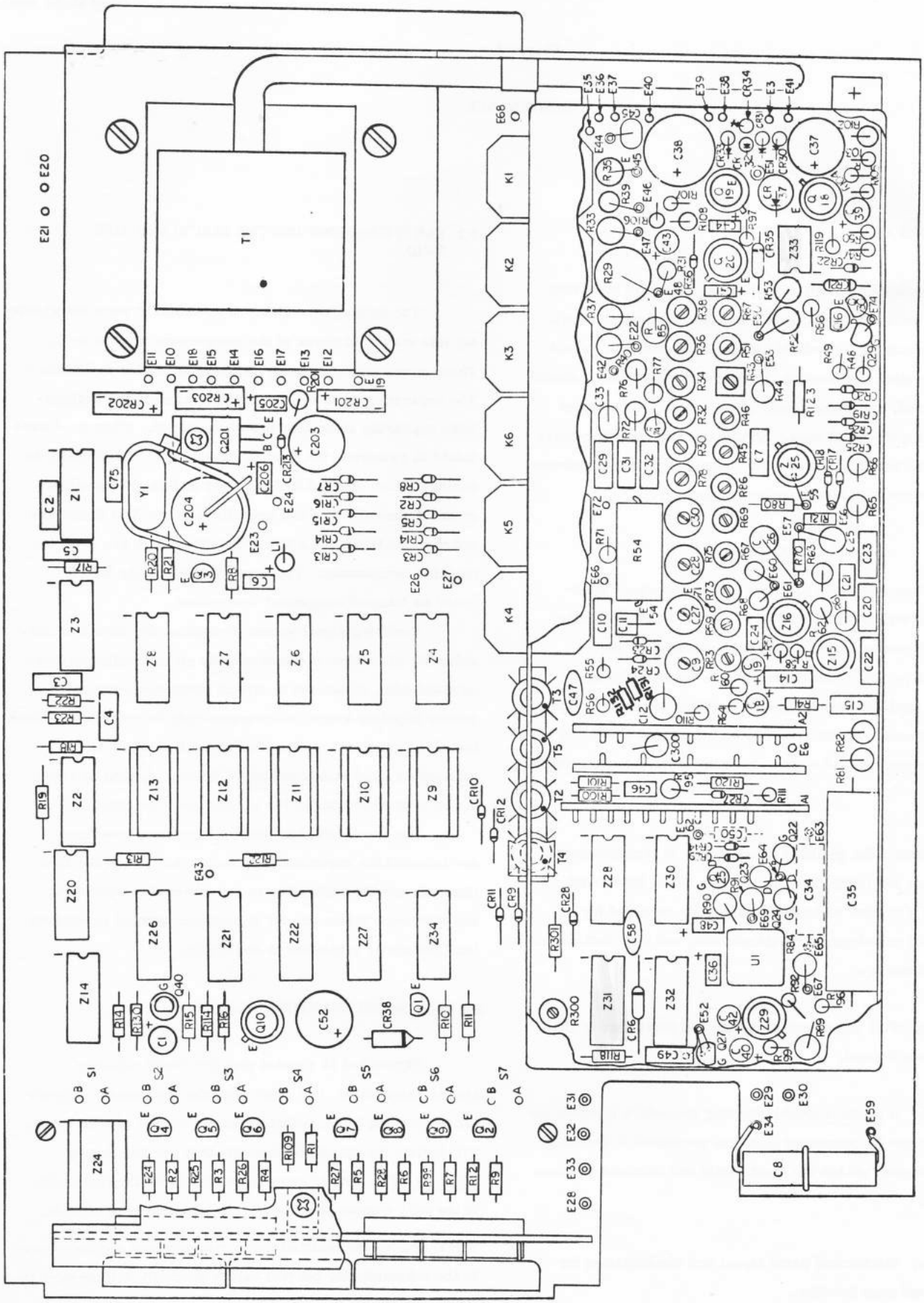
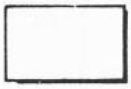


Figure 5-1. Parts and Stand-Off Layout on PC Board Assembly

A standard graphic code has been used in the flow chart:



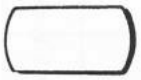
Set Up Instructions. Define input stimulus value and where applied.



Measure parameter (volts, amps, ohms)



Following measurement, evaluate for next path step



Remove and Replace if unique and unambiguous (Multiple source of malfunction possible)

5.4 USING THE TROUBLESHOOTING FLOW CHART

As shown in Figure 5-2, one starts by activating the POWER push button and checking to see if the Display comes ON. If not, the chart directs the maintenance man to perform Test No. 1 as defined in the integral Table of Tests. Test No. 1 calls for the measurement of a DC voltage between stand-offs E18 and E19, and checking for a nominal voltage of 180 volts. If the voltage is present, then, according to the chart, it is concluded that the display and its circuitry are in need of further fault isolation.

If the voltage check of Test No. 1 indicates an incorrect value of the DC voltage, then the chart directs the maintenance technician to use Reference Dwg. Sheet 5 and to measure the other output voltages in accordance with Tests 2.1 and 2.2. The Tables of Tests also indicate the driven circuits for each of the supply voltages. These may be the cause of incorrect voltage measurements when checking power supply elvels and should be checked for excessive current drains by examining driven components and their nearby components for signs of elevated temperatures. The reference drawing includes the pin identification of the components driven by each supply.

Continue through the flow charts as directed, and the successive steps will confirm the proper operation of incremental portions of the DMM as they contribute to the performance as a whole. An incorrect reading in any step identified the circuit components as a group within which the malfunction most probably originates.

The testing sequence represented by the charts beginning with Figure 5-2 is concluded with a calibration to complete the maintenance process. Complete DMM function will have been verified by this process, but only those coded outputs actually tested are verified. Any pattern of missing digits may not be detected in these tests, and such a symptom is indicative of a malfunctioning counter, latch, or decoder IC.

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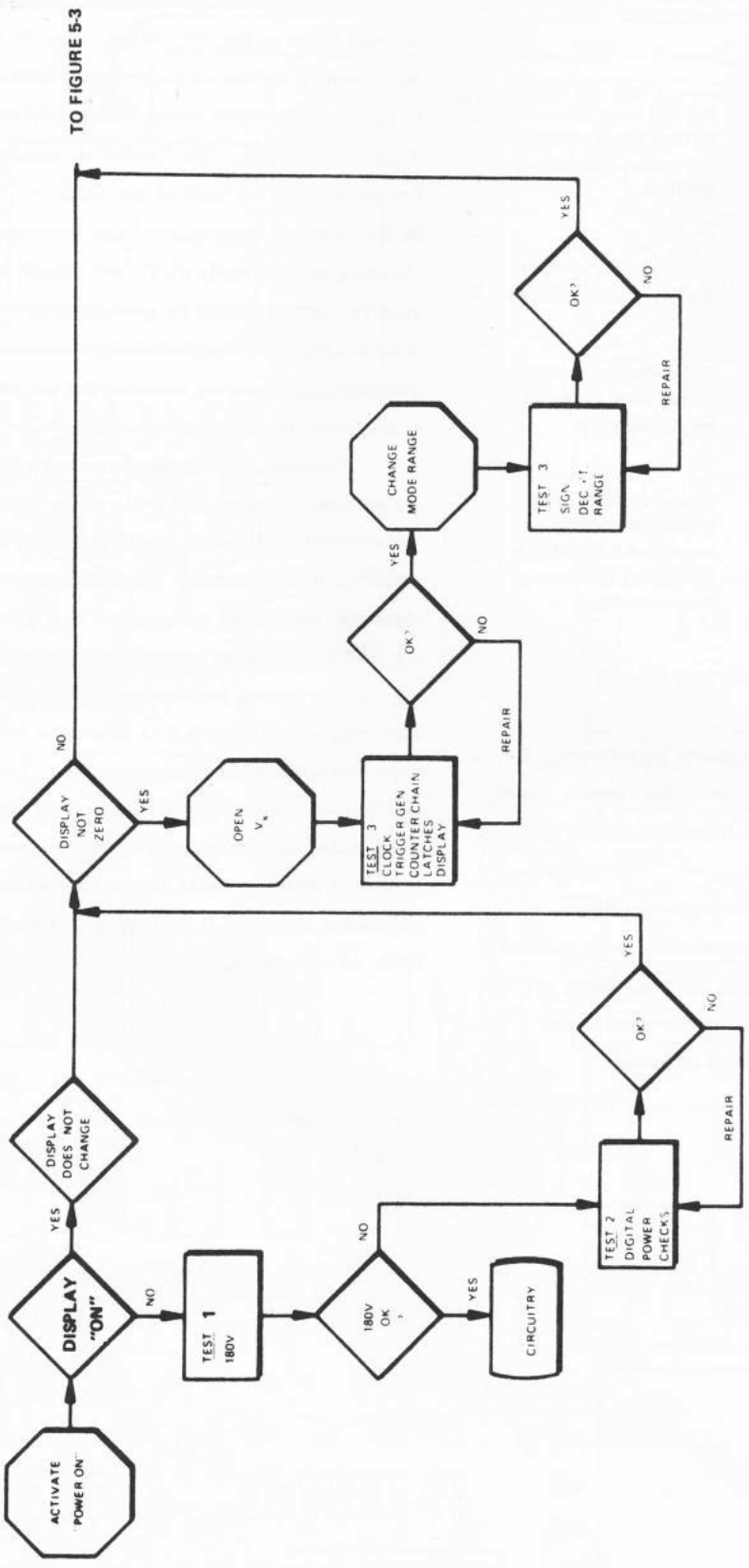


Figure 5-2 Trouble Shooting Sequence. Tests 1, 2, and 3.

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Tests 1,2 and 3. See Figure 5-2.

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
1	Activate Power ON	DC Volts	E18: E19	+180V 198	± 10%	Power Supply Drawing SH5	DISPLAY Supply
2.1		DC Volts	E17: E19	+20V 19.1	18 to 22	Power Supply Drawing SH5	Relay Supply
2.2		DC Volts	E16: E19	+5V 4.67	4.5 to 5.5	Power Supply Drawing SH5	Digital Logic Supply
3	Open Vx Short Z1A pin 1 to GND						$\phi1$, $\phi2$, $\phi3$; No EOC, 120000 Count
3.1		Frequency Count	Z2A pin 1	1 MHz	± 1 kHz	Clock Circuit Drawing SH1	Clock
3.2		Waveform Analysis	Z2A-2	Amp >+2.5V Rep Rate ~3 pps	-0, 2.5 - 5.5	Trigger Gen Drawing SH1	Trigger Generator
3.3		Frequency	Z4 through Z8 and Z2 Pin 14 on each	1 MHz to 10 Hz (by 10) and 5 Hz	± 0.1%	Decade Counter Drawing SH1	Decade Counter Chain and Binary Counter
3.4		Logic Levels	Rear Conn DATA OUT Tabs	BCD for 120000		Latches Z9–Z13 Drawing	Latch
3.5		Display	Front Panel	120000, Blinking "1"		Display Drawing SH1	Display
3.6	DC V Mode	Sign	Front Panel Display	"+"		Sign Circuit T5 Z14, etc. Drawing SH1	Sign Circuit
3.7	AC V Mode	Sign	Display	No Sign		Sign Circuit T5 Z14, etc. Drawing SH1	Sign Circuit
3.8	kΩ Mode	Sign	Display	No Sign		Sign Circuit T5 Z14, etc. Drawing SH1	Sign Circuit
3.9	No Range Activate	Impedance	Rear Panel Range Tabs 6, 11, T, B, H	Open Ckt		Auto Range Drawing SH2	x 10^{-3} Range
3.10	a) x .1 b) x 1 c) x 10 d) x 100 e) x 1K f) x 10K	Display, Relays	Display, Range Relays	Correct Decimal Point Relay per Table		Relay Table Drawing SH2	Decimal Point Display Relay Operation
3.11	Auto Range a) DC V b) kΩ c) Jump Z2 pin 8 to Z3 pin 8	Decimal Point Decimal Point Value	Display	Decimal Point a) x 1K b) x 10K c) "0" x .1		Auto Ranging Drawing SH2	Auto Range

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Tests 4 and 5. See Figure 5-3

TEST NO	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
4.1		DC Volts	Z33 pin 8	+15V	±1V Ripple 1mV RMS	Power Supply Drawing SH5	Analog Power Supply
4.2		DC Volts	Z33 pin 4	−15V	±1V Ripple 1mV RMS	Power Supply Drawing SH5	Analog Power Supply
4.3		DC Volts	Z31A pin 7	−5V	±1V Noise 25 μV	Power Supply Drawing SH5	Analog Power Supply
5	Short E62 to J21 Jumper Z32A pin 6 to pin 7						Zero Input to A/D No EOC at End of Phase 3
5.1		Waveform	Z31A pin 5	Positive Pulses 100 msec		A/D Conv. Drawing SH4	Trigger & 10 Carry Start and End Phase 2
5.2	Select x.1 DCV	DC Volts	Amp A1 pin 5	200 mV	+0, −	A/D Conv. Drawing SH4	A1 Operation OFF SET
5.3		DC Volts	Junction R96, R99	0V	±1V	A/D Conv. Drawing SH4	A2 and Clamp Circuits

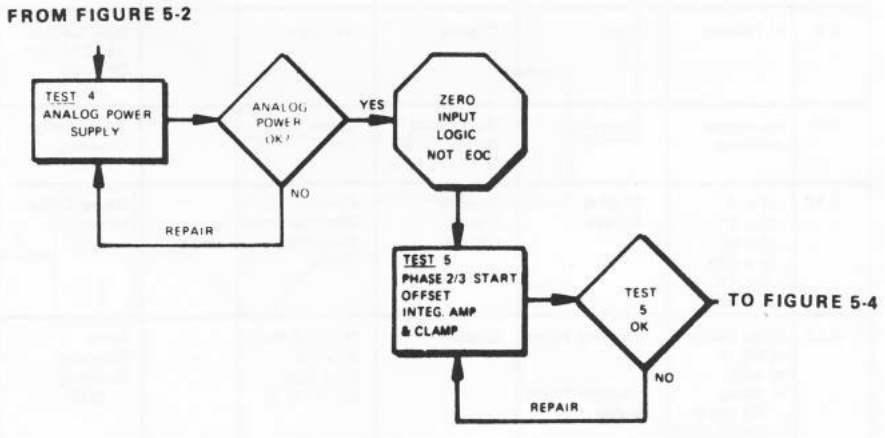


Figure 5-3 Trouble Shooting Sequence Tests 4 and 5

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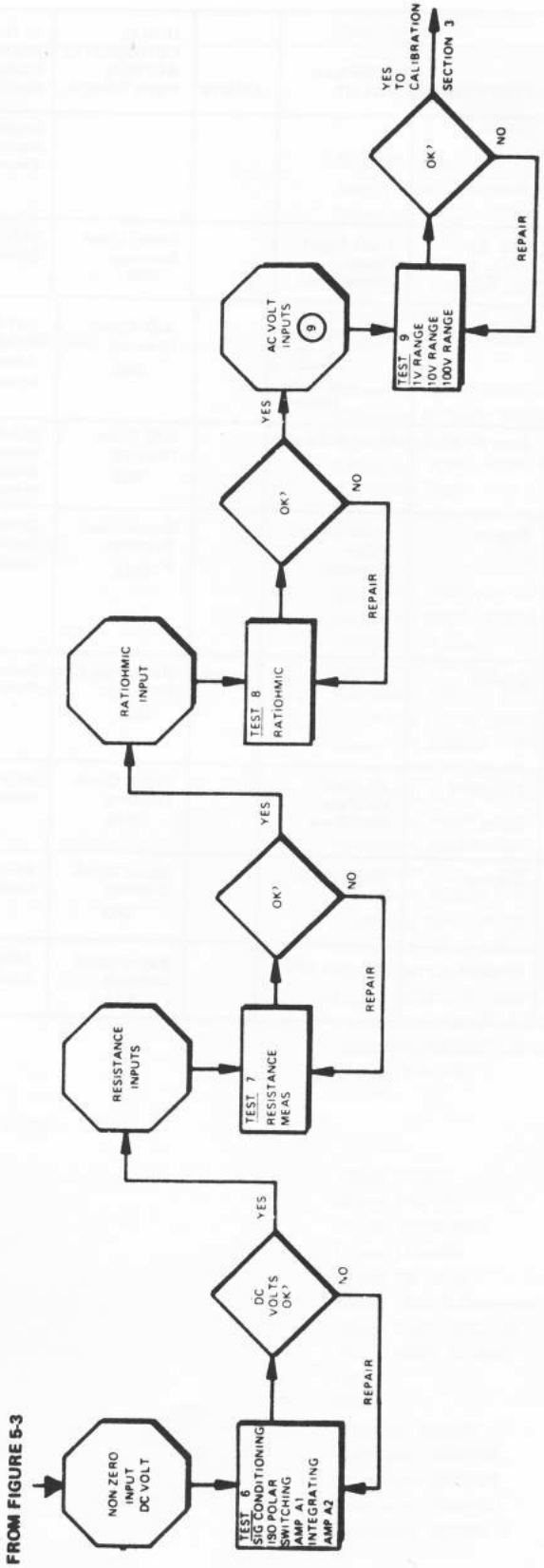
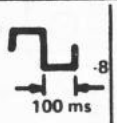


Figure 5-4 Trouble Shooting Sequence. Tests 6,7,and 8

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Tests 6, 7, 8, and 9. See Figure 5-4.

TEST NO.	SET-UP	PARAMETER	TEST POINTS	NOMINAL VALUE	LIMITS	IF N.G., CORRECTIVE ACTION REFERENCE	IF O.K., PROPERLY FUNCTIONING SUBSYSTEM
6	Remove Short Connect Varying Vx DCV ±11V						Supply Varying Input Voltage Values
6.1	DCV Mode Range x 10	DC Volts	E35: E6 or J2	Track Input Values (Scope Ind.)		Signal Cond. Drawing SH4	DCV Signal Conditioning
6.2	+10V to Vx Sync. Scope to Z31 pin 5	Waveform	Amp A1 pin 5	+8  -8 100 ms		A/D Conv. Drawing SH4	ISO-POLAR Switch Module, Amps A1, EOC Integrating A2
6.3	Reverse Input Vx Polarity	Waveform	Amp A1 pin 5	Reverse Polarity		A/D Conv. Drawing SH4	ISO-POLAR Switch Module, Amps A1, EOC Integrating A2
7	Connect for Resistance 2-Wire Connect Resistances in each Range kΩ Mode	Resistance Measurement	Display	Track Input Value Changes		Signal Cond. Drawing 3! SH3	Ohms Converter Signal Conditioning
8	Apply +10V to Both Vx and Rx RATIO Mode 10V Range	Display Count	Display	10.0000	± .010	Ratiohmic Ckt Drawing SH3	Ratiohmic Function
9.1	ACV Mode Range x 1 Apply -1V 200 Hz	Waveform	Z26 pin 6 CR25, Cathode	1V RMS sin Wave Half-Wave		Signal Cond. Drawing SH3	ACV Signal Conditioning
9.2	x 10 Range Apply 10 VRMS 200 Hz	Display Count	Display	Approx. 10		Signal Cond. Drawing SH3	ACV Signal Conditioning
9.3	x 100 Range	Display Count	Display	Approx. 100		Signal Cond. Drawing SH3	ACV Signal Conditioning

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MAIN ASSEMBLY

Symbol	Description	Part No.
A1	Amp 1B Assy	PL30-1052(B37-1021)
A2	Amp 2 Assy, Selected per Dwg 32-3006	PL30-1001 (B37-1001)
C1, 18, 19, 39 thru 43	Capacitor 6.8μF, 20V	23-441005
C39 thru C43		
C2, C75	Capacitor 270pF, DM15	23-311022
C3, 5, 58	Capacitor 1000pF, DM15	23-111005
C4	Capacitor 1500pF, DM15	23-311038
C6, 24, 36, 44, 48, 205, 206	Capacitor 15μF, 10V	23-441003
C7	Capacitor 30pF, DM15	23-111004
C8	Capacitor 0.15μF, 600V, Poly C	23-510021
C9, 27	Capacitor 2-9pF	23-810006
C10	Capacitor 10pF, 500V DM15	23-311001
C11	Capacitor 10pF, 1KV, 10%, Selected	23-110003-A
C12, 25, 26	Capacitor 1μF, 50V Poly C	23-510001
C20, 23	Capacitor, 5pF (Optional FSV)	23-111003
C21, 22	Capacitor 82pF, DM15	23-111008
C28	Capacitor 6-25pF	23-810007
C30	Capacitor 15-60pF	23-810005
C29	Capacitor 120pF, DM15	23-310025
C31	Capacitor DM15 (select)	FSV
C32	Capacitor 1200pF, DM15	23-311037
C33	Capacitor .015μF, 2%, Poly Sty	23-550101
C34	Capacitor 2μF, Poly Carb	23-510002
C35	Capacitor .68μF, 10%, 50V	23-550104
C37, 203	Capacitor 220μF, 35V	23-620006
C38	Capacitor 330μF, 50V	23-620007
C45	Capacitor .018μF, 10%, 50V	23-550105
C46, 50	Capacitor 5pF, DM15	23-111003
C47	Capacitor .01μF, 150V, Disk	23-111006
C49	Capacitor 12pF, DM15	23-111002
C52	Capacitor 4.7μF, 315V, Alum	23-620004
C204	Capacitor 2500μF, 16V	23-620005
C300	Capacitor 3000pF, 30V	23-550103
CR2, 3, 4, 5	Diode 1N4148	24-110001
CR7 thru CR20		
CR22 thru CR24,27,28		
CR29, 36, 44		
CR6	Diode 1N702	24-120002
CR21	Diode 1N270	24-140270
CR25, 26	Diode, 5082-2800	24-110004
CR30 thru CR34	Diode 1N4004	24-104004
CR35, 213	Diode 1N752A	24-120075
CR37	Diode 1N829 Selected	24-130004
CR38	Diode 180V, 5%, 1W	24-121008
CR201, 202, 203	Diode 400V Bridge	24-100021
K1, K2	Relay	25-171002
K3 thru K6	Relay	25-171003
L1	Inductor 100μH	25-100024
Q1, 2, Q4 thru Q9	Transistor 2N4410	24-234410
Q3	Transistor 2N3904	24-233904
Q10	Transistor 2N3440	24-203440
Q16	Transistor MPS6519	24-246519
Q18, 20	Transistor 40319	24-220319

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MAIN ASSEMBLY (Cont.)

Symbol	Description	Part No.
Q19	Transistor 40314	24-220314
Q22, 23	Transistor FET (Blue Dot)	24-48-1014-02
Q24, 25	Transistor FET (Yel Dot)	24-48-1014-05
Q27, 29, 30	Transistor FET (Orn Dot)	24-48-1014-10
Q40	Transistor 2N6027	24-206027
Q201	Transistor 2N5296	24-225296
R1, 8, 9, 10 R24 thru R28, 98, 109, 118, 121	Resistor 2.2K 5%, 1/4W, C. C.	22-022229
R2 thru R7, R122	Resistor 510K, 5%, 1/4W, C. C.	22-025149
R11	Resistor 11K, 5%, 1/4W, C. C.	22-021139
R12	Resistor 22K, 5%, 1/4W, C. C.	22-022239
R13, 17, 100, 101	Resistor 680Ω, 5%, 1/4W, C. C.	22-026819
R14, 18, 20, 22	Resistor 1.5K 5%, 1/4W, C. C.	22-021529
R15, 92	Resistor 33K 5%, 1/4W, C. C.	22-023339
R16	Resistor 100Ω, 5%, 1/4W, C. C.	22-021019-C
R19, 21, 23, 107	Resistor 3.3K, 5%, 1/4W, C. C.	22-023329
R29	Resistor Set Item 1 (6.429K)*	22-38-1006
R30, 38, 45, 300	Trimmer 25K	22-666253
R31	Resistor 162K, 1%, RN60C	22-371623
R32, 75, 87	Trimmer 250Ω	22-666251
R33	Resistor Set Item 2 (61.875K)*	22-38-1006
R34, 73, 78	Trimmer 2.5K	22-666252
R35	Resistor Set Item 3 (618.75K)*	22-38-1006
R36, 43, 51	Trimmer 500Ω	22-666501
R37, 52	Resistor Set Item 1 (89.75K, 0.1%)*	22-38-1007-3
R39	Resistor 6.19M, 0.1% RN65E	22-433000
R40, 53	Resistor Set Item 2 (10K, 0.1%)*	22-38-1007-3
R42	Resistor Set Item 1 (9.9M, 0.1%)*	22-38-1008-2
R44	Resistor Set Item 2 (99.75K, 0.1%)*	22-38-1008-2
R46, 86	Trimmer, 100Ω	22-666101
R47, 48, 96	Resistor 15K, 1%, RN55D	22-331502
R49, 97, 110, 119	Resistor 1K%, 1/4W, C. C.	22-021029-C
R50	Resistor 261K, 1%, RN60D	22-362613
R54	Resistor Set Item 1 (1 Meg)*	22-38-1008-1
R131, 132	Resistor 10Ω,5%, 1/8W, C.C.	22-011009
R58	Resistor 8.2M, 5%, 1/4W. C. C.	22-028259
R59, 83	Trimmer 100K	22-666104
R60, 95	Resistor 150K, 1%, RN55D	22-331503
R61	Resistor Set Item 6, (1.69K)*	22-38-1008-1
R62, 63, 74	Resistor Set Item 4 (10K)*	22-38-1008-1
R64	Resistor 100Ω 1%, RN60D	22-361000
R65, 66	Resistor Set Item 7 (2.49K)*	22-38-1008-1
R67	Resistor Set Item 8 (301K)*	22-38-1008-1
R68	Resistor Set Item 9 (178K)*	22-38-1008-1
R69	Trimmer 5K	22-666502
R70, 79	Resistor 100K, 5%, 1/4, C. C.	22-021049
R71	Resistor Set Item 2 (1 Meg)*	22-38-1008-1
R72	Resistor Set Item 3 (110K)*	22-38-1008-1
R76	Resistor Set Item 5 (1.1K)*	22-38-1008-1
R77, 106	Resistor 10K, 1%, RN55C	22-341002
R80	Resistor 47M 5%, 1/4W. C. C.	22-024769
R81	Resistor Set Item 2 (10.096K)*	22-38-1007-1
R82	Resistor 1M, 1%, RN65C	22-392001
R84	Resistor Set Item 1 (42K)*	22-38-1007-1
R85	Resistor Set Item 4 (37.95K)*	22-38-1007-1

*Must be ordered as part of designated set.

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MAIN ASSEMBLY (Cont.)

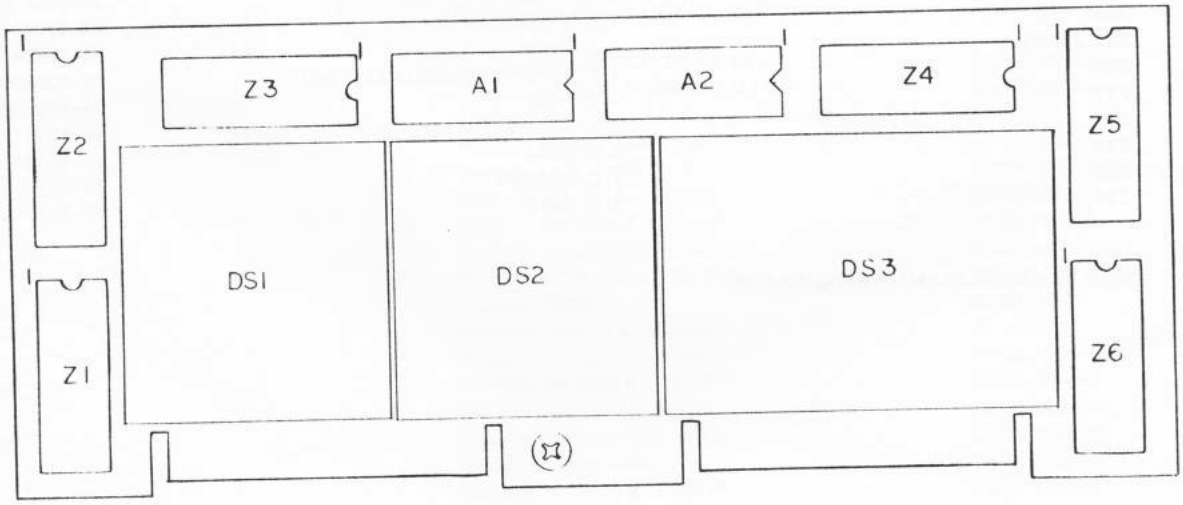
Symbol	Description	Part No.
R88	Resistor RN55E	FSV
R89	Resistor Set Item 3 (10K)*	22-38-1007-1
R90	Resistor Set Item 2 (10K, 0.01%)*	22-38-1007-2
R91	Resistor Set Item 1 (52K, 0.01%)*	22-38-1007-2
R99	Resistor 3.01K, 1%, RN55D	22-333011
R102	Resistor 1.1K, 1% RN60C	22-371101
R103	Resistor 8.66K, 1%, RN55C	22-348661
R104	Resistor 10.5K, 1%, RN55D	22-331052
R105	Resistor 6.19K 1%, RN55C	22-346191
R108	Resistor 100Ω, 5%, 1/2W. C. C.	22-031019
R111	Resistor 10K 5%, 1/4W. C. C.	22-021039-C
R114	Resistor 47K, 10%, 1/4W. C. C.	22-024739
R120	Resistor 1M 5% 1/4W. C. C.	22-021059
R123	Resistor 47M, 5%, 1/4W. (Opt. FSV)	22-024769
R130	Resistor 3.6K, 5%, 1/4W. C. C.	22-023629
R201	Resistor 1K 5% 1/2W. C. C.	22-031029
R301	Resistor 82K 5% 1/4W. C. C.	22-028239
S1-S7	Switch	B38-1010
T1	Transformer	D36-1094
T2 thru T5	Transformer, Pulse	C36-1056
U1	Switch Module Assy	PL30-1003 (B37-1003)
Y1	Crystal 1MHZ	A38-1012
Z1, 28	I. C. 9937	24-469937
Z2, 20, 22, 31	I. C. 9094	24-469094
Z3, 21	I. C. 9949	24-469949
Z4 thru Z8	I.C. 7490	24-A07490
Z9 thru Z14	I. C. 7475	24-A07475
Z15	I. C. LF356	24-420356
Z16	I. C. 7715	24-427715
Z24, 26, 30	I. C. 9948	24-469948
Z25	I. C. Selected LM308 (A32-3009)	24-420308
Z27	I. C. 7445	24-A07445
Z29	I. C. Selected LM311	24-420311-01
Z32	I. C. 9962	24-469962
Z33	I. C. N5558V	24-405558
Z34	I. C. 7407	24-A07407

*Must be ordered as part of designated set.

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DISPLAY ASSEMBLY

Symbol	Description	Part No.
A1	Res. Network, 2.2K, 14-Pin DIP	22-701002
A2	Res. Network, 15K, 14-Pin DIP	22-701000
DS1	Display	25-210351
DS2	Display	25-210352
DS3	Display	25-210353
Z1 thru Z6	I. C. DM8880	24-A08880



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Chapter 6

REFERENCE SCHEMATICS

Figure 6-1 Signal Conditioning Schematic Dwg 35-1027 Sheet 3 (SH3)

Figure 6-2 A/D Converter Schematic Dwg 35-1027 Sheet 4 (SH4)

Figure 6-3 Counter and Display Schematic Dwg 35 1027 Sheet 1 (SH1)

Figure 6-4 Ranging Schematic Dwg 35-1027 Sheet 2 (SH2)

Figure 6-5 Power Supply Schematic Dwg 35-1027 Sheet 5 (SH5)

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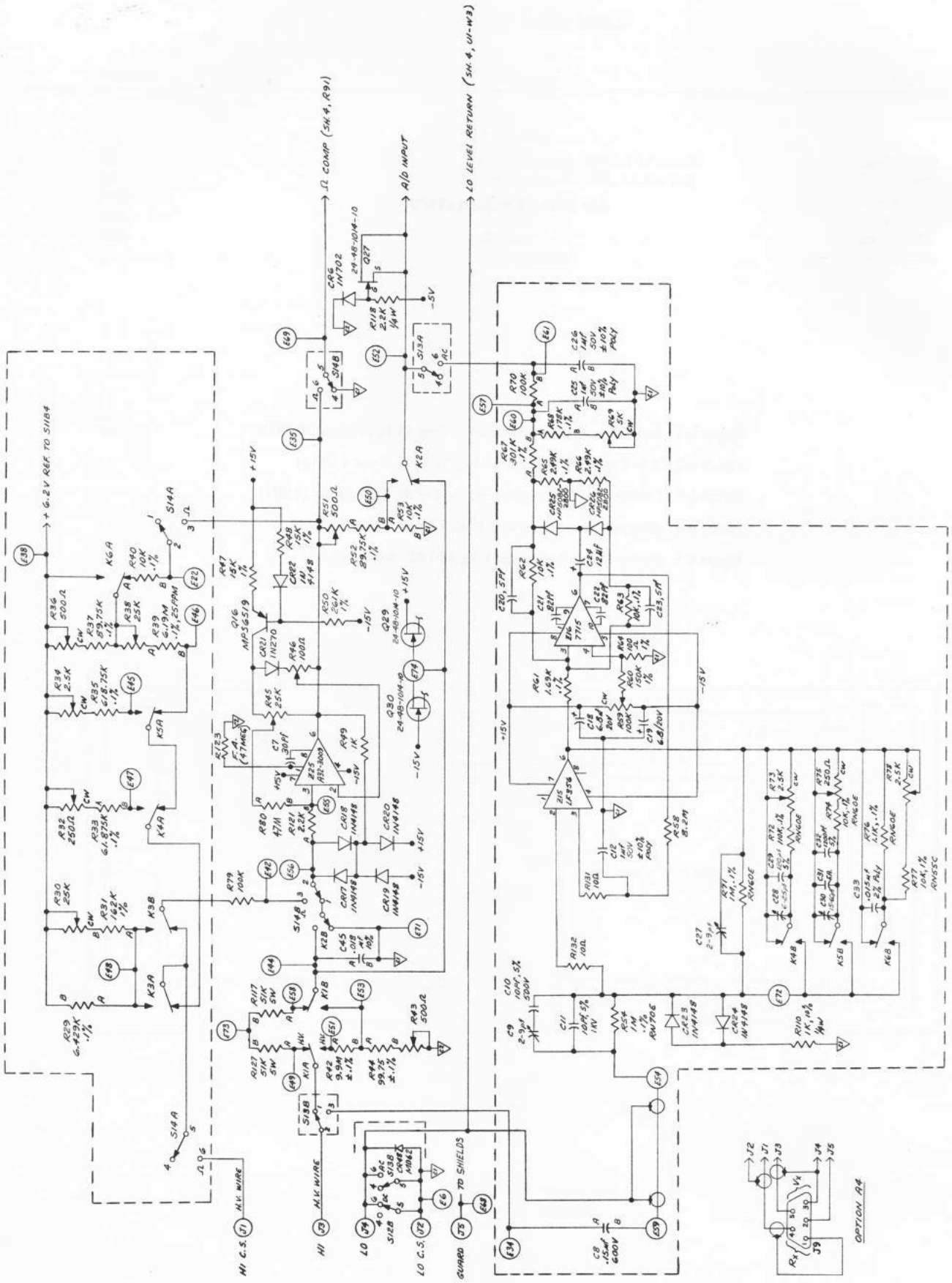


Figure 6-1 Signal Conditioning Schematic Dwg 35-1027 Sheet 3

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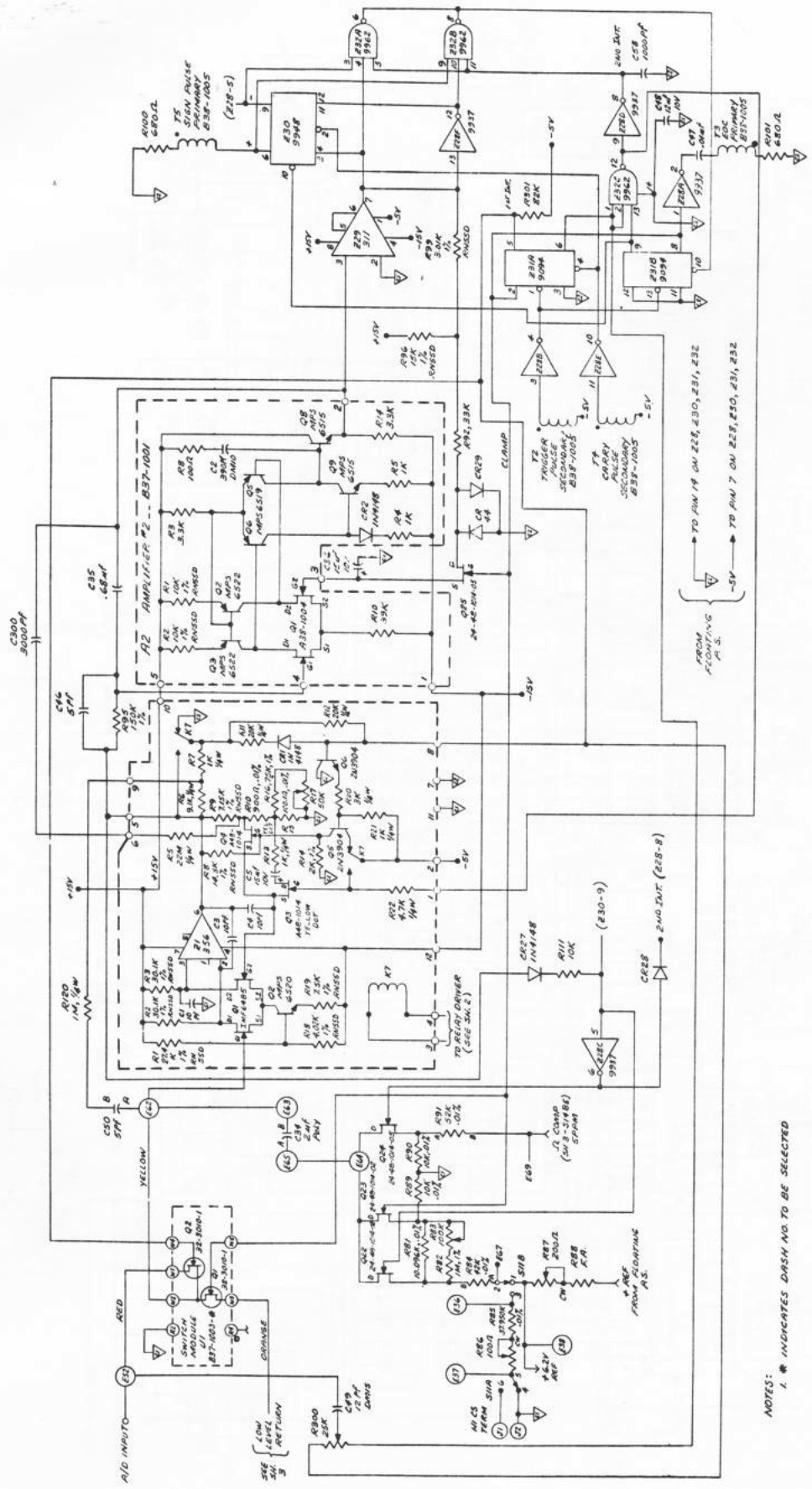


Figure 6-2 A/D Converter Schematic Dwg 35-1027 Sheet 4 (SH4)

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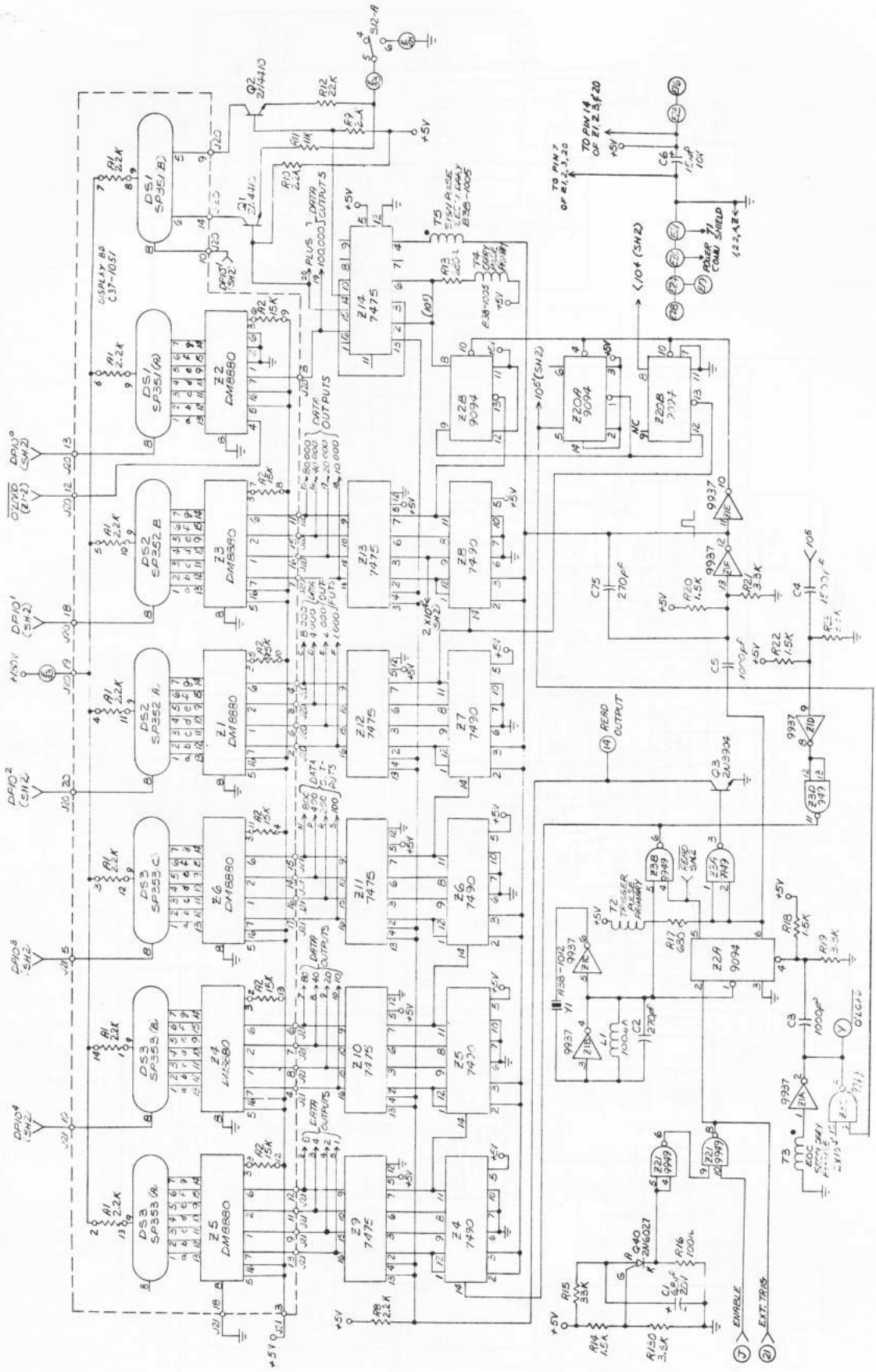


Figure 6-3 Counter and Display Schematic Dwg 35-1027 Sheet 1 (SH1)

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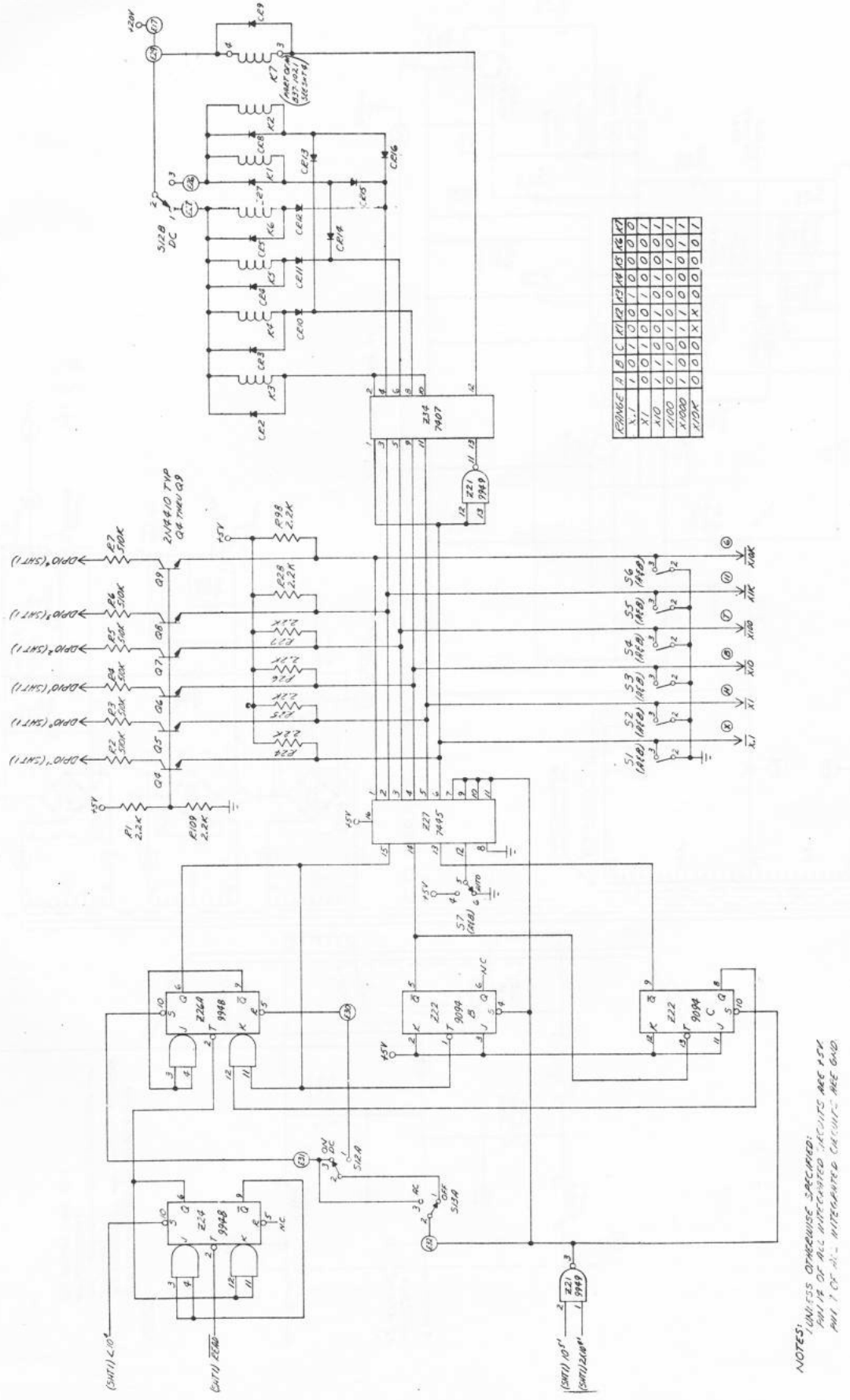


Figure 6-4 Ranging Schematic Dwg 35-1027 Sheet 2 (SH2)

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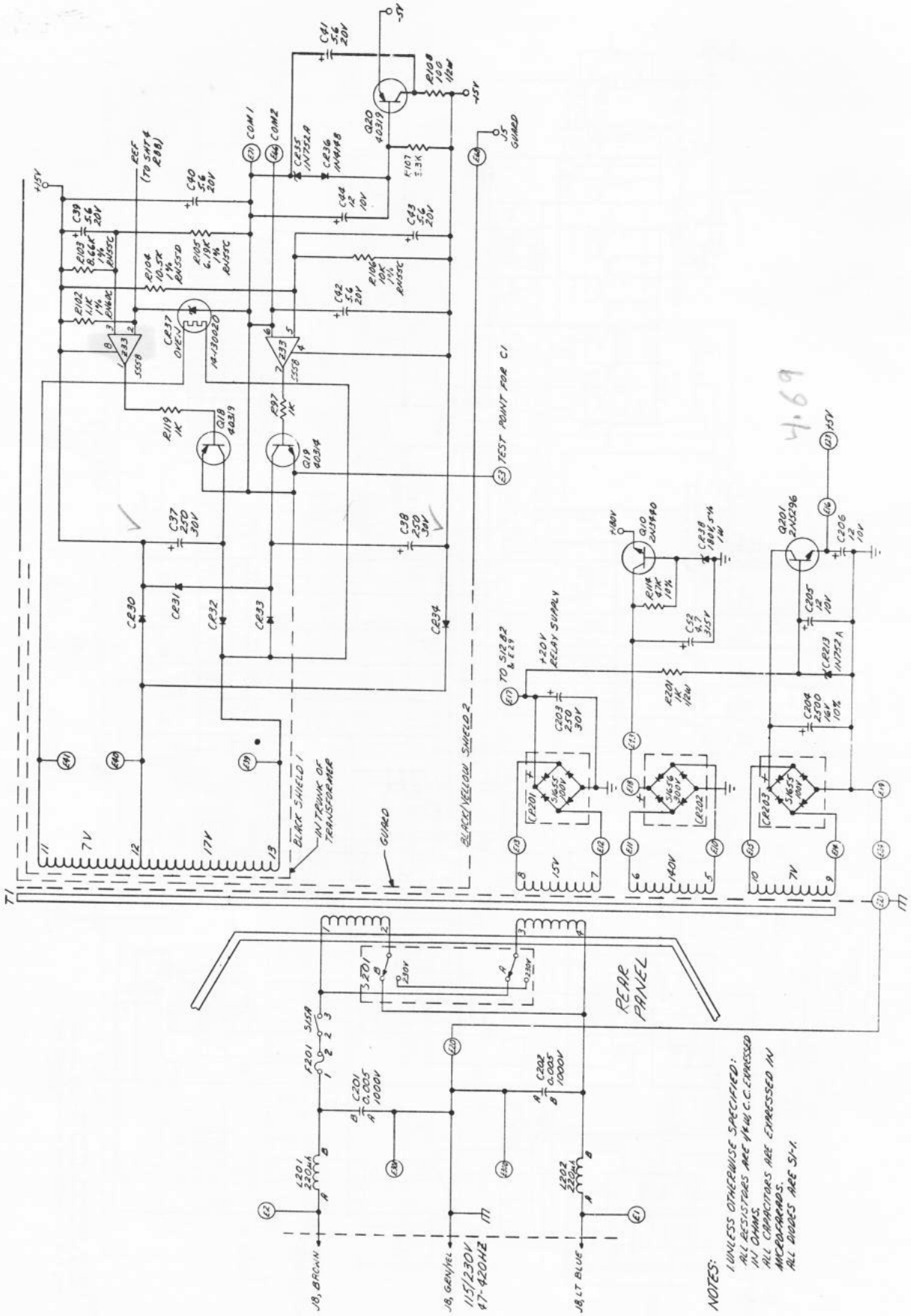


Figure 6-5 Power Supply Schematic Dwg 35-1027 Sheet 5 (SH5)

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